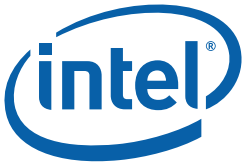

VR12 / IMVP7 Pulse Width Modulation (PWM) Specification

December 2009

Revision 1.4

Intel Confidential

Document Number: 397113

Contents

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Revision History

Document Number	Revision Number	Description	Revision Date
23812	0.8	• Initial release.	July 2007
	1.0	• Clarified required, optional platform programming • Clarified PMBUS support and Gamer Offset • Added market segment summary table and added single phase VR options • Clarified OCP and OVP protection schemes • Added PMBUS support section • Added clarification and figure on VR_Settled function • Updated VID table to show market segment requirements • Bounded slew rate fast and slow with minimum/maximum rates in each condition per Sandy Bridge silicon request.	November 2007
397113	1.1	• Added address table 3 • 2.2 added 6 & 8 phase options • 4.1 enable toggle > 10 ms, reset • 3.7.4 ADC for memory VRs • Change Vboot from 0.85, 0.9, 0.95 to 0.9, 1.0, 1.1 Added 1.5V option for memory • Remote sense bias current <500uA • Frequency, updated to allow for variable frequency designs. • Dual PWMs, if fault occurs on 1 rail, shut down both rails. • Updated 4.2 UVLO with recommendation for driver to hold input low during UVLO conditions	June 2008
397113	1.2	• VID table, all values required all segments • Start up timing table, Ta< 4ms, Tc< 3 us • Updated Iout with accuracy spec and required for all server segment parts. • Clarify Alert# and Vboot function • SVID address disable with disabled output • PMBUS/SMBUS/I2C must support separate programmable addressing and defined minimum	March 2009

Document Number	Revision Number	Description	Revision Date
		command set • 8 phase support HPC Server, EE desktop • Added more details to the requirements table 2.5	
397113	1.3	• Digital IOUT required DT, SVR and optional for NB, detailed specs and averaging times. • Clean up typo's in 1.2 (IE change list did not match text for start up timing…) • Independent temp sensors on all turbo rails for DT & Mobility in market segment table and thermal monitoring section. RE-scaled temperature zone register and moved Therm_Alert and VR_Hot# bit assertion points, IE Therm_Alert is 1 zone lower than VR_Hot# assertion. • Added single output 2 phase for Entry DT segment, updated market segment enabling configurations • Updated market segment table • Clarified Alert function and test conditions. • Updated SVID bus paramaters for signal integrity • Single phase and dual single phase (1+0. 1+1) VRs require pin strap for Vboot programming • Updated PMBUS Margin high command for over clocking • Added ripple targets to power states • Added IBIS references in collateral section • Vout_max default = 1.5V	July 2009
397113	1.4	• Temp_Max optional IMVP, notebook segment. • Added power state exit latency requirements. • Added % units to Iout accuracy targets and added 6 phase iout accuracy targets. Mobility Iout is optional until 2013 product family.. • VR_Hot output buffer must meet table 3 & 4 requirements. • VR_Enable shut down, allow <1mS sink • Offset register it is optional to support > 1.52V for server memory VRs. Not required for IMVP7 notebook segment. • Deleted nomenclature voltage rail names, see platform power delivery design guides for more information. • Deleted ripple target table 9, 10 and all ripple speciation's will be in platform Electrical Design Specs (EDS). • DAC table revised to show total tolerance band is	December 2009

Document Number	Revision Number	Description	Revision Date
		critical. DAC set point is a recommendation. < 0.5V changed from 35 mV to 8mV as a target only. • TOB sections removed from PWM and placed in EDS per platform, market segment.	

1 Introduction

This document defines the PWM control chip features for the VRD12, VRM12 & IMVP7 CPU dc-dc converters used in Intel platforms. VR12/IMVP7 includes a Serial VID (SVID) interface; benefits of SVID can be seen in reduced number of required pins and 2 way communications between the CPU and VR. Future platform power delivery design guidelines will contain the actual platform implementations for IMVP7 or VRD12 in mobility, desktop and server market segments and takes precedent over targets shown in this document.

VR12/IMVP7 PWM incorporates all of the VR11 functions from prior VR guidelines plus the following enhancements:

- SerialVID interface
- Low bias differential remote sense (<500 uA)
- Platform Programmable register set
- VR_Settled function
- Various VR status, monitoring and reporting functions
- VR_Hot# is active low, eliminating on board interface circuits from VR11.x series

1.1 Methodology, definition changes from VR11.x

VID = Nominal voltage set point @ 0A and is centered in the Load Line TOB window. This is different from previous VR11.0, VR11.1, but matches with IMVP methodology of VID specifications.

Tolerance budget (TOB) calls out PWM IC tolerance paramaters + Ripple targets for the total platform VR tolerance budget. This clarifies different market segment requirements. The main TOB is from VR PWM silicon features (DAC, AVP,) and the ripple is a function platform design. This is different from VR11, VR11.1 method and similar to IMVP method of specifying TOB.

1.2 Terminology

Table 1. Feature Support Terminology

Categories	Description
REQUIRED	An essential feature of the design that must be supported to ensure correct processor and voltage regulator (VR) functionality. Required functions are critical to CPU functions.
EXPECTED	A feature to ensure correct VR and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs if the intended functionality is fully supported.
PROPOSED	A feature that adds optional functionality to the VR and, therefore, is included as a design target. May be specified or expanded by system OEMs.
OPTIONAL	A feature that is not required for processor operation; however, specific platforms or OEMs may request this feature or function.

Table 2. Glossary

Term	Description
#	This symbol after a signal name means an active low signal (logic low = asserted)
Active high	Signal is asserted when logic is high or 1
Active low	Signal is asserted when logic is low or zero volts
AVP	Adaptive voltage positioning or Load Line (LL)
BJT	Bi-Polar Junction Transistor
CFM	Cubic Feet per Minute (airflow).
CMRR	Common-mode rejection ratio.
CPU	Central Processing Unit, microprocessor
CRC-8	8-bit Cyclic Redundancy Check
DAC	Digital to Analog Converter.
DCR	Direct Current Resistance.

Term	Description
D-VID	Dynamic Voltage ID A mode of operation where the output voltage is dynamically changed by changing the VID bits.
D-VID code	Dynamic Voltage Identification code
EMI	Electro-Magnetic Interference
EMTS	Electrical, Mechanical and Thermal Specification
ESD	Electrostatic Discharge
ESL	Equivalent series inductance.
ESR	Equivalent series resistance.
FET	Field Effect Transistor.
FMB	Flexible Motherboard
FR4	A type of printed circuit board (PCB) material.
GND	Ground (return)
HFM	High Frequency Mode
HS	Heat Sink
HVM	High volume manufacturing.
I_{cc}	Load current.
IPF	Itanium® Processor Family
Itt	Bus current associated with the Vtt supply.
Imon	Analog output (0-900mV) proportinal to average output current
Iout	Digitized version of Imon signal, avaliable over SVID bus
LFM	Depending on context: Linear Feet per Minute (airflow) or Low Frequency Mode
Load Line	A mathematical model that describes voltage current relationship given system impedance (R_{LL}). The nominal load line equations is V_{cc} = VID – I*R_{LL}.
LV	Low Voltage
MLCC	Multi-layer ceramic capacitor.
Monotonically	A waveform changes from one level to another in a steady fashion, without intermediate re-tracement or oscillation.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.

Term	Description
MTBF	Mean Time Between Failures
OCP	Over current protection.
OTP	Over-Temperature Protection
OVP	Over Voltage Protection
PEC	Packet Error Correction
Processor Datasheet	A document that defines the processor electrical, mechanical, and thermal specifications.
PROCHOT#	Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator.
PSI#	Power Status Indicator
PWM	Pulse width modulation.
RDSon	MOSFET's Drain Source resistance
Ripple & Noise	The periodic or random signals measured over frequency band of 0 Hz to 20 MHz.
Rise Time	Rise time is defined as the time it takes any output voltage to rise from 10% to 90% of its nominal voltage.
R_{LL}	Load line impedance. Defined as the ratio: Voltage droop/current. This is the load line slope.
RMS	Root Mean Square
RSS	Root Sum Square. A method of adding statistical variables.
SerialVID	Serial Voltage Identification code
SFF	Small Form Factor
Slope	Load line resistance. See $R_{LL.}$
SVID	Serial Voltage Identification code
TDC	Thermal Design Current (continuous current while CPU is drawing thermal design power)
TDE	Thermal Design Envelope
TDP	Thermal Design Power

Term	Description
Thermal Monitor	A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature.
Tolerance budget (TOB)	Defines the voltage regulator's 3-σ voltage variation across temperature, manufacturing variation, and age factors. Must be ensured by design through component selection.
Transient Load Line or AC LL	Equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection and motherboard layout parasitics.
ULV	Ultra Low Voltage
UVLO	Under-voltage lock-out
Vcc	Processor core voltage defined in the processor datasheet.
VccP	IO termination voltage in notebook systems for front side bus typically 1.05 V
VCLK	SVID clock
Alert#	SVID Alert line or interrupt line
VDIO	SVID Data I/O
VID	Voltage Identification: A code supplied by the processor that determines the reference output voltage to be delivered to the processor Vcc lands. At zero amperes and the tolerance band at + 3-σ, VID is the voltage at the processor.
VR	Voltage Regulator
VRD	Voltage regulator down. A VR circuit resident on the motherboard.
VRM	Voltage regulator module that is socketed to a motherboard.
Vtt	IO termination voltage in desktop, server systems for front side bus or CSI link, typically 1.1 or 1.05 V
VR_HOT#	Active low output indicating the VR is over temperature and will be connected on the platform to force thermal throttle to reduce VR load.

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2 Market Segment Definitions

The VR12/IMVP7 will cover multiple market segments from notebooks, desktops to server products over a range of power levels from 10-50W, 100W, 130W +. PWM control ICs for all market segments will implement a common Serial VID interface and command protocol; basic feature sets (VID table, fault response, power states etc.).

All 3 market segment CPUs require multiple VID controlled voltage rails. For lower power, low phase count market segments, dual output PWM IC are desired. Where pin counts exceed low cost packaging constraints, individual PWM ICs can be made to meet the multi-rail requirements.

2.1 Mobility (Notebook, Netbook, Nettop) Market Segments

Sandy Bridge CPUs (2010)
1. Dual output 3 phase +1 phase PWM control IC with single SVID interface.
2. Dual output 2 phase +1 phase PWM control IC with single SVID interface
3. Dual output 1 phase +1 phase PWM control IC with single SVID interface
4. Single output 1 phase with SVID interface

Ivy Bridge CPUs (2012)
1. four configurations above for Sandy Bridge
2. Dual output 3 phase +2 phase PWM control IC with single SVID interface.
3. Dual output 2 phase +2 phase PWM control IC with single SVID interface

Note: Extreme edition notebooks with over clocking up to 1.52V can use standard IMVP7 PWM IC offset function over SVID in the 3+1 or 3+2 configurations. If the OEM extreme edition needs to support over 1.52V, the OEM should select a 4+1 desktop part with PMBUS interface.

2.2 Desktop Market Segment

1. Dual output 4(2-3-4) phase + 1 phase PWM control IC with single SVID interface
2. Dual 3 (2-3)+1 phase PWM IC with single SVID interface.
3. Dual 2+1 phase PWM IC with single SVID interface
4. Single output 2+0 phase PWM IC with SVID interface
5. Dual output 6(4-5-6) +1 phase with PMBUS options for high end and extreme edition 150A designs

6. 8 phase with external drivers and separate single Phase with integrated drivers for 180 – 200A extreme edition. Both VRs support PMBUS options. Both parts should support programming to any SVID address.

Note VR control ICs & drivers for memory VRs must support 5 V operations for S3 operation.

2.3 Server Market Segment

1. Dual 4(2-3-4) Phase + 1 Phase PWM control IC.
2. Dual output 6(4-5-6) phase +1 phase
3. 8 phase with external drivers and separate single phase with integrated drivers for High Performance Compute market segment ~ 200A Both VRs support PMBUS options. Both parts should support programming to any SVID address.
4. Dual output 2+1 phase PWM control IC for Memory applications (Vboot = 1.5V, +1 configured for DDR VTT tracking ½ of main rail)

An additional PMBUS port will be optional for some server market segment VR12 ICs.

Note VR control ICs & drivers for memory VRs must support 5 V operation for S3 operation.

2.4 For dual output VR, the following features are common:

- Addr_0 = multiphase, Addr_1 = single phase
- Dual rail PWM must have assignable addressing 0/1, 2/3, 4/5, 6/7…
- 1 enable pin for both rails
- 1 soft start ramp for both rails
- Dual VR_Ready outputs for power sequencing and rail fault indication
- Dual Independent feedback for both rails
- Dual Differential remote sense pairs on a dual rail PWM
- Dual temperature sensor inputs for each rail as required by segment
- Independent LL or AVP functions for both rails, including setting to zero
- Independent loop compensation both rails
- Independent Vboot on both rails
- Independent OVP, OCP functions
- Dual, independent Icc_MAX setting for each rail
- Dual, independent Iout digital reporting for each rail
- Single VR_Hot# output, either rail's thermal sensor can trip VR_Hot#
- Single Temp_max programming level
- If a rail is disabled or not stuffed on a dual PWM, SVID address should be disabled for that address and the PWM should reject commands to the disabled rail address.

2.5 Summary of market segment requirements (X=required, O=optional)

X=Required	Segment						NOTES
O=Optional	Server		Client/Desktop		Notebook		
Feature	Vcore - MULTI PH	LOGIC +1 PH	Vcore - MULTI PH	LOGIC +1 PH	Vcore - MULTI PH	LOGIC +1 PH	
VID 0.25-1.52	X	X	X	X	X	X	Full VID table required on both rails all segments.
Dynamic VID Fast	20mV/us	10mV/us	10mV/us	10mV/us	10mV/us	10mV/us	Minimum or Target slew rate
Dynamic VID Slow	5 mV/us	2.5mV/us	2.5 mV/us	2.5 mV/us	2.5 mV/us	2.5 mV/us	Minimum or Target slew rate
Decay Slew Rate	X	X	X	X	X	X	All segments support decay slew
Voltage Settled	X	X	X	X	X	X	See 3.7.4
VR Power States:							
PS0	X	X	X	X	X	X	Normal power mode
PS1	X	NA	X	NA	X	NA	Low power mode, (PSI#), single phase rail cannot phase shed)
PS2	X	X	X	X	X	X	Very low power mode, (PSI#+sleep)
PS3	O	O	O	O	X	X	Ultra low power state, VID < 0.5V
Temp max	X	X	X	X	O	O	OTP or pin programmed, Read by master, supports temperature zones & VRHOT trip point, common temp max for both rails
Temp sensor input	X	O (Vsa no turbo)	X	X	X	X	Rails that support turbo must have independent Temp sensor inputs (common Temp max, & VR_Hot# output)
DC LL or AVP	X	O (no LL on VSA)	X	X	X	X	OTP or pin programmed, If pin programmed, not read by master.
Enable	X	X	X	X	X	X	One enable for both rails on dual PWM
VR_Ready1	X	NA	X	NA	X	NA	Multiphase output Ready
VR_Ready2	NA	X	NA	X	NA	X	Single phase output Ready

X=Required	Segment						NOTES
O=Optional	Server		Client/Desktop		Notebook		
Feature	Vcore - MULTI PH	LOGIC +1 PH	Vcore - MULTI PH	LOGIC +1 PH	Vcore - MULTI PH	LOGIC +1 PH	
VR_Hot#	X	O (optional for VSA)	X	X	X	X	One Active Low Thermal Monitor output, common output for both rails, utilizing either temperature sensor input. (hottest rail will activate)
Address	X	X	X	X	O	O	OTP or pin programmed. Mobility segment only needs to support address 00h, 01h see 3.5 for more information
VR Data registers a value below required, optional X, O indicates default value from VR Vendor. For more information see SVID Protocol Specification							
Capability (06h)	X 2012/13 xxxx xxx1b 20/13 1xxx xxx1b		X 2012/13 xxxx xxxxb 2013 1xxx xxx1b		X 2012/13 xxxx xxxxb 2013 1xxx xxx1b		**Note 2013 mobile productw will require Iout support.**
Icc_MAX (21h)	X 00h	X 00h	X 00h	X 00h	X 00h	X 00h	**Must be programmed by platform designer to reflect capability of platform Default 00h indicates this value is not programmed and platform won't boot.**
Temp_Max (22h)	X	X	X	X	O	O	
Slew Rate Fast (24h)	X 14h	X 0Ah	X 0Ah	X 02h	X 0Ah	X 02h	Indicates slew rate fast capability of VR.
Slew Rate Slow (25h)	X 05h	X 02h	02hX	X	X 02h	X	Indicates slew rate slow capability of VR.
Vboot (26h)	X	X	X	X	X	X	OTP or pin programmed, not read by master
VR tolerance (27h)	O	O	O	O	O	O	Optional read by master
Current Calibration offset (28h)	O	O	O	O	O	O	OTP or pin programmed, not read by master, used in PWM only

X=Required	Segment						NOTES
O=Optional	Server		Client/Desktop		Notebook		
Feature	Vcore - MULTI PH	LOGIC +1 PH	Vcore - MULTI PH	LOGIC +1 PH	Vcore - MULTI PH	LOGIC +1 PH	
Temp Calibration Offset (29h)	O	O	O	O	O	O	OTP or pin programmed, not read by master, used in PWM only
Vout Max (30h)	X	X	X	X	X	X	programmed by master See protocol spec for more information
Voltage Offset (33h)	X 00h	X 00h	X 00h	X 00h	X 00h	X 00h	programmed by master
Iout (15h)	X	X (Optional for VSA)	X	X	2011, 2012 O 2013 X	2011, 2012 O 2013 X	Read by master **Note 2013 mobile products will require Iout support.**
VR Temperature (17h)) (ADC)	O	O	O	O	O	O	Read by master
Output Voltage (16h) (ADC)	O	O	O	O	O	O	Read by master
Output Power (18h) (ADC)	O	O	O	O	O	O	Read by master
Temperature zone (12h)	X 00h	X 00h	X 00h	X 00h	X 00h	X 00h	Read by master
Multi VR config (34h)	X 00h	X 00h	X 00h	X 01h	X 00h	X 01h	

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3 VID Operating Features

3.1 SerialVID (SVID) Overview

SerialVID bus is a three wire (clock, data, alert) serial source synchronous interface used to transfer power management information between a microprocessor and one or more voltage regulator control ICs. For more information see the *VR12/IMVP7 SVID Protocol* document.

The Serial VID bus is a high speed data bus and routing of the traces should be done to limit noise coupling from VR phase nodes or MOSFET switching nodes. Do not route traced under any switching MOSFET or phase node. The signals should be routed with the Alert# line in between the SVID clock and SVID data lines. The SVID lines must be ground referenced and the line width should be such that the 3 lines have a nominal 50 ohm impedance with the board stackup. The PCB vendor can help with line and spacing recommendations based on the distance to the ground plane to achieve a 50 ohm impedance.

3.2 SVID DC Electrical Parameters Required

The following table outlines the DC electrical parameters. Note that low voltage operation is essential to avoid level converters to/from the processor. It is optional on the VR controller to bring in the Vtt voltage from the platform as a reference voltage for improved signal integrity at the receiver.

See Table 3 for voltage definitions.

Table 3. VR DC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	CPU I/O Voltage (also know as Vccp for mobility)	0.95	1.05 to 1.0	1.08	V	5
V_{IL}	Input Low Voltage			0.45	V	1
V_{IH}	Input High Voltage	0.65			V	1
Vhyst	Hysteresis Voltage	0.05			V	
V_{OH}	Output High Voltage		V_{TT}		V	1
R_{ON}	Buffer On Resistance (data line, alert# line, VR_Hot# line)	4		13	Ω	2
I_L	Leakage Current	-100		100	µA	3
C_{PAD}	Pad Capacitance			4.0	pF	4

Symbol	Parameter	Min	Typ	Max	Units	Notes
Cpin	Pin capacitance			5.0	pF	

NOTES:

1. V_{TT} refers to instantaneous V_{TT}.
2. Measured at 0.31 * V_{TT}.
3. Vin between 0V and V_{TT}.
4. C_{PAD} includes die capacitance only. No package parasitics are included.
5. Sandy Bridge, 2010 generation is 1.05 V, Ivy Bridge generation 2013 targeting 1.0 V.

Figure 1 Definition of Vhysteresis in table 3

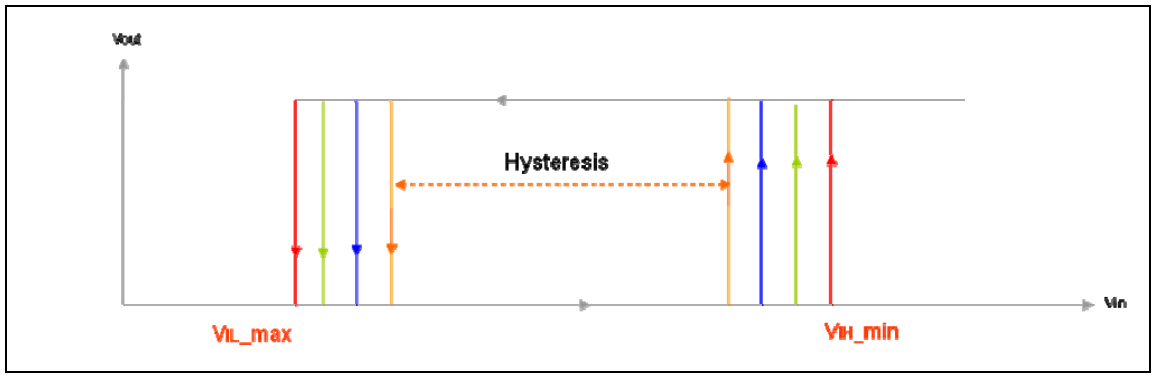


Table 4 VR AC Electrical parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
Vmax	VDS Max open drain buffer to accommodate ringing on bus	-1.0		3.3	volts	
SR Fall Data		1.2		4.08	V/ns	Load: Rpu=64.9Ω
SR Rise Data		1.1		3.62	V/ns	Load: Rpu=64.9Ω
SR Fall Alert/VR_Hot		1.25		4.2	V/ns	Load: Rpu=75Ω
SR Rise Alert/VR_Hot		1.15		3.33	V/ns	Load: Rpu=75Ω

SR is measured between between 0.735V and 0.315V (Vtt=1.05V). SR is measured at the output of the buffer Rpu is connected to Vtt as a load with no additional capacitance on the board. The slew rate is defined with VR buffer capacitance only..

3.3 VCLK Timing Parameters Required

The VCLK AC timing specification is an input specification for SerialVID devices. The VCLK output device must be designed to meet this specification at the clock receiver. The VCLK output device must have a platform design specification that guarantees that its VCLK output meets this AC timing specification at the VCLK receiver. See Figure 2.

The receiver clock should be edge triggered to detect the first falling edge of the clock when it restarts from an idle or high state.

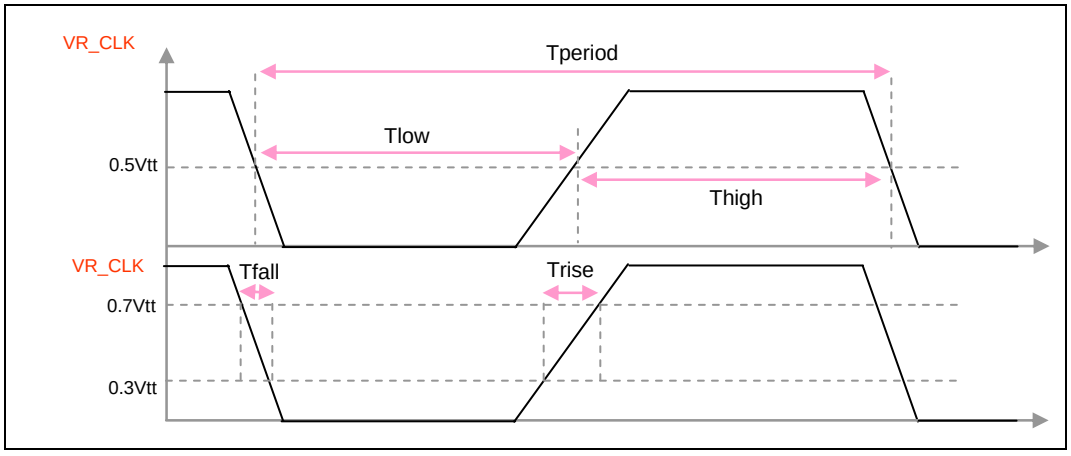
Table 5. VCLK AC Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes
	VCLK Frequency (Intel processor POR, different segments will use different Vclk freqeuncy)	13.3	25	26. 25	MHz	1, 4, 5
Tperiod	Absolute Min/Max VCLK Period	-1.25%		+1.25%	% of VCLK	1, 5
Thigh	VCLK High Time	-1.25%		+1.25%	% of 0.5 Tperiod	2, 5
Tlow	VCLK Low Time	-1.25%		+1.25%	% of 0.5 Tperiod	2, 5
Trise	VCLK Rise Time (@VR Pad)	0.25		2.5	ns	3
Tfall	VCLK Fall Time (@VR Pad)	0.25		2.5	ns	3
	Duty Cycle	49.375		50.625	%	1, 5

NOTES:

1. Period and duty cycle are measured with respect to 0.5 * VTT. See Figure 2
2. High time is measured with respect to 0.5 * V_{TT}. Low time is measured with respect to 0.3 * V_{TT}. See Figure 2.
3. Rise time is measured from 0.3 * V_{TT} to 0.7 * V_{TT}. Fall time is measured 0.7 * V_{TT} to 0.3 * V_{TT}. See Figure 2.
4. Many ICT test systems will stimulate Vclock 300 KHz - 1 MHz clock rate during platform manufacturing. The bus time out detection should be > 20 us to allow for detection of 2 valid clocks at 100 Khz during ICT board testing.
5. Tperiod, Thigh, Tlow and Duty Cycle variation as a result of internal CPU Clock logic only. Additional variation may be introduced as a result of the Clock MB topology (like different Rpu values or MB impedance).

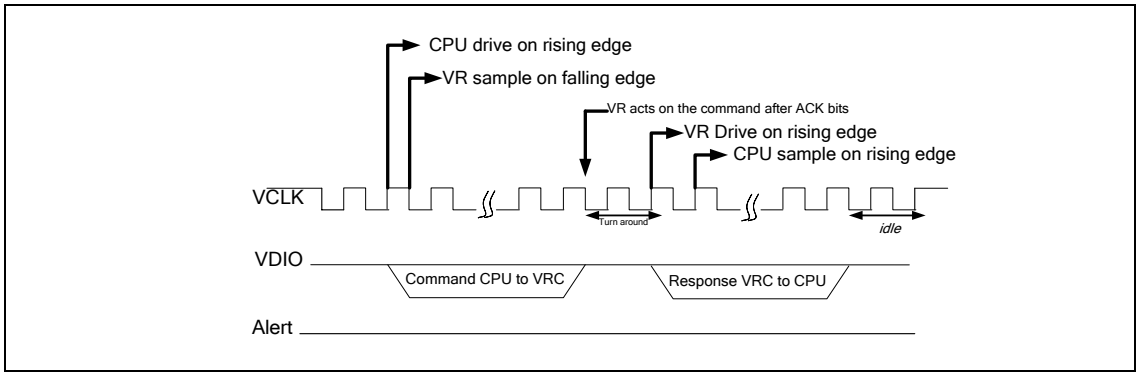
Figure 2. Measurement Points for VCLK High, Low, Rise and Fall Time, Tperiod



3.4 Data Sampling and Timing analysis

The clock to data delay or skew is different in the CPU or master vs. the VR control IC. To accommodate this and flight time and the process technology differences between the CPU and the VR, the data is sampled on different edges of the clock depending on the CPU or the VR driving data on the bus. See, Figure 4, Figure 5 and Figure 5.

Figure 3. Serial VID Bit Transfer



NOTES:

1. Sampling changes depending on CPU driving data or VR driving data on the bus

3.4.1 Silicon Validation, CRB, Electrical Validation Platforms Bus Timing all market segments

Tco_max_VR Clock to data delay = 8.3 ns

Tco_min VR clock to data delay = 4 ns

Tsu_VR - Setup time of signal VDIO at VR side = 7 ns

Thld_VR - hold time of signal VDIO at VR side = 14

Tco_max_CPU Clock to data delay @bump = 0.65 ns (measured vs Rpu of 50 Ohms without the channel, this value can change as a result of different Rpu and channel loads)

Tco_min_CPU Clock to data delay @bump= -0.65 ns (measured vs Rpu of 50 Ohms without the channel, this value can change as a result of different Rpu and channel loads)

Tsu_CPU - Setup time of signal VDIO at CPU side = 1 ns

Thld_CPU - hold time of signal VDIO at CPU side = 3 ns

3.4.2 OEM Production Platform Bus Timing All Market Segments

Tco_max_VR Clock to data delay = 12 ns

Tco_min VR clock to data delay = 4 ns

Tsu_VR - Setup time of signal VDIO at VR side = 7 ns

Thld_VR - hold time of signal VDIO at VR side = 14

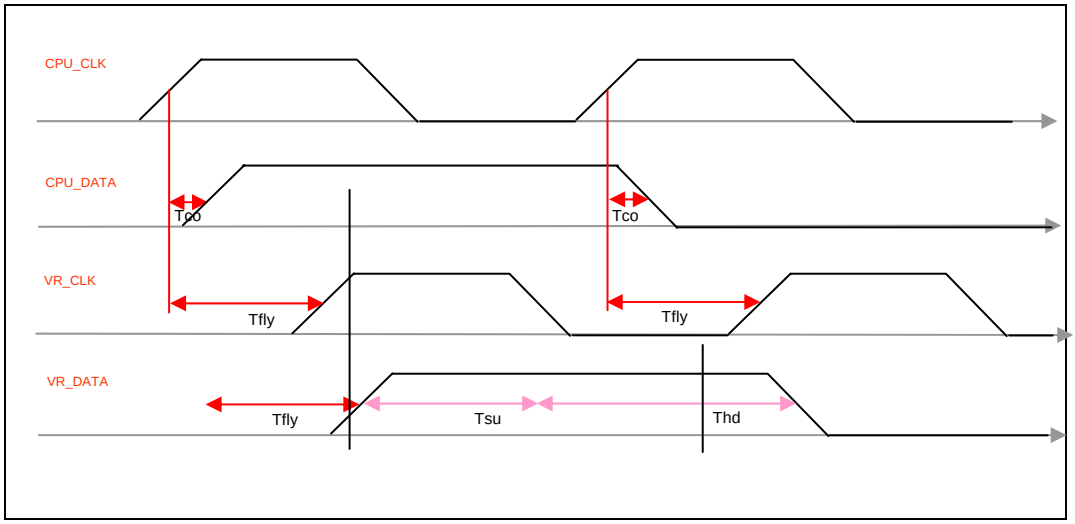
Tco_max_CPU Clock to data delay @bump = 0.65 ns (measured vs Rpu of 50 Ohms without the channel, this value can change as a result of different Rpu and channel loads)

Tco_min_CPU Clock to data delay @bump= -0.65 ns (measured vs Rpu of 50 Ohms without the channel, this value can change as a result of different Rpu and channel loads)

Tsu_CPU - Setup time of signal VDIO at CPU side = 1 ns

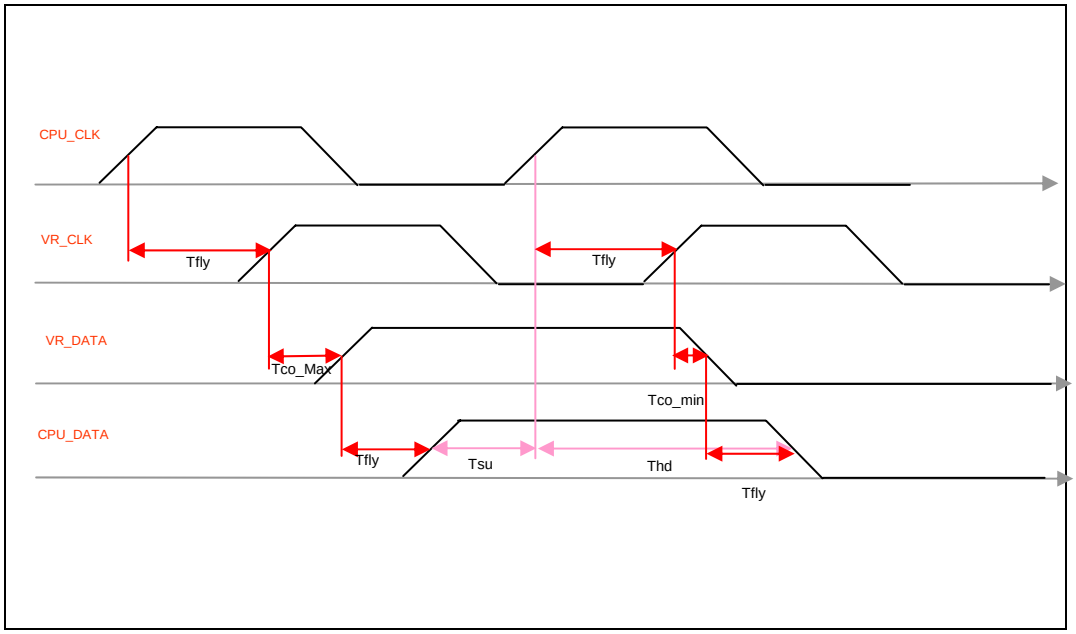
Thld_CPU - hold time of signal VDIO at CPU side = 3 ns

Figure 4. Clock and Data sample CPU driving timing definitions (all market segments)



NOTES:
1. All timings shown at VR or CPU pads, not at the pins.
2. Tfly = propagation time on the serial VID bus

Figure 5. Clock and Data sample VR driving timing definitions (all market segments)



NOTES:
1. All timings shown at VR or CPU pads, not at the pins.
2. Tfly = propagation time on Serial VID bus

3.5 Addressing required all segments

The data packet will contain a 4 bit addressing code for future platform flexibility. 15 address ranges are used for up to 15 distinct voltage rails. The final address, 1111b is used for all-call instructions. Controllers must respond to the all call FFh or FEh address command. Initial board products in 2010 plan to use the lower 8 address ranges (A0, A1, A2, A3, A4, A5), so initial VR12 control ICs only need to be able to resolve the lower 8 addresses. The VR vendor is responsible for determining the physical address assignment on their chip. Examples include: single pin with resistor divider to program the unique addresses, binary encoded 3 address pins, OTP programming etc.

VR Addressing is assigned on a per voltage rail basis. A dual VR controller will have 2 addresses, address a0=0000b and a1=0001b pre-assigned internally. The lowest order address will always be the high phase count rail. For platform flexibility the VR controller should include an address offset pin or pins to move these address from VR0/1 to VR2/3, VR4/5, VR 6/7 etc. Single rail controller should be programmable to any of the 15 address locations, VR0, VR1…VR14. See Table 6 for planned address usage.

If a power stage is not stuffed or used on a dual VR PWM, the SVID bus should be set to reject commands to that address. IE if the single phase is not stuffed or used, any commands to address 01h should be rejected.

Note: Mobility segment dual controllers only need to support address 0/1 pairs. Address offset is not required for mobility segment parts.

Table 6 Address definitions per socket

VR12 based platforms address usage

VR12 PWM Address, HEX		Servers Socket R	Servers Ararat-2	Desktop, socket R Server Socket B2	Desktop Socket H2	Mobility socket G2 rPGA, BGA
0	0	Vcore	Vuncore, cache	Vcore	Vcore	Vcore
0	1	VSA	+1 not used	VSA	VGFX	VGFX
0	2	VDDR1	Vcore1	VDDR1	VDDR?	
0	3	+1 not used	+1 not used			
0	4	VDDR2	Vcore2	VDDR2		
0	5	+1 not used	+1 not used			
0	6		Vcore3			
0	7		+1 not used			
0	8		Vcore4			
0	9		+1 not used			
0	A	-				
0	B	-	-			
0	C	-	-	-		
0	D					
0	E	All Call	All Call	All Call	All Call	All Call
0	F	All Call	All Call	All Call	All Call	All Call

Note: The VR All Call command functions on either address 0Eh or 0Fh

3.6 VID Table Required all segments

VR12/IMVP7 will have a 5 mV step size, linear VID table with one off code, 00h sets output to zero volts, not switching, no active pull down & de-asserts VR_Ready as a default state, as long as enable is asserted, the SVID bus is idle waiting on next

instruction. If the Multi_VR_config register is set to 01h, then the VR_Ready line will remain asserted when receiving a 00h VID code. See SVID protocol for more information.

- Nominal operating VID range is 0.6 to 1.35 V for 2010 products.
- Sleep states VID range < 0.5 V.
  While VID< 0.5V it is assumed the PWM is in DCM, hysteretic or bang-bang control with output ripple/regulation envelope relaxed to +-35mV. Output current reporting, load line or Adaptive Voltage Positioning tracking are not required for VID < 0.5V. The purpose of VID < 0.5 V is to maintain charge on bulk caps for quick resume back to operating voltage ranges.
- Extreme Edition over clocking platforms need optional DAC offset through the PMBUS, pin straps or other platform circuits (IE voltage divider on feedback voltage etc.) programming method. A DAC offset would shift the entire VID table up for platform designers who desire Vout> 1.52V.
- **DAC accuracy is a recommendation only.**
  Total tolerance band must be met, IE.RSS sum of DAC set point + current sense AVP droop accuracy. See applicable platform design guideline for total tolerance band requirements.

-

Table 7 VID range and power state support

VID Range	Required Power State Support
VID≥ 0.5 V	PS0, PS1, PS2, PS3
VID < 0.5 V	PS2, PS3

Table 8: VID Table

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
0	0	0	0	0	0	0	0	0	0	0.00000	NA	All
0	0	0	0	0	0	0	1	0	1	0.25000	+- 8 mV	Req. MBL, DT, Optional SVR
0	0	0	0	0	0	1	0	0	2	0.25500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	0	0	1	1	0	3	0.26000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	0	1	0	0	0	4	0.26500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	0	1	0	1	0	5	0.27000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	0	1	1	0	0	6	0.27500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	0	1	1	1	0	7	0.28000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	0	0	0	0	8	0.28500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	0	0	1	0	9	0.29000	+- 8 mV	Req. MBL, DT Optional SVR

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
0	0	0	0	1	0	1	0	0	A	0.29500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	0	1	1	0	B	0.30000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	1	0	0	0	C	0.30500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	1	0	1	0	D	0.31000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	1	1	0	0	E	0.31500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	0	1	1	1	1	0	F	0.32000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	0	0	0	1	0	0.32500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	0	0	1	1	1	0.33000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	0	1	0	1	2	0.33500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	0	1	1	1	3	0.34000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	1	0	0	1	4	0.34500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	1	0	1	1	5	0.35000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	1	1	0	1	6	0.35500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	0	1	1	1	1	7	0.36000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	0	0	0	1	8	0.36500	+- 8 mV	Req. MBL,

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
												DT Optional SVR
0	0	0	1	1	0	0	1	1	9	0.37000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	0	1	0	1	A	0.37500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	0	1	1	1	B	0.38000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	1	0	0	1	C	0.38500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	1	0	1	1	D	0.39000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	1	1	0	1	E	0.39500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	0	1	1	1	1	1	1	F	0.40000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	0	0	0	2	0	0.40500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	0	0	1	2	1	0.41000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	0	1	0	2	2	0.41500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	0	1	1	2	3	0.42000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	1	0	0	2	4	0.42500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	1	0	1	2	5	0.43000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	0	1	1	0	2	6	0.43500	+- 8 mV	Req. MBL, DT Optional

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
												SVR
0	0	1	0	0	1	1	1	2	7	0.44000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	0	0	0	2	8	0.44500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	0	0	1	2	9	0.45000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	0	1	0	2	A	0.45500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	0	1	1	2	B	0.46000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	1	0	0	2	C	0.46500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	1	0	1	2	D	0.47000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	1	1	0	2	E	0.47500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	0	1	1	1	1	2	F	0.48000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	1	0	0	0	0	3	0	0.48500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	1	0	0	0	1	3	1	0.49000	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	1	0	0	1	0	3	2	0.49500	+- 8 mV	Req. MBL, DT Optional SVR
0	0	1	1	0	0	1	1	3	3	0.50000	+- 8mV	All
0	0	1	1	0	1	0	0	3	4	0.50500	+- 8mV	All
0	0	1	1	0	1	0	1	3	5	0.51000	+- 8mV	All
0	0	1	1	0	1	1	0	3	6	0.51500	+- 8mV	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
0	0	1	1	0	1	1	1	3	7	0.52000	+- 8mV	All
0	0	1	1	1	0	0	0	3	8	0.52500	+- 8mV	All
0	0	1	1	1	0	0	1	3	9	0.53000	+- 8mV	All
0	0	1	1	1	0	1	0	3	A	0.53500	+- 8mV	All
0	0	1	1	1	0	1	1	3	B	0.54000	+- 8mV	All
0	0	1	1	1	1	0	0	3	C	0.54500	+- 8mV	All
0	0	1	1	1	1	0	1	3	D	0.55000	+- 8mV	All
0	0	1	1	1	1	1	0	3	E	0.55500	+- 8mV	All
0	0	1	1	1	1	1	1	3	F	0.56000	+- 8mV	All
0	1	0	0	0	0	0	0	4	0	0.56500	+- 8mV	All
0	1	0	0	0	0	0	1	4	1	0.57000	+- 8mV	All
0	1	0	0	0	0	1	0	4	2	0.57500	+- 8mV	All
0	1	0	0	0	0	1	1	4	3	0.58000	+- 8mV	All
0	1	0	0	0	1	0	0	4	4	0.58500	+- 8mV	All
0	1	0	0	0	1	0	1	4	5	0.59000	+- 8mV	All
0	1	0	0	0	1	1	0	4	6	0.59500	+- 8mV	All
0	1	0	0	0	1	1	1	4	7	0.60000	+- 8mV	All
0	1	0	0	1	0	0	0	4	8	0.60500	+- 8mV	All
0	1	0	0	1	0	0	1	4	9	0.61000	+- 8mV	All
0	1	0	0	1	0	1	0	4	A	0.61500	+- 8mV	All
0	1	0	0	1	0	1	1	4	B	0.62000	+- 8mV	All
0	1	0	0	1	1	0	0	4	C	0.62500	+- 8mV	All
0	1	0	0	1	1	0	1	4	D	0.63000	+- 8mV	All
0	1	0	0	1	1	1	0	4	E	0.63500	+- 8mV	All
0	1	0	0	1	1	1	1	4	F	0.64000	+- 8mV	All
0	1	0	1	0	0	0	0	5	0	0.64500	+- 8mV	All
0	1	0	1	0	0	0	1	5	1	0.65000	+- 8mV	All
0	1	0	1	0	0	1	0	5	2	0.65500	+- 8mV	All
0	1	0	1	0	0	1	1	5	3	0.66000	+- 8mV	All
0	1	0	1	0	1	0	0	5	4	0.66500	+- 8mV	All
0	1	0	1	0	1	0	1	5	5	0.67000	+- 8mV	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
0	1	0	1	0	1	1	0	5	6	0.67500	+- 8mV	All
0	1	0	1	0	1	1	1	5	7	0.68000	+- 8mV	All
0	1	0	1	1	0	0	0	5	8	0.68500	+- 8mV	All
0	1	0	1	1	0	0	1	5	9	0.69000	+- 8mV	All
0	1	0	1	1	0	1	0	5	A	0.69500	+- 8mV	All
0	1	0	1	1	0	1	1	5	B	0.70000	+- 8mV	All
0	1	0	1	1	1	0	0	5	C	0.70500	+- 8mV	All
0	1	0	1	1	1	0	1	5	D	0.71000	+- 8mV	All
0	1	0	1	1	1	1	0	5	E	0.71500	+- 8mV	All
0	1	0	1	1	1	1	1	5	F	0.72000	+- 8mV	All
0	1	1	0	0	0	0	0	6	0	0.72500	+- 8mV	All
0	1	1	0	0	0	0	1	6	1	0.73000	+- 8mV	All
0	1	1	0	0	0	1	0	6	2	0.73500	+- 8mV	All
0	1	1	0	0	0	1	1	6	3	0.74000	+- 8mV	All
0	1	1	0	0	1	0	0	6	4	0.74500	+- 8mV	All
0	1	1	0	0	1	0	1	6	5	0.75000	+- 8mV	All
0	1	1	0	0	1	1	0	6	6	0.75500	+- 8mV	All
0	1	1	0	0	1	1	1	6	7	0.76000	+- 8mV	All
0	1	1	0	1	0	0	0	6	8	0.76500	+- 8mV	All
0	1	1	0	1	0	0	1	6	9	0.77000	+- 8mV	All
0	1	1	0	1	0	1	0	6	A	0.77500	+- 8mV	All
0	1	1	0	1	0	1	1	6	B	0.78000	+- 8mV	All
0	1	1	0	1	1	0	0	6	C	0.78500	+- 8mV	All
0	1	1	0	1	1	0	1	6	D	0.79000	+- 8mV	All
0	1	1	0	1	1	1	0	6	E	0.79500	+- 8mV	All
0	1	1	0	1	1	1	1	6	F	0.80000	+- 5mV	All
0	1	1	1	0	0	0	0	7	0	0.80500	+- 5mV	All
0	1	1	1	0	0	0	1	7	1	0.81000	+- 5mV	All
0	1	1	1	0	0	1	0	7	2	0.81500	+- 5mV	All
0	1	1	1	0	0	1	1	7	3	0.82000	+- 5mV	All
0	1	1	1	0	1	0	0	7	4	0.82500	+- 5mV	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
0	1	1	1	0	1	0	1	7	5	0.83000	+- 5mV	All
0	1	1	1	0	1	1	0	7	6	0.83500	+- 5mV	All
0	1	1	1	0	1	1	1	7	7	0.84000	+- 5mV	All
0	1	1	1	1	0	0	0	7	8	0.84500	+- 5mV	All
0	1	1	1	1	0	0	1	7	9	0.85000	+- 5mV	All
0	1	1	1	1	0	1	0	7	A	0.85500	+- 5mV	All
0	1	1	1	1	0	1	1	7	B	0.86000	+- 5mV	All
0	1	1	1	1	1	0	0	7	C	0.86500	+- 5mV	All
0	1	1	1	1	1	0	1	7	D	0.87000	+- 5mV	All
0	1	1	1	1	1	1	0	7	E	0.87500	+- 5mV	All
0	1	1	1	1	1	1	1	7	F	0.88000	+- 5mV	All
1	0	0	0	0	0	0	0	8	0	0.88500	+- 5mV	All
1	0	0	0	0	0	0	1	8	1	0.89000	+- 5mV	All
1	0	0	0	0	0	1	0	8	2	0.89500	+- 5mV	All
1	0	0	0	0	0	1	1	8	3	0.90000	+- 5mV	All
1	0	0	0	0	1	0	0	8	4	0.90500	+- 5mV	All
1	0	0	0	0	1	0	1	8	5	0.91000	+- 5mV	All
1	0	0	0	0	1	1	0	8	6	0.91500	+- 5mV	All
1	0	0	0	0	1	1	1	8	7	0.92000	+- 5mV	All
1	0	0	0	1	0	0	0	8	8	0.92500	+- 5mV	All
1	0	0	0	1	0	0	1	8	9	0.93000	+- 5mV	All
1	0	0	0	1	0	1	0	8	A	0.93500	+- 5mV	All
1	0	0	0	1	0	1	1	8	B	0.94000	+- 5mV	All
1	0	0	0	1	1	0	0	8	C	0.94500	+- 5mV	All
1	0	0	0	1	1	0	1	8	D	0.95000	+- 5mV	All
1	0	0	0	1	1	1	0	8	E	0.95500	+- 5mV	All
1	0	0	0	1	1	1	1	8	F	0.96000	+- 5mV	All
1	0	0	1	0	0	0	0	9	0	0.96500	+- 5mV	All
1	0	0	1	0	0	0	1	9	1	0.97000	+- 5mV	All
1	0	0	1	0	0	1	0	9	2	0.97500	+- 5mV	All
1	0	0	1	0	0	1	1	9	3	0.98000	+- 5mV	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
1	0	0	1	0	1	0	0	9	4	0.98500	+- 5mV	All
1	0	0	1	0	1	0	1	9	5	0.99000	+- 5mV	All
1	0	0	1	0	1	1	0	9	6	0.99500	+- 5mV	All
1	0	0	1	0	1	1	1	9	7	1.00000	+- 0.5% VID	All
1	0	0	1	1	0	0	0	9	8	1.00500	+- 0.5% VID	All
1	0	0	1	1	0	0	1	9	9	1.01000	+- 0.5% VID	All
1	0	0	1	1	0	1	0	9	A	1.01500	+- 0.5% VID	All
1	0	0	1	1	0	1	1	9	B	1.02000	+- 0.5% VID	All
1	0	0	1	1	1	0	0	9	C	1.02500	+- 0.5% VID	All
1	0	0	1	1	1	0	1	9	D	1.03000	+- 0.5% VID	All
1	0	0	1	1	1	1	0	9	E	1.03500	+- 0.5% VID	All
1	0	0	1	1	1	1	1	9	F	1.04000	+- 0.5% VID	All
1	0	1	0	0	0	0	0	A	0	1.04500	+- 0.5% VID	All
1	0	1	0	0	0	0	1	A	1	1.05000	+- 0.5% VID	All
1	0	1	0	0	0	1	0	A	2	1.05500	+- 0.5% VID	All
1	0	1	0	0	0	1	1	A	3	1.06000	+- 0.5% VID	All
1	0	1	0	0	1	0	0	A	4	1.06500	+- 0.5% VID	All
1	0	1	0	0	1	0	1	A	5	1.07000	+- 0.5% VID	All
1	0	1	0	0	1	1	0	A	6	1.07500	+- 0.5% VID	All
1	0	1	0	0	1	1	1	A	7	1.08000	+- 0.5% VID	All
1	0	1	0	1	0	0	0	A	8	1.08500	+- 0.5% VID	All
1	0	1	0	1	0	0	1	A	9	1.09000	+- 0.5% VID	All
1	0	1	0	1	0	1	0	A	A	1.09500	+- 0.5% VID	All
1	0	1	0	1	0	1	1	A	B	1.10000	+- 0.5% VID	All
1	0	1	0	1	1	0	0	A	C	1.10500	+- 0.5% VID	All
1	0	1	0	1	1	0	1	A	D	1.11000	+- 0.5% VID	All
1	0	1	0	1	1	1	0	A	E	1.11500	+- 0.5% VID	All
1	0	1	0	1	1	1	1	A	F	1.12000	+- 0.5% VID	All
1	0	1	1	0	0	0	0	B	0	1.12500	+- 0.5% VID	All
1	0	1	1	0	0	0	1	B	1	1.13000	+- 0.5% VID	All
1	0	1	1	0	0	1	0	B	2	1.13500	+- 0.5% VID	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
1	0	1	1	0	0	1	1	B	3	1.14000	+- 0.5% VID	All
1	0	1	1	0	1	0	0	B	4	1.14500	+- 0.5% VID	All
1	0	1	1	0	1	0	1	B	5	1.15000	+- 0.5% VID	All
1	0	1	1	0	1	1	0	B	6	1.15500	+- 0.5% VID	All
1	0	1	1	0	1	1	1	B	7	1.16000	+- 0.5% VID	All
1	0	1	1	1	0	0	0	B	8	1.16500	+- 0.5% VID	All
1	0	1	1	1	0	0	1	B	9	1.17000	+- 0.5% VID	All
1	0	1	1	1	0	1	0	B	A	1.17500	+- 0.5% VID	All
1	0	1	1	1	0	1	1	B	B	1.18000	+- 0.5% VID	All
1	0	1	1	1	1	0	0	B	C	1.18500	+- 0.5% VID	All
1	0	1	1	1	1	0	1	B	D	1.19000	+- 0.5% VID	All
1	0	1	1	1	1	1	0	B	E	1.19500	+- 0.5% VID	All
1	0	1	1	1	1	1	1	B	F	1.20000	+- 0.5% VID	All
1	1	0	0	0	0	0	0	C	0	1.20500	+- 0.5% VID	All
1	1	0	0	0	0	0	1	C	1	1.21000	+- 0.5% VID	All
1	1	0	0	0	0	1	0	C	2	1.21500	+- 0.5% VID	All
1	1	0	0	0	0	1	1	C	3	1.22000	+- 0.5% VID	All
1	1	0	0	0	1	0	0	C	4	1.22500	+- 0.5% VID	All
1	1	0	0	0	1	0	1	C	5	1.23000	+- 0.5% VID	All
1	1	0	0	0	1	1	0	C	6	1.23500	+- 0.5% VID	All
1	1	0	0	0	1	1	1	C	7	1.24000	+- 0.5% VID	All
1	1	0	0	1	0	0	0	C	8	1.24500	+- 0.5% VID	All
1	1	0	0	1	0	0	1	C	9	1.25000	+- 0.5% VID	All
1	1	0	0	1	0	1	0	C	A	1.25500	+- 0.5% VID	All
1	1	0	0	1	0	1	1	C	B	1.26000	+- 0.5% VID	All
1	1	0	0	1	1	0	0	C	C	1.26500	+- 0.5% VID	All
1	1	0	0	1	1	0	1	C	D	1.27000	+- 0.5% VID	All
1	1	0	0	1	1	1	0	C	E	1.27500	+- 0.5% VID	All
1	1	0	0	1	1	1	1	C	F	1.28000	+- 0.5% VID	All
1	1	0	1	0	0	0	0	D	0	1.28500	+- 0.5% VID	All
1	1	0	1	0	0	0	1	D	1	1.29000	+- 0.5% VID	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
1	1	0	1	0	0	1	0	D	2	1.29500	+- 0.5% VID	All
1	1	0	1	0	0	1	1	D	3	1.30000	+- 0.5% VID	All
1	1	0	1	0	1	0	0	D	4	1.30500	+- 0.5% VID	All
1	1	0	1	0	1	0	1	D	5	1.31000	+- 0.5% VID	All
1	1	0	1	0	1	1	0	D	6	1.31500	+- 0.5% VID	All
1	1	0	1	0	1	1	1	D	7	1.32000	+- 0.5% VID	All
1	1	0	1	1	0	0	0	D	8	1.32500	+- 0.5% VID	All
1	1	0	1	1	0	0	1	D	9	1.33000	+- 0.5% VID	All
1	1	0	1	1	0	1	0	D	A	1.33500	+- 0.5% VID	All
1	1	0	1	1	0	1	1	D	B	1.34000	+- 0.5% VID	All
1	1	0	1	1	1	0	0	D	C	1.34500	+- 0.5% VID	All
1	1	0	1	1	1	0	1	D	D	1.35000	+- 0.5% VID	All
1	1	0	1	1	1	1	0	D	E	1.35500	+- 0.5% VID	All
1	1	0	1	1	1	1	1	D	F	1.36000	+- 0.5% VID	All
1	1	1	0	0	0	0	0	E	0	1.36500	+- 0.5% VID	All
1	1	1	0	0	0	0	1	E	1	1.37000	+- 0.5% VID	All
1	1	1	0	0	0	1	0	E	2	1.37500	+- 0.5% VID	All
1	1	1	0	0	0	1	1	E	3	1.38000	+- 0.5% VID	All
1	1	1	0	0	1	0	0	E	4	1.38500	+- 0.5% VID	All
1	1	1	0	0	1	0	1	E	5	1.39000	+- 0.5% VID	All
1	1	1	0	0	1	1	0	E	6	1.39500	+- 0.5% VID	All
1	1	1	0	0	1	1	1	E	7	1.40000	+- 0.5% VID	All
1	1	1	0	1	0	0	0	E	8	1.40500	+- 0.5% VID	All
1	1	1	0	1	0	0	1	E	9	1.41000	+- 0.5% VID	All
1	1	1	0	1	0	1	0	E	A	1.41500	+- 0.5% VID	All
1	1	1	0	1	0	1	1	E	B	1.42000	+- 0.5% VID	All
1	1	1	0	1	1	0	0	E	C	1.42500	+- 0.5% VID	All
1	1	1	0	1	1	0	1	E	D	1.43000	+- 0.5% VID	All
1	1	1	0	1	1	1	0	E	E	1.43500	+- 0.5% VID	All
1	1	1	0	1	1	1	1	E	F	1.44000	+- 0.5% VID	All
1	1	1	1	0	0	0	0	F	0	1.44500	+- 0.5% VID	All

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Hex		Voltage	Recommended DAC Set point Accuracy Note 1	Market Segment
1	1	1	1	0	0	0	1	F	1	1.45000	+- 0.5% VID	All
1	1	1	1	0	0	1	0	F	2	1.45500	+- 0.5% VID	All
1	1	1	1	0	0	1	1	F	3	1.46000	+- 0.5% VID	All
1	1	1	1	0	1	0	0	F	4	1.46500	+- 0.5% VID	All
1	1	1	1	0	1	0	1	F	5	1.47000	+- 0.5% VID	All
1	1	1	1	0	1	1	0	F	6	1.47500	+- 0.5% VID	All
1	1	1	1	0	1	1	1	F	7	1.48000	+- 0.5% VID	All
1	1	1	1	1	0	0	0	F	8	1.48500	+- 0.5% VID	All
1	1	1	1	1	0	0	1	F	9	1.49000	+- 0.5% VID	All
1	1	1	1	1	0	1	0	F	A	1.49500	+- 0.5% VID	All
1	1	1	1	1	0	1	1	F	B	1.50000	+- 0.5% VID	All
1	1	1	1	1	1	0	0	F	C	1.50500	+- 0.5% VID	All
1	1	1	1	1	1	0	1	F	D	1.51000	+- 0.5% VID	All
1	1	1	1	1	1	1	0	F	E	1.51500	+- 0.5% VID	All
1	1	1	1	1	1	1	1	F	F	1.52000	+- 0.5% VID	All

Note: DAC accuracy is a recommendation only. Total tolerance band must be met, IE. DAC set point + current sense AVP droop accuracy. See applicable platform design guideline for Total tolerance band requirements.

3.7 Dynamic Voltage Identification (D-VID) REQUIRED all segments

The SVID bus will be used to send out a new target voltage and slew rate command to the PWM IC. The VR responds by slewing to the new voltage in a controlled manner with out false tripping of VR_Ready, over voltage or over current protection circuits.

To meet all market segment requirements there are 3 different slew rates, fast, slow and decay.

If the VR is in a low power state (PS1, PS2, PS3) and receives a SetVID_fast or SetVID_Slow (up or dn) the VR should return to power state PS0 enabling all phases to slew the voltage at the commanded slew rate. . The VR will remain in PS0 until the CPU commands it to re-enter a low power state. If a SetVID_Decay is received while in a low power state, the VR slews with the decay rate.

During Dynamic VID operation, the VR's OVP circuitry should be designed to prevent false tripping due the output voltage lagging the DAC set point. Examples of this are to have the OVP set at 200 mV above highest VID voltage. Do not reset OVP threshold as DVID commands a lower voltage. Another method would be to blank the OVP circuits until the VR has settled to the new DAC value. It is left to the vendor as to the implementation method to avoid false tripping of OVP circuits.

3.7.1 Dynamic VID Slew rates- Mobility segment

- Set VID fast= 10 mV/us minimum
- SetVID slow= 1/4 Fast or 2.5 mV/us
    - Optional to program Slow to ½ Fast
- SetVID_Decay- VR does not control slew rate and the output voltage ramps down proportional to current and the magnitude of the capacitor bank. The VR does not control the slew rate, the output voltage declines wiht the output load current only. SetVID_Decay implies diode emulation mode of operation, i.e. the low side MOSFET is not allowed to sync current and the VR automatically goes into PS2 when it receives a SetVID_Decay command. Back to back SetVID_Decay and SetPS command can occur. IE SetVID_Decay and SetPS(PS3). VR_Settled and Alert# functions are disabled during SetVID_Decay

3.7.2 Dynamic VID Slew rates – Desktop segment

- SetVID_Fast= 10 mV/us minimum
- SetVID_Slow = ¼ of fast
- SetVID_Decay- VR does not control slew rate and the output voltage ramps down proportional to current and the magnitude of the capacitor bank. The VR does not control the slew rate, the output voltage declines wiht the output load current only. SetVID_Decay implies diode emulation mode of operation, i.e. the low side MOSFET is not allowed to sync current and the VR automatically goes into PS2 when it receives a SetVID_Decay command. Back to back SetVID_Decay and SetPS command can occur. IE SetVID_Decay and SetPS(PS3). VR_Settled and Alert# functions are disabled during SetVID_Decay

3.7.3 Dynamic VID slew rates - Server segment

- SetVID_Fast= 10 mV/us minimum, 20mV/us typical programmability is desired or optional.
- SetVID_Slow = ¼ of fast
- SetVID_Decay- VR does not control slew rate and the output voltage ramps down proportional to current and the magnitude of the capacitor bank. The VR

does not control the slew rate, the output voltage declines wiht the output load current only. SetVID_Decay implies diode emulation mode of operation, i.e. the low side MOSFET is not allowed to sync current and the VR automatically goes into PS2 when it receives a SetVID_Decay command. Back to back SetVID_Decay and SetPS command can occur. IE SetVID_Decay and SetPS(PS3). VR_Settled and Alert# functions are disabled during SetVID_Decay

3.7.4 Voltage Settled function Required all segments

The VR PWM control IC needs to have a method that detects when the DVID transition is complete and the output voltage is within 10 mV or 2 VID steps targeted voltage. See Figure 6 and Figure 7 for more information. The VR settled function is critical to function when moving from a lower VID to a higher VID.

After the VR has settled, it asserts the VR settled bit in the status register and asserts the Alert line. The VR Settled bit in the status register is a representation of the comparator output. 1= VR is at target VID, 0= VR is slewing to new target. This bit toggles asynchronously with the status of the output voltage changes (settled at VID or slewing). See Serial VID Protocol document for more information on the registers and Alert line.

The VR settled function eliminates the CPU waiting for RC charging time constants for various platform decoupling configurations. A Fast response VR with small capacitor banks will settle faster than slow VR with large capacitor banks and enhance the end user experience. The VR is required to meet the minimum slew rates, IE a SetVID Fast command of 100mV is expected to be completed in 5 us + 3RC time constants where R=LL impedance target and C= total decoupling capacitance.

Overshoot is allowed for a SetVID going upward from LFM VID to higher HFM VID. Getting to the final Vccmin @ new target in the fastest manner results in higher performing platform.

Undershoot is not allowed for a downward direction from HFM VID to LFM VID. Undershoot risks Vmin violation and platform blue screen.

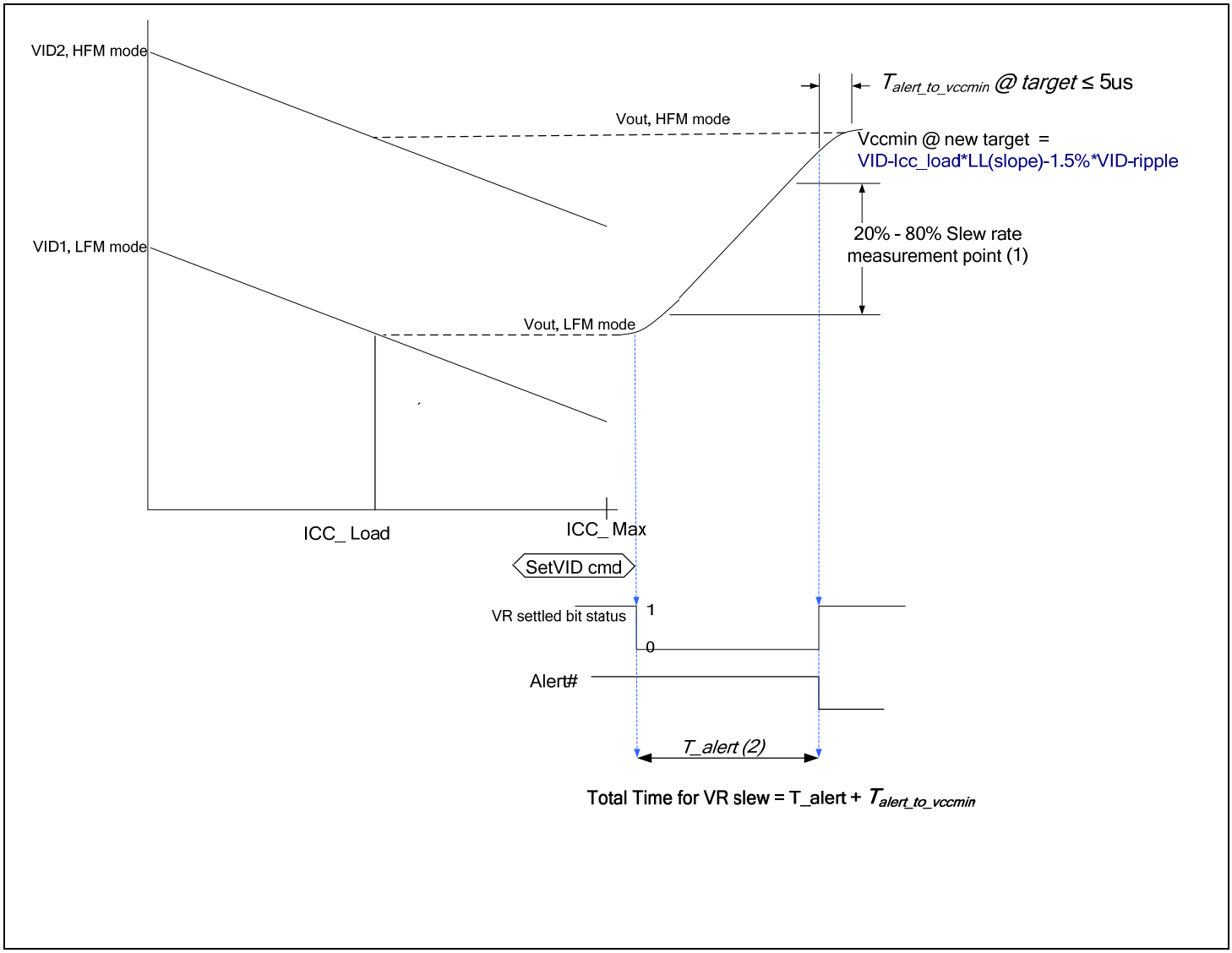


Figure 6 VR Settled example moving from lower to higher VID & VR settled

Notes VR Settled:

1. 20 – 80% is for measuring SetVID Fast, SetVID_Slow for slew rate validation in the test lab. The non-linear regions < 20% and > 80% should be minimized in the PWM control loop.

2. T_Alert target <= $\frac{VID\_Step - 10mV}{SlewRate} + 3RC$ Where R=Load Line target slope, C=total decoupling capacitor value. Actual pass fail validation numbers to be included in market segment VRD and platform design guidelines.

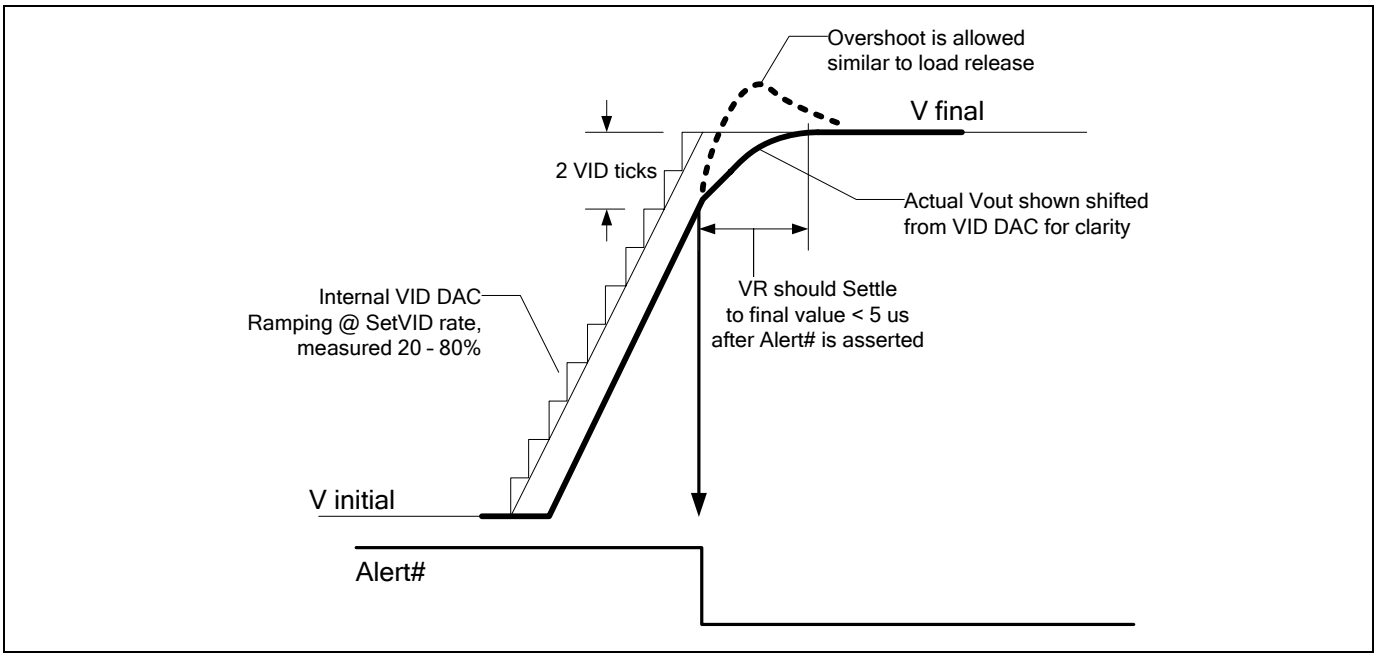


Figure 7 Example of Dynamic VID and VR_Settled, Alert# function

Note: for VID down, undershoot is not allowed.

3.8 VR Power States (PS) Required all segments

The SVID bus can be used to place the VR into multiple VR states for High Efficiency Light Load conditions. These states are entered by programming the power state register using the SVID commands. The power states are listed in order of power savings:

- PS0 = Represents full power or Active mode
- PS1 = Used in Active Mode or Idle Mode and it represents a low current state. Similar to PSI# definition in VR11.1 or IMVP6.5; < 20 A typical
  Ripple is allowed to increase in PS1, PS2, PS3 states. See Figure 8.
- PS2 = Used in Sleep Mode and it represents a lower current state than PS1. <5A typical
- PS3= ultra low current mode lower than PS2, < 1A typical

Support for PS3 is required, even if the VR does not change configuration for PS2 to PS3, it should acknowledge the PS3 command and optimize itself for the low power state.

Actual voltage and current levels in each power state will be detailed in the VR design guidelines and processor EMTS specifications.

VID and Power states are independent and either one can change at anytime as determined by the CPU operating state. The VR output voltage must remain within the

load line tolerance band while transitioning into low power states, since ICC steps can occur at any time. While transitioning out of a lower power state, overshoot relief is allowed similar to load line overshoot specification when the load is released. See Figure 8.

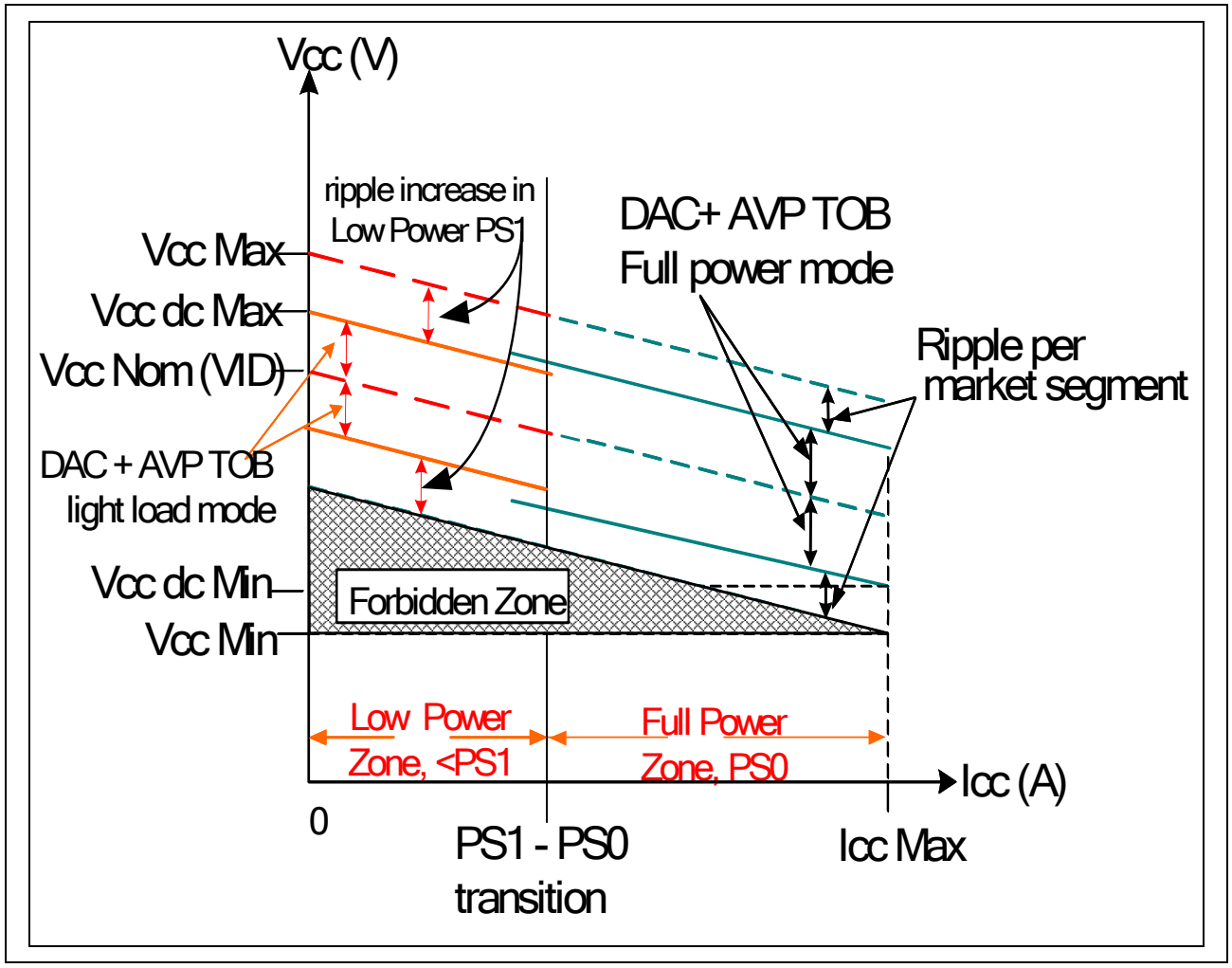


Figure 8 Allowable Power State operating window

Note: Ripple is allowed to increase when going into low power zone (PS1, PS2, PS3) and the VR drops phases. Platform design guidelines will provide ripple specifications per power state for each of the market segment and platforms.

The PWM should exit any low power state and return to PS0 for SetVID_Fast or SetVID_Slow up or down command. If after reaching new higher voltage and the CPU is still in a low current state, it will re-issue PS command to enter High Efficiency Light Load mode.

3.8.1 Power State Exit Latencies

- PS1 to PS0, PS2 to PS0 exit due to SetVID up command, exit latency is zero. IE the VR should be ready for full load step when the VR has reached the new target voltage and has completed the VR_Settled function.
- PS1 to PS0 with out accompanying SetVID < 3.3 us for full load step
- PS2 to PS0 with out accompanying SetVID < 3.3 us for full load step

3.9 VR Data Registers

There are multiple configuration registers that indicate to the CPU the capabilities of the platform. The required functions can be either pin programmed by the VR designer, or programmed into OTP memory at time of board manufacturing by the OEM. If pin programmed, these registers must be loaded after VCC > ULVO and prior to enable being received or during Ta of the start up sequence.

If these data registers are stored in NVRAM or OTP memory, the NVRAM can be internal to the PWM control IC or an external low cost sot23 NVRAM chip. Regardless of the internal or external location, the PWM vendor must provide a method to flash the data during platform manufacturing. If the part supports optional PMBUS, the PMBUS can be used to load this data.

This data is used to configure the CPU power management and performance features. Address of the registers is contained in the *VR12/IMVP7 SVID Protocol* document.

3.9.1 ICC max (21h) Required all segments

Must be programmed by the platform designer. This registers contains information on the maximum current the motherboard VR supports and this can be equivalent to the CPU's Icc_MAX for VR as designed for the system. The master reads this register for platform compatibility checking at boot time and uses this data in conjunction with the Iout register for performance management. See 3.10.3 for more information.

8 bit binary format in amps, i.e. 75A = 4Bh.

Required for both rails in a dual VR.

3.9.2 Temp max (22h) Optional IMVP/Notebook segment, Required Server segments

Register is programmed by platform designer. This register contains the maximum temperature the VR supports prior to issuing a thermal alert or VR_Hot. The master reads this register and uses this data in conjunction with the Temperature Zones for performance management. See 5.6.2 for more information. Typical range is 90 – 120C depending on market segment. One Temp Max set point for both thermal sensors is sufficient as the MOSFET and inductor technology will be similar between the multiphase and single phase rails.

8 bit binary format in deg C, IE 100C = 64h. Accuracy ~ 3 deg C

3.9.3 DC_LL or AVP (23h) Required all segments

The DC_LL or AVP must be programmable on each rail, including being set to 0 or no AVP. Zero LL setting cannot impact OCP levels. This can be pin/resistor programmed or stored in a NVRAM register. Read back of the load line setting is optional.

If programmed in a NVRAM register use the following format: 8 bit binary format in ohms $x10^{-4}$, IE 0Ch = 12d = 1.2 milliohms and read back must be supported.

Platform design guidelines will specify DC_LL value per CPU or market segment. The ranges below are expected operating ranges.

3.9.3.1 Mobility, Desktop segment

Multiphase Rails will have load line range of 0 – 4 milliohms, 2-3 milliohms typical

Single phase rails will have load line range of 0 – 8 milliohms, 3-5 milliohms typical

Required for both outputs on a dual output controller.

3.9.3.2 Server segment

Multiphase Rails will have load line range of 0 – 3 milliohms, 0.8 - 2 milliohms typical

Single phase rails will have load line range of 0 – 4 milliohms, 0 milliohms typical for VSA, 1-3 milliohms other applications

Required for both outputs on a dual output controller.

3.9.4 Slew Rate Fast (24h) Required

Register contains the Fast slew rate capability.

3.9.5 Slew Rate Slow (25h) Required

Register contains the Slow slew rate capability. Default value is ¼ the Fast slew rate. It is optional to support a ½ Fast slow setting.

3.9.6 Vboot (26h) Required all segments

Vboot must be programmable on the platform. Vboot programming is required for both outputs on a dual output VR.

If the value of the Vboot voltage as program as a VID setting 00h=off, no Vboot, the VR waits until it gets SVID VID command. The PWM control IC must be capable of having enable asserted, Vboot= 0.0 V for an indefinite period of time while waiting for initial SetVID_Slow command to ramp the voltage.

If Vboot is programmed to a value, the VR ramps to that VID setting on assertion of enable and stay until SVID command sets new VID. If no SVID command is received, the VR stays at the Vboot voltage. Default value is 00h, no Vboot. 8 bit VID table format.

If resistor pin strapped programming, Vboot must support a minimum of **0.0 V, 0.9 V, 1.0 V, 1.1 V programming levels.** VR12 memory applications require 1.5 V Vboot level. These levels should be programmable by the PWM manufacturer and be able to be changed to different levels with out PWM redesign or mask changes. Low power CPUs utilizing 1+0 and 1+1 PWMs require resistor pin strap programming of Vboot. The final platform design guidelines will specify the value of Vboot.

If register programmed through PMBUS or NVRAM the entire VID table is required to be supported.

3.9.7 VR tolerance (27h) Optional

A register is programmed by the platform designer. The register contains the load line tolerance window based on motherboard part tolerances.

3.9.8 Current Calibration offset (28h) Optional

A register is programmed by the platform designer. Register contains either offset or calibration constants for the output current measurements. Default value is 00h, meaning no calibration has been done.

3.9.9 Temperature Calibration offset (29h) Optional

A register is programmed by the platform designer. Register contains offset to compensate for different thermal sensor locations. Default value of 00h meaning no calibration or offset.

3.10 VR operating Registers

There are multiple VR operating status and configuration registers described in the Intel™ Serial VID Protocol specification. The VR12/IMVP7 PWM must support these data registers. All operating registers are required for each output of a dual output PWM IC.

3.10.1 Vout-max (30h) Required all segments

This register is programmed by the CPU or SVID bus master to the maximum output voltage the load die can support. All VID settings above Vout max should be "rejected" and ignored. The PWM vendor can use this data to set the OVP level at 200mV above Vout_max. Default is 1.5 V. Vout_max is programmed as a VID value format. The CPU can over write this value if it needs a different Vout_max.

Server market segment PWM IC designed for memory applications require default Vout_Max of 1.52V.

3.10.2 Temperature zone (12h) Required all segments

See output monitoring 5.6.2

3.10.3 Iout, Output Current (15h) Required Desktop, Server segments, Optional Mobility

Note: Mobility Segment is not requiring the digital current output reporting through register 15h for 2011/2012 CPUs. Future mobility CPUs in 2013 will require Iout function.

Future Platform Power Management requires the VR to report a digitized value of output current over the SVID bus. The output current is to be sensed in a similar manner as VR Load line and phase current balance. The VR must support, 1-2 ms averaging interval of total output current done in either the analog or digital domain. The target ADC conversion and register update rate is approximately 500 us. The CPU will poll the VR on an approximate 1 ms interval.

If averaging is done in the analog domain, the PWM vendor may choose the voltage scaling and gain terms for the analog current output pin. The voltage range should be specified in the data sheets to aide in lab testing and board debug. (Note: Analog IMON requirements have been removed from the VR12/IMVP7 specifications since it is not required for CPU operation.). The ADC should be scaled such that FFh= ICC_Max for the VR for maximum resolution of the ADC data.

3.10.3.1 Data encoding & ADC Resolution All segments

ADC resolution should target a~ 1 A to 1.2A per LSB or better resolution at ICC max. IE a 3 phase VR targeting 70A ICC_Max should have minimum ADC resolution of 6 bits. 4 phase VRs should have a 8 bit ADC.

- 1-phase VR (~ 20-30 A) requires ADC resolution >= 5 bits minimum
- 2-phase VR (~50-60 A) requires ADC resolution >= 6 bits minimum
- 3-phase VR (~ 75-90 A) requires ADC resolution >= 6 bits minimum
- 4-phase VR (~90-130 A) requires ADC resolution >= 7 bits minimum
- 4-6 phase VR (~130-200 A) required ADC resolution = 8 bit

If a less than 8 bit ADC is used, the data is to be left justified in the register for example a 6 bit ADC the 2 lower LSB filled with 1's. ICC_Max always = FFh in the Iout register.

Bit 7 in the capability register should be set to 1 when Iout register is scaled to FFh=ICC_Max.

3.10.3.2 Data encoding & ADC Resolution – Alternate format for Server market segment

To remain compliant with legacy VR12 silicon implementation, 4+1, 6+1 VRs for the server market segment utilizing an 8 bit ADC, may use register encoding of 1A per LSB, where 01h = 1A, FFh= 255A.

Bit 7 in the capability register should be set to 0 when the Iout register is scaled to FFh=255A.

3.10.3.3 Iout accuracy Targets

Accuracy is a function of the PWM internal circuits, external inductor or shunt and NTC temperature coefficient matching network. Below are typical, RSS 3 sigma platform accuracy targets shown double sided for different phase configurations and different inductor, NTC tolerance assumptions**. Note: CPU Single sided vs. double sided specification is still under debate.** 7% or 5% inductor refers to tolerance of the inductor winding resistance, assuming 0.5 mohm nominal resistance. 3% or 1% NTC refers to an NTC temperature compensation resistor with a 3% or 1% initial tolerance. Tighter tolerance on current reporting will yield a platform with better turbo performance.

Final accuracy targets per market segment will be documented in platform design guidelines with inductor resistance, tolerance, NTC tolerance etc, defined for the typical board in that segment.

Accuracy Targets for various configurations and sense element tolerance

6 Phase VR (130-180 typical)	
VR Load	5% DCR inductor, 1% NTC
5%	+-13.0 %
10%	+-12.0 %
20%	+-6.5 %
30%	+-5.0 %
40%	+-4.5.%
50%	+-4.0 %
60%	+-3.0 %
70%	+-3.0 %
80%	+-3.0 %
90%	+-3.0 %
100%	+-3.0 %

4 Phase VR (90-150 typical)			
VR Load	7% DCR Inductor, 3% NTC	5% DCR inductor, 1% NTC	1% shunt, 0.8 mohm
5%	+-16.0 %	+-15.0 %	+-10.0 %
10%	+-14.0 %	+-13.0 %	+6.0 %
20%	+-8.5 %	+-7.5 %	+-3.0 %
30%	+-7.0 %	+-6.0 %	+-2.5 %
40%	+-6.0 %	+-5.0 %	+-2.0 %

4 Phase VR (90-150 typical)			
VR Load	7% DCR Inductor, 3% NTC	5% DCR inductor, 1% NTC	1% shunt, 0.8 mohm
50%	+-5.5 %	+-4.5 %	+-2.0 %
60%	+-5.0 %	+-4.0 %	+-1.8 %
70%	+-5.0 %	+-4.0 %	+-1.8 %
80%	+-5.0 %	+-4.0 %	+-1.8 %
90%	+-5.0 %	+-4.0 %	+-1.8 %
100%	+-5.0 %	+-4.0 %	+-1.8 %

3 phase VR (60 - 90A typical)		
VR Load	7% DCR Inductor, 3% NTC	5% DCR inductor, 1% NTC
5%	+-18.0 %	+-16 %
10%	+-15.0 %	+-14 %
20%	+-9.5 %	+-8.0 %
30%	+-8.0 %	+-6.5 %
40%	+-7.0 %	+-5.5 %
50%	+-6.5 %	+-5.0 %
60%	+-6.0 %	+-4.5 %
70%	+-6.0 %	+-4.5 %
80%	+-6.0 %	+-4.5 %
90%	+-6.0 %	+-4.5 %
100%	+-6.0 %	+-4.5 %

2 phase VR (45-60A typical)			
VR Load	7% DCR Inductor, 3% NTC	5% DCR inductor, 1% NTC	1% shunt, 0.8 mohm

5%	+-16.0 %	+-15.0 %	+-14.0 %
10%	+-14.0 %	+-11.0 %	+-7.5 %
20%	+-12.0 %	+-9.0 %	+-5.0 %
30%	+-10.0 %	+-8.5 %	+-4.0 %
40%	+-9.0 %	+-7.5 %	+-3.3 %
50%	+-8.0 %	+-7.0 %	+-3.0 %
60%	+-7.5 %	+-6.0 %	+-2.5 %
70%	+-7.0 %	+-6.0 %	+- 2.0 %
80%	+-7.0 %	+-6.0 %	+- 2.0 %
90%	+-7.0 %	+-6.0 %	+- 2.0 %
100%	+-7.0 %	+-6.0 %	+- 2.0 %

1 phase VR(5-30A typical)	
VR Load	7% DCR Inductor, 3% NTC
5%	+-22.0 %
10%	+-20.0 %
20%	+-17.0 %
30%	+-15.0 %
40%	+-12.5 %
50%	+-10.5 %
60%	+-9.5 %
70%	+-9.5 %
80%	+-9.5 %
90%	+-9.5 %
100%	+-9.5 %

3.10.4 VR Temperature (17h) Optional

For PWMs with ADC, store the digitized output temperature in addition to output temperature zones.

3.10.5 Output Voltage (16h) Optional

For PWMs with ADC, store the current output voltage for CPU read back.

3.10.6 Offset (33h) Required all segments

A register programmed by the CPU through the SVID bus to set the number of VID step offset for voltage margining. The offset will also be used on platforms that over clock the CPU and require higher than normal voltage.

IMVP, Notebook market segment VID + Offset does not extend the range of the VID table over 1.52 V. If table extension is not supported, any combination of VID + offset > FFh (1.52V) in VID table should be Rejected and stay at current VID setting.

Server Memory & Desktop Extreme Edition segment it is optional for offset to extend the VID to voltages > FFh, (1.52V) for CPU over clocking, memory VR margining and DC droop compensation.

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4 Start up sequence Required all segments

VR reads the pin programming values or NVRAM register's default values once PWM Vcc is > UVLO, after enable being asserted, during the time period Ta. The various market segment platform design guideline will contain Vboot requirements on the multiphase rail and single phase rail per CPU and memory application.

Start up sequence of VR related signals only:

1. VR has power and chip VCC is > UVLO
2. VR receives hardware enable
3. VR SVID bus is active and idle
4. If Vboot register = 00h, VR waits at 0 volts, VR_Ready de-asserted, hold until SVID command, Alert# remains de-asserted.
   If Vboot register is programmed to a VID setting other than zero, VR ramps to the programmed voltage, asserts VR_Ready and holds until SVID command. It is optional to assert Alert# at the end of Vboot ramp. IE either assert or not assert is OK for the platform.
5. CPU initiates the SVID clock
6. CPU sends out "SetVID_Slow" command to program the initial output voltage
7. VR acknowledges and ramps to the voltage in the SetVID_Slow command at the slow slew rate.
8. VR asserts VR_Ready for that rail.
9. Repeat steps 4, 5, 6, 7, 8 for 2nd VR rail in a dual controller.
10. Start up sequence over.

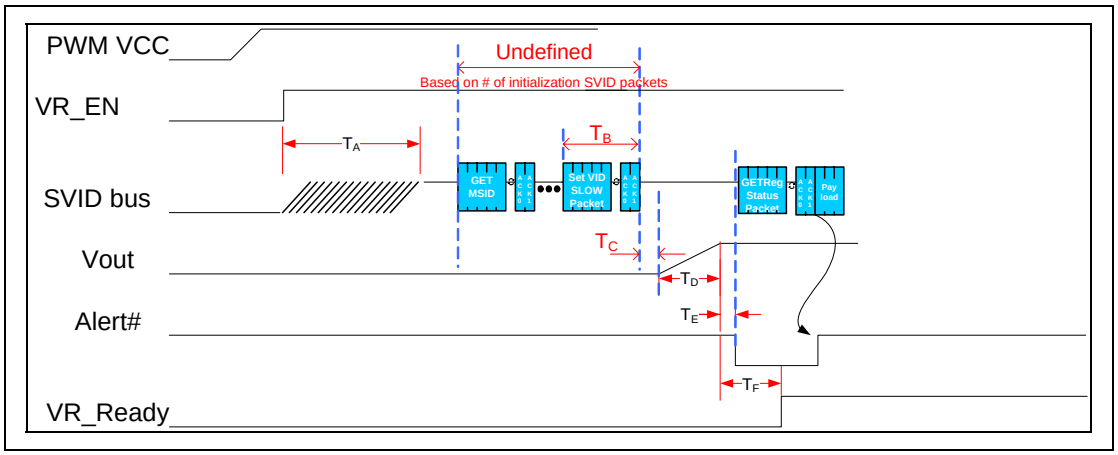

Figure 9 VR start up timings

SVID will have multiple data packets to initialize the VR and the processor. Examples of this are setting Vout_Max register, reading Icc_MAX register etc. followed by SetVID_Slow to the initial voltage to start the voltage ramp.

Table 9 VR Start UP Timings

Description		Min	Typ	Max	Note
T_A	VR_EN until VR Controller is ready accept SVID command			**5 ms**	PWM IC must complete all internal analog and digital configuration and reset protocols during T_A.
T_B	Duration of SVID data packets and SetVID CMD @25 MHz typical.	**SVID protocol dependent**			Any number of packets may occur before 1 SetVID_Slow command
T_C	Acknowledge of SetVID_x CMD to start of voltage ramp, SVID protocol parameter	**0**		**50 us**	Initial Voltage Set or cold boot point only from zero volts. Subsequent SetVID commands delay from ACK to voltage ramp < 5 us
TD	Voltage ramp time, (SetVID_Slow ramp, target voltage dependent)	**50 us**	**440 us**	**2 ms**	Typ represents 1.1V @ SetVID slow 2.5 mV/us. Maximum represents maximum time with optional soft start programmed.
TE	Completion of SetVID ramp to assertion of ALERT# signal			**1 us**	Alert# should comply with to the "within 10 mV of VID target" definition. There should be minimal delay after crossing 10 mV threshold
TF	Completion of SetVID ramp to assertion of associated VR_READY	**TE actual**		**5 ms**	

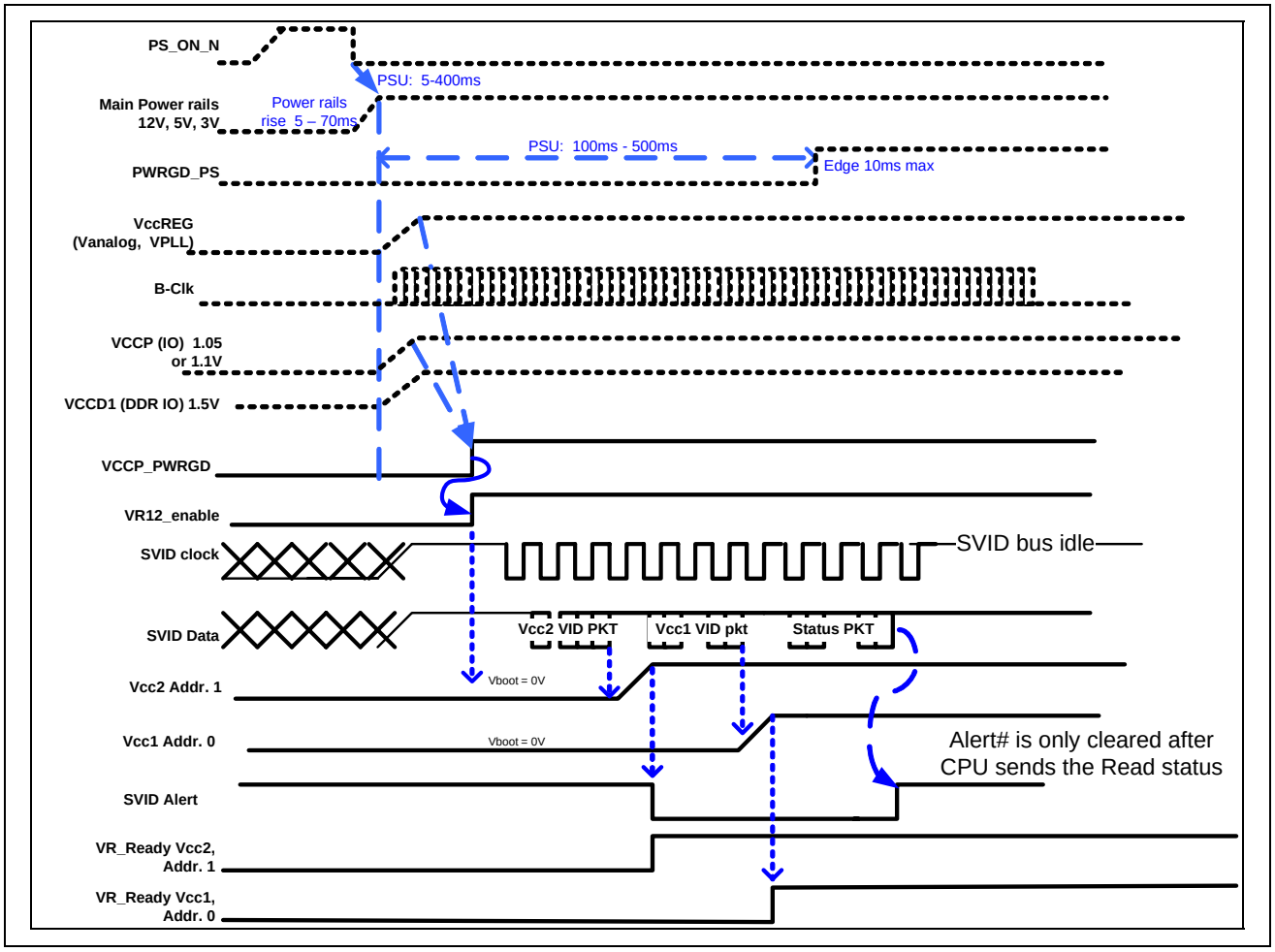

Figure 10. Typical Example Platform Startup Sequence Note Vboot=0V on each rail

NOTES:

1. Vboot = 0 volts shown. If Vboot was programmed, VR would ramp to Vboot and wait for 1st SVID command.
2. All platforms must have Bclock enabled in order to send SVID commands.
3. This example does not represent any market segment power on sequence.
   - .3.1. Server segment will have VSA or address 01h ramp to Vboot then send SVID to ramp address 00h for Vcore.
   - .3.2. Mobility segment will not use Vboot and the CPU will control sequencing between rails 00h and 01h by the SVID command sequence.
   - .3.3. Mainstream Desktop segment will not use Vboot and the CPU will control sequencing between rails 00h and 01h by the SVID command sequence.
   - .3.4. Extreme Edition desktop will follow server sequence.
4. Consult applicable platform VR design guideline for detailed power sequencing.
5. CPU determines when Alert# is cleared. It may choose to ignore the Alert# until after both rails are up. Or it may clear the Alert# after the 1st rail is up.

4.1 VR_Enable REQUIRED all segments

VR_Enable pin is active high and is compatible with 1 V logic (VIH = 0.8V). A single enable pin controls both outputs on a dual output VR control IC.

When VR_Enable is asserted, SVID bus is active and in an idle state waiting for first commands and initial voltage target. When VR_Enable is pulled low or disabled, VR_Ready should be de-asserted and the DC-DC should shut down in a manner that limits the amplitude of below ground ringing to less than 100mV. It is permissible to have a small current sink <1 mA when the VR_Enable is de-asserted to bleed off output capacitor bank. Output. If VR_Enable is toggled for a minimum of 10 ms, the VR should return to the default register states and reinitiate the startup sequence.

During the shut down process, no negative voltage below –100 mV may be present at the DC-DC output when loaded with a resistive load or microprocessor in the system. Caution: Some electronic loads with long leads may cause false readings at turn off.

Table 10 Enable pin voltage levels

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VR_Enable or VR_On	ON/OFF control signal for voltage regulator. CMOS logic.	0	1.0	3.3	V	Input Signal from Platform Logic. When high, the voltage regulator ramps up to $V_{CC-CORE}$. When low, the voltage regulator is disabled.

4.2 Under Voltage Lock Out (UVLO) REQUIRED all segments

The PWM IC should detect the Vcc input and remain in the disabled state until valid Vcc level is available or reached. UVLO is typically 3.0 V in a 3.3 V system, 4.0 V in a 5 V system or 7-8 V in a 12 V system. Ultimately the PWM vendor should set the level to meet his market segment requirements. However, the PWM and driver chips should coordinate start up such that both the PWM Vcc and power conversion rail (typically +12V) of the buck converter are both up and valid prior to enabling the PWM function. The PWM and Driver combination need to be tolerant of any sequencing combination of 3.3 V, 5 V or 12 V input rails. If either the Vcc or power conversion rail falls below the UVLO thresholds, the PWM should shutdown in an orderly manner and restart the start up sequence.

One method to coordinate driver & PWM start up would be for the driver to actively hold the PWM input low, this way the PWM Control IC could sense if the driver was below its under voltage lock out or there was another fault in the driver.

4.3 Soft Start (SS) Optional all segments

The PWM controller should have a programmable soft start function to limit inrush current into the output capacitor bank and prevent false over current protection (OCP) trips. The implementation of the soft start function is left to the vendor. The default Soft Start rate can be the same as the SetVID_Slow slew rate. The 1st SetVID command will be a SetVID_Slow. If optional soft start programming is included, it must comply with the maximum timings in Table 9 VR Start UP Timings.

4.4 Vboot

See section 3.9.6 for Vboot definitions

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5 General Operation

5.1 # phases EXPECTED

See Market Segment Requirements section 2.

5.2 Phase Current Sense Input Expected

The type of current sensing is determined by the tolerance band calculations. Common methods for current sensing are shunts, inductor DCR, MOSFET RDSon and silicon based current mirrors. Due to the large variation in RDSon from lot to lot and manufacturer to manufacturer, Intel does not recommend RDSon sensing for AVP functions. RDSon sensing is acceptable for phase current balance. Inductor DCR or silicon based current mirrors are recommended to implement AVP functions to minimize tolerance band.

The current sense amplifier should be able to work with low resistances in the range of 0.3 - 2.0 mΩ for compatibility with low loss inductors and shunts.

5.3 Error Amp specification: EXPECTED

The error amp should be designed with a sufficient gain BW product to ensure duty cycle saturation does not occur with large signal current transients. Typical target closed loop VR bandwidths of 30-300 kHz expected in VR12/IMVP7 system designs. The output of the error amp should also have high slew rates to avoid duty cycle saturation.

5.4 PWM Operating Frequency EXPECTED

VR12 PWM must be designed to work across various market segments. Typical per phase switching frequencies will be from 200 kHz up to 1 MHz and corresponding loop bandwidths of 50 kHz to 250 kHz respectively.

For fixed frequency PWM topologies, the tolerance of the PWM oscillator should be <+-10%. This applies to power state 0 (PS0) normal operating mode only. In power state 2, the PWM is allowed to vary its frequency or pulse skip.

Vendors with variable frequency topologies should document the limits of the frequency range over load and VID. No load and full load operation should not cause frequency run away.

The design of the VRD and output capacitor technology selection will determine the operating frequency and target loop bandwidths.

5.5 Differential Remote Sense Input REQUIRED

The PWM controller must include differential sense inputs (remote sense, remote sense return) for each PWM control loop. The remote sense will be used for 'die sensing" and to compensate for output voltage droop due to resistance in the output power planes, sockets etc. The remote sense lines should draw no more than **<500** uA to minimize offset errors. The remote sense input needs to have sufficient CMRR to not pass and amplify high frequency processor noise to the VR output.

In the case of a dual VR configuration, dual differential remote sense pairs must be routed to the PWM control IC.

5.6 Output Indicators

5.6.1 VR_Ready REQUIRED

VR_Ready is an active high output that indicates the start up sequence is complete and the output voltage has moved to the Vboot value or the SVID programmed VID value. For a Dual PWM IC, 2 independent VR_Ready lines are required each representing their respective output voltage rails. This signal will be used for start up sequencing for other voltage regulators, the clock, and microprocessor reset etc. The signal should remain asserted during normal dc-dc operating conditions and de-assert for any fault (OCP, OVP etc.) or shutdown conditions. If a fault occurs on one of the rails, its VR ready should de-assert while the non-faulted rail remains asserted.

This signal is not a representation of the accuracy of the DC output to its VID value and does not track the VID during dynamic VID events. The VR Ready line is an indication that the VR is operating properly and all phases are switching. The VR Ready lines should not false trip during any dynamic VID transitions. See Table 11 for signal specifications.

See Figure 9 VR start up timings, Table 9 VR Start UP Timings for more information.

Table 11, Open Drain Output Signal Specifications (VR_Ready)

Signal Type		Open Collector/Drain Logic output from PWM IC, with external pull-up resistor and reference voltage.			
HIGH		Active / Asserted			
LOW		Not Active / De-Asserted			
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Remarks**
VOH	Output Voltage High	**0.8**	**3.3**	Vdc	Vtt rail is expected; however, some systems may pull-up to a maximum voltage of 3.3 V, with external pull-up resistor; Open Coll. /Drain Trans. OFF, Imp. >100kΩ depending on system implementation

Signal Type		Open Collector / Drain Logic output from PWM IC, with external pull-up resistor and reference voltage.			
HIGH		Active / Asserted			
LOW		Not Active / De-Asserted			
Symbol	Parameter	Min	Max	Units	Remarks
VOL	Output Voltage Low	**0**	**0.3**	Vdc	With external pull-up resistor; Open Coll./Drain Trans. ON
IOL	Output Low Sink Current	**1.0**	**4.0**	mA dc	Current limit set by external pull-up resistor
	Transition Edge Rate		**150 ns**		From 10-90% rise

5.6.2 Thermal Monitoring AKA VR_Hot# REQUIRED all segments

VR12/IMVP7 has thermal logic signal output and a temperature zone register for reporting VR temperature status over the SVID bus. VR_Hot# also called VRTT# in IMVP 6.5.. **VR_Hot# is required to be routed to the processors PROCHOT# input pin for all market segments, to initiate thermal throttle low power state of the CPU to protect the VR from overheating.** VR_hot# may also be routed to various system thermal management controllers.

VR_Hot#, VRTT# is Open Drain logic, active low and will be used to drive the CPU's force thermal throttle input. VR_Hot# driver needs to be < 13 ohm resistance to meet the CPU signal integrity requirements, similar to the SVID Alert#. VR_Hot# is typically pulled up to the platform's VTT (1.0 - 1.05V) rail. VR_Hot# output buffer should meet the requirements in Table 3 and Table 4.

For multi-output VR control ICs, there is one VR_Hot# output signal that asserts if either the multiphase or single phase thermal sensor indicates an over temperature condition. The trip point for VR_Hot# is the same for either rail on a dual PWM IC.

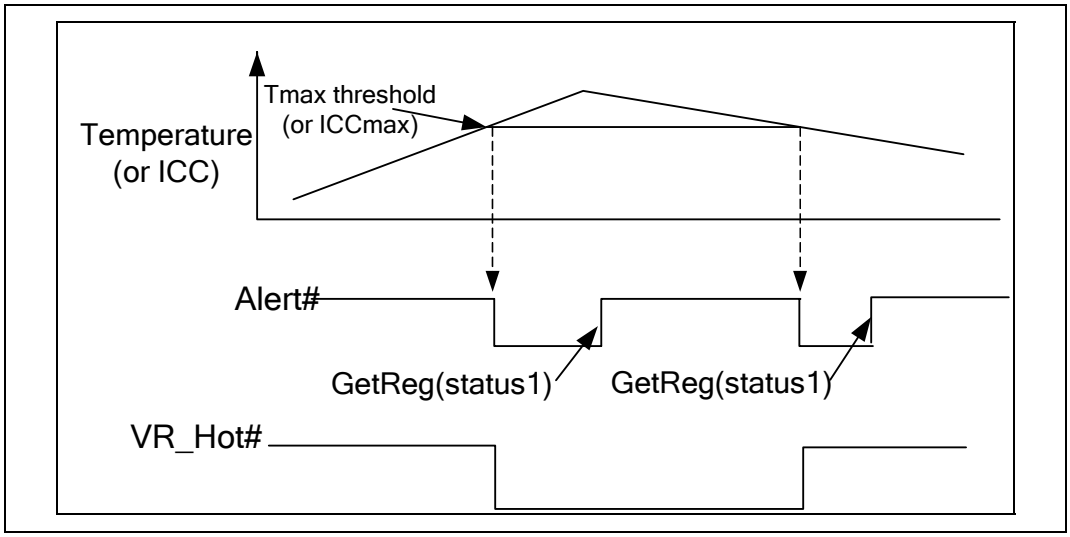
2 thermal sensor inputs are required, one for each rail on a dual PWM ic in the desktop and mobile market segment. The 2nd thermal sensor for the single phase rail is optional for server market segment. The thermal sensor should be external to the PWM control IC since the PWM control IC is normally not located near heat generating components. Thermal sensors need to be implemented in a manner that allows sensing of phase temperature. The trip point needs to be externally programmable by the system designer. The hysteresis VR_Hot or SVID Thermal_Alert should be 1 tick in the temperature zone register or approximately 3%. The tolerance on VR_Hot should be +- 4% or approximately +-4 deg C, optimized in the target range of 90 to 120 deg C. Accuracy window can be larger at lower temperatures to accommodate non-linearity of NTC thermister.

In addition to the VR_Hot# hardware signal, there is a Temperature zone register that indicates how close the VR is operating to the VR_Hot trip point. When the VR temperature reaches bit 6 or SVID Thermal alert state, it asserts bit 1 in the Status 1 register and asserts the Alert# line this condition is called SVID Therm_Alert. When the VR cools down bit 1 toggles from 1 to 0, the Alert# line is re-asserted to indicate the condition has cleared. SVID Thermal Alert bit is not cleared with a GetReg(status1) command. See Figure 12. The data in the temperature zone register should be updated asynchronously with the SVID bus and update as the temperature changes. As long as there is a VR thermal alert condition, bit 1 in status 1 stays asserted (IE bit 1 is a sticky bit).

Figure 11 Thermal zone and detection encoding

Temp. Max VR_Hot#	SVID Therm. Alert		Comparator Trip Points and example shows temperatures scaled to 100C=100%= Temp Max setting				
b7	b6	b5	b4	b3	b2	b1	b0
100%	97%	94%	91%	88%	85%	82%	75%
100C	97C	94C	91C	88C	85C	82C	75C
Example Register contents for 95C							
0	0	1	1	1	1	1	1

Figure 12 Alert#, Thermal_Alert & VR_HOT# behavior.



There can be multiple GetReg(status1) commands between when SVID Therm_Alert asserts and de-asserts since thermal time constants are much longer than dynamic VID transitions.

Optional features include digitizing of the temperature sensor and storing that data in the temperature register to be read back over the SVID or PMBUS interface.

5.7 Output Protection

These are features built into the DC-DC to prevent damage to itself, the processor, or other system components. Intel has left this section vague since these are system level features and we desire VR vendors to optimize their PWM chips to the market segments they service. The main function of OCP or OVP is to prevent damage to the system board in case of component failure. Operating in an OVP condition does not guarantee there will be no damage to the microprocessor. In the case of a dual PWM IC chip, if there is a fault on 1 rail, both rails should shut down as appropriate.

Note OVP and OCP are proposed in this document since they are not critical to Intel CPU functions. These are platform level requirements and VR control IC vendors should consult with their customers on how to support these functions.

5.7.1 Over-Voltage Protection (OVP) PROPOSED

The main function of OVP is to prevent smoke or fire in a platform from a failed VR circuit or component. An OVP circuit should monitor the output for an over-voltage condition. There are 2 methods to implement OVP functions:

1. Fixed OVP, output voltage can never exceed 200mV above the Vout_Max program level under any fault condition. See 3.10.1. This function allows the CPU designer to set the OVP level by changing the Vout_Max level as the CPU silicon technology changes.

2. Tracking OVP, output voltage can never exceed 200mV above programmed VID target+ positive offset . For tracking OVP, OVP can be blanked during dynamic VID events to prevent false trigger. The blanking time should be commensurate with the Dynamic VID settling time.

With either implementation, the VR should not have false OVP trip due to turn on into a pre-charged capacitor bank.

In the event of an OVP condition, the VR should turn off the top MOSFET driver, turn on the low side MOSFETs and de-assert VR_Ready and shut down until reset by toggling enable or PWM IC input Vcc (system power supply reset). It is desired that the OVP latch stay active below the standard UVLO for the PWM IC so that the low side MOSFETS clamp if the 12V rail sags below the PWM control IC UVLO point.

It is optional to support a VR Fault pin that asserts and notifies the platform of a VR fault condition for desktop and notebook platforms, it is required for server platforms.. The fault output will be used to turn off the platform AC-DC power supply to limit the energy into a failed VR. See 5.7.3

5.7.2 Over-Current Protection (OCP) PROPOSED

The DC-DC should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the DC-DC. The OCP trip level should be programmable by the dc-dc designer, typically 130% of rated output current. If an OCP fault is detected, the VR should change its mode of operation (fold back, hiccup

mode, regulate for X cycles then latch off etc.) to protect it self against damage, smoke etc.

OCP shall work on a per phase basis and be correctly scaled for the remaining phase or phases during low power states such as PS1. OCP shall work with any Load Line or AVP setting including 0 mohm LL or no LL support.

It is optional to support a VR Fault pin that asserts and notifies the platform of a VR fault condition for desktop and notebook platforms, it is required for server platforms.. The fault output will be used to turn off the platform AC-DC power supply to limit the energy into a failed VR. See 5.7.3

5.7.3 Catastrophic Fault Detect – Expected for Server Segment

The controller should accommodate Catastrophic Fault Protection (CFP) circuitry that detects a component failure in the regulator's power train. A catastrophic failure is a failure that will result in an exothermic event**2** if the power source is not removed. A predominate catastrophic failure is a high side FET shorting. Immediately upon detection of a catastrophic failure, the CFP circuit should assert a fault signal.

A shorted high side FET or a FET operating in its linear region may be detected by monitoring the phase node or by measuring and comparing the regulator's input power versus output power. An output over voltage condition cannot be relied upon to occur prior to an exothermic event.

The fault signal should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply. This feature should work during power on sequencing, in case a computer shuts down and the user just recycles the power supply's AC input.

1 This feature is EXPECTED by systems with power rails capable of supplying continuous power in excess of 240VA.

2 An exothermic event is an occurrence of smoke or flames that alarms an end user and generally ends with such extensive board and component damage that component failure analysis is not possible.

5.8 VR Tolerance

5.8.1 Load Line Definitions REQUIRED all segments

The PWM chip should not preclude programming any load line slope or AVP gain from 0 to 10 mohms. The individual processor or load specifications will set the load line and current level specification. Over current protection and 0 mohms load lines are required to be independent. IE setting a 0 mohm LL will have no effect on OCP trip points.

Load line settings are platform specific and will not be changed with SVID command nor will Master attempt to read the load line setting over the SVID bus.

5.8.2 Voltage Tolerance REQUIRED all segments

The voltage tolerance is required over DC input operation conditions, temperature operating conditions and lot to lot variation of PWM IC. The PWM design sets the steady state or DC load line accuracy based on DAC set point tolerance and Load Line or AVP tolerance.

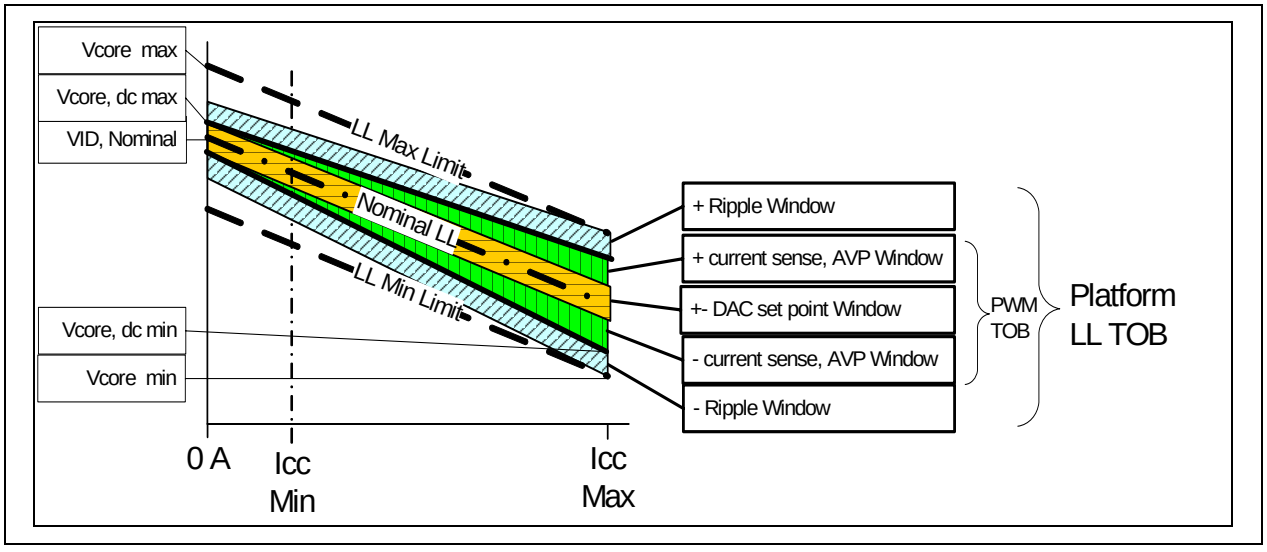
For the total platform load line tolerance, ripple voltage is added in separately to VR tolerance window based on platform and market segment requirements. Mobility typically uses +-10mV ripple specification; Desktop and Servers typically use +-5 mV ripple specification. The Electrical Design Specifications (EDS) & Platform Design Guidelines (PDG) will contain detailed breakdown of VR tolerance band per market segment and CPU type.

The overall requirement is for the VR to stay within the TOB window, the absolute values of set point, current sense, AVP and ripple voltages are not important.

Platform Tolerance Budget (TOB) window includes:

- +- Platform Ripple window
- +- DAC set point window – See 3.6 VID Table
- +- Current sense, AVP window
- Total TOB should be RSS sum of Dac set point window and AVP window with the Platform ripple added on top..
- When making tolerance band calculations the individual components that make up the tolerance should be specified as a percentage at the +- 3σ distribution points.
- VR tolerance bands will be documented inElectrical Design Sepecifications and Platform Design Guidelines per market segment.

Figure 13. VR tolerance definitions (neglecting overshoot relief)



5.8.3 Load Line Thermal Compensation REQUIRED all segments

Thermal compensation allows the microprocessor Vcc voltage regulator to respond to temperature drift in VRD electrical parameters. It is required to ensure that regulators using inductor current sensing maintain a stable voltage over the full range of load current and system temperatures. Thermal compensation is required on both rails in a dual output PWM controller.

If thermal compensation is not included, the output voltage of the regulator will droop as the resistance of the sense element increases with temperature. With the increased resistance, the regulator falsely detects an increase in load current and regulates to a lower voltage. Thermal compensation prevents this thermally induced voltage droop by adjusting the feedback path based on the temperature of the regulator. This is accomplished by placing a thermister in the feedback network, tuned with a resistor network to negate the effects of the increased resistance of the sense element.

The thermal compensation circuit is to be validated by running the regulator at the Voltage Regulator Thermal Design Current (VRTDC) and minimum required air flow for 30 to 45 minutes. This is to ensure the board is thermally stable and system temperatures have reached a maximum steady state condition. If the thermal compensation has been properly implemented, the output voltage will only drift 1-2 mV from its coolest temperature condition. If the thermal compensation has not been properly implemented, the voltage can droop in the tens of mV range

5.9 No load operation required all segments

The PWM chip design should be such that the VR can operate at no load or Zero current load without errors or false trip of OVP, or de-asserting VR_Ready.

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6 Design collateral

6.1 Demo, test board requirement (VRTB) REQUIRED

A test board with a socket LGA1366 & socket R will be required for evaluation of the PWM controllers submitted to Intel for evaluation.

Each segment will specify the VRTB requirements. Initial desktop and server PWMs can be submitted on the desktop VRTB with socket H2.

6.2 Computer models REQUIRED

Intel evaluation requires submission of both state averaged and switching computer compatible models of the PWM controller.

IBIS or Spice models of the SVID buffers is required for signal integrity study and simulation on the SVID bus. For more information on IBIS models see http://www.eigroup.org/ibis/ for more information. In particular down load the "Ibis Cookbook" and under Free Tools the IBIS Golden Parser to check your model formats.

6.3 VR Tolerance Band calculator REQUIRED

As an aid to VR design and component selection, Intel requires the PWM vendor to provide a Load Line tolerance band calculator that allows the OEM/ODM to calculate what tolerance band a particular design will have based on his component selection. This model should contain the parameters within the PWM IC that effect the load line tolerance. The format for the load line calculator should be an MS-Excel* spreadsheet or MathCAD* or web based design file.

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7 SMBUS/PMBUS support for Servers or extreme edition desktop – Optional

Some OEMs require PMBUS support for data collection from the VR. PWM ICs that supports this function should comply with the PMBus™ Application Profile for Vcore regulators for Compute Market Segment. See WWW.PMBUS.org for the latest application profile.

SetVID and Set power state commands from SVID bus always take precedent over PMBUS commands. The VR must acknowledge the SVID command when received, other wise the CPU will enter its error handling routine and eventually shut down due to catastrophic communications fault. PMBUS can be used to implement DAC offset or margin to shift the VID table for over clocking etc., read back telemetry data, programming of configuration registers etc.

Multiple VR12 controllers will be on a common SMBUS/I2C bus on server and desktop platforms. SMbus, PMBUS, I2C options must support programmable addressing for the respective communications bus that is independent of the SVID bus address.

It is recommended that SMBUS/PMBUS addresses be pin strapped or resistor programmed so simple manufacturing defect analysis (MDA) or flying probes can verify the address is programmed to the right location when there are multiple VR controller IC on the same board.

Table 12 Minimum Recommended PMBUS command set

Command code	Command	Description
01h	OPERATION	
20h	VOUT_MODE	The **VOUT_MODE** command, used for commanding and reading output voltage, consists of a three-bit mode (Only linear format is supported.) and a five-bit parameter representing the exponent used in output voltage Read/Writes.
21h	VOUT_COMMAND	The VOUT_COMMAND is used to set the output voltage, in volts (Linear Format).
25h	VOUT_MARGIN_HIGH	The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in volts (Linear Format), when the command is set to "Margin High". (typically used to offset VID command to voltages higher than 1.52V for over clocking) VR should still respond to VID commands.

26h	VOUT_MARGIN_LOW	The VOUT_**MARGIN_LOW** command loads the unit with the voltage to which the output is to be changed, in volts (Linear Format), when the command is set to "Margin Low".
8Bh	READ_VOUT	The READ_VOUT command returns the actual measured output voltage in the same format as set by the VOUT_MODE command In a LL enabled VR, this should be an averaged value.
8Ch	READ_IOUT	The READ_IOUT command returns the output current in amps (Literal Format)
8Dh	READ_TEMPERATURE_1	The READ_TEMPERATURE1 command returns the temperature, in □C (Literal Format), of the external sense element
96h	READ_POUT	Read back Output Power, read back in Linear Mode in Watts.

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