

Compal Confidential

PIQY1 M/B Schematics Document

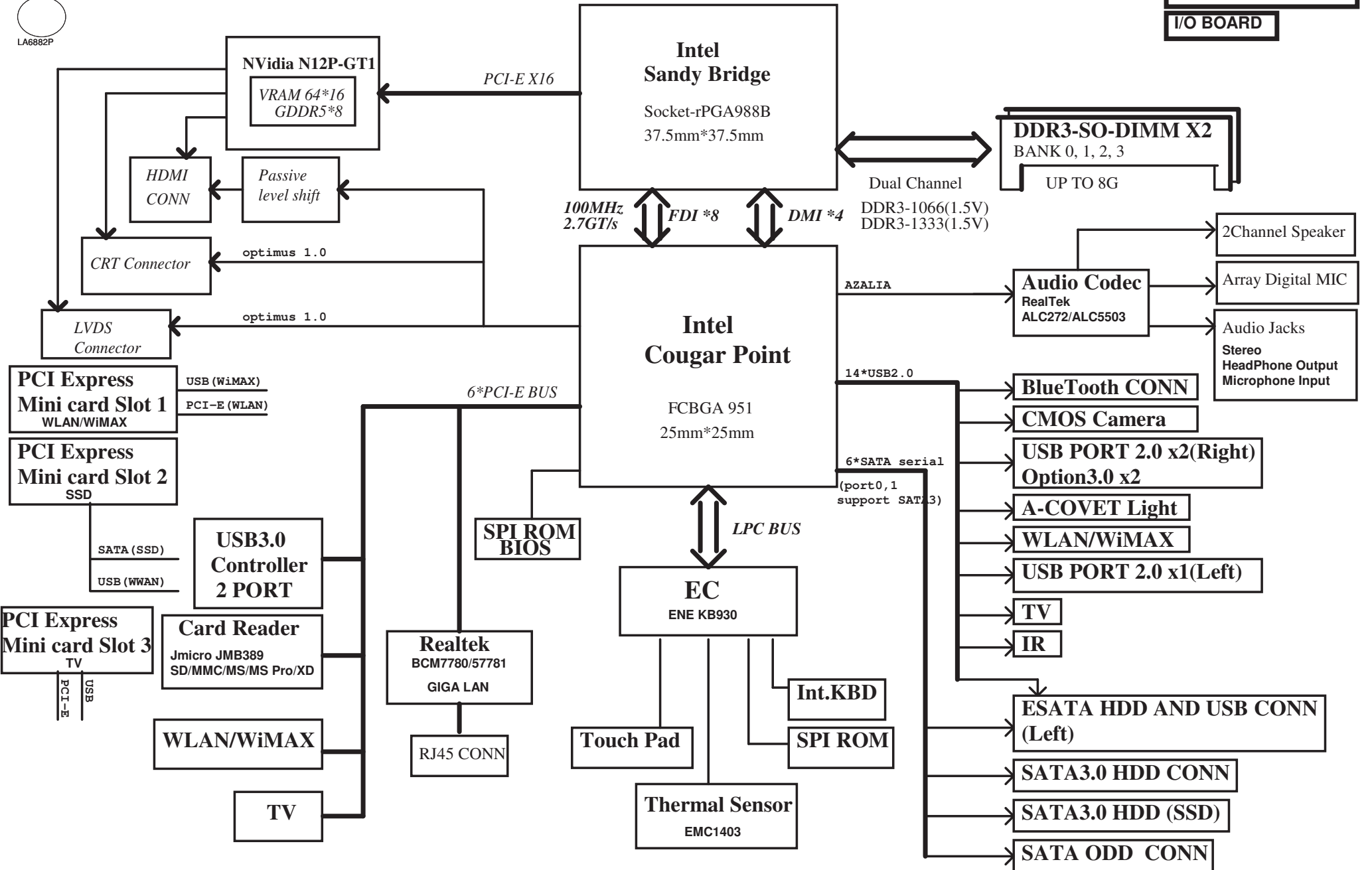
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT1

2010-10-05

REV: 0.2

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POWER & BOARD
CAP SENSOR BOARD
I/O BOARD



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Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
				State
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Board ID	Vcc		V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	
	Ra/Rc/Re	3.3V +/- 5% 10K +/- 5%				
0	0		0 V	0 V	0 V	EVT
1	8.2K +/- 5%		0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%		0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%		0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%		1.036 V	1.185 V	1.264 V	
5	100K +/- 5%		1.453 V	1.650 V	1.759 V	
6	200K +/- 5%		1.935 V	2.200 V	2.341 V	
7	NC		2.500 V	3.300 V	3.300 V	

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Right Side)
		3	USB Port (Right Side)
	UHCI2	4	Camera(3D)
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	IR
		9	Mini Card(WLAN)
	UHCI5	10	A Cover Light
		11	
UHCI6	12	Mini Card(TV)	
	13	Blue Tooth	

BOM Structure Table

BOM Structure	BTO Item
OPTI@	OPTIMUS part
DIS@	Discrete part
UMA@	UMA part
DIS_ONLY@	Discrete only part
HDMI@	HDMI part (DIS and UMA)
UMA_HDMI@	HDMI part (UMA)
DIS_HDMI@	HDMI part (DIS)
USB20@	USB20 option (Right side 2 ports)
USB30@	USB30 option (Right side 2 ports)
USB30_SUB@	USB30 part at sub-board
TV@	TV module part
TV_SW@	TV module power switch part
NO_TVSW@	No TV module power switch part
USB_CHG@	USB charger part
NO_CHG@	No USB charger part
272@	ALC272 audio codec part
5503@	ALC5503 audio codec part
57780@	BCM57780 LAN part
57781@	BCM57781 LAN part
ACOVER@	A cover light part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
ESATA@	E-SATA part
VENTURA@	NVIDIA VENTURA function part
X76@	X76 Level part
S1G@	Samsun VRAM 1G part
S2G@	Samsun VRAM 2G part
H1G@	Hynix VRAM 1G part
ME@	ME part
@	Unpop

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb
		Thermal Sensor EMC1402-1	100_1100 b

EC SM Bus2 address

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

PCI-E PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	USB3.0
5	Card Reader
6	TV
7	
8	

SKU

OPTIMUS	UMA@+DIS@+OPTI@
Discrete only	DIS@+DIS_ONLY@

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VGA and GDDR5 Voltage Rails (N12Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	I/O	N/A	
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	N/A	
GPIO14	OUT	N/A	
GPIO15	IN		Hot Plug Detect for IFPE
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

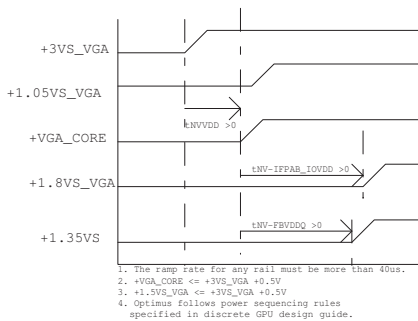
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N12P-GT1 64bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	BGIO_PAD_CFG_ADR[3]	BGIO_PAD_CFG_ADR[2]	BGIO_PAD_CFG_ADR[1]	BGIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

GPIO5 GPIO6

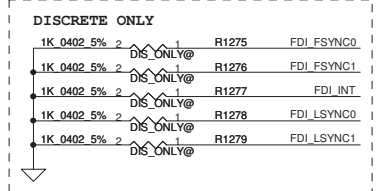
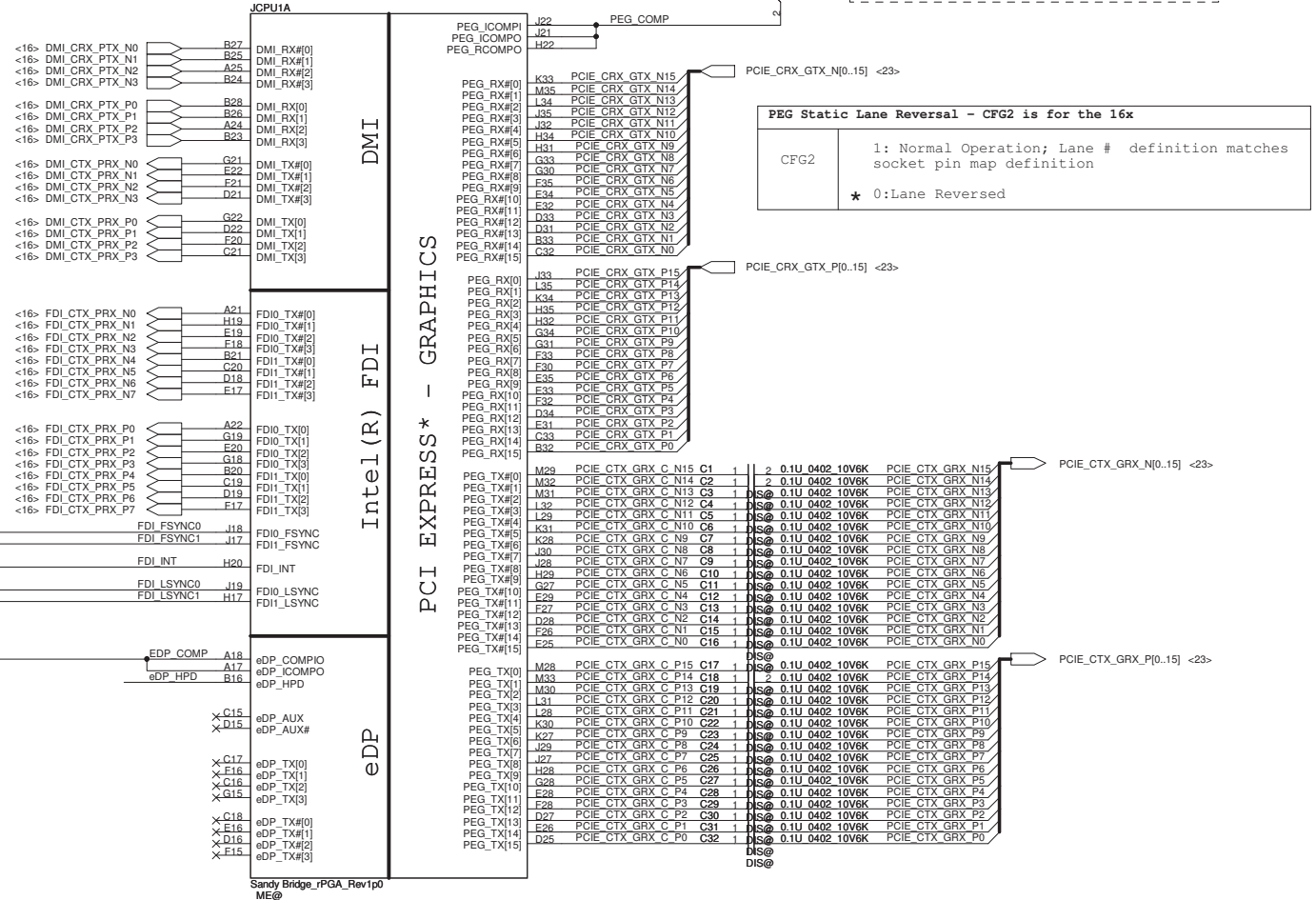
Device ID	GPU_VID0	GPU_VID1	VGA_CORE	P-State
	N12P-GT1 (40nm)	0	0	0.825V
	0	1	0.825V	P8
	1	1	1.075V	P0

GPU	FB Memory (GDDR5)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N12P-GT1	Samsung 1800MHz (default)	K4G10325FE-HC04					
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K PU 45K
	Hynix 1600MHz	H5GQ1H24AFR-T2L					
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K PU 45K



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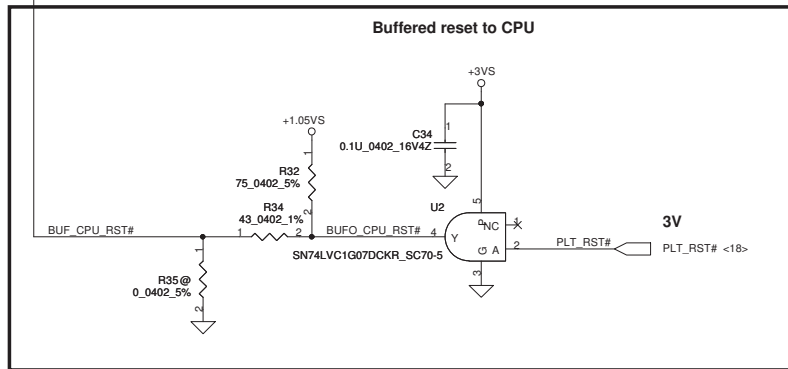
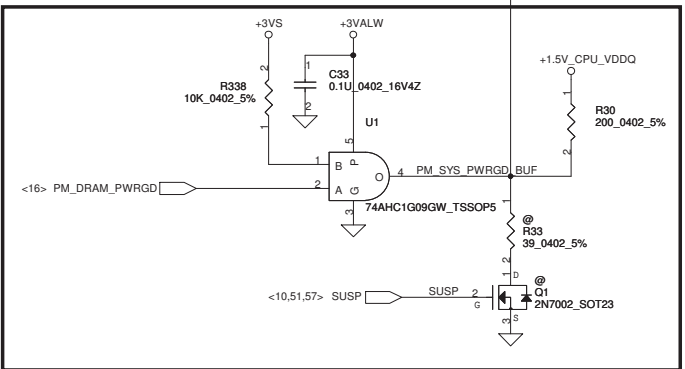
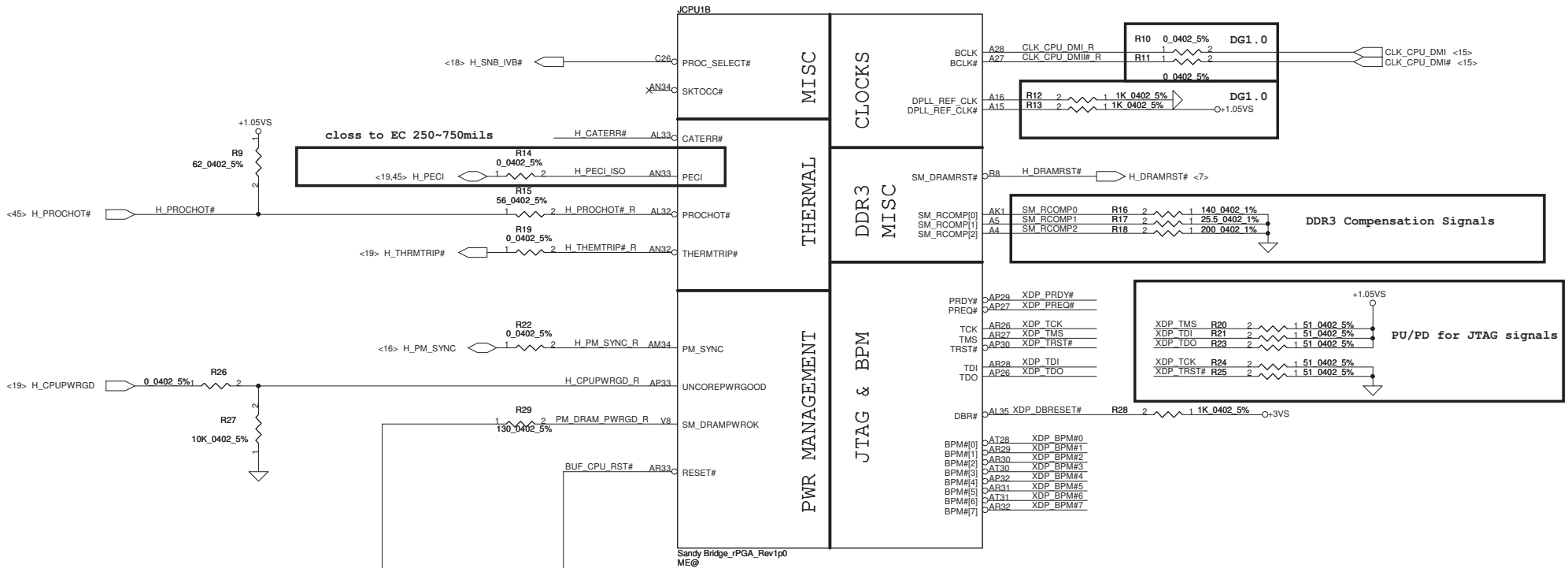
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



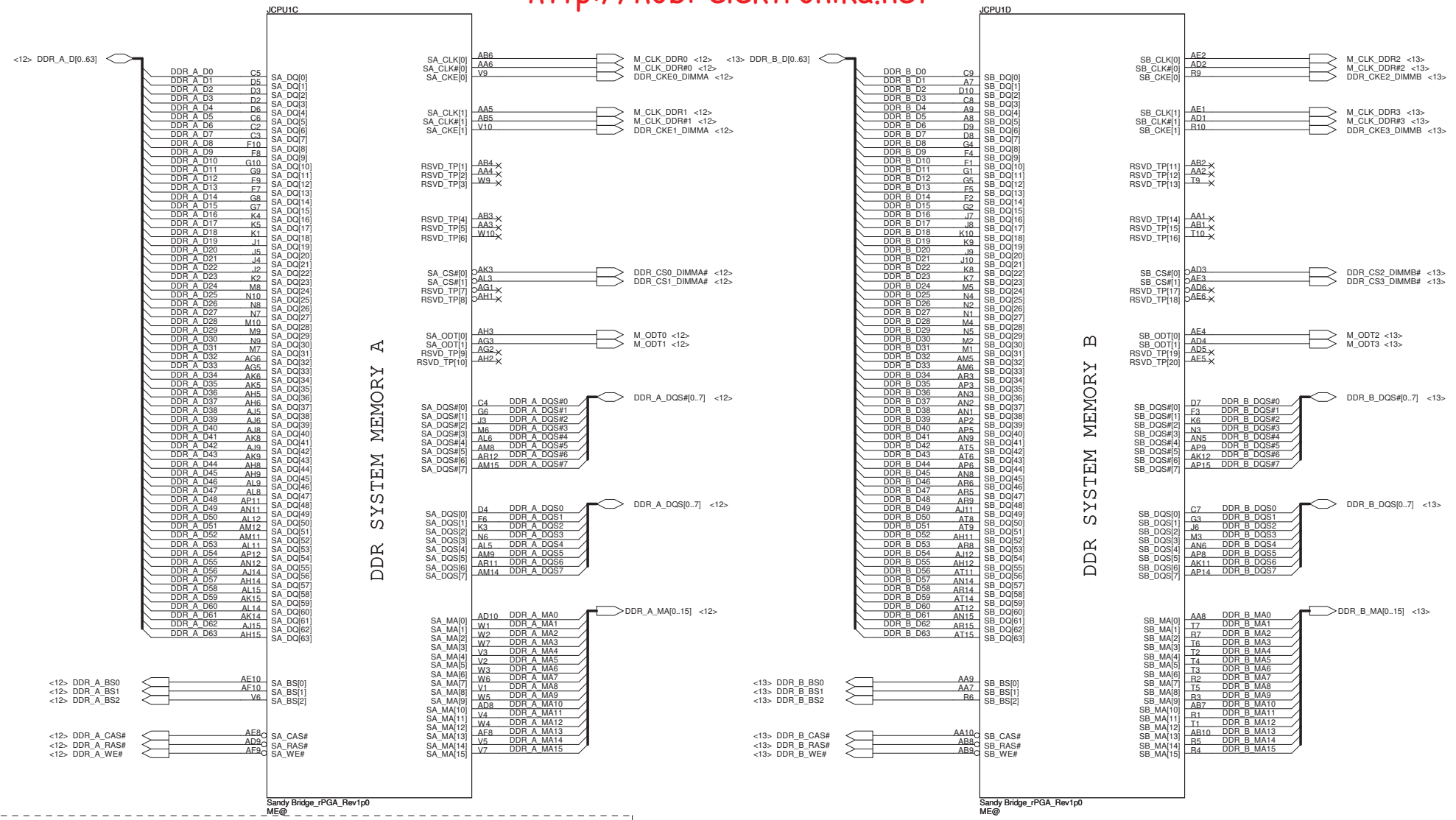
eDP_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG Static Lane Reversal - CFG2 is for the 16x

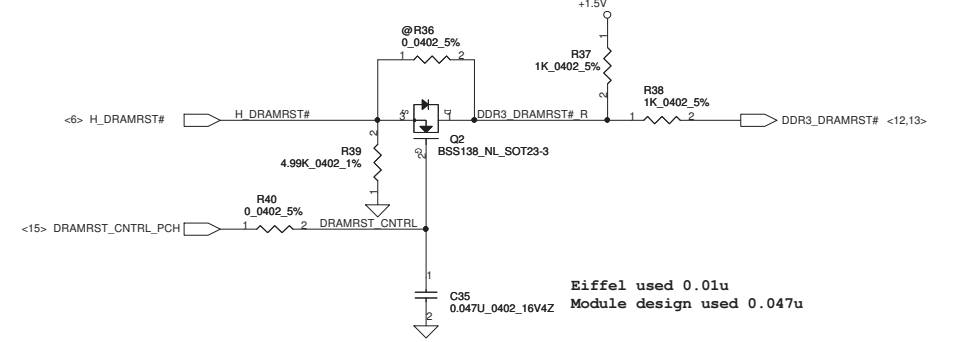
CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
 * 0: Lane Reversed



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Title	PROCESSOR(2/7) PM,XDP,CLK			
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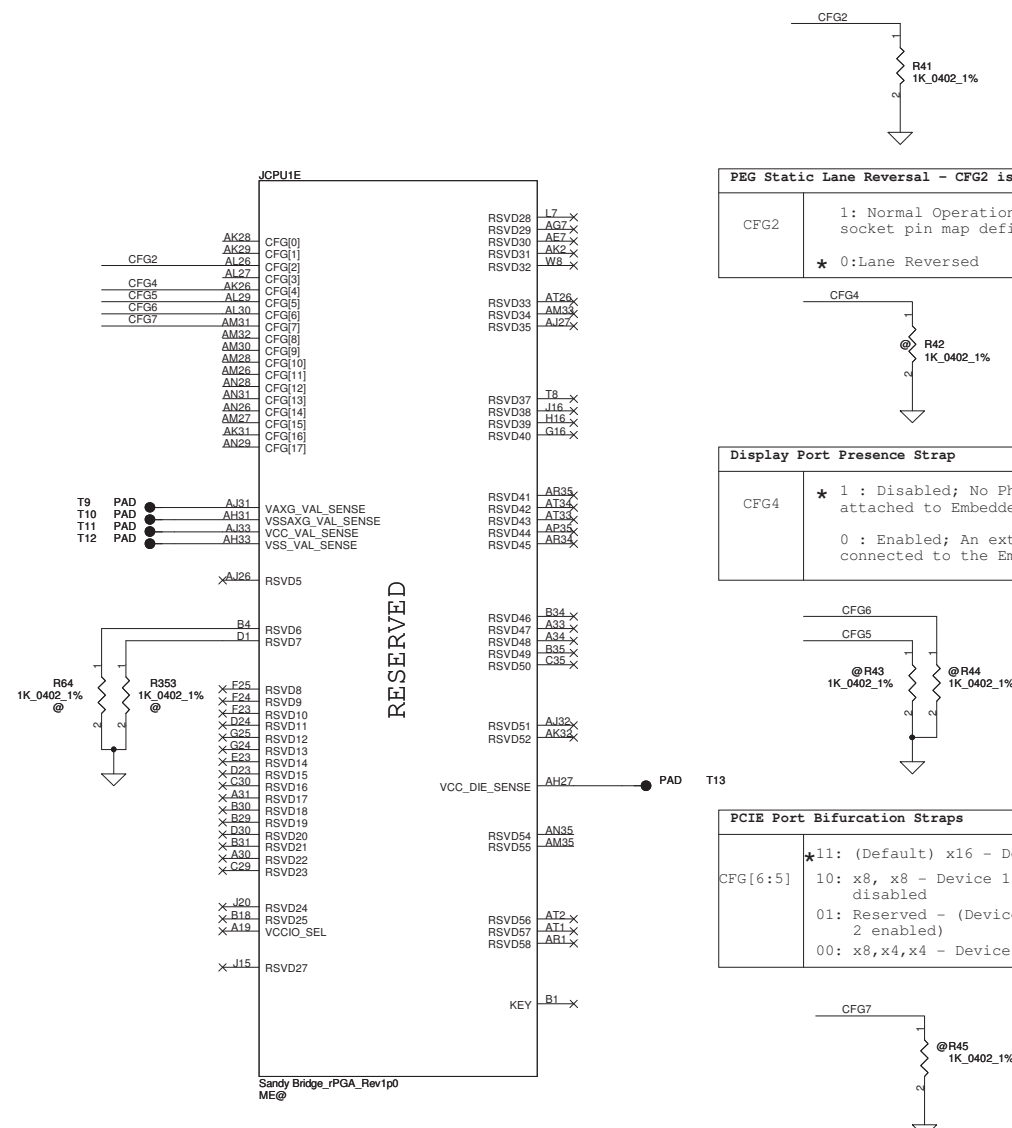
Sandy Bridge_rPGA_Rev1p0 ME@



Eiffel used 0.01u
Module design used 0.047u

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title	PROCESSOR(3/7) DDRIII
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PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed
------	--

Display Port Presence Strap

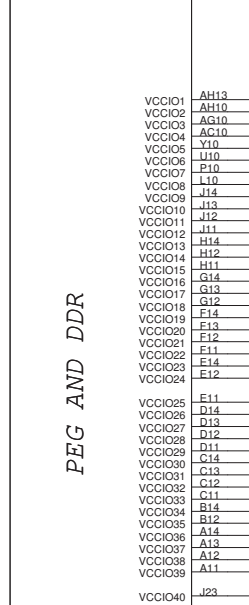
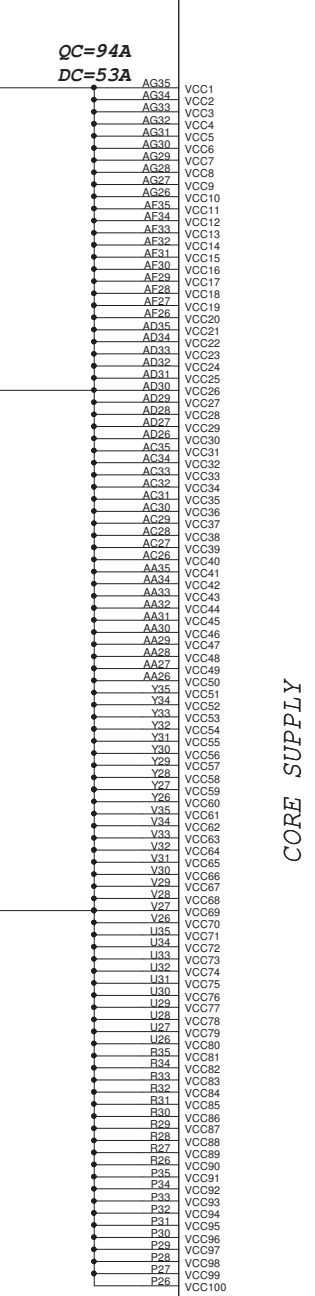
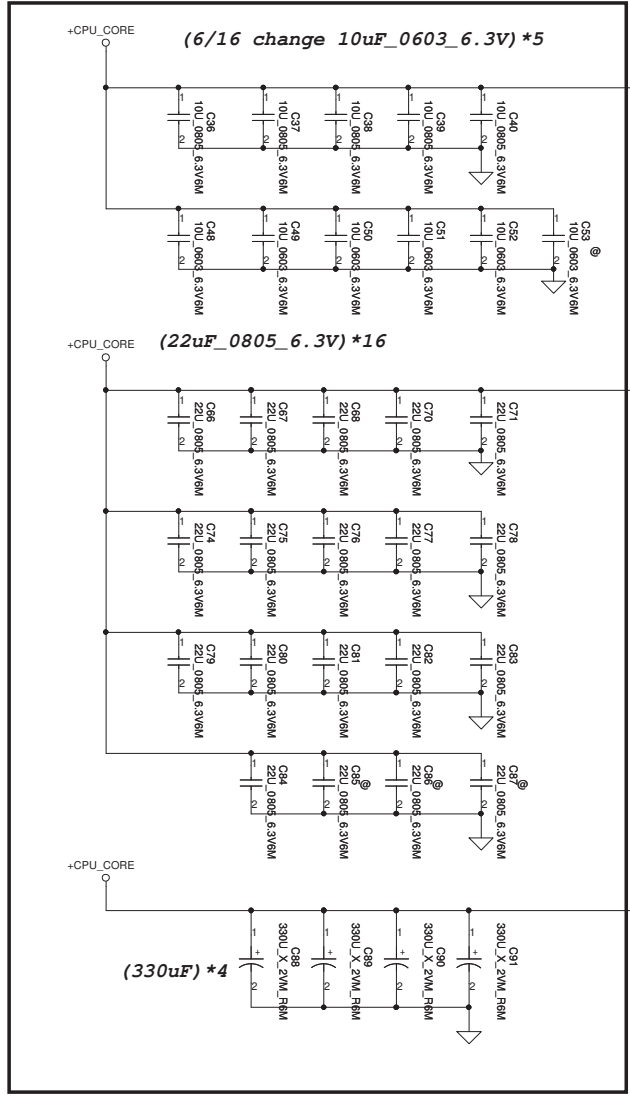
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

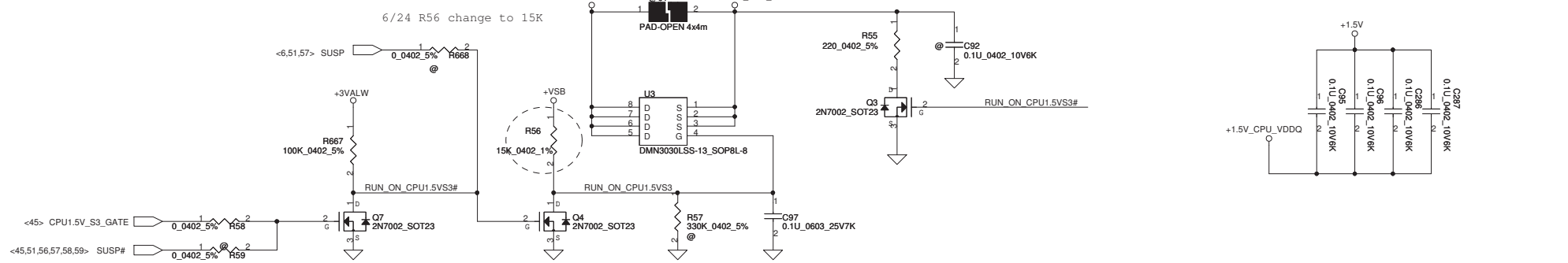
PCIe Port Bifurcation Straps

CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled
----------	--

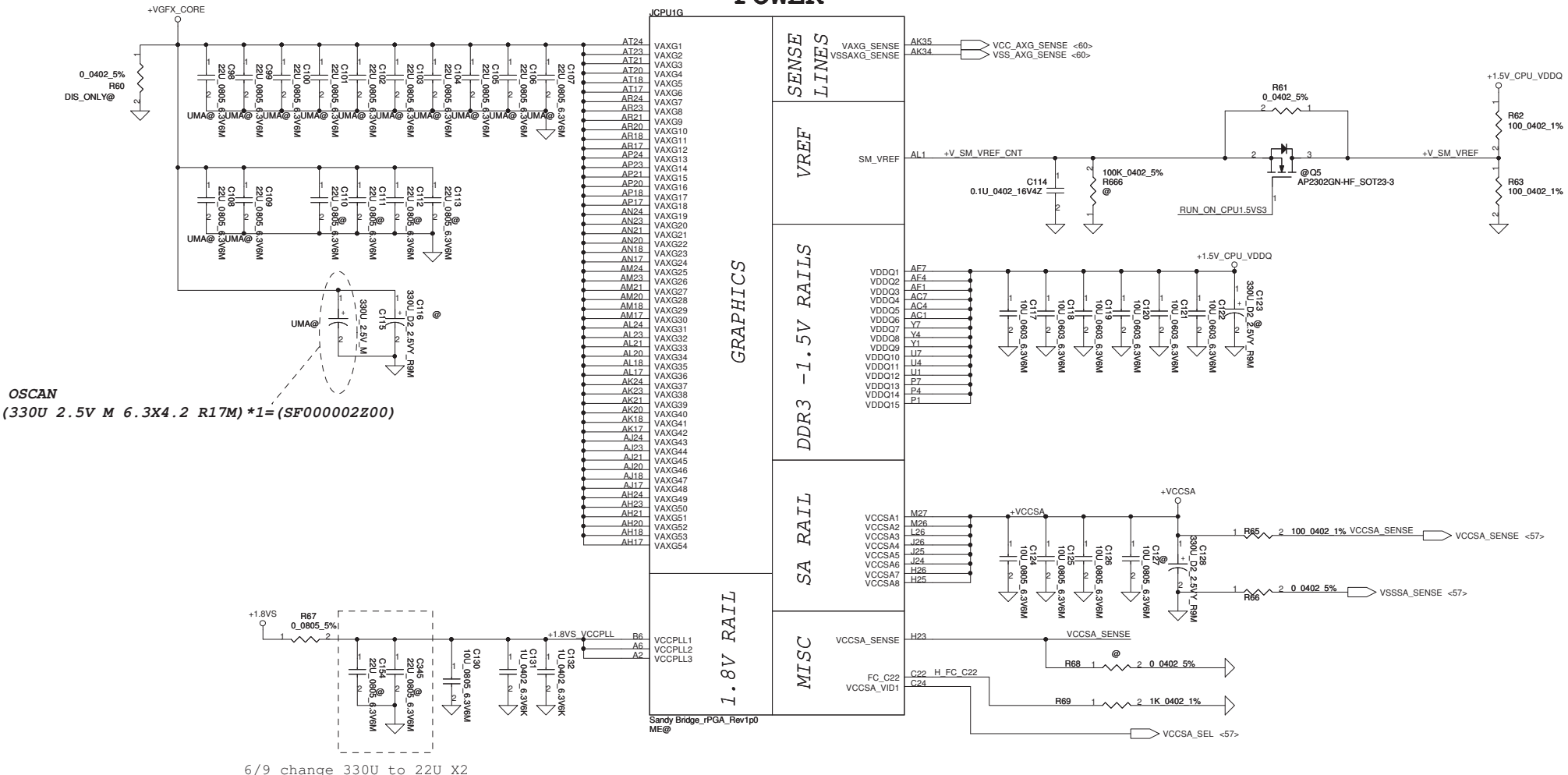
PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

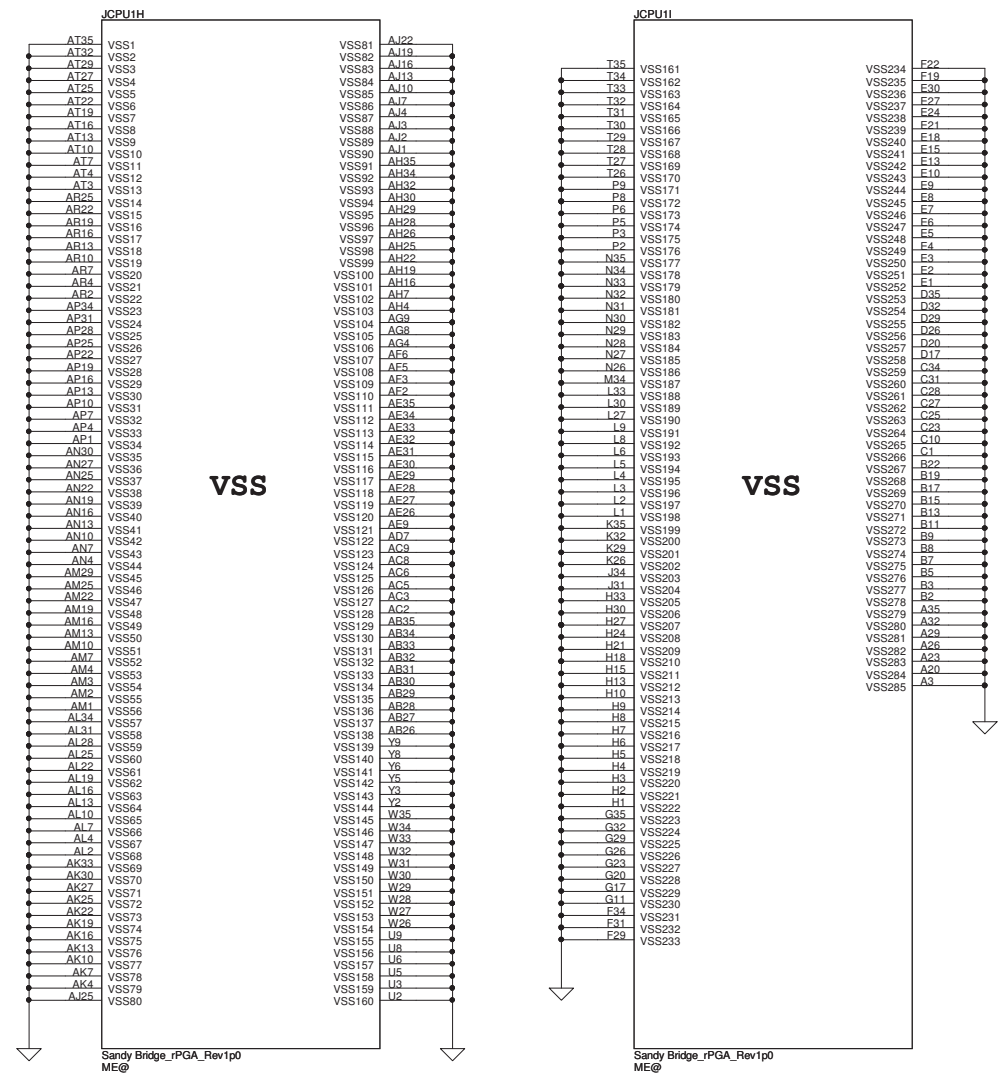




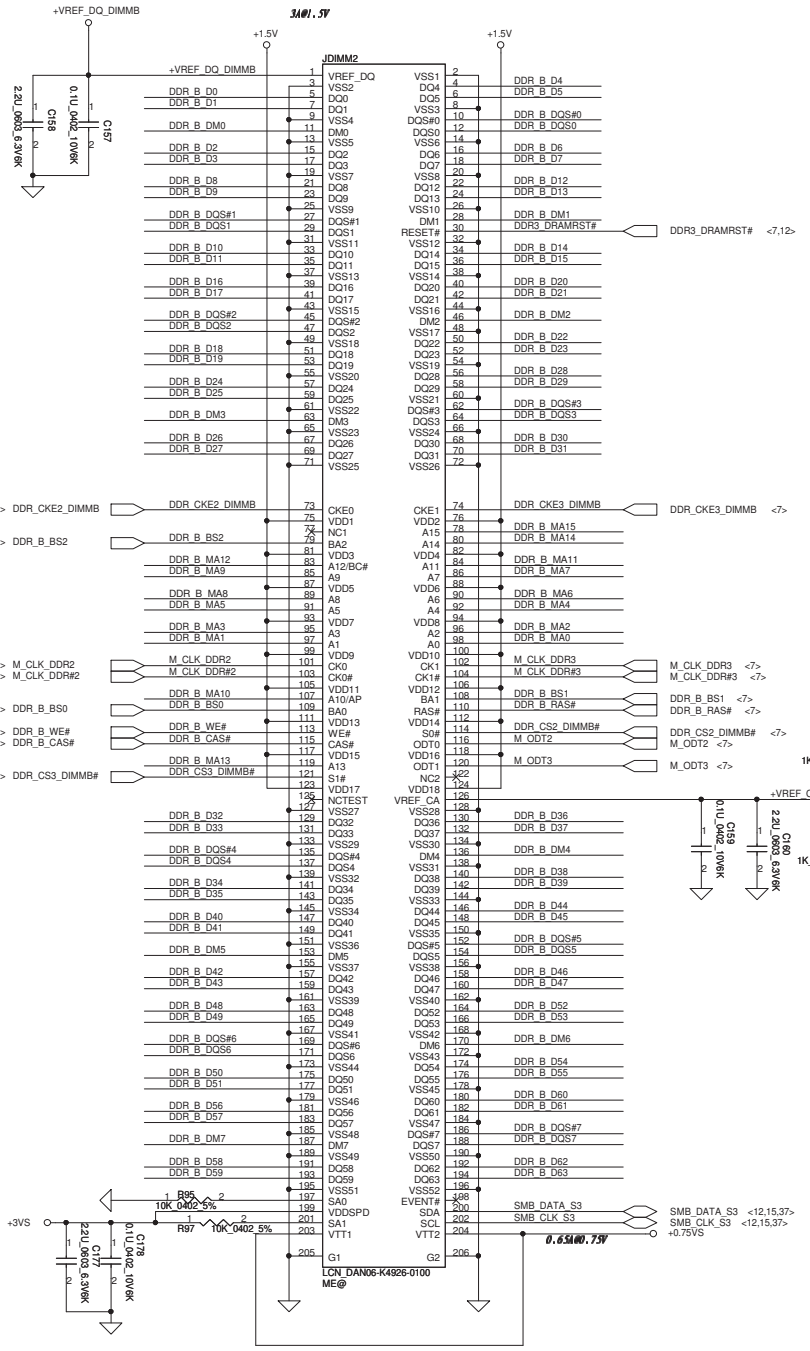
POWER



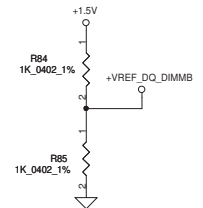
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Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title PROCESSOR(6/7) PWR	
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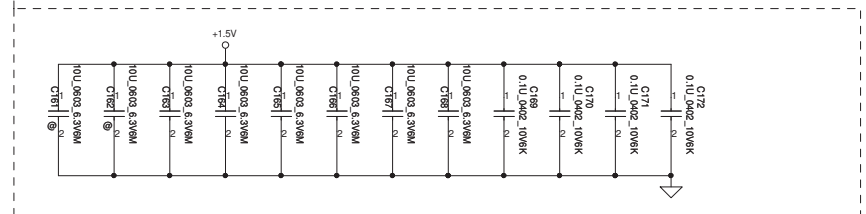


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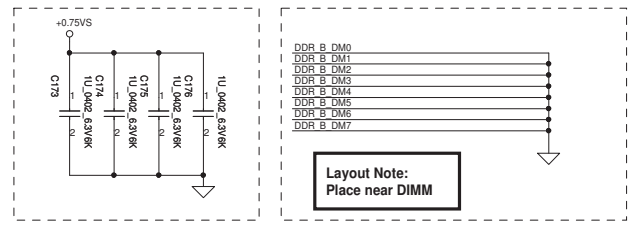


Layout Note:
Place near DIMM

(10uF_0603_6.3V) *8
 (0.1uF_402_10V) *4

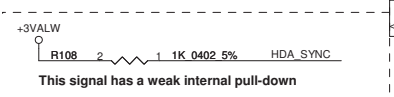
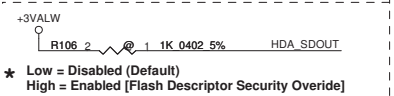
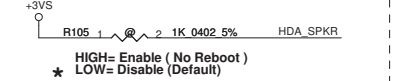
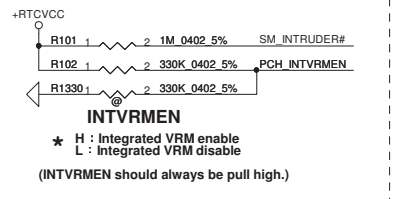
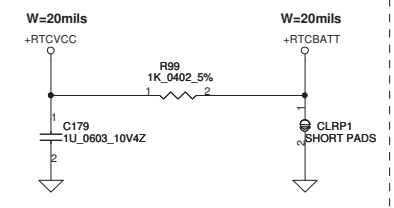


Layout Note:
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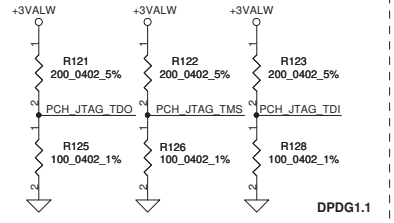
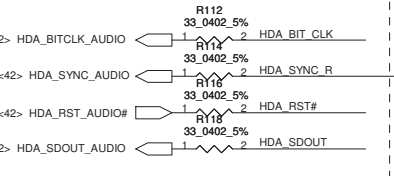


Layout Note:
Place near DIMM

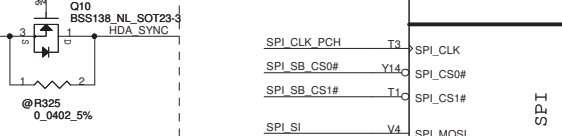
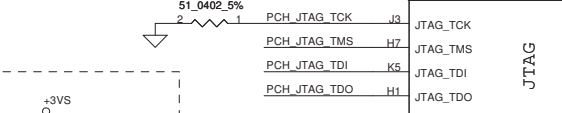
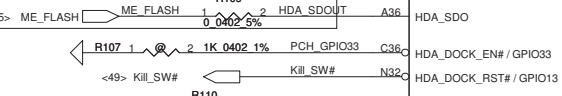
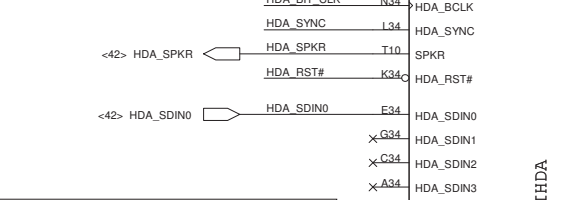
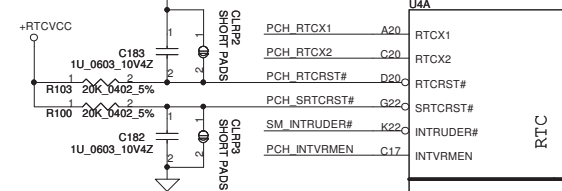
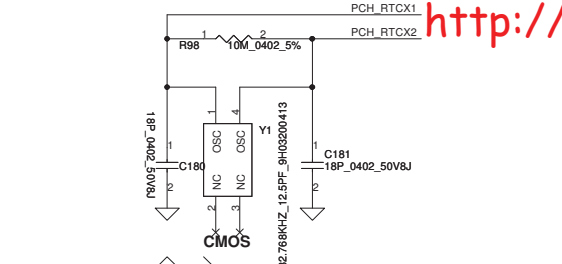
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Issued Date	2008/10/31	Deciphered Date	2009/10/31	DDRIII-SODIMM SLOT2	
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On Die PLL VR Select is supplied by 1.5V when sampled high 1.8V when sampled low Needs to be pulled High for Huron River platform

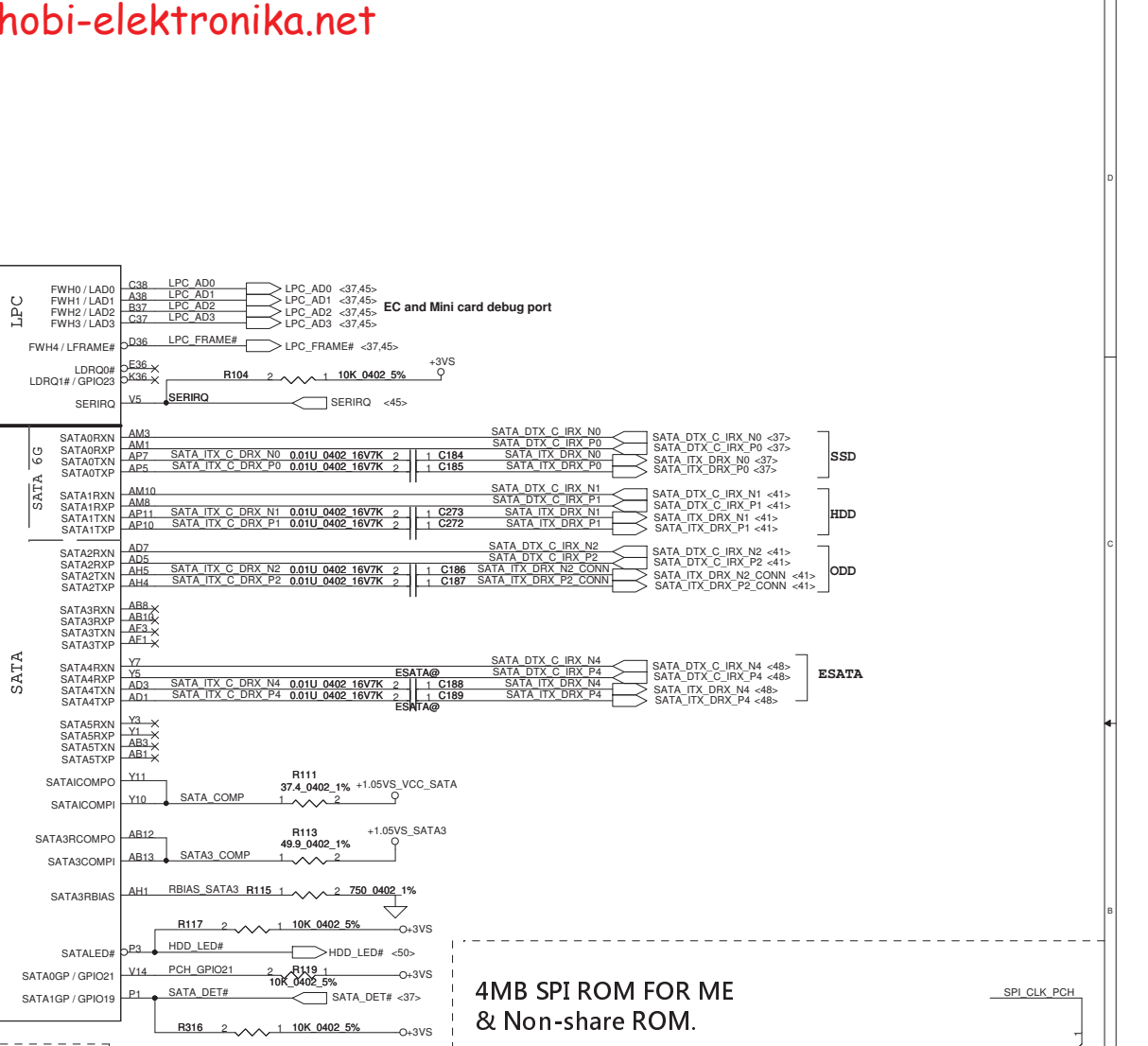
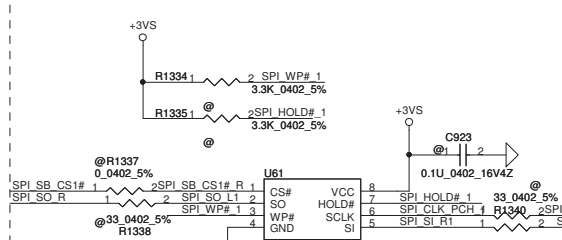


6/30 update R121, R122, R123

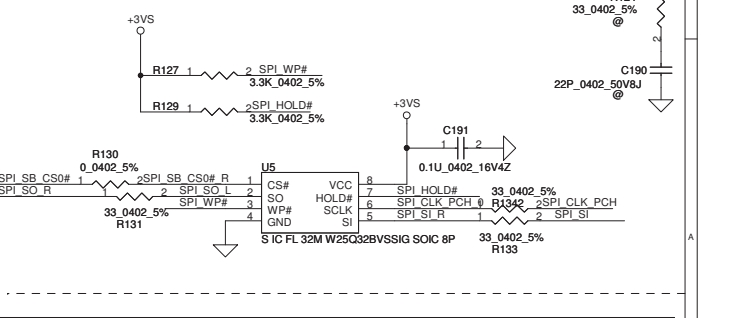


6/17 follow module design

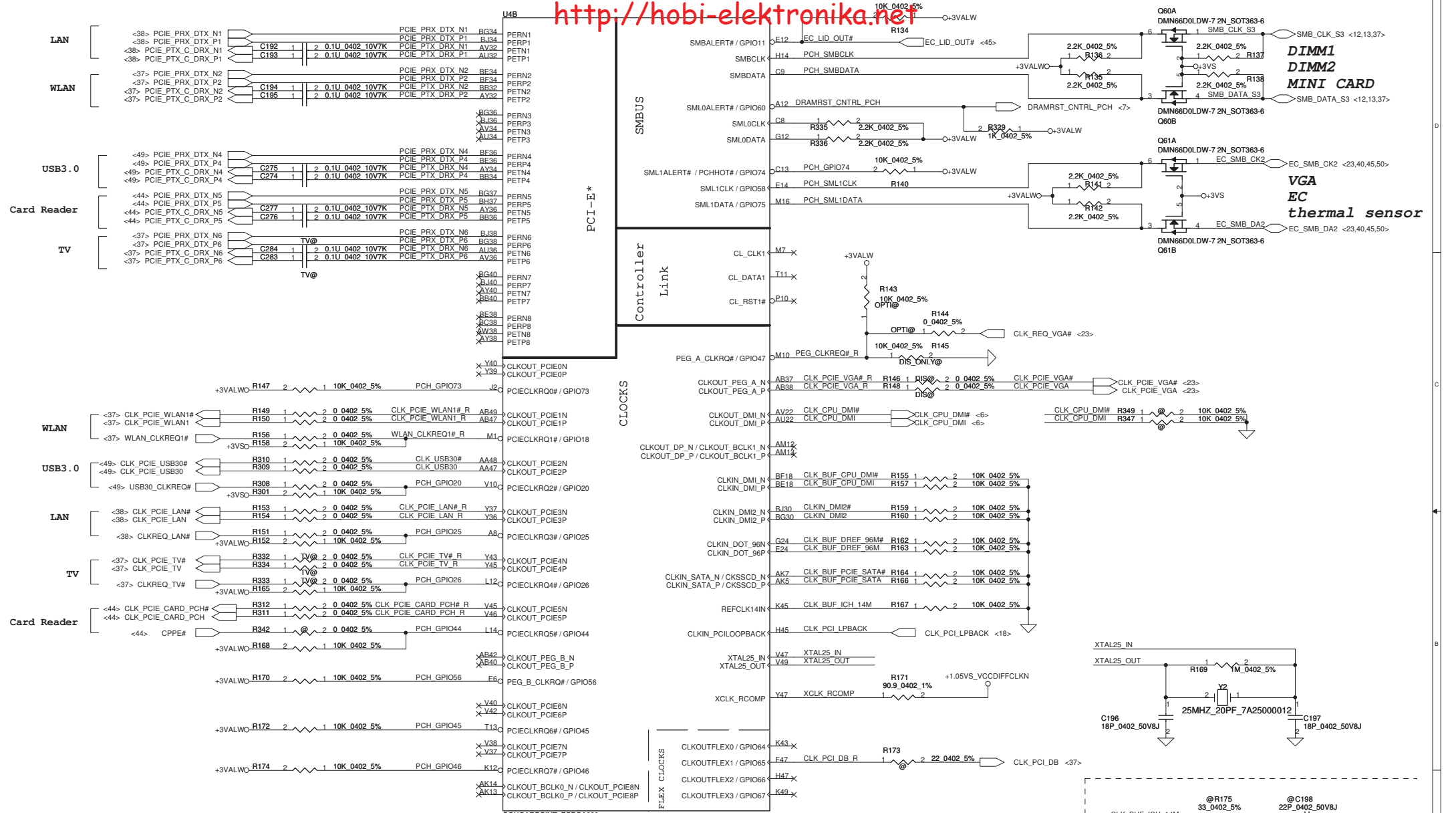
4MB SPI ROM FOR ME & Non-share ROM. For Fast Boot



4MB SPI ROM FOR ME & Non-share ROM.

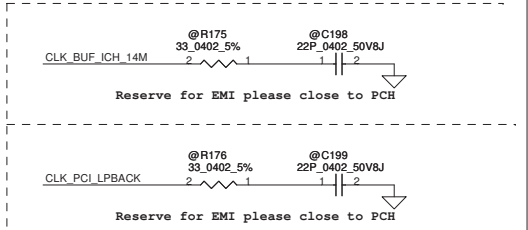


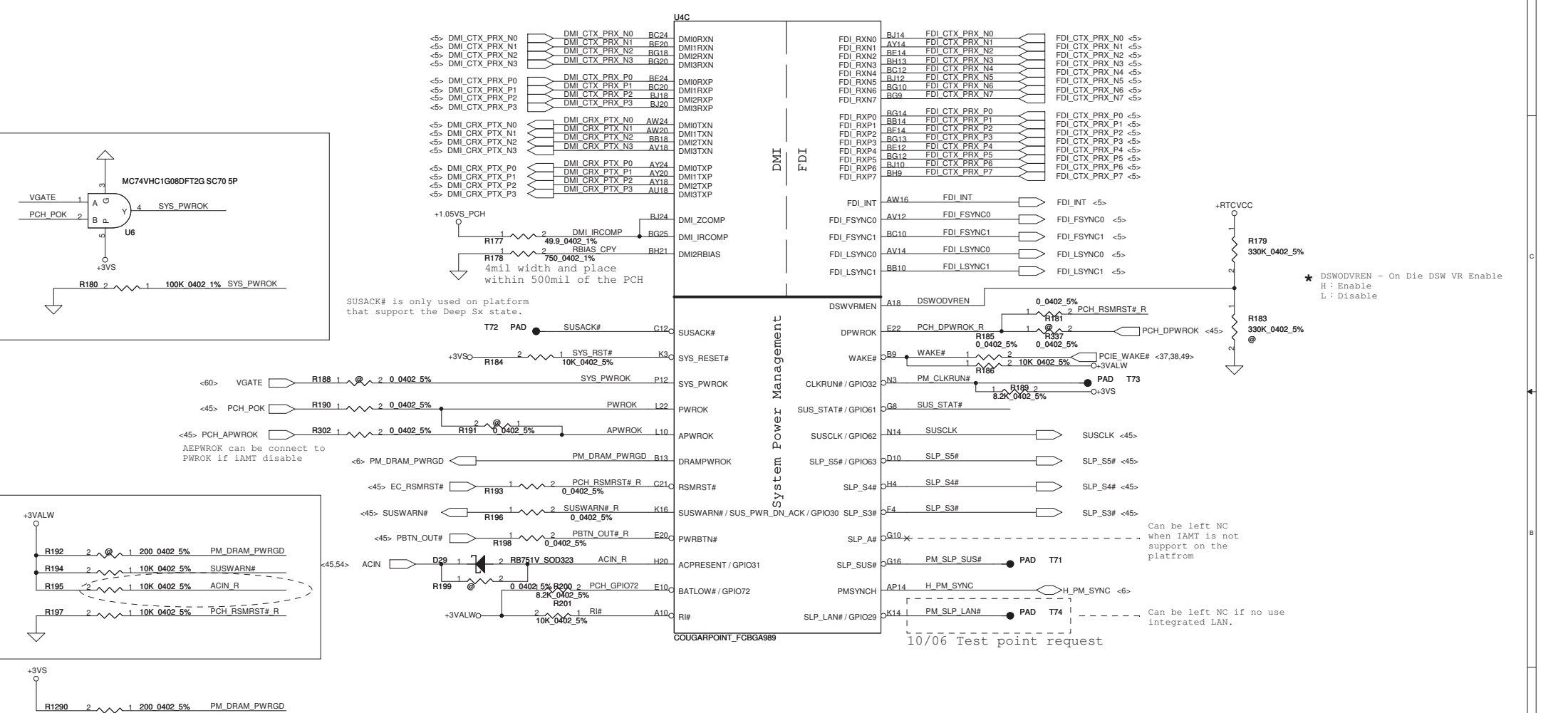
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Issued Date	2009/12/01	Deciphered Date	2010/12/31	Compal Electronics, Inc.
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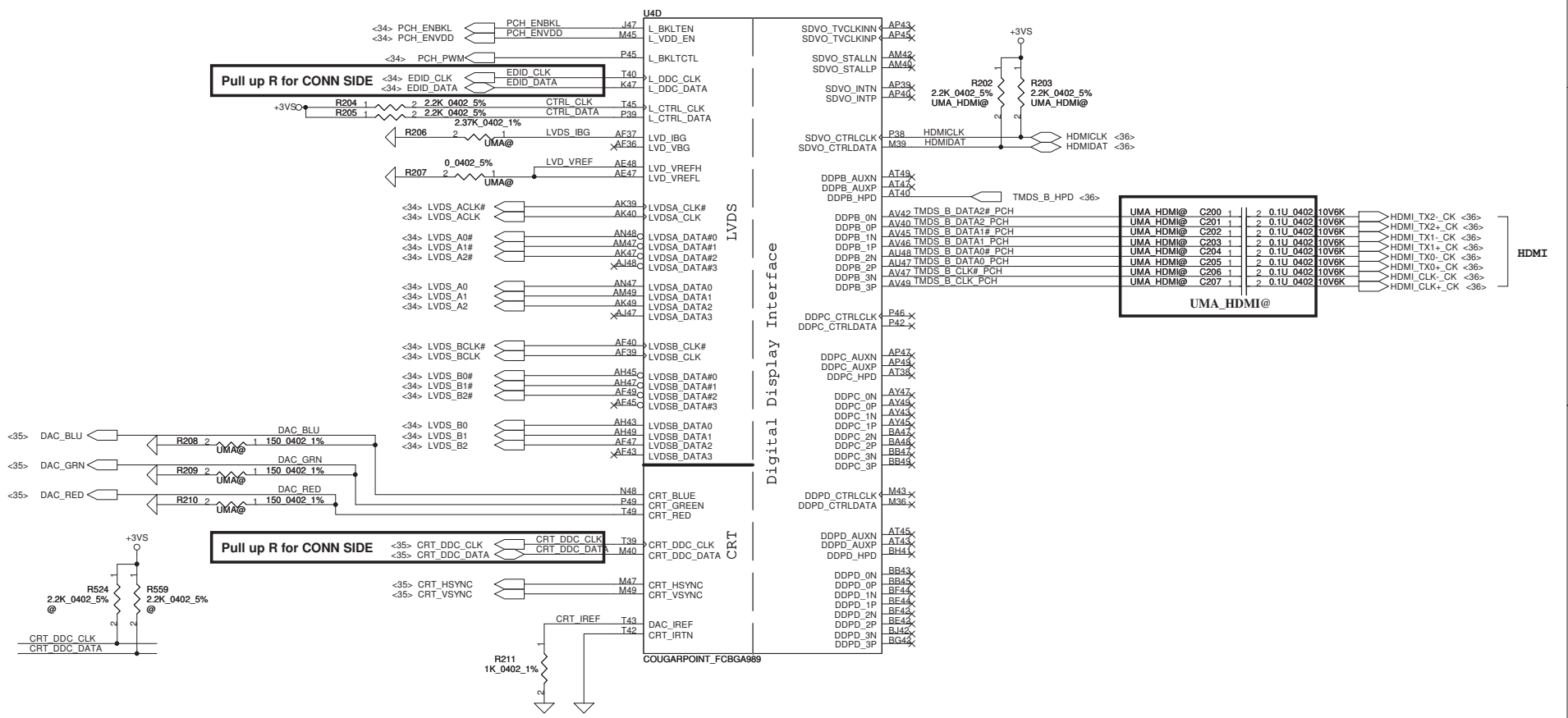
Compal Electronics, Inc.			
PCH (2/8) PCIE, SMBUS, CLK			
Title	Document Number	Rev	0.2
	LA-6882P		
Date:	Wednesday, October 06, 2010	Sheet	15 of 63



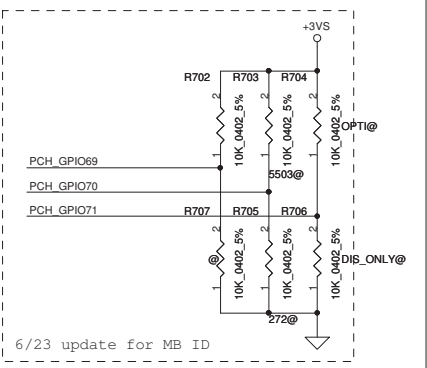


7/28 Modify follow Module Design.

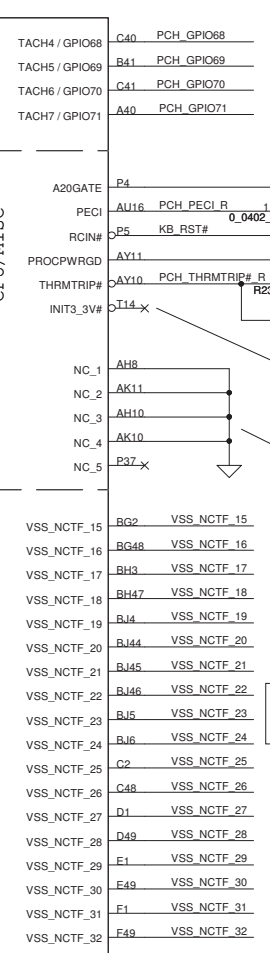
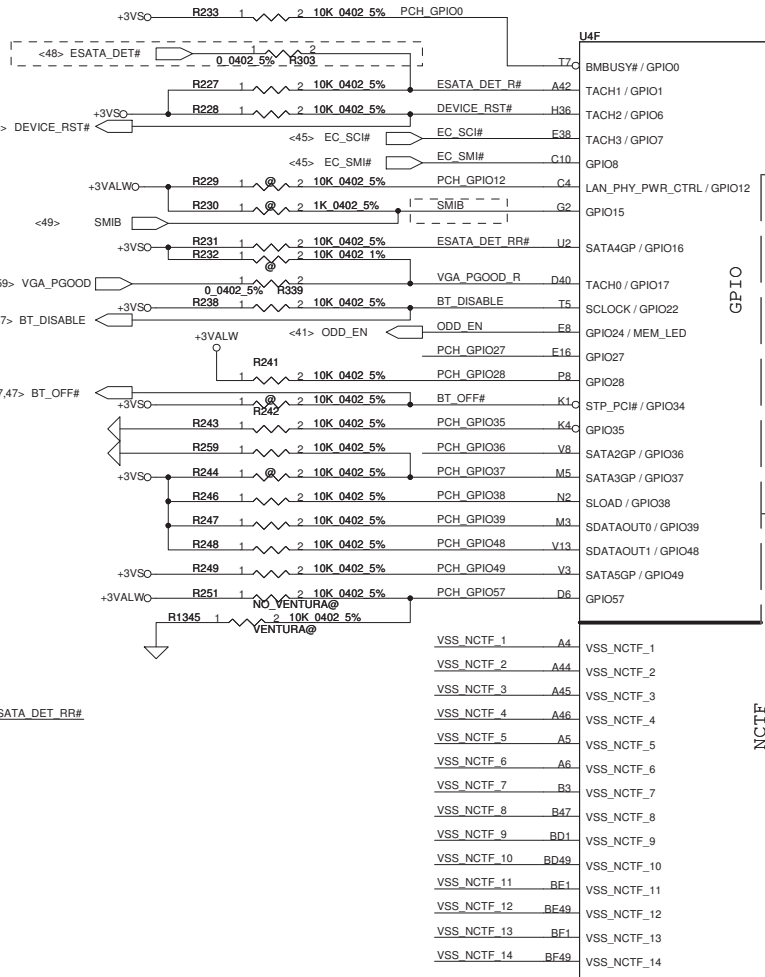
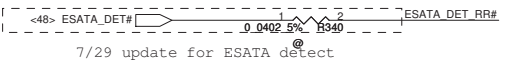
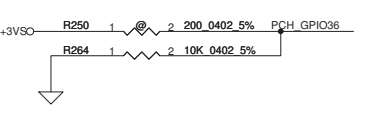
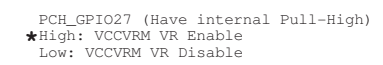
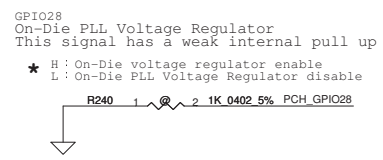
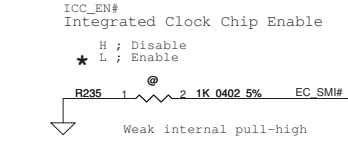
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GPIO69	GPIO70	GPIO71
15": Hi	ALC272: Low ALC5503: Hi	DIS ONLY: Low OPTIMUS: Hi
1	0	0
1	0	1
1	1	0
1	1	1



6/24 Change to @ follow module design and double check on module design meeting

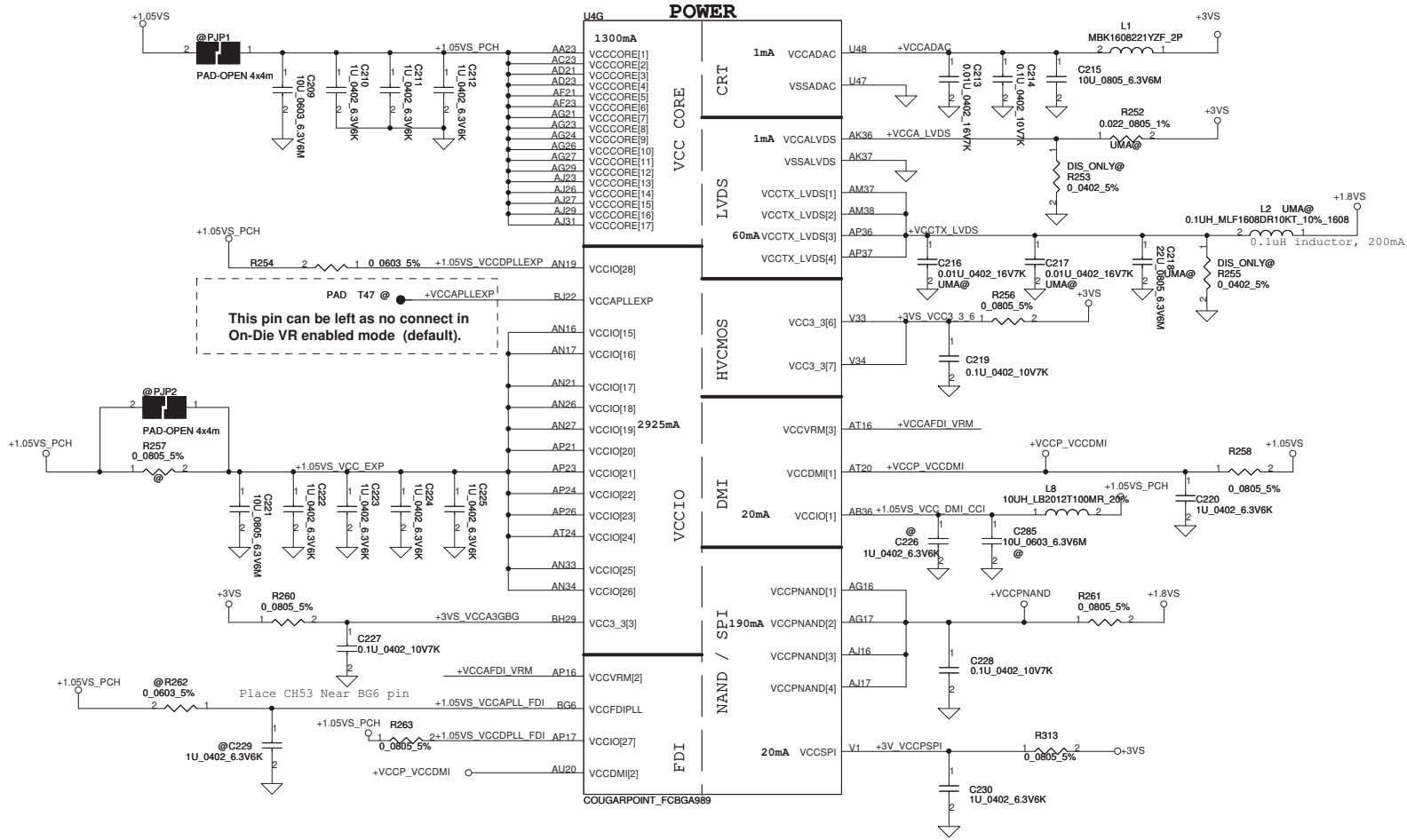


INIT3_3V
This signal has weak internal PU, can't pull low

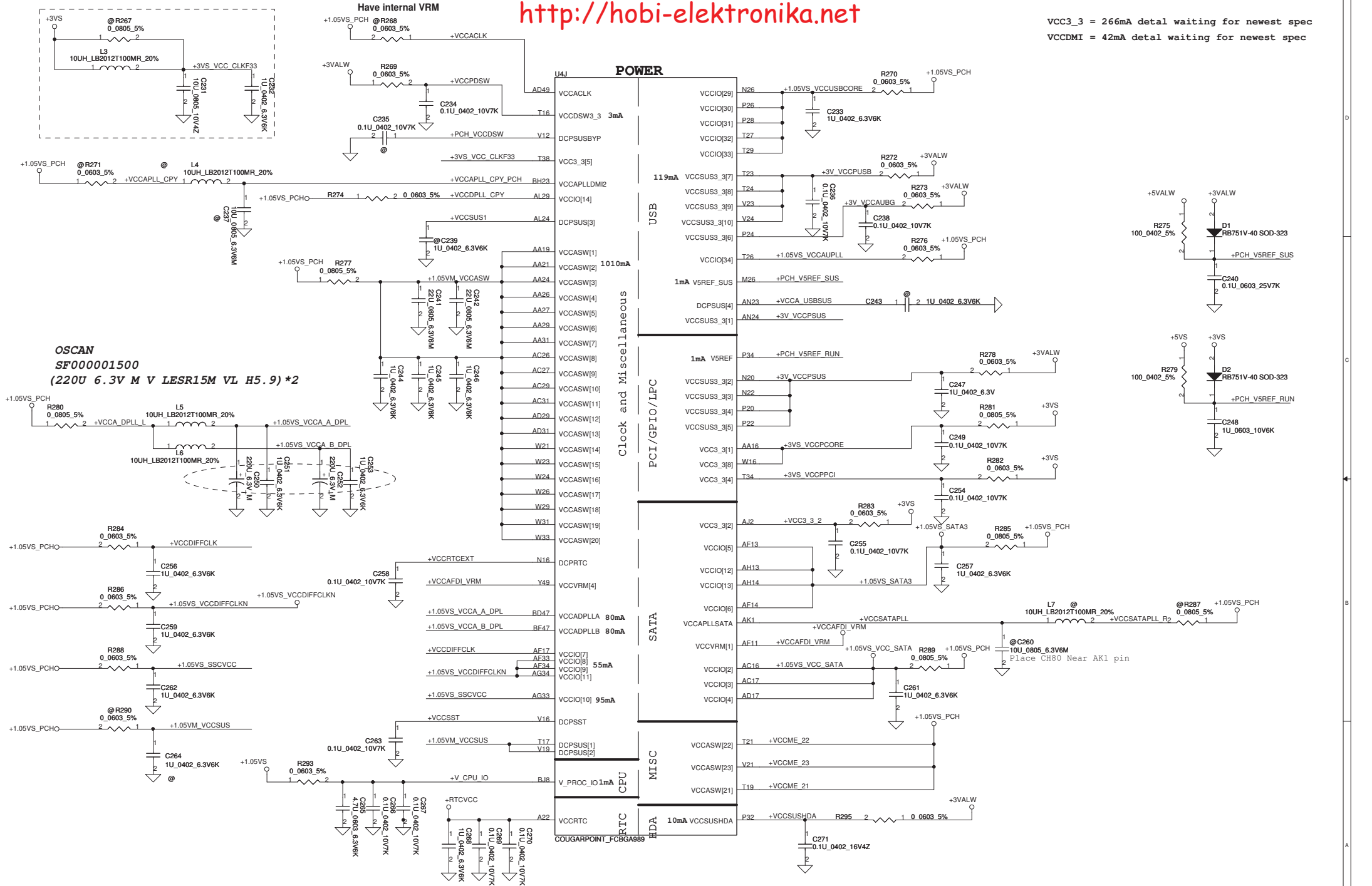
Intel schematic review recommend.

Change VSS_NCTF pin from TEST point to Trace for layout SPACE reducing..

COUGARPOINT_FCBGA989

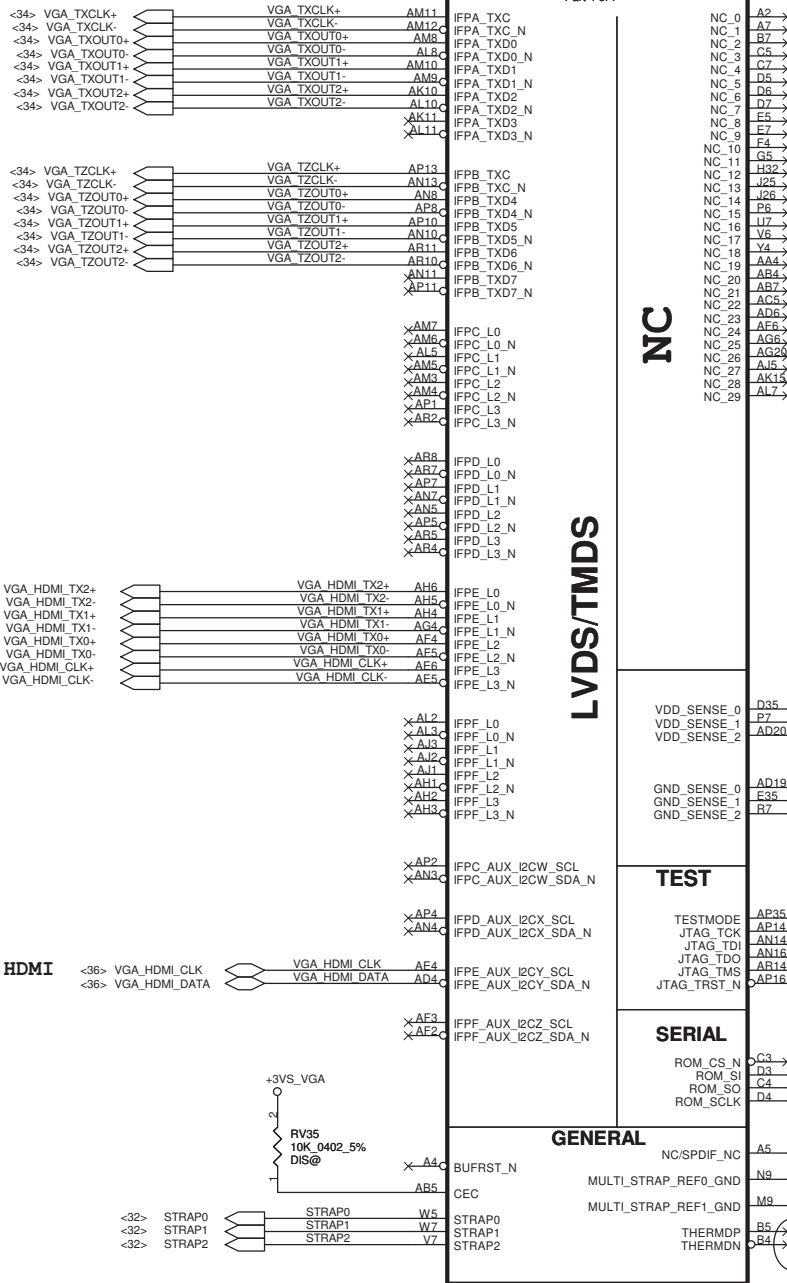


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



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PCH (8/9) PWR			
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NC

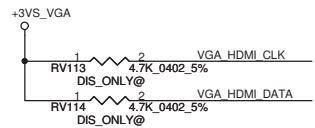
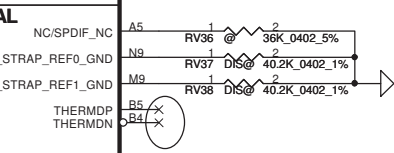
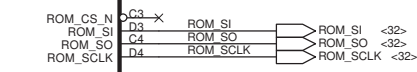
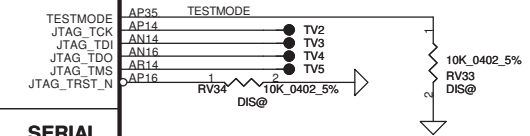
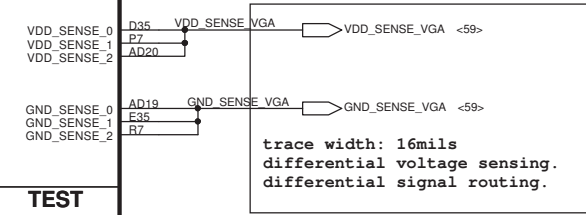
LVDS/TMDS

TEST

SERIAL

GENERAL

N12P-GT1-A1_BGA_973P DIS@



HDMI

+3VS_VGA

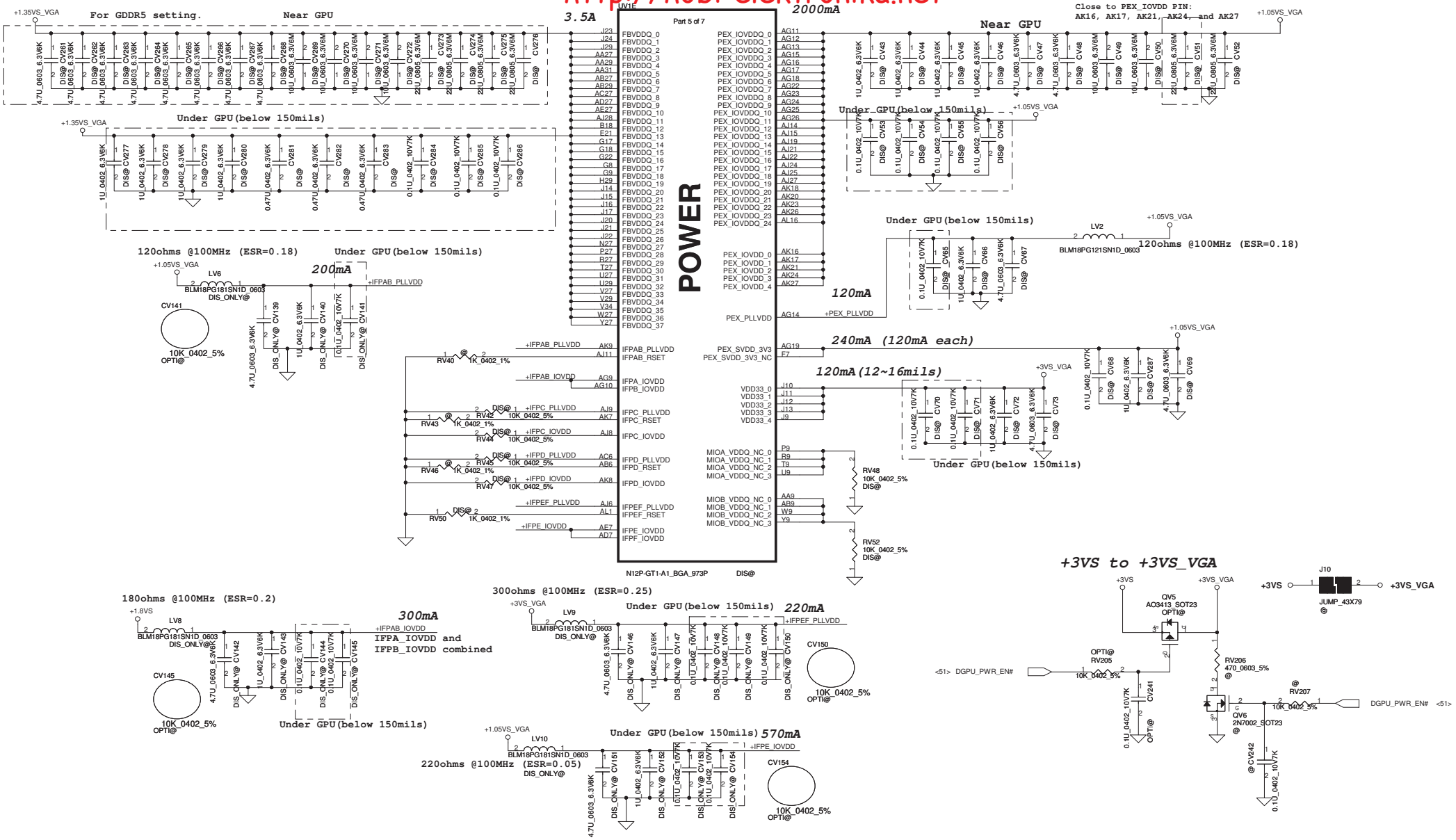
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Size	Document Number	Rev	Date: Wednesday, October 06, 2010 Sheet 24 of 63	
	LA-6882P	0.2		

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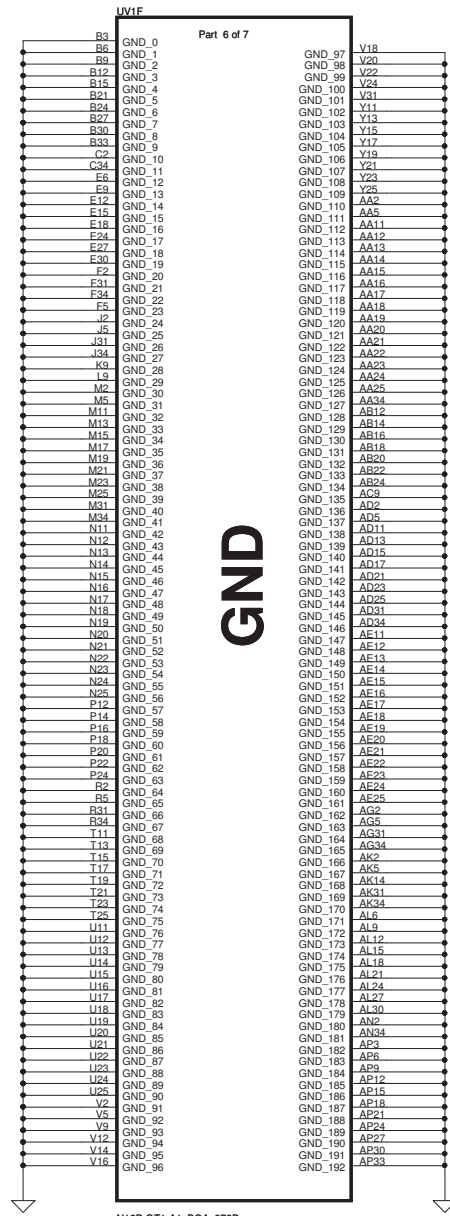
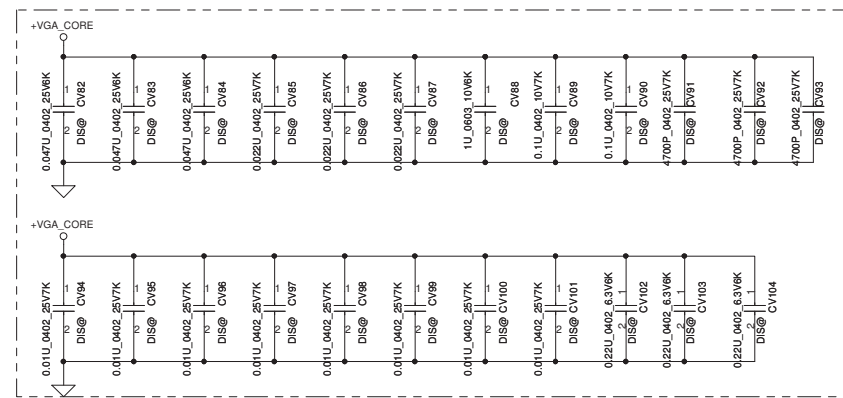
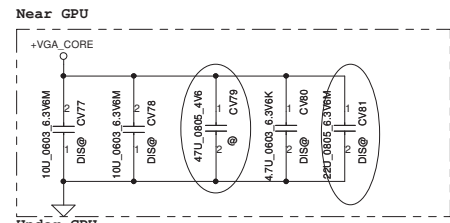
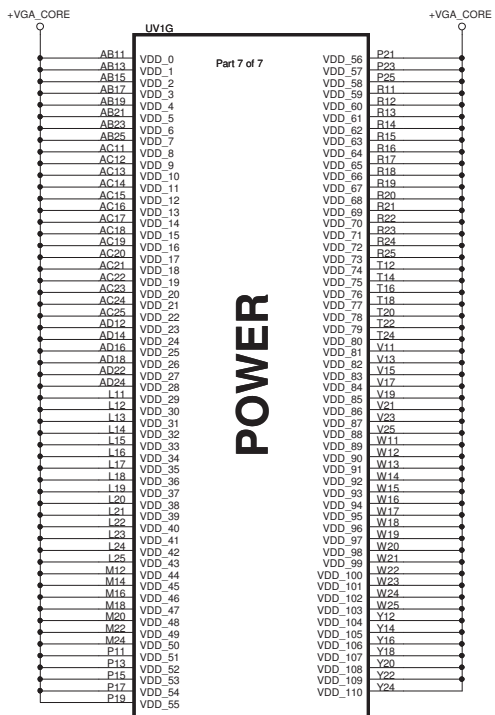
N12P-LVDS/HDMI/DP/THM

LA-6882P

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Size	Document Number	Rev		0.2	
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N12P-GT1-A1_BGA_973P

DIS@

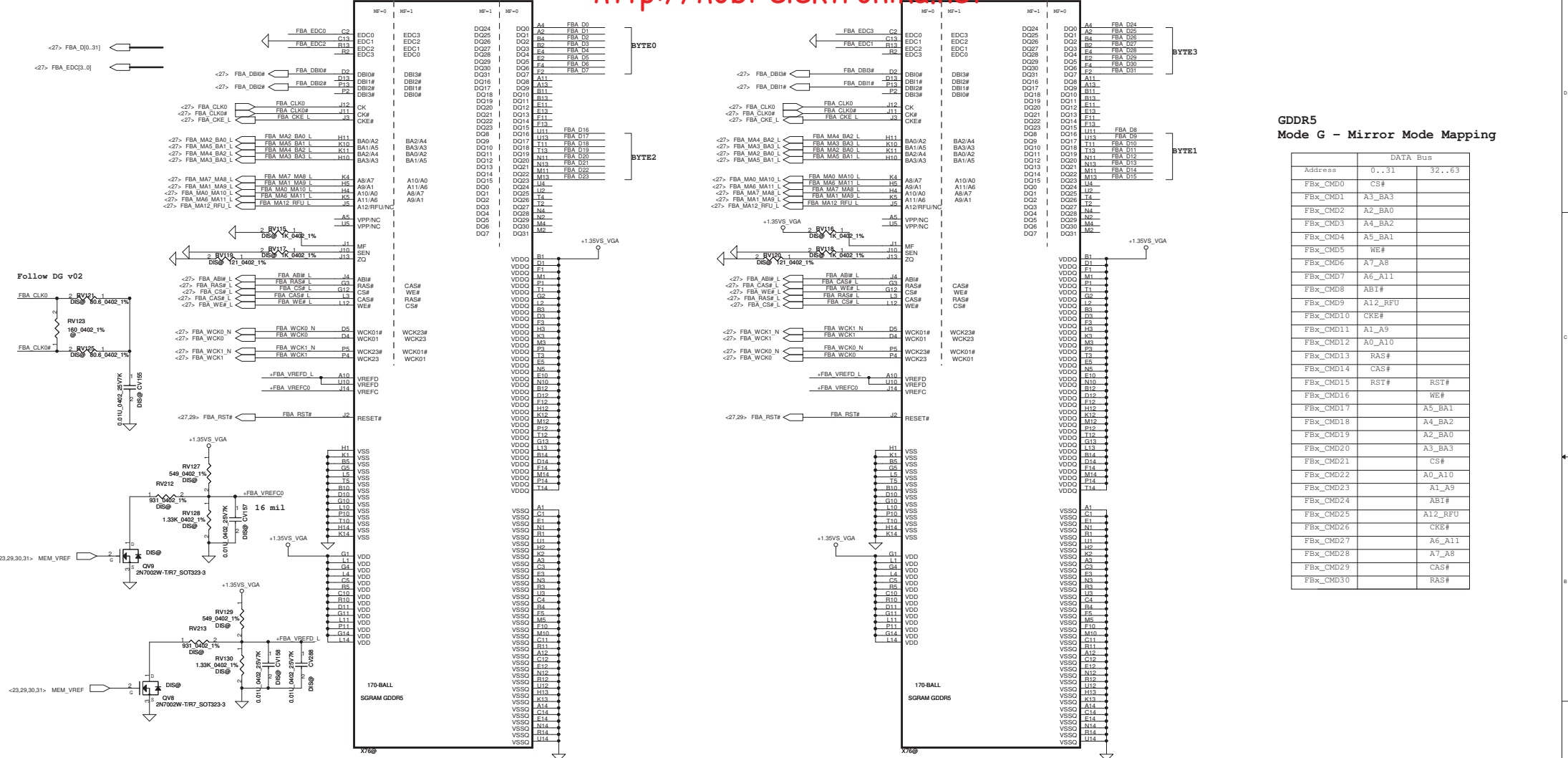
N12P-GT1-A1_BGA_973P

DIS@

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Size	Document Number	Rev		Date	
	LA-6882P	0.2		Wednesday, October 06, 2010	
		Sheet	26	of 63	

Memory Partition A - Lower 32 bits

<http://hobi-elektronika.net>



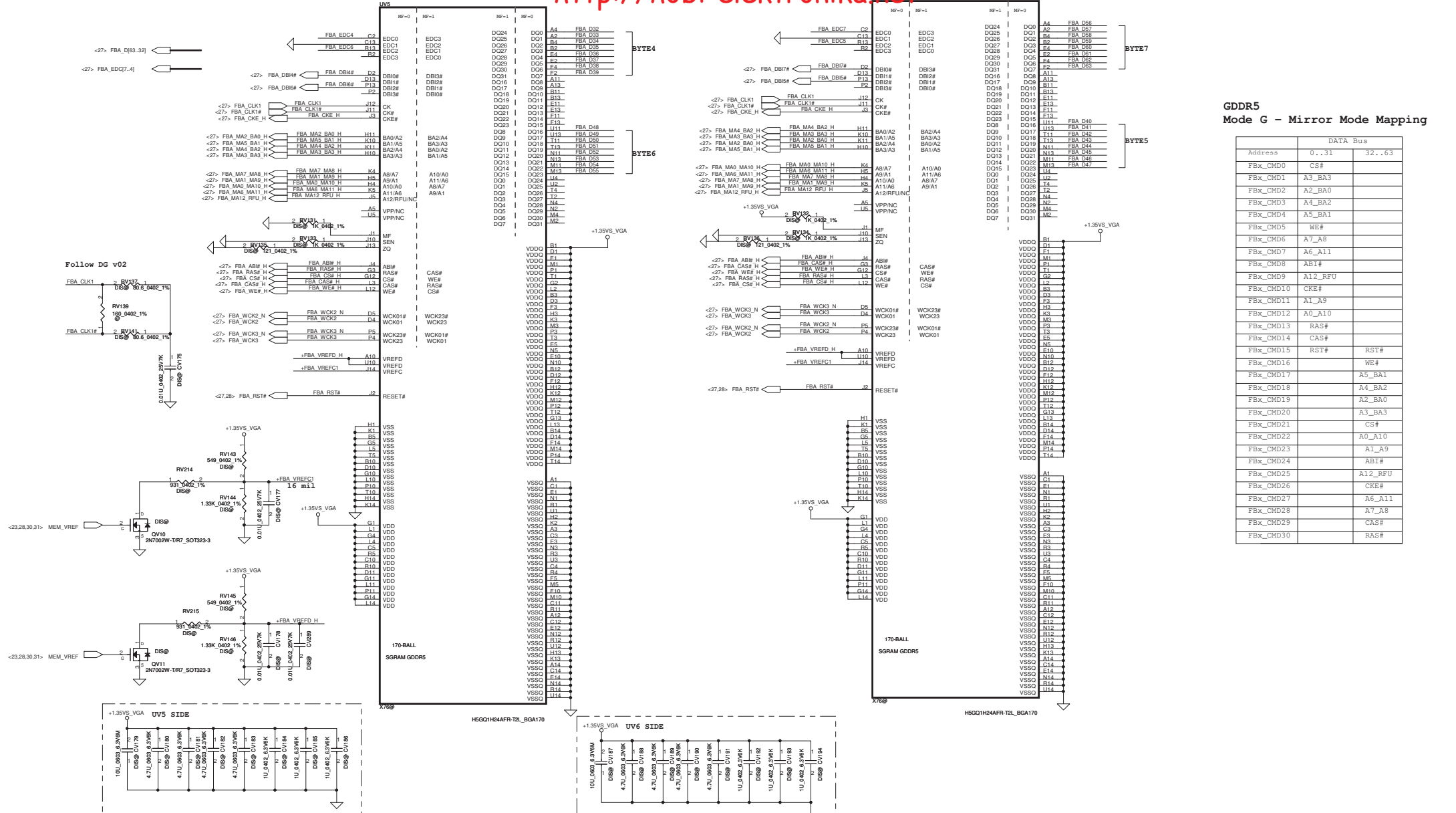
GDDR5
Mode G - Mirror Mode Mapping

Address	DATA Bus
0..31	32..63
Fbx_CMD0	CS#
Fbx_CMD1	A3_BA3
Fbx_CMD2	A2_BA0
Fbx_CMD3	A4_BA2
Fbx_CMD4	A5_BA1
Fbx_CMD5	WE#
Fbx_CMD6	A7_A8
Fbx_CMD7	A6_A11
Fbx_CMD8	AB1#
Fbx_CMD9	A12_RFU
Fbx_CMD10	CKE#
Fbx_CMD11	A1_A9
Fbx_CMD12	A0_A10
Fbx_CMD13	RAS#
Fbx_CMD14	CAS#
Fbx_CMD15	RST#
Fbx_CMD16	WE#
Fbx_CMD17	A5_BA1
Fbx_CMD18	A4_BA2
Fbx_CMD19	A2_BA0
Fbx_CMD20	A3_BA3
Fbx_CMD21	CS#
Fbx_CMD22	A0_A10
Fbx_CMD23	A1_A9
Fbx_CMD24	AB1#
Fbx_CMD25	A12_RFU
Fbx_CMD26	CKE#
Fbx_CMD27	A6_A11
Fbx_CMD28	A7_A8
Fbx_CMD29	CAS#
Fbx_CMD30	RAS#

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Title N12P-VRAM A Lower		File LA-6882P	
Size	Document Number	Rev	
		0.2	
Date	Wednesday, October 06, 2010	Sheet 28 of 63	

Memory Partition A - Upper 32 bits

<http://hobi-elektronika.net>

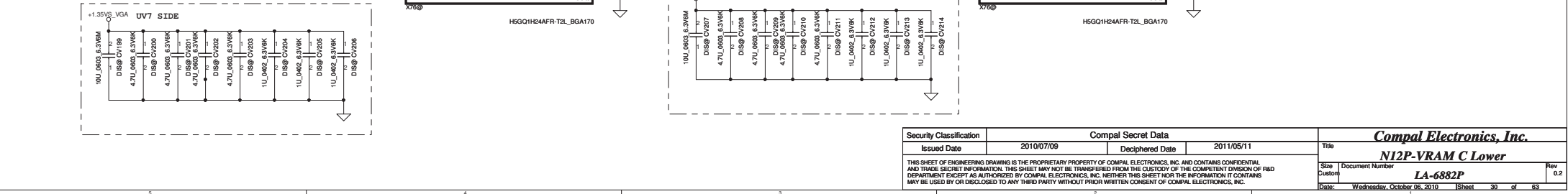
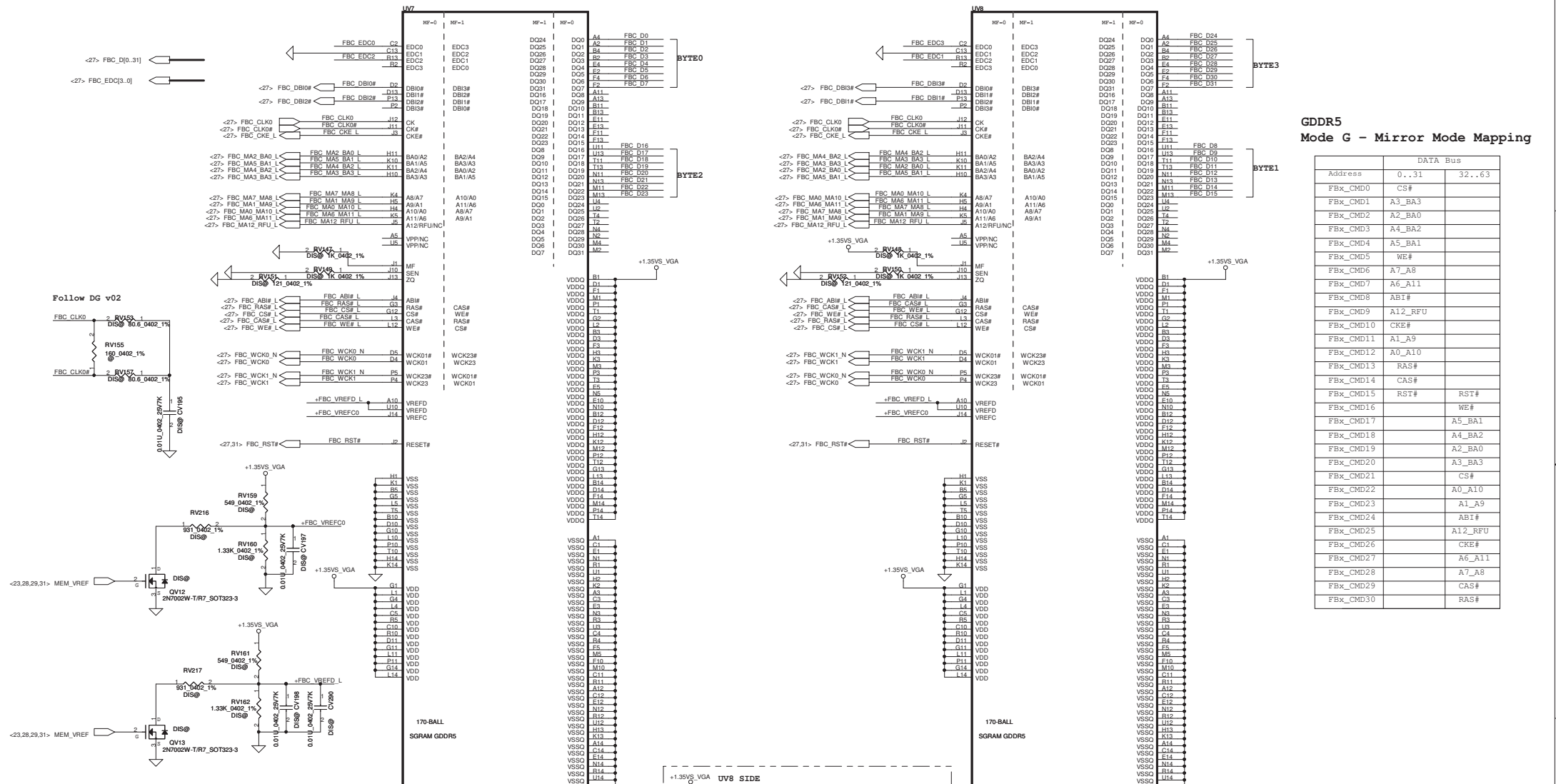


GDDR5 Mode G - Mirror Mode Mapping

Address	DATA Bus
FbX_CMD0	CS#
FbX_CMD1	A3_BA3
FbX_CMD2	A2_BA0
FbX_CMD3	A4_BA2
FbX_CMD4	A5_BA1
FbX_CMD5	WE#
FbX_CMD6	A7_A8
FbX_CMD7	A6_A11
FbX_CMD8	AB1#
FbX_CMD9	A12_RFU
FbX_CMD10	CKE#
FbX_CMD11	A1_A9
FbX_CMD12	A0_A10
FbX_CMD13	RAS#
FbX_CMD14	CAS#
FbX_CMD15	RST#
FbX_CMD16	WE#
FbX_CMD17	A5_BA1
FbX_CMD18	A4_BA2
FbX_CMD19	A2_BA0
FbX_CMD20	A3_BA3
FbX_CMD21	CS#
FbX_CMD22	A0_A10
FbX_CMD23	A1_A9
FbX_CMD24	AB1#
FbX_CMD25	A12_RFU
FbX_CMD26	CKE#
FbX_CMD27	A6_A11
FbX_CMD28	A7_A8
FbX_CMD29	CAS#
FbX_CMD30	RAS#

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N12P-VRAM A Upper	
Size	Document Number
	LA-682P
Date	Wednesday, October 06, 2010
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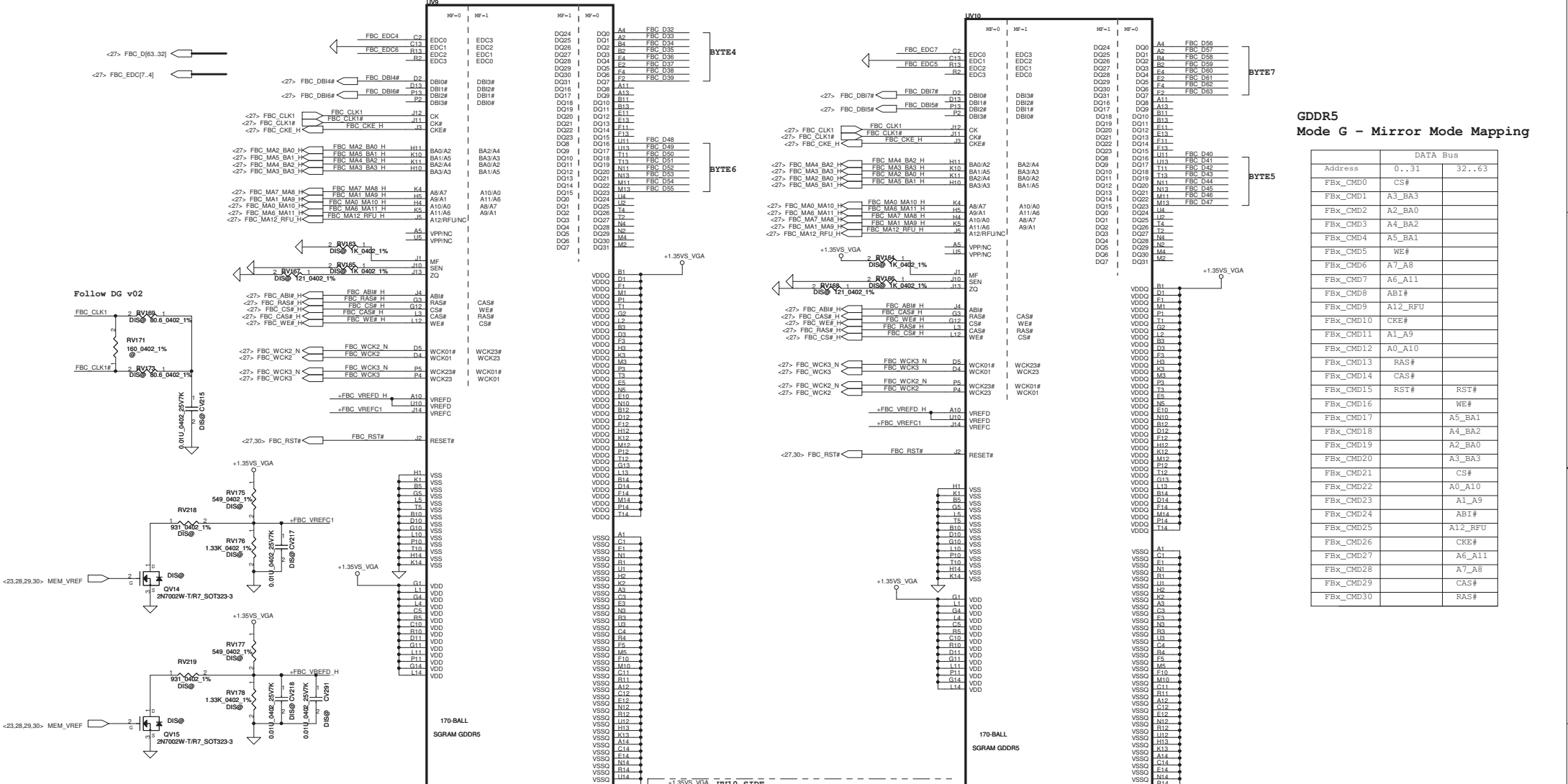
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Title N12P-VRAM C Lower			Size Document Number LA-6882P	
Date: Wednesday, October 08, 2010			Sheet 30 of 93	

Memory Partition C - Upper 32 bits

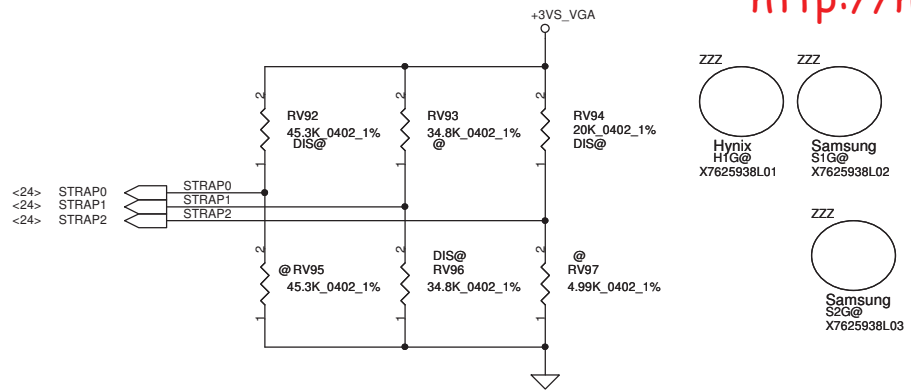
http://hobi-elektronika.net



GDDR5 Mode G - Mirror Mode Mapping

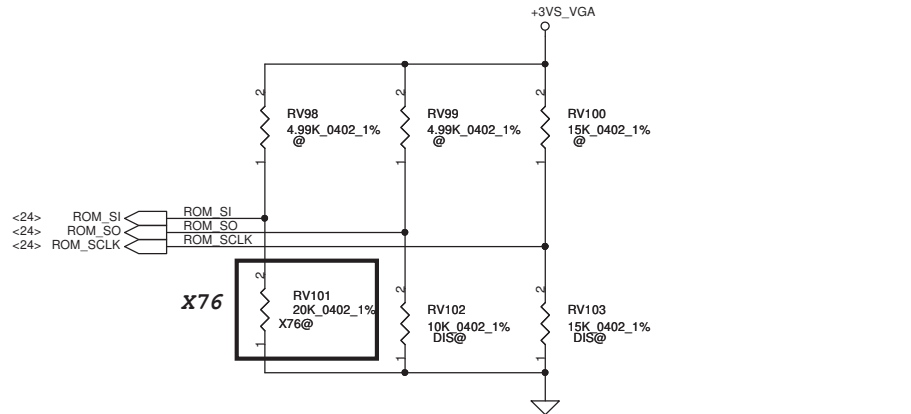
Address	DATA Bus
0..31	32..63
FBx_CMD0	CS#
FBx_CMD1	A3_BA3
FBx_CMD2	A2_BA0
FBx_CMD3	A4_BA2
FBx_CMD4	A5_BA1
FBx_CMD5	WE#
FBx_CMD6	A7_A8
FBx_CMD7	A6_A11
FBx_CMD8	ABI#
FBx_CMD9	A12_RFU
FBx_CMD10	CKE#
FBx_CMD11	A1_A9
FBx_CMD12	A0_A10
FBx_CMD13	RAS#
FBx_CMD14	CAS#
FBx_CMD15	RST#
FBx_CMD16	WE#
FBx_CMD17	A5_BA1
FBx_CMD18	A4_BA2
FBx_CMD19	A2_BA0
FBx_CMD20	A3_BA3
FBx_CMD21	CS#
FBx_CMD22	A0_A10
FBx_CMD23	A1_A9
FBx_CMD24	ABI#
FBx_CMD25	A12_RFU
FBx_CMD26	CKE#
FBx_CMD27	A6_A11
FBx_CMD28	A7_A8
FBx_CMD29	CAS#
FBx_CMD30	RAS#

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Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0		
ROM_SO	+3VS_VGA	XCCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



GPU	FB Memory (GDDR5)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N12P-GT1	Samsung 1800MHz (default)	K4G10325FE-HC04					
		PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 1600MHz	H5GQ1H24AFR-T2L					
		PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
				X76			

SUB_VENDOR		XCCLK_417	
0	No VBIOS ROM	0	277MHz (Default)
1	BIOS ROM is present (Default)	1	Reserved

FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User[3:0]	
1	Reserved	1000-1100	Customer defined

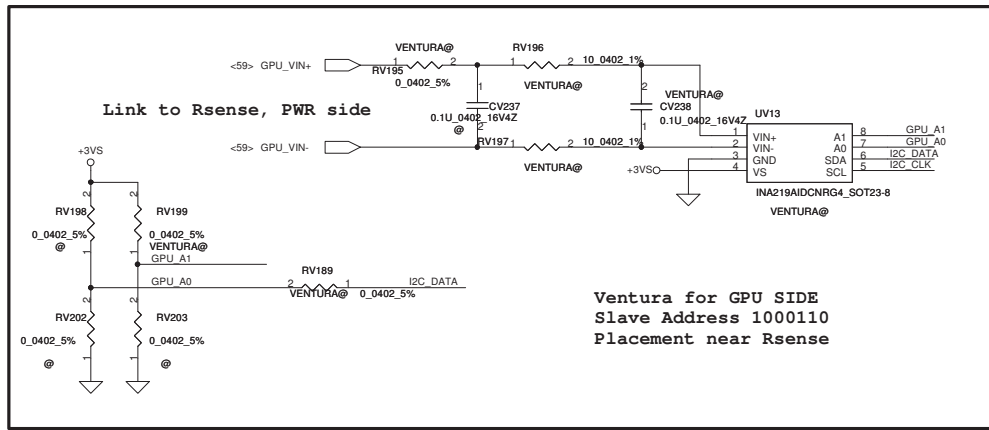
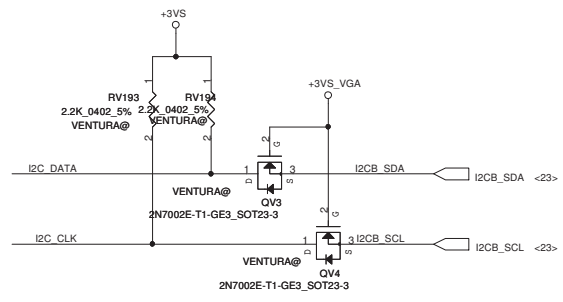
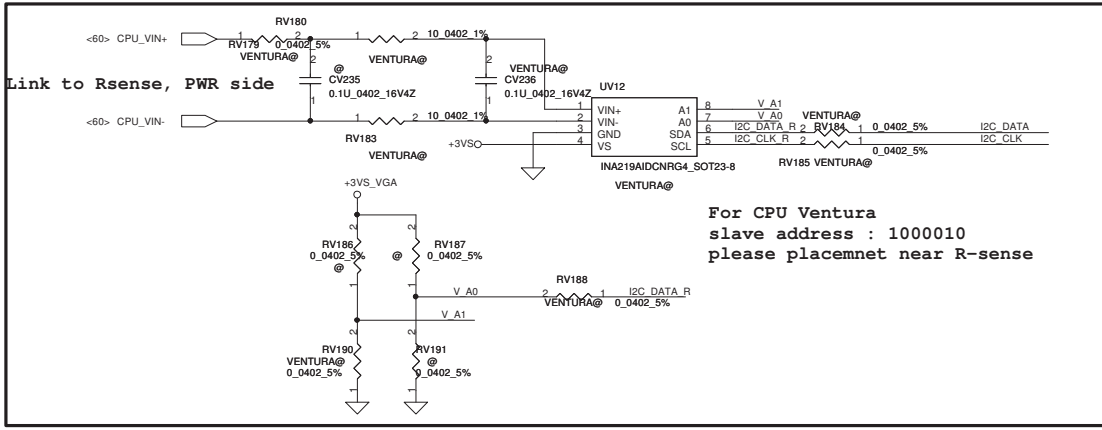
3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
0110	Notebook Default	1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

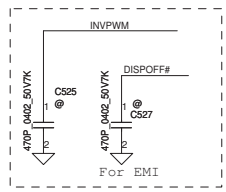
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device (Class Code 302h)
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

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				N12P MISC		
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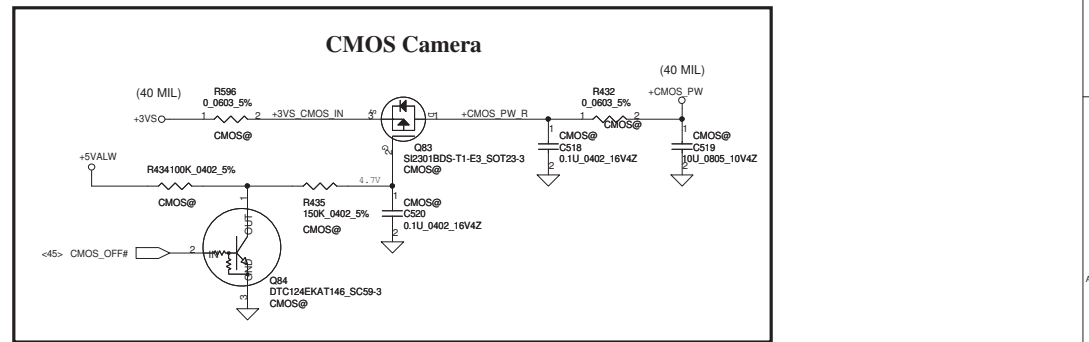
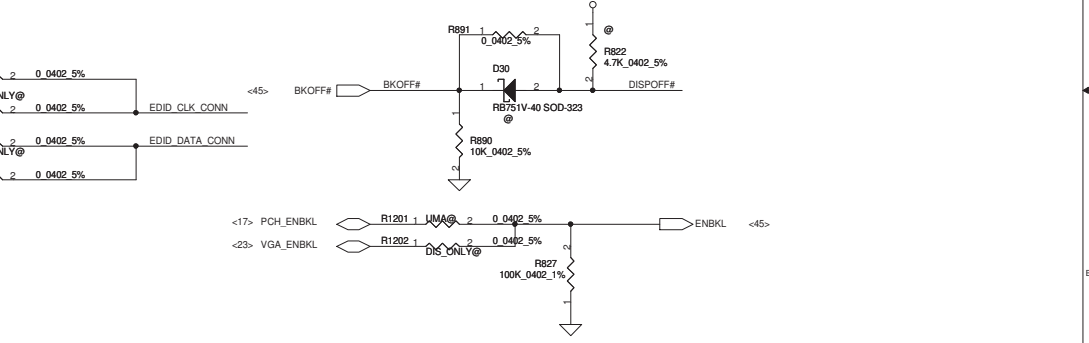
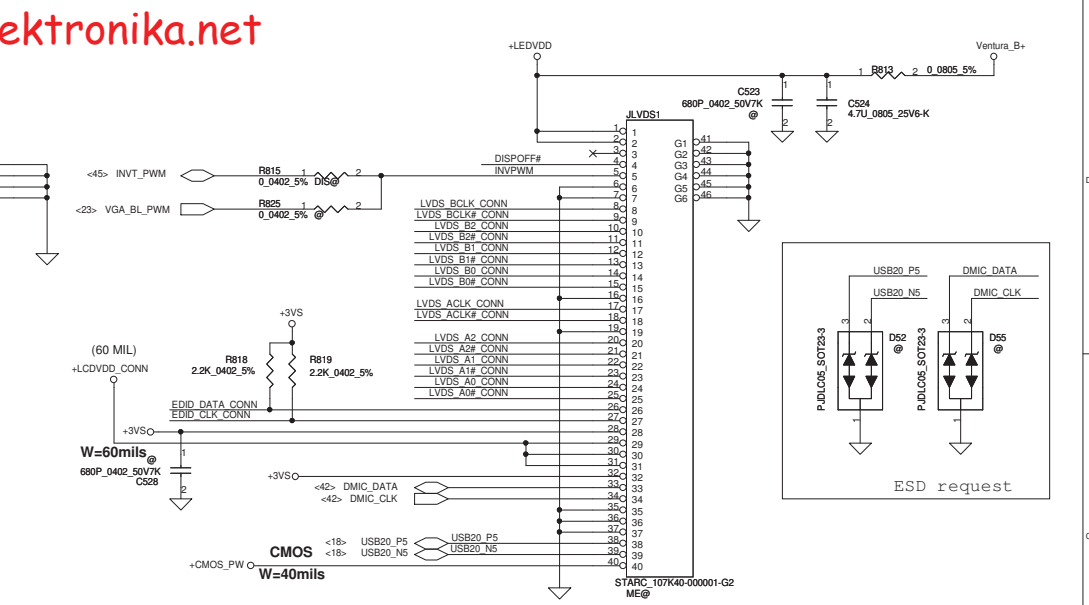
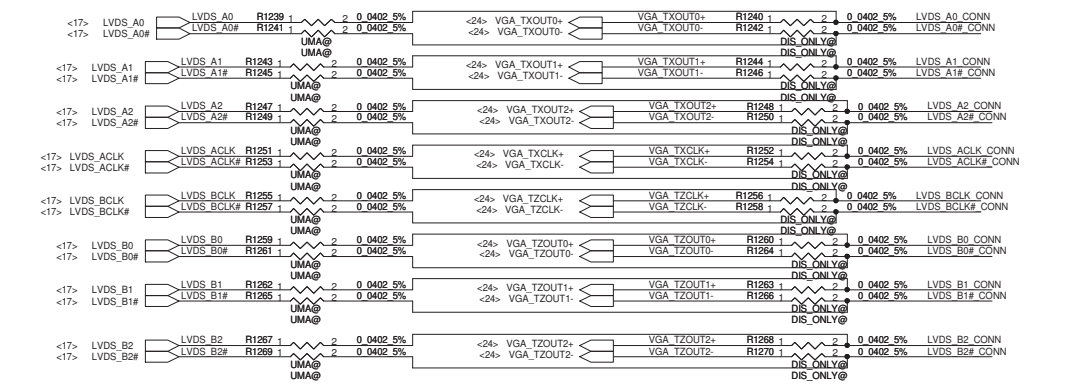
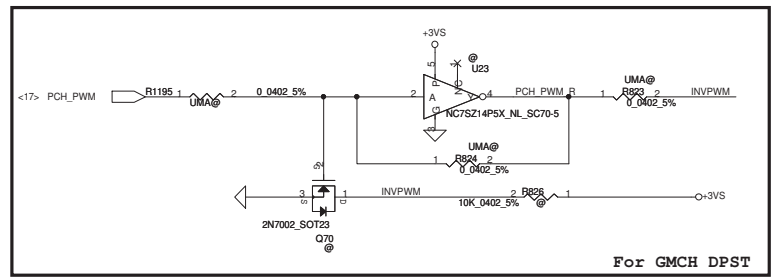
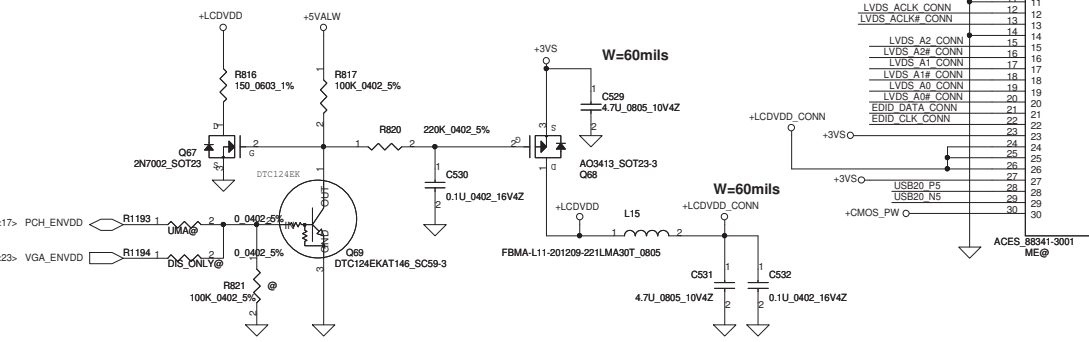
TOP side (under inductor)



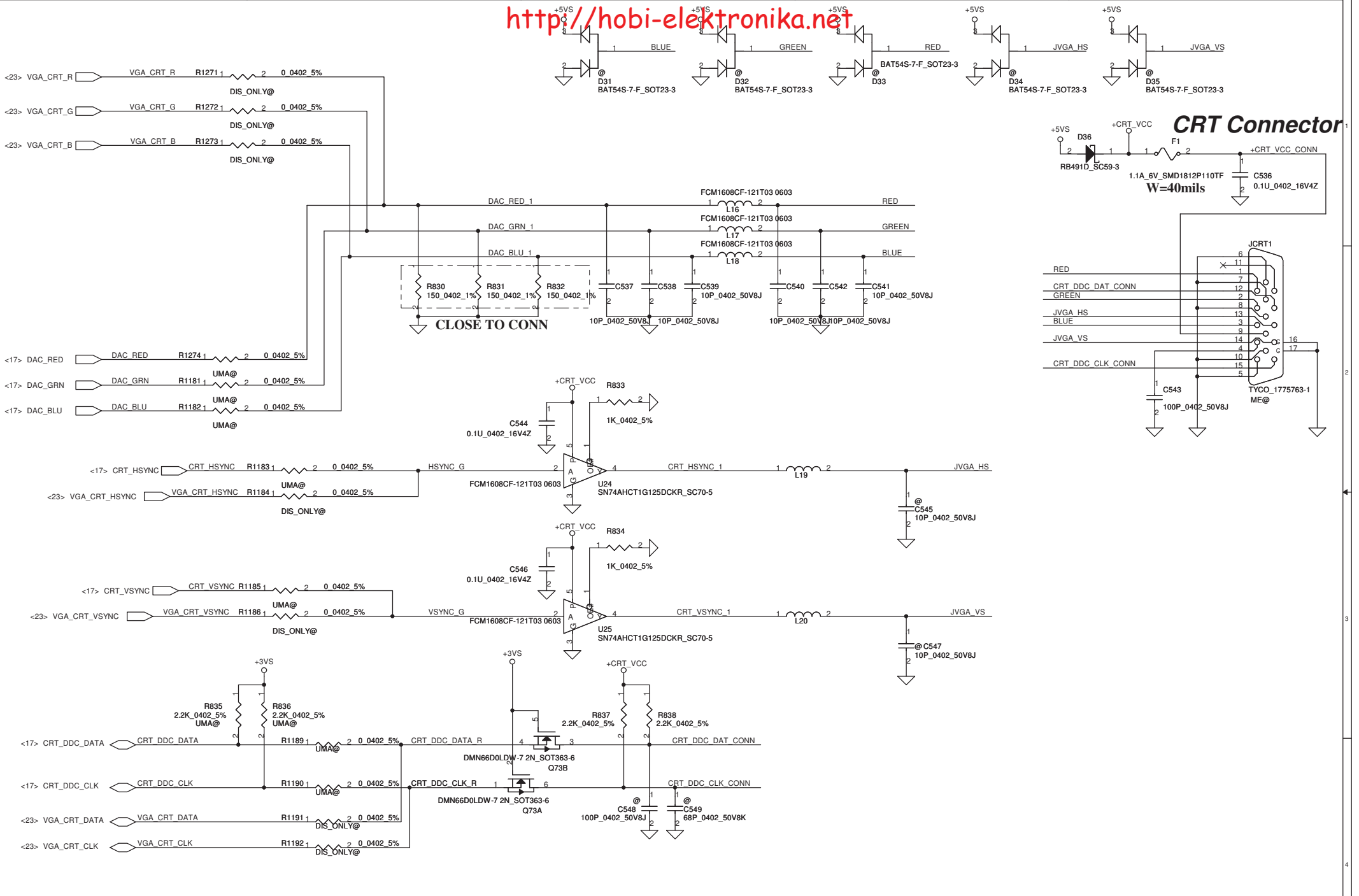
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Issued Date	2010/07/09	Deciphered Date	2011/05/11	Compal Electronics, Inc.	
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				Size	Document Number
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LCD POWER CIRCUIT



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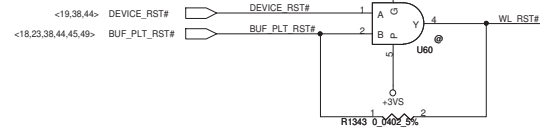
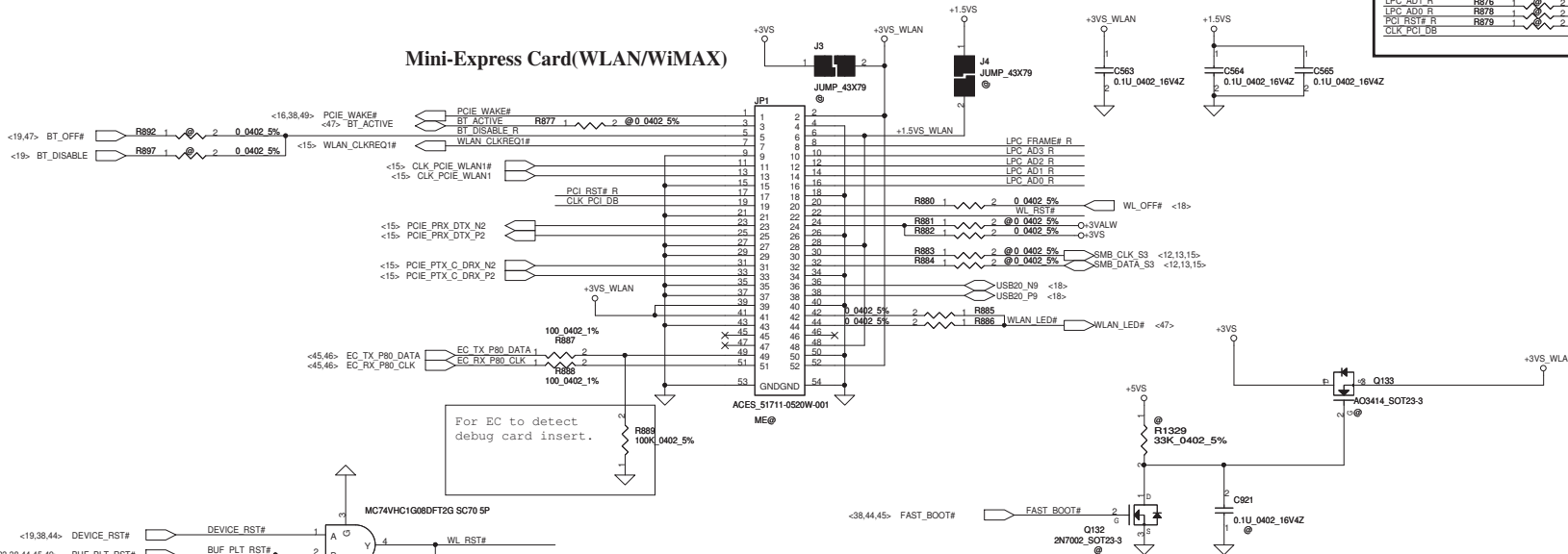
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

<http://hobi-elektronika.net>

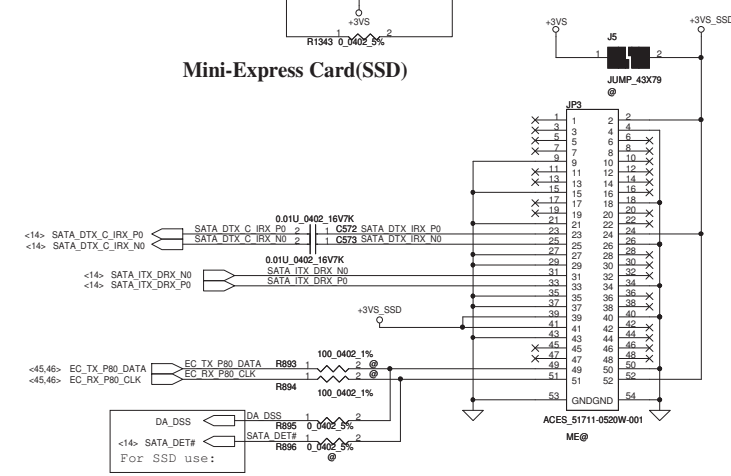
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC FRAME#_R	R873	1	2	0.0402_5%	LPC FRAME#	LPC FRAME#	<14,45>
LPC AD3_R	R874	1	2	0.0402_5%	LPC AD3	LPC AD3	<14,45>
LPC AD2_R	R875	1	2	0.0402_5%	LPC AD2	LPC AD2	<14,45>
LPC AD1_R	R876	1	2	0.0402_5%	LPC AD1	LPC AD1	<14,45>
LPC AD0_R	R878	1	2	0.0402_5%	LPC AD0	LPC AD0	<14,45>
PCI_RST#_R	R879	1	2	0.0402_5%	BUF_PLT_RST#	CLK_PCI_DB	<15>
CLK_PCI_DB	R879	1	2	0.0402_5%	BUF_PLT_RST#	CLK_PCI_DB	<15>

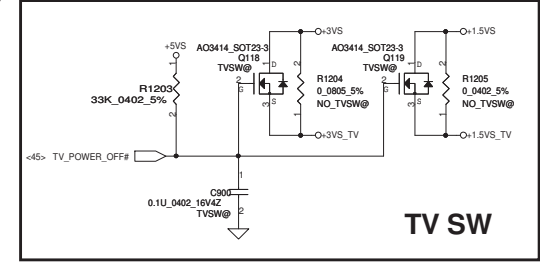
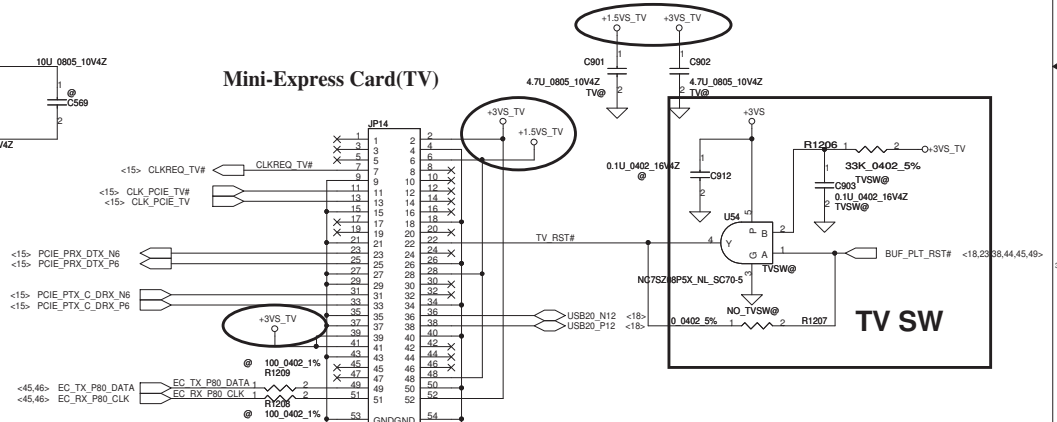
Mini-Express Card(WLAN/WiMAX)

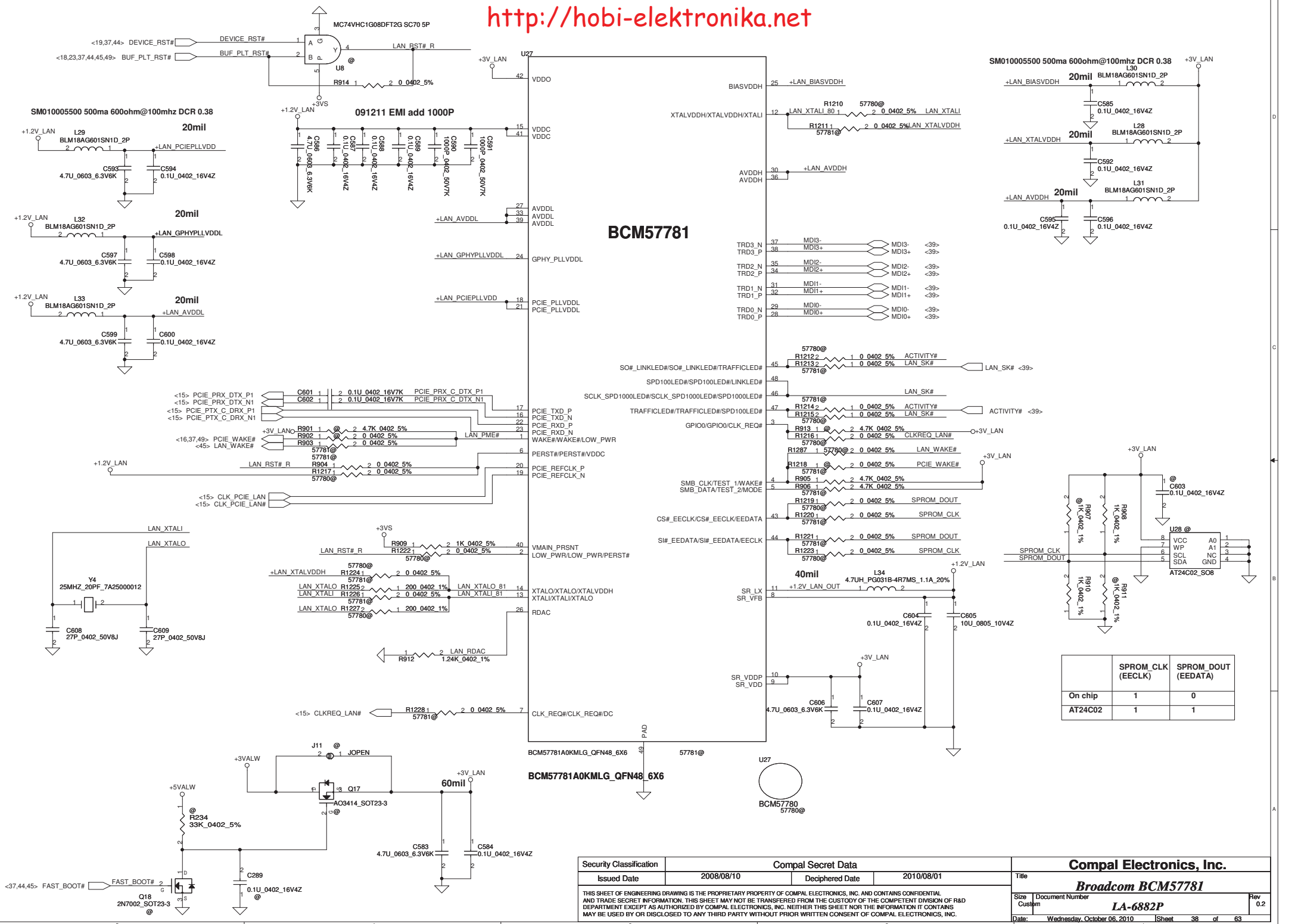


SSD Active:4.5W(1.5A)



Mini-Express Card(TV)



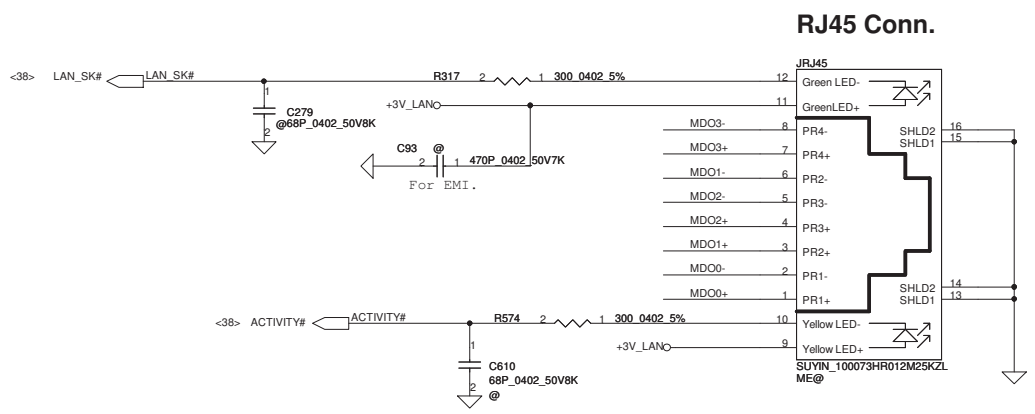
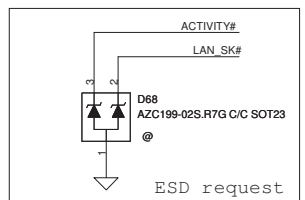
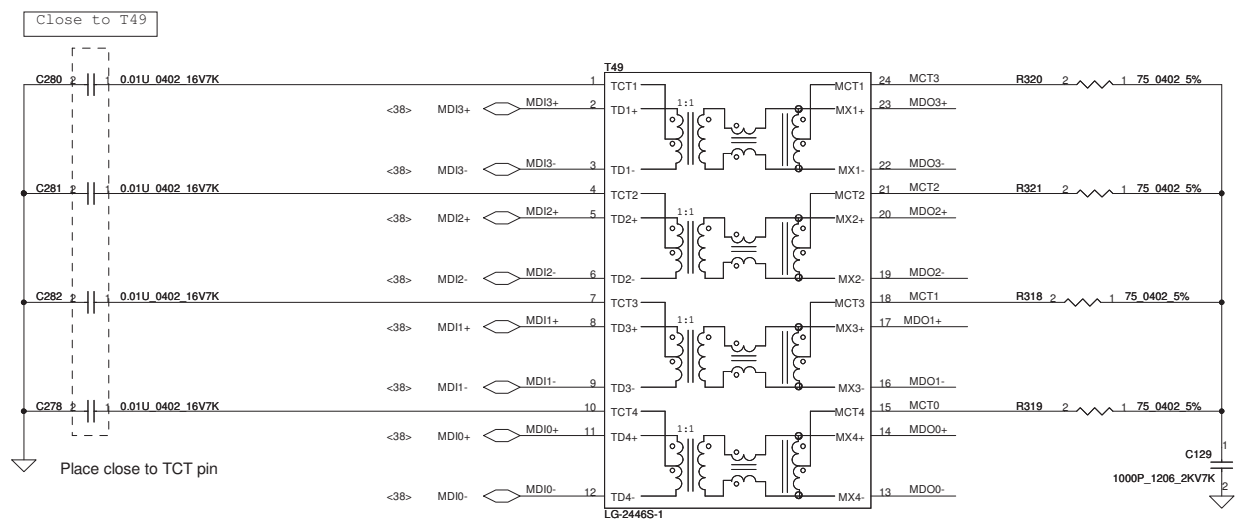


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Issued Date	2008/08/10	Deciphered Date 2010/08/01

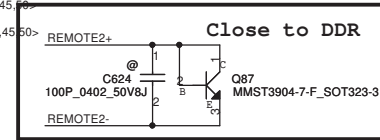
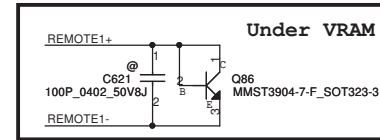
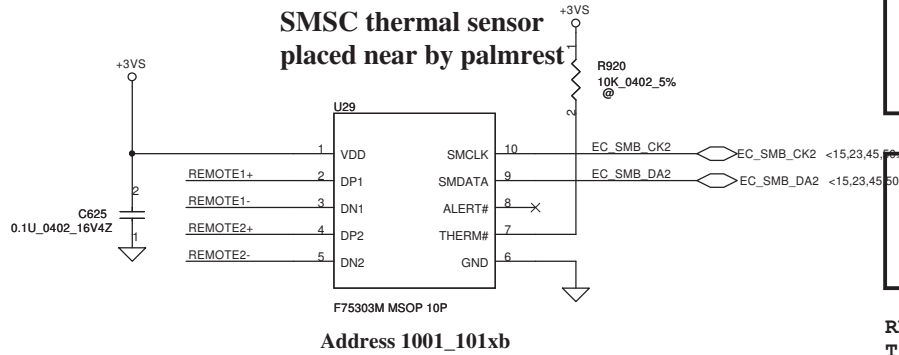
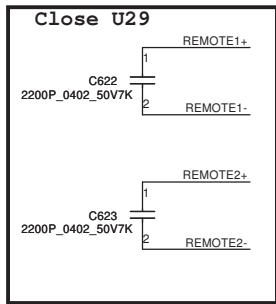
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	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

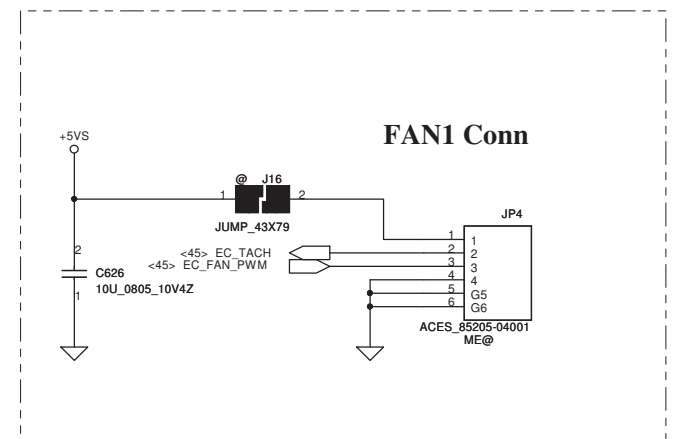
Compal Electronics, Inc.		
Broadcom BCM57781		
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Size	Document Number	Rev		Date	
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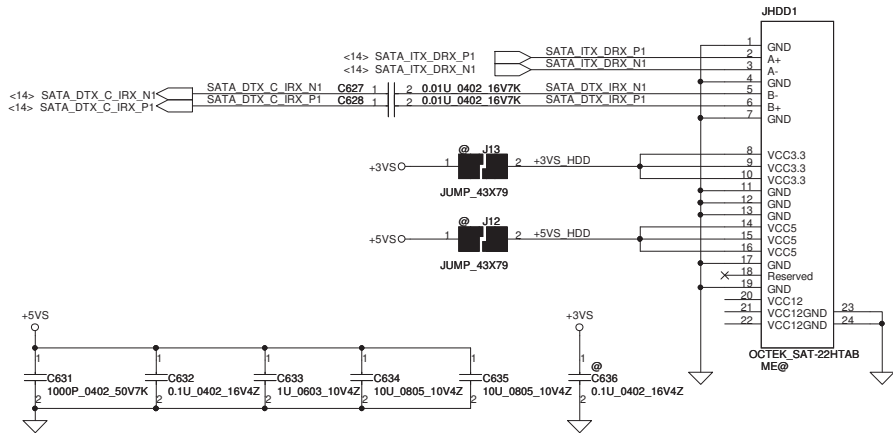


REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

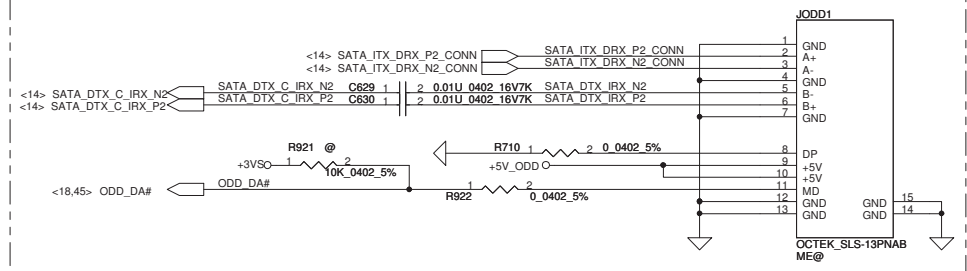


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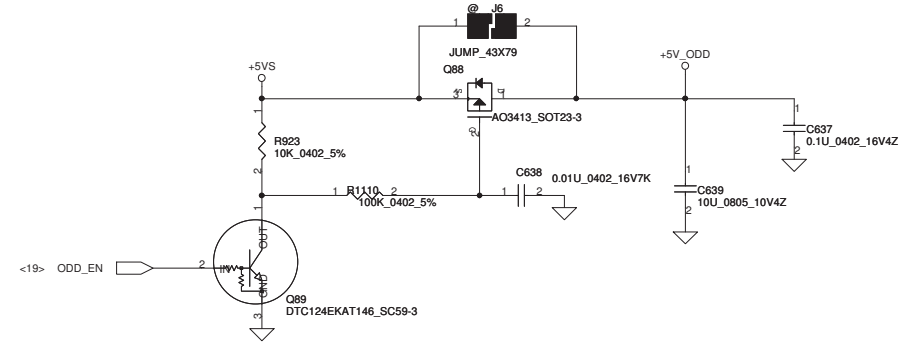
SATA HDD Conn.



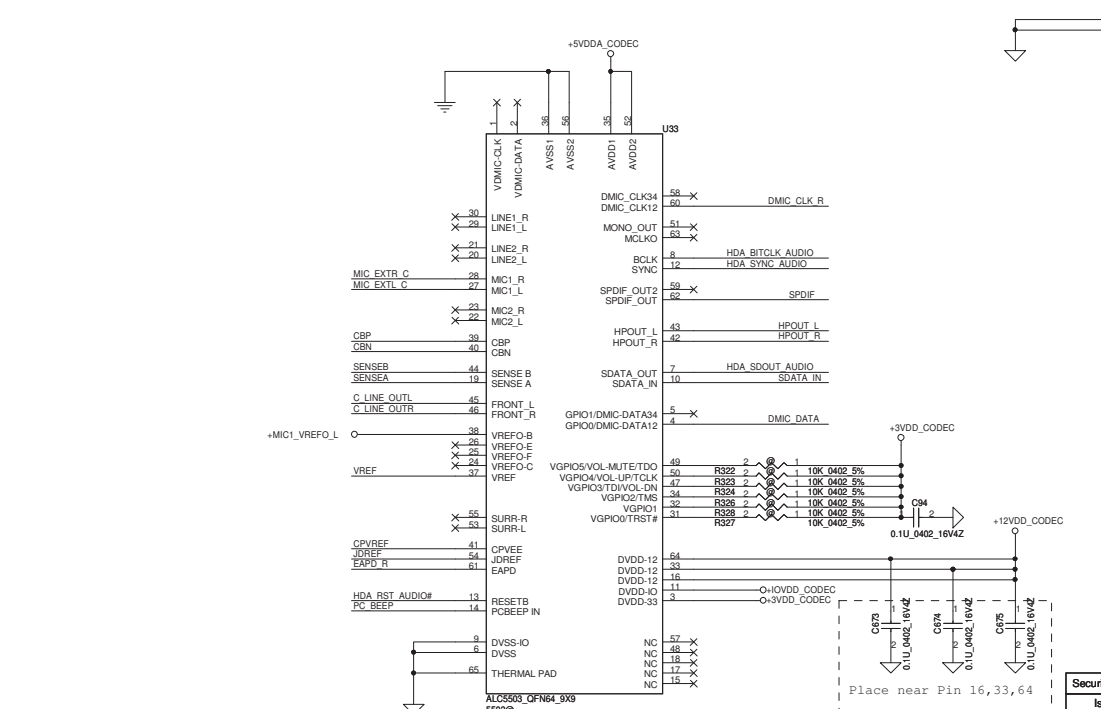
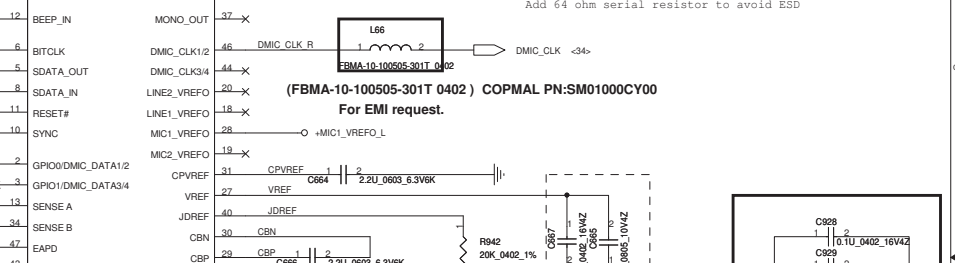
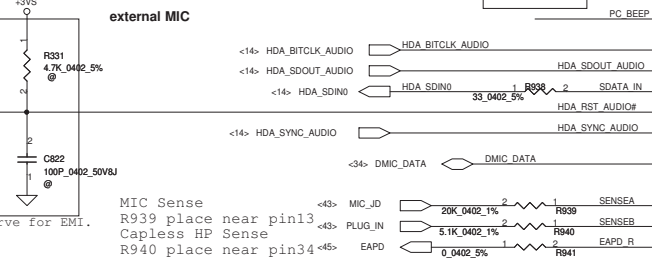
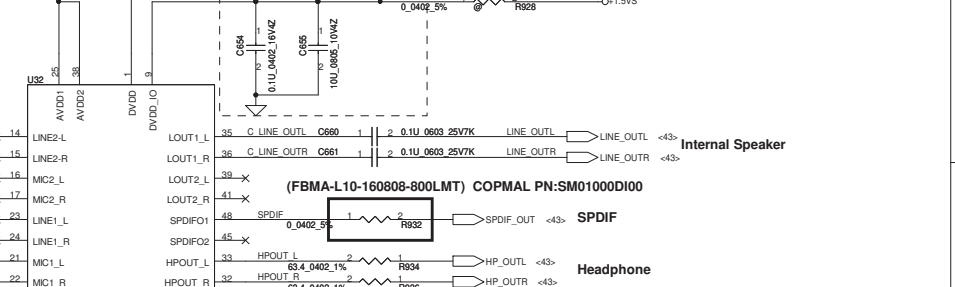
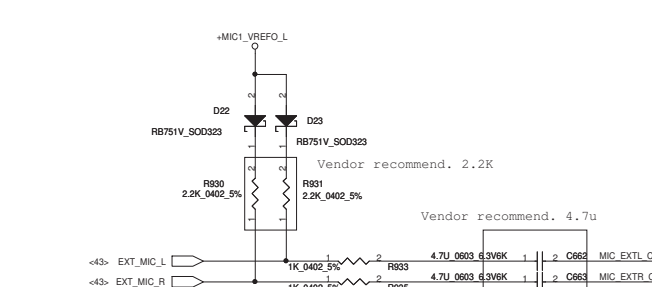
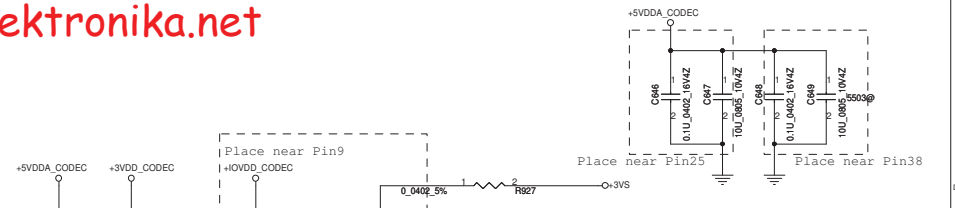
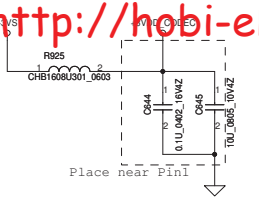
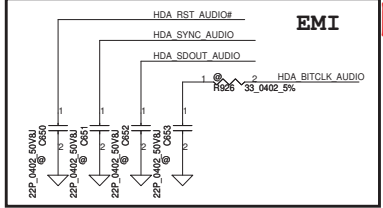
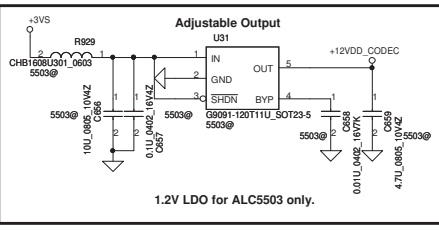
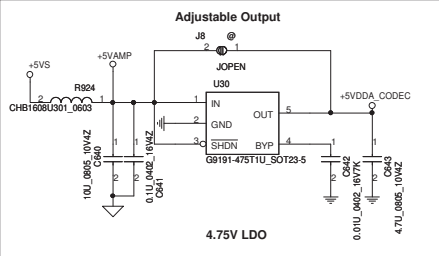
SATA ODD Conn.



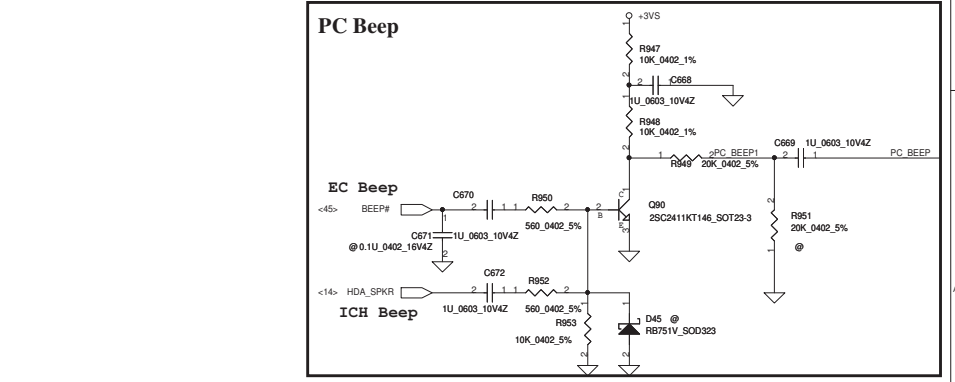
ODD Power Control



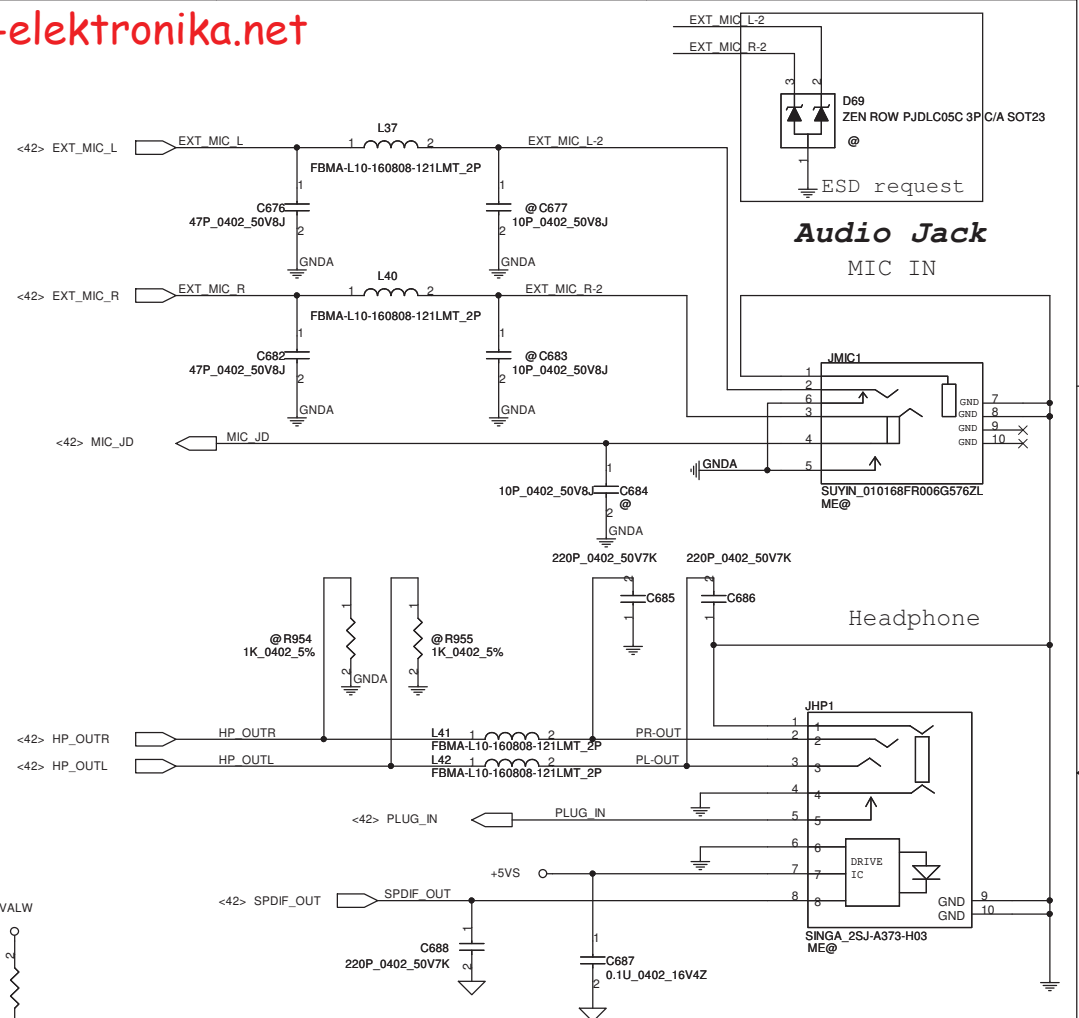
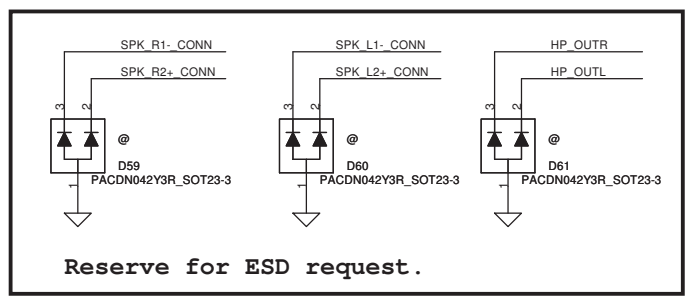
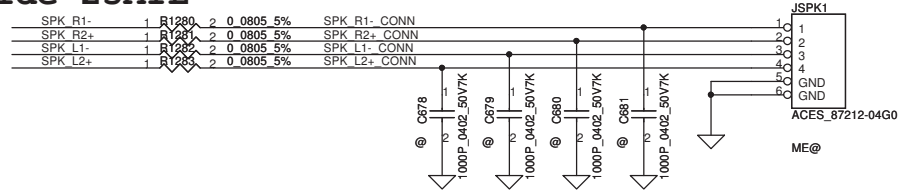
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Size B	Document Number	Date: Wednesday, October 06, 2010		Rev	0.2
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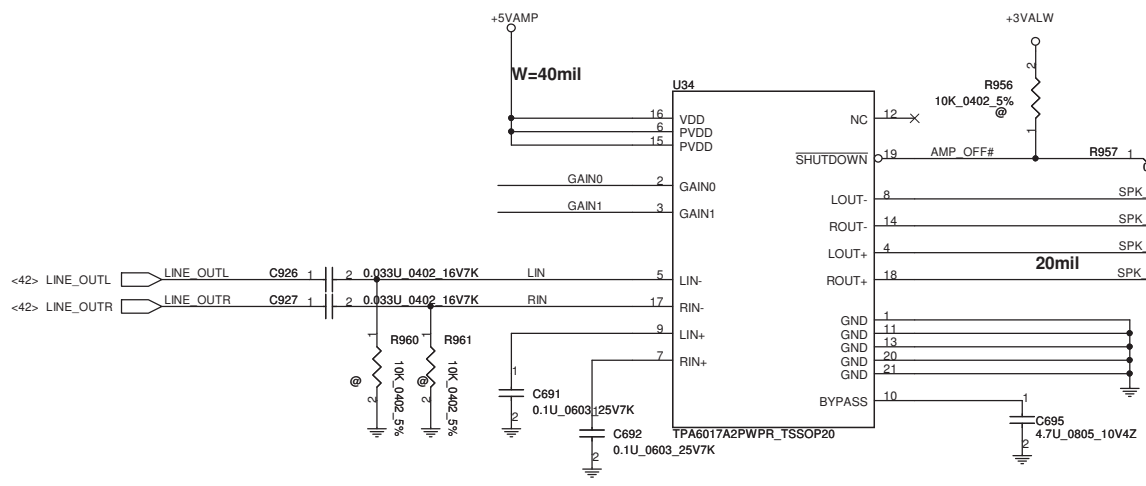
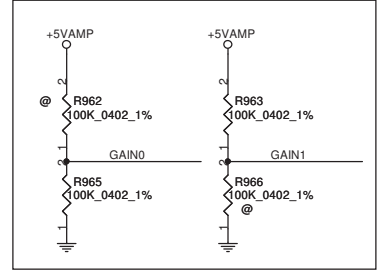
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MIC2 (Pin16/17)	Internal	Internal Mic



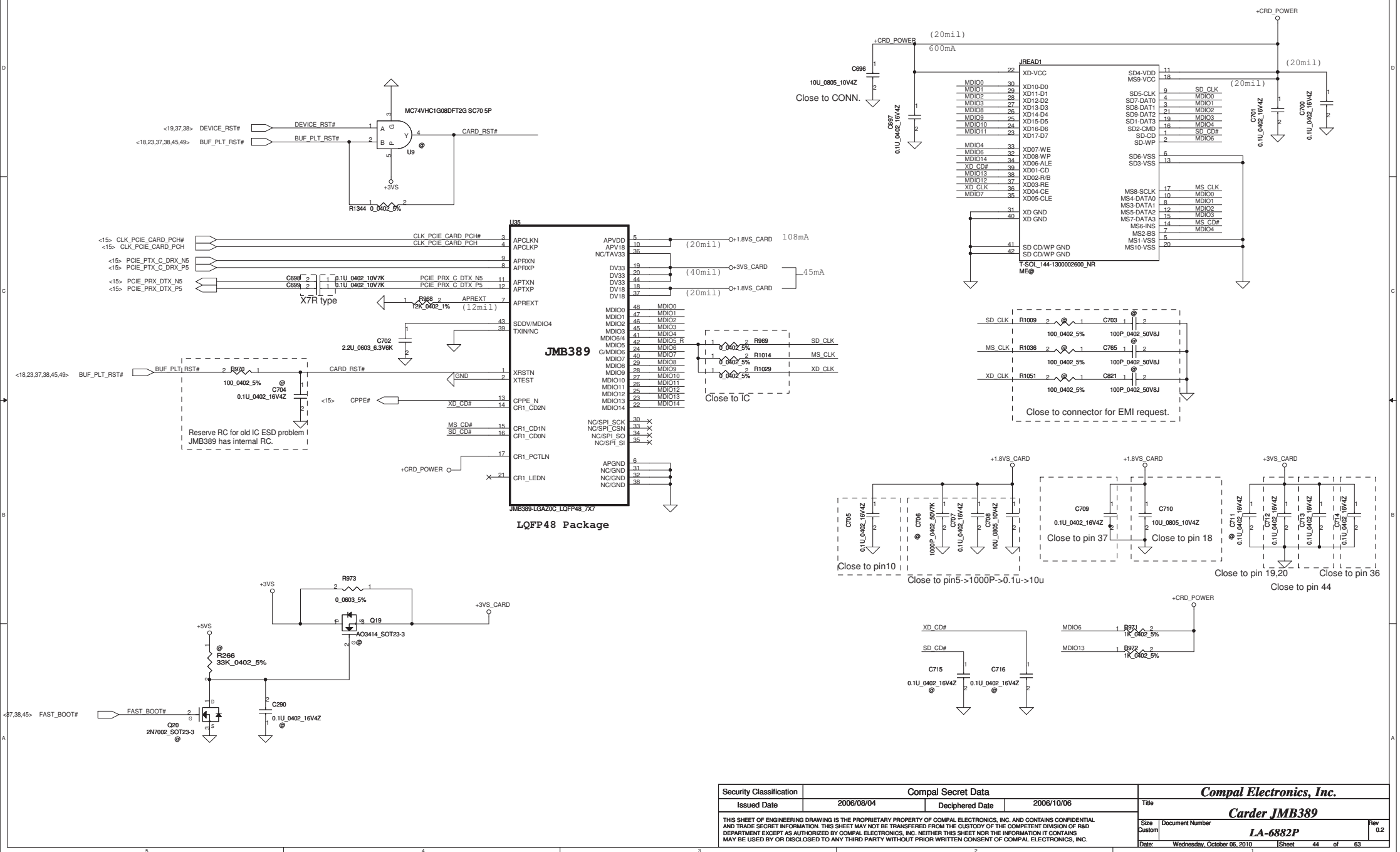
wide 25MIL



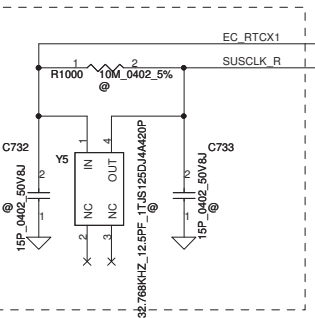
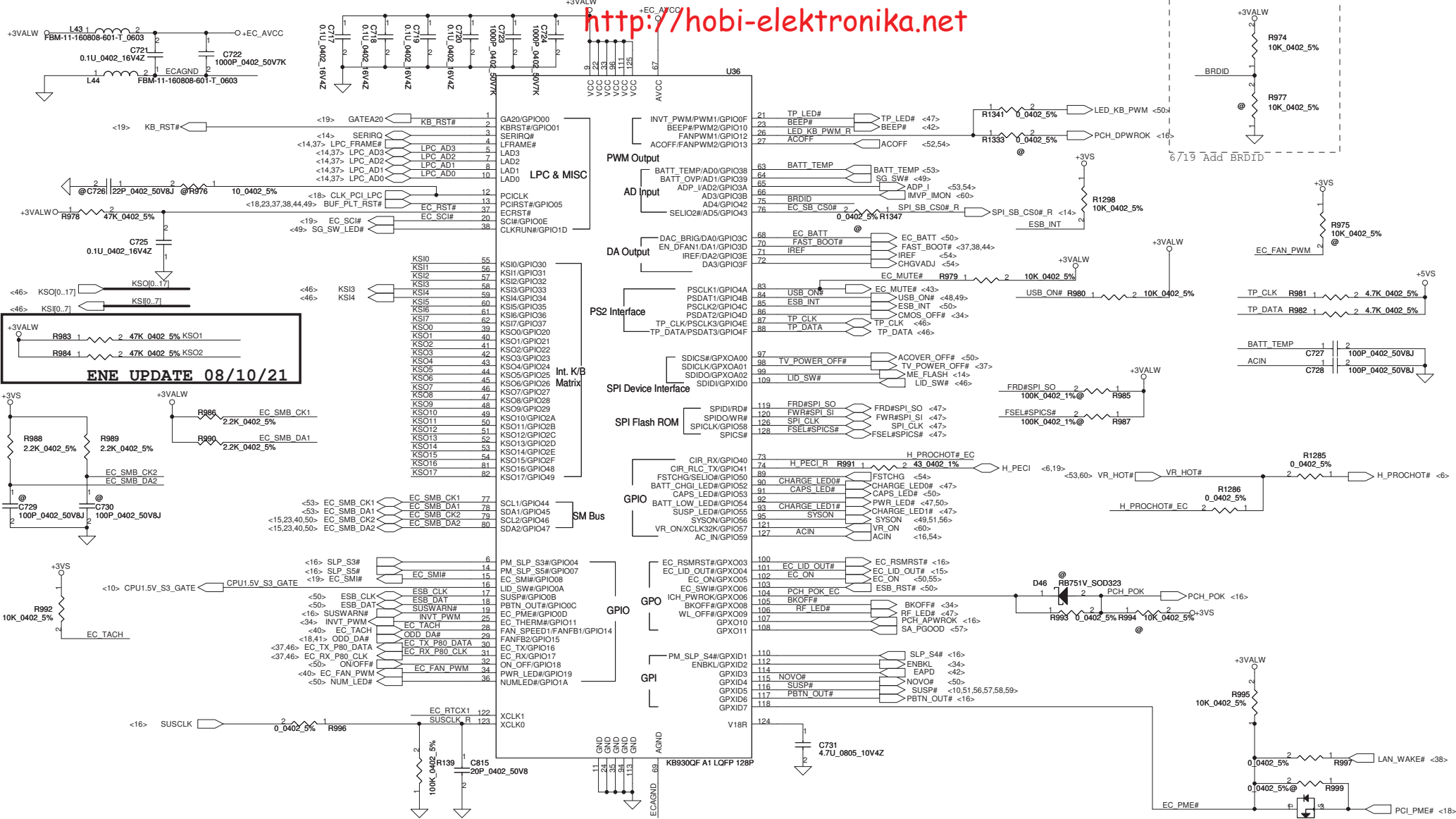
GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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				AMP Audio speaker CONN	
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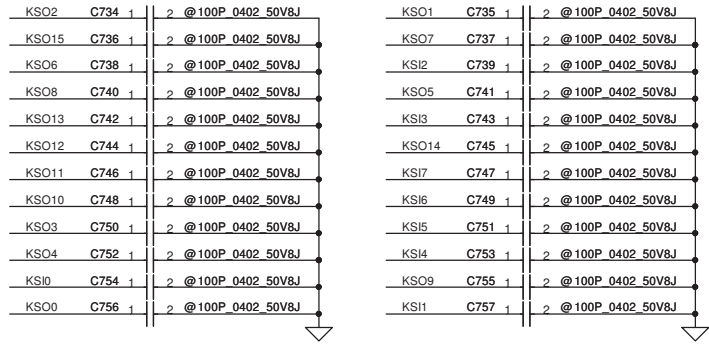
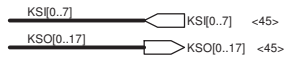
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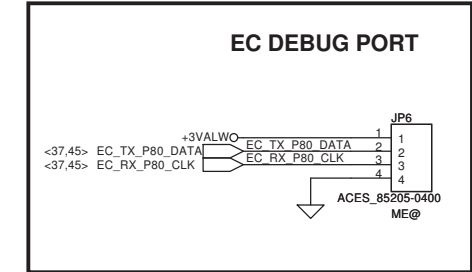
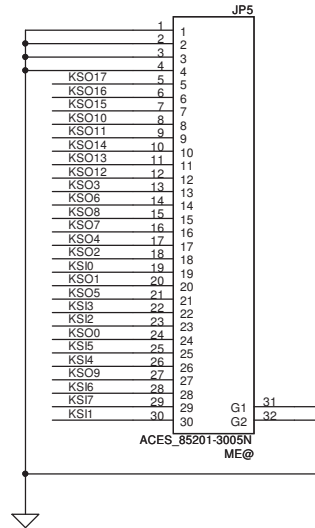
09/11 Unstuff

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Size	Document Number	Rev		0.2
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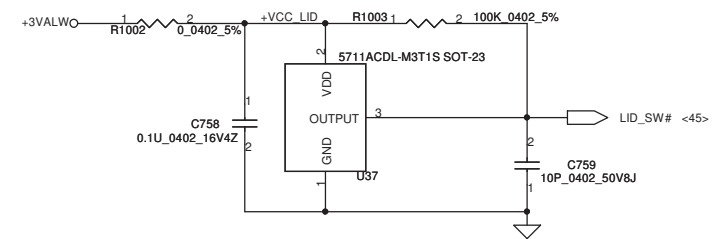
INT_KBD Conn.



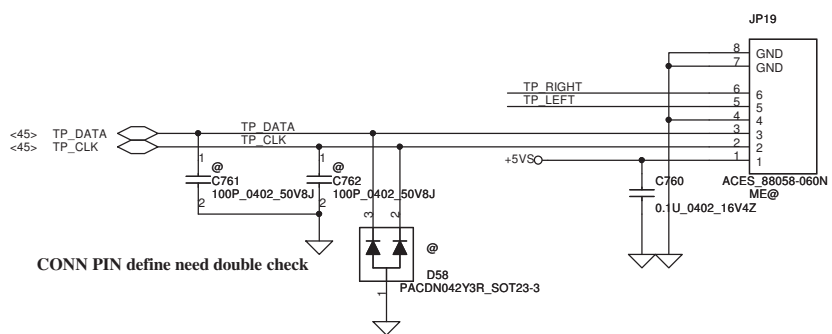
CONN PIN define need double check



Lid Switch

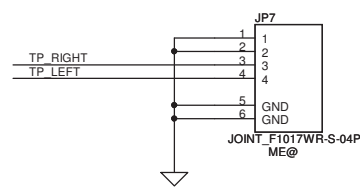


To TP/B Conn.



CONN PIN define need double check

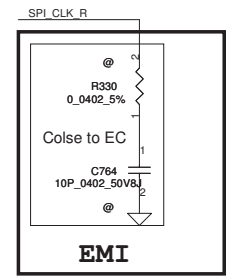
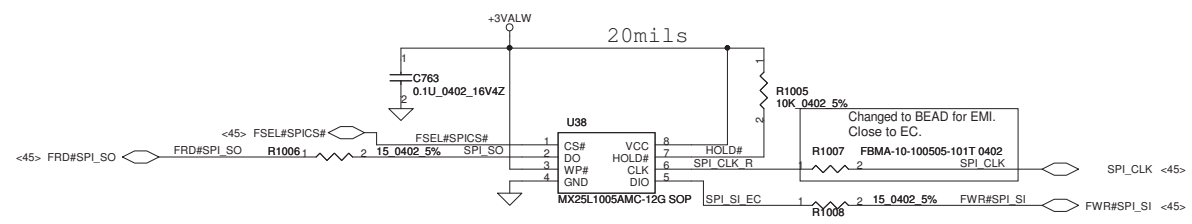
To TP Button/B Conn.



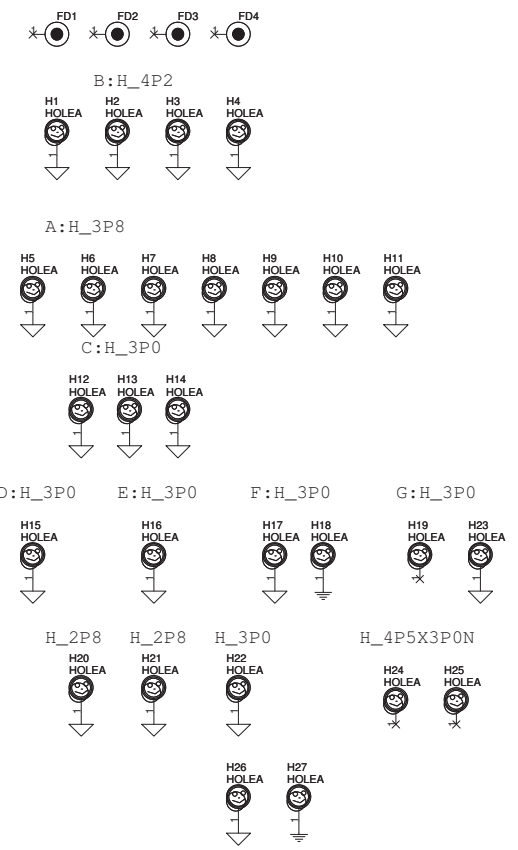
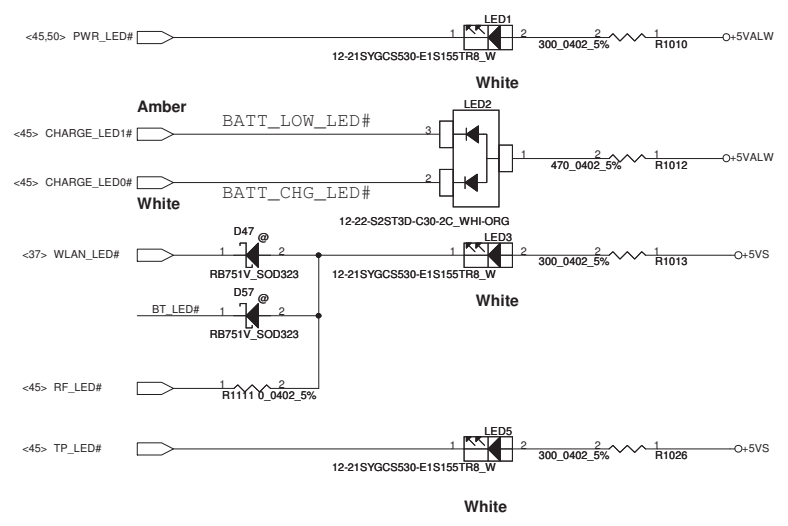
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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Size	Document Number			Rev	
B	LA-6882P			0.2	
Date:	Wednesday, October 06, 2010	Sheet	46	of 63	

FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100

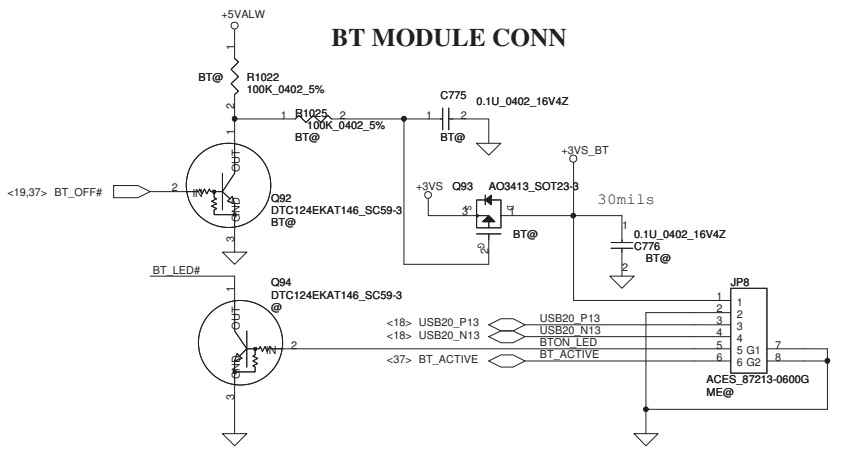
http://hobi-elektronika.net



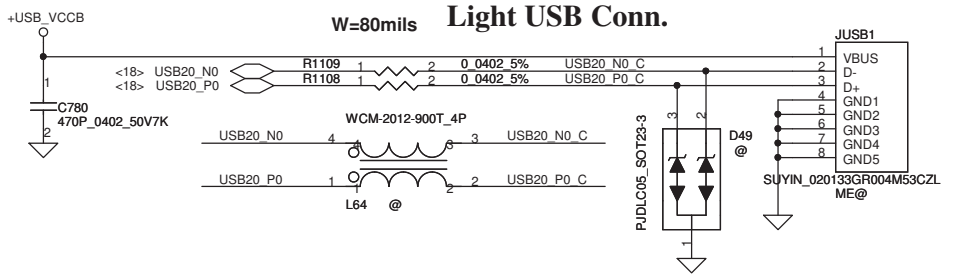
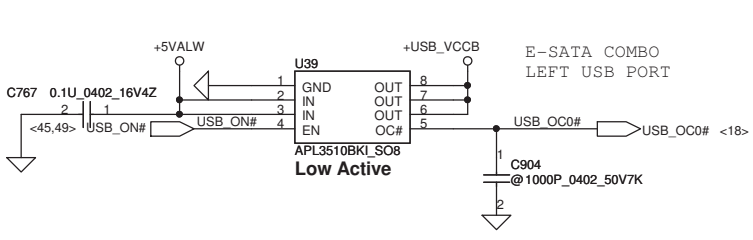
LED



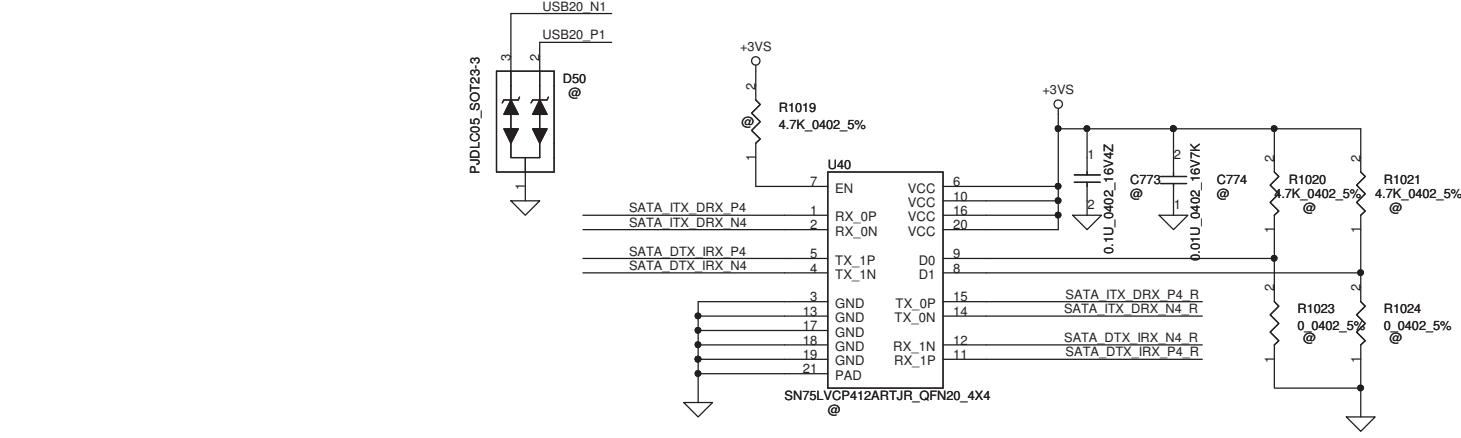
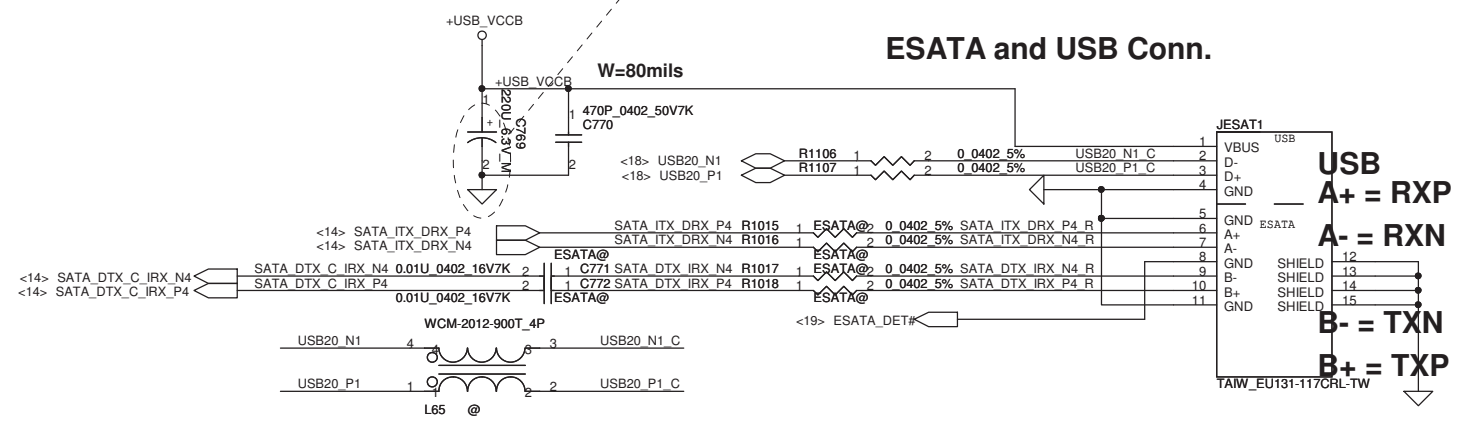
BT MODULE CONN



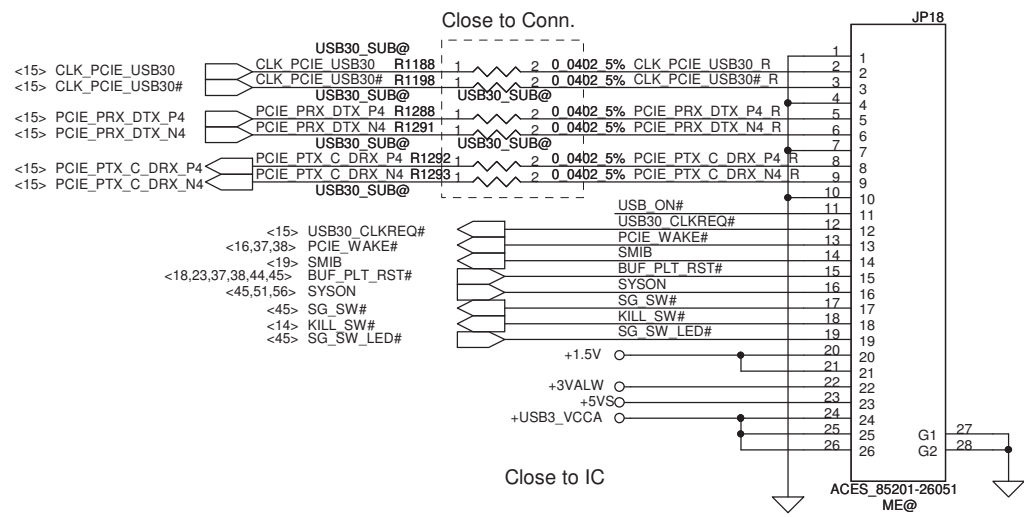
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2007/10/15		2008/10/15		LED/EC SPI ROM/BT	
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Date:	Wednesday, October 06, 2010		Sheet	47	of 63



OSCAN
(220uF_6.3V_5.9L_ESR17m) *1=(SF000001500)

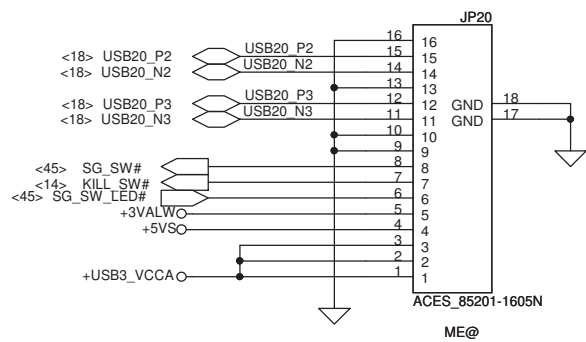
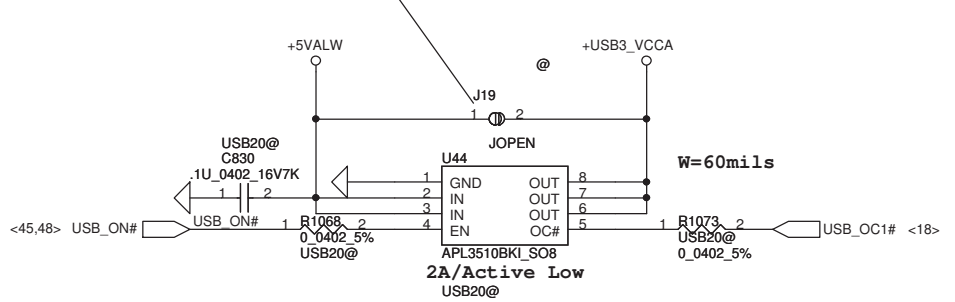


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Size	Document Number	Rev		0.2	
Custom	LA-6882P	Date: Wednesday, October 06, 2010		Sheet 48 of 63	



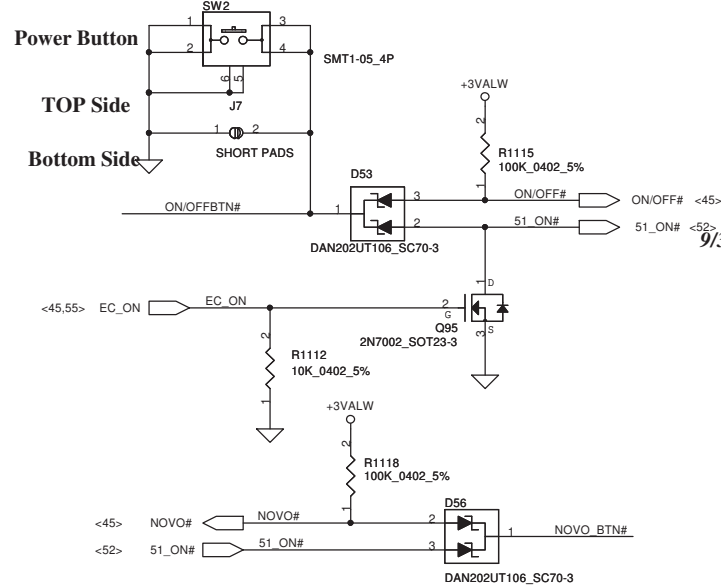
09/30 Delete USB3.0 controller

10/04 Short J19 with JP18.

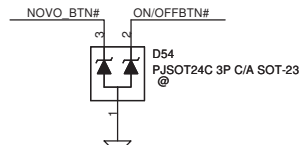
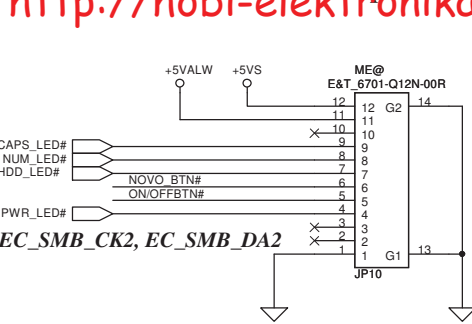


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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title
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				Size Custom
				LA-6882P
				Date: Wednesday, October 06, 2010
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ON/OFF switch



Power Button Conn. 10pin

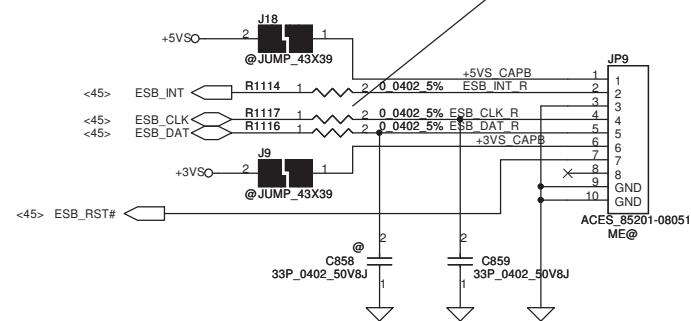


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

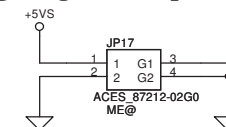
Cap Sensor Board Conn. 8pin

ENE SB3534

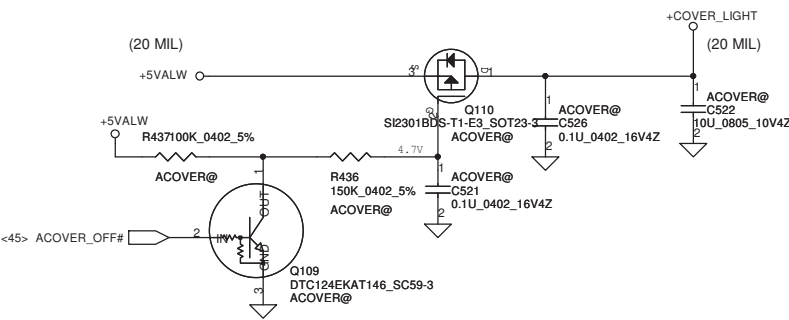
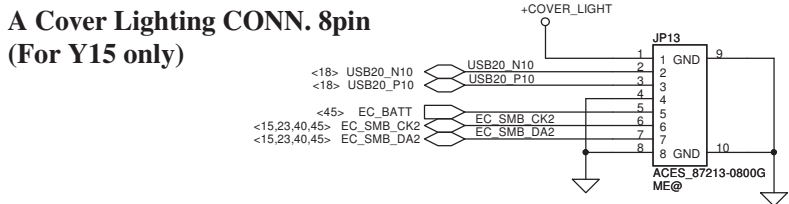
10/05 Change to SM01000CY00, EMI request



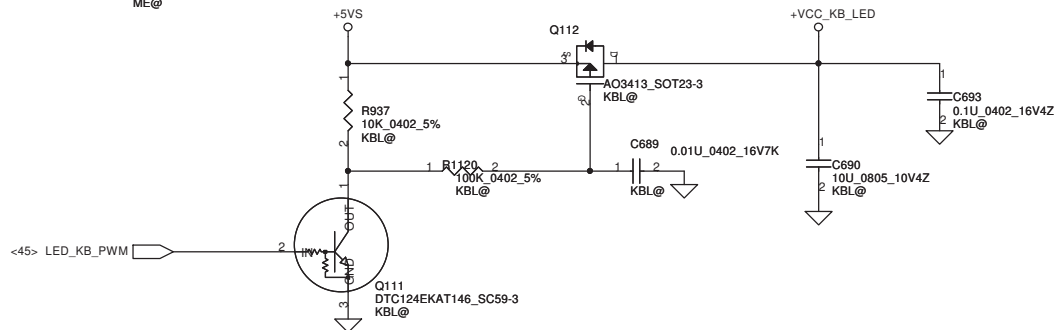
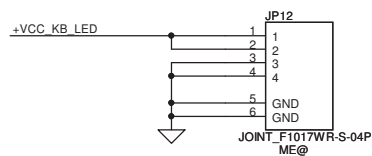
FAN Lighting Conn. 2pin (For Y15 only)



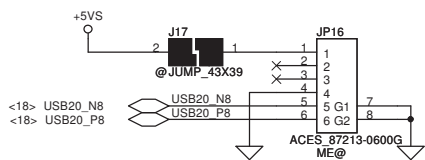
A Cover Lighting CONN. 8pin (For Y15 only)



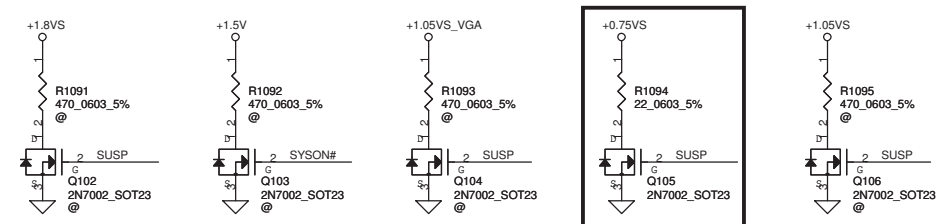
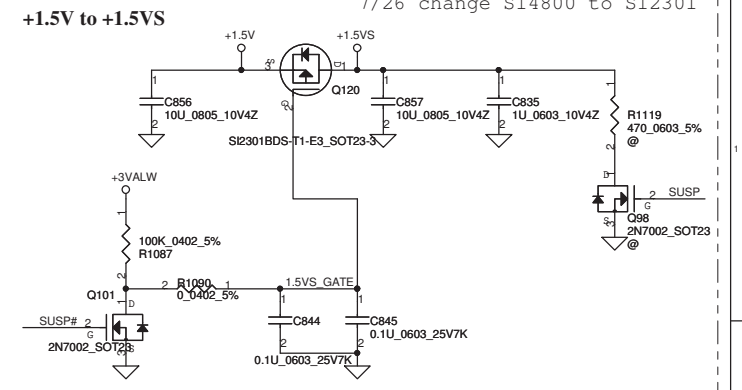
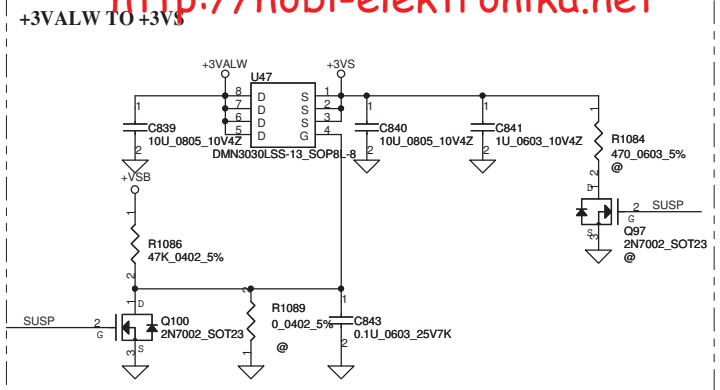
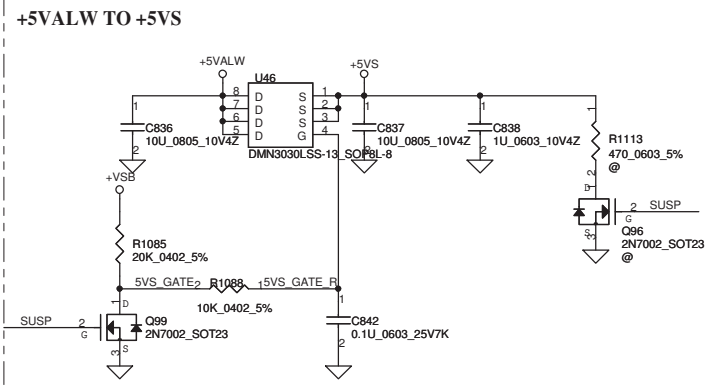
KB Lighting CONN.4pin



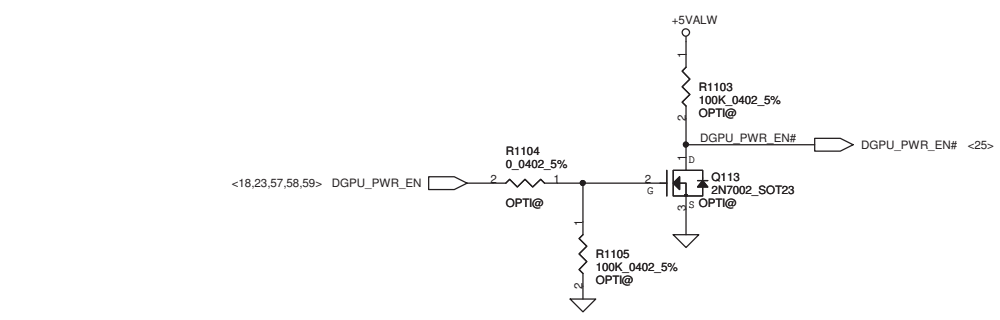
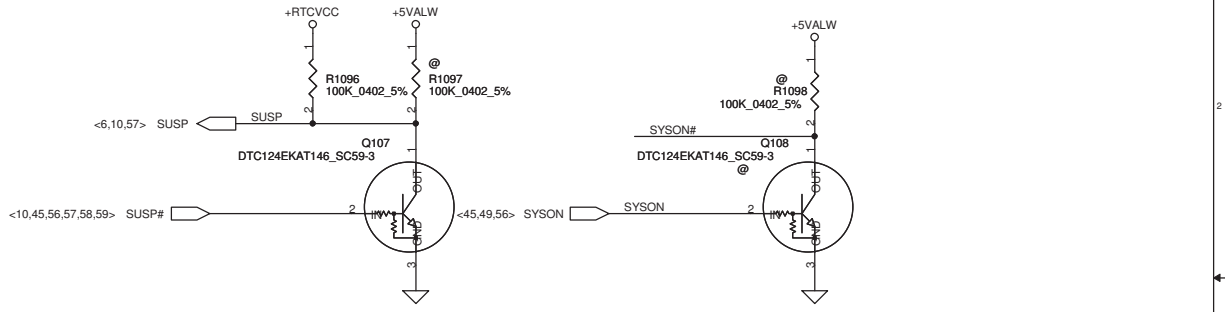
IR CONN. 6pin (For Y15 only)



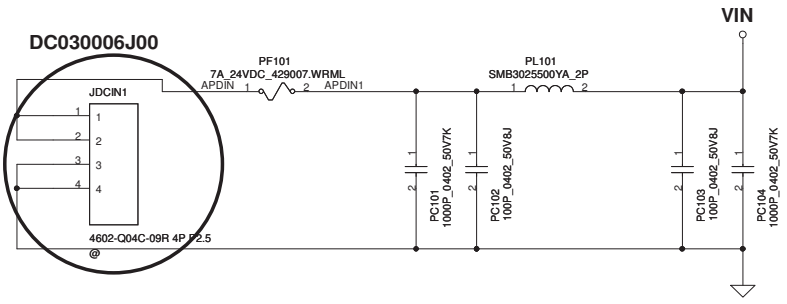
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Size Custom	Document Number	LA-6882P		Rev 0.2
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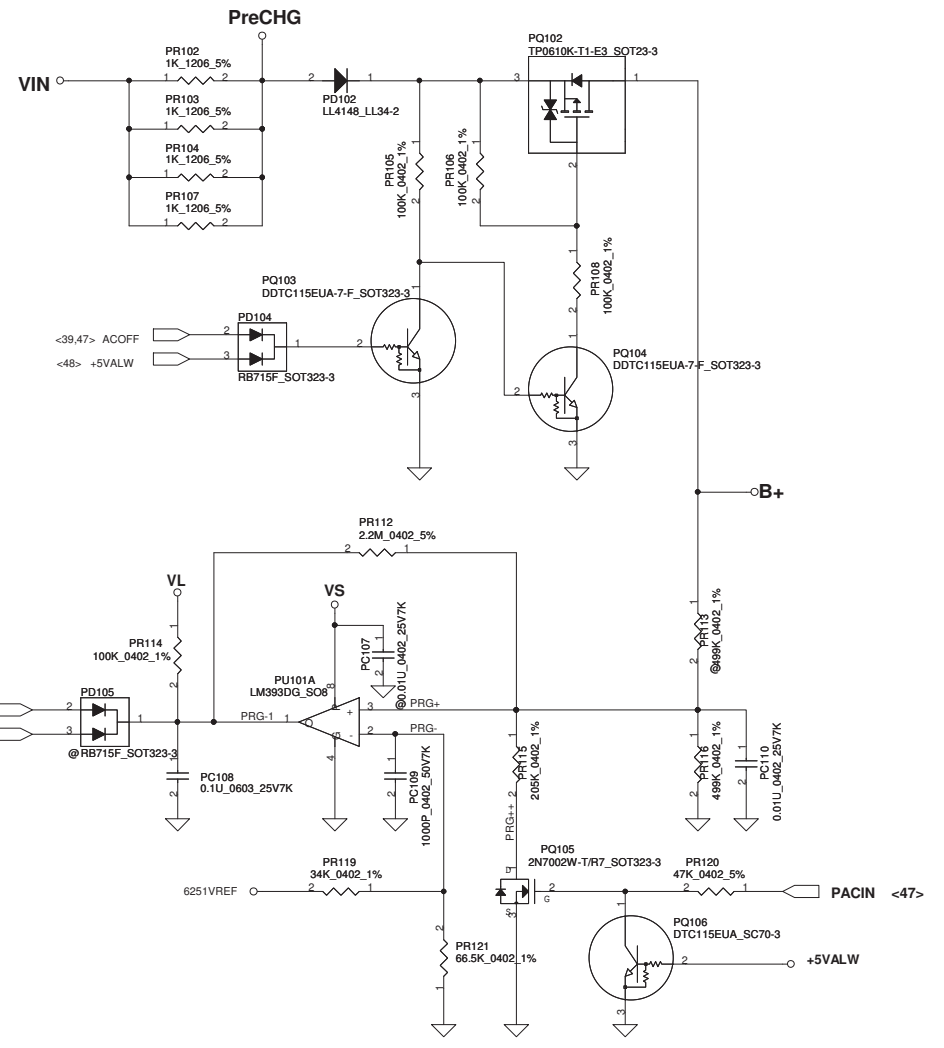
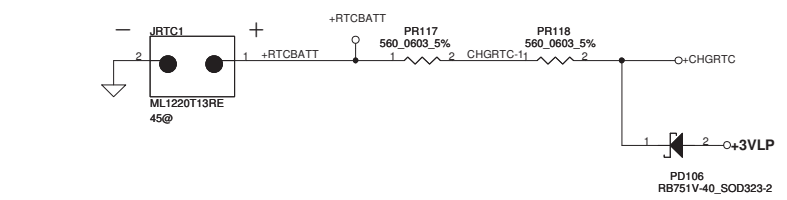
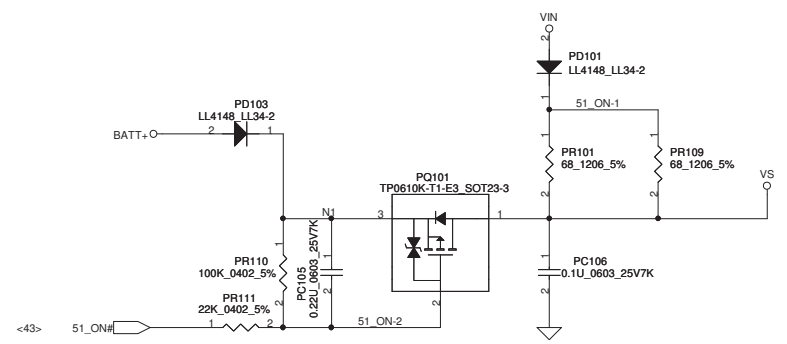
For Intel S3 Power Reduction.



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Size	Document Number	Date		Rev	
Custom	LA-6882P	Wednesday, October 06, 2010		0.2	
				Sheet	51 of 63



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**



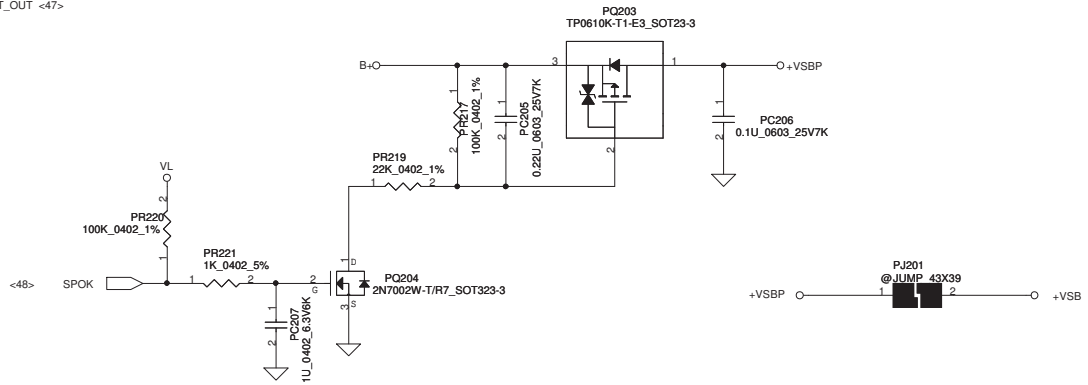
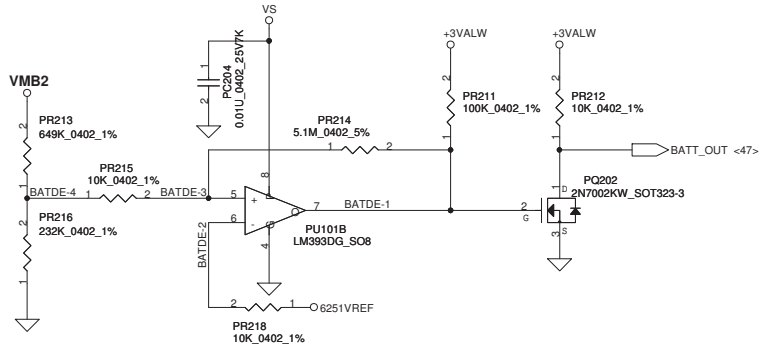
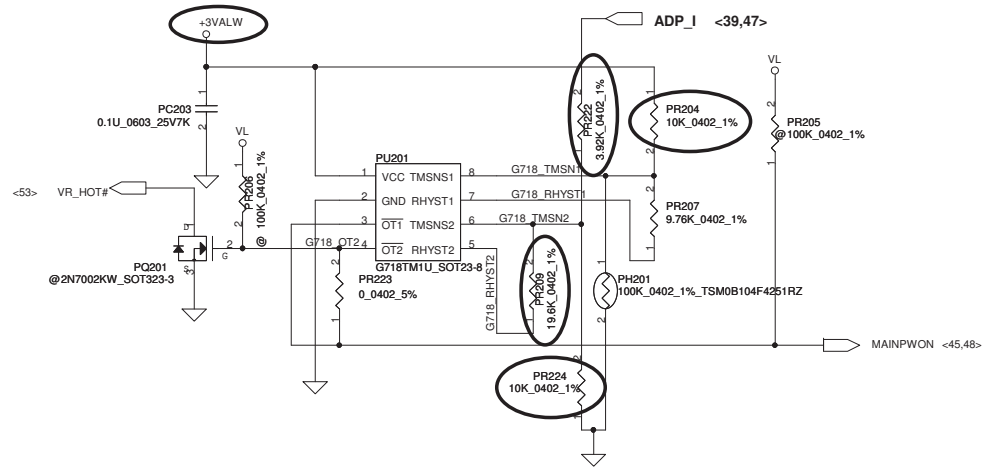
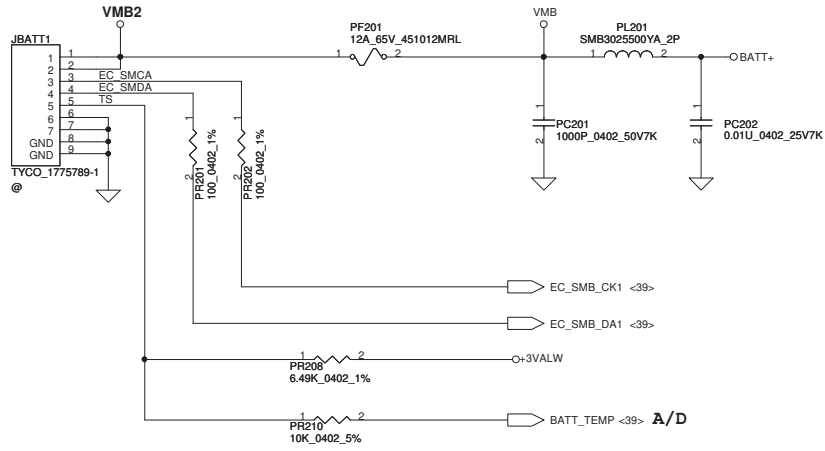
ACIN

Precharge detector			
Min.	typ.	Max.	
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

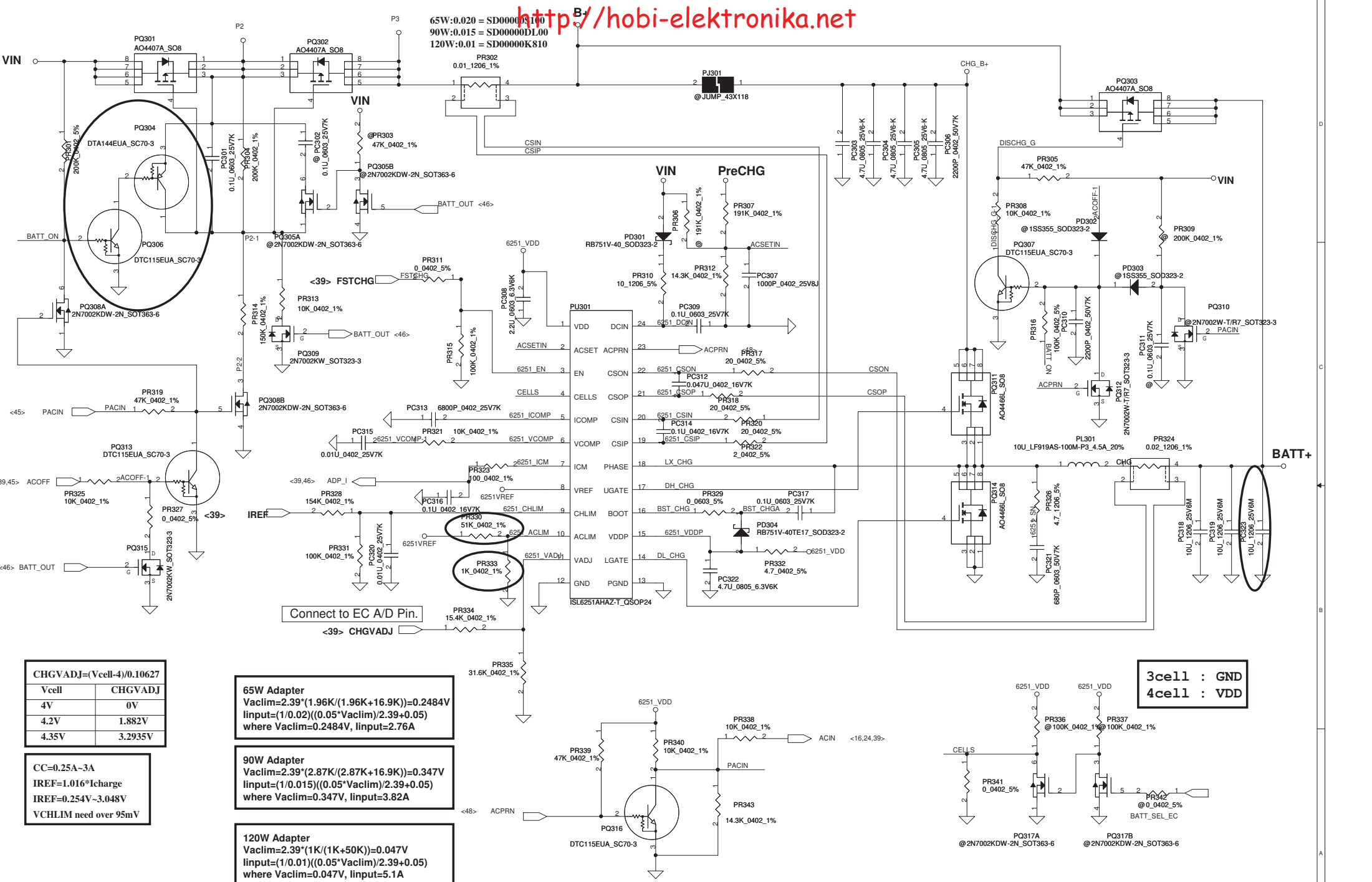
Precharge detector			
Min.	typ.	Max.	
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

PH201 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Issued Date	2010/01/25	Deciphered Date
		2010/12/31
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Compal Electronics, Inc. PWR-BATTERY CONN/OTP		
Title		
Size	Document Number	Rev
Custom	PIQY0/Y1	0.1
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$CHGVADJ = (V_{cell} - 4) / 0.10627$	
V _{cell}	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*I_{charge}
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

65W Adapter
 $V_{aclim} = 2.39 * (1.96K / (1.96K + 16.9K)) = 0.2484V$
 $I_{input} = (1 / 0.02) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 0.2484V$, $I_{input} = 2.76A$

90W Adapter
 $V_{aclim} = 2.39 * (2.87K / (2.87K + 16.9K)) = 0.347V$
 $I_{input} = (1 / 0.015) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 0.347V$, $I_{input} = 3.82A$

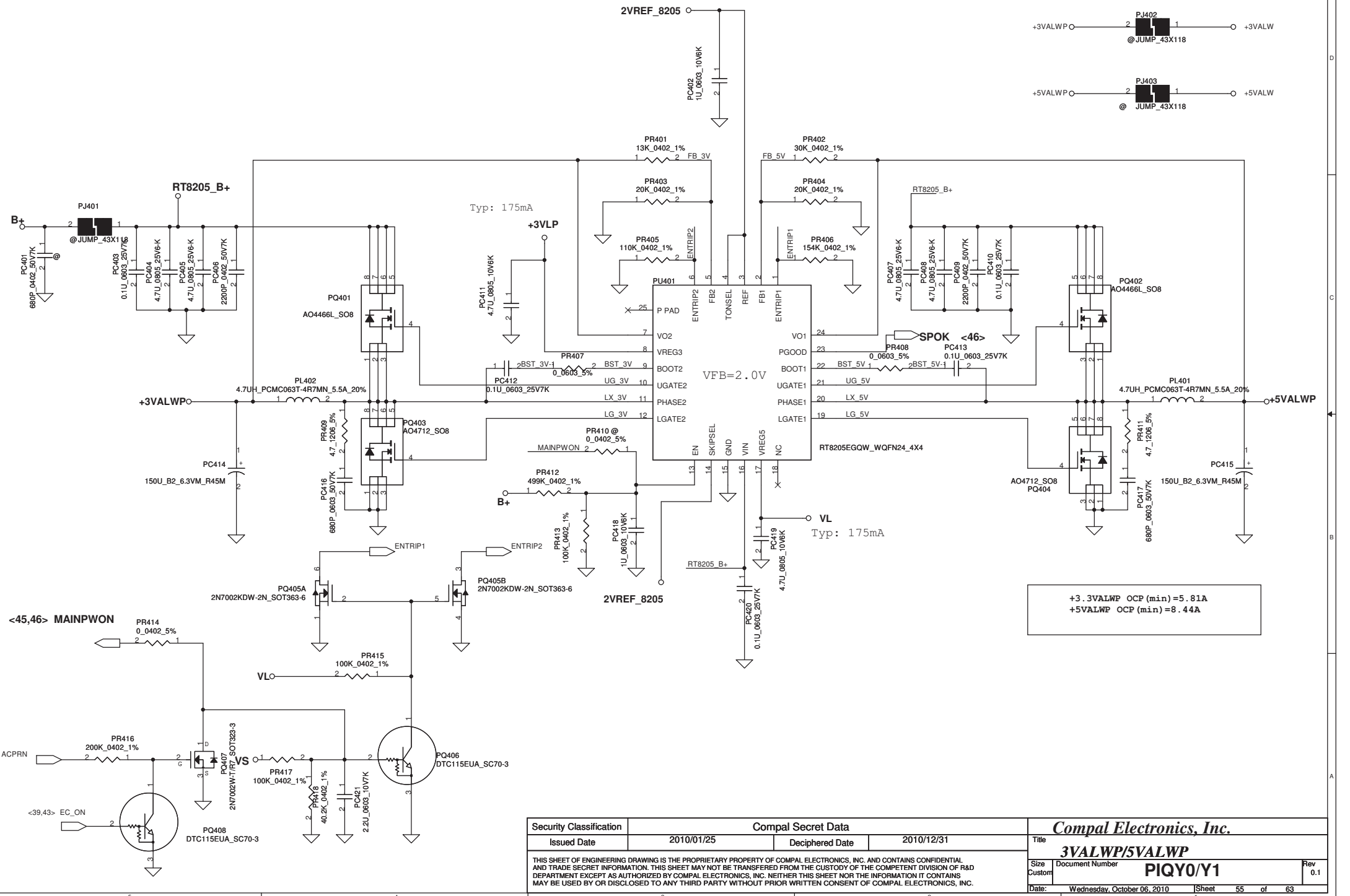
120W Adapter
 $V_{aclim} = 2.39 * (1K / (1K + 50K)) = 0.047V$
 $I_{input} = (1 / 0.01) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 0.047V$, $I_{input} = 5.1A$

65W : PR330=16.9K, PR333=1.96K
 90W : PR330=16.9K, PR333=2.87K
 120W : PR330=50K, PR333=1K

3cell : GND
 4cell : VDD

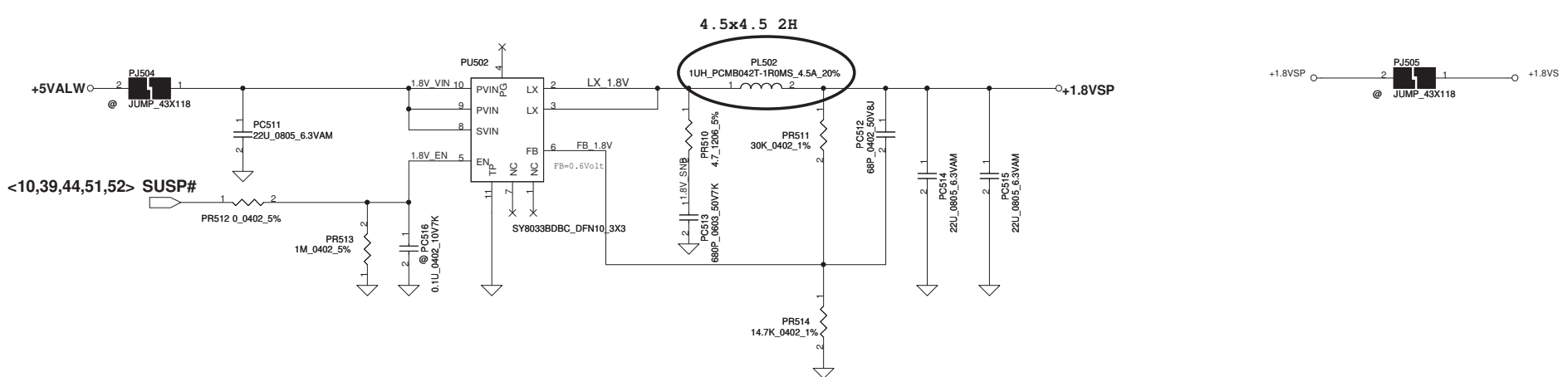
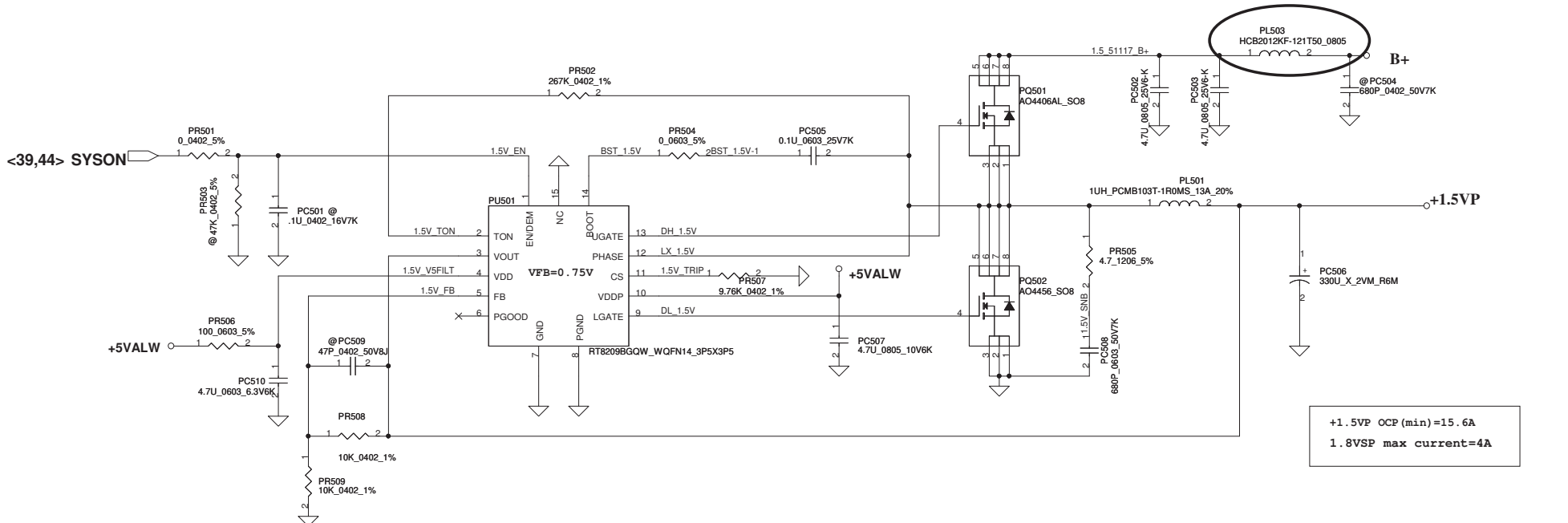
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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title	CHARGER
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				PIQY0/Y1	Rev 0.2
				Date: Wednesday, October 06, 2010	Sheet 54 of 63

Note:
 Use TPS51125 IC can remove RTC referenece LDO
 Use TPS51427 IC must keep RTC referenece LDO

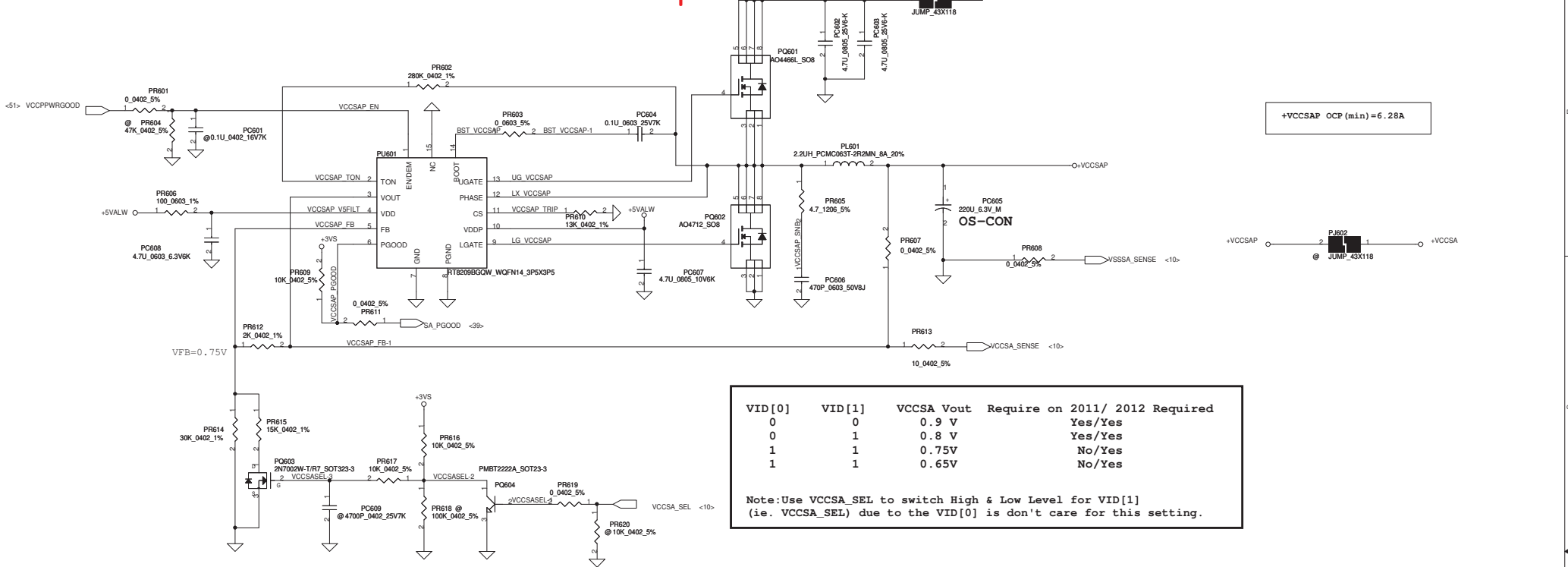


+3.3VALWP OCP (min) = 5.81A
 +5VALWP OCP (min) = 8.44A

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Date	Wednesday, October 06, 2010	Sheet	55	of	63
Document Number	PIQY0/Y1		Rev	0.1	

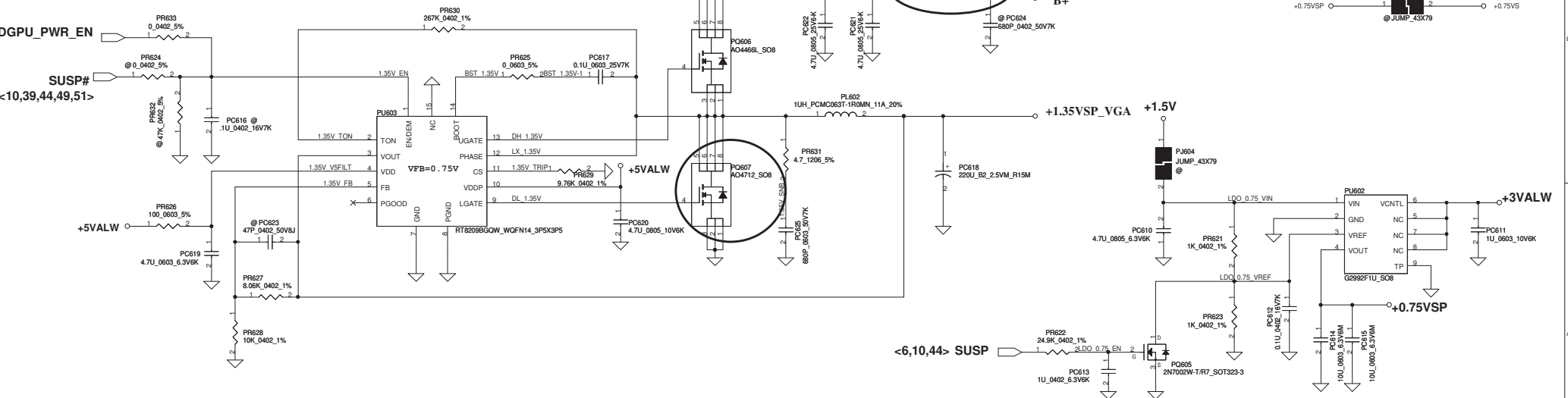


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				Customer	Rev 0.1
				Date:	Wednesday, October 06, 2010
				Sheet	56 of 63

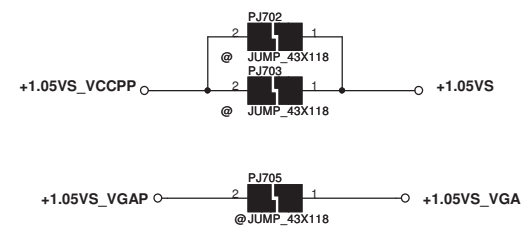
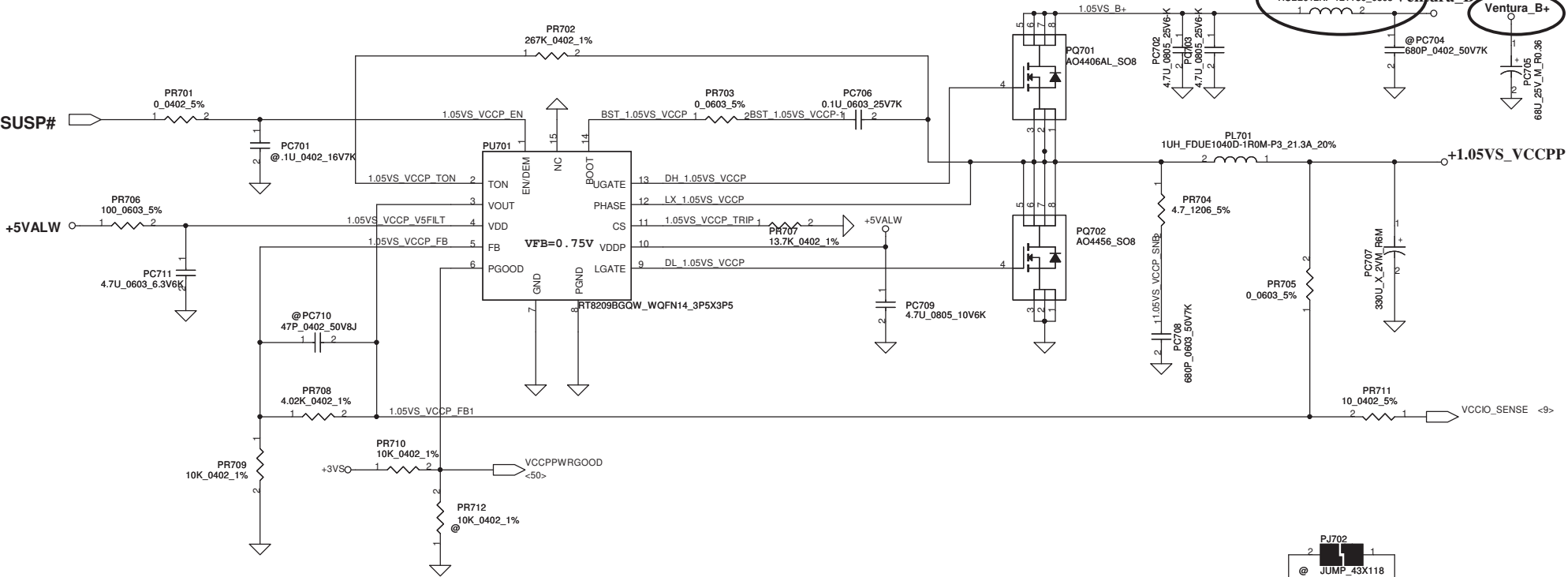
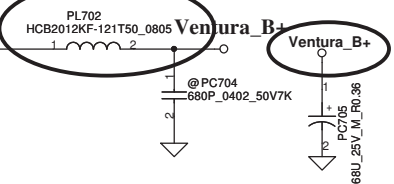


+VCCSAP OCP (min) = 6.28A

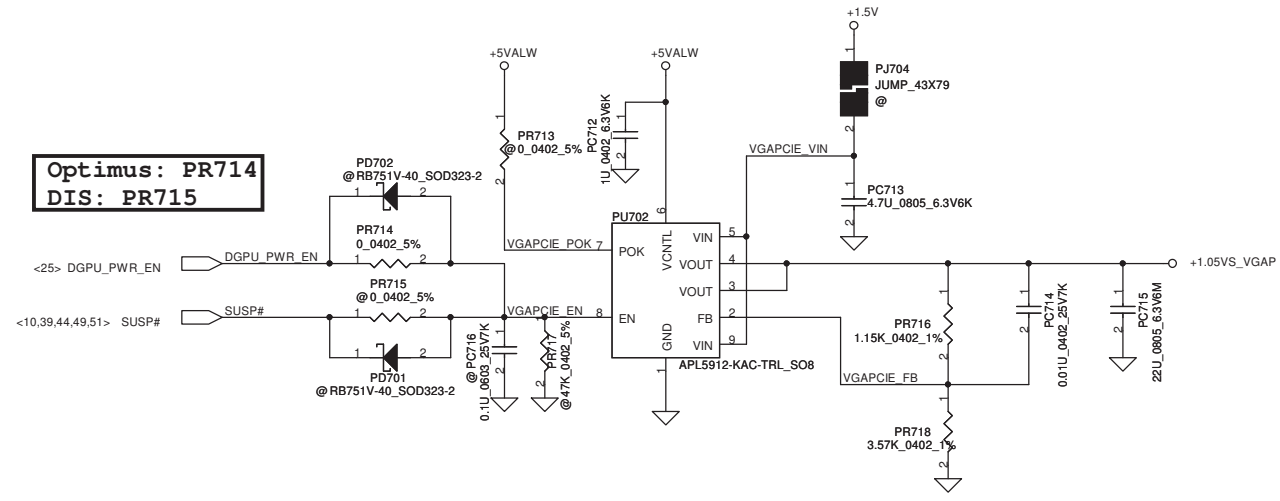
Optimus: PR633
DIS: PR624



+1.05VS_VCCPP OCP (min)=20.75A



Optimus: PR714
DIS: PR715



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Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR +1.05VS VCCPP/1.05VS VGA
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Optimus: PR801
DIS: PR802

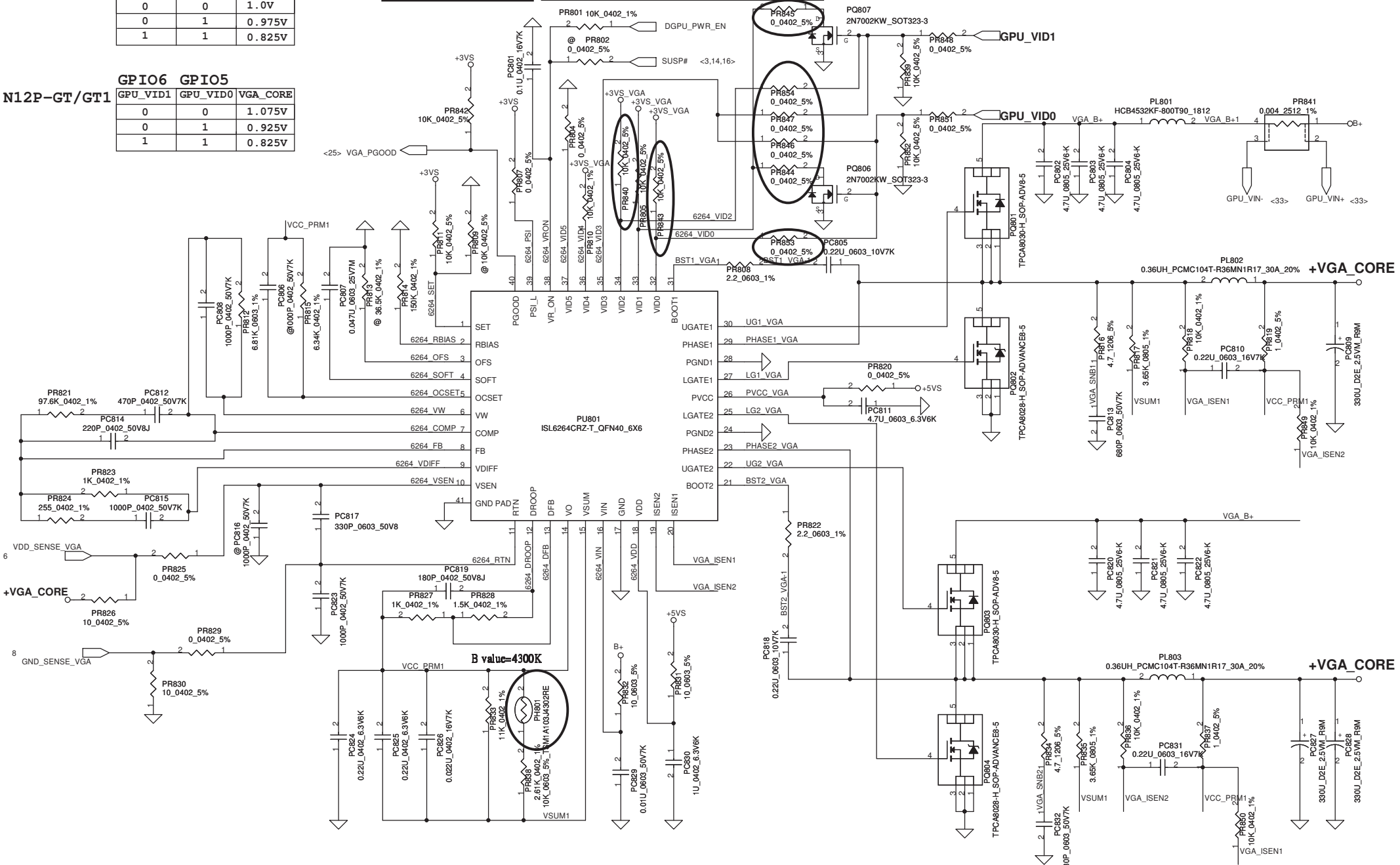
CS: PR840, PR845, PR847, PR858
GT/GT1: PR843, PR844, PR846, PR854

N12P-GS

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	1.0V
0	0	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	1.075V
0	0	0.925V
1	1	0.825V



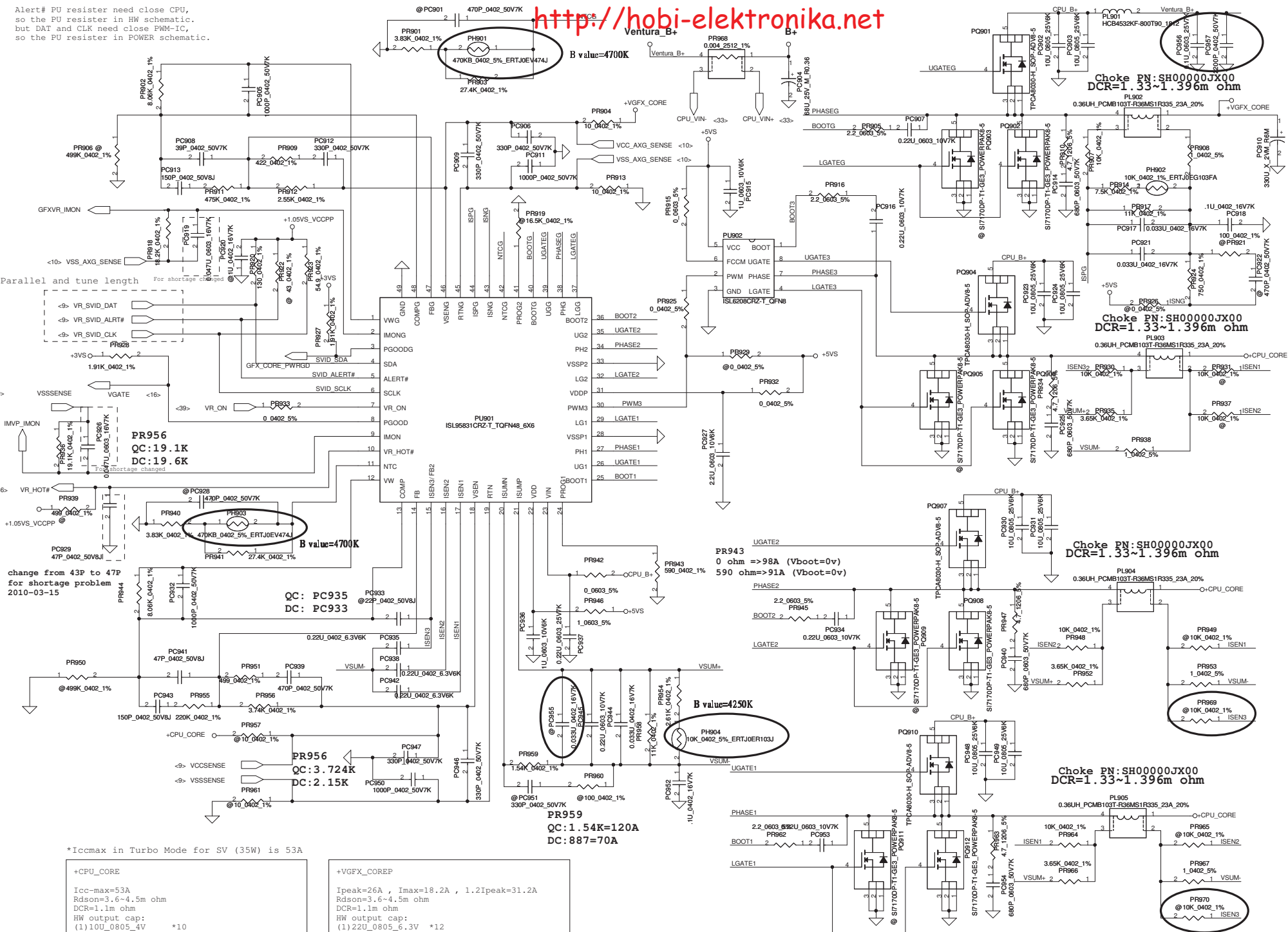
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Issued Date	2006/12/12	Deciphered Date
		2007/12/12

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Compal Electronics, Inc.		
Title	Power-VGA_CORE	
Size	Document Number	Rev
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Date:	Wednesday, October 06, 2010	Sheet 59 of 63

Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.

<http://hobi-elektronika.net>



Parallel and tune length
For shortage changed

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE
Icc-max=53A
Rdson=3.6-4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 10U_0805_4V *10
(2) 22U_0805_6.3V *15
(3) 470U_D2_2V *4 (ESR=4.5m ohm)

+VGFX_COREP
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A
Rdson=3.6-4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 22U_0805_6.3V *12
(2) 470U_D2_2V *2 (ESR=4.5m ohm)

*OCP setting value=71.5A

*OCP setting value=37A

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		2010/12/31

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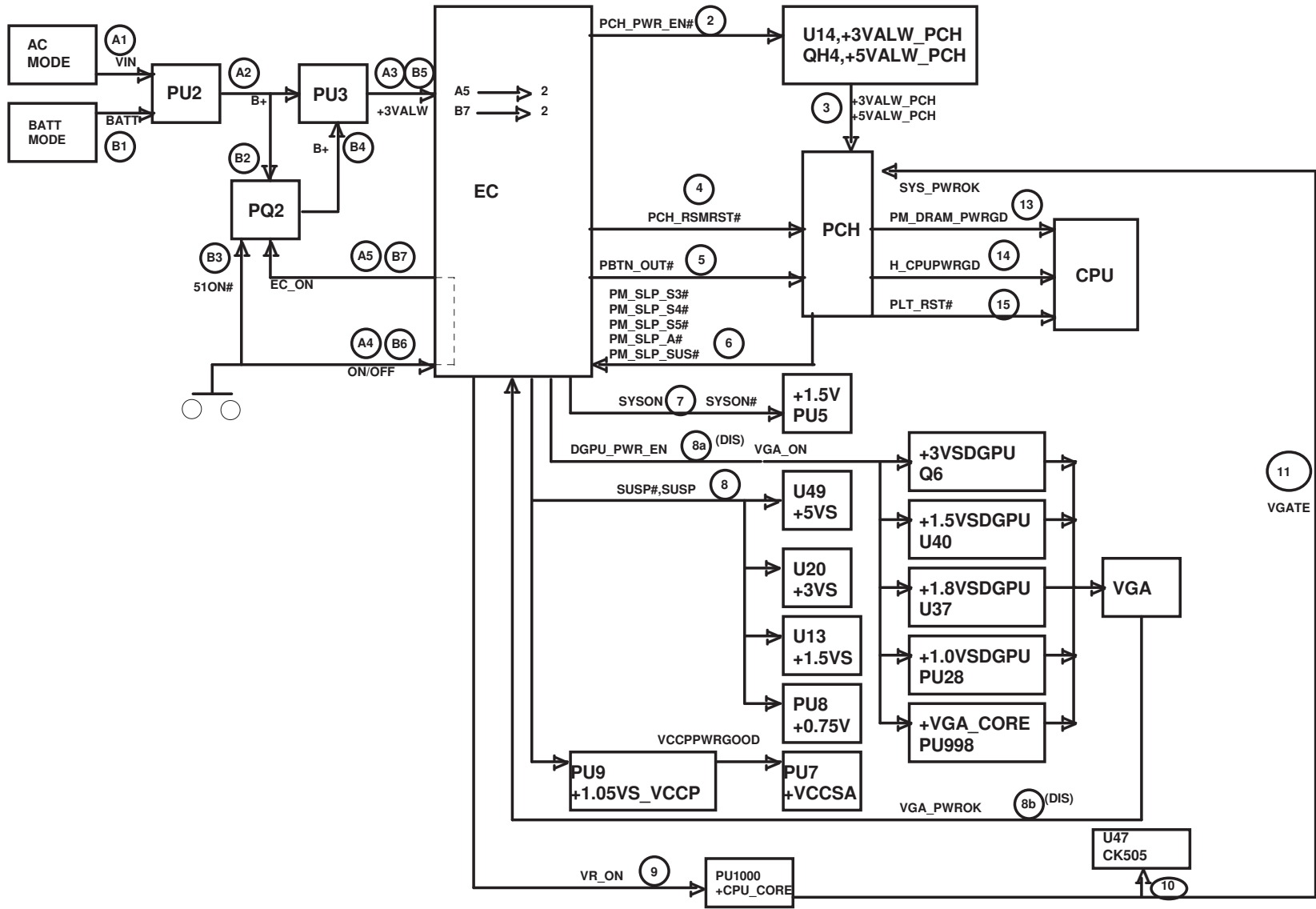
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PIQY1 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- EVT TO DVT				
1		P18	Reserve R297	Reserve pull down for PCH GPIO53.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GPIO1.
6		P49	Stuff R1068, reserve R1071, R1072, R1099, Q121	Reserve USB3.0 power swith control inverter circuit.
7		P48	Add R1154	For CHG_ON# pull down.
8		P45	Stuff R996, R139, C815, unstuff R1000, C732, C733, Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P09	Add C922	Add C922 to place at CPU sdie.
11		P21	Add R1330	Add for INTVREN control
12		P47	Modify LED1, LED2, LED3, LED5	Change LED type
13		P45	Modify TP_LED#, PCH_DPWR0K and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GPIO12.
14		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
15		P48	Delete USB charger circuit	Remove USB charger function
16		P47	Modify H5, H6, H7 size	From H_3P0 to H_3P8
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C926, C927 0.033u	For 100Hz High Pass filter
19		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
20		P42	Add C928, C929	EMI Request
21		P49	Add J19	for USB30, USB20 colayout design
			Modify J18, J20	for USB30, USB20 colayout design
22		P14	Add Q134, R1347, R1346	Add for Fast boot SPI ROM selection by EC.
23		P37, P44	Add R1344, R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1345	Added for VENTURA detection.

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