CM6802SAH/SBH (Turbo-Speed PFC+Green PWM)

EPA/85+ ZVS-Like PFC+PWM COMBO CONTROLLER

Design for High Efficient Power Supply at both Full Load and Light Load

GENERAL DESCRIPTION

CM6802SAH/SBH is a turbo-speed PFC and a Green PWM controller. It is designed to further increase power supply efficiency while using the relatively lower 380V Bulk Capacitor value.
Switching to CM6802SAH/SBH from your existing CM6800 family boards can gain the following advanced performances:

1.) Around 2% efficiency gain when the output load is below 40% of the full load
2.) Hold Up time can be increased ~ 30% from the existing 6800 power supply
3.) Turbo Speed PFC may reduce 420 Bulk Capacitor size
4.) 420V bulk capacitor value may be reduced and PFC Boost Capacitor ripple current can be reduced
5.) No Load Consumption can be reduced 290mW at 270VAC
6.) Better Power Factor and Better THD
7.) Clean Digital PFC Brown Out
8.) PWM transformer size can be smaller
9.) Superior Surge Noise Immunity
10.) To design 12V, 5V, and 3.3V output filters can be easy
11.) The stress over the entire external power device is reduced and EMI noise maybe reduced; PFC inductor core might be reduced
12.) Monotonic Output design is easy
13.) And more… Of course, the cost can be reduced

CM6802SAH/SBH is pin to pin compatible with CM6800 family.
Beside all the goodies in the CM6800, it is designed to meet the EPA/85+ regulation. With the proper design, its efficiency of power supply can easily approach 85%.

To start evaluating CM6802SAH/SBH from the exiting CM6800, CM6800A, or ML4800 board, 6 things need to be taken care before doing the fine tune:

1.) Change RAC resistor (on pin 2, IAC) from the old value to a higher resistor value between 4.7 Mega ohm to 8 Mega ohm. Start with 6 Mega ohm for RAC first.
2.) Change RTCT pin (pin 7) from the existing value to RT=5.88K ohm and CT=1000pF to have fpfc=68Khz, fpwm=68Khz, frtct=272Khz for CM6802SAH and fpfc=68Khz, fpwm=136Khz, frtct=272Khz for CM6802SBH
3.) Adjust all high voltage resistor around 5 mega ohm or higher.
4.) VRMS pin(pin 4) needs to be 1.14V at VIN=80VAC for universal input application from line input from 80VAC to 270VAC. Both poles for the Vrms of the CM6802SAH/SBH needs to substantially slow than CM6800 about 5 to 10 times.
5.) At full load, the average Veao needs to around 4.5V and the ripple on the Veao needs to be less than 250mV when the load triggers the light load comparator.
6.) Soft Start pin (pin 5), the soft start current has been reduced from CM6800's 20uA to CM6802SAH/SBH's 10uA.Soft Start capacitor can be reduced to 1/2 from your original CM6800 capacitor.

FEATURES

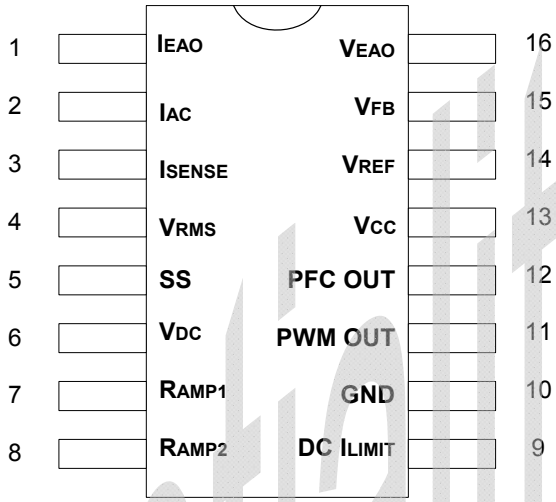
- Patents Pending
- Pin to pin compatible with CM6800, CM6800A, ML4800, and FAN4800
- 23V Bi-CMOS process
- Designed for EPA/85+ efficiency
- Selectable Boost output from 380V to 342V during light load
- Digitized Exactly 50% Maximum PWM Duty Cycle
- All high voltage resistors can be greater than 4.7 Mega ohm (4.7 Mega to 8 Mega ohm) to improve the no load consumption
- Rail to rail CMOS Drivers with on, 60 ohm and off, 30 ohm for both PFC and PWM with two 17V zeners
- Fast Start-UP Circuit without extra bleed resistor to aid VCC reaches 13V sooner
- Low start-up current (55uA typ.)
- Low operating current (2.5mA typ.)
- 16.5V VCC shunt regulator
- Leading Edge Blanking for both PFC and PWM
- fRTCT = 4*fpfc =4*fpwm for CM6802SAH
- fRTCT = 4*fpfc =2*fpwm for CM6802SBH
- Dynamic Soft PFC to ease the stress of the Power Device and Ease the EMI filter design
- Clean Digital PFC Brown Out and PWM Brown Out
- Turbo Speed PFC may reduce 420 Bulk Capacitor size
- Internally synchronized leading edge PFC and trailing edge PWM in one IC to Reduces ripple current in the 420V storage capacitor between the PFC and PWM sections
- Better Power Factor and Better THD
- Average current, continuous or discontinuous boost leading edge PFC
- PWM configurable for current mode or feed-forward voltage mode operation
- Current fed Gain Modulator for improved noise immunity
- Gain Modulator is a constant maximum power limiter
- Precision Current Limit, over-voltage protection, UVLO, soft start, and Reference OK

APPLICATIONS

- EPA/85+ related Power Supply
- Desktop PC Power Supply
- Internet Server Power Supply
- LCD Power Supply
- PDP Power Supply
- IPC Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

PIN CONFIGURATION

SOP-16 (S16) / PDIP-16 (P16)



PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	I_{EAO}	PFC transconductance current error amplifier output **(Gmi).**	0		VREF	V
2	I_{AC}	IAC has 2 functions: 1. PFC gain modulator reference input. 2. Typical RAC resistor is about 6 Mega ohm to sense the line.	0		100	uA
3	I_{SENSE}	PFC Current Sense: for both Gain Modulator and PFC ILIMIT comparator.	-1.2		0.7	V
4	V_{RMS}	Line Input Sense pin and also, it is the brown out sense pin.	0		VCC+0.3	V
5	SS	Soft start capacitor pin; can use it to on/off the boost follower function; it is pulled down by 70K ohm internal resistor when DCILIMIT reach 1V; the power is limited during the PWM Brown out.	0		10	V

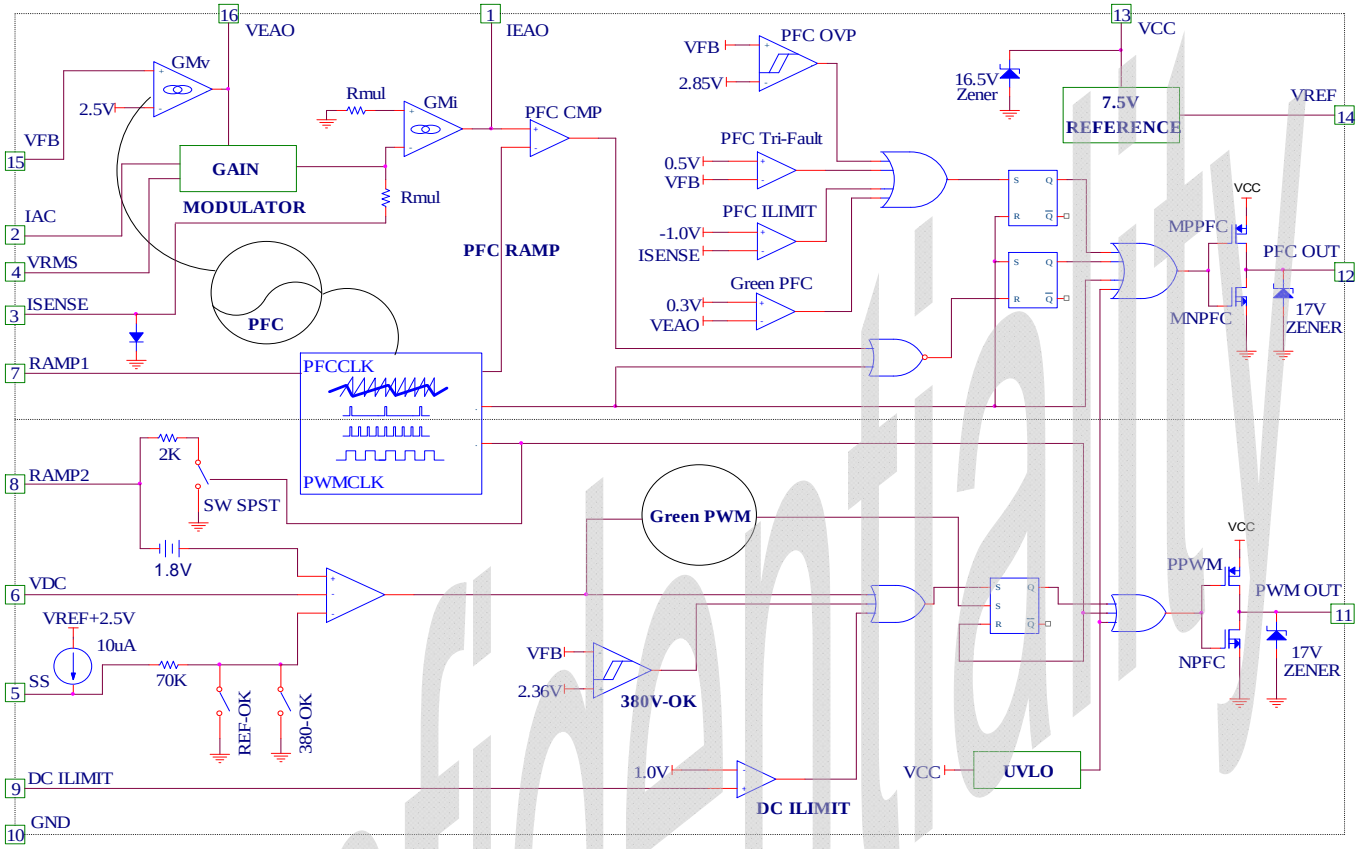
6	**V_{DC}**	DC to DC PWM voltage feedback input.	0		10	V
7	**RAMP1 (RTCT)**	Oscillator timing node; timing set by RT and CT	0.8		4	V
8	**RAMP 2 (PWM RAMP)**	In current mode, this pin functions as the current sense input; when in voltage mode, it is the feed-forward sense input from PFC output 380V (feed forward ramp).	0		V_{DCmax}-1.8	V
9	**DC I_{LIMIT}**	PWM current limit comparator input	0		1	V
10	**GND**	Ground				
11	**PWM OUT**	PWM driver output	0		VCC	V
12	**PFC OUT**	PFC driver output	0		VCC	V
13	**V_{CC}**	Positive supply for CM6802SAH/SBH	10	15	20	V
14	**VREF**	Maximum 3.5mA buffered output for the internal 7.5V reference when VCC=14V		7.5		V
15	**V_{FB}**	PFC transconductance voltage error amplifier input	0	2.5	3	V
16	**VEAO**	PFC transconductance voltage error amplifier output **(GmV)**	0		6	V

ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6802SAH/SBHGIP*	-40℃ to 125℃	16-Pin PDIP (P16)
CM6802SAH/SBHGIS*	-40℃ to 125℃	16-Pin Narrow SOP (S16)
CM6802SAH/SBHGISTR*	-40℃ to 125℃	16-Pin Narrow SOP (S16)
CM6802SAH/SBHXIP*	-40℃ to 125℃	16-Pin PDIP (P16)
CM6802SAH/SBHXIS*	-40℃ to 125℃	16-Pin Narrow SOP (S16)
CM6802SAH/SBHXISTR*	-40℃ to 125℃	16-Pin Narrow SOP (S16)

***Note:** G : Suffix for Pb Free Product
X : Suffix for Halogen Free Product
TR : Package is Typing Reel

Simplified Block Diagram (CM6802SAH/SBH)



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC}		20	V
IEAO	0	VREF+0.3	V
I_{SENSE} Voltage	-5	0.7	V
PFC OUT	GND – 0.3	VCC + 0.3	V
PWMOUT	GND – 0.3	VCC + 0.3	V
Voltage on Any Other Pin	GND – 0.3	VCC + 0.3	V
I_{REF}		3.5	mA
I_{AC} Input Current		1	mA
Peak PFC OUT Current, Source or Sink		0.5	A
Peak PWM OUT Current, Source or Sink		0.5	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA}) Plastic DIP Plastic SOIC		 80 105	 ℃/W ℃/W
Power Dissipation (PD) T_A<50℃		800	mW
ESD Capability, HBM Model		5.5	KV
ESD Capability, CDM Model		1250	V

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply Vcc=+14V, R_T = 5.88 kΩ, C_T = 1000pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6802SAH/SBH			Unit
			Min.	Typ.	Max.	
Clean Digital PFC Brown Out						
	VRMS Threshold High	Room Temperature=25℃	1.70	1.78	1.88	V
	VRMS Threshold Low	Room Temperature=25℃	0.978	1.03	1.081	V
	Hysteresis		710	760	810	mV
	AC High Line	Sweep Vrms Pin	2.81	3	3.19	V
	AC Low Line	Sweep Vrms Pin	1.86	2	2.14	V
	Hysteresis		0.91	1	1.09	V
Voltage Error Amplifier (g_{mv})						
	Input Voltage Range		0		3	V
	Transconductance	V_{NONINV} = V_{INV}, VEAO = 2.25V @ T=25℃	40	50	65	μmho
	Feedback Reference Voltage (High)	SS < VREF and Veao > 2.25V and Vrms<2V	2.45	2.52	2.58	V
	Feedback Reference Voltage (Low)	SS > VREF and Veao < 1.75V and Vrms<2V	2.17	2.26	2.35	V
Light Load Veao Threshold						
	Light Load Threshold (High)	Room Temperature=25℃	2.15	2.25	2.38	V
	Light Load Threshold (Low)	Room Temperature=25℃	1.67	1.75	1.88	V
	Hysteresis		450		650	mV
	Input Bias Current	Note 2	-1.0	-0.05		μA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V_{FB} = 1.5V, VEAO = 1.5V	-65	-53	-40	μA
	Source Current	V_{FB} = 2.5V, VEAO = 3.75V	1.5	3.5	6	μA
	Open Loop Gain	DC gain	30	40		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB

ELECTRICAL CHARACTERISTICS:

(Conti.) Unless otherwise stated, these specifications apply Vcc=+14V, R_T = 5.88 kΩ, C_T = 1000pF, T_A=OperatingTemperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6802SAH/SBH			Unit
			Min.	Typ.	Max.	
Current Error Amplifier (g_{mi})						
	Input Voltage Range (Isense pin)		-1.2		0.7	V
	Transconductance	V_{NONINV} = V_{INV}, IEAO = 1.5V @ T=25℃	50	67	85	μmho
	Input Offset Voltage	VEAO=0V, IAC is open	-10		50	mV
	Output High Voltage		6.8	7.4	7.7	V
	Output Low Voltage			0.1	0.4	V
	Sink Current	I_{SENSE} = -0.5V, IEAO = 1.5V @ T=25℃	-40	-35.5	-28.4	μA
	Source Current	I_{SENSE} = +0.5V, IEAO = 4.0V @ T=25℃	25.2	32	40	μA
	Open Loop Gain	DC Gain	30	40		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	60	75		dB
PFC OVP Comparator						
	Threshold Voltage		2.70	2.85	3.0	V
	Hysteresis		200		320	mV
PFC Green Power Detect Comparator						
	Veao Threshold Voltage		0.17	0.28	0.4	V
Tri-Fault Detect						
	Fault Detect HIGH		2.70	2.85	3.0	V
	Time to Fault Detect HIGH	V_{FB}=$V_{FAULT\ DETECT\ LOW}$ to V_{FB}=OPEN, 470pF from V_{FB} to GND		2	4	ms
	Fault Detect Low		0.1	0.28	0.4	V
PFC I_{LIMIT} Comparator						
	Threshold Voltage		-1.10	-1.00	-0.90	V
	($PFCI_{LIMIT}$– Gain Modulator Output)		70	200		mV
	Delay to Output (Note 4)	Overdrive Voltage = -100mV		700		ns

ELECTRICAL CHARACTERISTICS:

(Conti.) Unless otherwise stated, these specifications apply Vcc=+14V, R_T = 5.88 kΩ, C_T = 1000pF, T_A=OperatingTemperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6802SAH/SBH			Unit
			Min.	Typ.	Max.	
DC I_{LIMIT} Comparator						
	Threshold Voltage		0.92	1.0	1.08	V
	Delay to Output (Note 4)	Overdrive Voltage = 100mV		700		ns
DC to DC PWM Brown Out Comparator						
	OK Threshold Voltage		2.1	2.3	2.5	V
	Hysteresis		900	950	1000	mV
GAIN Modulator						
	Gain1 (Note 3)	I_{AC} = 20 μA, V_{RMS} =1.125, V_{FB} = 2.375V @ T=25℃ SS<VREF	5.05	5.7	6.35	
	Gain2 (Note)3	I_{AC} = 20 μA, V_{RMS} = 1.45588V, V_{FB} = 2.375V @ T=25℃ SS<VREF	4.54	5.1	5.66	
	Gain3 (Note 3)	I_{AC} = 20 μA, V_{RMS} =2.91V, V_{FB} = 2.375V @ T=25℃ SS<VREF	1.27	1.5	1.72	
	Gain4 (Note 3)	I_{AC} = 20 μA, V_{RMS} = 3.44V, V_{FB} = 2.375V @ T=25℃ SS<VREF	0.93	1.1	1.26	
	Bandwidth (Note 4)	I_{AC} = 40 μA		1		MHz
	Output Voltage = Rmul * (I_{SENSE}-I_{OFFSET})	I_{AC} = 50 μA, V_{RMS} = 1.125V, V_{FB} = 2V SS<VREF	0.74	0.8	0.86	V
Oscillator (Measuring fpfc)						
	Initial fpfc Accuracy 1	R_T = 5.88 kΩ, C_T = 1000pF, T_A = 25℃ IAC=0uA	64	68	72	kHz
	Voltage Stability	11V < V_{CC} < 16.5V		2		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	60		75	kHz
	Ramp Valley to Peak Voltage	VEAO=6V and IAC=20uA		2.5		V
	PFC Dead Time (Note 4)		550		950	ns
	CT Discharge Current	V_{RAMP2} = 0V, V_{RAMP1} = 2.5V	10	11	12	mA

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

Vcc=+14V, R_T = 5.88 kΩ, C_T = 1000pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6802SAH/SBH			Unit
			Min.	Typ.	Max.	
Reference						
	Output Voltage	T_A = -45℃~85℃, I(VREF) = 0~3.5mA	7.3	7.5	7.7	V
	Line Regulation	11V < V_{CC} < 16.5V@ T=25℃		3	5	mV
	Load Regulation	VCC=10.5V,0mA < I(VREF) < 2mA; @ T=25℃		25	50	mV
		VCC=14V,0mA < I(VREF) < 3.5mA; T_A = -40℃~85℃		25	50	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.3		7.7	V
	Long Term Stability	T_J = 125℃, 1000HRs	5		25	mV
PFC						
	Minimum Duty Cycle	IEAO > 4.5V			0	%
	Maximum Duty Cycle	V_{IEAO} < 1.2V	93	95		%
	Output Low Rdson	I_{OUT} = -20mA @ T=25℃		11.8	15	ohm
		I_{OUT} = -100mA @ T=25℃			18	ohm
		I_{OUT} = 10mA, V_{CC} = 9V @ T=25℃		0.5	1	V
	Output High Rdson	I_{OUT} = 20mA @ T=25℃		24	30	ohm
		I_{OUT} = 100mA @ T=25℃			40	ohm
	Rise/Fall Time (Note 4)	C_L = 100pF @ T=25℃		50		ns
PWM						
	Duty Cycle Range		0-49.5		0-50	%
	Output Low Rdson	I_{OUT} = -20mA @ T=25℃		11.8	15	ohm
		I_{OUT} = -100mA @ T=25℃			18	ohm
		I_{OUT} = 10mA, V_{CC} = 9V		0.5	1	V
	Output High Rdson	I_{OUT} = 20mA @ T=25℃		26.5	40	ohm
		I_{OUT} = 100mA @ T=25℃			40	ohm
	Rise/Fall Time (Note 4)	C_L = 100pF		50		ns
	PWM Comparator Level Shift	@ T=25℃	1.6	1.8	2	V
Soft Start						
	Soft Start Current	Room Temperature=25℃	7	8.5	10.5	μA
Supply						
	Start-Up Current	V_{CC} = 12V, C_L = 0 @ T=25℃		50	65	μA
	Operating Current	14V, C_L = 0		2.35	3.5	mA
Turn-on	Undervoltage Lockout Threshold	CM6802SAH/SBH	12.35	12.85	13.65	V
Turn-off	Undervoltage Lockout Hysteresis	CM6802SAH/SBH	2.8	2.95	3.1	V
Shunt Regulator (VCC zener)						
	Zener Threshold Voltage	Apply VCC with Iop=20mA	16.15	17	17.85	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the V_{FB} pin.

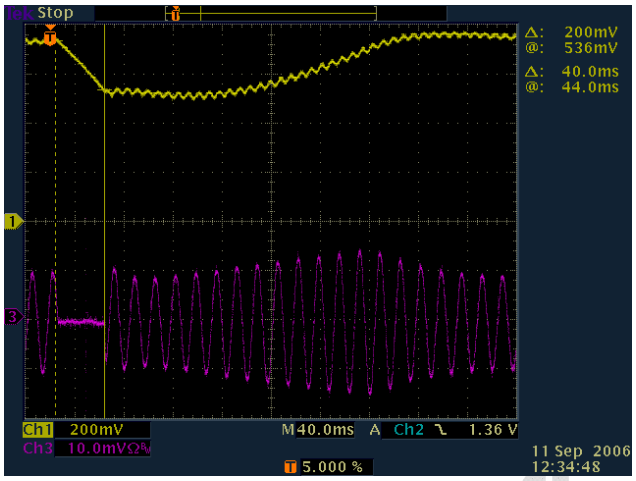
Note 3: Gain ~ K x 5.3V; K = (I_{SENSE} – I_{OFFSET}) x [I_{AC} (VEAO – 0.7)]$^{-1}$; $VEAO_{MAX}$ = 6V

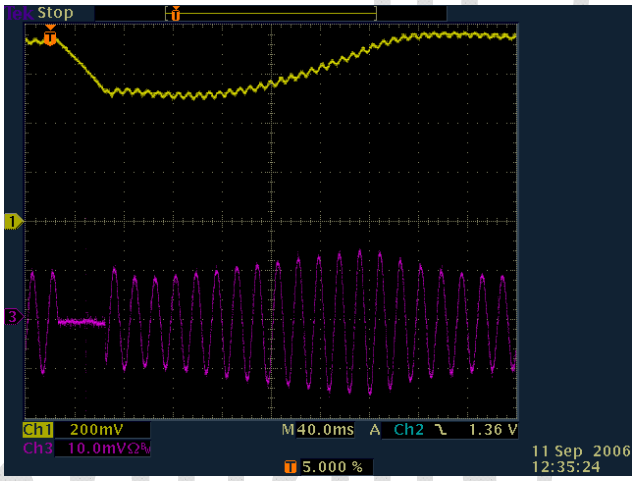
Note 4: Guaranteed by design, not 100% production test.

TYPICAL PERFORMANCE CHARACTERISTIC:

PFC Soft Diagram :

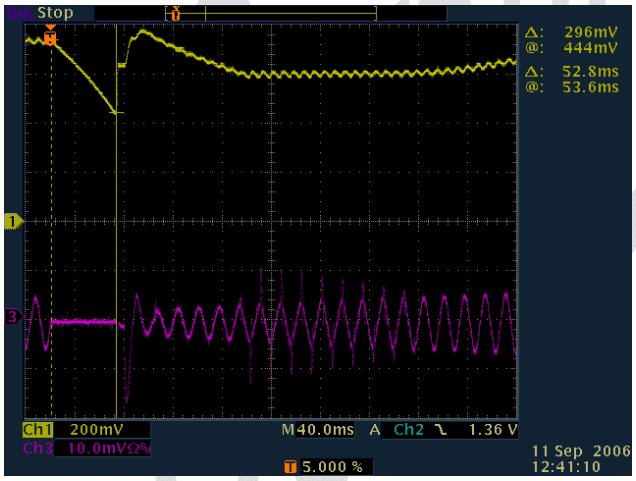
Dynamic Soft PFC Performance @ Vin=110 Vac

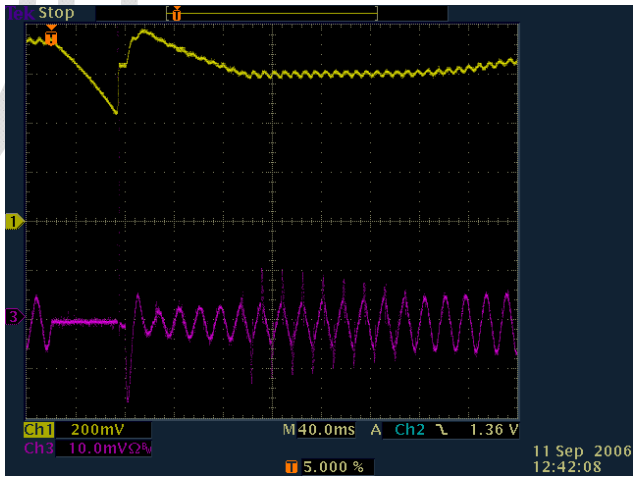




Ch1 is 380V bulk cap voltage which is 100V/div.
Ch3 is Input Line Current which is 1A/div.
Input Line Voltage (110 Vac) was turned off for 40mS before reaching PWM Brownout which is 209Vdc. When the bulk cap voltage goes below 209V, the system will reset the PWM soft start. The result of the CM6802SAH/SBH Input Line Current has a clean Off and softly On even the system does not reset PWM soft-start.

Dynamic Soft PFC Performance @ Vin=220 Vac

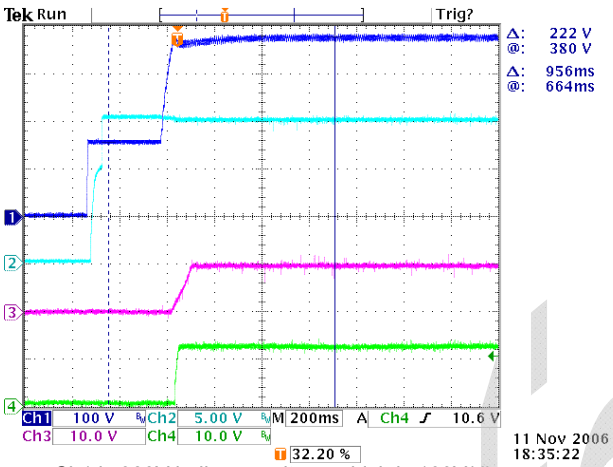




Ch1 is 380V bulk cap voltage which is 100V/div.
Ch3 is Input Line Current which is 1A/div.
Input Line Voltage (220 Vac) was turned off for 40mS before reaching PWM Brownout which is 209Vdc when Bulk cap voltage drops below 209V. When the bulk cap voltage goes below 209V, the system will reset the PWM soft start. The result of the CM6802SAH/SBH Input Line Current has a clean Off and softly On even the system does not reset itself. The first peak current at the beginning of the On time is the inrush current.

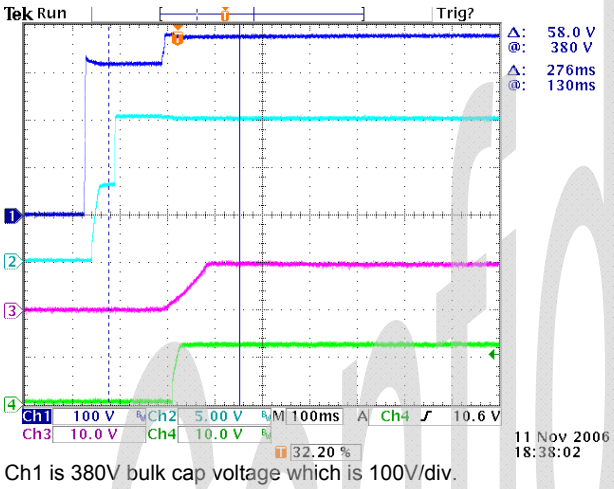
Turn on Timing :

Output 50% and 100% load turn on waveform at 110Vac



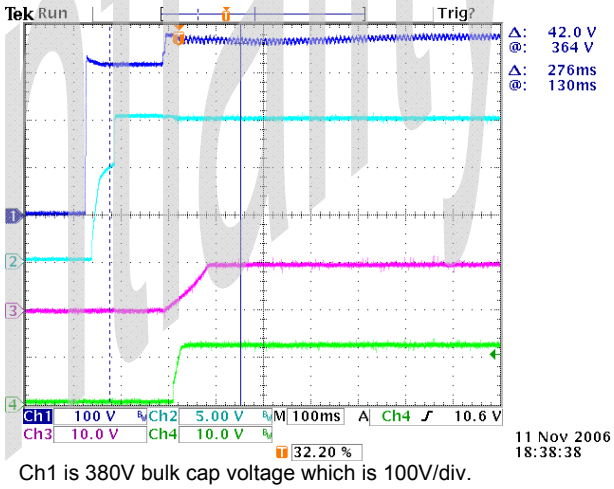
Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V).

Output 10% and 20% load turn on waveform at 230Vac



Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V)

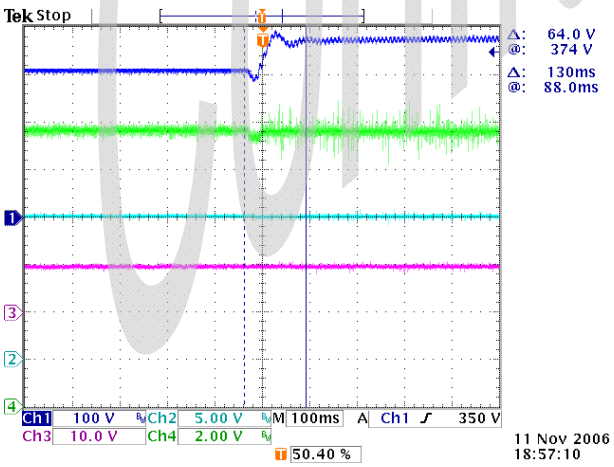
Output 50% and 100% load turn on waveform at 230Vac



Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V)

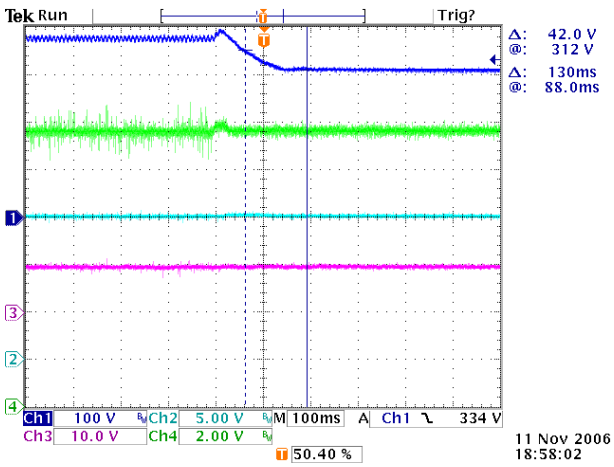
Dynamic load:

Output step load 10% to 100% load at 90Vac



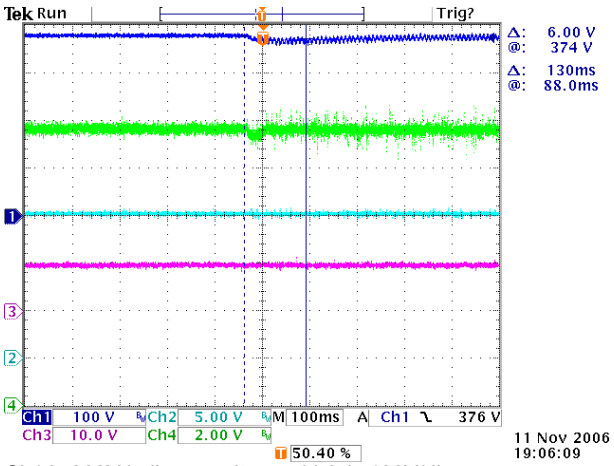
Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V)

Output step 100% load to 10% load at 90Vac



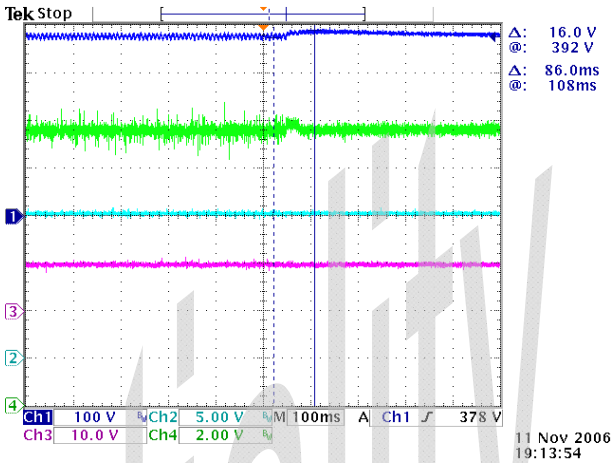
Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V)

Output step load 10% to 100% load at 230Vac



Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V)

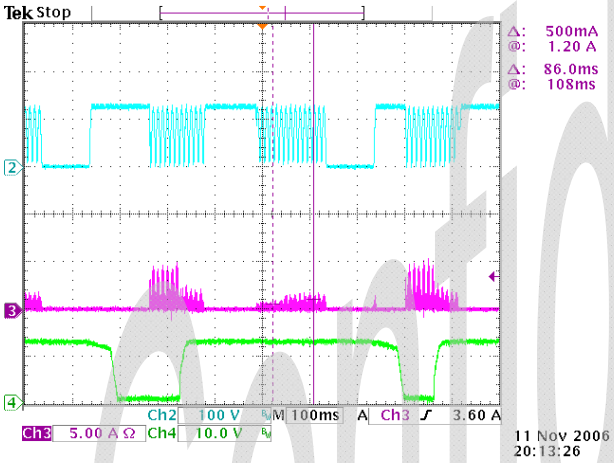
Output step 100% load to 10% load at 230Vac



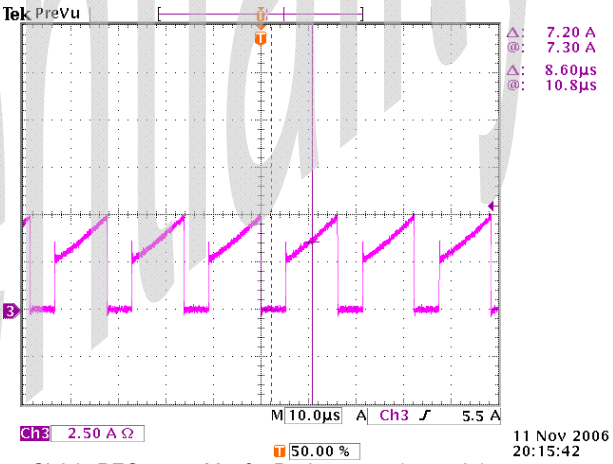
Ch1 is 380V bulk cap voltage which is 100V/div.
Ch2 is VCC,Ch3 is SS(soft start pin),CH4 is Vo(12V)

AC power cycling :

90VAC turn on 500ms turn off 100ms at 10%LOAD

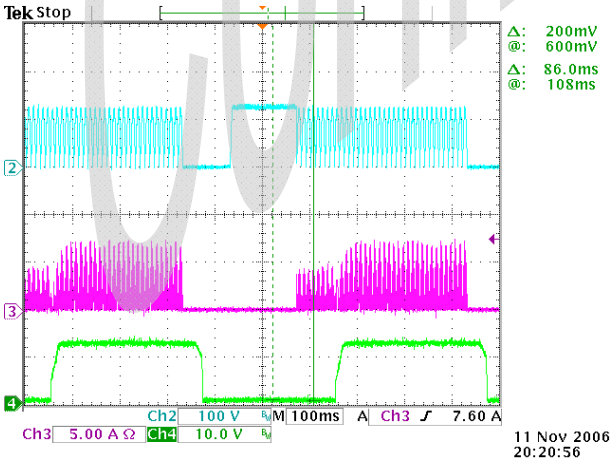


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo(12V)

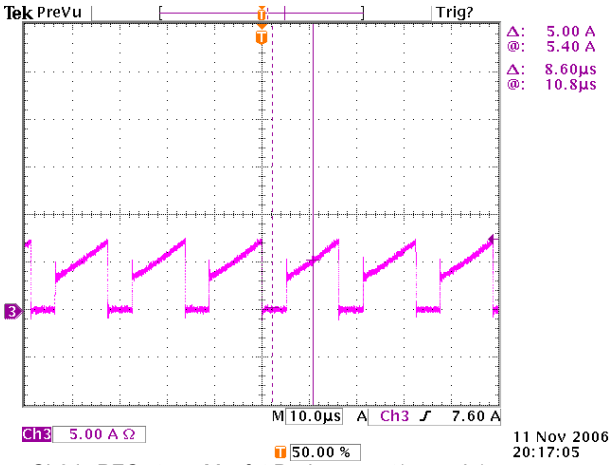


Ch3 is PFC stage Mosfet Drain current(zoom In)

90VAC turn on 500ms turn off 100ms at 100%LOAD

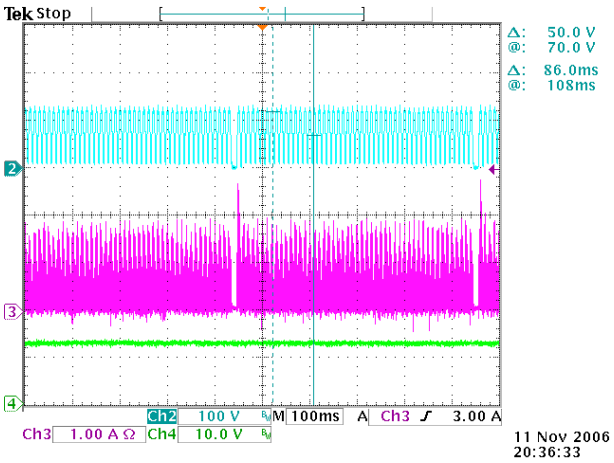


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo(12V)

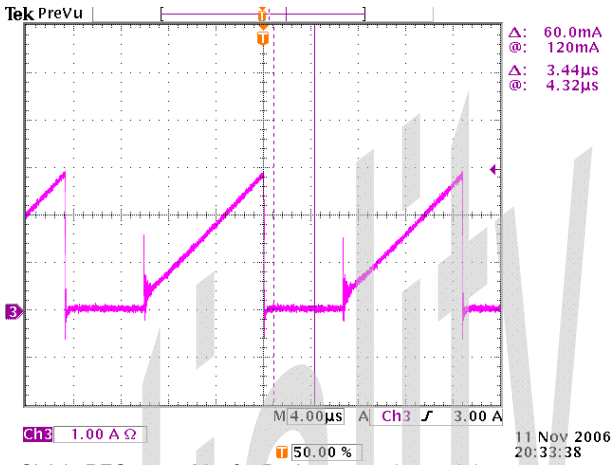


Ch3 is PFC stage Mosfet Drain current(zoom In)

90VAC turn on 500ms turn off 10ms at 10%LOAD

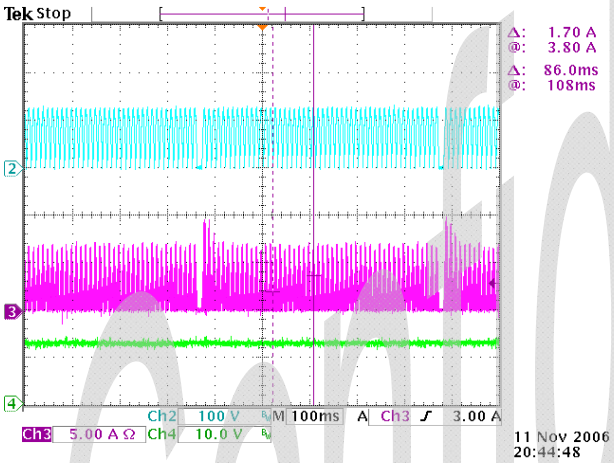


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo (12V)

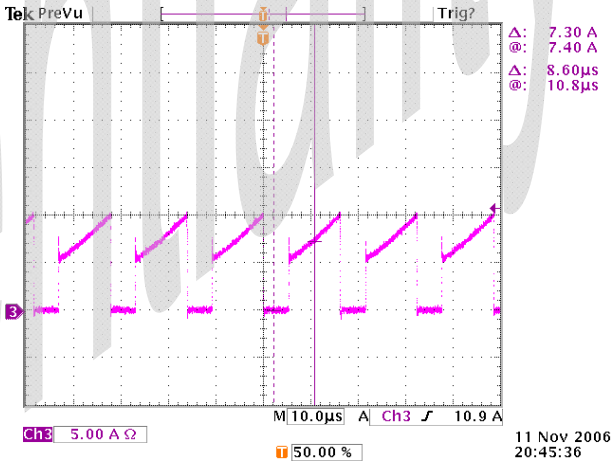


Ch3 is PFC stage Mosfet Drain current (zoom In)

90VAC turn on 500ms turn off 10ms at 100%LOAD

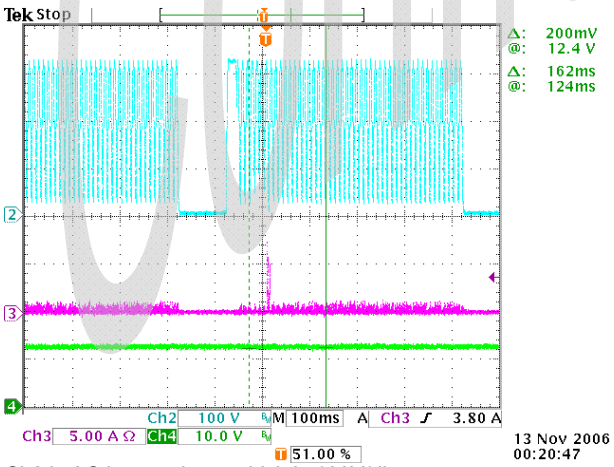


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo (12V)

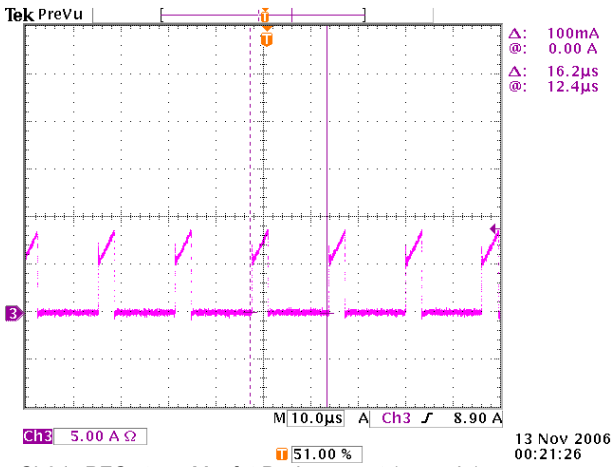


Ch3 is PFC stage Mosfet Drain current (zoom In)

230VAC turn on 500ms turn off 100ms at 10%LOAD

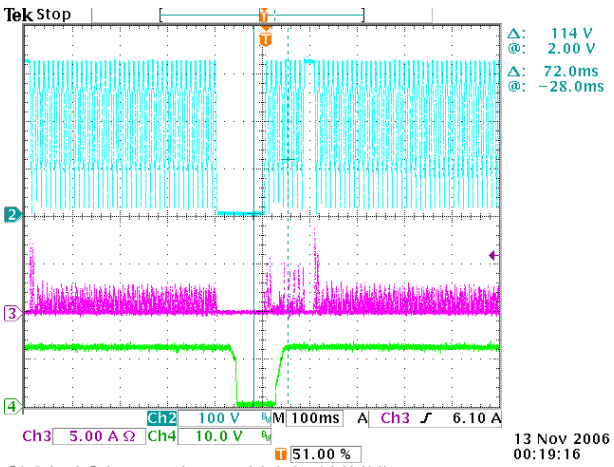


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo (12V)

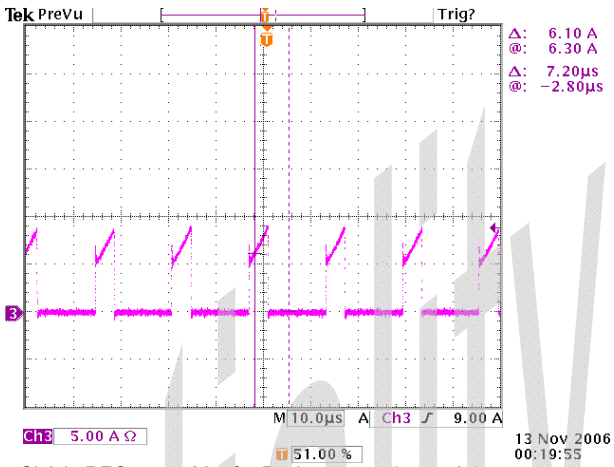


Ch3 is PFC stage Mosfet Drain current (zoom In)

230VAC turn on 500ms turn off 100ms at 100%LOAD

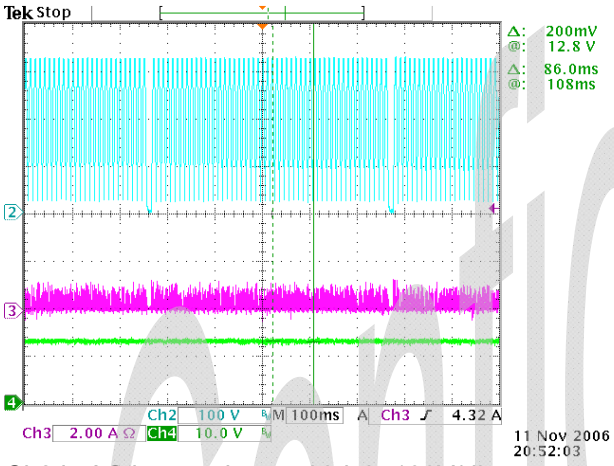


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo (12V)

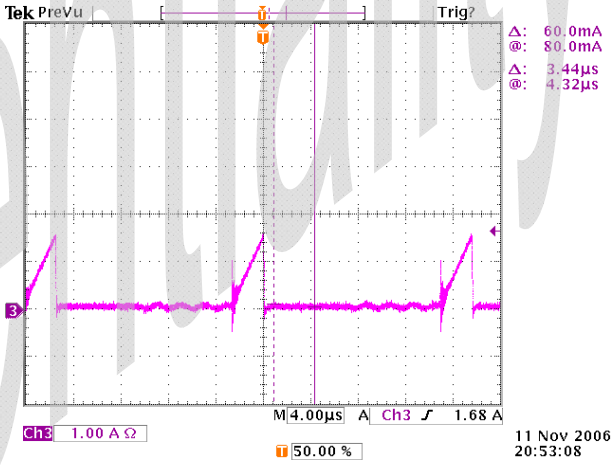


Ch3 is PFC stage Mosfet Drain current (zoom In)

230VAC turn on 500ms turn off 10ms at 10%LOAD

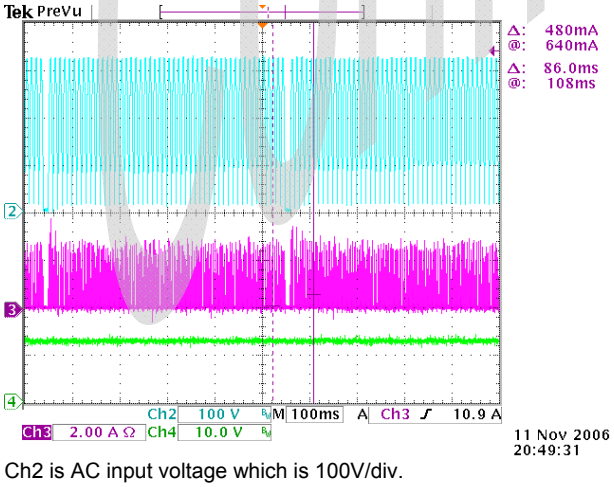


Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo (12V)

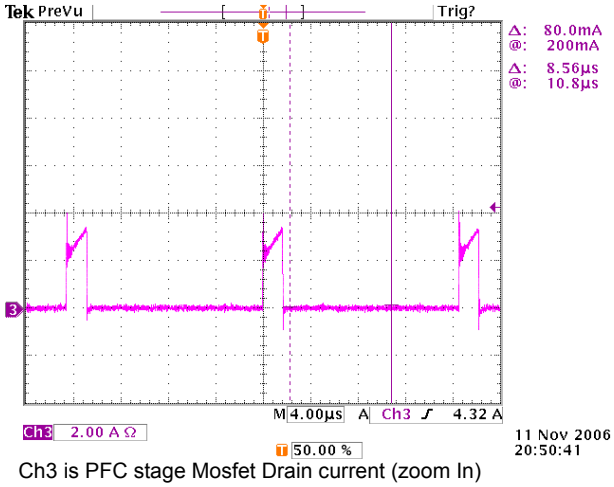


Ch3 is PFC stage Mosfet Drain current (zoom In)

230VAC turn on 500ms turn off 10ms at 100%LOAD



Ch2 is AC input voltage which is 100V/div.
Ch3 is PFC stage Mosfet drain current, CH4 is Vo (12V)



Ch3 is PFC stage Mosfet Drain current (zoom In)

Getting Start:

To start evaluating CM6802SAH/SBH from the exiting CM6800 or ML4800 board, 6 things need to be taken care before doing the fine tune:

1.) Change RAC resistor (on pin 2, IAC) from the old value to a higher resistor value between 4.7 Mega ohms to 8 Mega ohms.
2.) Change RTCT pin (pin 7) from the existing value to RT=5.88K ohm and CT=1000pF to have fpfc=68 Khz, fpwm=68Khz, fRTCT=272Khz for CM6802SAH and fpfc=68Khz, fpwm=136Khz, fRTCT=272Khz for CM6802SBH.
3.) Adjust all high voltage resistor around 5 mega ohm or higher.
4.) VRMS pin (pin 4) needs to be 1.14V at VIN=80Vac and to be 1.21V at VIN=80VAC for universal input application from line input from 80VAC to 270VAC.
5.) At full load, the average Veao needs to around 4.5V and the ripple on the Veao needs to be less than 250mV when the light load comparator are triggerred.
6.) Soft Start pin (pin 5), the soft start current has been reduced from CM6800's 20uA to CM6802SAH/SBH's 10uA.Soft Start capacitor can be reduced to 1/2 from your original CM6800 capacitor.

Functional Description

CM6802SAH/SBH is designed for high efficient power supply for both full load and light load. It is a popular EPA/85+ PFC-PWM power supply controller.

The CM6802SAH/SBH consists of an average current controlled continuous/discontinuous boost Power Factor Correction (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feed-forward from the PFC output bus can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing edge duty cycle modulation, while the PFC uses leading edge modulation. This patented leading/trailing edge modulation technique results in a higher usable PFC error amplifier bandwidth, and can significantly reduce the size of the PFC DC buss capacitor.

The synchronized of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). In addition to power factor correction, a number of protection features have been built into the CM6802SAH/SBH. These include soft-start, PFC over-voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6802SAH/SBH uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385V DC level); from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to 1/(Vin x Vin), which linearizes the transfer function of the system as the AC input to voltage varies.

Since the boost converter topology in the CM6802SAH/SBH PFC is of the current-averaging type, no slope compensation is required.

More exactly, the output current of the gain modulator is given by:

Dynamic Soft PFC (patent pending)

Besides all the goodies from CM6800A, Dynamic Soft PFC is the main feature of CM6802SAH/SBH. Dynamic Soft PFC is to improve the efficiency, to reduce power device stress, to ease EMI, and to ease the monotonic output design while it has the more protection such as the short circuit with power-foldback protection. Its unique sequential control maximizes the performance and the protections among steady state, transient and the power on/off conditions.

PFC Section:

Gain Modulator

Figure 1 shows a block diagram of the PFC section of the CM6802SAH/SBH. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and wave-shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at VRMS. The gain modulator's output is inversely proportional to V_{RMS}^2. The relationship between V_{RMS} and gain is illustrated in the Typical Performance Characteristics of this page.
3. The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general formula of the output of the gain modulator is:

$$I_{mul} = \frac{I_{AC} \times (VEAO - 0.7V)}{V_{RMS}^2} \text{ x constant} \qquad (1)$$

Gain=Imul/Iac

K=Gain/(VEAO-0.7V)

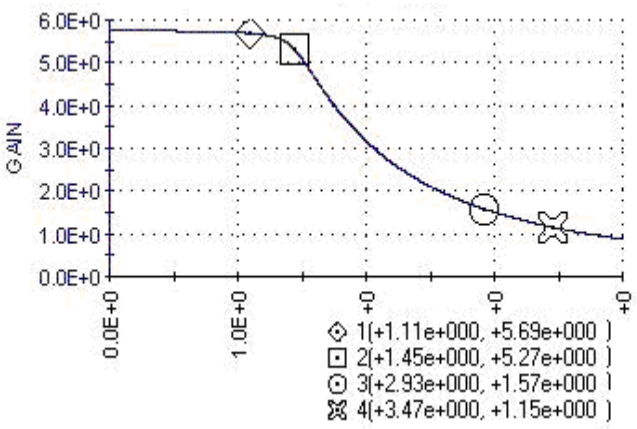
$I_{mul} = K \times (VEAO - 0.7V) \times I_{AC}$

Where K is in units of $[V^{-1}]$

Note that the output current of the gain modulator is limited around 100μA and the maximum output voltage of the gain modulator is limited to 100uA x 7.75K≒0.8V. This 0.8V also will determine the maximum input power.

However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE}. I_{SENSE} = $I_{GAINMOD}$-I_{OFFSET} and I_{OFFSET} can only be measured when VEAO is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 25uA.

IAC=20uA, Veao=6V



Gain vs. VRMS (pin4)

When VRMS below 1V, the PFC is shut off. Designer needs to design 80VAC with VRMS average voltage= 1.14V.

$$\text{Gain} = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}} = \frac{I_{MUL}}{I_{AC}}$$

Selecting R_{AC} for IAC pin

IAC pin is the input of the gain modulator. IAC also is a current mirror input and it requires current input. By selecting a proper resistor R_{AC}, it will provide a good sine wave current derived from the line voltage and it also helps program the maximum input power and minimum input line voltage.

R_{AC}=Vin min peak x 53.03K. For example, if the minimum line voltage is 80VAC, the R_{AC}=80 x 1.414 x 53.03K = 6 Mega ohm.

Vrms Description:

VRMS pin is designed for the following functions:

1. VRMS is used to detect the AC Brown Out (Also, we can call it Clean Digital PFC brown out.). When VRMS is less than 1.0 V +/-3%, PFCOUT will be turned off and VEAO will be softly discharged. When VRMS is greater than 1.75V +/-3%, PFCOUT is enabled and VEAO is released.
2. VRMS also is used to determine if the AC Line is high line or it is low line. If VRMS is above 3.0V +/- 5%, IC will recognize it is high line the. If VRMS is below 2.0V +/- 5%, it is low line. Between 2V <=~ Vrms <=~ 3.0, it is the hysteresis.
3. At High Line and Light Load, 380V to 342V (Vfb threshold moves from 2.5V to 2.25V) is prohibited. At Low Line and Light Load, 380V to 342V (Vfb threshold moves from 2.5V to 2.25V) is enable. It provides ZVS-Like performance.

Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin. The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

In higher power applications, two current transformers are sometimes used, one to monitor the IF of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the I_{SENSE} pin.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on I_{EAO} which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

Clean Digital PFC Brown Out

Clean Digital PFC Brown Out provides a clean cut off when AC input is much lower than regular AC input voltage such as 67Vac.

Inside of Clean Digital PFC Brown Out, there is a comparator monitors the Vrms (pin 4) voltage. Clean Digital PFC Brown Out inhibits the PFC, and Veao (PFC error amplifier output) is pulled down when the Vrms is lower than off threshold, 1.0V (The off Vin voltage usually corresponds to 67.2Vac). When the Vrms voltage reaches 1.75V (The On Vin voltage usually corresponds to 86.6V and when Vin = 80Vac, Vrms = 1.14V), PFC is on.

Before PFC is turned on, Vrms (pin 4) represents the peak voltage of the AC input. Before PFC is turned off, Vrms (pin 4) represents the Vrms voltage of the AC input.

Cycle-By-Cycle Current Limiter and Selecting R_{SENSE}

The I_{SENSE} pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than –1V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

R_S is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_{SENSE} = I_{mul} x 7.75K. Since the maximum output voltage of the gain modulator is I_{mul} max x 7.75K≒ 0.8V during the steady state, R_{SENSE} x line input current will be limited below 0.8V as well. When VEAO reaches maximum VEAO which is 6V, Isense can reach 0.8V. At 100% load, VEAO should be around 4.5V and ISENSE average peak is 0.6V. It will provide the optimal dynamic response + tolerance of the components.

Therefore, to choose R_{SENSE}, we use the following equation:

R_{SENSE} + $R_{Parasitic}$ =0.6V x Vinpeak / (2 x Line Input power)

For example, if the minimum input voltage is 80VAC, and the maximum input rms power is 200Watt, R_{SENSE} + $R_{Parasitic}$ = (0.6V x 80V x 1.414) / (2 x 200) = 0.169 ohm. The designer needs to consider the parasitic resistance and the margin of the power supply and dynamic response. Assume $R_{Parasitic}$ = 0.03Ohm, R_{SENSE} = 0.139Ohm.

PFC OVP

In the CM6802SAH/SBH, PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to VFB. When the voltage on VFB exceeds ~ 2.85V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB drops below ~ 2.55V. The VFB power components and the CM6802SAH/SBH are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop.

PFC Voltage Loop

There are two major concerns when compensating the voltage loop error amplifier, V_{EAO}; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency).

deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier, GMv will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristics.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$
$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GM_V: Transconductance of VEAO
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

PFC Current Loop

The current transcondutance amplifier, GMi, I_{EAO} compensation is similar to that of the voltage error amplifier, V_{EAO} with exception of the choice of crossover frequency. The crossover frequency of the

current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 8.33kHz for a 50kHz switching frequency.

The Current Loop Gain (S)

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} * \frac{\Delta D_{OFF}}{\Delta I_{EAO}} * \frac{\Delta I_{EAO}}{\Delta I_{SENSE}}$$
$$\approx \frac{V_{OUTDC} * R_S}{S * L * 2.5V} * GM_I * Z_{CI}$$

Z_{CI}: Compensation Net Work for the Current Loop
GM_I: Transconductance of IEAO
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V and we use the worst condition to calculate the Z_{CI}
R_{SENSE}: The Sensing Resistor of the Boost Converter
2.5V: The Amplitude of the PFC Leading Edge Modulation Ramp(typical)
L: The Boost Inductor

The gain vs. input voltage of the CM6802SAH/SBH's voltage error amplifier, V_{EAO} has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier, GMv is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier (V_{FB}) to I_{SENSE} Filter, the RC filter between R_{SENSE} and I_{SENSE} :

There are 2 purposes to add a filter at I_{SENSE} pin:

1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} Filter to attenuate the energy.

2.) To reduce L, the Boost Inductor: The I_{SENSE} Filter To reduce L, the Boost Inductor: The I_{SENSE} Filter also can reduce the Boost Inductor value since the I_{SENSE} Filter behaves like an integrator before going I_{SENSE} which is the input of the current error amplifier, IEAO.

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is between 100 ohm and 50 ohm because I_{OFFSET} x the resistor can generate an offset voltage of IEAO. By selecting R_{FILTER} equal to 50 ohm will keep the offset of the IEAO less than 5mV. Usually, we design the pole of I_{SENSE} Filter at fpfc/6=8.33Khz, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 381nF.

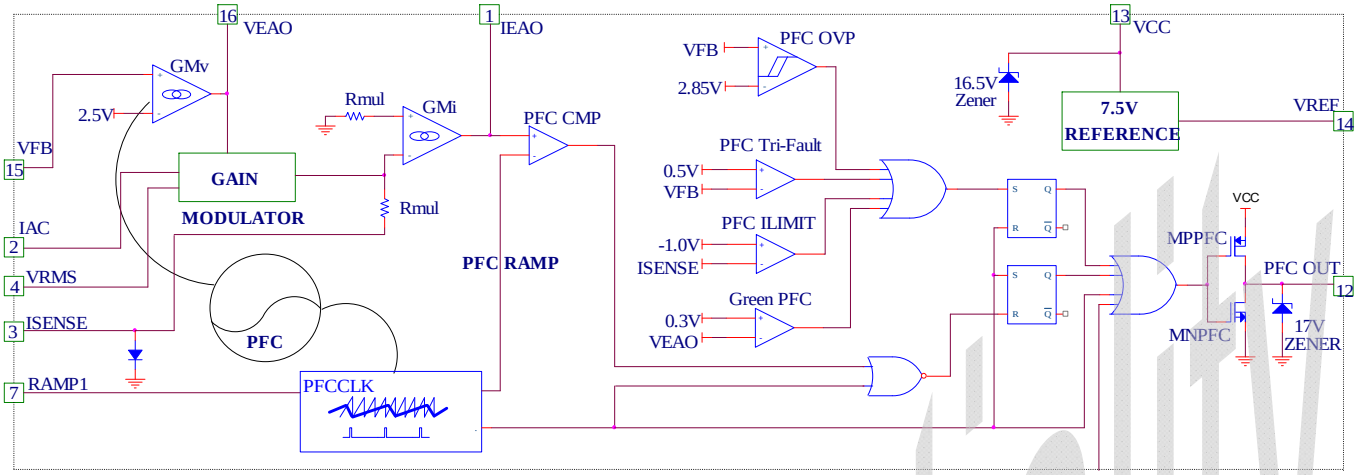


Figure 1. PFC Section Block Diagram

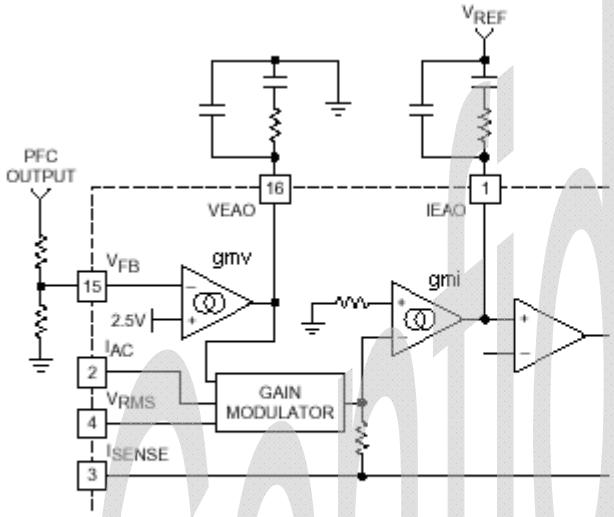


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

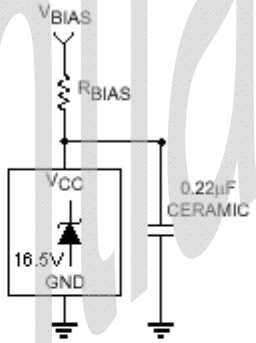


Figure 3. External Component Connections to V_{CC}

Oscillator (RAMP1, or called RTCT)

In CM6802SAH, fRTCT=4xfpwm=4xfpfc fRTCT=272Khz, fpwm=68Khz and fpfc=68Khz or In CM6802SBH, fRTCT=2xfpwm=4xfpfc fRTCT=272Khz, fpwm=136Khz and fpfc=68Khz, it provides the best performance in the PC application.
The oscillator frequency, fRTCT is the similar formula in CM6800:

$$fRTCT = \frac{1}{t_{RAMP} + t_{DEADTIME}}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln \frac{V_{REF} - 1.25}{V_{REF} - 3.75}$$

at VREF = 7.5V:

$$t_{RAMP} = C_T \times R_T \times 0.51$$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5V}{3.64mA} \times C_T = 686.8 \times C_T$$

The dead time is so small ($t_{RAMP} >> t_{DEADTIME}$) that the operating frequency can typically be approximately by:

$$fRTCT = \frac{1}{t_{RAMP}}$$

Ct should be greater than 470pF.

Let us use 1000PF Solving for R_T yields 5.88K. Selecting standard components values, C_T = 1000pF, and R_T = 5.88kΩ

The dead time of the oscillator determined two things:

1.) PFC minimum off time which is the dead time

2.) PWM skipping reference duty cycle: when the PWM duty cycle is less than the dead time, the next cycle will be skipped and it reduces no load consumption in some applications.

PWM Section

Pulse Width Modulator

The PWM section of the CM6802SAH/SBH is straightforward, but there are several points which should be noted. Foremost among these is its inherent synchronization to the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage-mode operation.

In current-mode applications, the PWM ramp (RAMP2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage, and is thereby representative of the current flowing in the converter's output stage. DCI_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP2 in such applications. For voltage-mode, operation or certain specialized applications, RAMP2 can be connected to a separate RC timing network to generate a voltage ramp against which V_{DC} will be compared. Under these conditions, the use of voltage feed-forward from the PFC buss can assist in line regulation accuracy and response. As in current mode operation, the DC I_{LIMIT} input is used for output stage over-current protection.

No voltage error amplifier is included in the PWM stage of the CM6802SAH/SBH, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of opto-coupler feedback circuitry, an offset has been built into the PWM's RAMP2 input which allows V_{DC} to command a zero percent duty cycle for input voltages below around 1.8V.

PWM Current Limit (DCILIMIT)

The DC I_{LIMIT} pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle. Beside, the cycle-by-cycle current, when the DC ILIMIT triggered the cycle-by-cycle current. It will limit PWM duty cycle mode. Therefore, the power dissipation will be reduced during the dead short condition.
When DCILIMIT pin is connected with RAMP2 pin, the CM6802SAH/SBH's PWM section becomes a current mode PWM controller. Sometimes, network between DCILIMIT and RAMP2 is a resistor divider so the DCILIMIT's 1V threshold can be amplified to 1.8V or higher for easy layout purpose.

PWM Brown Out (380V-OK Comparator)

The 380V-OK comparator monitors the DC output of the PFC and inhibits the PWM if this voltage on V_{FB} is less than its nominal 2.36V. Once this voltage reaches 2.36V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins. It is a hysteresis comparator and its lower threshold is 1.35V.

PWM Control (RAMP2)

When the PWM section is used in current mode, RAMP2 is generally used as the sampling point for a voltage representing the current on the primary of the PWM's output transformer, derived either by a current sensing resistor or a current transformer. In voltage mode, it is the input for a ramp voltage generated by a second set of timing components (R_{RAMP2}, C_{RAMP2}),that will have a minimum value of zero volts and should have a peak value of approximately 5V. In voltage mode operation, feed-forward from the PFC output buss is an excellent way to derive the timing ramp for the PWM stage.

Soft Start (SS)

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of 10μA supplies the charging current for the capacitor, and start-up of the PWM begins at SS~1.8V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{10\mu A}{1.8V}$$

where C_{SS} is the required soft start capacitance, and the t_{DEALY} is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C_{SS}:

$$C_{SS} = 5ms \times \frac{10\mu A}{1.8V} \fallingdotseq 27nF$$

Caution should be exercised when using this minimum soft start capacitance value because premature charging of the SS capacitor and activation of the PWM section can result if VFB is in the hysteresis band of the 380V-OK comparator at start-up. The magnitude of V_{FB} at start-up is related both to line voltage and nominal PFC output voltage. Typically, a 0.05μF soft start capacitor will allow time for V_{FB} and PFC out to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

Generating V_{CC}

After turning on CM6802SAH/SBH at 13V, the operating voltage can vary from 10V to 17.9V. That's the two ways to generate VCC. One way is to use auxiliary power supply around 15V, and the other way is to use bootstrap winding to self-bias CM6802SAH/SBH system. The bootstrap winding can be either taped from PFC boost choke or from the transformer of the DC to DC stage. The ratio of winding transformer for the bootstrap should be set between 18V and 15V.

A filter network is recommended between VCC (pin 13) and bootstrap winding. The resistor of the filter can be set as following.

$R_{FILTER} \times I_{VCC} \sim 2V$, $I_{VCC} = I_{OP} + (Q_{PFCFET} + Q_{PWMFET}) \times fsw$

I_{OP} = 3mA (typ.)

EXAMPLE:

With a wanting voltage called, V_{BIAS} ,of 18V, a VCC of 15V and the CM6802SAH/SBH driving a total gate charge of 90nC at 100kHz (e.g. 1 IRF840 MOSFET and 2 IRF820 MOSFET), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA$$

$$R_{BIAS} = \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_G}$$

$$R_{BIAS} = \frac{18V - 15V}{5mA + 9mA}$$

Choose R_{BIAS} = 214Ω

The CM6802SAH/SBH should be locally bypassed with a 1.0μF ceramic capacitor. In most applications, an electrolytic capacitor of between 47μF and 220μF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 4 shows a typical trailing edge control scheme.

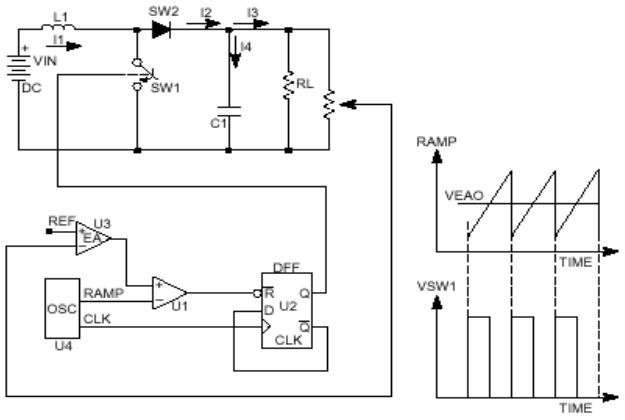


Figure 4. Typical Trailing Edge Control Scheme

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch.

Figure 5 shows a leading edge control scheme.
One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary “no-load” period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC’s output ripple voltage can be reduced by as much as 30% using this method.

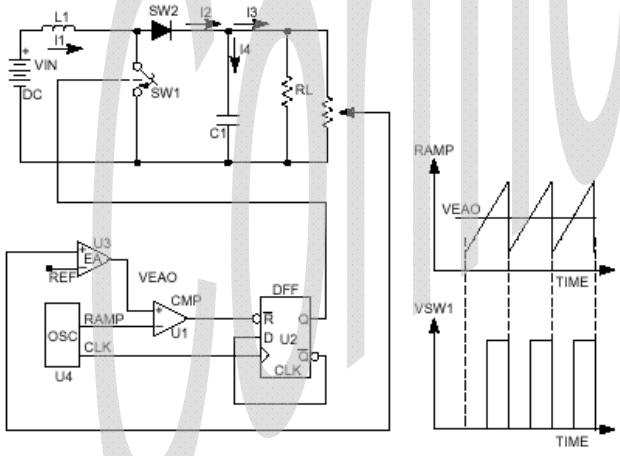
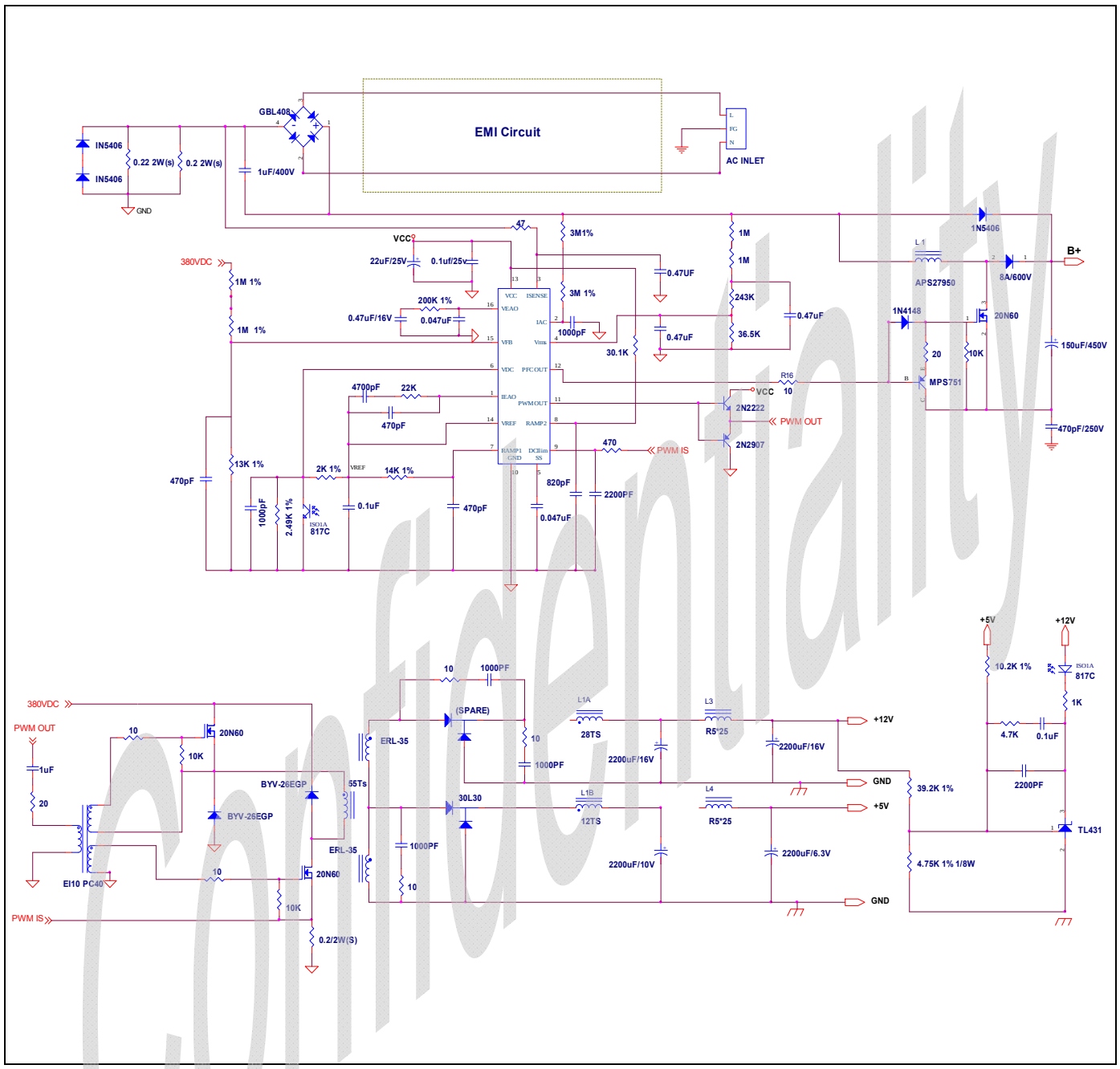
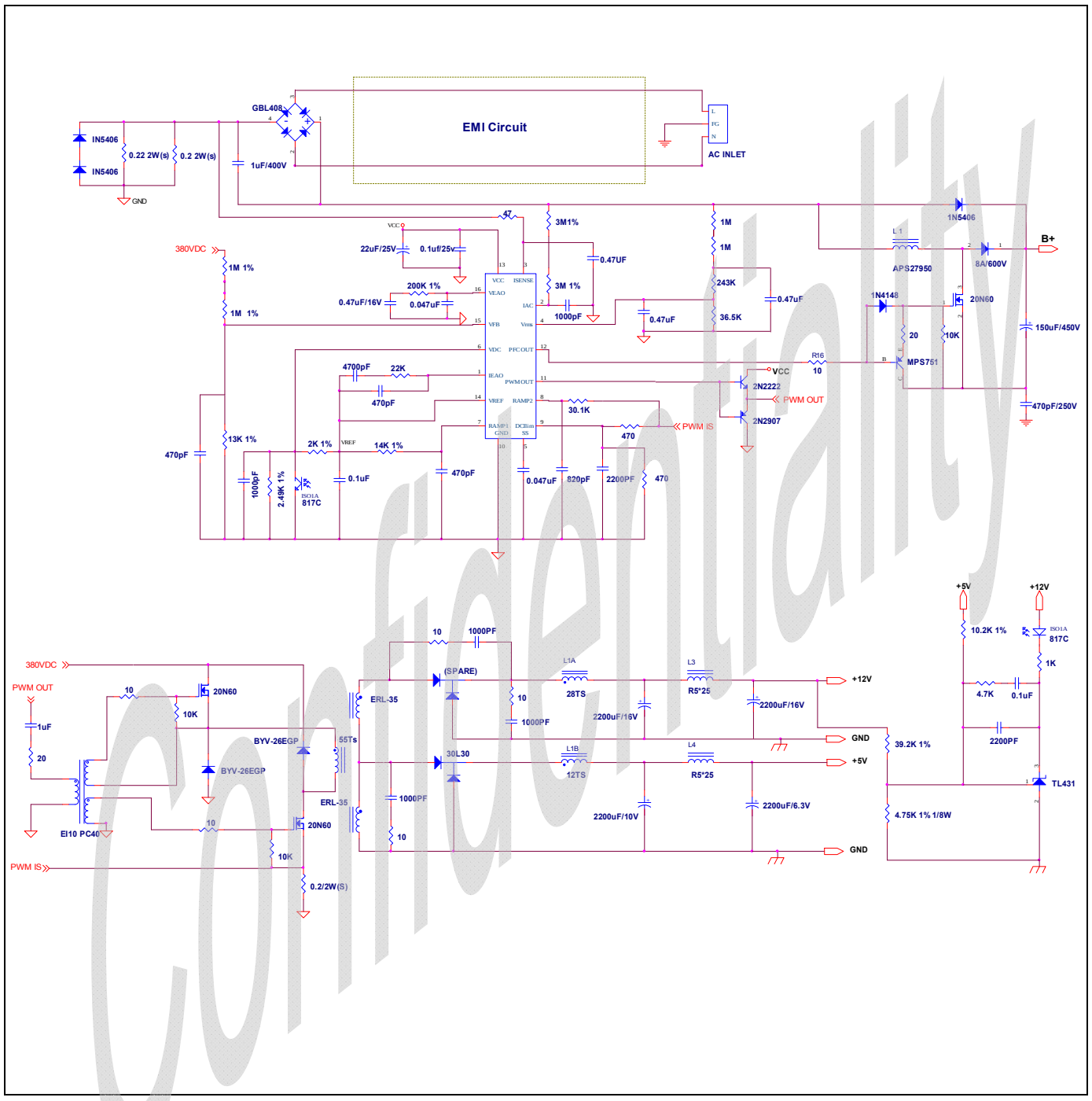


Figure 5. Typical Leading Edge Control Scheme

APPLICATION CIRCUIT (Voltage Mode)

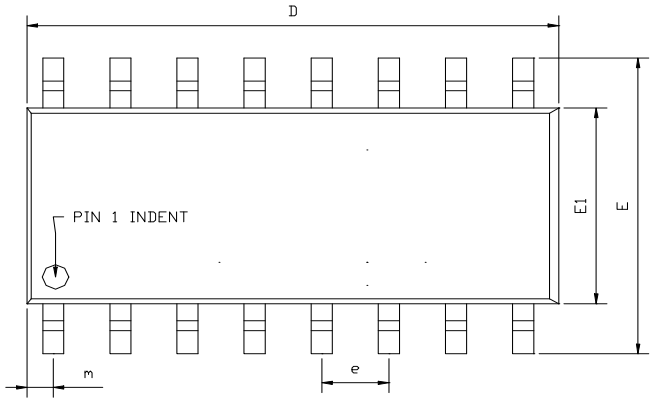


APPLICATION CIRCUIT (Current Mode)



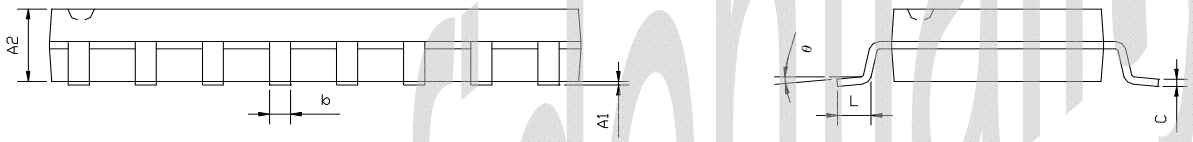
PACKAGE DIMENSION

16-PIN SOP (S16)

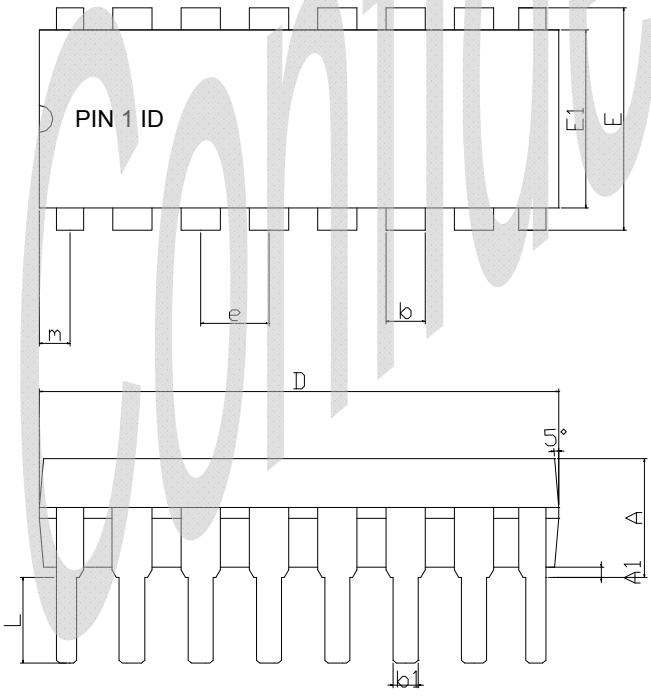


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.05	---	0.15	0.002	---	0.006
A2	1.40	---	1.55	0.055	---	0.061
b	0.30	---	0.51	0.012	---	0.020
C	0.15	---	0.26	0.006	---	0.010
D	9.80	---	10.06	0.386	---	0.396
E	5.79	---	6.20	0.228	---	0.244
E1	3.76	---	4.01	0.148	---	0.158
e	---	1.27	---	---	0.050	---
L	0.38	---	0.69	0.015	---	0.035
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

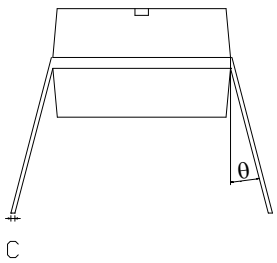
EXPOSED PAD DIMENSION : (mm)
PAD SIZE: X=2.3 ; Y=2.8



16-PIN PDIP (P16)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	4.32	---	---	0.170
A1	0.38	---	---	0.015	---	---
b	1.40	---	1.65	0.055	---	0.065
b1	0.40	---	0.56	0.016	---	0.022
C	0.20	---	0.31	0.008	---	0.012
D	18.79	---	19.31	0.740	---	0.760
E	7.49	---	8.26	0.295	---	0.325
E1	6.09	---	6.61	0.240	---	0.260
e	---	2.54	---	---	0.100	---
L	3.18	---	---	0.125	---	---
m	0.50	---	---	0.02	---	---
θ	0°	---	15°	0°	---	15°



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HsinChu Headquarter

5F, No. 11, Park Avenue II,
Science-Based Industrial Park,
HsinChu City, Taiwan

TEL: +886-3-567 9979
FAX: +886-3-567 9909
http://www.champion-micro.com

Sales & Marketing

21F., No. 96, Sec. 1, Sintai 5th Rd., Sijhih City,
Taipei County 22102,
Taiwan, R.O.C.

TEL: +886-2-2696 3558
FAX: +886-2-2696 3559