0.8V Reference LDO with Source-Sink & Output Selection Functions

Features

- **LDO with Source and Sink Capabilities**
- **Single Input Voltage**
- **Input Voltage Range from 2.5V to 5.0V**
- **Use One Pin to Select Fixed Output Voltage**
- **Use One Pin to Choose Output Voltage by External Resistors**
- **Output Voltage Accuracy : ±2%**
- **Current-Limit Protection**
- **Thermal Shutdown Protection**
- **Fast Transient Response**
- **Stability with Low-ESR Capacitors**
- **TO-252-5, SOP-8, and SOP-8P Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Desktop Computers**
- **Springdale MCH Power**
- **0.8V~1.2V Linear Regulator**

General Description

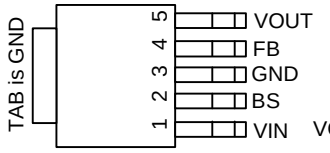
The APL5332 is a precise CMOS LDO with source sink and output selection functions. The APL5332 offers 2% output accuracy. The APL5332 integrates with two power mosfets to source and sink current as well as current and thermal limit into a single chip.

The output voltage can be 1.225V or 1.45V by BS pin selection, and also can be adjusted by an external resistor divider connected to FB pin.

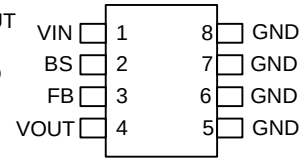
The APL5332 also works with low-ESR output capacitors, reducing the amount of board space necessary for power applications.

The APL5332 key features include current-limit, thermal shutdown, and fast transient response. A compact package TO-252-5 for power consumption purpose, and SOP-8 and SOP-8P for space saving purpose.

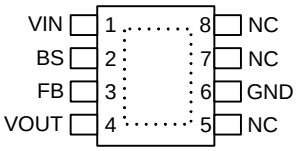
Pin Configuration



TO-252-5 (Top View)



SOP-8 (Top View)



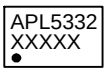
SOP-8P (Top View)

NC = No internal connection

= Thermal Pad (connected to GND plane for better heat dissipation)

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL5332 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code U5 : TO-252-5 K : SOP-8 KA : SOP-8P Temperature Range C : 0 to 70 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL5332 K/KA : 	XXXXX - Date Code
APL5332 U5 : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Supply Voltage, VIN to GND	-0.2 ~ 5.5	V
	BS, FB to GND	-0.2 ~ V_{IN}	V
V_{OUT}	VOUT Output Voltage, VOUT to GND	-0.2 ~ V_{IN}	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air (Note 2) TO-252-5 SOP-8P SOP-8	 80 80 150	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	2.4 ~ 3.5	V
I_{OUT}	VOUT Output Current (Note 3,4)	-1 ~ +2	A
T_J	Junction Temperature	0 ~ 125	°C

Note 3 : The symbol "+" means the VOUT sources current to load; the symbol "-" means the VOUT sinks current to GND.
Note 4 : The max. IOUT varies with the T_J. Please refer to the typical characteristics.

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Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{IN}=2.5~3.3V, and T_J= 0 to 125°C, unless otherwise specified. Typical values refer to T_J =25°C.

Symbol	Parameter	Test Conditions		APL5332			Unit
				Min.	Typ.	Max.	
OUTPUT VOLTAGE							
V_{REF}	Reference Voltage	FB=VOUT		-	0.8	-	V
V_{OUT}	VOUT Output Voltage	BS=VIN, FB=VIN		-	1.225	-	V
		BS=GND, FB=VIN		-	1.45	-	
	Accuracy	I_{OUT}=0A, T_J=25°C		-1	-	+1	%
		I_{OUT}= -1~+2A, T_J=0~125°C		-2	-	+2	
	Load Regulation	I_{OUT}=0A~+2A V_{IN}=2.5V V_{IN}=3.3V		- -	0.5 1	-	%
		I_{OUT}= 0~-1A, V_{IN}=2.5V or 3.3V		-	0.7	-	
	Line Regulation	I_{OUT}=0A, V_{IN}=2.5V ~ 3.3V		-	0.05	0.2	%
PROTECTION							
I_{LIM}	Current Limit	Sourcing Current (V_{IN}=3.3V)	T_J=25°C	2.0	2.3	-	A
			T_J=125°C	-	1.7	-	
		Sinking Current (V_{IN}=2.5V or 3.3V)	T_J=25°C	1.2	1.7	-	
			T_J=125°C	-	1.3	-	
		Sourcing Current (V_{IN}=2.5V)	T_J=25°C	1.7	2.0	-	A
			T_J=125°C	-	1.5	-	
T_{SD}	Thermal Shutdown Temperature	Rising T_J		-	150	-	°C
	Thermal Shutdown Hysteresis			-	25	-	°C
BS AND FB THRESHOLD VOLTAGES							
	BS Logic High Threshold Voltage	V_{BS} Rising		0.6	0.8	1.0	V
	BS Hysteresis			-	35		mV
	BS Input Bias Current	V_{IN}=3.3V, BS=GND		-	-0.17	-0.3	µA
	FB Logic High Threshold Voltage (V_{FB}- V_{IN})	V_{FB} Rising		-0.3	-0.46	-0.8	V
	FB Hysteresis			-	35	-	mV
	FB Input Bias Current	V_{IN}=3.3V, FB=0.8V		-	-0.17	-0.3	µA
OTHER							
I_Q	Quiescent VIN Supply Current	I_{OUT}=0A		4	8	14	mA
V_{POR}	VIN Power-On-Reset Threshold Voltage			1.4	2.1	2.4	V
T_{SS}	Soft-Start Interval			-	1	-	mS

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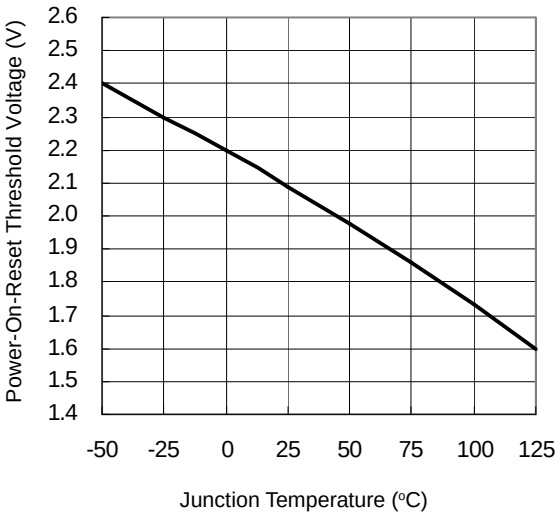
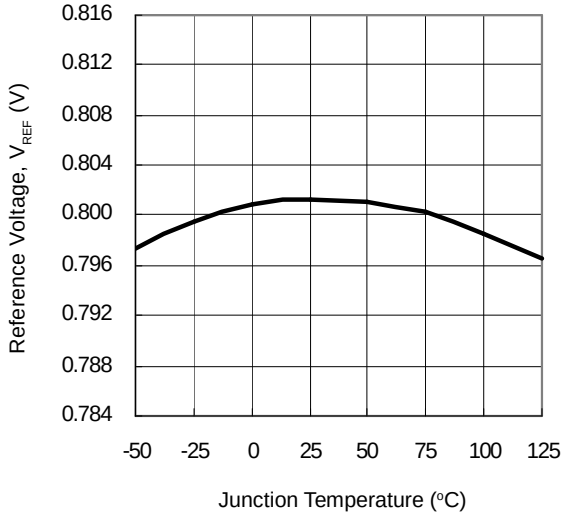
Typical Operating Characteristics

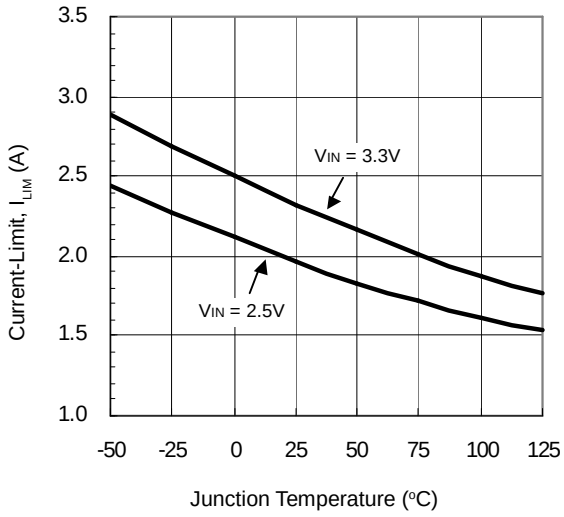
Power-On-Reset Threshold Voltage vs. Junction Temperature



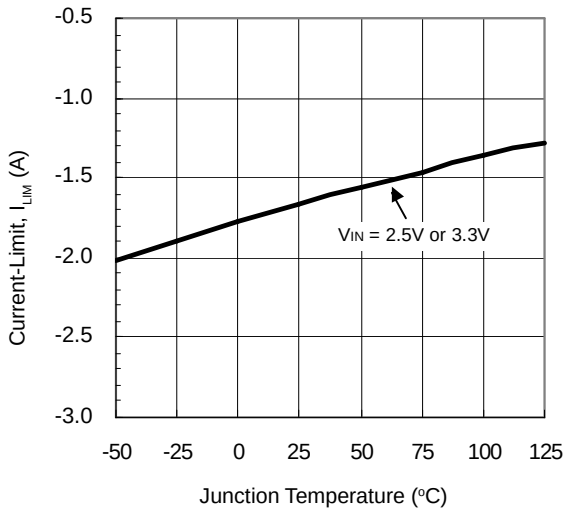
VREF Shutdown Threshold vs. Junction Temperature



Sourcing Current-Limit vs. Junction Temperature

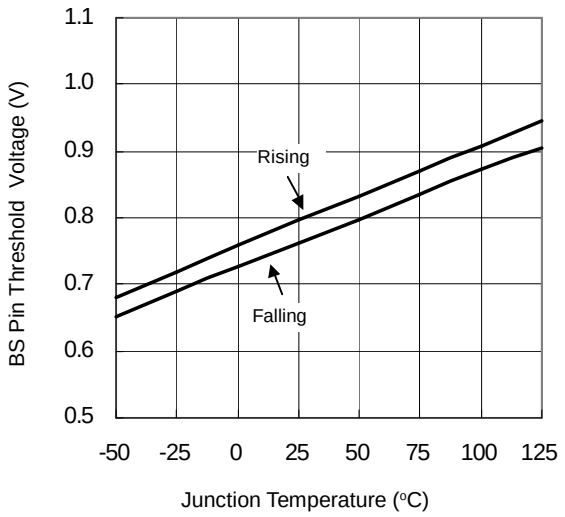


Sinking Current-Limit vs. Junction Temperature

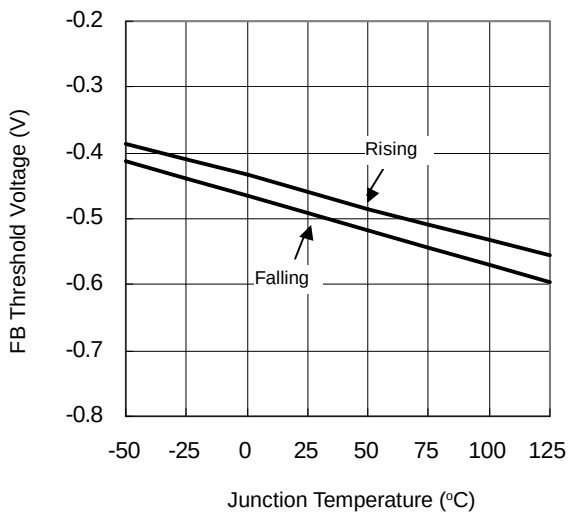


Typical Operating Characteristics (Cont.)

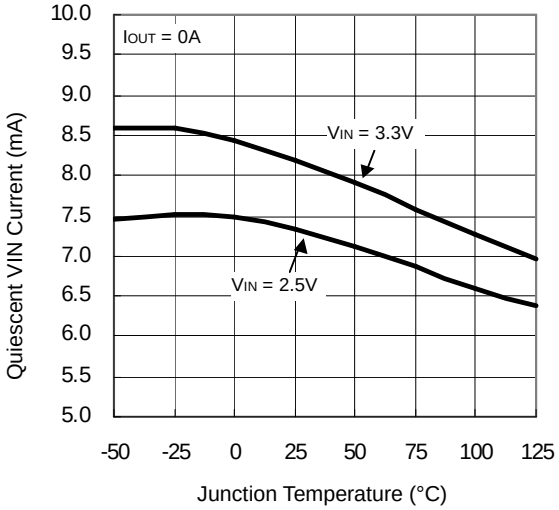
BS Pin Threshold Voltage vs. Junction Temperature



FB Threshold Voltage vs. Junction Temperature



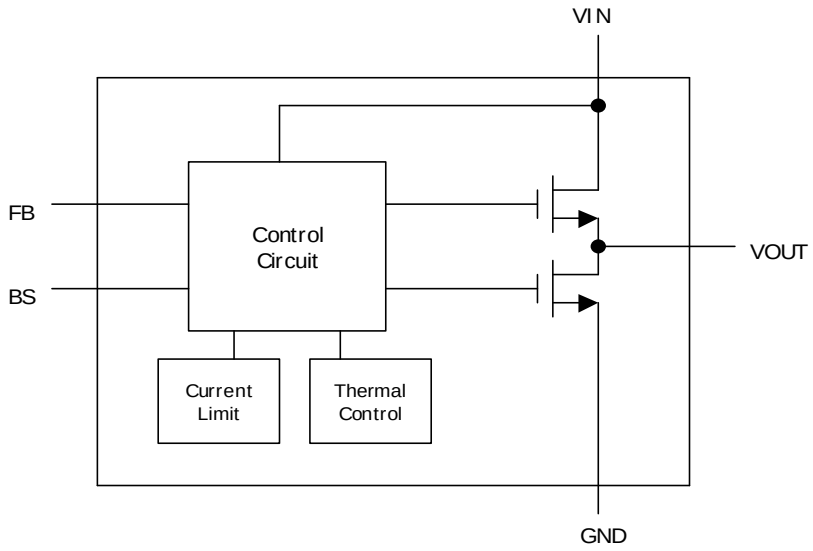
Quiescent VIN Current vs. Junction Temperature



Pin Description

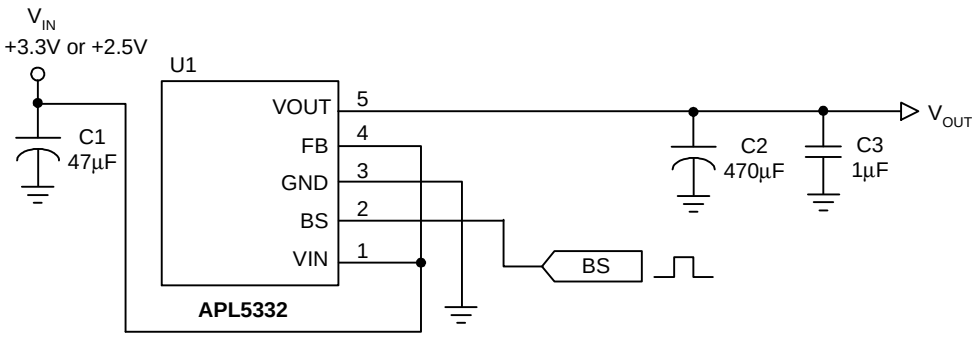
PIN		I/O	FUNCTION
NO.	NAME		
1	VIN	I	Input supply voltage.
2	BS	I	Fixed output voltage selection by this pin.
3	GND	O	Ground pin for signal ground and power ground.
4	FB	I	Adjust output voltage by this pin
5	VOUT	O	Regulator output voltage.

Block Diagram



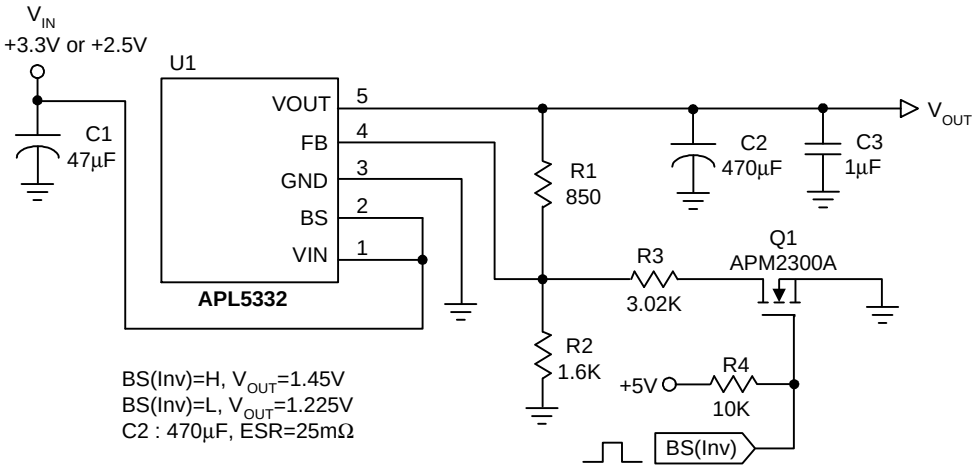
Typical Application Circuit

(1) For Processor MCH Power Selection Schematic
(Fixed Voltage Mode Operation selected by BS Pin)



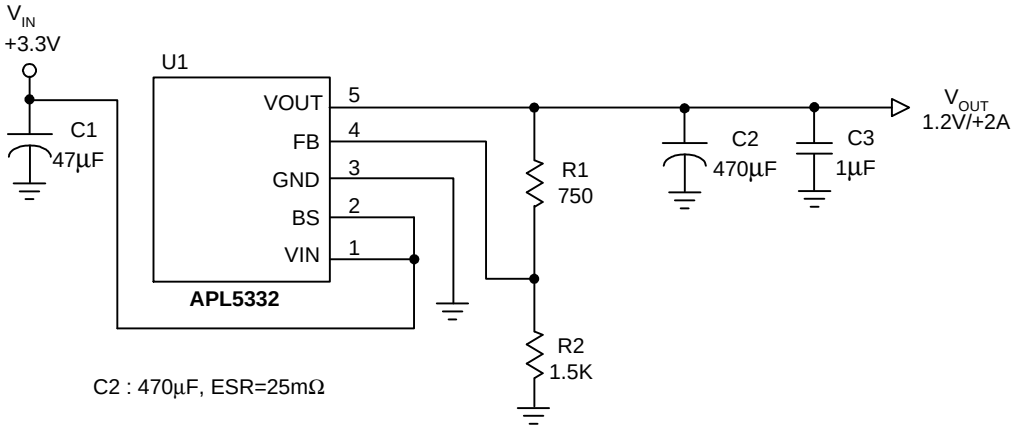
BS=H, V_{OUT}=1.225V
BS=L, V_{OUT}=1.45V
C2 : 470µF, ESR=25mΩ

(2) Use External Resistors to Select the Desired Output Voltage Schematic
(Adjustable Voltage Mode Operation)



BS(Inv)=H, V_{OUT}=1.45V
BS(Inv)=L, V_{OUT}=1.225V
C2 : 470µF, ESR=25mΩ

(3) 1.2V Output LDO
(Adjustable Voltage Mode Operation set by External Resistor Divider)



C2 : 470µF, ESR=25mΩ

Function Description

General

APL5332 is a source-sink linear regulator designed for motherboard front side bus. The device can supply loads from -1A to 2A in either fixed or adjustable voltage mode. APL5332 has a 0.8V reference, an error amplifier, two pass transistors, fixed voltage selection, an internal feedback resistor-divider, soft-start control, and fault protections (current-limit and thermal shutdown). The output voltage is either 1.225V or 1.45V selected by the BS pin when fixed voltage mode is active by setting FB=VIN. When the FB is connected with a feedback resistor-divider, the IC operates in adjustable voltage mode and the voltage of FB is regulated to 0.8V. In the mode, the input of BS pin is ignored. APL5332 is available in the SOP-8, SOP-8P, and TO-252-5 packages to meet different power dissipation applications.

Output Voltage Regulation

The error amplifier working with the temperature-compensated 0.8V reference and the two pass transistors (high-side and low-side) regulates the output to the preset voltage. The error amplifier compares the reference with the feedback voltage and amplifies the difference to drive one of the pass transistors. The high-side pass transistor provides current from VIN to VOUT and increases the output voltage when the feedback voltage is lower than the reference. The low-side pass transistor provides current from VOUT to GND and decreases the output voltage when the feedback voltage is higher than the reference. The two pass transistors are well controlled by the error amplifier and prevented short-through conditions. An internal output voltage sense pad is bonded to the VOUT pin for perfect load regulation in fixed voltage mode.

Current Limit

The APL5332 monitors the sourcing or sinking currents and limits the maximum output current to prevent damages during overload or short-circuit conditions.

Power-On-Reset and Soft-Start

A Power-On-Reset circuit monitors input voltage of the VIN pin and prevents wrong logic controls. When the input voltage rises up more than the Power-On-Reset threshold voltage, the device starts to output current. Therefore, a soft-start circuit which controls the reference voltage to rise up is required, limiting surge input currents. The typical soft-start interval is about 1mS.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APL5332. When the junction temperature exceeds +150°C, a thermal sensor turns off the both pass transistors, allowing the device to cool down. The regulator starts to regulate again after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 25°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of APL5332.
For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

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Application Information

Internal Parasitic Diode

Do not apply a voltage to VOUT when the voltage applied at VIN is not present. The reason is that the internal parasitic diodes from VOUT to VIN will conduct due to the forward-voltage applied at VOUT.

Output Voltage Selection

The APL5332 allows operation in either fixed voltage or adjustable mode. Connecting FB to VIN selects fixed output voltage which is either 1.225V or 1.45V by setting the BS pin to be logic "High" or "Low". The output voltage may also be adjusted by connecting a resistor-divider from VOUT to FB to GND (See the Typical Application Circuit). Selecting R2 in the 100Ω to 5kΩ range ignors the voltage offset caused by the internal pull-up current of FB. Calculate R1 with the following equation:

$R1 = R2\ [(V_{OUT} / V_{REF}) - 1]$

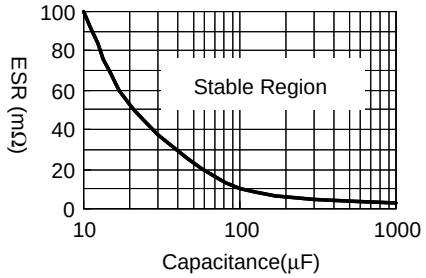
where V_{REF} = 0.8V.

The output voltage selection table is :

		BS	
		H	L
FB	H	1.225V	1.45V
	L	Adjustable	Adjustable

Output Capacitor

The APL5332 requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon the ESR (equivalent series resistance) and capacitance over temperature and current ranges. The following chart shows a stable region to select output capacitor for APL5332. This region above the curve indicates minimum required ESR and capacitance to maintain stability. However, the output capacitor should have an ESR less than1Ω.



Ultra-low-ESR capacitors, such as ceramic chip capacitors, may promote unstable or under-damped transient response, but proper ceramic chip capacitors placed near loads can be used as decoupling capacitors. A low-ESR solid tantalum and aluminum electrolytic capacitor (ESR <1Ω) works extremely well and provides good transient response and stability over temperature.

The output capacitors are also used to reduce the slew rate of load current and help the APL5332 to minimize variations of the output voltage, improving transient response. For this purpose, the low-ESR capacitors are recommended.

Input Capacitor

The VIN input capacitor is not required for stability but for supplying surge currents during large load transients, preventing the input rail from dropping, and improving performance of APL5332. The parasitic inductors from the voltage sources or other bulk capacitors to the VIN pins will limit the slew rate of the surge currents during large load transients, resulting in voltage drop at VIN pin. An aluminum electrolytic capacitor (>47μF) is recommended for VIN pin, and It is not necessary to use low-ESR capacitors.

Layout and Thermal Consideration

The input capacitors are normally placed near VIN for good performances. Ceramic decoupling capacitors for load must be placed as close to the load to reduce the parasitic inductors of traces. It is also recommended that the APL5332 and output capacitors are placed near the load for good load regulation and transient response. The negative pins of the input and output capacitors and the GND pin of the APL5332 are connected to analog the ground plane of the load.

See Figure 1. The SOP-8P is a cost-effective package featuring a small size as a standard SOP-8 and a bottom thermal pad to minimize the thermal resistance of the package, being applicable to high current applications. The thermal pad of SOP-8P or TO-252-5 is soldered to the top ground pad which is connected to the internal or bottom ground plane by several vias. The printed circuit board (PCB) forms a heat sink and dissipates major heat into ambient air.

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Application Information (Cont.)

Layout and Thermal Consideration (Cont.)

Thermal resistance consists of two main elements, θ_{JC} (junction-to-case thermal resistance) and θ_{CA} (case-to-ambient thermal resistance). θ_{JC} is specified from the IC junction to the bottom of the thermal pad directly below the die. θ_{CA} is the resistance from the bottom of thermal pad to the ambient air and it includes θ_{CS} (case-to-sink thermal resistance) and (sink-to-ambient thermal resistance). The specified path for heat flow is the lowest resistance path and it dissipates major heat to the ambient air. Normally θ_{CA} is a major resistance in the path. Enlarging the internal or the bottom ground plane reduces the resistance θ_{CA}. The relationship between power dissipation and temperature is the following equation:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where,

P_D : power dissipation

T_J : Junction Temperature

T_A : Ambient Temperature

θ_{JA} : Junction-to-Ambient Thermal Resistance

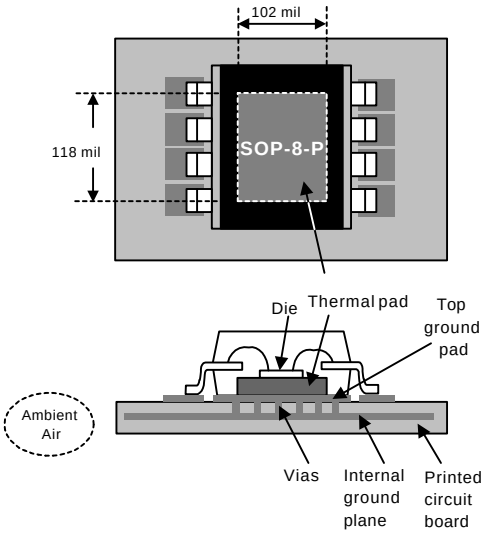


Figure 1

Figure 2 shows a recommended board layout using the SOP-8P package. An area of 140milx110mil on the top layer (250milx250mil) is used as a thermal pad for APL5332 and is connected to the internal or the bottom ground plane by vias. The vias should have proper hole size to retain solder and help heat conduction. More area of the internal or the bottom plane reduces θ_{JA} and is better for dissipating power. The recommended area is without limit. Therefore, the PCB and all components form a heat sink.

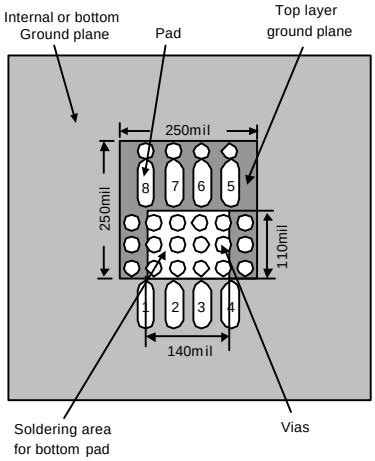


Figure 2

Figure 3 shows a board layout using the SOP-8P package. The demoboard is made of FR-4 material and is a two-layer PCB. The board size and thickness are 65mmx65mm and 1.6mm. The copper thickness of top and bottom layers is 2 oz. The partial layout around APL5332 is as the details above and shown in the figure 2. It uses 15mil vias to connect the top and bottom ground plane. The θ_{JA} of the APL5332 (SOP-8P) mounted on the demodoard is about 41.3°C/W in free air. Assuming the T_A=25°C and the maximum T_J=150°C (typical thermal limit temperature), the maximum power dissipation is calculated as below:

$$P_{D(max)} = (150 - 25) / 41.3 = 3.03W$$

If the T_J is designed below 125°C, the calculated power dissipation should be less than:

$$P_D = (125 - 25) / 41.3 = 2.42W$$

Application Information (Cont.)

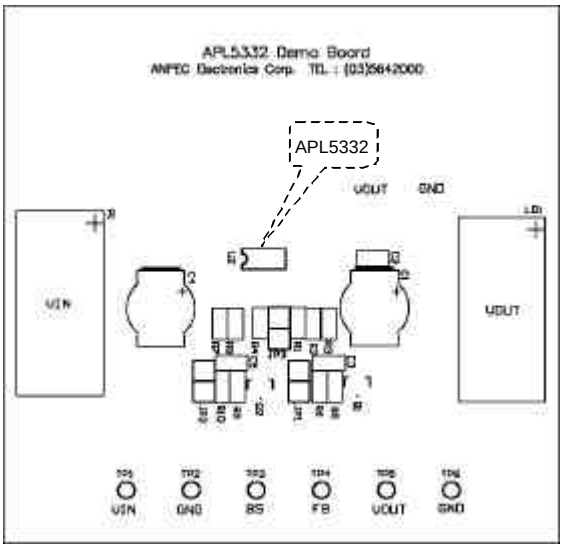


Figure 3(a) TopOver Layer

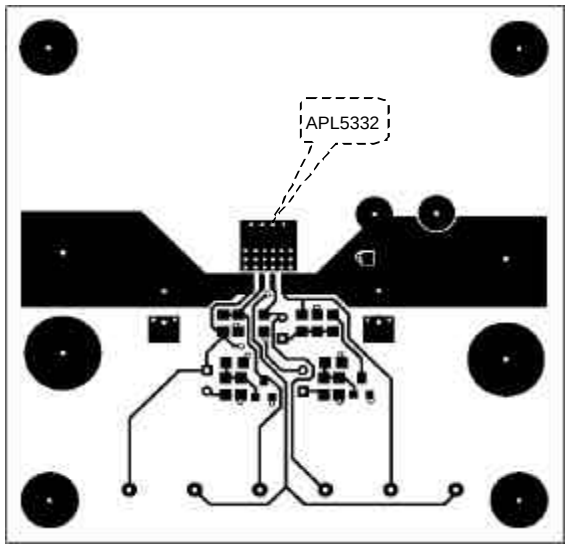


Figure 3(b) Top Layer

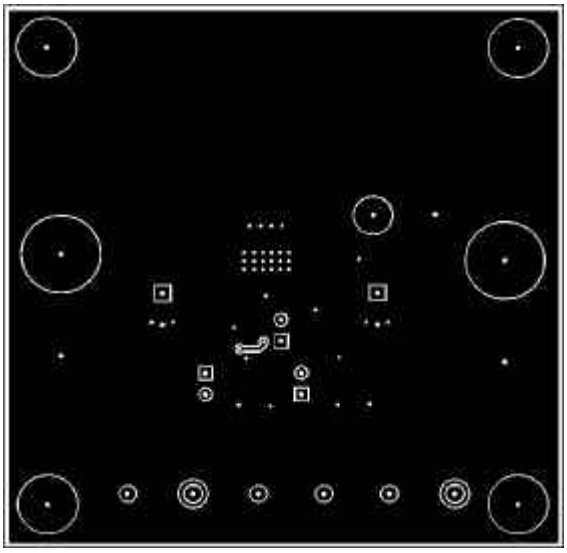
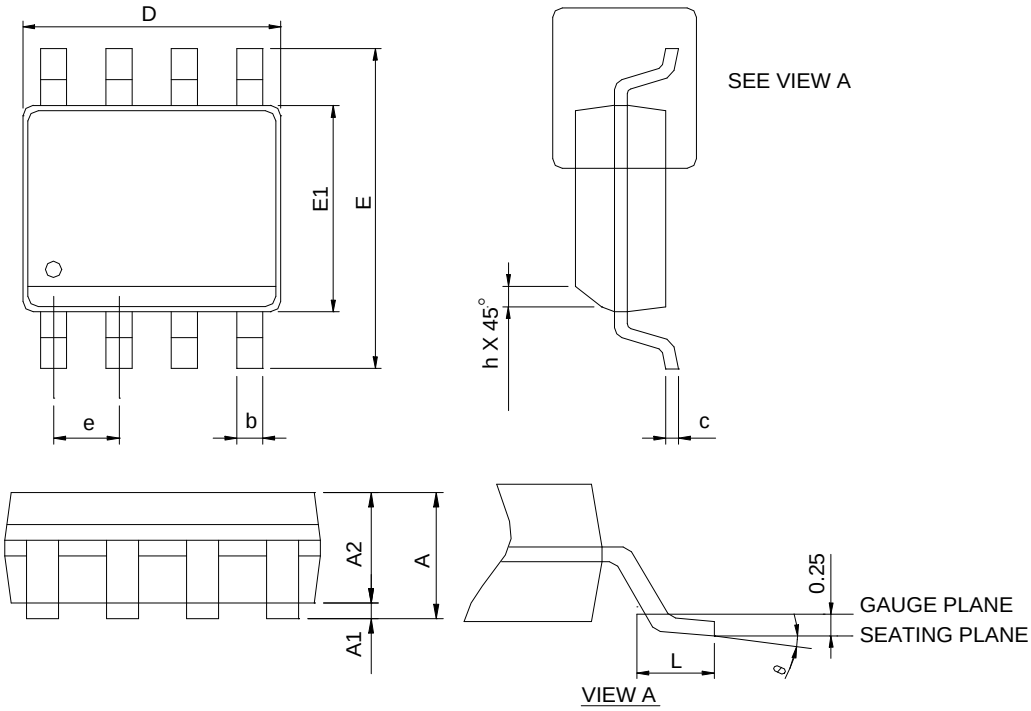


Figure 3(c) Bottom Layer

Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

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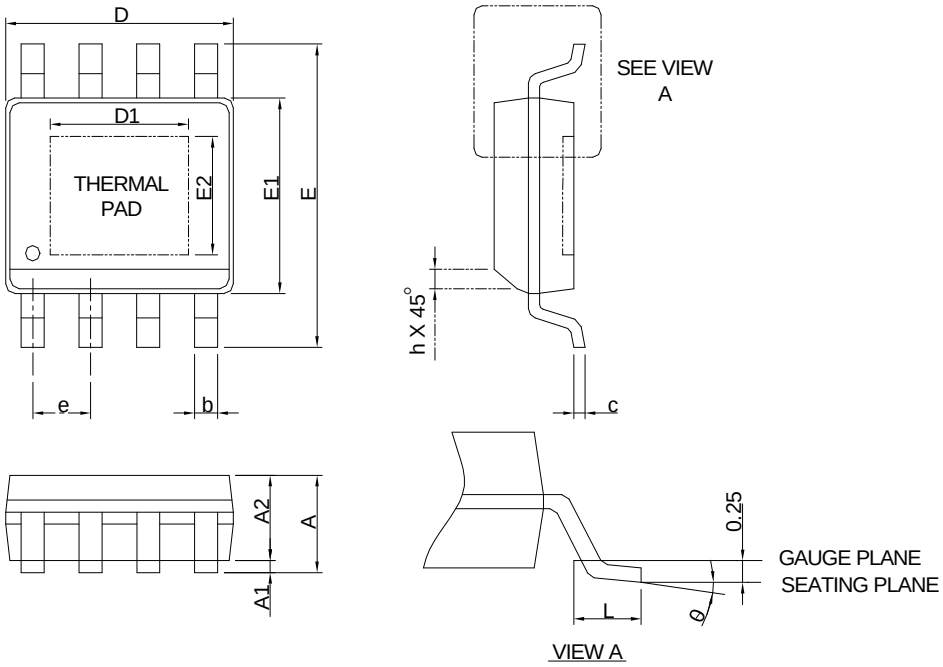
Package Information

SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.25	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC MS-012 BA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

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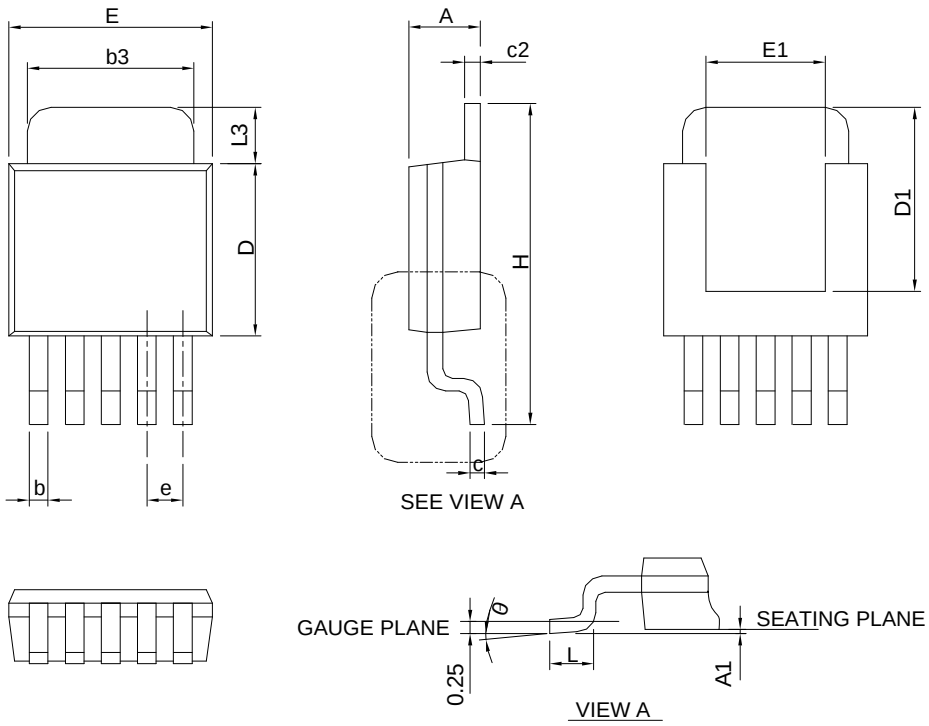
Package Information

TO-252-5



SYMBOL	TO-252-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1		0.13		0.005
b	0.50	0.89	0.020	0.035
b3	4.32	5.46	0.170	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	1.27 BSC		0.050 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L3	0.89	2.03	0.035	0.080
θ	0°	8°	0°	8°

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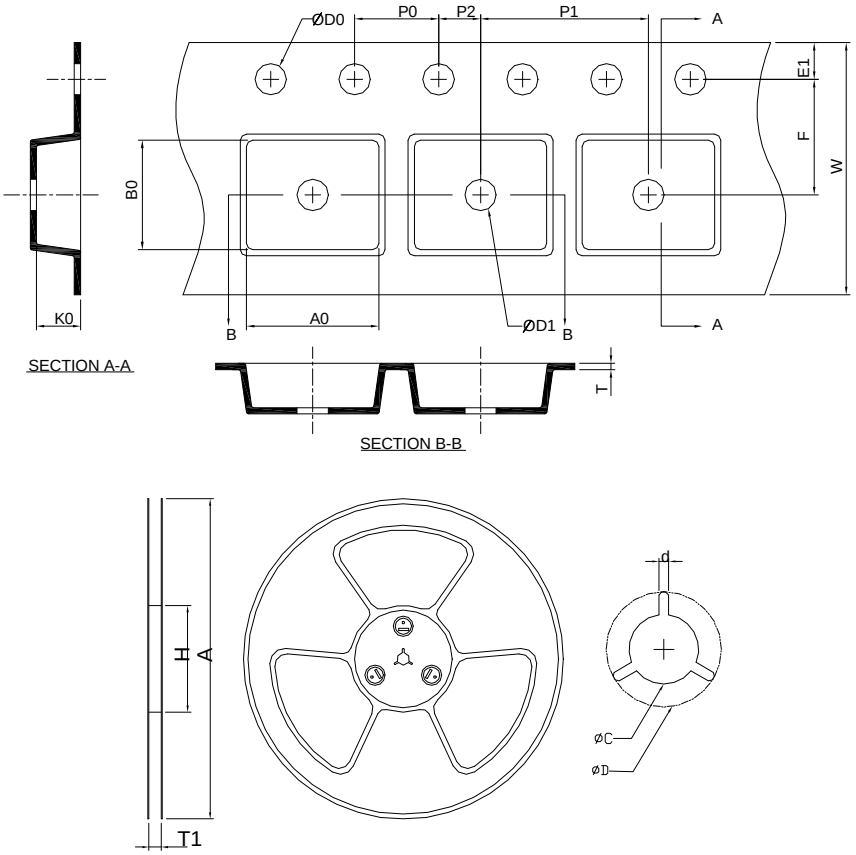
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8(P)	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TO-252-5	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.80±0.20	10.40±0.20	2.50±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-8(P)	Tape & Reel	2500
TO-252-5	Tape & Reel	2500

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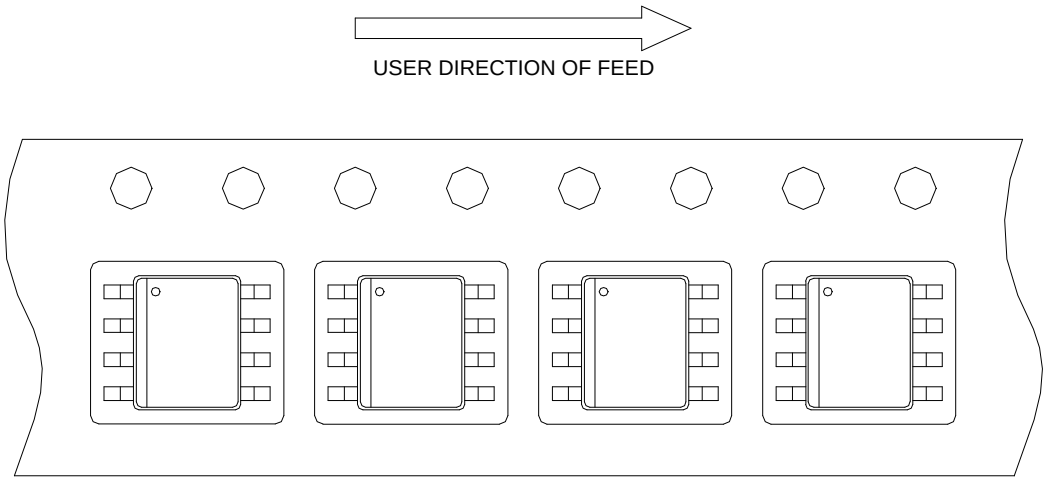
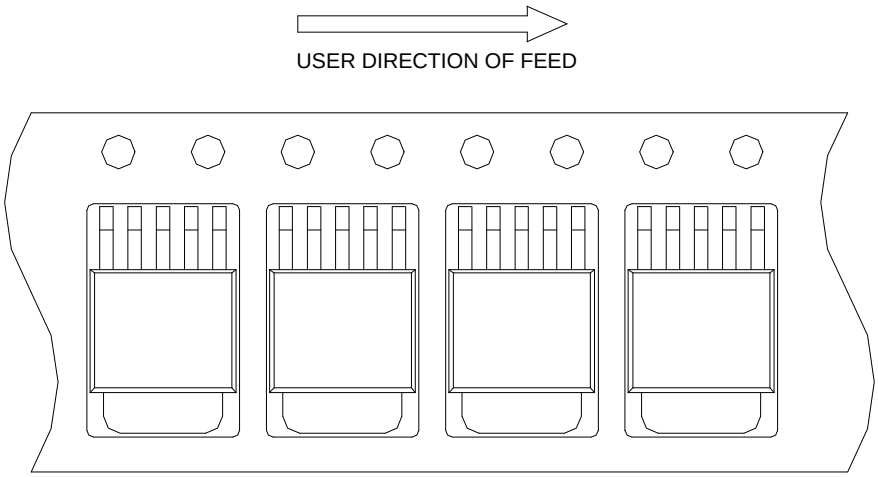
Taping Direction Information

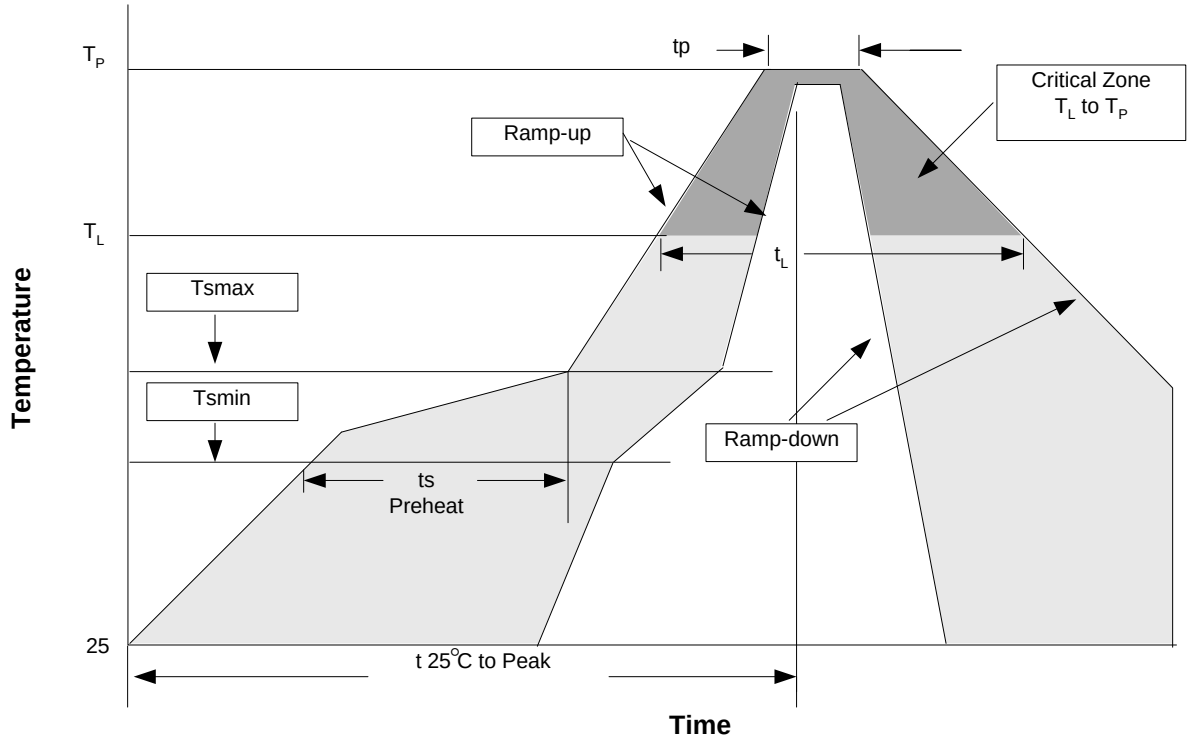
SOP-8(P)



TO-252-5



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

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Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

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