Attansic Technology Corp.

GENERAL DESCRIPTION

ASUS ASIC

FEATURE

1. Support LPC interface I/O read/write cycle only (LPCCLKmax=50MHz), without IRQ & DMA
2. Support Smbus interface
3. PC hardware monitor : 11 Voltage inputs, 4 Thermal inputs, 4 FAN inputs & 2 FAN outputs voltage input – 5VMB, 3VMB, 2.5V, 1.5V, Vcore0, 12V, 5VSB, 3VSB, VBATDET, VBAT Thermal input – TXD1(LM78), TXD2(LM75), TXD3(LM75),TXD4(LM78)

   Fan input – FANIN1, FANIN2, FANIN3,FANIN4 with digital filter

   Fan output – DCFANOUT(DAC o/p), PWMFANOUT
4. Two SMBus path control mode

   a.) MUX 1 -> 4 mode

   b.) SMBus Hub mode
5. AOL2 interrupt output : inform Voltage & Fan error
6. 1 sets 3.6V reference voltage output(5V power) and 2 set 1V reference voltage outputs(5V & 5VSB power).
11. support 3VSB power output (10mA driving current)
12. 2 trapping pins to GPIO latch for IDE 80-pin cable
13. LPC / GPIO multi-function trapping pin
14. 3 trapping pins for PCB version
15. 3 Clock buffers with independent power source
16. ASUS Glue Logic
17. 8 bytes general registers powered by VBAT.
18. 1-to-3 clock buffers powered by VDDCKBF.

Revision Histroy

2000/11/25	1. Modify target temperature tolerance for TXD2, TXD3 & TXD4. 2. Modify Bank0 CR4D & remove Bank3 CR1A. 3. Add default value for VBAT back-up registers.
2000/11/27	Add VRM 8.5/9.0 Table. VID voltage check for Hardware Monitor is +/-20%, and for VIDLIMIT control is +20% and –10%.
2001/5/15	Add 10Kohm pull-down resistor to PCB1 & PCB2(pin 8 & 9).
2001/9/3 Revision 0.8	1. Modify RING_IN (pin 66) pull-down resistor from 100Kohm to 20Kohm. 2. Add BIOSW#/VIDLIMIT# (pin 99) pull-down 10Kohm resistor. 3. Move Bank 7 CR98 bit 1~0 to Bank 7 CR 81 Bit 7~6, and remove register Bank 7 CR 98. 4. Modify LPC I/F access address can be programable to 4E/4F or 5E/5F, and inhibit data being read out when ASIC is outside access window. The control bit is Bank 7 CR81 bit 5. 5. Remove PCB0 power-on starpping function. 6. Swap 3VSB_GATE & 3VSB_GATE# pin.
2001/9/10 Revision 0.81	1. Remove GPIO 7 & 8 input mode, and change pin name.
2001/9/28 Revision 0.82	1. Modify Bank0 CR46 definition.
2002/1/17 Revision 0.85	1.Reveal Reserved bit definition for Bank 3 CR18 PWMFAN frequency select. 2.Change Bank 0 CR 49 Chip revision for ASB100-A. 3. Enable TXD4 over-temperature shut-down function Bank 7 CR 93 & CR97.
2002/1/18 Revision 0.87	1. Exchange DCFAN & PWMFAN for TXD1~4 2. PWMFAN related to TXD1 only under Temperature Mode. 3. DCFAN related to TXD2, TXD3 and TXD4 under Temperature Mode. 4. Redefine Bank 0 CR59, BANK 3 CR13 & CR19.
2002/2/7 Revision 0.88	1. Exchange Bank 3 CR28 & CR29 Definition.
2002/2/18 Revision 0.89	1. Over-temperature shut-down function, if TXD4 is not used, please connect it "GND"!!!

Warning: If TXD4 is not used, please tie it up to "GND" or system won't power-up.

1. Pin description & I/O spec.

Note:**I/O type list ---**

INt : TTL level input

INtx : Special TTL level input , @VDD=2.6V, VIT+=2.0V / VIT- =0.8V

INtx1 : Special TTL level input , V_{IH}=0.8V(min) & V_{IL}=0.6V(max)

INts : TTL level input with schmitt-trigger

INts-10k-5v-up : TTL level input with schmitt-trigger, 10Kohm 5V pull up

INts-100k-3vsb-up : TTL level input with schmitt-trigger, 100Kohm 3VSB pull up

INts-10M-vbat_up : TTL level input with 10Mohm VBAT pull-up

INts-1.2k-down : TTL level input with 1.2Kohm pull-down

INcs : CMOS level input

OD4 : Open-Drain with 4mA sink current

OD4-10k-3vsb-up : Open-Drain with 4mA sink current and 10k ohm 3VSB pull-up

OD16 : Open-Drain with 16mA sink current

OD16-1k-3v-up : Open-Drain with 1Kohm 3V pull-up, 16mA sink current

OD16-5.6k-5vsb-up : Open-Drain with 5.6Kohm 5VSB pull-up, 16mA sink current

OD48 : Open-Drain with 48mA sink current

OUT4 : Output buffer with 4mA drive/sink current

OUT16 : Output buffer with 16mA drive/sink current

IO8t : TTL level bi-directional pin,and output with 8mA drive/sink current

IO16t : TTL level bi-directional pin and output with 16mA drive/sink current

IO4ts : TTL level bi-directional pin with schmitt-trigger,and output with 4mA drive/sink current

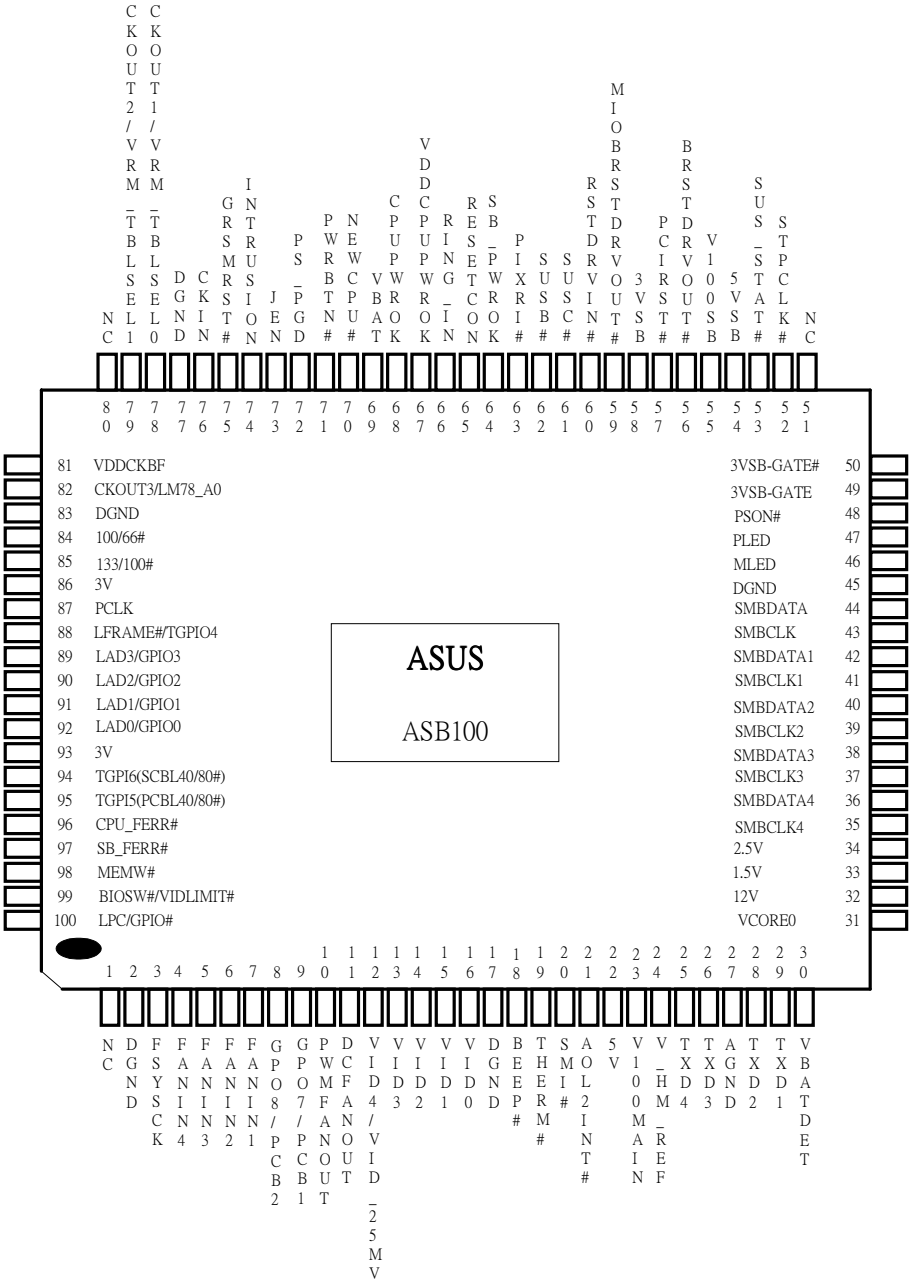
IO16ts : TTL level bi-directional pin with schmitt-trigger,and output with 16mA drive/sink current

IOD4ts : TTL level bi-directional pin with schmitt-trigger,and Open- Drain output with 4mA sink current

1. PIN ASSIGNMENT OF ASB100

Package

- **100-pin PQFP**



1.1.1 AS2000F PIN DESCRIPTION

PIN	SYMBOL	I/O & POWER	FUNCTION
1	NC		
2	DGND		
3	FSYSCK	INt ; 5V	This clock is used by chip, can support 14.318MHz, 24MHz and 48MHz. default 24MHz.
4	FANIN4	INts_10k_5v_up; 5V	The fan speed inport pin 4, internal filter with 100us.
5	FANIN3	INts_10k_5v_up; 5V	The fan speed inport pin 3, internal filter with 100us.
6	FANIN2	INts_10k_5v_up; 5V	The fan speed inport pin 2, internal filter with 100us.
7	FANIN1	INts_10k_5v_up; 5V	The fan speed inport pin 1, internal filter with 100us.
8	***GPO8/PCB2***	***IO8t_10k_down ; 5V***	***GPO8 pin*** ***PCB2 power-on trapping pin input.*** ***Internal 10Kohm pull-down resistor.***
9	***GPO7/PCB1***	***IO8t_10k_down ; 5V***	***GPO7 pin*** ***PCB1 power-on trapping pin input.*** ***Internal 10Kohm pull-down resistor.***
10	***PWMFANOUT***	***IO8t ; 5V***	***PWM Fan control output***
11	DCFANOUT	DAC output	Extrenal connected to HI-Z OPA input pin
12	VID4/VID_25MV	IO16ts ; 5V	I/O: 5V , internal function : 5VSB
13	VID3	IO16ts ; 5V	I/O: 5V , internal function : 5VSB
14	VID2	IO16ts ; 5V	I/O: 5V , internal function : 5VSB
15	VID1	IO16ts ; 5V	I/O: 5V , internal function : 5VSB
16	VID0	IO16ts ; 5V	I/O: 5V , internal function : 5VSB
17	DGND		
18	BEEP#	OD48 ; 5V	
19	THERM#	OD4 ; 5V	
20	SMI#	OD4 ; 5V	
21	***AOL2INT#***	***OD4 ; 5V***	Active low, until trigger event is cleared.
22	5V	POWER PIN	

23	V100MAIN	1.0V reference voltage	20mA output driving current
24	***V_HM_REF***	3.6V reference voltage	20mA output driving current
25	TXD4	Thermal 4 input pin	
26	TXD3	Thermal 3 input pin	
27	AGND	Analog ground pin	
28	TXD2	Thermal 2 input pin	
29	TXD1	Thermal 1 input pin	
30	VBATDET	Input Range 0~4.096	
31	VCORE0	Input Range 0~4.096	
32	12V	Input Range 0~4.096	
33	1.5V	Input Range 0~4.096	
34	***2.5V***	***Input Range 0~4.096***	
35	SMBCLK4	Analog switch(50ohm); 5VSB	Analog switch
36	SMBDATA4	Analog switch(50ohm); 5VSB	Analog switch
37	SMBCLK3	Analog switch(50ohm); 5VSB	Analog switch
38	SMBDATA3	Analog switch(50ohm); 5VSB	Analog switch
39	SMBCLK2	Analog switch(50ohm); 5VSB	Analog switch
40	SMBDATA2	Analog switch(50ohm); 5VSB	Analog switch
41	SMBCLK1	Analog switch(50ohm); 5VSB	Analog switch
42	SMBDATA1	Analog switch(50ohm); 5VSB	Analog switch
43	SMBCLK	IOD4ts; 5VSB	
44	SMBDATA	IOD4ts; 5VSB	
45	DGND		
46	MLED	OD16 ; 5VSB	
47	PLED	OD16 ; 5VSB	
48	PSON#	OD16-5.6k-5vsb-up ; 5VSB	
49	***3VSB_GATE***	***OUT4 ; 5VSB***	
50	***3VSB_GATE#***	***OUT4 ; 5VSB***	
51	NC		
52	STPCLK#	INts ; 5VSB	***Pin 52 & 53 OR together for FAN control***
53	SUS_STAT#	INts ; 5VSB	
54	5VSB		
55	V100SB	1V reference voltage output	20mA output driving current
56	***BRSTDRVOUT#***	***OUT12***	***IO:5VSB***
57	***PCIRST#***	***OUT12***	***IO:3VSB***
58	3VSB	3.3V standby power	20mA output driving current

		output(10mA)	
59	***MIOBRSTDRVOUT#***	***OUT4***	***IO:3VSB***
60	***RSTDRVIN#***	***INts-down-1.2k***	***IO:3VSB***
61	SUSC#	INts ; 3VSB	
62	SUSB#	INts ; 3VSB	
63	PIXRI#	***OD4-10k-3vsb-up ;3VSB***	
64	SB_PWROK	OUT4; 3VSB	
65	RESETCON	INts-100k-3vsb-up ; 3VSB	
66	RING_IN	***INts-20k-down ; 3VSB***	(OC protect 2mA) with 20Kohm pull-down resistor.
67	***VDDCPUPWROK***		Power pin for CPUPWROK
68	CPUPWROK	***OUT4***	***Pure open-drain. (Function 3VSB; I/O VDDCPUPWROK)***
69	VBAT		
70	NEWCPU#	INts-10M-vbat-up; VBAT	
71	PWRBTN#	INts; VBAT	
72	PS_PGD	INtx; VBAT	
73	JEN	Incs; VBAT	
74	INTRUSION	INts-10M-vbat-up; VBAT	
75	GRSMRST#	OUT4; VBAT	
76	***CKIN***	***INt; VDDCKBF***	***Clock input for clock buffer***
77	***DGND***		
78	***CKOUT1/ VRM_TBLSEL0***	***OUT12; VDDCKBF***	***Clock buffer output 1/ VRM Table select 0 power-on strapping input pin***
79	***CKOUT2/ VRM_TBLSEL1***	***OUT12; VDDCKBF***	***Clock buffer output 2/ VRM Table select 1 power-on strapping input pin***
80	***NC***		
81	***VDDCKBF***		***Clock buffers power pin***
82	***CKOUT3/LM78_A0***	***IO12t; VDDCKBF***	***Clock buffer output 3/Power-on trapping pin for LM78_A0***
83	DGND		
84	100/66#	OD4-1k-3v-up	I/O:3V, function:VBAT

85	133/100#	OD4-1k-3v-up	I/O:3V, function:VBAT
86	3V		
87	PCLK	INt; 3V	PCI clock input for LPC I/F
88	LFRAME#/TGPIO4	IO16t; 3V	
89	LAD3/GPIO3	IO16t; 3V	
90	LAD2/GPIO2	IO16t; 3V	
91	LAD1/GPIO1	IO16t; 3V	
92	LAD0/GPIO0	IO16t; 3V	
93	3V		
94	TGPI6(SCBL40/80#)	IO8ts; 5V	
95	TGPI5(PCBL40/80#)	IO8ts; 5V	
96	CPU_FERR#	INtx1; 5V	***V_{IH}=0.8(min), V_{IL}=0.6(max)***
97	SB_FERR#	OD8; 5V	
98	MEMW#	INts; 5V	
99	***BIOSW#/VIDLIMIT#***	***IO4ts-10k-down; 5V***	BIOS write-protect control output ***Pin use as VIDLIMITpower-on starpping input.***
100	LPC/GPIO#	INts; 5V	Pin use as LPC(“1”)/GPIO(“0”) select input pin.

2 ASIC CONFIGURATION REGISTERS

Register	Offset	Power on/Reset Default value	Description
~~LM78 Register 40h - 4Fh can be accessed in all Banks~~			
Configuration (LM78 compliant)	40h	00000001b	Configuration register ***<7>/RW=1, reset the whole environment monitor sub-unit.*** <6:4>= Reserved <3>/RW=1, Disable the SMI# output without affecting the contents of interrupt status registers. The AMU will stop monitoring. It will resume on clearing of this bit. <2>= Reserved <1>/RW=1, Enable the SMI# output 0, Disable the SMI# output <0>/RW=1, Enable the monitoring operation 0, Disable the monitoring operation
Interrupt Status 1 (Reading the interrupt status register will output the content of the register, and reset the register.) (LM78 compliant)	41h	00000000b	Interrupt status 1 register <7>/RO= 1, indicates a High or Low limit on FAN2 has been exceeded. <6>/RO= 1, indicates a High or Low limit on FAN1 has been exceeded. <5>/RO= 1, indicates a High or Low limit on TXD2 temperature has been exceeded. <4>/RO= 1, indicates a High or Low limit on TXD1 temperature has been exceeded. <3>/RO= 1, indicates a High or Low limit on VIN3 has been exceeded. (+5V) <2>/RO= 1, indicates a High or Low limit on VIN2 has been exceeded. (+3V) <1> ***Reserved*** <0>/RO= 1, indicates a High or Low limit on VIN0 has been exceeded. (Vcore0)

Interrupt Status 2 (LM78 compliant)	42h	00000000b	Interrupt status 2 register <7:6>= Reserved. <5>/RO= 1, indicates a High or Low limit on TXD3 temperature has been exceeded. <4>/RO= 1, indicates chassis intrusion has been detected. **This status bit is power by VBAT.** <3>/RO= 1, indicates a High or Low limit on FAN3 has been exceeded. <2> ***Reserved*** <1> ***Reserved*** <0>/RO= 1, indicates a High or Low limit on VIN4 has been exceeded. (+12V)
SMI# Mask 1 (LM78 compliant)	43h	00000000b	SMI# mask 1 register <7>/RW=1, disable the FAN2 interrupt status bit to generate SMI# interrupt. <6>/RW=1, disable the FAN1 interrupt status bit to generate SMI# interrupt. ***<5>/RW=1, disable the TXD2 interrupt status bit to generate SMI# interrupt.*** <4>/RW=1, disable the TXD1 interrupt status bit to generate SMI# interrupt. <3>/RW=1, disable the VIN3 interrupt status bit to generate SMI# interrupt. (5V) <2>/RW=1, disable the VIN2 interrupt status bit to generate SMI# interrupt. (3V) <1> ***Reserved*** <0>/RW=1, disable the VIN0(VCORE0) interrupt status bit to generate SMI# interrupt..(Vcore0)
SMI# Mask 2 (LM78 compliant)	44h	00000000b	SMI# mask 2 register <7:6>= Reserved ***<5>/RW=1, disable the TXD3 interrupt status bit to generate SMI# interrupt.*** <4>/RW=1, disable the chassis intrusion interrupt status bit to generate SMI# interrupt. <3>/RW=1, disable the FAN3 interrupt status bit to generate SMI# interrupt. <2> ***Reserved***

			<1> ***Reserved*** <0>/RW=1, disable the VIN4 interrupt status bit to generate SMI# interrupt.
Interrupt Status 3 mirror register (read the register will clear status, same as the Reg00h_Bank#3)	45h	00000000	Interrupt Status 3 register (read to clear) <7>/RO= 1, indicates TXD2 temperature sense cann't match the target temperature value in FAN control 2 register. <6>/RO= 1, indicates TXD1 temperature sense can't match the target temperature value in the FAN control 1 register. <5>/RO= 1, indicates TXD3 temperature sense can't match the target temperature value in the FAN control 3 register. <4>/ RO =1, indicates a High or Low limit on VIN11 has been exceeded.(VBATdet) <3>/ RO =1, indicates a High or Low limit on VIN10 has been exceeded.(1.5V) <2>/ RO =1, indicates a High or Low limit on VIN9 has been exceeded.(2.5V) <1>/ RO =1, indicates a High or Low limit on VIN8 has been exceeded.(VBAT) <0>/ RO =1, indicates a High or Low limit on VIN7 has been exceeded.(5VSB)
Intrusion reset	46h	00000000	Intrusion reset register <7>/RW=1, a 20ms LOW pulse will be generated on the internal INTRUDE signal to clear the chassis intrusion Flip-Flop. This bit self clears after the pulse has been output. ***<6>/RW=1, indicates an ASR SMI counter timeout occur. The ASR RESET count register begins to count down. This bit won't be cleared through reset. Only power on or a software write can change its value.*** 0, No ASR SMI counter timeout occurs ***<5>/RW=1, indicates an ASR RESET counter timeout occurs during last reboot. This bit won't be cleared through reset. Only power on or a software write can change its value.*** 0, No ASR RESET counter timeout occurs since

			last reboot this bit is effective when select PATH A *<4>/RO=1, ASR_RESET time-out. this bit is effective when select PATH B* *0, No ASR RESET counter timeout occurs since last reboot.* *This bit is effective when select PATH B and can be cleared by write a "0" to bit 5.* P.S.: Whenever the counter counts down to zero, the corresponding timeout flag will always be set to a "1" no matter whether the corresponding signal is enabled to be asserted or not. By writing a "0" to the bit *6* will deassert the SMI# signal if it is asserted. If the SMI# signal is not asserted (due to ASR SMI# output is disabled), the SMI# signal will be left as deasserted. <3:0>= Reserved
VID/Fan divisor (LM78 compliant)	47h	<7:4>=0101, <3:0>=VID3~0	VID/Fan divisor register <7:6>/RW= Fan 2 tachometer divisor. <5:4>/RW= Fan 1 tachometer divisor. 00 divide by 1 01 divide by 2 10 divide by 4 11 divide by 8 <3:0>/RO= The logic value of VID3~VID0 pins
Interrupt Status 4 mirror register (read the register will clear status, same as the Reg01h_Bank#3)	48h	00000000	Interrupt Status 4 register (read to clear) <7>=Reserved <6> ***Reserved*** <5>/RO= 1, indicates TXD4 temperature sense cann't match the target temperature value in the FAN control 4 register <4> ***Reserved*** <3>/RO= 1, indicates a High or Low limit on TXD4 temperature has been exceeded. <2> ***Reserved*** <1>/RO= 1, indicates a High or Low limit on FAN4 has been exceeded. <0>/ RO =1, indicates a High or Low limit on VIN12 has

			been exceeded.(3VSB)
Chip version and Voltage ID (W83781D compliant)	49h	***<7:1>=0100001*** <0>=VID4	Chip version and Voltage ID register ***<7:1>/RO= version number (2.1 for ASB100-A)*** <0>/RO= The logic value of VID4 pin
LM75 serial address (W83781D compliant)	4Ah	00000001	LM75 serial address register <7>/RW=1, Disable secondary LM75 thermal sensor, (TXD3) 0, Enable secondary LM75 thermal sensor. <6:4>/RW= SMBus lower 3-bit address of secondary LM75 sensor. Default SMBus ID: 1001000 <3>/RW=1, Disable primary LM75 thermal sensor;(TXD2) 0, Enable primary LM75 thermal sensor. <2:0>/RW= SMBus lower 3-bit address of primary LM75 sensor, deafult SMBuz ID : 1001001
Pin Control (W83781D compliant)	4Bh	01000100	Pin control register <7:6>/RW= Fan 3 tachometer divisor. 00 divide by 1 01 divide by 2 10 divide by 4 11 divide by 8 <5:4> = Reserved <3:2>/RW = FSYSCK input pin Clock select 00 input clock is 14.31818Mhz 01 input clock is 24Mhz 10 input clock is 48Mhz 11 reserved ***<1:0> Reserved***
Register reserved for Vendor manufacture test	4Ch Bank#0		This register should not be accessed in normal operation.
Power on voltage check	4Dh	00000000	Power on voltage check register <7>/RW=1, Disable the power on voltage check with beeper alarm feature. 0, Enable the power on voltage check with beeper alarm feature. Note: Which voltages will be checked after power on can be controlled by the

			power_on_voltage_check_mask register with offset 5Eh/5Fh/Bank#0. Those registers should be kept by standby power plane such that once set, it can remember which voltages need to be checked after power on in the future. ***<6:3>Reserved*** ***<2:0>/RW= target temperature tolerance for TXD2, TXD3 and TXD4 (1 ℃ precision)*** Note: Once the power on voltage check finds some abnormal voltage, the beeper will start to beep after 5 second later for S/W a chance to disabled it without extra beep sound.
Bank select (W83781D compliant)	4Eh	10000000	Register Bank select register <7>/RW=1, access register 4Fh high byte register 0, access register 4Fh low byte register <6:4>/RW= target temperature tolerance for TXD1 (1 ℃ precision <3> Reserved <2:0>/RW= 000, select register bank #0 001~010 Reserved 011, select register bank #3 100~110 Reserved 111, select register bank #7 ***This register can be accessed in all banks, and bit2-0 have two independent sets for SMB & LPC I/F.***
Vendor ID (W83781D compliant)	4Fh	<15:0>=0694H (Attansic ID)	Vendor ID register <7:0>/RO=High byte Vendor ID if bit_7 of Bank select register is "1" Low byte Vendor ID if bit_7 of Bank select register is "0"

Register	Offset	Power on/Reset Default value	Description
LM78 Bank #0 Register description ---			
Register reserved for	50~55h		These registers should not be accessed in normal operation.

Vendor manufacture test	Bank#0		
BEEPER Mask 1 (W83781D compliant)	56h Bank#0	11111111b	BEEPER control 1 register <7>/RW=1, disable the FAN2 beeper status bit to generate beeper output. <6>/RW=1, disable the FAN1 beeper status bit to generate beeper output. <5>/RW=1, disable the TXD2 beeper status bit to generate beeper output. <4>/RW=1, disable the TXD1 beeper status bit to generate beeper output. <3>/RW=1, disable the VIN3 beeper status bit to generate beeper output. <2>/RW=1, disable the VIN2 beeper status bit to generate beeper output. <1> ***Reserved*** <0>/RW=1, disable the VIN0 beeper status bit to generate beeper output.
BEEPER Mask 2 (W83781D compliant)	57h Bank#0	11111111b	BEEPER control 2 register <7>/RW=1, Enable the global beeper output. <6>= Reserved ***<5>/RW=1, disable the TXD3 beeper status bit to generate beeper output.*** <4>/RW=1, disable the Chassis intrusion beeper status bit to generate beeper output. <3>/RW,=1, disable the FAN3 beeper status bit to generate beeper output. <2:1> ***Reserved*** <0>/RW=1, disable the VIN4 beeper status bit to generate beeper output.(+12V)
Chip ID (W83781D compliant)	58h Bank#0	00110001	Chip ID register <7:4>/RO= Chip major ID number <3:0>/RO= Chip minor ID number
PWM Fan control	***59h*** ***Bank#0***	10001111b	***Fan control 1 register (PWMFANOUT)*** ***PWM output frequency is setted by PWM frequency select 1 register(18h/bank#3) bit[2:0]*** ***<7>/RW= 1, speed setting mode*** ***<6:4>= Reserved***

			<3:0>/RW= speed grading *0000 (PWMFANOUT DUTY = 15/256)* *0001 (PWMFANOUT DUTY = 31/256)* *0010 (PWMFANOUT DUTY = 47/256)* *0011 (PWMFANOUT DUTY = 63/256)* *0100 (PWMFANOUT DUTY = 79/256)* *0101 (PWMFANOUT DUTY = 95/256)* *0110 (PWMFANOUT DUTY = 111/256)* *0111 (PWMFANOUT DUTY = 127/256)* *1000 (PWMFANOUT DUTY = 143/256)* *1001 (PWMFANOUT DUTY = 159/256)* *1010 (PWMFANOUT DUTY = 175/256)* *1011 (PWMFANOUT DUTY = 191/256)* *1100 (PWMFANOUT DUTY = 217/256)* *1101 (PWMFANOUT DUTY = 223/256)* *1110 (PWMFANOUT DUTY = 239/256)* *1111 (PWMFANOUT DUTY = 256/256)* *<7>/RW= 0, temperature setting mode* *<6:0>/RW= Target temperature (1℃ precision). AMU will automatically adjust the speed of fan to keep the sensing temperature within target temperature. TXD1 signal is used here as temperature sensing source.* *The value will be compared with LM78 (TXD1) temperature register (27h/Bank#0) to determine whether the measured temperature has matched the target temperature.* *NOTE: In order to avoid the fan speed threshing, a tolerance of plus/minus bit_6:bit_4 of 4Eh register should be considered in designing this close-loop control mechanism. In other words, the fan can be kept in any speed when the detected temperature is within (target temperature – tolerance, target temperature + tolerance).* *In temperature setting mode, if the target temperature can not be achieved when fan speed has reached 100% for 3 minutes, bit_6 of interrupt status 3 register(00h/bank#3) will be*

			set. ***Also, if the target temperature is set too high, there may be no fan required. The fan will stop. Again, it is 60 seconds that the fan will really stop after the a fan stop command has been issued. Under this mode, the time interval of the voltage step incremented/ decremented is*** controlled by the fan_step_control register in offset (5Dh/Bank#0). NOTE: BIOS should turn off the FAN control interrupt when using temperature setting mode.
THERM# pin output control register	5Ah Bank#0	00000000	THERM# output pin control <7:4> Reserved ***<3>/RW = 0 disbale TXD4 event trigger THERM# output*** ***= 1 enable TXD4 event trigger THERM# output*** ***<2>/RW = 0 disbale TXD3 event trigger THERM# output*** ***= 1 enable TXD3 event trigger THERM# output*** ***<1>/RW = 0 disbale TXD2 event trigger THERM# output*** ***= 1 enable TXD2 event trigger THERM# output*** ***<0>/RW = 0 disbale TXD1 event trigger THERM# output*** ***= 1 enable TXD1 event trigger THERM# output***
Thermal Sensor type (default: : TXD1 thermal resistor, : TXD2 thermal diode, : TXD3 thermal resistor, : TXD4 thremal diode)	5Bh Bank#0	11011101	Thermal sensor type register <7:6>/RW = type of TXD4(LM78 extension1) 00 no sensor connection, Thermal sensor reading register (Bank#0_17h/97h) is writable,HMI will not update the reading register 01 Thermister/10K,B=3435 10 3904 transistor 11 Intel thermal diode(default) <5:4>/RW= type of TXD 3 (secondary LM75) 00 no sensor connection, Thermal sensor reading register is writable, HMI will not update the reading registe 01 Thermister/10K,B=3435(default)

			10 3904 transistor 11 Intel thermal diode <3:2>/RW= type of TXD2(primary LM75) 00 no sensor connection, Thermal sensor reading register is writable, HMI will not update the reading registe 01 Thermister/10K,B=3435 10 3904 transistor 11 Intel thermal diode(default) <1:0>/RW= type of TXD1(LM78) 00 no sensor connection, Thermal sensor reading register (Bank#0_27h/67h) is writable,HMI will not update the reading registe 01 Thermister/10K,B=3435(default) 10 3904 transistor 11 Intel thermal diode *** This register is powered by 5VSB , reset soure only from NEWCPU_FLAG=0 or RSMRSTZ=0
Reserved	5Ch Bank#0		***Reserved***
Fan step control	5Dh Bank#0	01001000	Fan step control register (for all fanout step time) <7:4>/RW= The time interval, one seconds as a unit, when ***DCFANOUT/PWMFANOUT*** voltage is incremented to increase the fan speed and reduce the temperature (Only when fan control is under temperature setting mode) <3:0>/RW= The time interval, one second as a unit, when ***DCFANOUT/PWMFANOUT*** voltage is decremented to decrease the fan speed (Only when fan control is under temperature setting mode)
Power on Voltage check mask 1	5Eh Bank#0	11100010	Power on Voltage check mask 1 register <7>/RW=1, VIN7 won't be check on power on. 0, VIN7 will be checked on power on.

			<6> ***Reserved*** <5> ***Reserved*** <4>/RW=1, VIN4 won't be check on power on. 0, VIN4 will be checked on power on. <3>/RW=1, VIN3 won't be check on power on. 0, VIN3 will be checked on power on. <2>/RW=1, VIN2 won't be check on power on. 0, VIN2 will be checked on power on. <1> ***Reserved*** <0>/RW=1, VIN0 won't be check on power on. 0, VIN0 will be checked on power on. PS. This register is powered by +5V standby voltage and won't be affected through system reset. It can only be reset by the RSMRST signal.
Power on Voltage check mask 2	5Fh Bank#0	0**00**11111	Power on Voltage check mask 2 register <7:5>= Reserved <4>/RW=1, VIN12 won't be check on power on. 0, VIN12 will be checked on power on. <3>/RW=1, VIN11 won't be check on power on. 0, VIN11 will be checked on power on. <2>/RW=1, VIN10 won't be check on power on. 0, VIN10 will be checked on power on. <1>/RW=1, VIN9 won't be check on power on. 0, VIN9 will be checked on power on. <0>/RW=1, VIN8 won't be check on power on. 0, VIN8 will be checked on power on. PS. This register is powered by +5V standby voltage and won't be affected through system reset. It can only be reset by the RSMRST signal.
Value RAM	00h-3Fh 60h-9Fh Bank#0		

Value RAM- Address 00h~3Fh_Bank#0 or 60h~9Fh_Bank#0 (auto-increment)

Address Bank#0	Address with Auto-increment Bank#0	Description	Remark

20h	60h	VIN0 reading (Vcore0)	
21h	61h	***Reserved***	
22h	62h	VIN2 reading (+3V)	
23h	63h	VIN3 reading (+5V)	
24h	64h	VIN4 reading (+12V)	
25h	65h	***Reserved***	
26h	66h	***Reserved***	
27h	67h	TXD1 temperature reading	If the thermal sensor is not connected, the read out value should be 80h
28h	68h	Fan 1 speed reading default=FFH	If the FAN is not connected, the read out value should be FFh
29h	69h	Fan 2 speed reading default=FFH	If the FAN is not connected, the read out value should be FFh
2Ah	6Ah	Fan 3 speed reading default=FFH	If the FAN is not connected, the read out value should be FFh
2Bh	6Bh	VIN0 (Vcore0)High limit	
2Ch	6Ch	VIN0(Vcore0) Low limit	
2Dh	6Dh	***Reserved***	
2Eh	6Eh	***Reserved***	
2Fh	6Fh	VIN2 (+3V)High limit	
30h	70h	VIN2 (+3V)Low limit	
31h	71h	VIN3 (+5V)High limit	
32h	72h	VIN3 (+5V)Low limit	
33h	73h	VIN4 (+12V)High limit	
34h	74h	VIN4 (+12V)Low limit	
35h	75h	***Reserved***	
36h	76h	***Reserved***	
37h	77h	***Reserved***	
38h	78h	***Reserved***	
39h	79h	TXD1 Ambient over temperature limit Default=50h(80℃)	
3Ah	7Ah	TXD1 Ambient temperature Hysteresis limit Default=4Bh(75℃)	

3Bh	7Bh	Fan 1 fan count limit	
3Ch	7Ch	Fan 2 fan count limit	
3Dh	7Dh	Fan 3 fan count limit	
3E~3Fh	7E~7Fh	Reserved	
00h	80h	VIN7 reading (+5VSB)	
01h	81h	VIN8 reading (VBAT)	
02h	82h	VIN9 reading (+2.5V)	
03h	83h	VIN10 reading (+1.5V)	
04h	84h	VIN11 reading (VBATdet)	
05h	85h	VIN12 reading (+3VSB)	
06h	86h	Reserved	
07h	87h	VIN7 (+5VSB)High limit	
08h	88h	VIN7(+5VSB) Low limit	
09h	89h	VIN8(VBAT) High limit	
0Ah	8Ah	VIN8 (VBAT)Low limit	
0Bh	8Bh	VIN9(+2.5V) High limit	
0Ch	8Ch	VIN9(+2.5V) Low limit	
0Dh	8Dh	VIN10 (+1.5V) High limit	
0Eh	8Eh	VIN10 (+1.5V) Low limit	
0Fh	8Fh	VIN11(VBATdet) High limit	
10h	90h	VIN11(VBATdet) Low limit	
11h	91h	VIN12 (+3VSB) High limit	
12h	92h	VIN12 (+3VSB) Low limit	
13h	93h	Fan 4 speed reading default=FFH	If the FAN is not connected, the read out value should be FFh
14h	94h	***Reserved***	
15h	95h	Fan 4 fan count limit	
16h	96h	***Reserved***	
17h	97h	TXD4 temperature reading register	If the thermal sensor is not connected, the read out value should be 80h
18h	98h	TXD4 Tos register Default=50h(80℃)	
19h	99h	TXD4 Thyst register	

		Default=4Bh(75℃)	
1A~1Fh	9A~9Fh	Reserved	

BANK#3 Registers

Register	Offset	Power on/Reset default value	Description
LM78 Bank # 3 Register description			
Interrupt Status 3	00h Bank#3	00000000	Interrupt Status 3 register (read to clear) <7>/RO= 1, indicates TXD2 temperature sense cann't match the target temperature value in FAN control 2 register. <6>/RO= 1, indicates TXD1 temperature sense cann't match the target temperature value in the FAN control 1 register. <5>/RO= 1, indicates TXD3 temperature sense cann't match the target temperature value in the FAN control 3 register. <4>/ RO =1, indicates a High or Low limit on VIN11 has been exceeded. (VBATdet) <3>/ RO =1, indicates a High or Low limit on VIN10 has been exceeded.(1.5V) <2>/ RO =1, indicates a High or Low limit on VIN9 has been exceeded.(2.5V) <1>/ RO =1, indicates a High or Low limit on VIN8 has been exceeded.(VBAT) <0>/ RO =1, indicates a High or Low limit on VIN7 has been exceeded.(5VSB)
Interrupt Status 4	01h Bank#3	00000000	Interrupt Status 4 register (read to clear) ***<7:6>Reserved*** <5>/RO= 1, indicates TXD4 temperature sense cann't match the target temperature value in the FAN control 4 register <4> ***Reserved*** <3>/RO= 1, indicates a High or Low limit on TXD4 temperature has been exceeded. <2> ***Reserved*** <1>/RO= 1, indicates a High or Low limit on FAN4 has been exceeded. <0>/ RO =1, indicates a High or Low limit on VIN12 has been exceeded.(3VSB)
SMI# Mask 3	02h Bank#3	11111111	SMI# mask3 register <7>/RW=1, disable the TXD2 temperature sense cann't

			match the target temperature value in the FAN control 2 register to generate a SMI# <6>/RW=1, disable the TXD1 temperature sense cann't match the target temperature value in the FAN control 1 register to generate a SMI#. <5>/RW=1, disable the TXD3 temperature sense cann't match the target temperature value in the FAN control 3 register to generate a SMI#. <4>/RW=1, disable the VIN11 interrupt status bit to generate SMI# interrupt(VBATdet) <3>/RW=1, disable the VIN10 interrupt status bit to generate SMI# interrupt(1.5V) <2>/RW=1, disable the VIN9 interrupt status bit to generate SMI# interrupt(2.5V) <1>/RW=1, disable the VIN8 interrupt status bit to generate SMI# interrupt (VBAT) <0>/RW=1, disable the VIN7 interrupt status bit to generate SMI# interrupt(5VSB)
SMI# Mask 4	03h Bank#3	11111111	SMI# mask4 register <7:6>Reserved <5>/RW=1, disable the TXD4 temperature sense cann't match the target temperature value in the FAN control 4 register to generate a SMI#. <4> ***Reserved*** <3>/RW=1, disable the TXD4 interrupt status bit to generate SMI# interrupt <2> ***Reserved*** <1>/RW=1, disable the FAN4 interrupt status bit to generate SMI# interrup <0>/RW=1, disable the VIN12 interrupt status bit to generate SMI# interrupt(3VSB)
Beeper Status 1 (A read to this register will clear/reset all bit-field back to 0)	04h Bank#3	00000000	Beeper status 1 register (read to clear) <7>/RO= 1, indicates a High or Low limit on FAN2 has been exceeded. <6>/RO= 1, indicates a High or Low limit on FAN1 has been exceeded. <5>/RO= 1, indicates a High or Low limit on TXD2 temperature has been exceeded. <4>/RO= 1, indicates a High or Low limit on TXD1 temperature has been exceeded.

			<3>/RO= 1, indicates a High or Low limit on VIN3 has been exceeded. (+5V) <2>/RO= 1, indicates a High or Low limit on VIN2 has been exceeded. (+3V) <1> ***Reserved*** <0>/RO= 1, indicates a High or Low limit on VIN0 has been exceeded. (Vcore0)
Beeper Status 2 (A read to this register will clear/reset all bit-field back to 0)	05h Bank#3	00000000	Beeper status 2 register <7:6>= Reserved. <5>/RO= 1, indicates a High or Low limit on TXD3 temperature has been exceeded. <4>/RO= 1, indicates chassis intrusion has been detected. <3>/RO= 1, indicates a High or Low limit on FAN3 pin has been exceeded. <2:1> ***Reserved*** <0>/RO= 1, indicates a High or Low limit on VIN4 has been exceeded. (+12V)
Beeper Status 3	06h Bank#3	00000000	Beeper Status 3 register (read to clear) <7>/RO= 1, indicates TXD2 temperature sense can match the target temperature value in FAN control 2 register. <6>/RO= 1, indicates TXD1 temperature sense can match the target temperature value in the FAN control 1 register. <5>/RO= 1, indicates TXD3 temperature sense cann't match the target temperature value in the FAN control 3 register. <4>/ RO =1, indicates a High or Low limit on VIN11 has been exceeded.(VBATdet) <3>/ RO =1, indicates a High or Low limit on VIN10 has been exceeded.(1.5V) <2>/ RO =1, indicates a High or Low limit on VIN9 has been exceeded.(2.5V) <1>/ RO =1, indicates a High or Low limit on VIN8 has been exceeded.(VBAT) <0>/ RO =1, indicates a High or Low limit on VIN7 has been exceeded.(5VSB)
Beeper Status 4	07h Bank#3	00000000	Beeper Status 4 register (read to clear) <7:6>=Reserved

			<5>/RO= 1, indicates TXD4 temperature sense cann't match the target temperature value in the FAN control 4 register <4> ***Reserved*** <3>/RO= 1, indicates a High or Low limit on TXD4 temperature has been exceeded. <2> ***Reserved*** <1>/RO= 1, indicates a High or Low limit on FAN4 has been exceeded. <0>/ RO =1, indicates a High or Low limit on VIN12 has been exceeded.(3VSB)
Beeper Mask 3	08h Bank#3	11111111	Beeper mask3 register <7>/RW=1, disable the TXD2 temperature sense cann't match the target temperature value in the FAN control 2 register to generate the beep tone. <6>/RW=1, disable the TXD1 temperature sense cann't match the target temperature value in the FAN control 1 register to generate the beep tone. <5>/RO= 1, disable the TXD3 temperature sense cann't match the target temperature value in the FAN control 3 register to generate the beep tone.. <4>/RW=1, disable the VIN11 beeper status bit to generate the beep tone.(VBATdet) <3>/RW=1, disable the VIN10 beeper status bit to generate the beep tone.(1.5V) <2>/RW=1, disable the VIN9 beeper status bit to generate the beep tone.(2.5V) <1>/RW=1, disable the VIN8 beeper status bit to generate the beep tone. (VBAT) <0>/RW=1, disable the VIN7 beeper status bit to generate the beep tone.(5VSB)
Beeper Mask 4	09h Bank#3	11111111	Beeper mask4 register <7:6>=Reserved <5>/RW=1, disable the TXD4 temperature sense cann't match the target temperature value in the FAN control 4 register to the beep tone <4> ***Reserved*** <3>/RW=1, disable the TXD4 interrupt status bit to generate the beep tone <2> ***Reserved***

			<1>/RW=1, disable the FAN4 interrupt status bit to generate the beep tone <0>/RW=1, disable the VIN12 beeper status bit to generate the beep tone.(3VSB)
Beeper Control	0Ah Bank#3	00000000	Beeper Control register <7:1>= Reserved <0>/RW = 1, BEEPER# pin output for visual identification.LED Flash : LED-On(1sec) -> LED-Off(1sec) -> LED-On(1sec) -> …. 0, BEEPER# pin output for audio identification.Beep sound: 700Hz(0.5sec)-> 350Hz(0.5sec)-> 700Hz(0.5sec)-> ….
Reserved	0Bh Bank#3	00000000	***Reserved***
Reserved	0CH Bank#3	00000000	***Reserved***
Fan4 divisor	0Dh Bank#3	01010000	VID/Fan divisor register <7:6>***Reserved*** <5:4>/RW= Fan 4 tachometer divisor. 00 divide by 1 01 divide by 2(default) 10 divide by 4 11 divide by 8 <3:0>***Reserved***
Reserved	0Eh Bank#3		
Temperature adjust 4	0Fh Bank#3	00000000	Temperature adjustment 4 register <7:5> = Reserved. <4:0>/RW = offset value for TXD4 read out 01111 +30 degree 01110 +28egree 01101 +26 degree 01100 +24 degree 01011 +22 degree

			01010	+20 degree
			01001	+18 degree
			01000	+16 degree
			00111	+14 degree
			00110	+12 degree
			00101	+10 degree
			00100	+8 degree
			00011	+6 degree
			00010	+4 degree
			00001	+2degree
			00000	No adjustment
			11111	-2 degree
			11110	-4 degree
			11101	-6 degree
			11100	-8 degree
			11011	-10 degree
			11010	-12 degree
			11001	-14 degree
			11000	-16 degree
			10111	-18 degree
			10110	-20 degree
			10101	-22 degree
			10100	-24 degree
			10011	-26 degree
			10010	-28 degree
			10001	-30 degree
			10000	-32 degree
Temperature adjust 1	10h Bank#3	00000000	Temperature adjustment 1 register <7:5> = Reserved. <4:0>/RW = offset value for TXD1 read out	

			01111	+30 degree
			01110	+28egree
			01101	+26 degree
			01100	+24 degree
			01011	+22 degree
			01010	+20 degree
			01001	+18 degree
			01000	+16 degree
			00111	+14 degree
			00110	+12 degree
			00101	+10 degree
			00100	+8 degree
			00011	+6 degree
			00010	+4 degree
			00001	+2degree
			00000	No adjustment
			11111	-2 degree
			11110	-4 degree
			11101	-6 degree
			11100	-8 degree
			11011	-10 degree
			11010	-12 degree
			11001	-14 degree
			11000	-16 degree
			10111	-18 degree
			10110	-20 degree
			10101	-22 degree
			10100	-24 degree
			10011	-26 degree
			10010	-28 degree
			10001	-30 degree

			10000 -32 degree
Temperature adjust 2	11h Bank#3	00000000	Temperature adjustment 2 register <7:5> = Reserved. <4:0>/RW = offset value for TXD2 read out 01111 +30 degree 01110 +28egree 01101 +26 degree 01100 +24 degree 01011 +22 degree 01010 +20 degree 01001 +18 degree 01000 +16 degree 00111 +14 degree 00110 +12 degree 00101 +10 degree 00100 +8 degree 00011 +6 degree 00010 +4 degree 00001 +2degree 00000 No adjustment 11111 -2 degree 11110 -4 degree 11101 -6 degree 11100 -8 degree 11011 -10 degree 11010 -12 degree 11001 -14 degree 11000 -16 degree 10111 -18 degree 10110 -20 degree 10101 -22 degree

			10100	-24 degree
			10011	-26 degree
			10010	-28 degree
			10001	-30 degree
			10000	-32 degree
Temperature adjust 3	12h Bank#3	00000000	Temperature adjustment 3 register <7:5> = Reserved. <4:0>/RW = offset value for TXD3 read out	
			01111	+30 degree
			01110	+28egree
			01101	+26 degree
			01100	+24 degree
			01011	+22 degree
			01010	+20 degree
			01001	+18 degree
			01000	+16 degree
			00111	+14 degree
			00110	+12 degree
			00101	+10 degree
			00100	+8 degree
			00011	+6 degree
			00010	+4 degree
			00001	+2degree
			00000	No adjustment
			11111	-2 degree
			11110	-4 degree
			11101	-6 degree
			11100	-8 degree
			11011	-10 degree
			11010	-12 degree
			11001	-14 degree

			11000 -16 degree 10111 -18 degree 10110 -20 degree 10101 -22 degree 10100 -24 degree 10011 -26 degree 10010 -28 degree 10001 -30 degree 10000 -32 degree
DC Fan control *(DAC output)*	13h Bank#3	11111111b	*DC Fan control register (DCFANOUT)* *Fan control mode is setted by 19h/Bank#3_bit0* *PWM output frequency is setted by PWM frequency select 1 register(18h/bank#3) bit[2:0]* *In speed setting mode* *<7:4>/RW= DAC output voltage level* *0000 Fan stop (DCFANOUT1 = 0V)* *0001 (DCFANAOUT=0.3125V)* *0010 (DCFANAOUT=0.625V)* *0011 (DCFANAOUT=0.9375V)* *0100 (DCFANAOUT=1.25V)* *0101 (DCFANAOUT=1.5625V)* *0110 (DCFANAOUT=1.875V)* *0111 (DCFANAOUT=2.1875V)* *1000 (DCFANAOUT=2.5V)* *1001 (DCFANAOUT=2.8125V)* *1010 (DCFANAOUT=3.125V)* *1011 (DCFANAOUT=3.4375V)* *1100 (DCFANAOUT=3.75V)* *1101 (DCFANAOUT=4.0625V)* *1110 (DCFANAOUT=4.375V)* *1111 (DCFANAOUT=4.68V)* *In temperature setting mode* *<7:0>/RW= Target temperature (1 ℃ precision). AMU*

			will automatically adjust the speed of fan to keep the sensing temperature within target temperature. (TXD2, TXD3, and TXD4) signals are used here as temperature sensing source. *The value will be compared with TXD2, TXD3, and TXD4 temperature registers to determine whether the measured temperature has matched the target temperature.* ***NOTE:*** *In order to avoid the fan speed threshing, a tolerance of TXD2, TXD3, and TXD4 should be considered in designing this close-loop control mechanism. In other words, the fan can be kept in any speed when the detected temperature is within (target temperature – tolerance, target temperature + tolerance).* *In temperature setting mode, if the one of three (TXD2, TXD3, and TXD4) target temperature can not be achieved when fan speed has reached 100% for 3 minutes, bit_7 of interrupt status 3 register (00h/BANK#3)will be set.* *Also, if the all target temperatures are set too high, there may be no fan required. The fan will stop. Again, it is 60 seconds that the fan will really stop after the a fan stop command has been issued. Under this mode, the time interval of the voltage step incremented/ decremented is controlled by the fan_step_control register in offset (5Dh/Bank#0). PWM output in target temperature mode is only divided into 16 steps:* *0000 Fan stop (DCFANOUT1 = 0V)* *0001 (DCFANAOUT=0.3125V)* *0010 (DCFANAOUT=0.625V)* *0011 (DCFANAOUT=0.9375V)* *0100 (DCFANAOUT=1.25V)* *0101 (DCFANAOUT=1.5625V)* *0110 (DCFANAOUT=1.875V)* *0111 (DCFANAOUT=2.1875V)* *1000 (DCFANAOUT=2.5V)* *1001 (DCFANAOUT=2.8125V)* *1010 (DCFANAOUT=3.125V)* *1011 (DCFANAOUT=3.4375V)*

			1100 (DCFANAOUT=3.75V) *1101 (DCFANAOUT=4.0625V)* *1110 (DCFANAOUT=4.375V)* *1111 (DCFANAOUT=4.68V)* *NOTE: BIOS should turn off the FAN control interrupt when using temperature setting mode.*
Reserved	14h Bank#3		*Reserved*
Reserved	15h Bank#3		*Reserved*
Reserved	16h Bank#3		*Reserved*
Reserved	17h Bank#3		*Reserved*
PWM Frequency Select	18h Bank#3	00010001	<7:3> Reserved <2:0>/RW : PWMFANOUT frequency select 000 : 46.87KHz 001:23.43KHz (default) 010:11.72KHz 011:5.85KHz 100:2.93KHz *101:3MHz* *110:6MHz* *111:12MHz(FANSYSCLK=24MHz)*
Fan Mode Control	19h Bank#3	*00000001*	*<7:1> Reserved* *<0>/RW= DCFANOUT mode select* *'0': temperature setting mode, '1' : speed setting*
Reserevd	*1Ah* *Bank#3*		*<7:0> Reserved*
AOL2 mask register 1	1Bh Bank#3	11111111	AOL2INT# mask register 1 <7>/RW=1, disable the VIN7 interrupt status bit to generate AOL2INT# interrupt.(5VSB) <6:5>*Reserved* *<4>/RW=1, disable the VIN4 interrupt status bit to*

			generate AOL2INT# interrupt.(+12V) <3>/RW=1, disable the VIN3 interrupt status bit to generate AOL2INT# interrupt.(5V) <2>/RW=1, disable the VIN2 interrupt status bit to generate AOL1INT# interrupt.(3V) <1> ***Reserved*** ***<0>/RW=1,. Disable the VIN0 interrupt status bit to generate AOL2INT# interrupt.(Vcore0)***
AOL2 mask register 2	1Ch Bank#3	00011111	AOL2INT# mask register 2 ***<7:5> Reserved*** <4>/RW=1, disable the VIN12 interrupt status bit to generate AOL2INT# interrupt.(3VSB) <3>/RW=1, disable the VIN11 interrupt status bit to generate AOL2INT# interrupt.(VBATdet) <2>/RW=1, disable the VIN10 interrupt status bit to generate AOL1INT# interrupt.(1.5V) <1>/RW=1, disable the VIN9 interrupt status bit to generate AOL2INT# interrupt.(2.5V) <0>/RW=1,. Disable the VIN8 interrupt status bit to generate AOL2INT# interrupt.(VBAT)
AOL2 mask register 3	1Dh Bank#3	10011111	AOL2INT# mask register 3 <7>/RW=1, disable global AOL2INT# pin output <6:4>Reserved <3>/RW=1, disable the FAN4 interrupt status bit to generate AOL2INT# interrupt. <2>/RW=1, disable the FAN3 interrupt status bit to generate AOL2INT# interrupt <1>/RW=1, disable the FAN2 interrupt status bit to generate AOL2INT# interrupt. <0>/RW=1, disable the FAN1 interrupt status bit to generate AOL2INT# interrupt
No Implement	1Eh,1Fh Bank#3		
ASR control (refer to NOTE 2,3)	20h Bank#3	<7>=0, <6:0>= 0000000	Automatic Server Restart control register <7>/RO= 1, Enable the ASR; 0, Disable the ASR <6:0>/RW= ASR enable/disable pattern field
ASR SMI count (refer to NOTE 2,3)	21h Bank#3	00000000	Automatic Server Restart SMI count register <7:0>/RW=time out period left in minute, where 00000000

			indicates that ASR is disabled.
ASR RESET minute count (refer to NOTE 2,3)	22h Bank#3	00000000	Automatic Server Restart RESET count register <7:0>/RW=time out period left in minute, where minut & second counter both 00000000 indicates that ASR is disabled.
ASR signal control (refer to NOTE 2,3,4)	23h Bank#3	00000000	Automatic Server Restart signal control register <7:3>= Reserved. <2>/RW '0' : select path A (ASR_SMI counter + ASR_RESET counter) '1': select Path B (ASR_RESET counter only) <1>/RW 1, Enable the assert/output of internal AMURSTOUT signal when ASR RESET counter counts down to zero. 0, Disable the output of internal AMURSTOUT signal when ASR RESET counter counts down to zero. The AMURSTOUT won't be asserted until ASR is enabled through writing correct patterns into the ASR control register. <0>/RW= 1, Enable the assert/output of SMI# signal when ASR SMI counter counts down to zero. 0, Disable the output of SMI# signal when ASR SMI counter counts down to zero. . The SMI# won't be asserted until ASR is enabled through writing correct patterns into the ASR control register.
ASR RESET Second counter	24h Bank#3	00000000	Automatic Server Restart RESET count register <7:0>/RW=time out period left in second, where 00000000 indicates that ASR is disabled. Range from 0~59sec (0~3Bh)
No Implement	25-26h Bank#3		
Fan Health Status Rgeister	***27h Bank#3***	*00000000*	***<7:4> Reserved. <3> =1 FAN 4 failed. R/O <2> = 1 FAN 3 failed. R/O <1> = 1 FAN 2 failed. R/O <0> = 1 FAN 1 failed. R/O***
PWMFANOUT No Stop Limit Register	***28h Bank#3***	***00000000***	***<7:4> Reserved. <3:0> No-stop output voltage limitation for***

			PWMFANOUT under temperature mode. (R/W)
DCFANOUT No Stop Limit Register	*29h Bank#3*	*00000000*	*<7:0> No-stop output duty cycle limitation for DCFANOUT under temperature mode. (R/W)*
Reserved	*2Ah Bank#3*		*Reserved*
Reserved	*2Bh Bank#3*		*Reserved*
Reserved	*2Ch Bank#3*		*Reserved*
FAN Output Suspend Control Register	*2Dh Bank#3*	*00000000*	*<7:2> Reserved.* *<1> = 1 Enable PWMFANOUT shuts down under suspend mode.(R/W)* *<0> = 1 Enable DCFANOUT shuts down under suspend mode.(R/W)* *The suspend status indicated by STPCLK# and SUS_STAT#(pin 40 and 56), and both "Low" means "Suspend mode" and FANOUTx stop output if enabled.*
No Implement	2Eh –2Fh Bank#3		
System Management Bus Hub Control Register	*30h Bank#3*	*00000000*	*<7:5> Reserved.* *<4> = 1 Enable SMB hub.(R/W)* *<3> = 1 Disable Channel 4 under SMB hub mode.(R/W* *<2> = 1 Disable Channel 3 under SMB hub mode.(R/W)* *<1> = 1 Disable Channel 2 under SMB hub mode.(R/W)* *<0> = 1 Disable Channel 1 under SMB hub mode.(R/W)*
No Implement	31h –7Fh Bank#3		
Reserved	80h Bank#3		
TGPI/O Register	81h Bank#3	0xx11000	TGPI/O pin register output data register <7> Reserved <6>/RO TGPI6 input data. <5>/RO TGPI5 input data. <4:2>/RW TGPIO[4:2] in/out data, pins is 3V signal level

			I/O mode select by Bank#3_82h_bit[4:2] Output mode – To write data will output at pin, To read will read back the last time wrote data. Input mode – To write data will be ignored, To read will read back the state on pin. ***<1:0>Reserved***
TGPIO I/O mode register	82h Bank#3	00011111	TGPIO[4:2] pins I/O mode register The Register is only effective when LPC/TGPIO trapping state is '0' , select TGPIO function <7:5> Reserved <4:2>/RW TGPIO[4:2] pin in/out mode select = 1 , input mode = 0 , output mode ***<1:0>Reserved***
Trapping Register	83h Bank#3		Pin trapping stats when RESET <7>/RO LPC/TGPIO tarpping state 1: LPC interface enable 0: LPC interface disable, pin LFRAME#, LAD[3:0] used as GPIO function <6>/RO LM78_A0 trapping state 1: LM78 SMBus ID = 0101101 0: LM78 SMBus ID = 0101100 <5>/RO SCBL40/80# trapping state <4>/RO PCBL40/80# trapping state <3>/RO SMBus mode pin state bit 1: SMBus MUX mode 0: SMBus HUB mode <2>/RO PCB2 trapping state <1>/RO PCB1 trapping state ***<0> Reserved.***
SMBus MUX select & Quick Switch MUX select	84h Bank#3	00000000	<7:2> Reserved <1:0>/RW SMBus MUX channel select

			00 : select channel 1 01 : select channel 2 10 : select channel 3 11 : select channel 4 ** Bit<1:0> is only effect when select SMBus Mux mode and LPC interface enable, ** If LPC interface is disabled and SMBus is selected MUX mode, the MUX channel selection is by pin LAD[1:0] , not by this register bit<1:0>. ** This register powered by 5V, reseted by PWROK & RSTDRV#
GPO 7 & 8	85h Bank#3	*00000000*	*<7:2>Reserved* <1:0>/RW TGPIO[8:7] out data, pins is 3V signal level Output mode – To write data will output at pin, To read will read back the last time wrote data.
No Implement	86h-9fh Bank#3		
VBAT backed-up 8 bytes Registers	*A0h-A7h* *Bank#3*	*11111111*	*8 bytes Registers* *These 8 bytes registers are powered by VBAT.*
No Implement	85h –FFh Bank#3		

Below contain the ASUSTeK ASIC extension register definition which should be implemented in the Bank#7 of LM78

Register	Offset	Power on/reset default value	Description
LM78 Bank # 7 ASUS ASIC extension register description			
Access pattern regsiter (Refer to note)	7Eh Bank#7	<7:0>=00000000	<7:0>/RW ASUS ASIC extension register access control pattern field , assess function can only be enabled by consecutively writing a pattern of 40h, 52h, 54h, 52h to the register then Access Control regiater bit7 will set. ** *Register powered by +5V VDD, reset by PWROK or*

			RSTDRV# .
Access control register (Refer to note)	7Fh Bank#7	<7:0>=00000000	<7>/R =1 , ASUS extension register (80h_Bank#7 ~ A7h_Bank#7) access is enable =0, ASUS extension register access is disable /W write bit data '0', will disable ASUS extension register access function, it ignore write bit data '1' to this bit <6:0>Reserved *** Register powered by +5V VDD, reset by PWROK or RSTDRV#*
General Purpose Output 1	80h Bank#7	<7:0>=00000000	General Purpose Output 1 register <7>=/RW, SWRST ,software reset bit for ***IGPO11,12***, and CLKRST#, active high, self–clear, default LOW. If a "1" is written to this register, then the above signals mentioned should be initiated to its default value. <6:4>Reserved ***<3>/RW, DIS_RESETCON = 1 RESETCON input signal is blocked; 0 RESETCON input signal is effective.*** <2>/RW= 1, ***IGPO12*** is HIGH; 0, ***IGPO12*** is LOW <1>/RW= 1, ***IGPO11*** is HIGH; 0, ***IGPO11*** is LOW ***<0>= Reserved*** *** Register powered by +5V VDD, reset by PWROK or RSTDRV# .*
General Purpose Output 2***/VRM Table Select/LPC interface address select***	81h Bank#7	<7:0>=ss000001	General Purpose Output 2 register***/VRM table select/LPC interface address select*** ***<7:6>/RO = 00 VRM 8.4*** ***= 01 VRM 8.5*** ***= 10 VRM 9.0*** ***= 11 Reserved*** ***<5>/RW = 0 LPC I/F access address is 4Eh/4Fh.*** ***= 1 LPC I/F access address is 5Eh/5Fh.*** ***<4:1>= Reserved*** *<0>/RW= 1, **IGPO18** is HIGH. 0, **IGPO18** is LOW.* *** Register powered by 5VSB, initiated by GRSMRST#.*

General Purpose Output 3	82h Bank#7	<7:0>=00000010	General Purpose Output 3 register ***<7:3>= Reserved*** <2>/RW CLR_NEWCPU_EVENT; write this bit '1' will send a low pulse (10us) to CLR_NEWCPU# signal to clean NEWCPU_FLAG event (NEWCPU_FLAG will be set to '1'). This bit will self-clear after the pulse has been output. ****This bit is powered by Battery voltage (VBAT), This bit** can be by battery power-on reset *<1>/RW= 1, **IGPO16** is HIGH. 0, **IGPO16** is LOW.* ****This bit is powered by Battery voltage (VBAT), This bit** **can be initiate by battery power-on reset.** ***<0>= Reserved***
General Purpose Input 1	83h Bank#7	<7:0>=X00000XX	General Purpose Input 1 register <7>/RW=1 soft power on, set by H/W event, when 5VSB power-off change to power-on or SUSC#=0 will set, BIOS can only write '0' to clear, write '1' will be ignored. **This status bit is power by VBAT.** <6:2>= Reserved <1>/R= PWRLOSS_FLAG: 1, ***IGPI2*** is HIGH; 0, ***IGPI2*** is LOW (event happened) **This status bit is power by VBAT.** <0>/R= NEWCPU_FLAG: 1, ***IGPI1*** is HIGH; 0, ***IGPI1*** is LOW (event happened) **This status bit is power by VBAT.**
CLKRST# control register (refer to note)	84h Bank#7	<7:0>=10000011	CLKRST# Output control register <7>/RW= 1, CLKRST# is HIGH. 0, CLKRST# is LOW for 50ms and then return to 1/HIGH. In other words, a 50ms LOW pulse is asserted. *** When bit 7 is programmed to "0", the CLKRST# signal will not be asserted as LOW until CLKRST#*

			delay timer is time out. Once asserted, the LOW level will be kept for 50ms and then de-asserted *** Bit7 Powered by +5VSB , initiated by GRSMRST# or Software reset(80h_Bank#7_bit7),RSTDRV#, LMRST#, Or AMURSTOUT* <6:4> Reserved <3:0>/RW= CLKRST# delay timer, unit : 100ms, default delay timer 300ms *** Powered by +5VSB , reset by GRSMRST#*
Reserved	85H Bank#7		***Reserved***
FS pin Register	86H Bank#7	0sss0000	<7>Reserved. <6>/R=JEN Pin status bit. <5>/R=133/100# Pin status bit. <4>/R=100/66# Pin status bit <3:0> ***Reserved***
FS Register	87H Bank#7	Initial value is depend on JEN – when JEN=1 <7:0>=00111111 when JEN=0 <7:0>=00000011	<7:6>Reserved = 00 <5>/RW=133/100#, representing the register value of 133/100#. <4>/RW=100/66#, representing the register value of 100/66#. <3:0> ***Reserved*** *** Register bit<5:4> is powered by Battery voltage (VBAT), Register bit<5:4> can be set to initial value by IN_NEWCPU#=0 or GRSMRST#=0 or JEN=1* *** Register bit<5:4> is also initiated by AMURSTOUT=0 (ASR timeout event) when Jen=0 and ASR select pathB (23h_Bank#3_bit2=1)*
POR_VID REGISTER	88h Bank#7	<7:0>=00000000	<7:5> Reserved <4:0>/RO Latch VID[4:0] pin state at first time PWROK rising edge when SUSC# ='1' *** powered by VBAT, reseted by VBAT power on*
VID output register	89h Bank#7	<7:0>=0s011111	General Purpose Output 4 register VID output on bit <4:0> <7>= Reserved

			<6>/RO ***VIDLIMIT#*** pin trapping bit, this bit is latched when 5V power on <5>/RW VIDCTRL bit =1, VID4~VID0 are output pins, and bit<4:0> control VID4~0 pin output values. =0, VIDCTRL VID4~0 are input pins and ignore bit<4:0>setting. <4>/RW=***VID4/VID25mV output when bit 5 is set.*** ***<3>/RW=VID3 output when bit 5 is set.*** <2>/RW=VID2 output when bit 5 is set. <1>/RW=VID1 output when bit 5 is set. <0>/RW=VID0 output when bit 5 is set. *** Registers powered by +5VSB, but output buffer driving by +5V. initial value is setted by GRSMRST#=0 or IN_NEWCPU#=0 or Jen=1* *** Register bit<5:0> is also initiated by AMURSTOUT=0 (ASR timeout event) when Jen=0 and ASR select pathB (23h_Bank#3_bit2=1)*
LED control register	8Ah Bank#7	<7:0>=00000000	<7:4> Reserved <3:2>/RW : MLED mode control (default) = '00' : MLED 'ON', MLED pin output 'Low' = '01' : MLED 'OFF', MLED pin output 'Hi' = '10' : MLED flash , 1Hz flash cycle = '11' : MLED flash, 2HZ flash cycle <1:0>/RW : PLED mode control (default) = '00' : PLED 'ON', PLED pin output 'Low' = '01' : PLED 'OFF', PLED pin output 'Hi' = '10' : PLED flash , 1Hz flash cycle = '11' : PLED flash, 2HZ flash cycle *** Registers powered by +5VSB, initial value is setted by GRSMRST#=0* *** PLED & MLED pin output is gated by BXPWROK pin , if BXPWROK pin state is 'Low' , PLED & MLED pin output state is 'Hi' , if BXPWROK pin state*

			is 'Hi' , PLED & MLED pin output state is control by this register.
LPC I/F & PCI CGNT# timing control (POWER by 5V, Initial by PWROK)			
Reserved	90h Bank#7		***Reserved***
LPC wait state register	91h Bank#7	00100000	<7:0> R/W LPC insert wait state number This register is effective when use LPC single-phase access timing mode and the actual inserted wait state number = 8 + <7:0> . Default value is 32 so the LPC wait state number is 40 (=32+8) PCLK cycles
BIOS Write Protection Control Register	92h Bank#7	***00000001***	<7:1> Reseved ***<0>/RW = 0 MEMW# pass to BIOSW#*** ***= 1 MEMW# is blocked and BIOSW# always drive high.***
Over Temp. shutdown control register	93h Bank#7	***00001000***	<7:4> Reserved <3> R/W = 1 Enable TXD4 over temperature shut down function. = 0 Disable TXD4 over temperature shut down function. <2> R/W = 1 Enable TXD3 over temperature shut down function. = 0 Disable TXD3 over temperature shut down function. <1> R/W = 1 Enable TXD2 over temperature shut down function. = 0 Disable TXD2 over temperature shut down function. <0> R/W = 1 Enable TXD1 over temperature shut down function. = 0 Disable TXD1 over temperature shut down function.
TXD1 Temperature High Limit for Power shut-down	94h Bank#7	01100100	<7:0> R/W Temperature high limit for TXD1 to shut-down power.
TXD2 Temperature High Limit for Power shut-down	95h Bank#7	01100100	<7:0> R/W Temperature high limit for TXD2 to shut-down power.
TXD3 Temperature High Limit for Power shut-down	96h Bank#7	01100100	<7:0> R/W Temperature high limit for TXD3 to shut-down power.

down			
TXD4 Temperature High Limit for Power shut-down	*97h Bank#7*	*01010000*	*<7:0> R/W Temperature high limit for TXD4 to shut-down power. Change Shut-down temperature to 80℃.*
Reserved	*98h~A8h Bank#7*		*Reserved*
AOL2 Device SMBus ID (POWER by 5V, Initial by PWROK)			
AOL2 Device ID1 (read the ID use SMBus Receive Byte Protocol, After ID byte, device will send out LM78_Reg41H ISR1 data)	A9h Bank#7	<7:0>=00000000	<7:1> R/W SMBus AOL2 device ID1 <0>R/W = 1, enable the AOL2 ID1 devcice = 0, disable the AOL2 ID1 device
AOL2 Device ID2 (read the ID use SMBus Receive Byte Protocol, After ID byte, device will send out LM78_Reg42H ISR2 data)	AAh Bank#7	<7:0>=00000000	<7:1> R/W SMBus AOL2 device ID2 <0>R/W = 1, enable the AOL2 ID2 devcice = 0, disable the AOL2 ID2 device
AOL2 Device ID3 (read the ID use SMBus Receive Byte Protocol, After ID byte, device will send out LM78_Reg45H ISR3 data)	ABh Bank#7	<7:0>=00000000	<7:1> R/W SMBus AOL2 device ID3 <0>R/W = 1, enable the AOL2 ID3 devcice = 0, disable the AOL2 ID3 device
AOL2 Device ID4 (read the ID use SMBus Receive Byte Protocol, After ID byte, device will send out LM78_Reg48H ISR4 data)	ACh Bank#7	<7:0>=00000000	<7:1> R/W SMBus AOL2 device ID4 <0>R/W = 1, enable the AOL2 ID4 devcice = 0, disable the AOL2 ID4 device

Note:

1. Reading the interrupt/beeper status register will output the content of the register, and reset the register.

2. The ASR is disabled after power on or reset. The function can only be enabled by consecutively writing a pattern of 40h, 52h, 54h, 52h to this field. After the ASR is enabled, bit-7 of ASR control register will be set to "1". To disable the ASR feature, a consecutive pattern of 4Eh, 55h, 44h, 51h should be written into this field. The bit-7 of this register will be reset to "0".

3.Write to the ASR SMI/RESET count register will set the ASR time out period. After a non-zero value is written into ASR

SMI count register, the SMI count register begins to count down no matter the ASR is enabled or disabled. When the

register count down to zero (The bit_7 of the intrusion control register is set to reflect the fact that ASR SMI counter has

count down to zero) and the SMI# output is enabled in the ASR signal control register, SMI# signal will be asserted. At the

same time, the ASR RESET count register begins to count (as long as its value is not zero) no matter the SMI# assertion is

enabled or disabled. When the ASR RESET count register also counts down to zero, the AMURSTOUT (once asserted, it

will last for 30ms and then deasserted automatically) will be asserted to reset the system, if its assertion is enabled by the

bit 1 of ASR signal control register, and bit_7 of the Intrusion Reset register will be set to a "1" to indicate there occurs

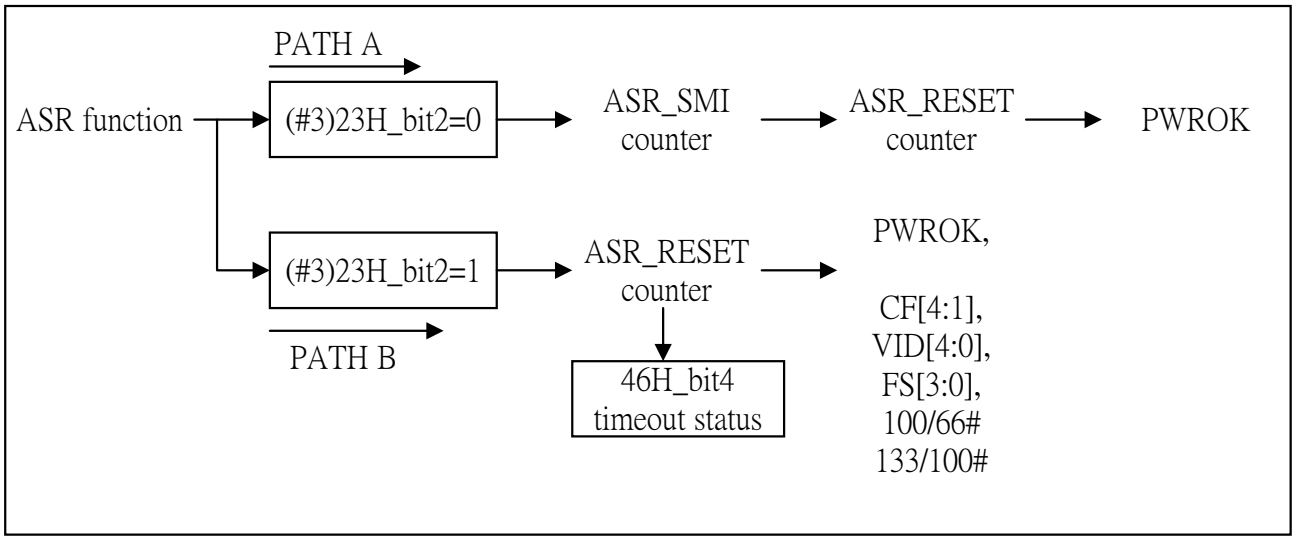
ASR RESET count to zero. The design of ASR signal control register intends to provide the testing of those counter

function. For normal operation, the ASR SMI count register must be updated periodically to prevent the ASR RESET

counter to count down and thus to avoid a system reset. Those registers will count down no matter the ASR feature is

enabled or disabled.

3. ASR path select



4. Bank select Register (Reg4Eh_[2:0]):

There are 3 Banks in the LM78 registers.

1.) Register offset from 40h to 4Fh –

These registers are accessed directly , don't care the value of bank select register.

2.) Register offset in bank#0 –

They belong to Bank#0. To set Reg4Eh_[2:0]=000b before to access these registers.

Value RAM is only assessed in bank#0.

3.) Register offset in bank#3 –

They belong to Bank#3. To set Reg4Eh_[2:0]=011b before to access these registers.

4.) Register offset in bank#7 –

They belong to Bank#7. To set Reg4Eh_[2:0]=111b before to access these registers.

Bank#7

5. Functions of device default I2C ID address :

1.) Enhanced LM78/W83781D compatible function's SMBus ID: 010110(A0)b

Address bit0 (A0) is changeable by trapping pin , so there are two possible I2C ID address:

Trap1 pin=1, I2C ID address=0101101b

Trap1 pin=0, I2C ID address=0101100b

2.) Primary LM75 compatible function's SMBus ID : 1001001b

If Reg4Ah_[3]=0, enable the function, otherwise disable it,

SMBus ID address bit2 to bit0 (A2~A0) is changeable by Reg4Ah_[2:0]

3.) Secondary LM75 compatible function's SMBus ID : 1001001b

Asus Extension GPIO Register's SMBus ID : 1001001b (same as secondary LM75)

If Reg4Ah_[7]=0, enable these function, otherwise disable them,

SMBus ID address bit2 to bit0 (A2~A0) is changeable by Reg4Ah_[6:4]

6. Fan PWM output frequency is difference depend on Fsysck

	Fan PWM Freq. Select = 000	Fan PWM Freq. Select = 000	Fan PWM Freq. Select = 000	Fan PWM Freq. Select = 000	Fan PWM Freq. Select = 000
4Bh_Bank#0 bit<3:2>=00 F=14.3MHz	14.318M / 256 = 55.93KHz	55.93K / 2 = 27.96KHz	27.96K / 2 = 13.98KHz	13.98K / 2 = 6.99KHz	6.99K / 2 = 3.49KHz
4Bh_Bank#0 bit<3:2>=01 F=24MHz	24M / 512 = 46.87KHz	46.87K / 2 = 23.43KHz	23.43K / 2 = 11.72KHz	11.72K / 2 = 5.85KHz	5.85K / 2 = 2.93KHz
4Bh_Bank#0 bit<3:2>=10 F=48MHz	48M / 1024 = 46.87KHz	46.87K / 2 = 23.43KHz	23.43K / 2 = 11.72KHz	11.72K / 2 = 5.85KHz	5.85K / 2 = 2.93KHz

7. Default Power-on-voltage check limit

VIN0 : Vcore0 +/- 10% , Vcore0 is decide by VID

VIN1 : Vcore1 +/- 10% , Vcore1=2.5V

VIN2 : 3.3V +/- 10%

VIN3 : 5V +/- 10%

VIN4 : 12V +/- 20%

VIN7 : 5VSB +/- 10% , 5VSB=5V

VIN8 : VBAT +/- 20% , VBAT=3.3V

VIN9 : 2.5V +/- 10%

VIN10 : 1.5V +/- 10%

VIN11 : VBATDet +/- 20%, VBATDet = 3.3V

VIN12 : 3VSB +/- 20% , 3VSB = 3.3V

9. Register didn't describe above is no implement, to read any dosen't exist register will return value 00h

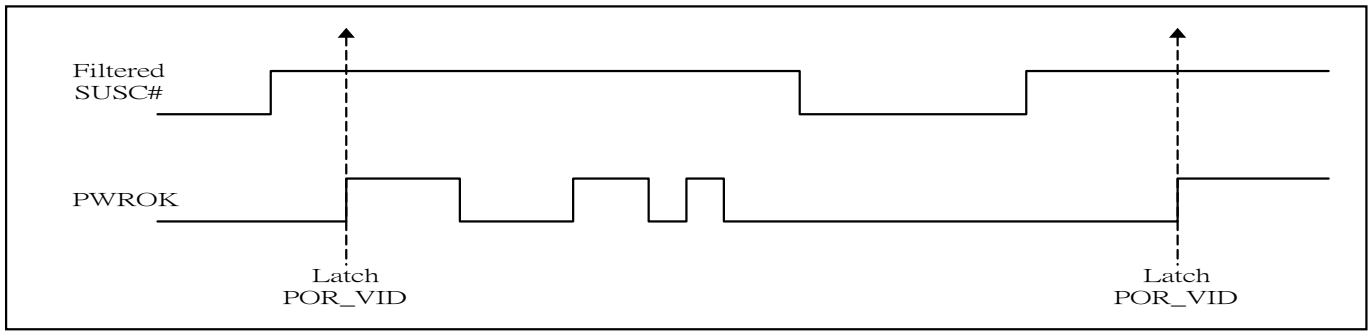
10. For protection, the ASUS ASIC exetension register (LM78 Bank#7) access is disabled after power on or reset. The access

can only be enabled by consecutively writing a pattern of 40h, 52h, 54h, 52h to LM78_Reg7Eh_Bank#7 . After the access is

enabled, bit-7 of ASIC access control register (LM78_Reg7Fh_Bank#7) will be set to "1". To disable the access function

just write '0' to bit-7 of ASIC access control register (LM78_Reg7Fh_Bank#7).

11. PORVID Latched timing



12. When VIDLIMT trapping state is '0', the VID output adjust range show as following

ASUS VID adjustable range Table (VRM 8.4)

VID4	VID3	VID2	VID1	VID0	Normal DACout Voltage	Limited Low Adjustable Range	Limited High Adjustable Range
0	1	1	1	1	1.30	1.20	1.55
0	1	1	1	0	1.35	1.25	1.55
0	1	1	0	1	1.40	1.30	1.70
0	1	1	0	0	1.45	1.30	1.70
0	1	0	1	1	1.50	1.35	1.80
0	1	0	1	0	1.55	1.35	1.80
0	1	0	0	1	1.60	1.40	1.9
0	1	0	0	0	1.65	1.45	1.9

0	0	1	1	1	1.70	1.50	2.0
0	0	1	1	0	1.75	1.55	2.0
0	0	1	0	1	1.80	1.60	2.2
0	0	1	0	0	1.85	1.65	2.2
0	0	0	1	1	1.90	1.70	2.3
0	0	0	1	0	1.95	1.75	2.3
0	0	0	0	1	2.00	1.80	2.4
0	0	0	0	0	2.05	1.85	2.4
1	1	1	1	1	X	X	X
1	1	1	1	0	2.1	1.9	2.5
1	1	1	0	1	2.2	2.0	2.6
1	1	1	0	0	2.3	2.1	2.7
1	1	0	1	1	2.4	2.2	2.8
1	1	0	1	0	2.5	2.3	3.0
1	1	0	0	1	2.6	2.4	3.1
1	1	0	0	0	2.7	2.5	3.2
1	0	1	1	1	2.8	2.5	3.3
1	0	1	1	0	2.9	2.6	3.4
1	0	1	0	1	3.0	2.7	3.5
1	0	1	0	0	3.1	2.8	3.5
1	0	0	1	1	3.2	2.9	3.5
1	0	0	1	0	3.3	3.0	3.5
1	0	0	0	1	3.4	3.1	3.5
1	0	0	0	0	3.5	3.2	3.5

ASUS VID adjustable range Table (VRM 8.5)

VID25mV	VID3	VID2	VID1	VID0	VOUT	Low limit	High Limit
0	0	0	0	0	1.250	1.125	1.500
1	0	0	0	0	1.275	1.150	1.500
0	0	0	0	1	1.200	1.100	1.425
1	0	0	0	1	1.225	1.100	1.450
0	0	0	1	0	1.150	1.050	1.400
1	0	0	1	0	1.175	1.050	1.400

0	0	0	1	1	1.10	1.050	1.350
1	0	0	1	1	1.125	1.050	1.350
0	0	1	0	0	1.05	1.050	1.250
1	0	1	0	0	1.075	1.050	1.275
0	0	1	0	1	1.800	1.600	1.825
1	0	1	0	1	1.825	1.625	1.825
0	0	1	1	0	1.75	1.575	1.825
1	0	1	1	0	1.775	1.575	1.825
0	0	1	1	1	1.700	1.525	1.825
1	0	1	1	1	1.725	1.525	1.825
0	1	0	0	0	1.650	1.475	1.825
1	1	0	0	0	1.675	1.475	1.825
0	1	0	0	1	1.600	1.425	1.825
1	1	0	0	1	1.625	1.425	1.825
0	1	0	1	0	1.550	1.400	1.825
1	1	0	1	0	1.575	1.425	1.825
0	1	0	1	1	1.500	1.350	1.800
1	1	0	1	1	1.525	1.375	1.825
0	1	1	0	0	1.450	1.300	1.725
1	1	1	0	0	1.475	1.325	1.750
0	1	1	0	1	1.400	1.250	1.675
1	1	1	0	1	1.425	1.275	1.700
0	1	1	1	0	1.35	1.200	1.600
1	1	1	1	0	1.375	1.225	1.625
0	1	1	1	1	1.300	1.150	1.550
1	1	1	1	1	1.325	1.175	1.575

ASUS VID adjustable range Table (VRM 9.0)

VID4	VID3	VID2	VID1	VID0	VOUT	Low limit	High Limit
1	1	1	1	1	No CPU		
1	1	1	1	0	1.100	1.100	1.300
1	1	1	0	1	1.125	1.100	1.325
1	1	1	0	0	1.150	1.100	1.350

1	1	0	1	1	1.175	1.100	1.375
1	1	0	1	0	1.200	1.100	1.400
1	1	0	0	1	1.225	1.100	1.425
1	1	0	0	0	1.250	1.100	1.450
1	0	1	1	1	1.275	1.100	1.475
1	0	1	1	0	1.300	1.100	1.500
1	0	1	0	1	1.325	1.125	1.575
1	0	1	0	0	1.350	1.150	1.600
1	0	0	1	1	1.375	1.175	1.625
1	0	0	1	0	1.400	1.200	1.650
1	0	0	0	1	1.425	1.225	1.675
1	0	0	0	0	1.450	1.250	1.700
0	1	1	1	1	1.475	1.275	1.725
0	1	1	1	0	1.500	1.300	1.750
0	1	1	0	1	1.525	1.325	1.775
0	1	1	0	0	1.550	1.350	1.800
0	1	0	1	1	1.575	1.375	1.825
0	1	0	1	0	1.600	1.400	1.850
0	1	0	0	1	1.625	1.425	1.850
0	1	0	0	0	1.650	1.450	1.850
0	0	1	1	1	1.675	1.475	1.850
0	0	1	1	0	1.700	1.500	1.850
0	0	1	0	1	1.725	1.525	1.850
0	0	1	0	0	1.750	1.550	1.850
0	0	0	1	1	1.775	1.575	1.850
0	0	0	1	0	1.800	1.625	1.850
0	0	0	0	1	1.825	1.625	1.850
0	0	0	0	0	1.850	1.650	1.850

Note: PORVID="1FH" is abnormal, "X" means VIDO register remaining as input mode always.

If VIDLIMT trapping state is '0' and the BIOS write data to VID output register (LM78_89h_Bank#7), the VIDO[4:0] value must inside the range table. If the BIOS write VIDO[4:0] value outside the VID range table then the writing data will be ignored and VID output register keep the last value (include VIDCTRL & VID[4:0]).

14. It's ignored the BIOS writes data to VID[4:0] if VIDCTRL bit is '0' (input mode). Any time if BIOS wrte VIDCTRL='0' the

VIDO[4:0] value will be forced to '1Fh' .

15. It's ignored If BIOS write VIDCTRL='1' (output mode) and VID[4:0]='1Fh' to VID output register and the VID output register

will keep last value.

16. It's ignored the BIOS write data to VID output register if PORVID = '1Fh' , the VIDCTRL bit will be forced to '0' (VIDO input

mode).

LM75 register set (Primary & Secondary LM75 each has its own register set))

The standard LM75 contains 4 registers: TEMPERATURE register, CONFIGURE register, Thyst register, Tos register as defined below, but for LPC only byte access there are 3 MSB registers defined for TEMPERATURE register, Thyst register, Tos register

Register	Offset	Power on/reset default value	Description
Temperature	00h	-	Detected temperature register It's different behavior when SMBus & LPC bus to access the register. In SMBus access-- <15:7> Current measured temperature (0.5 ℃ precision, 2's complement value) <6:0> Reserved In LPC Bus acccess Only the LSB of temperature is accessed NOTE: If there is no thermister/transistor connected, the readout value should be all "1"
Control Note: Secondary LM75	01h	<7:0>=00001000	Control register (R/W) <7:5> Reserved

control register bit<2:1> is mirrored of Primary LM75 control register bit<2:1>. It's ignored any data wrote to Secondary LM75 control register bit<2:1>.			<4:3> Fault Queue- Number of faults necessary to detect before setting THERM# output to avoid false tripping due to noise 00 1 time 01 2 times 10 4 times 11 6 times <2> THERM# polarity- 1, active HIGH; 0, active LOW <1> Comparator/interrupt mode- 0, comparator mode; 1, interrupt mode. <0> Shutdown- A "1" will set the LM75 goes to low power shutdown mode.
Thyst	02h	<15:0>= 01001011_00000000 (75 ℃)	Thyst register It's different behavior when SMBus & LPC bus to access the register. In SMBus access-- <15:7> Thyst value (0.5℃ precision). This value is designed to de-asserted THERM# while it is asserted. The THERM# is asserted when LM75 detects a temperature higher than the value in Tos register. Thatan over temperature situation. However, The THERM# won't be de-asserted until the detected temperature goes below the value of Thyst. <6:0> Reserved In LPC Bus acccess Only the LSB of Thyst register is accessed
Tos	03h	<15:0>= 01010000_00000000 (80 ℃)	Tos register It's different behavior when SMBus & LPC bus to access the register. In SMBus access-- <15:7> Over temperature limit (0.5°C precision). The THERM# will be asserted while the detected temperature goes above the value of this register. <6:0> Reserved In LPC Bus acccess

			Only the LSB of Tos register is accessed
Temperature MSB	80h	-	Detected temperature register MSB Only the MSB of temperature is accessed The register is created for LPC byte access
no implement	81h		
Thyst MSB	82h	01001011 (75 ℃)	Thyst register MSB Only the MSB of Thyst register is accessed The register is created for LPC byte access
Tos MSB	83h	01010000 (80 ℃)	Tos register MSB Only the MSB of Tos register is accessed The register is created for LPC byte access

LPC accesss methode

1. LPC I/O Addreess defined

   5Eh : index register, used for command, offset

   5Fh : data register, used for SMBusID, data

2. Command defined

   a.) BEGIN Command: before to accessed ASIC internal registers , must issued the command otherwise access is ignored.

   OUT ***5Eh***, FFh

   OUT ***5Eh***, FFh

   The BEGIN command is finished by consecutively write pattern FFh to I/O port ***5Eh*** twice.

   b.) END Command : after finished accessed ASIC internal registers, used the command to disable following access.

   OUT ***5Eh***,FDh

   OUT ***5Eh***,FDh

   The END command is finished by consecutively write pattern FDh to I/O port ***5Eh*** twice.

   LPC is able to access ASIC internal registers only in the access window from command BEGIN to END period.

3. Register's data access

   Inside the access window, LPC can access ASIC internal regiister's data. The access first set the SMBusID, and set offset then to access register's data.

a.) Set SMBusID : To set SMBusID is finished by consecutively write pattern FEh to I/O port ***5Eh*** twice then follow a write

SMBusID to I/O port ***5Fh***.

. OUT ***5Eh***, FEh

OUT ***5Eh***, FEh

OUT ***5Fh***, SMBusID

b.) Set offset

OUT ***5Eh***, offset

c.) Write register's data

OUT ***5Fh***, data

c.) Read register's data

IN ***5Fh***, data

4. Access last SMBusID

OUT ***5Eh***, FEh

OUT ***5Eh***, FEh

IN ***5Fh***, last_SMBusID

5. Access last offset

IN ***5Eh***, last_offset

6. Programming Note:

a.) Due to the command is combined by consecutively write pattern (FFh/FEh/FDh) to I/O port ***5Eh*** twice, it can not happen the

same sequence during normal data access, otherwise it could be recognized as a valid command.

b.)Due to the LPC and SMBus could access the ASB100 at the same time. The Bank selection may be changed by each and

the result will cause data access error. To solve the problem there are 2 sets Bank selection (LM78_Reg4Eh_Bit<2:0>) for LPC & SMBus each.

SMBus MUX Control Description

The SMBus MUX channel may be selected by MUXS[1:0](pin LAD[1:0]/ MUXS[1:0]) ,
or by LM78_Reg84h_Bank#3_bit<1:0> depend on LPC/TGPIO trapping state.

SMBus MUX select the SMBus device connection is one-to-one , and SMBus traffic only existed between the host and the selected device, others non-selected device can not watch the SMBus signal traffic. ***ASB100 is always connected to I2C bus.***

1.) If LPC interface enable that means LPC/TGPIO trapping state is '1' --
(The trapping state can be read by M78_Reg83h_Bank#3_bit7)

When LPC/TGPIO trapping state is '1' , SMBus MUX channel is selected by LM78_Reg84h_Bank#3_bit<1:0>

	LM78_Reg84h_Bank#3_bit<1:0> = 00	LM78_Reg84h_Bank#3_bit<1:0> = 01	LM78_Reg84h_Bank#3_bit<1:0> = 10	LM78_Reg84h_Bank#3_bit<1:0> = 11
SMBSDA pin (host side)	***SMBSDATA1 pin (device side)***	***SMBSDATA2 pin (device side)***	***SMBSDATA3 pin (device side)***	***SMBSDATA4 pin (device side)***
SMBSCL pin (host side)	***SMBSCLK1 pin (device side)***	***SMBSCLK2 pin (device side)***	***SMBSCLK3 pin (device side)***	***SMBSCLK4 pin (device side)***

2.) If LPC interface disable that means LPC/TGPIO trapping state is '0' --
When LPC/TGPIO trapping state is '0' , SMBus MUX channel is selected by MUXS[1:0](pin LAD[1:0]/MUXS[1:0])

	Pin MUXS[1:0] = 00	Pin MUXS[1:0] = 01	Pin MUXS[1:0] = 10	Pin MUXS[1:0] = 11
SMBSDA pin (host side)	***SMBSDATA1 pin (device side)***	***SMBSDATA2 pin (device side)***	***SMBSDATA3 pin (device side)***	***SMBSDATA4 pin (device side)***
SMBSCL pin (host side)	***SMBSCLK1 pin (device side)***	***SMBSCLK2 pin (device side)***	***SMBSCLK3 pin (device side)***	***SMBSCLK4 pin (device side)***

Application circuit for Voltage & Temperature Measurement

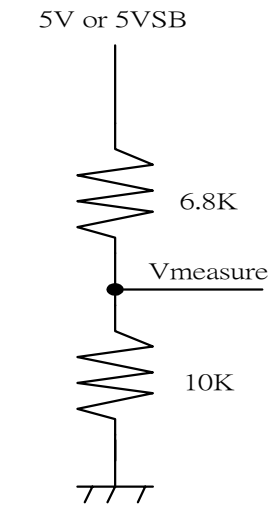


Fig. (A)
IC internal CKT:
Resistor dividor is
built-in

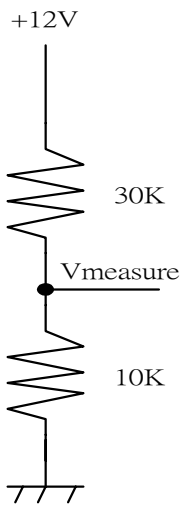


Fig. (B)

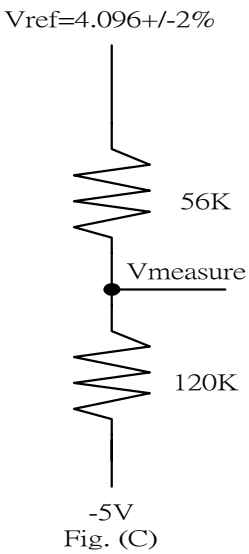


Fig. (C)

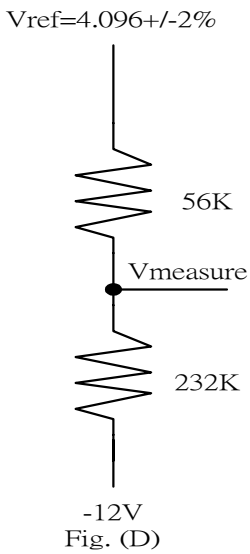


Fig. (D)

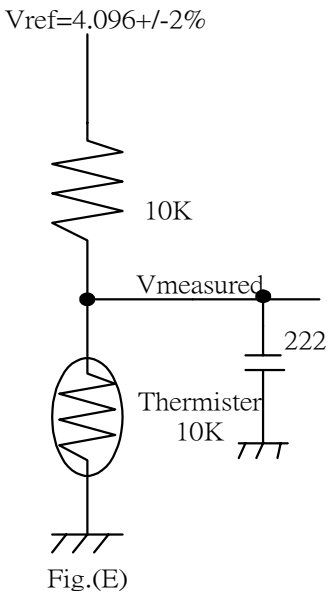


Fig.(E)

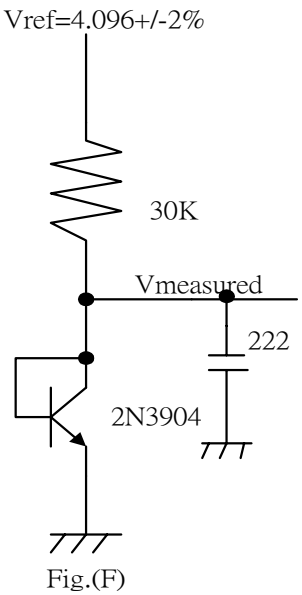


Fig.(F)

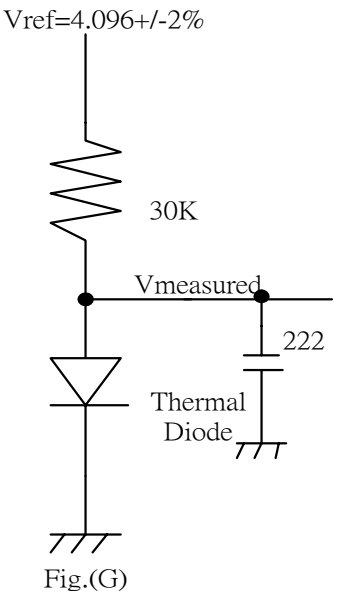


Fig.(G)