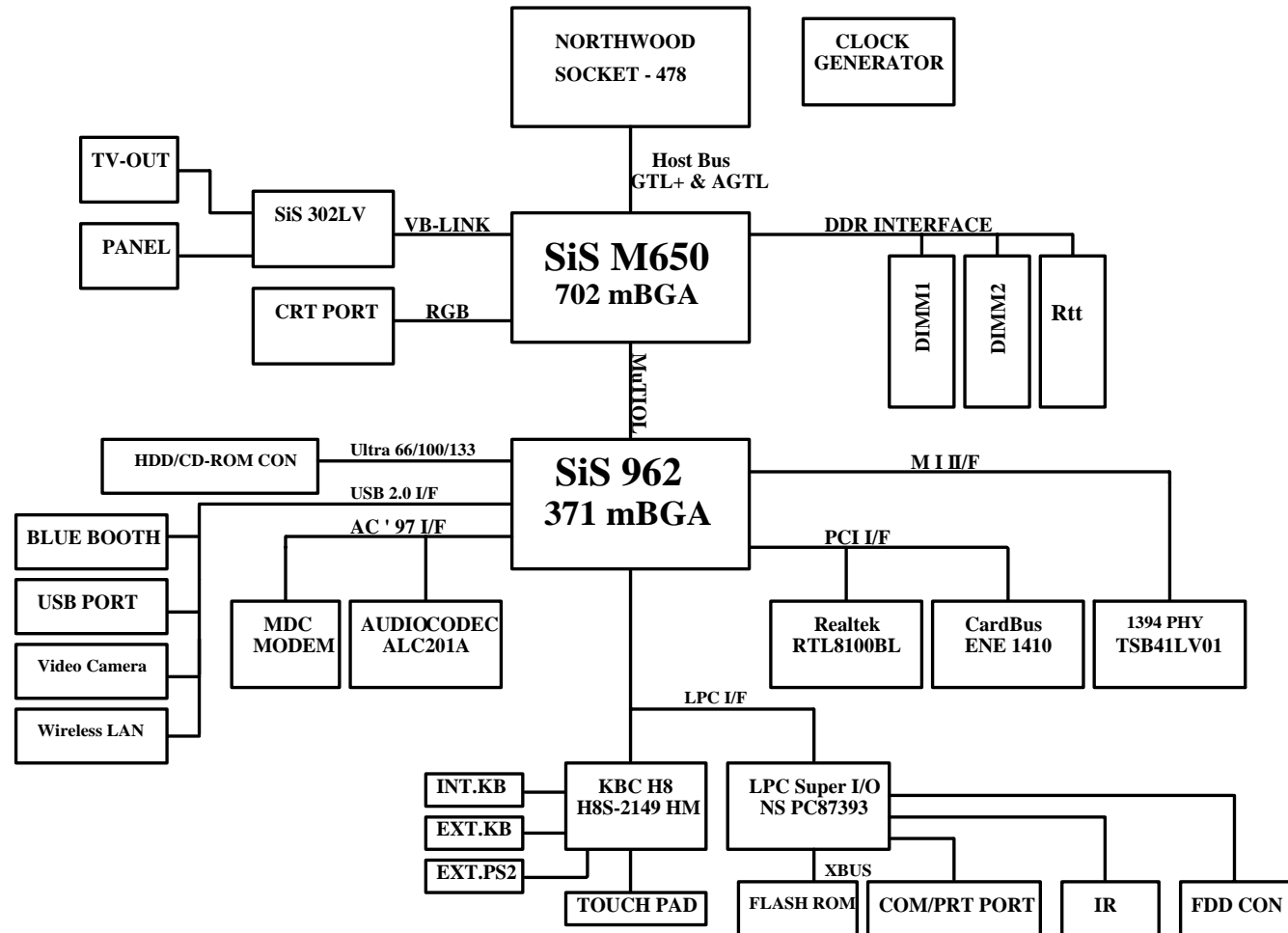


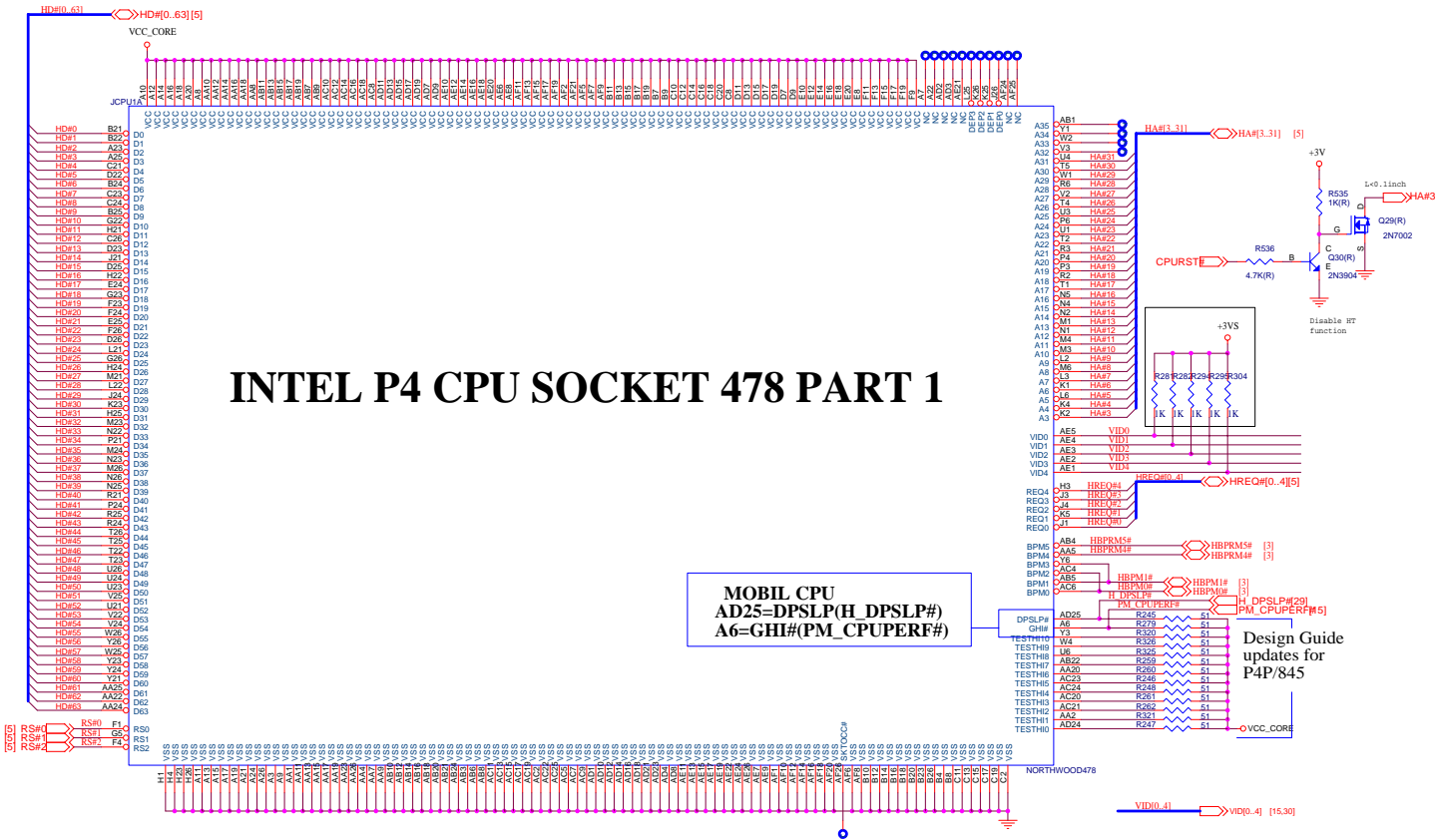
System Block Diagram

D400 System Block Diagram



Sheet 1 of 35
System Block
Diagram

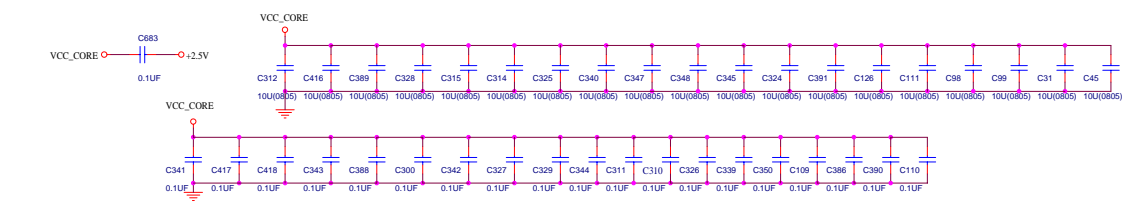
Socket 478 1 of 2



INTEL P4 CPU SOCKET 478 PART 1

MOBIL CPU
AD25=DPSLP(H_DPSLP#)
A6=GHI#(PM_CUPERF#)

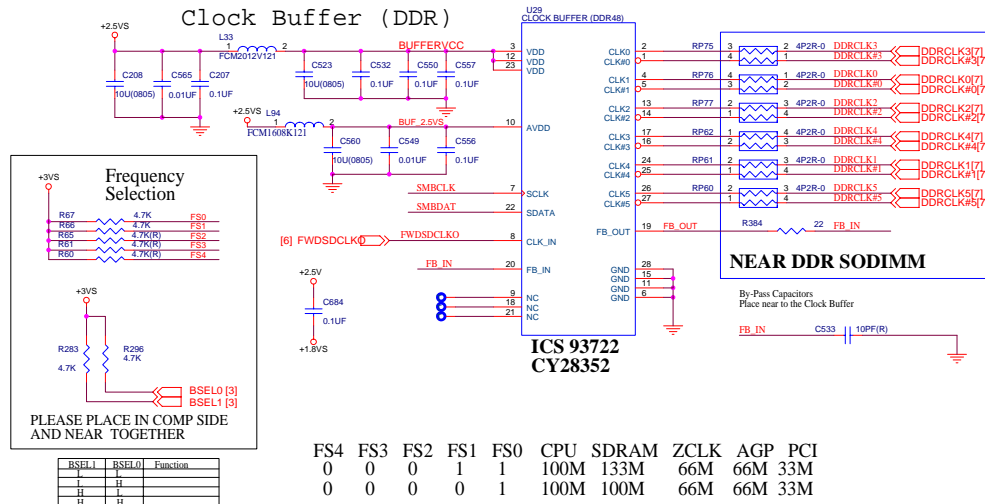
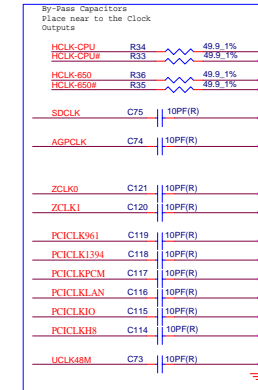
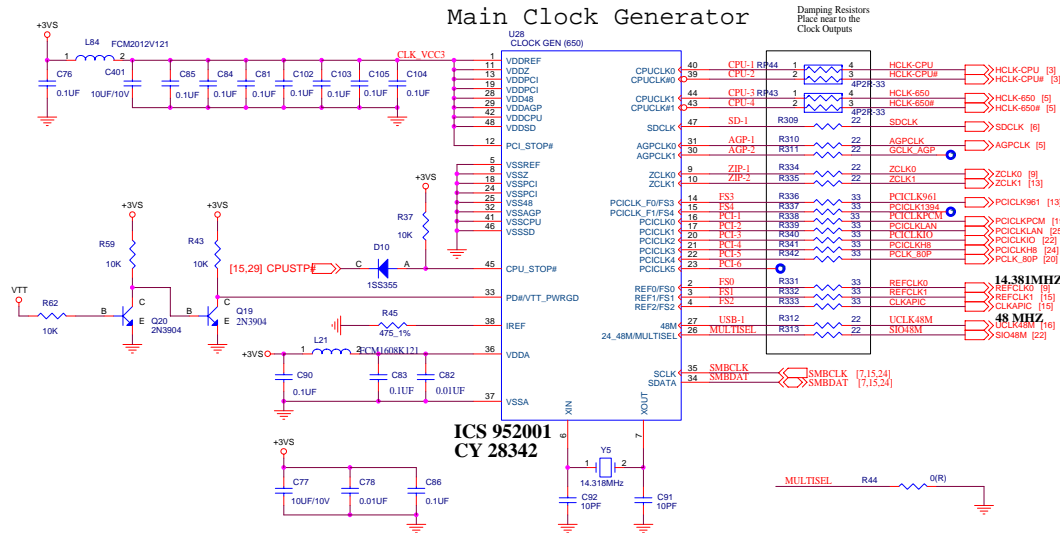
Design Guide updates for P4P/845



Sheet 2 of 35
 Socket 478 1 of 2

B. Schematic Diagrams

Clock Generator



B. Schematic Diagrams

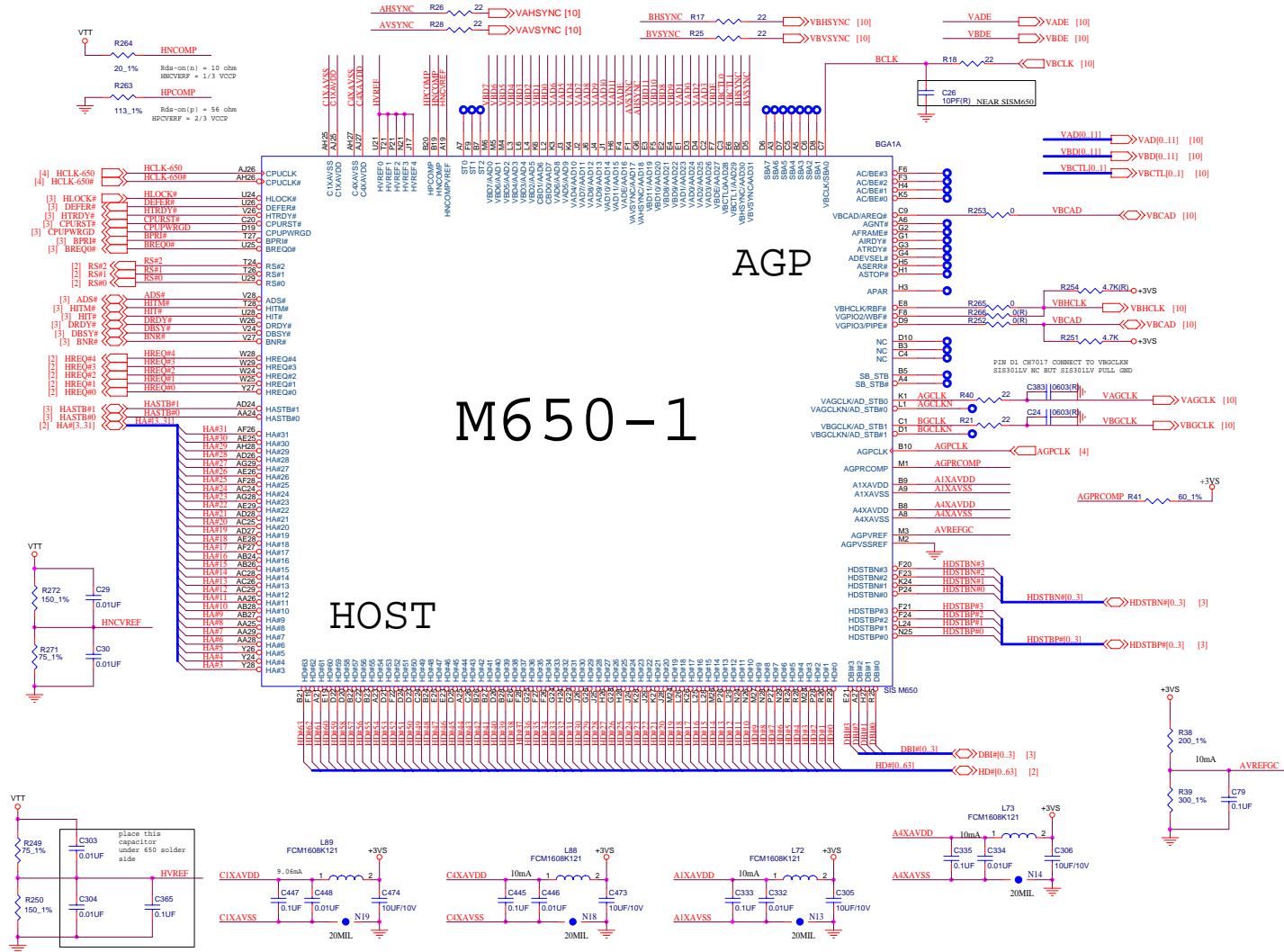
Sheet 4 of 35
Clock Generator

Schematic Diagrams

M650 (Host/AGP) 1 of 4

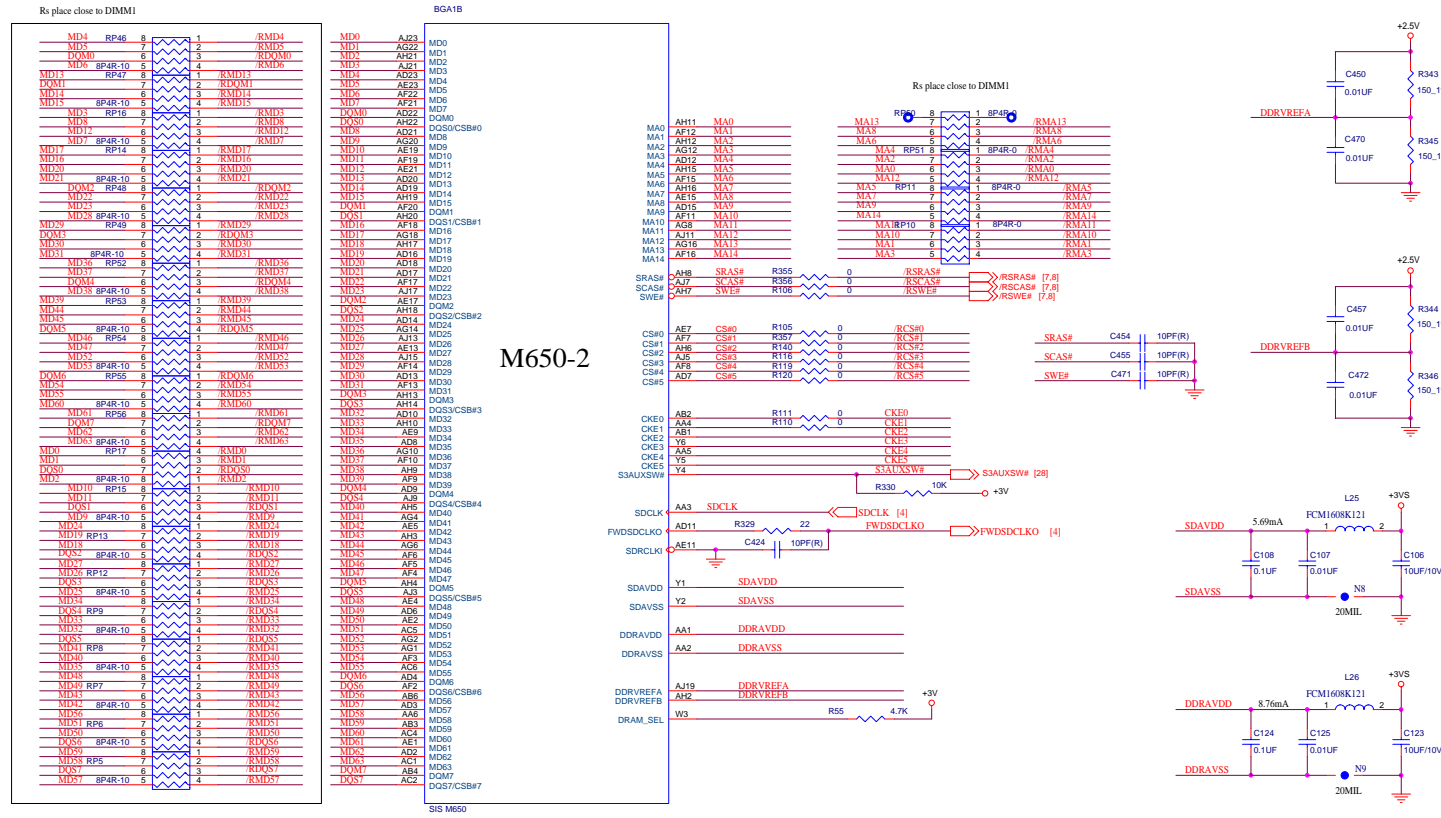
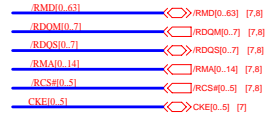
B.Schematic Diagrams

Sheet 5 of 35
M650 (Host/AGP)
1 of 4



M650-1

M650 (Memory for DDR) 2 of 4



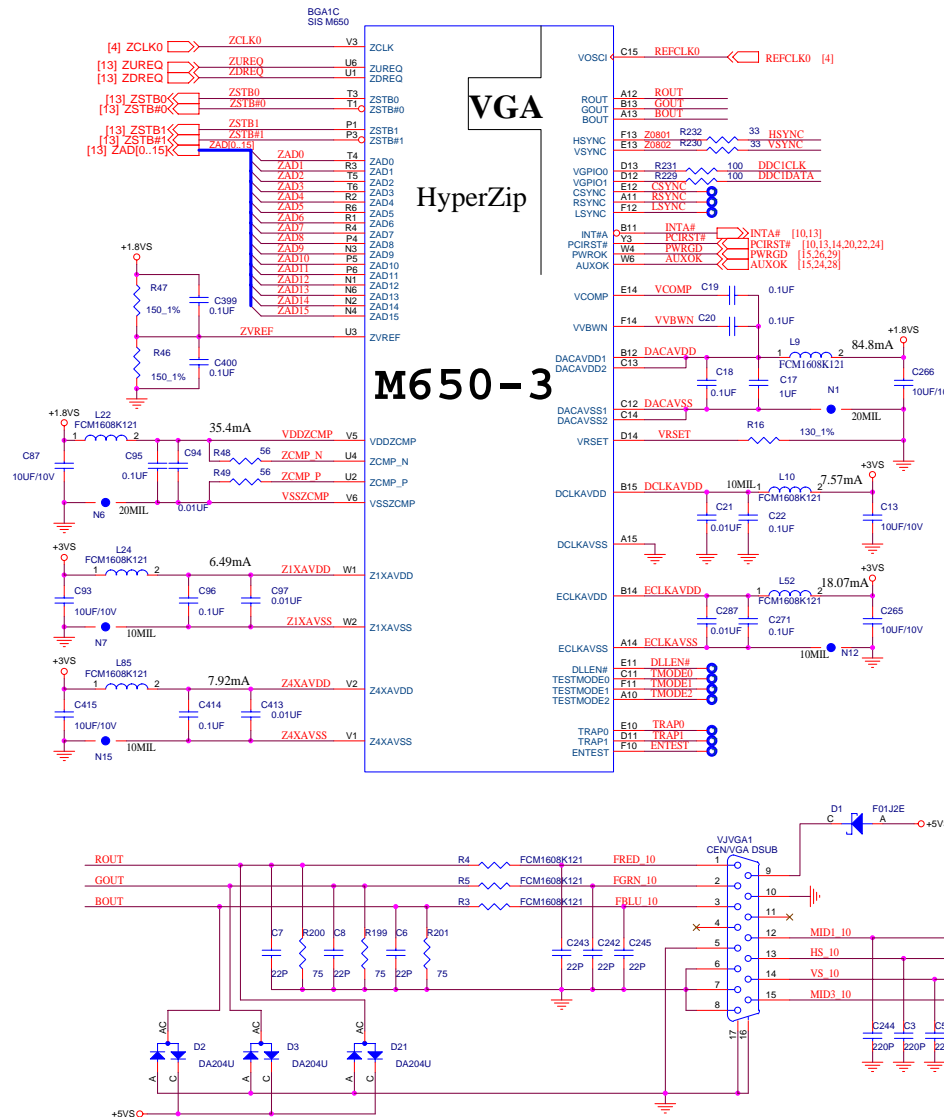
Sheet 6 of 35
M650
(Memory for DDR)
2 of 4

B. Schematic Diagrams

Schematic Diagrams

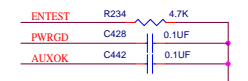
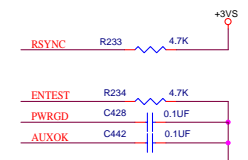
M650 (& CRT Out) 3 of 4

Sheet 7 of 35
M650 & CRT Out
3 of 4

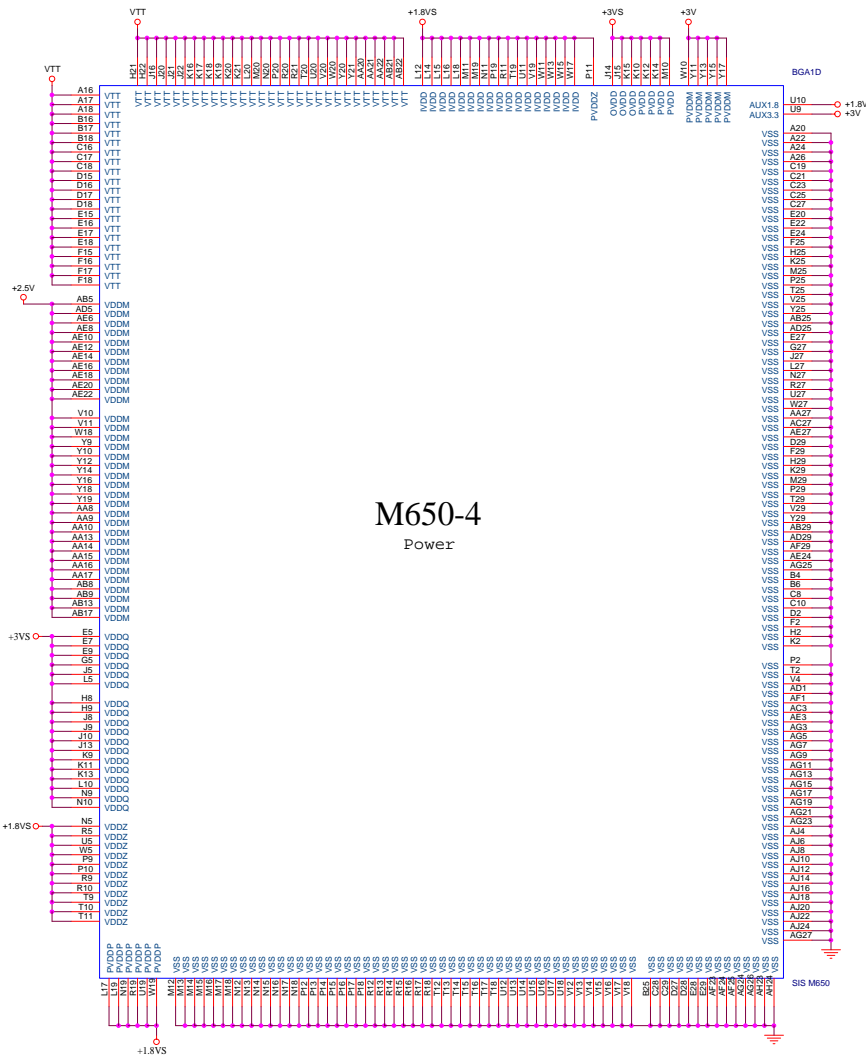


NOTE: This page is for universal PCB design (suitable for both 645 or 650)

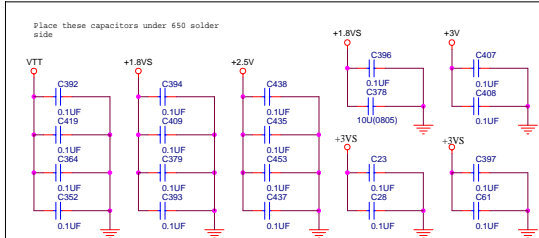
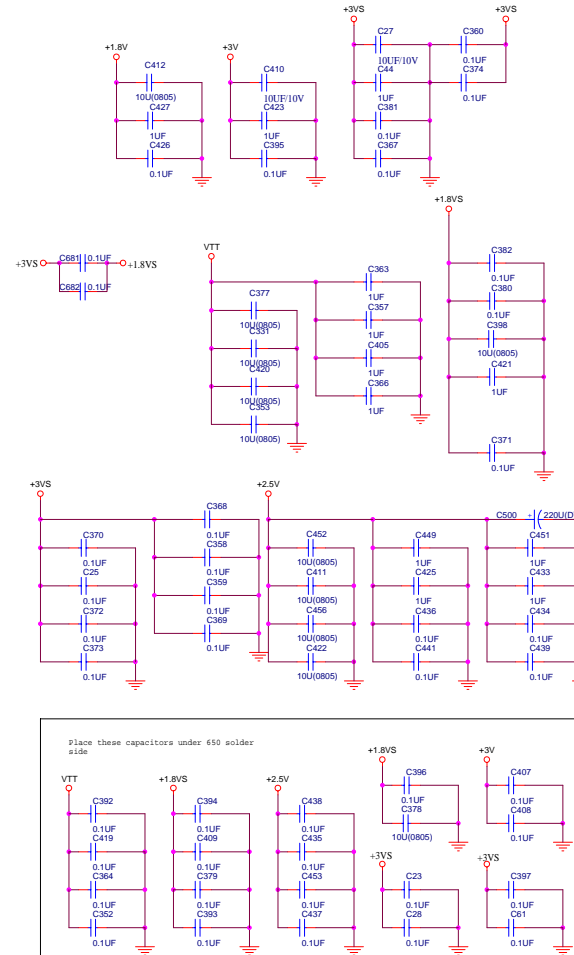
Trap	0	1	Default	embedded null-low (30-50K Ohm)
DLLEN#	enable PLL	disable PLL	0	yes
DRAM_SEL	SDR	DDR	1(DDR)	yes
TRAP0	normal	NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)		0	
CSYNC	enable VB		0	
RSYNC	enable VGA interface		1	
LSYNC	enable panel link		0	



M650 (Power) 4 of 4



M650-4
Power



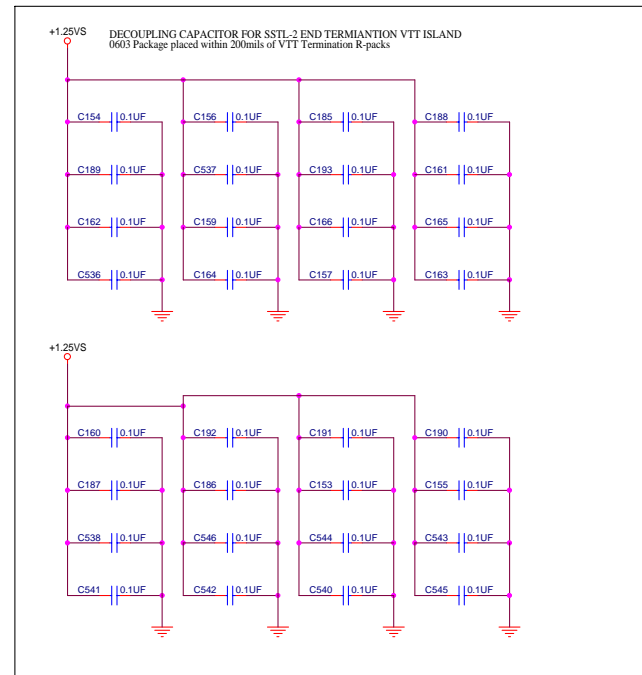
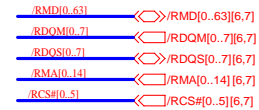
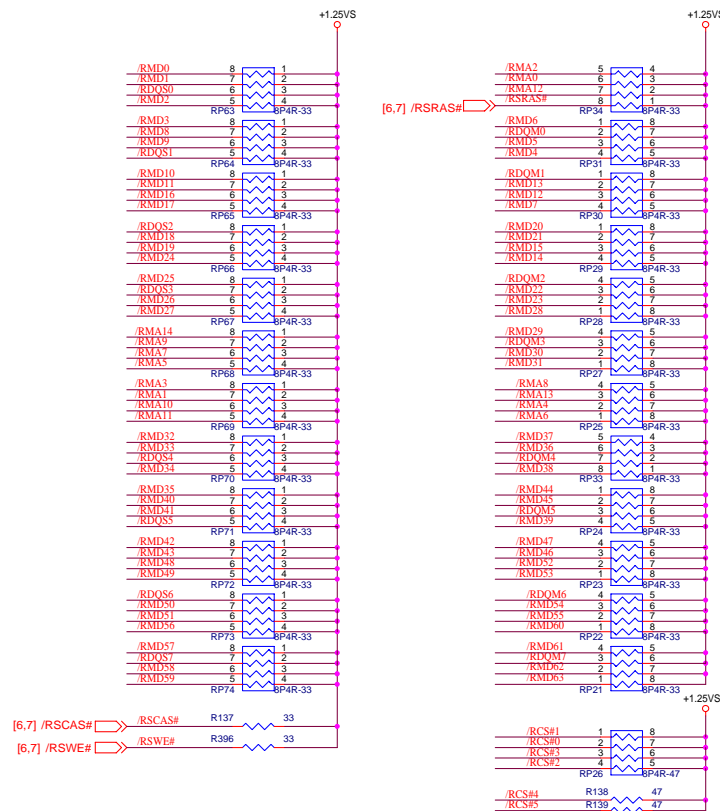
Sheet 8 of 35
M650 (Power)
4 of 4

B. Schematic Diagrams

DDR SSTL-2 Termination

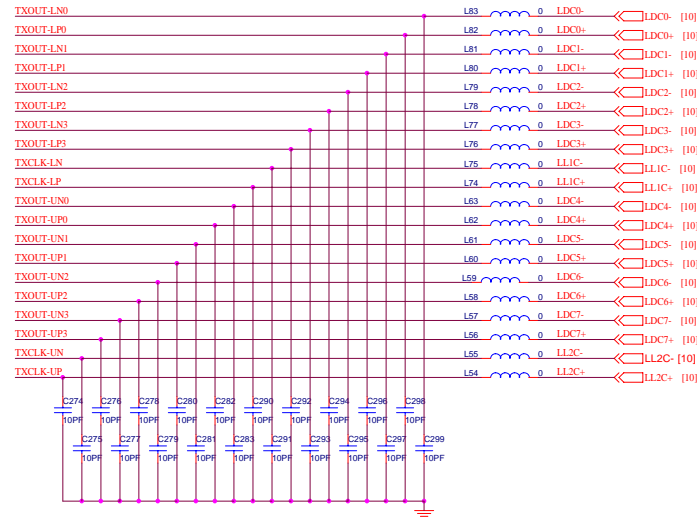
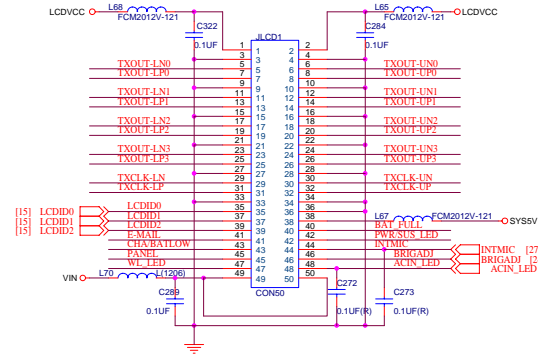
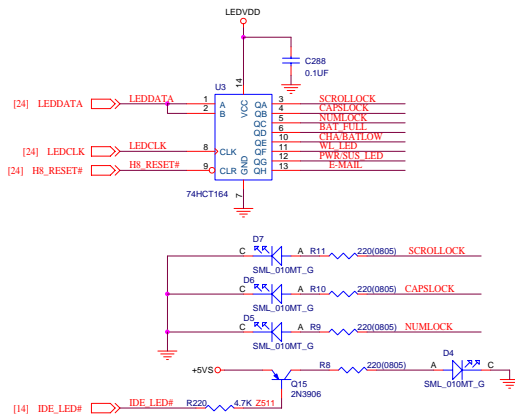
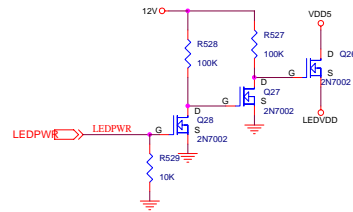
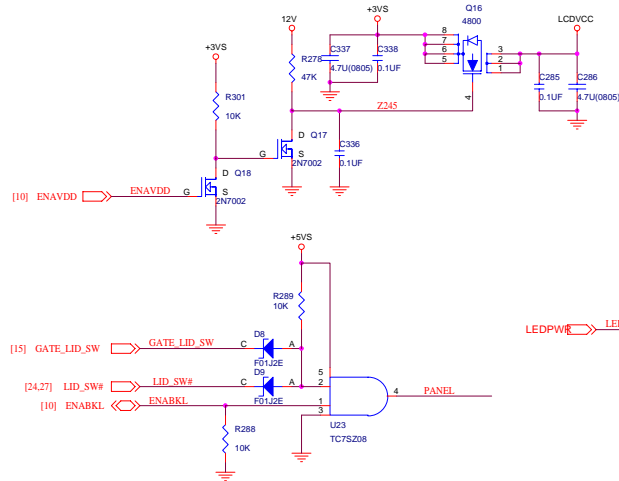
SSTL-2 Termination Resistors

MD/DQM/(DQS) MA/Control CS	DDR SSTL-2 SSTL-2 OD 2.5V	Rs 10 0 0	R _{tt} 33 33 47



Sheet 10 of 35
DDR SSTL-2
Termination

Panel Con & LED Indicator



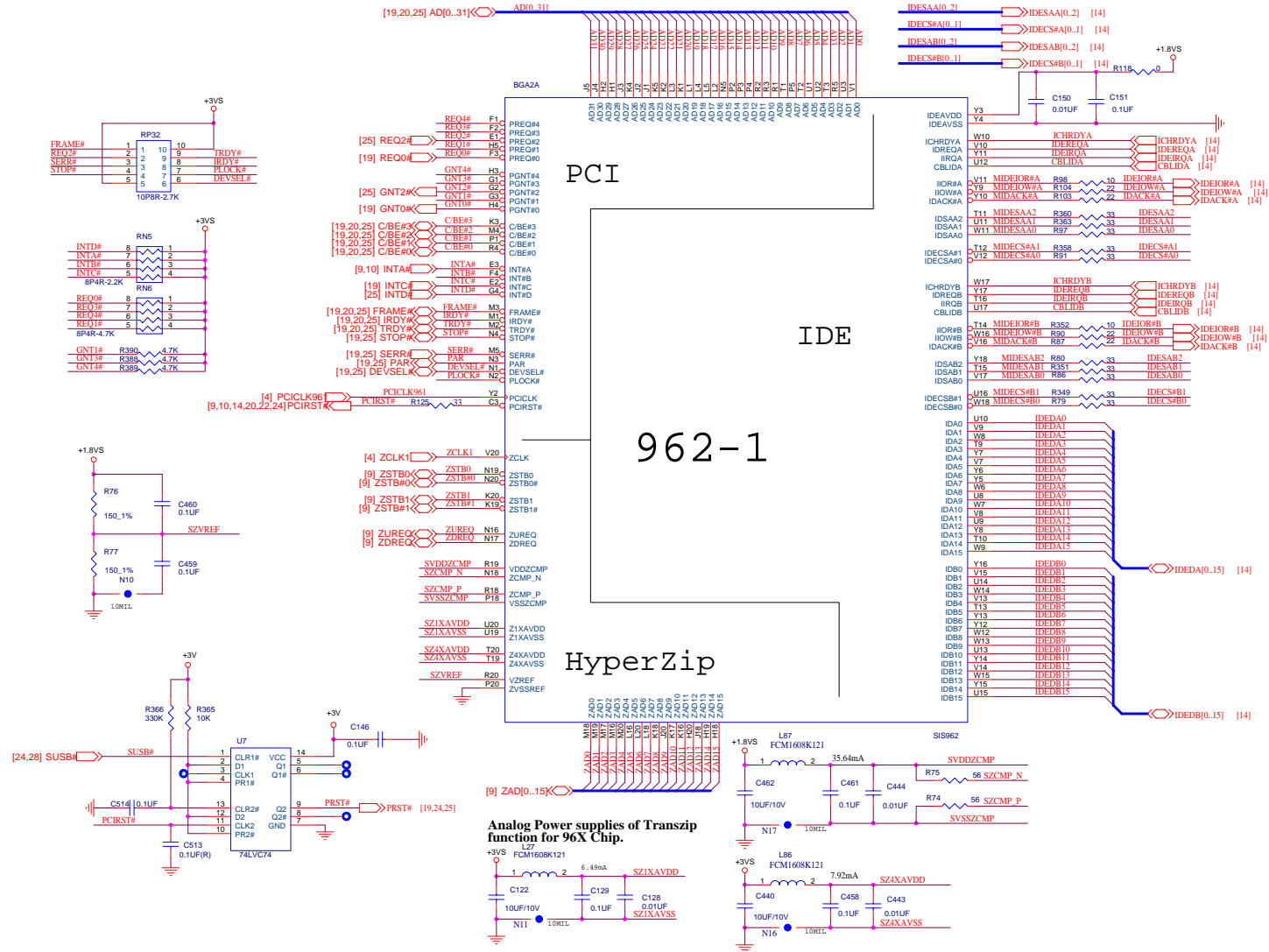
Sheet 12 of 35
Panel Con & LED
Indicator

Schematic Diagrams

962 (PCI/IDE/HyperZip) 1 of 4

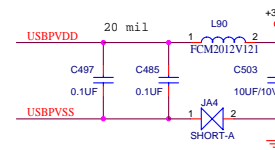
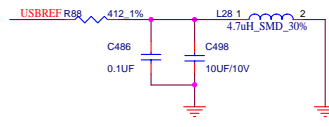
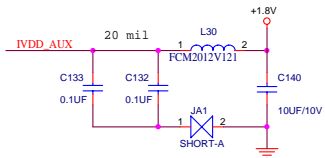
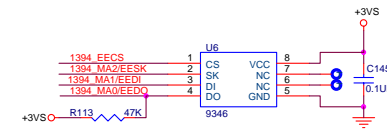
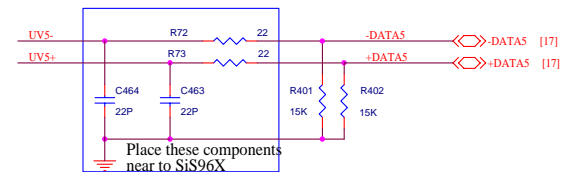
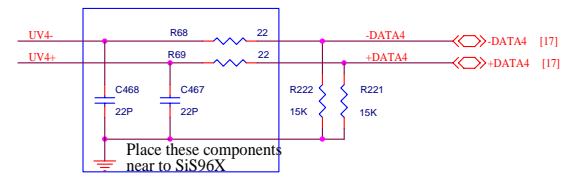
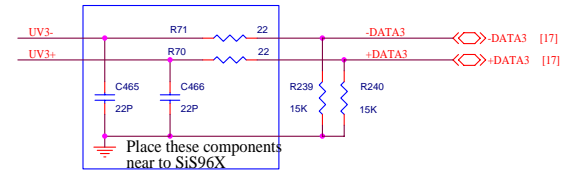
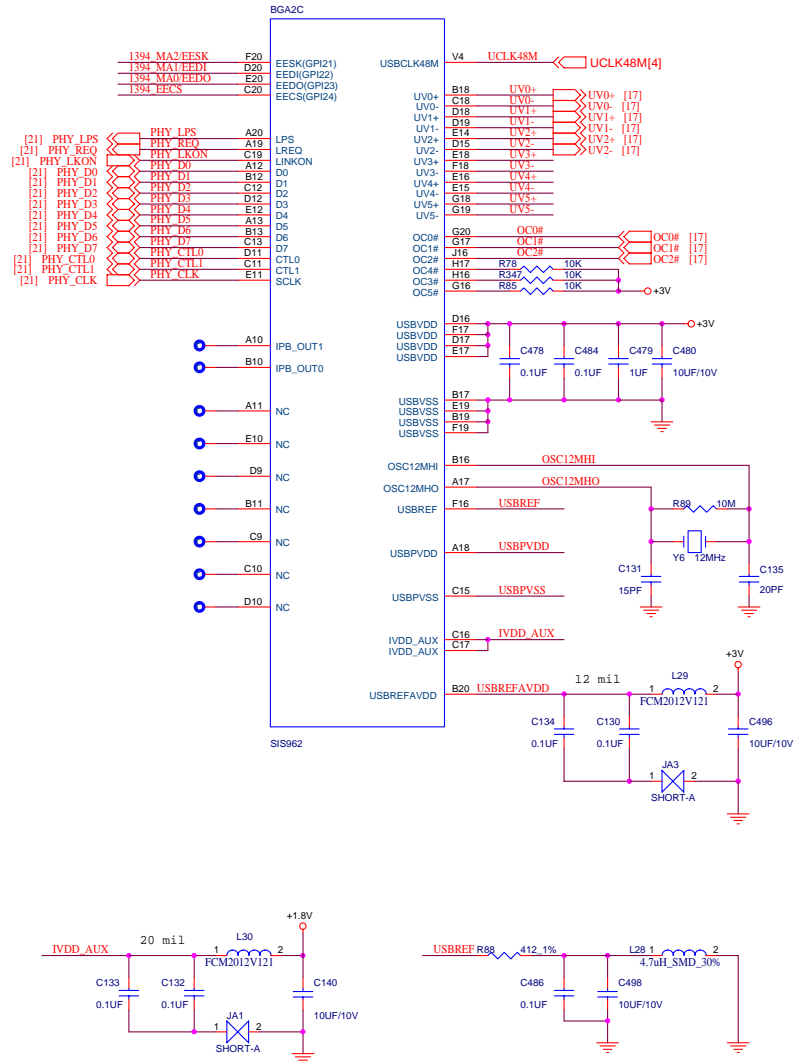
B.Schematic Diagrams

Sheet 13 of 35
962 (PCI/IDE/
HyperZip)
1 of 4

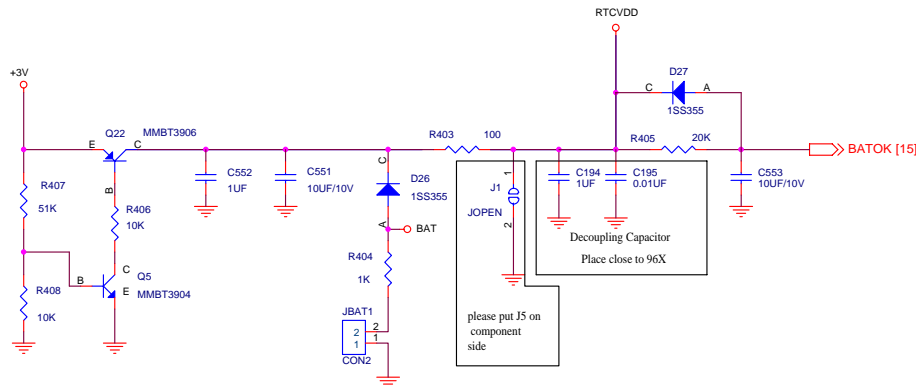
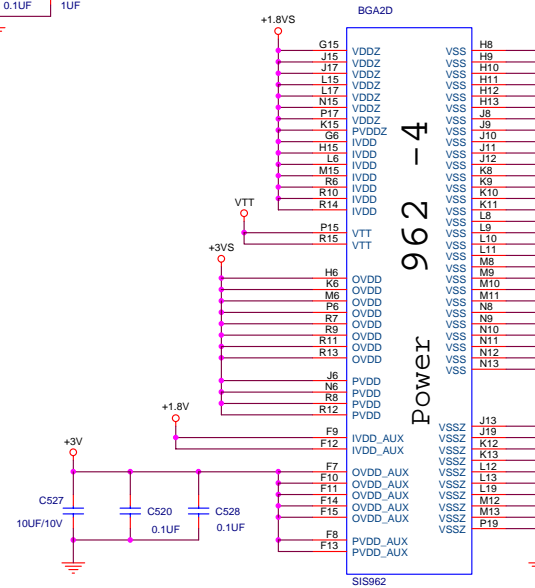
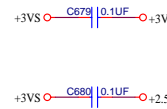
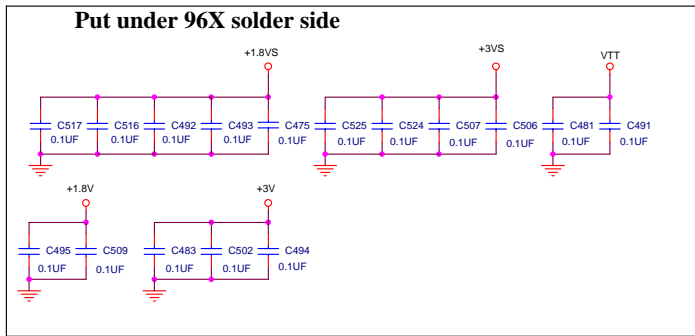
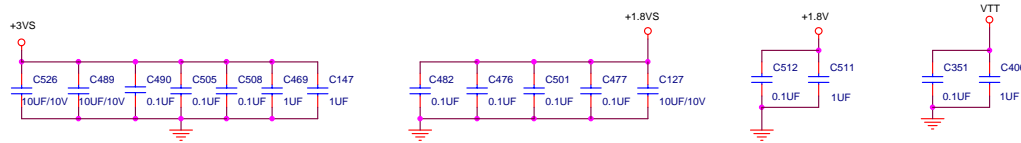


962 (USB I/F) 3 of 4

Sheet 15 of 35
962 (USB I/F)
3 of 4



962 (Power & RTC) 4 of 4



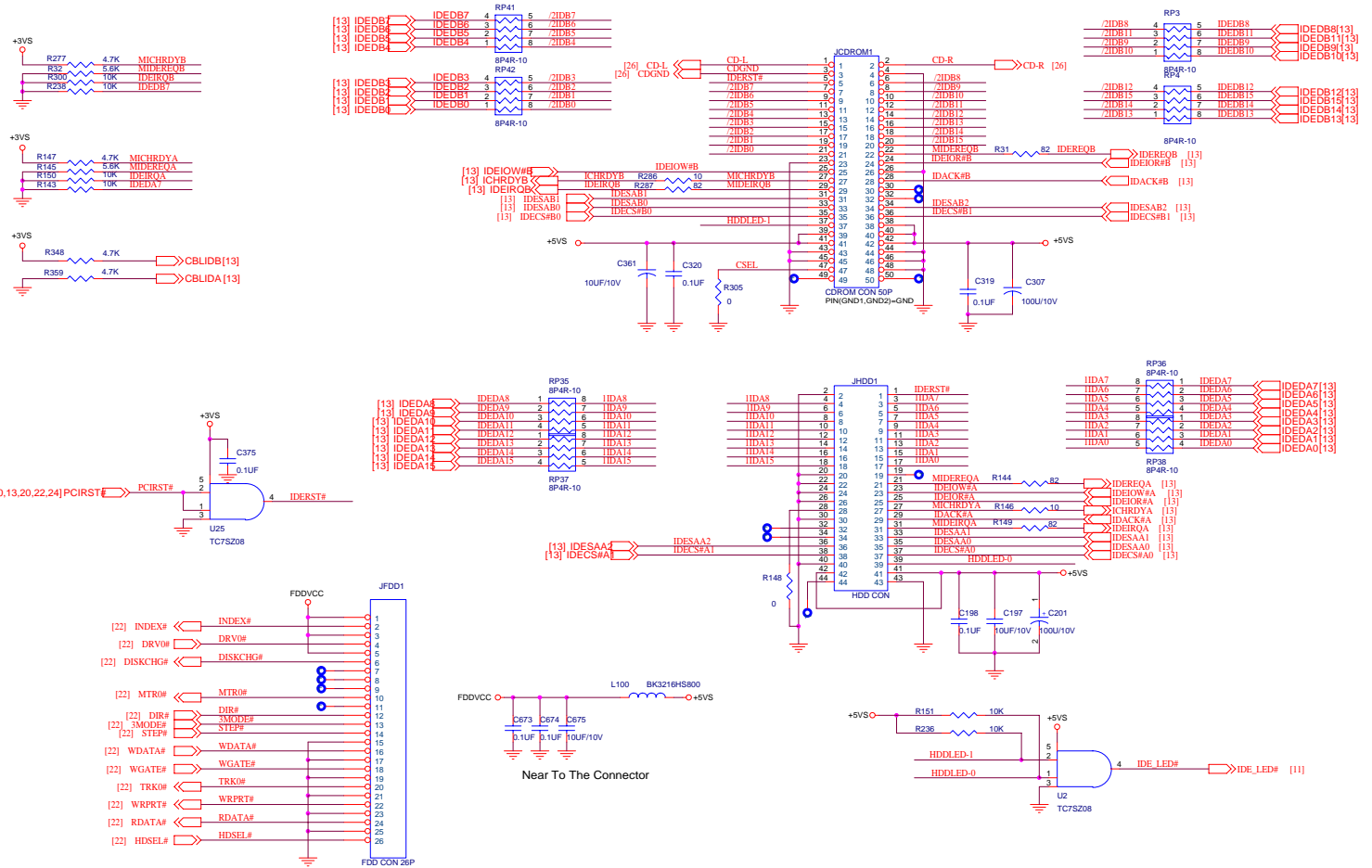
Sheet 16 of 35
962 (Power & RTC)
4 of 4

Schematic Diagrams

HDD/Combo Connector

B.Schematic Diagrams

Sheet 17 of 35
HDD/Combo
Connector

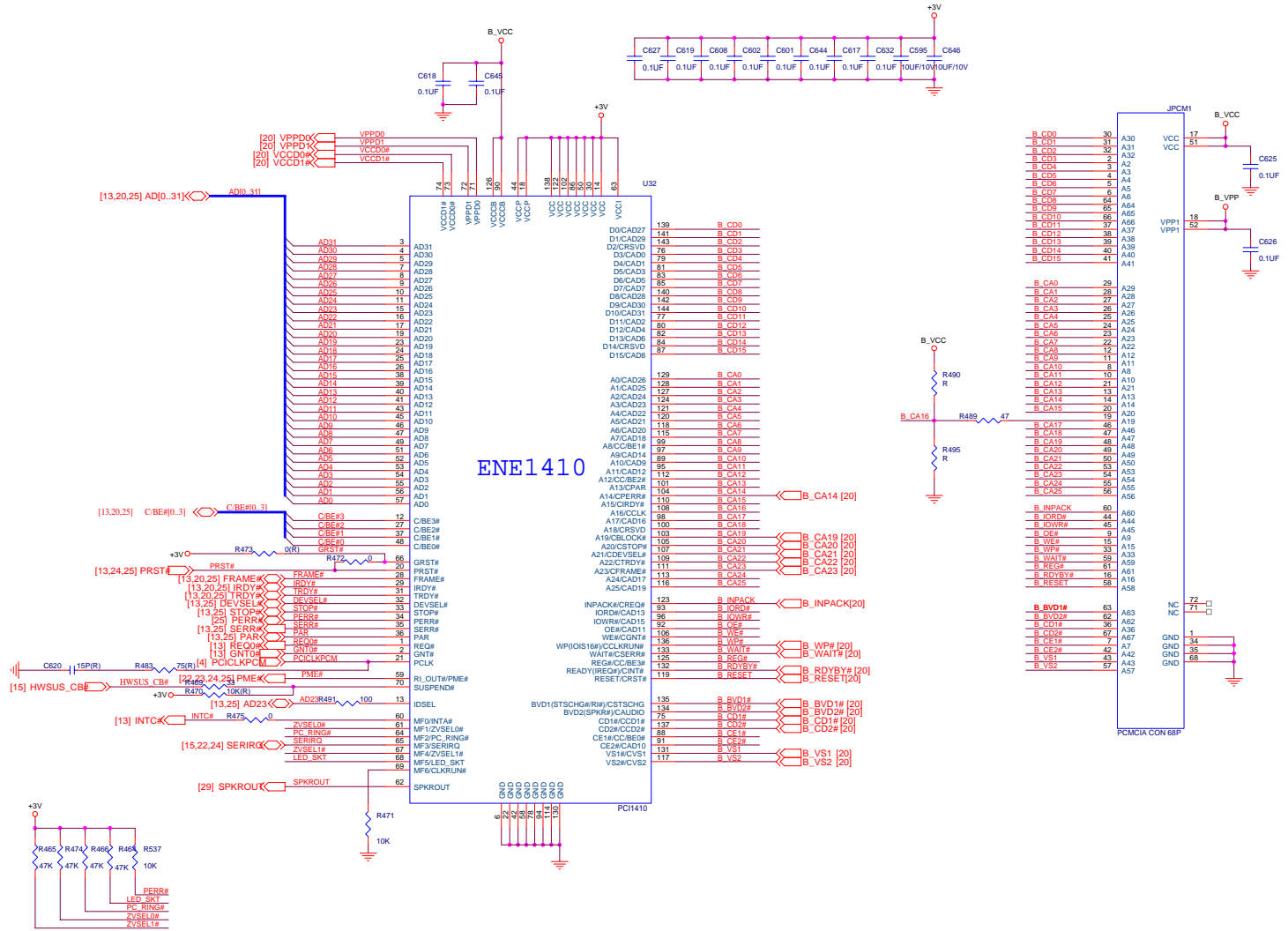


Schematic Diagrams

PCMCIA TI1410

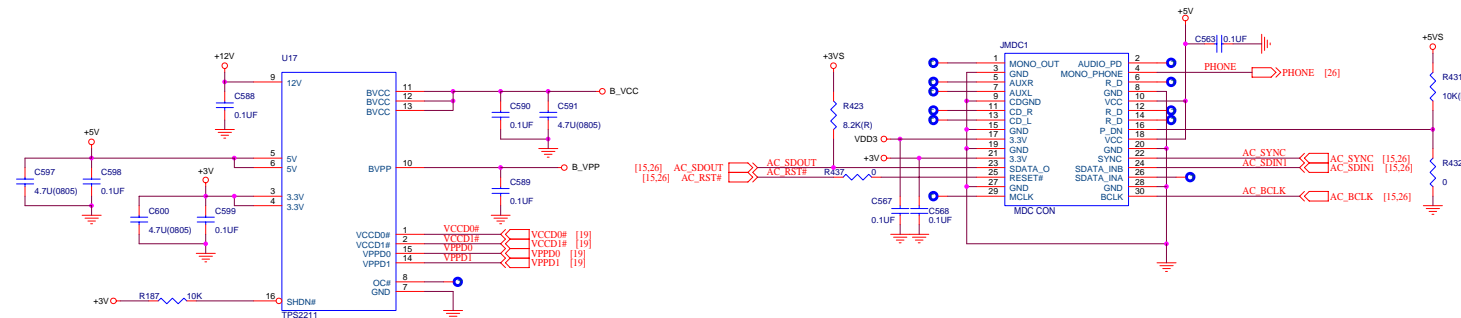
B.Schematic Diagrams

Sheet 19 of 35
PCMCIA TI1410

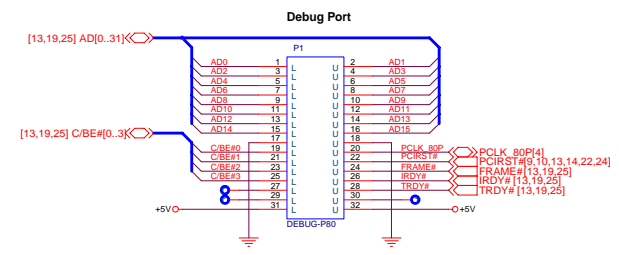
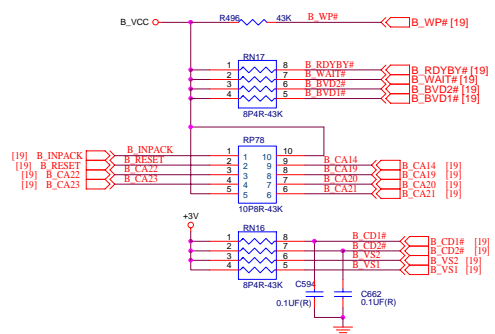


B - 20 PCMCIA TI1410 (71-D4000-D04)

PCMCIA Power



Sheet 20 of 35
PCMCIA Power



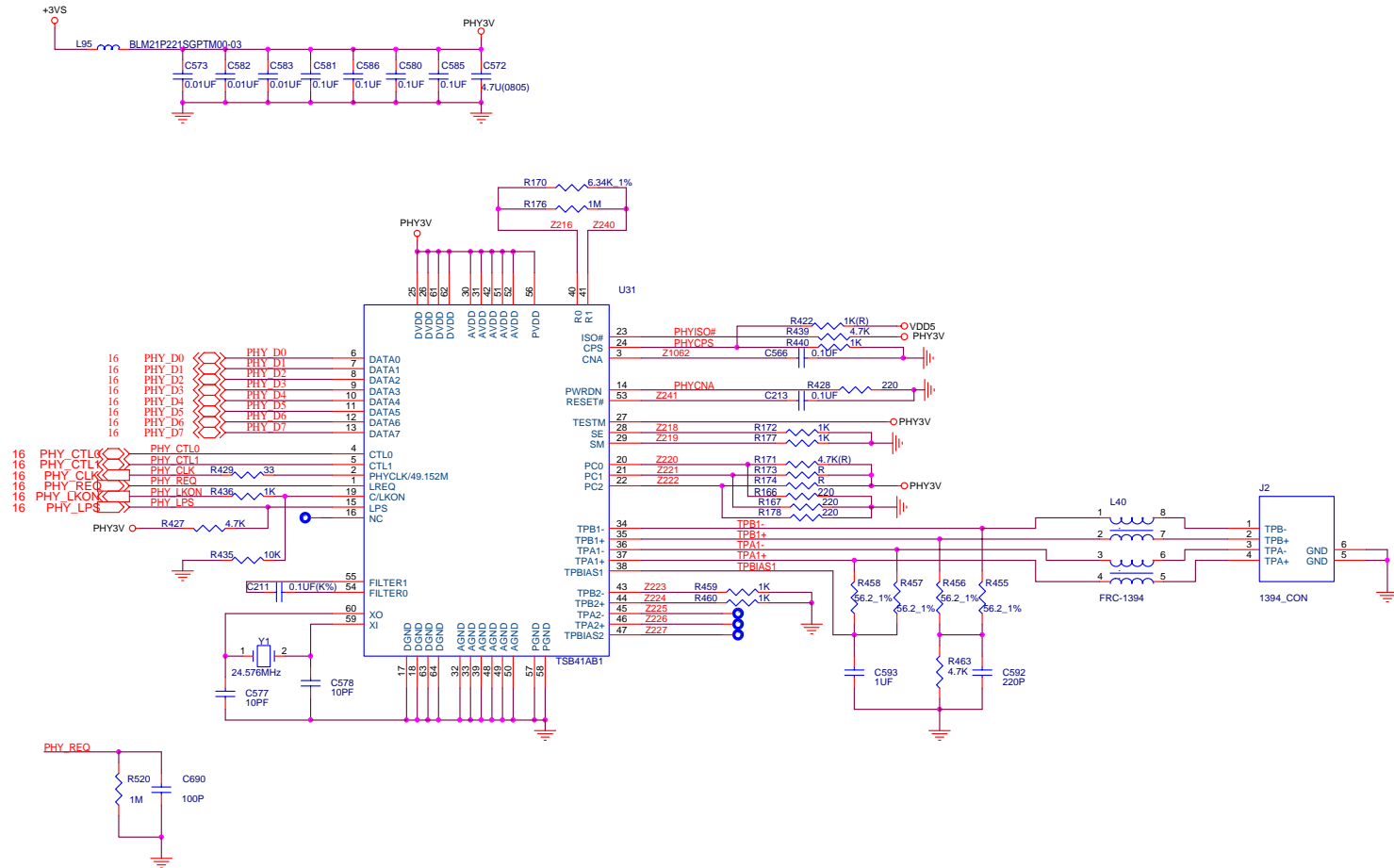
B. Schematic Diagrams

Schematic Diagrams

1394 PHY TSB41LV01

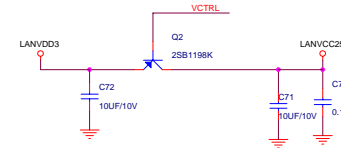
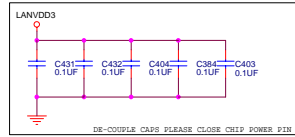
B.Schematic Diagrams

Sheet 21 of 35
1394 PHY
TSB41LV01

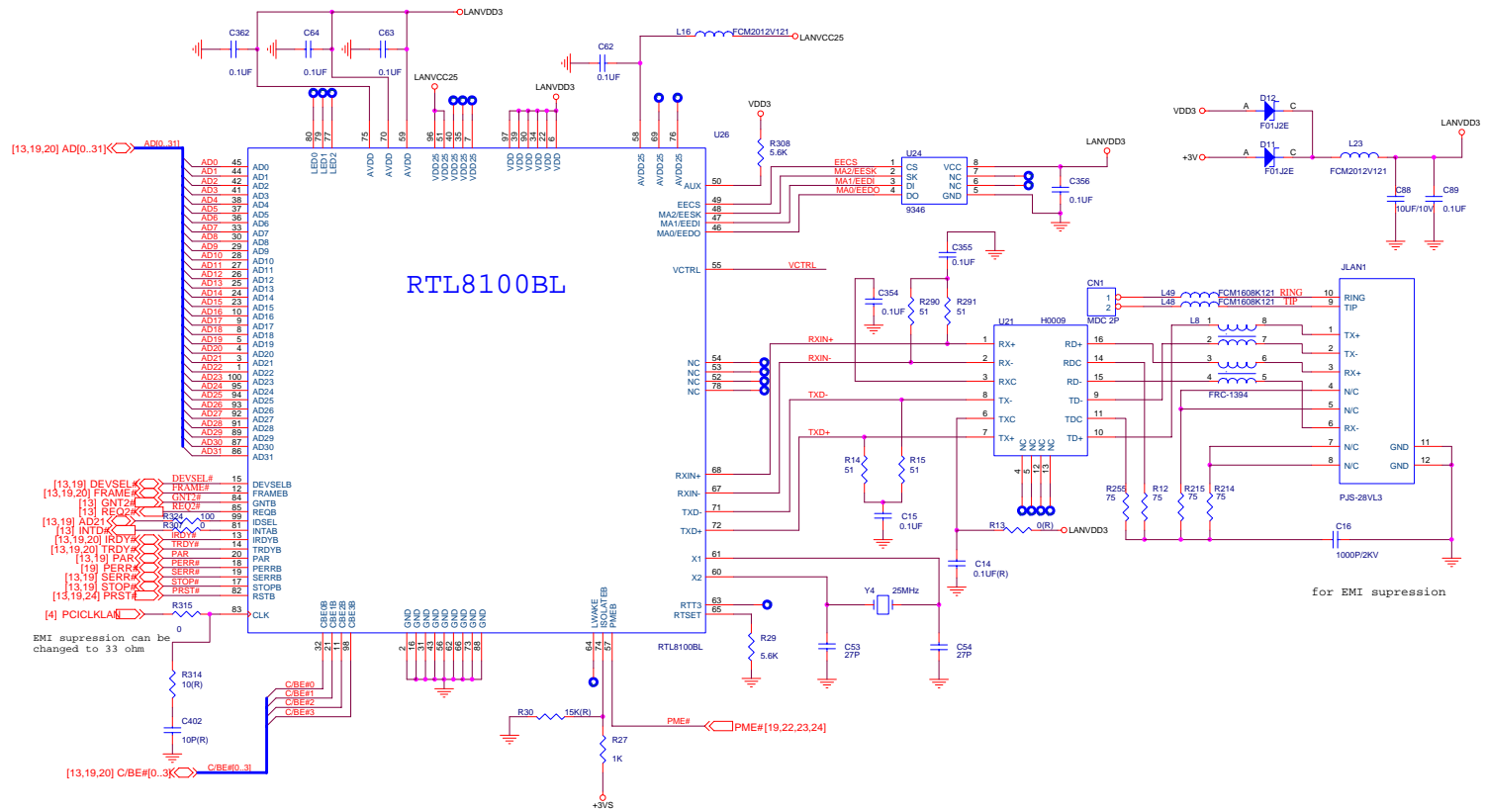


Schematic Diagrams

LAN RTL8100BL

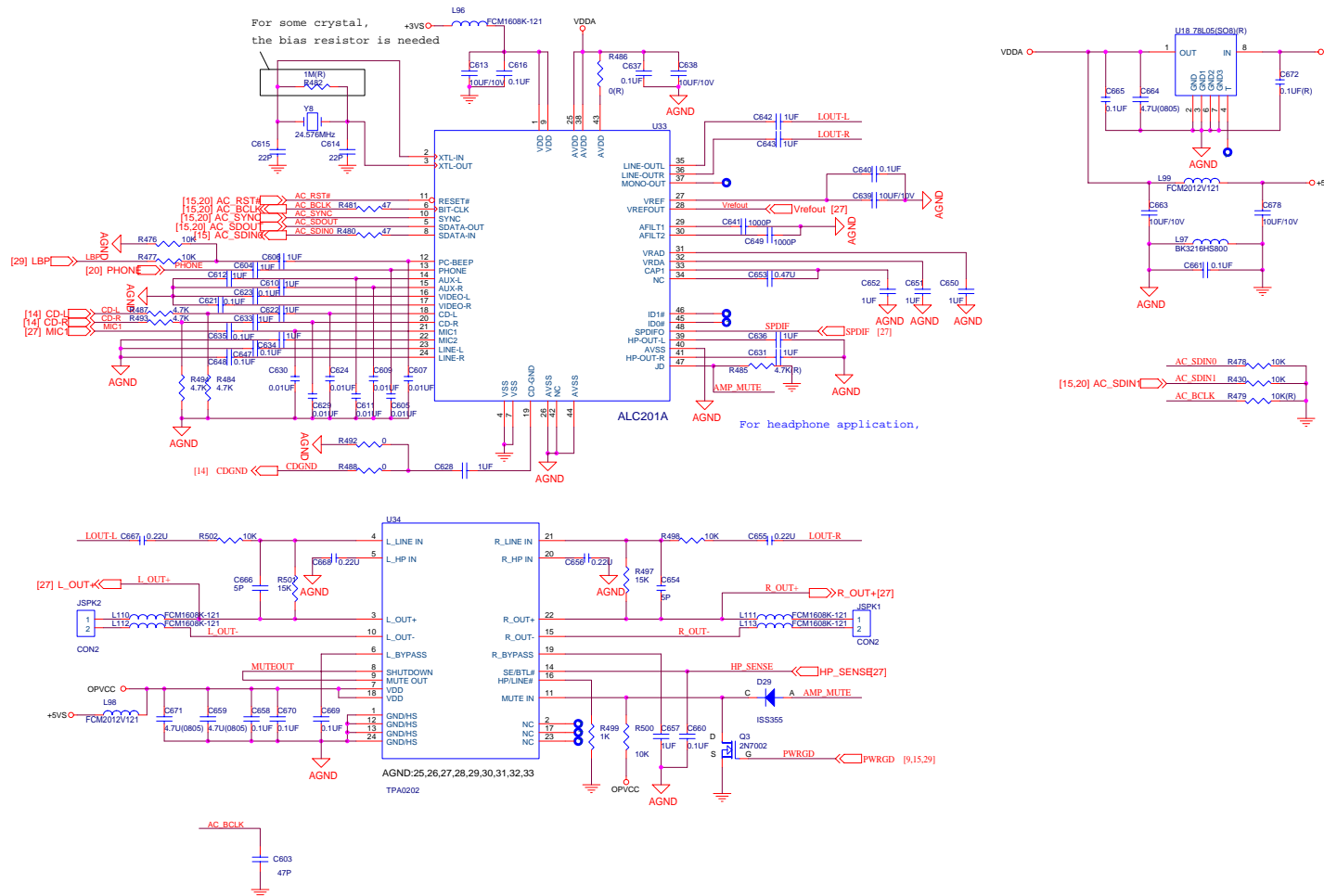


*For RTL8100C application, all bead must be rated 300mA/100ohm@100kHz
The maximum voltage drop when on should be less than 0.3V



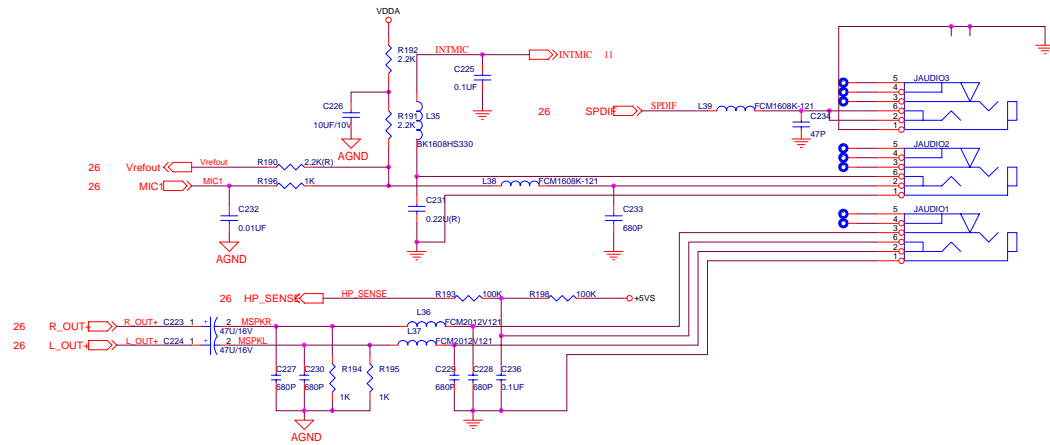
Sheet 25 of 35
LAN RTL8100BL

Audio Codec ALC201A



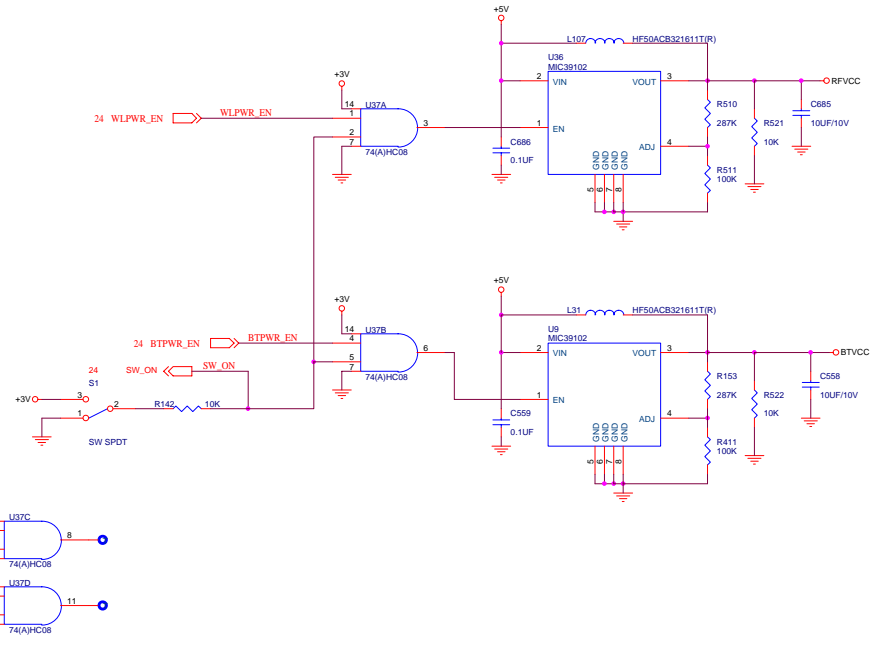
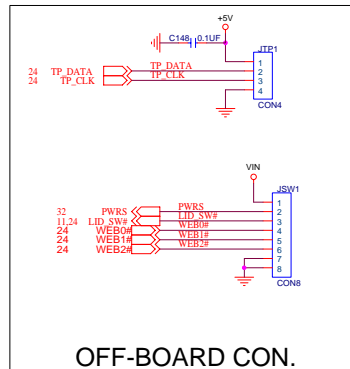
Sheet 26 of 35
Audio Codec
ALC201A

Audio Out & Off Board Connectors



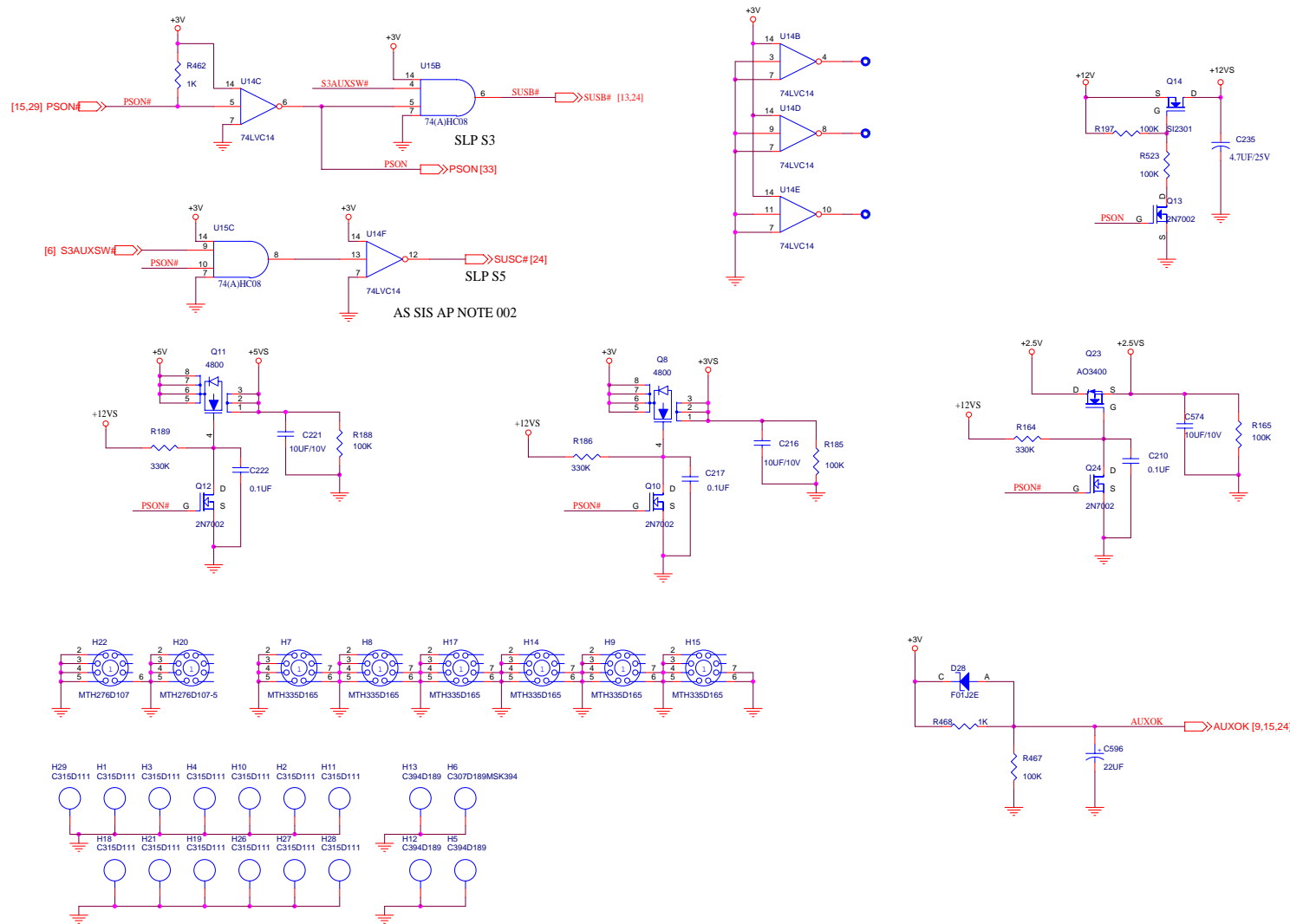
SPIDF OUT
MIC IN
SPEAKER OUT

Sheet 27 of 35
Audio Out & Off
Board Connectors



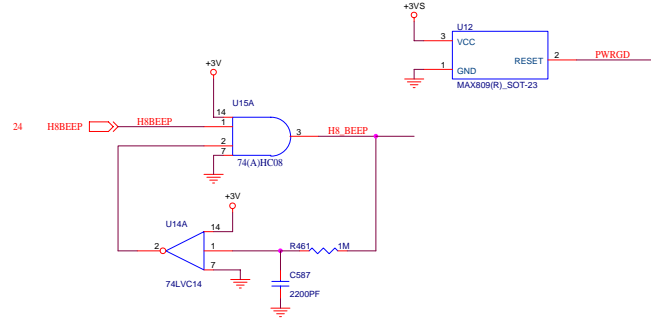
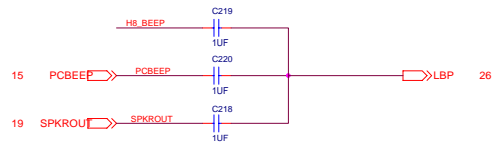
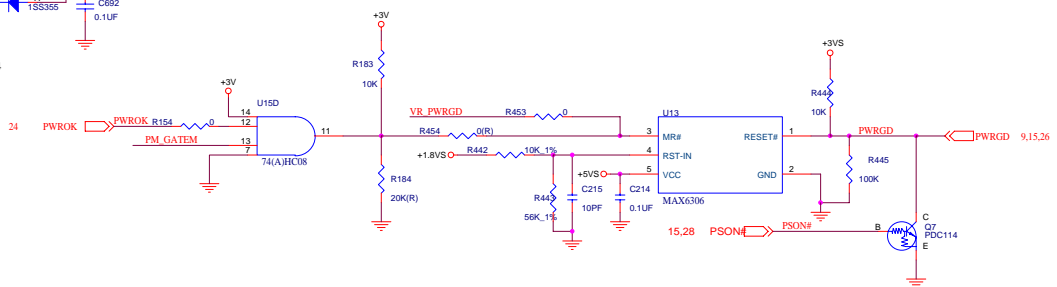
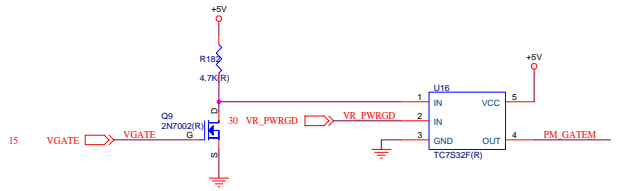
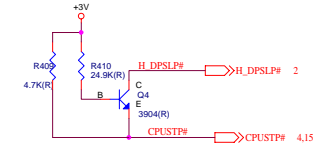
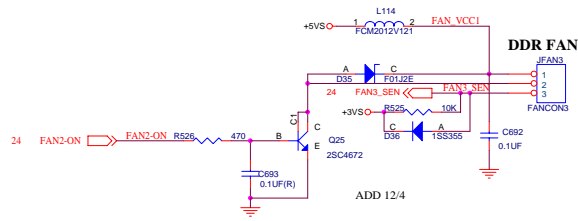
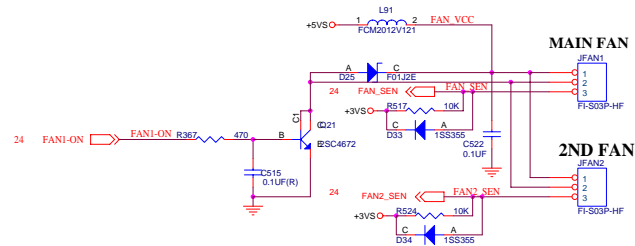
B.Schematic Diagrams

System Power Control



Sheet 28 of 35
System Power
Control

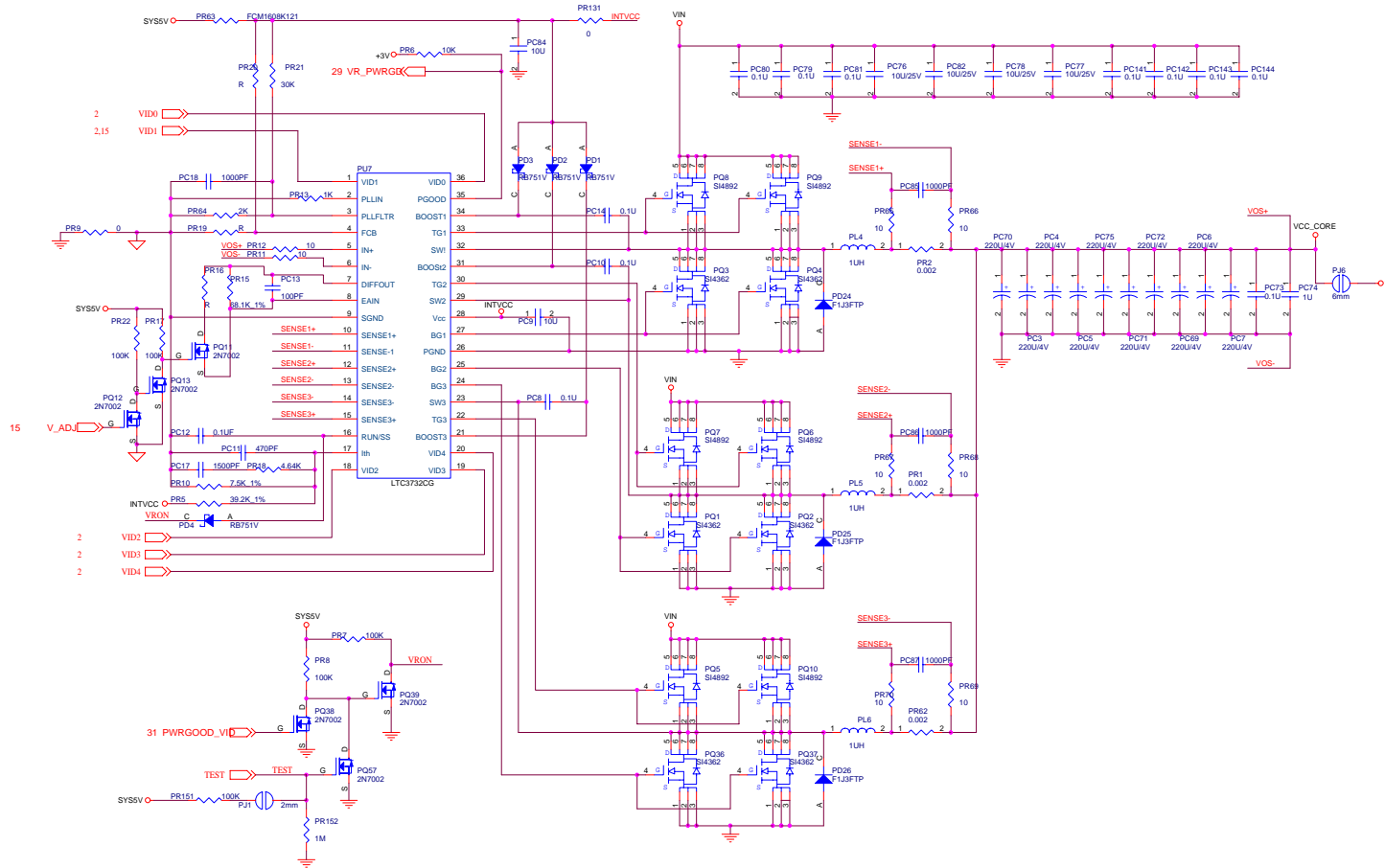
Fan Control and SpeedStep



Sheet 29 of 35
Fan Control &
SpeedStep

B.Schematic Diagrams

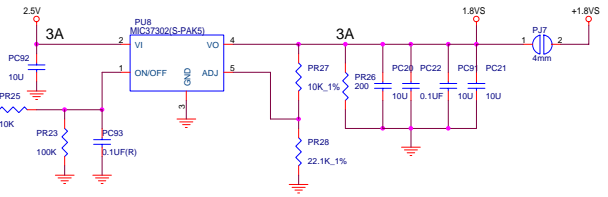
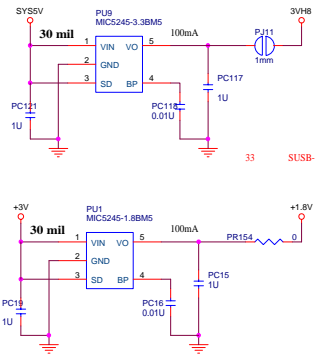
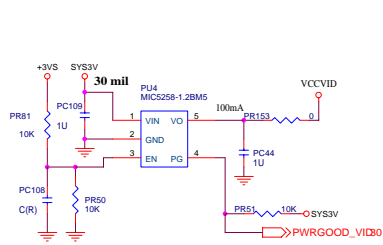
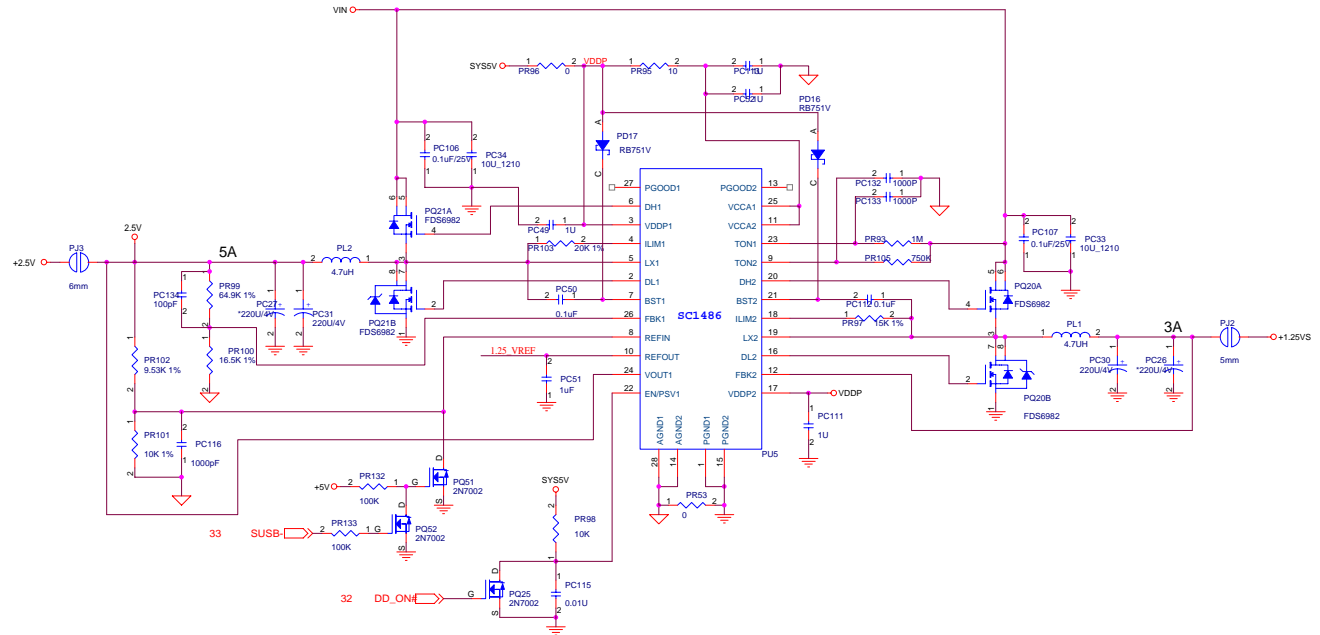
VCORE



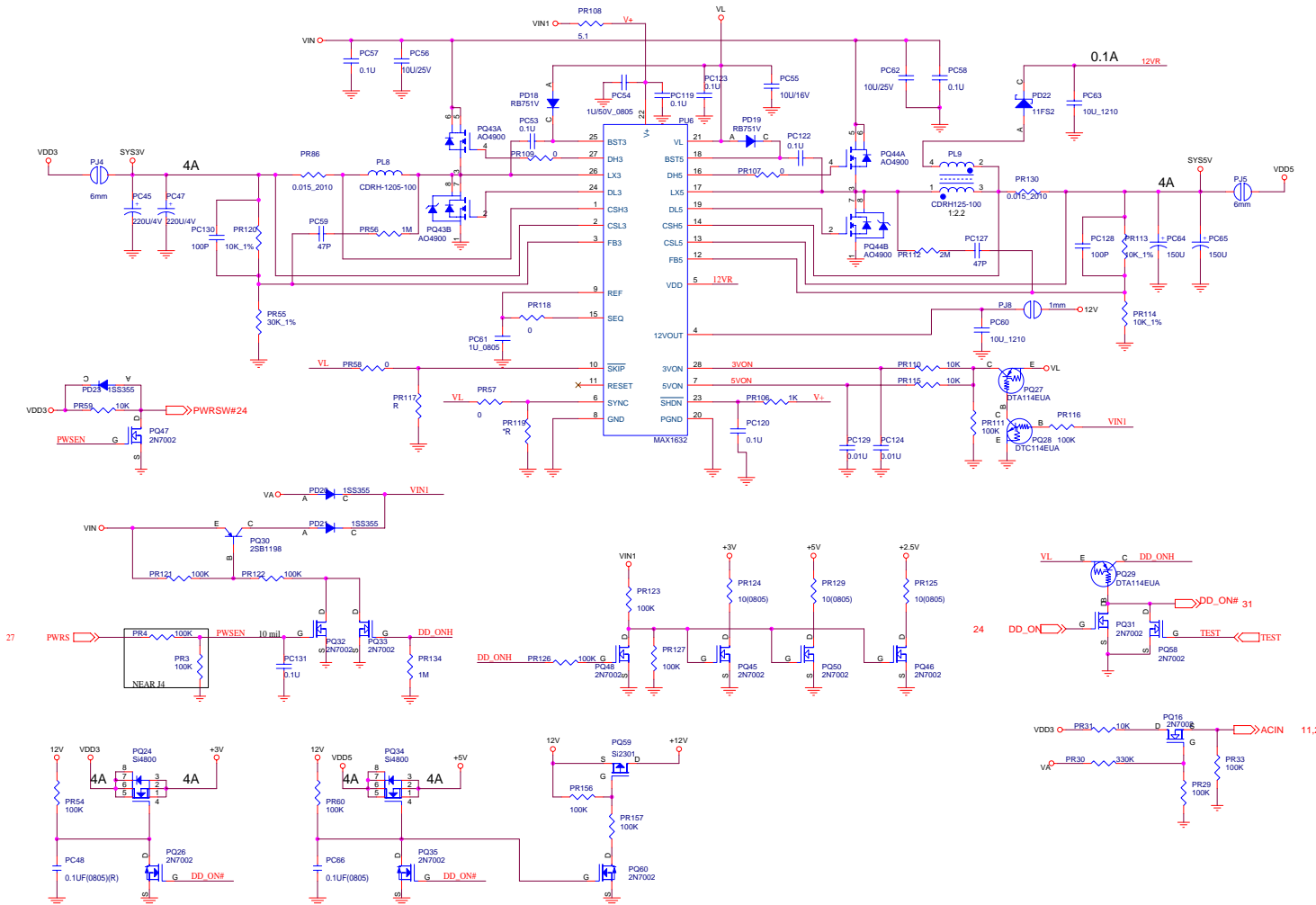
Sheet 30 of 35
VCORE

DDR Power

Sheet 31 of 35
DDR Power



System



Sheet 32 of 35
System

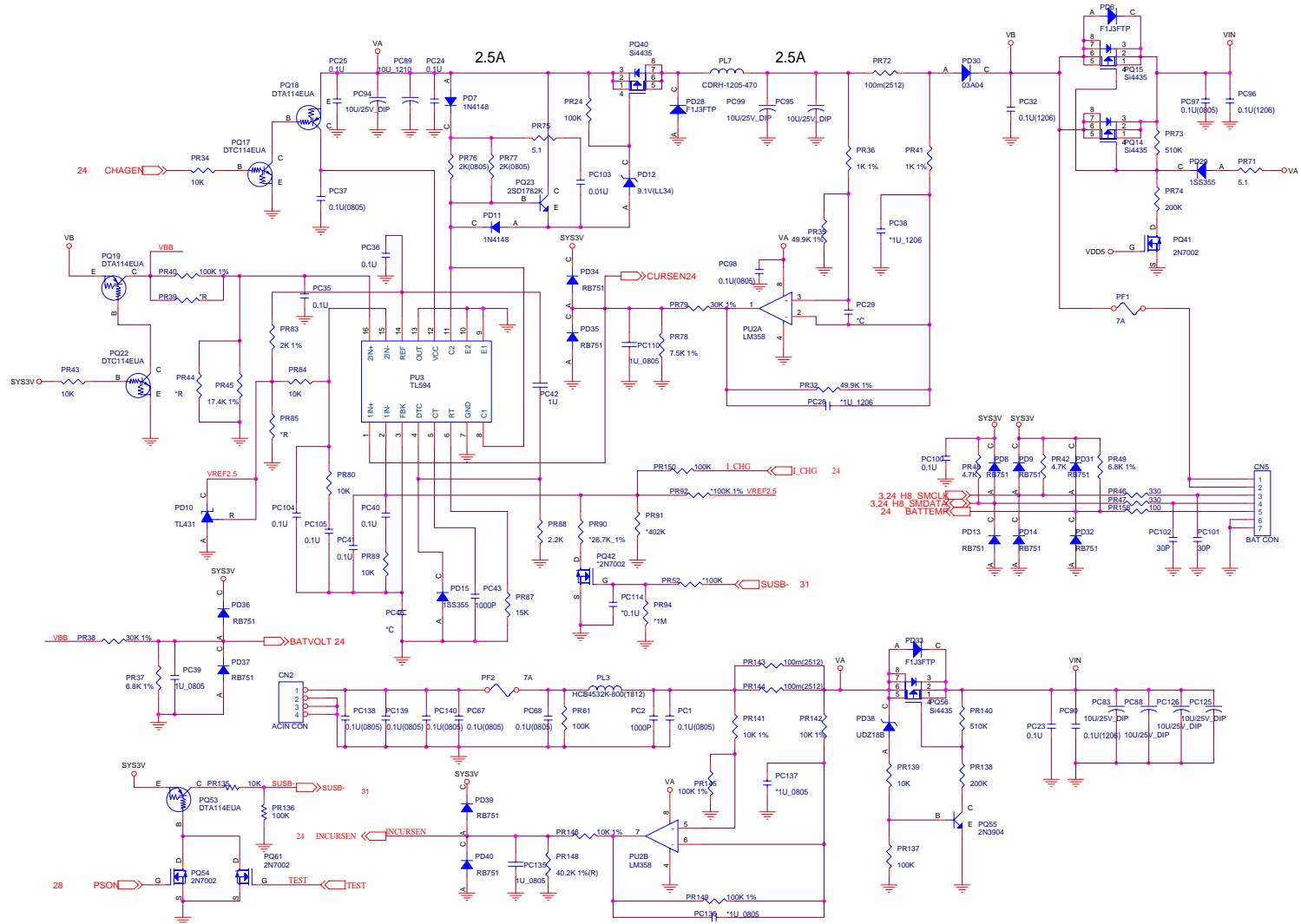
B.Schematic Diagrams

Schematic Diagrams

Charger

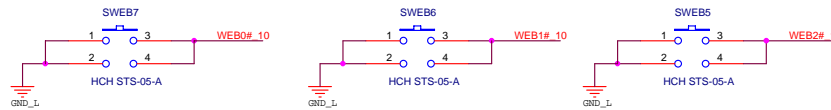
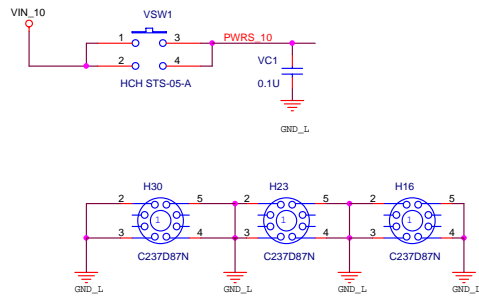
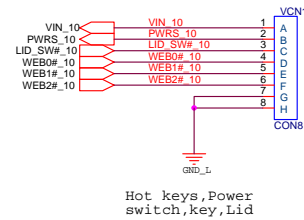
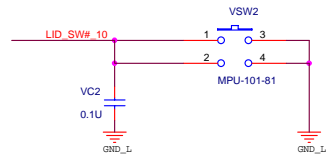
B.Schematic Diagrams

Sheet 33 of 35
Charger



B - 34 Charger (71-D4000-D04)

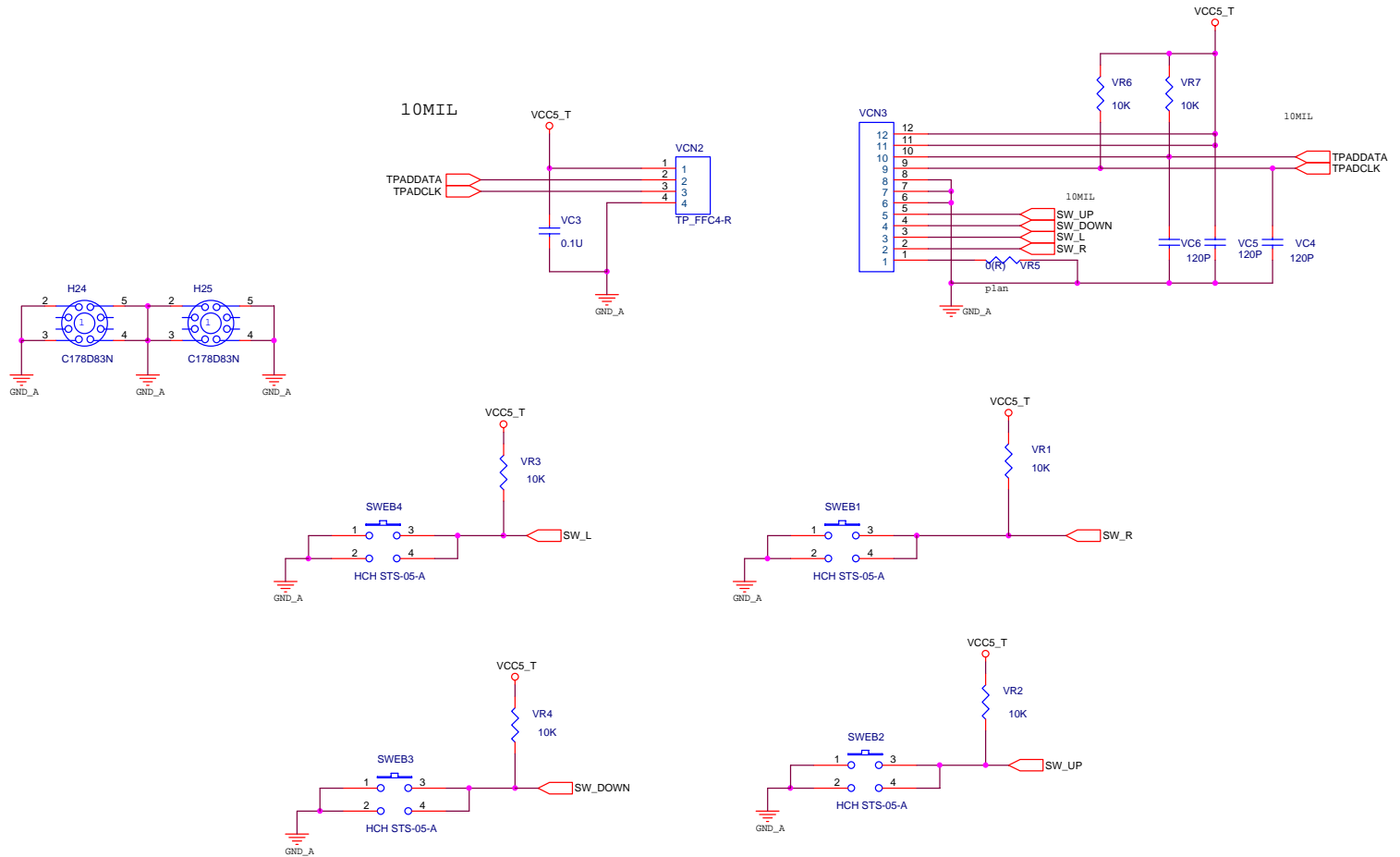
SW Board and HotKey



Sheet 34 of 35
SW Board and
HotKey

TouchPad and Switch Board

Sheet 35 of 35
TouchPad and
Switch Board



Appendix C:Updating the FLASH ROM BIOS

To update the FLASH ROM BIOS you must:

- Download the BIOS update from the web site.
 - Unzip the files onto a bootable Floppy Disk.
 - Reboot your computer from the FDD.
 - Use the flash tools to update the flash BIOS.
 - Restart the computer booting from the HDD.
1. Using your web browser go to www.clevo.com.tw
 2. Choose **Download** from the menu bar at the top of the page.
 3. In the **Driver** section select the model of your computer (**D400S/D410S Series**) and the driver type (**BIOS**).
 4. Select **GO**.
 5. Click on **D4x0Sxxx.zip** to download the BIOS files (including BIOS refresh tools).

Unzip the file you have just downloaded on to a bootable floppy disk.

(The files you should see on this disk are: Phlash.exe, autoexec.bat, Platform.bin, D4x0Sxxx.ROM & Readme.txt)

1. With the bootable floppy disk containing the BIOS files in your floppy drive, restart the computer.
2. The BIOS refresh process will execute automatically.
3. Reboot the computer and enter the BIOS setup.
4. Exit the BIOS and restore the default settings by choosing “Save and Exit”.