F71872F/FG

Super H/W Monitor + LPC IO

Release Date: Dec., 2006
Revision: V0.27P

F71872 Datasheet Revision History

Version	Date	Page	Revision History
0.20P	07/07/2004	-	Preliminary Release Version.
0.21P	07/28/2004	-	Revise PWM Frequency Range
0.22P	10/12/2004	-	Added BEEP/LED_VCC/LED_VSB/FANCTL Functions.
		-	Modified Application Circuit.
0.23P	02/25/2005	-	Added 24MHz Clock Input.
0.24P	04/15/2005	109	Added “Green Package” Ordering Information.
0.25P	08/16/2005	-	Added VID_OTF# Function for Vcore OTF use.
0.26P	09/05/2005	111	Updated Application Circuit.
0.27P	12/28/2006	5	Added Patent Note.

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LIFE SUPPORT APPLICATIONS

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1 General Description

The F71872 is the featured IO chip specifically for PC system. Equipped with one IEEE 1284 parallel port , two UART port and FDC. The F71872 provides SIR and key board controller compatible with PS/2 keyboard and mouse as well, integrated with hardware monitor, supports 11 sets of voltage sensor and 4 voltage fault signal outputs, 3 sets of creative auto-controlling fans and 3 temperature sensor pins for the accurate current type temp. Measurement for CPU thermal diode or external transistors 2N3906.

The F71872 provides flexible features for multi-directional application. For instance, supports CPU VID (Intel CPU On The Fly) controlling and comply with VRM10.0, provides 24 GPIO pins which include pulse/level mode selection, IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature.

Furthermore, the F71872 supports an automatic/dynamic over-voltage function (Vcore change) for application of over-clocking or under clocking. This function provides a pin (VID_OTF#) by external trigger signal to improve the CPU's performance by voltage (Vcore) changing automatically when system is going to run over-clocking or under-clocking. Due to achieve this action, suggest F75133S Loading Gauge can be the part detects system/CPU loading to decide when issues the over-clocking/under-clocking and dynamic signals for system executing. Briefly, user can gain more features on motherboard by these two parts which improve performance and efficiency.

The F71872 is powered by 3.3V voltage, with the LPC interface in the package of 128-QFP.

2 Features

General Functions

- Comply with LPC Spec. 1.0
- Support DPM (Device Power Management), ACPI
- Support CPU VID (Intel CPU On The Fly) controlling and comply with VRM10.0
- Vcore monitoring supports dynamic VID
- Support automatic and dynamic vcore change function for over/under clocking use
- 24 GPIO Pins for flexible application
- 24/48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and under run conditions
- Built-in address mark detection circuit to simplify the read electronics
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

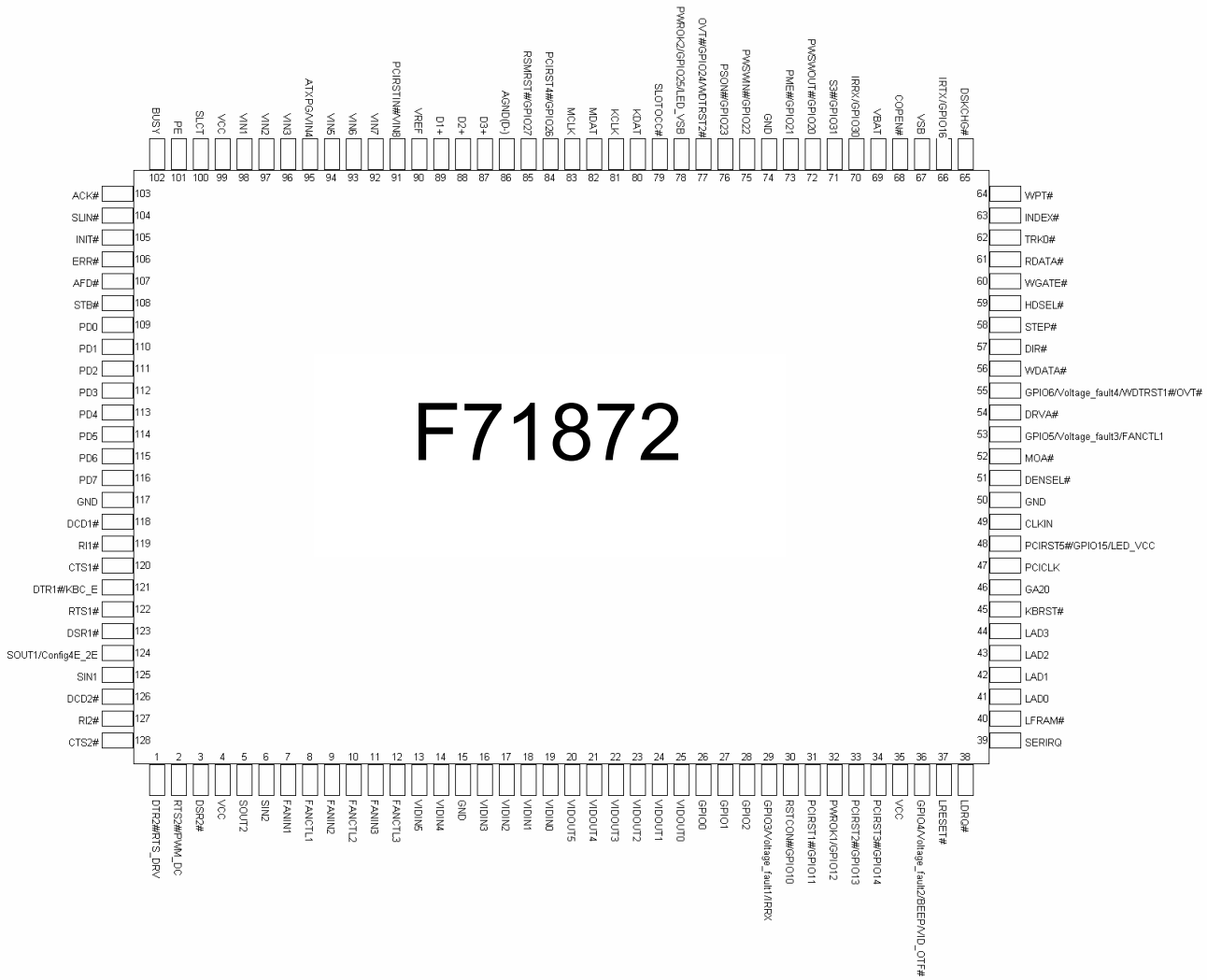
- **UART**
  - Two high-speed 16C550 compatible UART with 16-byte FIFOs
  - Fully programmable serial-interface characteristics
  - Baud rate up to 115.2K
- **Infrared**
  - Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- **Parallel Port**
  - One PS/2 compatible bi-directional parallel port
  - Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
  - Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
  - Enhanced printer port back-drive current protection
- **Keyboard Controller**
  - 8042 based with optional F/W from AMIKKEYTM-2, with 2K bytes of programmable ROM, and 256 bytes of RAM
  - Asynchronous Access to Two Data Registers and One status Register
  - Software compatibility with the 8042
  - Support PS/2 mouse
  - Support both interrupt and polling modes
  - Fast Gate A20 and Hardware Keyboard Reset
  - 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency
- **Hardware Monitor Functions**
  - 12 VID pins for VRM10.0 and CPU VID OTF (On The Fly)
  - 3 current type accurate (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
  - 11 sets voltage monitoring (8 external and 3 internal powers)
  - 4 voltage_fault# hardware signal outputs
  - 3 fan speed monitoring inputs
  - 3 fan speed auto-control (support 3 wire and 4 wire fans)
  - Case intrusion detection circuit
  - WATCHDOG comparison of all monitored values
  - Issue PME# and independent Voltage_fault #
- **Package**
  - 128-pin PQFP

Noted: Patented TW207103 TW207104 US6788131 B1 TW235231 TW237183 TWI263778

3 Key Specifications

Supply Voltage	3.0V to 3.6V
Operating Supply Current	10 mA typ.
Power Down Current (Suspension Mode)	6 mA typ.

4 Pin Configuration



5 Pin Descriptions

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink cap ability.

I/OOD_{12t} - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability.

I/OOD_{16t} - TTL level bi-directional pin, can select to OD or OUT by register, with 16 mA source-sink

capability.

I/OD_{12t} - TTL level bi-directional pin, Open-drain outpu with 12 mA sink capability.

I/OD_{12ts5V} - TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.

I/O_{12ts5V} - TTL level bi-directional pin and schmitt trigger with 12 mA sink capability, 5V tolerance.

$I/OD_{16t,5V}$ - TTL level bi-directional pin, Open-drain outpu with 16 mA sink capability, 5V tolerance.

$I/O_{8t\text{-}u47,5V}$ - TTL level bi-directional pin with 8 mA sink capability, pull-up 47k ohms, 5V tolerance.

O_{12} - Output pin with 12 mA source-sink capability.

AOUT - Output pin(Analog).

OD_{12} - Open-drain output pin with 12 mA sink capability.

$OD_{16\text{-}u10,5V}$ - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.

OD_{24} - Open-drain output pin with 24 mA sink capability.

IN_{t5V} - TTL level input pin,5V tolerance.

IN_{ts} - TTL level input pin and schmitt trigger.

IN_{ts5V} - TTL level input pin and schmitt trigger, 5V tolerance.

AIN - Input pin(Analog).

P - Power.

5.1 Power Pin

Pin No.	Pin Name	Type	Description
4,35,99	VCC	P	Power supply voltage input with 3.3V
67	VSB	P	Stand-by power supply voltage input 3.3V
69	VBAT	P	Battery voltage input
86	AGND(D-)	P	Analog GND
15,50,74, 117	GND	P	Digital GND

5.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
37	LRESET#	IN_{ts}	VCC	Reset signal. It can connect to PCIRST# signal on the host.
38	LDRQ#	O_{12}	VCC	Encoded DMA Request signal.
39	SERIRQ	I/O_{12t}	VCC	Serial IRQ input/Output.
40	LFRAM#	IN_{ts}	VCC	Indicates start of a new cycle or termination of a broken cycle.
41-44	LAD[3:0]	I/O_{12t}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
47	PCICLK	IN_{ts}	VCC	33MHz PCI clock input.
49	CLKIN	IN_{ts}	VCC	System clock input. According to the input frequency 24/48MHz.

5.3 FDC

Pin No.	Pin Name	Type	PWR	Description
51	DENSEL#	OD_{24}	VCC	Drive Density Select. Set to 1 - High data rate.(500Kbps, 1Mbps) Set to 0 – Low data rate. (250Kbps, 300Kbps)
52	MOA#	OD_{24}	VCC	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
54	DRVA#	OD_{24}	VCC	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
56	WDATA#	OD_{24}	VCC	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
57	DIR#	OD_{24}	VCC	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
58	STEP#	OD_{24}	VCC	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
59	HDSEL#	OD_{24}	VCC	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
60	WGATE#	OD_{24}	VCC	Write enable. An open drain output.
61	RDATA#	IN_{ts5V}	VCC	The read data input signal from the FDD.
62	TRK0#	IN_{ts5V}	VCC	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
63	INDEX#	IN_{ts5V}	VCC	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
64	WPT#	IN_{ts5V}	VCC	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
65	DSKCHG#	IN_{ts5V}	VCC	Diskette change. This signal is active low at power on and whenever the diskette is removed.

5.4 UART Port and SIR

Pin No.	Pin Name	Type	PWR	Description
66	IRTX/GPIO16	O_{12}	VCC	Infrared Transmitter Output.
		I/O_{12t}		General Purpose IO
70	IRRX/GPIO30	IN_{ts}	VSB	Infrared Receiver input.
		I/OOD_{12t}		General Purpose IO. Open drain and drive select by register.
118	DCD1#	IN_{t5V}	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
119	RI1#	IN_{t5V}	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
120	CTS1#	IN_{t5V}	VCC	Clear To Send is the modem control input.

121	DTR1#/ KBC_EN	$I/O_{8t-u47,5V}$	VCC	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping. Power on strapping : 1 (Default) KBC Enable 0 KBC Disable
122	RTS1#	$I/O_{8t-u47,5V}$	VCC	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
123	DSR1#	IN_{t5V}	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
124	SOUT1/ Config4E_2E	$I/O_{8t-u47,5V}$	VCC	UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping. Power on strapping : 1 (Default) Configuration register:4E 0 Configuration register:2E
125	SIN1	IN_{t5V}	VCC	Serial Input. Used to receive serial data through the communication link.
126	DCD2#	IN_{t5V}	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
127	RI2#	IN_{t5V}	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
128	CTS2#	IN_{t5V}	VCC	Clear To Send is the modem control input.
1	DTR2# / RST_DRV	$I/O_{8t-u47,5V}$	VCC	UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping. Power on strapping : 1 (Default) : pin31/33/34/48/84 OD 0 Drive
2	RTS2#/PWM_DC	$I/O_{8t-u47,5V}$	VCC	UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping. Power on strapping : 1 (Default) PWM Mode 0 Drive Linear Mode
3	DSR2#	IN_{t5V}	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
5	SOUT2	$I/O_{8t-u47,5V}$	VCC	UART 2 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
6	SIN2	IN_{t5V}	VCC	Serial Input. Used to receive serial data through the communication link.

5.5 KBC I/F

Pin No.	Pin Name	Type	PWR	Description
45	KBRST#	$OD_{16-u10,5V}$	VCC	Keyboard reset. This pin is high after system reset. Internal

				pull high 3.3V with 10k ohms. (KBC P20)
46	GA20	$OD_{16\text{-}u10,5V}$	VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
80	KDAT	$I/OD_{16t,5V}$	VSB	Keyboard Data.
81	KCLK	$I/OD_{16t,5V}$	VSB	Keyboard Clock.
82	MDAT	$I/OD_{16t,5V}$	VSB	PS2 Mouse Data.
83	MCLK	$I/OD_{16t,5V}$	VSB	PS2 Mouse Clock.

5.6 IEEE 1284 Parallel Port

Pin No.	Pin Name	Type	PWR	Description
100	SLCT	IN_{ts5V}	VCC	An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
101	PE	IN_{ts5V}	VCC	An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
102	BUSY	IN_{ts5V}	VCC	An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
103	ACK#	IN_{ts5V}	VCC	An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
104	SLIN#	I/OD_{12ts5V}	VCC	Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
105	INIT#	I/OD_{12ts5V}	VCC	Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
106	ERR#	IN_{ts5V}	VCC	An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
107	AFD#	I/OD_{12ts5V}	VCC	An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
108	STB#	I/OD_{12ts5V}	VCC	An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
109	PD0	I/O_{12ts5V}	VCC	Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
110	PD1	I/O_{12ts5V}	VCC	Parallel port data bus bit 1.
111	PD2	I/O_{12ts5V}	VCC	Parallel port data bus bit 2.
112	PD3	I/O_{12ts5V}	VCC	Parallel port data bus bit 3.
113	PD4	I/O_{12ts5V}	VCC	Parallel port data bus bit 4.
114	PD5	I/O_{12ts5V}	VCC	Parallel port data bus bit 5.

115	PD6	I/O_{12ts5V}	VCC	Parallel port data bus bit 6.
116	PD7	I/O_{12ts5V}	VCC	Parallel port data bus bit 7.

5.7 H/W Monitor

Pin No.	Pin Name	Type	PWR	Description
95	ATXPG/VIN4	AIN	VCC	ATX Power Good. Voltage Input 4.
91	PCIRSTIN#/VIN8	AIN	VCC	PCI Reset # signal input. Voltage Input 8.
92-94,	VIN7~VIN5	AIN	VCC	Voltage Input 7 ~ 5.
96-98	VIN3~VIN1	AIN	VCC	Voltage Input 3 ~ 1.
7	FANIN1	IN_{ts}	VCC	Fan 1 tachometer input.
8	FANCTL1	O_{12}	VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output.
9	FANIN2	IN_{ts}	VCC	Fan 2 tachometer input.
10	FANCTL2	O_{12}	VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output.
11	FANIN3	IN_{ts}	VCC	Fan 3 speed input.
12	FANCTL3	O_{12}	VCC	Fan 3 control output. This pin provides PWM duty-cycle output or a voltage output.
87	D3+	AIN	VCC	CPU thermal diode/transistor temperature sensor input.
88	D2+	AIN	VCC	CPU thermal diode/transistor temperature sensor input.
89	D1+	AIN	VCC	CPU thermal diode/transistor temperature sensor input.
90	VREF	AOUT	VCC	Voltage sensor output.
73	PME#/GPIO21	OD_{12} I/OD_{12t}	VSB	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state. General Purpose IO.
26	GPIO0	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce.
27	GPIO1	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce.
28	GPIO2	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce.
29	GPIO3/ Voltage_Fault1#/ IRRX	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce. Voltage fault indication for VIN1 abnormal event. Infrared Receiver input. (Powered by Vcc)

36	GPIO4/ Voltage_Fault2#/ BEEP/ VID_OTF#	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce. Voltage fault indication for VIN2 abnormal event. Beep Pin. Voltage OTF Enable pin. This Pin can be selected to be a input pin for VID_OTF enable.
53	GPIO5/ Voltage_Fault3#/ FANCTL	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce. Voltage fault indication for VIN3 abnormal event. Fan 1 control output for Intel 4-pin Fan. All the registers are as same as FANCTL1.
55	GPIO6/ Voltage_Fault4#/ WDTRST1#/ OVT#	I/OOD_{12t}	VCC	General purpose IO. 1. Support Level and Pulse mode output. 2. Open drain and drive select 3. Without input de-bounce. Voltage fault indication for VIN4 abnormal event. Watch dog timer signal output 1. Over temperature signal output.
77	OVT#/ GPIO24/ WDTRST2#	I/OOD_{12t}	VSB	Over temperature signal output.(Default 85°C) General purpose IO. Open drain and drive select by register. Watch dog timer signal output 2.

5.8 ACPI function pins

Pin No.	Pin Name	Type	PWR	Description
30	RSTCON#/GPIO10	I/OD_{12t}	VCC	RESET connect# with 50ms debouce function, it connects to reset button, and also other reset source on the motherboard. If the register RSTCON_EN (5h) is set to 1, the pin 30 will infect PCIRST1# ~ PCIRST5# outcome. If the register RSTCON_EN is set to 0, the pin 30 will infect PWROK1 and PWROK2 outcome. General purpose IO.
31	PCIRST1#/GPIO11	I/OOD_{16t}	VCC	It is a output buffer of RSTCON# and LRESET#. General purpose IO. Pin1 RST_DRV = 1(high) : OD = 0(low) : Drive
32	PWROK1/GPIO12	I/OD_{12t}	VCC	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V. General purpose IO.
33	PCIRST2#/GPIO13	I/OOD_{16t}	VCC	It is a output buffer of RSTCON# and LRESET#. General purpose IO. Pin1 RST_DRV = 1(high) : OD =0(low): Drive
34	PCIRST3#/GPIO14	I/OOD_{16t}	VCC	It is a output buffer of RSTCON# and LRESET#. General purpose IO.

				Pin1 RST_DRV = 1(high) : OD =0(low) : Drive
48	PCIRST5#/GPIO15 LED_VCC	I/OOD_{16t}	VCC	It is a output buffer of RSTCON#,LRESET# and PCIRSTIN. General purpose IO. Pin1 RST_DRV = 1(high) : OD =0(low) : Drive Power LED for VCC.
68	COPEN#	IN_t	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.
71	S3#/GPIO31	IN_t I/OD_{12t}	VSB	S3# Input is Main power on-off switch input. General purpose IO.
72	PWSWOUT# /GPIO20	OD_{12} I/OD_{12t}	VSB	Panel Switch Output. This pin is low active and pulse output. It is power on request output#. General purpose IO.
75	PWSWIN# /GPIO22	IN_t I/OD_{12t}	VSB	Main power switch button input. General purpose IO.
76	PSON#/GPIO23	OD_{12} I/OD_{12t}	VSB	Power supply on-off control output. Connect to ATX power supply PS_ON# signal. General purpose IO.
78	PWROK2/GPIO25/ LED_VSB	I/OD_{12t}	VSB	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V. General purpose IO. Power LED for VSB
84	PCIRST4#/GPIO26	I/OOD_{16t}	VSB	It is a output buffer of RSTCON#,LRESET# and PCIRSTIN. General purpose IO. Pin1 RST_DRV = 1(high) : OD =0(low) : Drive
85	RSMRST#/GPIO27	I/OD_{12t}	VSB	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.3V. General purpose IO.

5.9 VID controlling pins

Pin No.	Pin Name	Type	PWR	Description
13,14, 16,17, 18,19	VIDIN[5:0]	IN_{ts}	VCC	CPU VID input pins. 1. Special level input VIH→ 0.9, VIL → 0.6. 2. Power by VCC.
20-25	VIDOUT[5:0]	OD_{12}	VCC	CPU VID output pins.
79	SLOTOCC#	IN_{ts}	VSB	CPU SLOTOCC# input.

6 Function Description

6.1 Power on Strapping Options

The F71872 provides four pins for power on hardware strapping to select functions. There is a form to describe how to set the functions you want.

Pin No.	Symbol	Value	Description
1	RST_DRV	1	Pin31/33/34/48/84 will be defined a Open Drain pin. (Default)
		0	Pin31/33/34/48/84 will be defined a Drive pin.
2	PWM_DC	1	Fan control mode: PWM mode. (Default)
		0	Fan control mode: Linear mode.
121	KBC_EN	1	KBC is enabled. (Default)
		0	KBC is disabled.
124	Config4E_2E	1	Chip selection in configuration 4E. (Default)
		0	Chip selection in configuration 2E.

6.2 ACPI

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

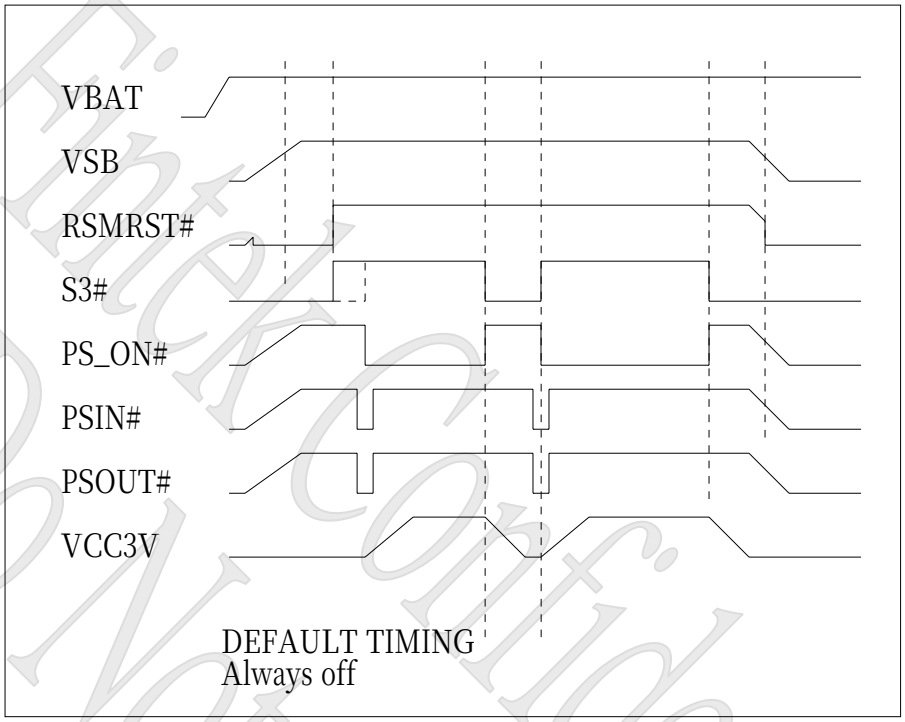
There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

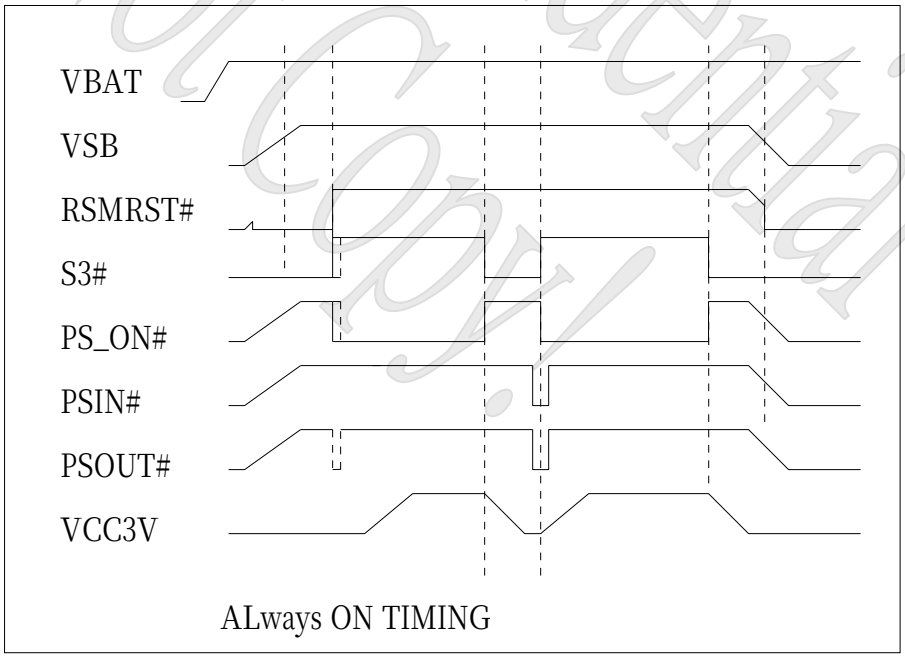
It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.





6.3 PCI Reset and PWROK Signals

The F71872 supports 5 output buffers for 5 reset signals. If the register RSTCON_EN (5h) is set to 1, the pin RSTCON# will infect PCIRST1# ~ PCIRST5# outcome. Then, the result of PCIRST# outcome will be affected by conditions as below:

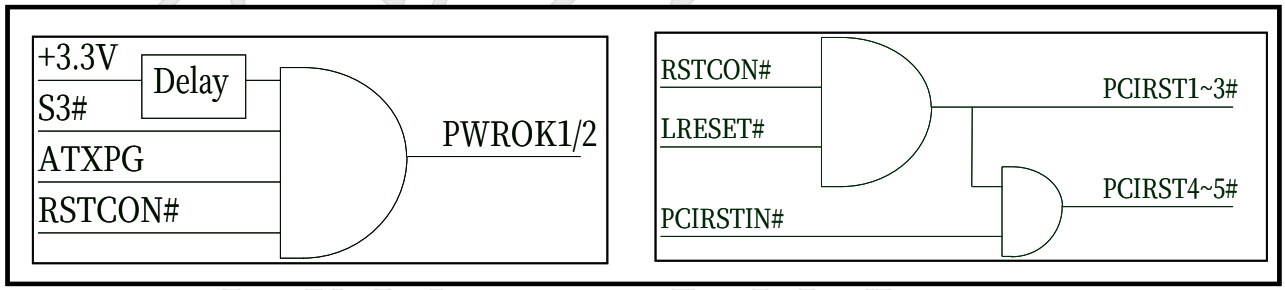
PCIRST1# → Output buffer of RSTCON# and LRESET#.

PCIRST2# → Output buffer of RSTCON# and LRESET#.

PCIRST3# → Output buffer of RSTCON# and LRESET#.

PCIRST4# → Output buffer of RSTCON#, LRESET# and PCIRSTIN#

PCIRST5# → Output buffer of RSTCON#, LRESET# and PCIRSTIN#



So far as the PWROK issue is as above figure. PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register. (100ms ~ 400ms)

In the figure, the RSTCON# will be implemented by register RSTCON_EN. If RSTCON_EN be set to 0, the RSTCON# pin will affect PWROK outputs. If RSTCON_EN be set to 1, the RSTCON# pin will affect PCIRST outputs (Default).

6.4 Hardware Monitor

6.4.1 Analog Input

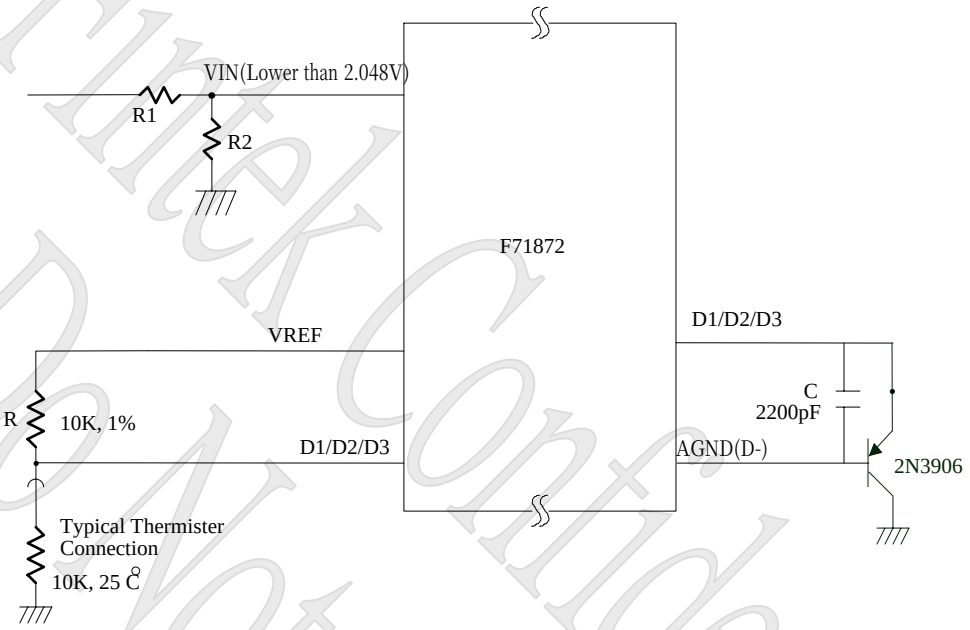
The F71872 provides 8 pins (8-bit) ADC voltage inputs. These input voltages should be positive and is limited at range of 0v to 2.048V. The minimum resolution (1-LSB) is 8mV. If the voltage is over this range, the divider resistor must be added and the divided voltage is also in the range of 0V to 2.048V.

The maximum input voltage of the analog pin is 2.048V because the 8-bit ADC has a 8mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The voltage range of 0V to 2.048V can be connected to these analog inputs. The 3.3V and VSB5V should be reduced a factor with external resistors so as to obtain the input range..

There are 8 voltage inputs in the F71872 and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ For instance, where V_{+12V} is the analog input voltage.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.



6.4.2 Temperature Monitoring and Offset

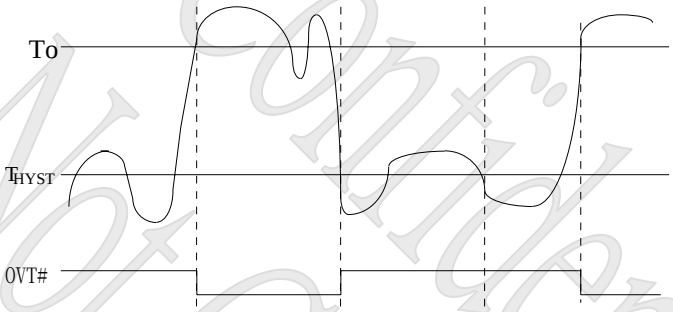
The F71872 can be measured from 0°C to 140°C. The status depends on different situation. As connected to a BJT thermal diode, detected temperature ranges from 0°C to 140°C without considering the OFFSET effect. As connected to a thermistor, detected temperature ranges from 0°C to 127°C without considering the OFFSET effect. The temperature format is as the following table:

Temperature (High Byte)	Digital Output
0°C	0000 0000
1°C	0000 0001
25°C	0001 1001
50°C	0011 0010
75°C	0100 1011
90°C	0101 1010
100°C	0110 0100
140°C	1000 1100

The F71872 provides offset register for each temperature. The offset value is an 7-bit, 2's complement value. The reading temperature value will be the result of the offset value added to the monitored value. The offset format is as the following table:

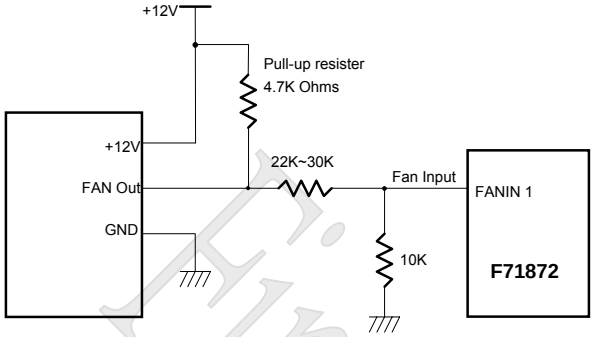
Offset Value	High Byte
63°C	0011 1111
2°C	0000 0010
1°C	0000 0001
0°C	0000 0000
-1°C	0100 0001
-2°C	0100 0010
-64°C	0100 0000

The F71872 can provide two external thermal sensors to detect temperature. When monitored temperature exceeds the over-temperature threshold value, OVT# (pin77) will be asserted until the temperature goes below the hysteresis temperature.

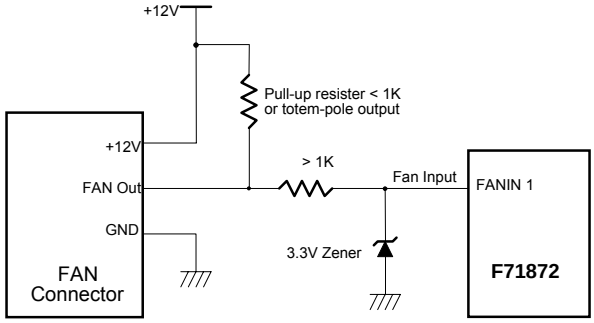


6.4.3 Fan speed count

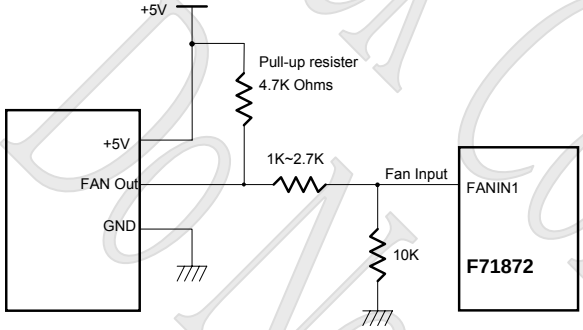
Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over VCC. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as follows:



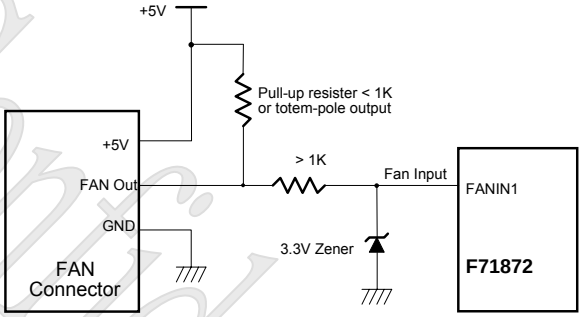
Fan with Tach Pull-Up to +12V, or Totern-Pole Output and Register Attenuator



Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp



Fan with Tach Pull-Up to +5V, or Totern-Pole Output and Register Attenuator



+5V, or

Fan with Tach Pull-Up to Totem-Pole Putput and Zener

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachmeter output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

6.4.4 Fan speed control

The F71872 provides 2 fan speed control methods: 1. Linear FAN Control 2. PWM Duty Cycle

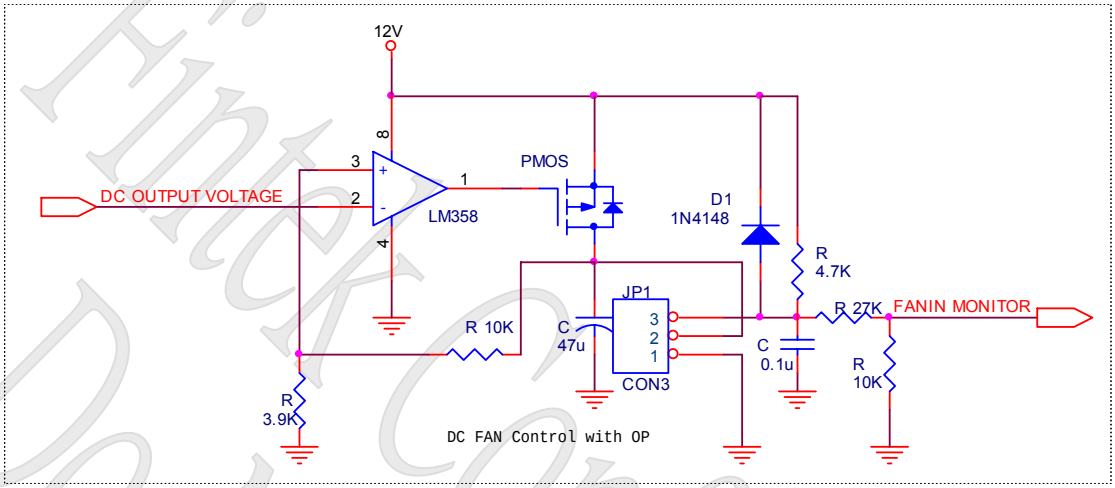
Linear Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register (CR6Bh for FAN1, CR7Bh for FAN2 and CR8Bh for FAN3). 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V.

The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = 3.3 \times \frac{\text{Programmed 8 - bit Register Value}}{255}$$

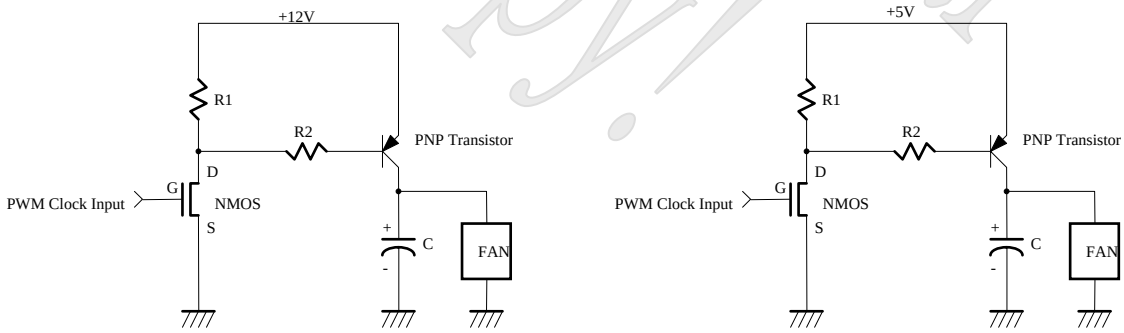
And the suggested application circuit for linear fac control would be:



PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register which are defined in the CR6Bh, CR7Bh and CR8Bh. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$



6.4.5 Fan speed control mechanism

There are 3 modes to control fan speed and they are manual, fan speed mode and temperature mode. For manual mode, it generally acts as PWM fan speed control. As for speed mode and temperature mode, they are more intelligent fan speed control and described as below:

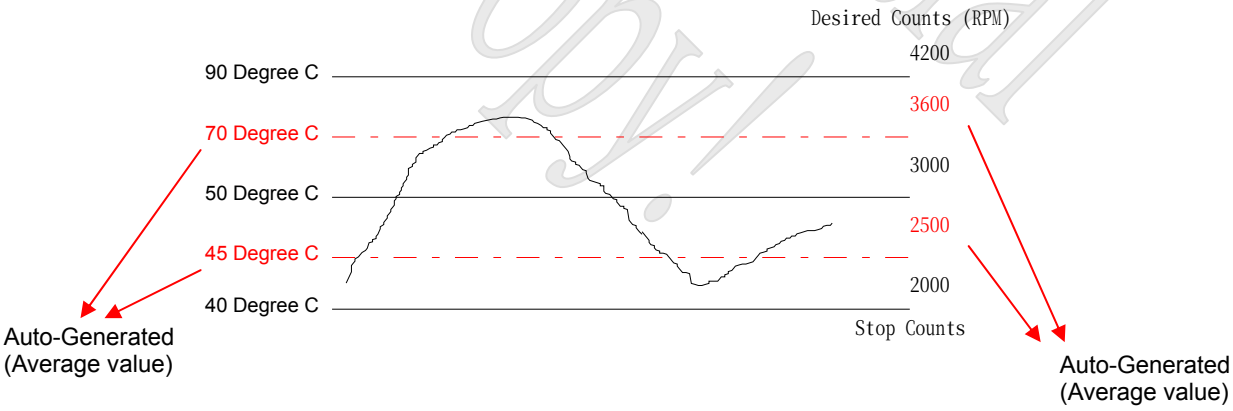
Fan Speed mode

Fan speed mode is an intelligent method according to expected fan speed pre-setting by BIOS. In the beginning, fan speed will be operated at full speed and the F71872 will get the full speed count value. After that, the fan speed will automatically rotate according to the expected fan speed setting by BIOS. For instance, the register CR69h and CR6Ah are used for this mode of FAN1.

Temperature mode

At this mode, F71872 provides the clever system to automatically control fan speed related to temperature system. The F71872 can provide three temperature boundaries and three intervals for user setting, and each interval has its related fan speed count. All these values should be set by BIOS first. In the F71872 design, the F71872 will auto-generate temperature boundaries (average value) between those boundaries that user setting, and it will auto-produce interval fan speed count (average value) between users setting value.

If the temperature value is set to 40, 50 and 90°C, it will auto-generate two temperature boundaries value of 45°C (This value is calculated automatically by hardware design of the F71872. (450+40)/2 =45) and 70°C. The same way, the related desired fan speed counts for each interval are 4200RPM, 3600RPM, 3000RPM, 2500RPM, 2000RPM and Stop Counts. When the temperature is within 50~70°C, the fan speed counts will be 3000RPM (Registers CRA4h~CRA9h, CRB4h~CRB9h and CRC4h~CRC9h). The F71872 will auto-adjust PWMOUT (PWM_DUTY) to make fan speed match the expected value. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature varying. The F71872 will take charge of all the fan speed control and need no software support.



PWMOUT Duty-cycle operating process

In both “FAN SPEED” and “TEMPERATURE” modes, F71872 adjust PWMOUT (PWM_DUTY1 (CR6B) of Fan1, PWM_DUTY2 (CR7B) of Fan2, PWM_DUTY3 (CR8B) of Fan3) duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is FFFFh, PWMOUT duty-cycle (PWM_DUTY)will be set to 00h to turn off fan.

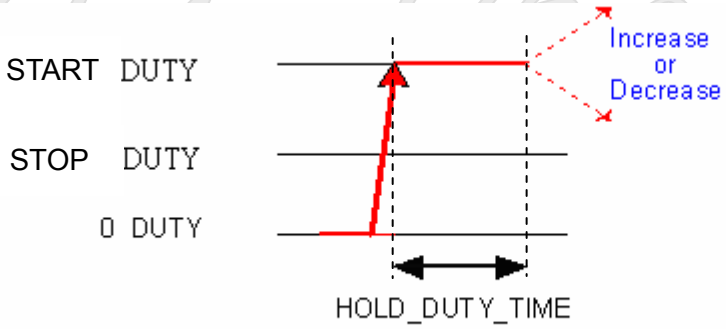
(2). When expected count is 0000h, PWMOUT duty-cycle (PWM_DUTY) will be set to FFh to turn on fan with full speed.

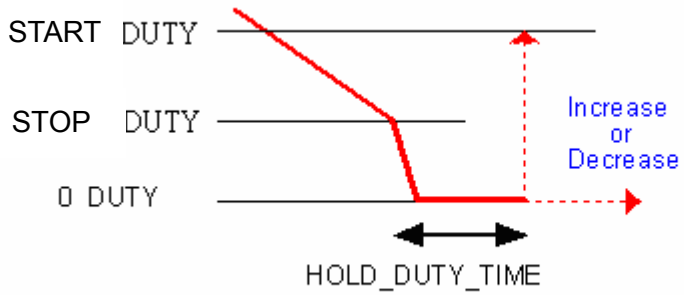
(3). If both (1) and (2) are not true and KEEP_STOP (see INDEX 60h) is set to 0:

(a). When PWMOUT duty-cycle decrease to STOP_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, F71872 will keep duty-cycle at 00h 3 seconds[1]. After that, F71872 starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the 3 seconds[1] period, F71872 will ignore it.

(b). When PWMOUT duty-cycle increase from 00h to START_DUTY(≠ 00h), F71872 also will keep duty-cycle at START_DUTY 3 seconds[1]. After that, F71872 starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the 3 seconds[1] period, F71872 will ignore it.

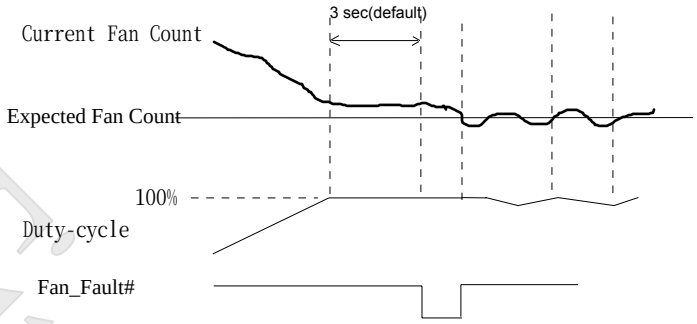
Note 1: The period of HOLD_DUTY_TIME can be programmed at INDEX 67h of FAN1.





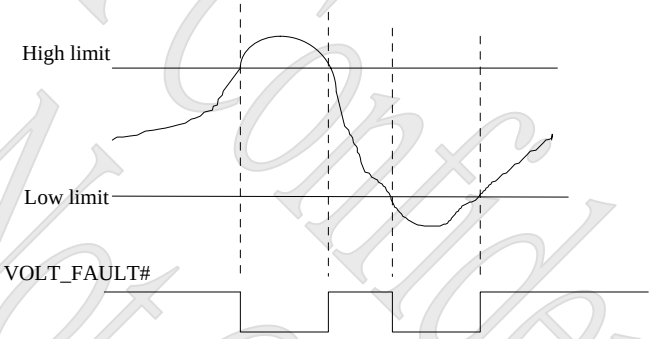
6.4.6 FAN_FAULT#

Fan_Fault will be asserted (throuth PME# Pin 73) when the fan speed doesn't meet the expected fan speed within a programmable period (default is 3 seconds) when PWMOUT duty-cycle is 100%.



6.4.7 VOLT_FAULT# (Voltage Fault Signal)

When voltage leaps from the security range setting by BIOS, the warning signal VOLT_FAULT# will be activated. Shown in figure.



6.5 FDC

The Floppy Disk Controller provides the interface between a host processor and one floppy disk drives. It integrates a controller and a digital data separator with write pre-compensation, data rate selection logic, microprocessor interface, and a set of registers. The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-mode type drives.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD. The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

6.6 UART

The F71872 provides two UART ports and supports IRQ sharing for system application. The UARTs are used to convert data between parallel format and serial format. They convert parallel data into serial format on transmission and serial format into parallel data on receiver side. The serial format is formed by one start bit, followed by five to eight data bits, a parity bit if programmed and one (1.5 or 2) stop bits. The UARTs include complete modem control capability and an interrupt system that may be software trailed to the computing time required to handle the communication link. They have FIFO mode to reduce the number of interrupts presented to the host. Both receiver and transmitter have a 16-byte FIFO.

6.7 Parallel Port

The parallel port in F71872 supports an IBM XT/AT compatible parallel port (SPP), bi-directional paralle port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP) mode. Refer to the configuration registers for more information on selecting the mode of operation.

6.8 Keyboard Controller

The keyboard controller is implemented using 8 bits microcontroller that is capable of executing the 8042 instruction set. the 8 bit microcontroller has 256 bytes of RAM for DATA memory and 2kbytes of ROM for program storage.

The keyboard controller receives serial data from keyboard or PS/2 mouse, check parity of data and placed data in output buffer, the keyboard controller will interrupt system when data is placed in its output buffer.

Keyboard and mouse interface

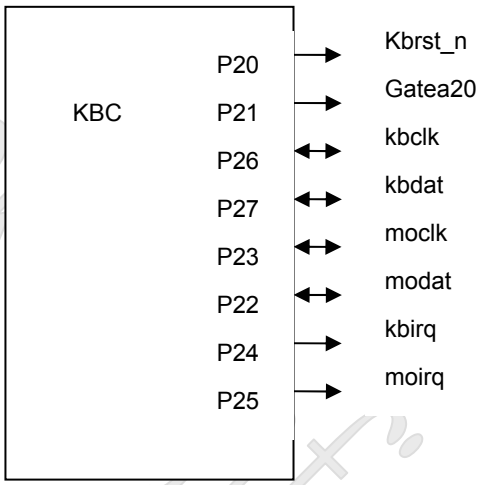
The kbclk is keyboard clock which is pin p26 of microcontroller and kbdat is Keyboard data which is pin p27 of microcontroller. The moclk is Mouse clock which is pin p23 of microcontroller and modat is mouse data which is pin p22 of microcontroller.

Kbirq and moirq

The kbirq is keyboard interrupt system signal which is pin p24 of microcontroller and moirq mouse is interrupt system which is pin p25 of microcontroller.

Keyboard reset and GateA20

Keyboard reset (kbrst_n) is pin p20 of microcontroller or hardware decode. It is selected by bit 0 of clock select register(index F0h).GateA20 is pin p21 of microcontroller or hardware decode, It is selected by bit 1 of clock select register(index F0h)



Host Phase

The table is keyboard controller interface with the system.

Read data: this is an 8 bit read only register, when system read this register; the interrupt and obf flag will be cleared.

Write data: this is an 8 bit write only register, when system write this register, the ibf flag will be set.

Read status: this is an 8 bit read only register, it replay KBC status.

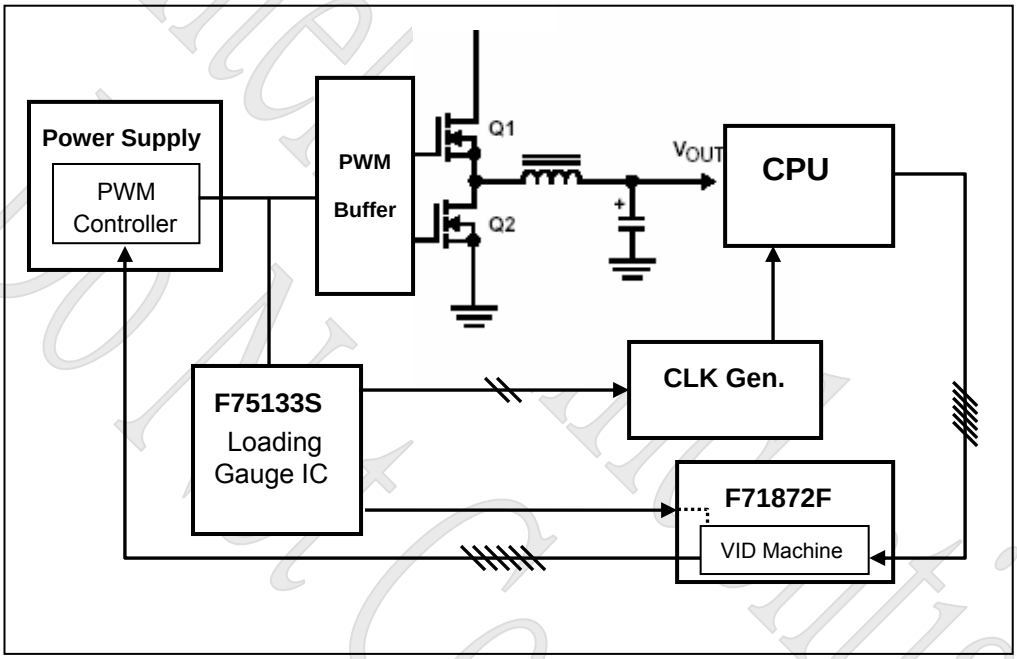
Write command: this is an 8 bit write only register, when system write this register, the ibf flag will be set.

Host address	R/W	Function
60h	R	Read data
60h	W	Write data
64h	R	Read status
64h	W	Write command

6.9 Dynamic Voltage Change Application

The F71872 supports an automatic/dynamic over-voltage function for application of over-clocking or under clocking. This function provides a pin by external trigger signal to improve the CPU's performance by

voltage changing automatically when system is going to run over-clocking or under-clocking. As the sketch shows as below, due to achieve this action, suggests using F75133S Loading Gauge to be a part that detects system/CPU loading to decide when issues the over-clocking/under-clocking and trigger VID signals for system executing. For instance, user would like to ensure system stably and run over-clocking/under-clocking on MB, the F75133S will sense the PWM duty to know the loading status. If the system loading reach the limit of over-clocking, F75133S will issue signal to F71872 to trigger Vcore increasing automatically for proper Vcore for running over-clocking, secondly F75133S issues signal to CLK Gen for over-clocking. That's what the F71872 facilitates system steady by auto-changing Vcore with F75133S when runs over-clocking.



7 Register Descriptions

7.1 Global Control Registers

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F (Can be programmed by register!). To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

7.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

7.1.2 Logic Device Number Register — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	03h	Chip ID 1 of F71872.

7.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	41h	Chip ID2 of F71872.

7.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1 of Fintek devices.

7.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2 of Fintek devices.

7.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	SOFTPD_KBC	R/W	0	Power down the KBC device. This will stop the KBC clock.
4	SOFTPD_HM	R/W	0	Power down the Hardware Monitor device. This will stop the Hardware Monitor clock.
3	SOFTPD_PRT	R/W	0	Power down the Parallel Port device. This will stop the Parallel Port clock.
2	SOFTPD_UR2	R/W	0	Power down the UART 2 device. This will stop the UART 2 clock.
1	SOFTPD_UR1	R/W	0	Power down the UART 1 device. This will stop the UART 1 clock.
0	SOFTPD_FDC	R/W	0	Power down the FDC device. This will stop the FDC clock.

7.1.8 UART IRQ Sharing Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	W	0	0: System external clock is 48MHz 1: System external clock is 24MHz
6-2	Reserved	-	-	Reserved.
1	IRQ_MODE	R/W	0	0: PCI IRQ sharing mode (low level). 1: ISA IRQ sharing mode (low pulse).
o	IRQ_SHAR	R/W	0	0: disable IRQ sharing of two UART devices. 1: enable IRQ sharing of two UART devices.

7.1.9 Port Select Register — Index 27h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	PORT_4E_EN	W	-	The default value of the register is power on trap by SOUT1. Pull down to select configuration register port 2E/2F, else 4E/4F. The port could be changed by writing this register. 0: Configuration register port is 2E/2F. 1: Configuration register port is 4E/4F.
3-0	Reserved	-	-	Reserved.

7.1.10 Power LED Function Select Register — Index 28h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.

6-5	VDDLED_SEL	R/W	2’b11	VDDLED function select, powered by VDD. 00: VDDLED always output low. 01: VDDLED tri-state 10: VDDLED output 0.5Hz clock. 11: VDDLED output 1Hz clock. (clock output is inverse with VSBLED clock output) (Powered by VDD)
4	VDDLED_EN	R/W	0	VDDLED enable, powered by VDD. 0: the function of PCIRST5#/GP15/VDDLED is PCIRST5#/GP15. 1: the function of PCIRST5#/GP15/VDDLED is VDDLED. (Powered by VDD)
3	Reserved	-	-	Reserved.
2-1	VSBLED_SEL	R/W	2’b11	VSBLED function select, powered by VSB3V. 00: VSBLED always output low. 01: VSBLED tri-state 10: VSBLED output 0.5Hz clock. 11: VSBLED output 1Hz clock. (Powered by VSB)
0	VSBLED_EN	R/W	0	VSBLED enable, powered by VSB3V. 0: the function of PWROK2/GP25/VSBLED is PWROK2/GP25. 1: the function of PWROK2/GP25/VSBLED is VSBLED. (Powered by VSB)

7.1.11 Multi Function Select 1 Register — Index 29h (Powered by VDD)

Bit	Name	R/W	Default	Description
7	RST_DRV_DIS	R	1	0: enable PCIRSTx pin driving. 1: disable PCIRSTx pin driving. Power on trap by DTR2#
6-5	Reserved	-	-	Reserved.

4	PIN29_IRRX_EN	W	0	0: the function of pin 29 is GPIO3/Voltage_fault1. 1: the function of pin 29 is IRRX.
3	BEEP_GPEN	R/W	0	0: the function of GPIO4/Voltage_fault2#/BEEP is GPIO4/Voltage_fault2#. 1: the function of GPIO4/Voltage_fault2#/BEEP is BEEP.
2	FANCTL_GPEN	R/W	0	0: the function of GPIO5/Voltage_fault3#/FANCTL is PIO5/Voltage_fault3#. 1: the function of GPIO5/Voltage_fault3#/FANCTL is FANCTL.
1	VIN8_EN	R/W	0	0: the function of PCIRSTIN#/VIN8 is PCIRSTIN#. 1: the function of PCIRSTIN#/VIN8 is VIN8.
0	VIN4_EN	R/W	0	0: the function of ATXPG/VIN4 is ATXPG. 1: the function of ATXPG/VIN4 is VIN4.

7.1.12 Multi Function Select 2 Register — Index 2Ah (Powered by VDD)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_EN	R/W	0	0: the function of IRTX/GPIO16 is IRTX. 1: the function of IRTX/GPIO16 is GPIO16.
5	GPIO15_EN	R/W	0	It works when VDDLED_EN is 0. 0: the function of PCIRST5#/GPIO15 is PCIRST5#. 1: the function of PCIRST5#/GPIO15 is GPIO15.
4	GPIO14_EN	R/W	0	0: the function of PCIRST3#/GPIO14 is PCIRST3#. 1: the function of PCIRST3#/GPIO14 is GPIO14.
3	GPIO13_EN	R/W	0	0: the function of PCIRST2#/GPIO13 is PCIRST2#. 1: the function of PCIRST2#/GPIO13 is GPIO13.
2	GPIO12_EN	R/W	0	0: the function of PWROK1/GPIO12 is PWROK1. 1: the function of PWROK1/GPIO12 is GPIO12.
1	GPIO11_EN	R/W	0	0: the function of PCIRST1#/GPIO11 is PCIRST1#. 1: the function of PCIRST1#/GPIO11 is GPIO11.
0	GPIO10_EN	R/W	0	0: the function of RSTCON#/GPIO10 is RSTCON#. 1: the function of PCIRST0#/GPIO10 is GPIO10.

7.1.13 Multi Function Select 3 Register — Index 2Bh (Powered by VDD)

Bit	Name	R/W	Default	Description
7-6	GPIO6_SEL	R/W	00	00: the function of GPIO6/Voltage_fault4#/WDTRST1#/OVT# is GPIO6. 01: the function of GPIO6/Voltage_fault4#/WDTRST1#/OVT# is Voltage_fault4#. 10: the function of GPIO6/Voltage_fault4#/WDTRST1#/OVT# is WDTRST1#. 11: the function of GPIO6/Voltage_fault4#/WDTRST1#/OVT# is OVT#. (Powered by VDD, reset by VDD3VOK)
5	VIN3F_EN	R/W	0	Functions when FANCTL_GPEN is 0. 0: the function of GPIO5/Voltage_fault3# is GPIO5. 1: the function of GPIO5/Voltage_fault3# is Voltage_fault3#.
4	VIN2F_EN	R/W	0	Functions when BEEP_GPEN is 0. 0: the function of GPIO4/Voltage_fault2# is GPIO4. 1: the function of GPIO4/Voltage_fault2# is Voltage_fault2#.
3	VIN1F_EN	R/W	0	0: the function of GPIO3/Voltage_fault1# is GPIO3. 1: the function of GPIO3/Voltage_fault1# is Voltage_fault1#.
2	VIN7_ID2_EN	R/W	0	0: the function of GPIO2 is GPIO2. 1: Reserved
1	VIN7_ID1_EN	R/W	0	0: the function of GPIO1 is GPIO1. 1: Reserved
0	VIN7_ID0_EN	R/W	0	0: the function of GPIO0 is GPIO0. 1: Reserved

7.1.14 Multi Function Select 4 Register — Index 2Ch (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO27_EN	R/W	0	0: the function of RSMRST#/GPIO27 is RSMRST#. 1: the function of RSMRST#/GPIO27 is GPIO27.
6	GPIO26_EN	R/W	0	0: the function of PCIRST4#/GPIO26 is PCIRST4#. 1: the function of PCIRST4#/GPIO26 is GPIO26.

5	GPIO25_EN	R/W	0	Functions when VSBLED_EN is 0. 0: the function of PWROK2/GPIO25 is PWROK2. 1: the function of PWROK2/GPIO25 is GPIO25.
4	Reserved	-	-	Reserved.
3	GPIO23_EN	R/W	0	0: the function of PSON#/GPIO23 is PSON#. 1: the function of PSON#/GPIO23 is GPIO23.
2	GPIO22_EN	R/W	0	0: the function of PWSWIN#/GPIO22 is PWSWIN#. 1: the function of PWSWIN#/GPIO22 is GPIO22.
1	GPIO21_EN	R/W	0	0: the function of PME#/GPIO21 is PME#. 1: the function of PME#/GPIO21 is GPIO21.
0	GPIO20_EN	R/W	0	0: the function of PWSWOUT#/GPIO20 is PWSWOUT#. 1: the function of PWSWOUT#/GPIO20 is GPIO20.

7.1.15 Multi Function Select 5 Register — Index 2Dh (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R	0	0: external clock is 48MHz 1: external clock is 24MHz.
6	PIN29_IRRX_EN	R	0	0: the function of pin 29 is GPIO3/Voltage_fault1. 1: the function of pin 29 is IRRX.
5	PIN77_DRV_EN	R/W	0	Set the output type of pin 77 when programmed as GPIO24. 0: open drain. 1: push-pull.
4	PIN70_DRV_EN	R/W	0	Set the output type of pin 70 when programmed as GPIO30. 0: open drain. 1: push-pull.
3-2	GPIO24_SEL	R/W	01	00: the function of GPIO24/OVT#/WDTRST2# is GPIO24. 01: the function of GPIO24/OVT#/WDTRST2# is OVT#. 10: the function of GPIO24/OVT#/WDTRST2# is WDTRST2#. 11: Reserved.

1	GPIO31_EN	R/W	0	0: the function of S3#/GPIO31 is S3#. 1: the function of S3#/GPIO31 is GPIO31.
0	GPIO30_EN	R/W	0	0: the function of IRRX/GPIO30 is IRRX. 1: the function of IRRX/GPIO30 is GPIO30.

7.2 FDC Registers

7.2.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.2.2 FDC Configuration Registers

FDC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	FDC_EN	R/W	1	0: disable FDC. 1: enable FDC.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description

7-0	BASE_ADDR_HI	R/W	03h	The MSB of FDC base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F0h	The LSB of FDC base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELFDCIRQ	R/W	06h	Select the IRQ channel for FDC.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2-0	SELFDCDMA	R/W	010	Select the DMA channel for FDC.

FDD Mode Register — Index F0h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-2	IF_MODE	R/W	11	00: Model 30 mode. 01: PS/2 mode. 10: Reserved. 11: AT mode (default).
1	FDMAMODE	R/W	1	0: enable burst mode. 1: non-busrt mode (default).
0	EN3MODE	R/W	0	0: normal floppy mode (default). 1: enhanced 3-mode FDD.

FDD Drive Type Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.

1-0	FDD_TYPE	R/W	11	FDD drive type.

FDD Selection Register — Index F4h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4-3	FDD_DRT	R/W	00	Data rate table select, refer to table A. 00: select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 mega tape. 11: reserved.
2	Reserved	-	-	Reserved.
1-0	FDD_DT	R/W	00	Drive type select, refer to table B.

TABLE A

Data Rate Table Select		Data Rate		Selected Data Rate		DENSEL
FDD_DRT[1]	FDD_DRT[0]	DATARATE1	DATARATE0	MFM	FM	
0	0	0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
0	1	0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
1	0	0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0
		1	1	1Meg	---	1

TABLE B

Drive Type		DRVDEN0	Remark
FDD_DT1	FDD_DT0		
0	0	DENSEL	4/2/1 MB 3.5” 2/1 MB 5.25” 1/1.6/1 MB 3.5” (3-Mode)
0	1	DATARATE1	

1	0	DENSEL#
1	1	DATARATE0

7.2.3 Device Registers

7.2.3.1 Status Register A (PS/2 mode) — Base + 0

Bit	Name	R/W	Default	Description
7	INTPEND	R	0	This bit indicates the state of the interrupt output.
6	DRV2_N	R	-	0: a second drive has been installed. 1: a second drive has not been installed.
5	STEP	R	0	This bit indicates the complement of STEP# disk interface output.
4	TRK0_N	R	-	This bit indicates the state of TRK0# disk interface input.
3	HDSEL	R	0	This bit indicates the complement of HDSEL# disk interface output. 0: side 0. 1: side 1.
2	INDEX_N	R	-	This bit indicates the state of INDEX# disk interface input.
1	WPT_N	R	-	This bit indicates the state of WPT# disk interface input. 0: disk is write-protected. 1: disk is not write-protected.
0	DIR	R	0	This bit indicates the complement of DIR# disk interface output.

7.2.3.2 Status Register A (Model 30 mode) — Base + 0

Bit	Name	R/W	Default	Description
7	INTPEND	R	0	This bit indicates the state of the interrupt output.
6	DRQ	R	0	This bit indicates the state of the DRQ signal.
5	STEP_FF	R	0	This bit indicates the complement of latched STEP# disk interface output.
4	TRK0	R	-	This bit indicates the complement of TRK0# disk interface input.
3	HDSEL_N	R	1	This bit indicates the state of HDSEL# disk interface output. 0: side 0. 1: side 1.
2	INDEX	R	-	This bit indicates the complement of INDEX# disk interface input.
1	WPT	R	-	This bit indicates the complement of WPT# disk interface input. 0: disk is write-protected. 1: disk is not write-protected.
0	DIR_N	R	1	This bit indicates the state of DIR# disk interface output. 0: head moves in inward direction. 1: head moves in outward direction.

7.2.3.3 Status Register B (PS/2 Mode) — Base + 1

Bit	Name	R/W	Default	Description
7-6	Reserved	R	11	Reserved. Return 11b when read.
5	DR0	R	0	Drive select 0. This bit reflects the bit 0 of Digital Output Register.
4	WDATA	R	0	This bit changes state at every rising edge of WDATA#.
3	RDATA	R	0	This bit changes state at every rising edge of RDATA#.
2	WGATE	R	0	This bit indicates the complement of WGATE# disk interface output.
1	MOTEN1	R	0	This bit indicates the complement of MOB# disk interface output. Not support in this design.
0	MOTEN0	R	0	This bit indicates the complement of MOA# disk interface output.

7.2.3.4 Status Register B (Model 30 Mode) — Base + 1

Bit	Name	R/W	Default	Description
7	DRV2_N	R	-	0: a second drive has been installed. 1: a second drive has not been installed.
6	DSB_N	R	1	This bit indicates the state of DRVB# disk interface output. Not support in this design.
5	DSA_N	R	1	This bit indicates the state of DRVA# disk interface output.
4	WDATA_FF	R	0	This bit is latched at the rising edge of WDATA# and is cleared by a read from the Digital Input Register.
3	RDATA_FF	R	0	This bit is latched at the rising edge of RDATA# and is cleared by a read form the Digital Input Register.
2	WGATE_FF	R	0	This bit is latched at the falling edge of WGATE# and is cleared by a read from the Digital Input Register.
1	DSD_N	R	1	This bit indicates the complement of DRVD# disk interface output. Not support in this design.
0	DSC_N	R	1	This bit indicates the complement of DRVC# disk interface output. Not support in this design.

7.2.3.5 Digital Output Register — Base + 2

Bit	Name	R/W	Default	Description
7	MOTEN3	R	0	Motor enable 3. Not support in this design.
6	MOTEN2	R	0	Motor enable 2. Not support in this design.
5	MOTEN1	R/W	0	Motor enable 1. Used to control MOB#. MOB# is not support in this design.
4	MOTEN0	R/W	0	Motor enable 0. Used to control MOA#.
3	DAMEN	R/W	0	DMA enable. This bit has two mode of operation. PC-AT and Model 30 mode: write 1 will enable DMA and IRQ, write 0 will disable DMA and IRQ. PS/2 mode: This bit is reserved. DMA and IRQ are always enabled in PS/2 mode.
2	RESET	R	0	Write 0 to this bit will reset the controller. I will remain in reset condition until a 1 is written.

1	DSD_N	R	1	This bit indicates the complement of DRVD# disk interface output. Not support in this design.
0	DSC_N	R	1	This bit indicates the complement of DRVC# disk interface output. Not support in this design.

7.2.3.6 Tape Drive Register — Base + 3

Bit	Name	R/W	Default	Description
7-6	Reserved	R	00	Reserved. Return 00b when read.
5-4	TYPEID	R	11	Reserved in normal function, return 11b when read. If 3 mode FDD function is enabled. These bits indicate the drive type ID.
3-2	Reserved	R	11	Reserved. Return 11b when read in normal function. Return 00b when read in 3 mode FDD function.
1-0	TAPESEL	R/W	0	These bits assign a logical drive number to be a tape drive.

7.2.3.7 Main Status Register — Base + 4

Bit	Name	R/W	Default	Description
7	RQM	R	0	Request for Master indicates that the controller is ready to send or receive data from the uP through the FIFO.
6	DIO	R	0	Data I/O (direction): 0: the controller is expecting a byte to be written to the Data Register. 1: the controller is expecting a byte to be read from the Data Register.
5	NON_DMA	R	0	Non DMA Mode: 0: the controller is in DAM mode. 1: the controller is interrupt or software polling mode.
4	FDC_BUSY	R	0	This bit indicate that a read or write command is in process.
3	DRV3_BUSY	R	0	FDD number 3 is in seek or calibration condition. FDD number 3 is not support in this design.
2	DRV2_BUSY	R	0	FDD number 2 is in seek or calibration condition. FDD number 2 is not support in this design.
1	DRV1_BUSY	R	0	FDD number 1 is in seek or calibration condition. FDD number 1 is not support in this design.
0	DRV0_BUSY	R	0	FDD number 0 is in seek or calibration condition.

7.2.3.8 Data Rate Select Register — Base + 4

Bit	Name	R/W	Default	Description
7	SOFTRST	W	0	A 1 written to this bit will software reset the controller. Auto clear after reset.
6	PWRDOWN	W	0	A 1 to this bit will put the controller into low power mode which will turn off the oscillator and data separator circuits.
5	Reserved	-	-	Return 0 when read.

4-2	PRECOMP	W	000	Select the value of write precompensation: 250K-1Mbps 2Mbps 000: default delays default delays 001: 41.67ns 20.8ns 010: 83.34ns 41.17ns 011: 125.00ns 62.5ns 100: 166.67ns 83.3ns 101: 208.33ns 104.2ns 110: 250.00ns 125.00ns 111: 0.00ns (disabled) 0.00ns (disabled) The default value of corresponding data rate: 250Kbps: 125ns 300Kbps: 125ns 500Kbps: 125ns 1Mbps: 41.67ns 2Mbps: 20.8ns
1-0	DRATE	W	10	Data rate select: MFM FM 00: 500Kbps 250Kbps 01: 300Kbps 150Kbps 10: 250Kbps 125Kbps 11: 1Mbps illegal

7.2.3.9 Data (FIFO) Register — Base + 5

Bit	Name	R/W	Default	Description
7-0	DATA	R/W	00h	The FIFO is used to transfer all commands, data and status between controller and the system. The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. The FIFO is default disabled and could be enabled via the CONFIGURE command.

Status Registers 0

Bit	Name	R/W	Default	Description
7-6	IC	R	-	Interrupt code : 00: Normal termination of command. 01: Abnormal termination of command. 10: Invalid command. 11: Abnormal termination caused by poling.
5	SE	R	-	Seek end. Set when a SEEK or RECALIBRATE or a READ or WRITE with implied seek command is completed.
4	EC	R	-	Equipment check. 0: No error 1: When a fault signal is received form the FDD or the TRK0# signal fails to occur after 77 step pulses.

3	NR	R	-	Not ready. 0: Drive is ready 1: Drive is not ready.
2	HD	R	-	Head address. The current head address.
1-0	DS	R	-	Drive select. 00: Drive A selected. 01: Drive B selected. 10: Drive C selected. 11: Drive D selected.

Status Registers 1

Bit	Name	R/W	Default	Description
7	EN	R	-	End of Track. Set when the FDC tries to access a sector beyond the final sector of a cylinder.
6	DE	R	-	Data Error. The FDC detect a CRC error in either the ID field or the data field of a sector.
4	OR	R	-	Overrun/Underrun. Set when the FDC is not serviced by the host system within a certain time interval during data transfer.
3	Reserved	-	-	Unused. This bit is always “0”
2	ND	R	-	No Data. Set when the following conditions occurred: 1. The specified sector is not found during any read command. 2. The ID field cannot be read without errors during a READ ID command. 3. The proper sector sequence cannot be found during a READ TRACK command.
1	NW	R	-	No Writable Set when WPT# is active during execution of write commands.
0	MA	R	-	Missing Address Mark. Set when the following conditions occurred: 1. Cannot detect an ID address mark at the specified track after encountering the index pulse form the INDEX# pin twice. 2. Cannot detect a data address mark or a deleted data address mark on the specified track.

Status Registers 2

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Unused. This bit is always “0”.
6	CM	R	-	Control Mark. Set when following conditions occurred: 1. Encounters a deleted data address mark during a READ DATA command. 2. Encounters a data address mark during a READ DELETED DATA command.

5	DD	R	-	Data Error in Data Field. The FDC detects a CRC error in the data field.
4	WC	R	-	Wrong Cylinder. Set when the track address from the sector ID field is different from the track address maintained inside the FDC.
3	SE	R	-	Scan Equal. Set if the equal condition is satisfied during execution of the SCAN command.
2	SN	R	-	Scan Not Satisfied. Set when the FDC cannot find a sector on the track which meets the desired condition during any scan command.
1	BC	R	-	Bad Cylinder. The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FFh which indicates a bad track.
0	MD	R	-	Missing Data Address Mark. Set when the FDC cannot detect a data address mark or a deleted data address mark.

Status Registers 3

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Unused. This bit is always “0”.
6	WP	R	-	Write Protect. Indicates the status of WPT# pin.
5	Reserved	R	-	Unused. This bit is always “1”.
4	T0	R	-	Track 0. Indicates the status of the TRK0# pin.
3	Reserved.	R	-	Unused. This bit is always “1”.
2	HD	R	-	Head Address. Indicates the status of the HDSEL# pin.
1	DS1	R	-	Drive Select. These two bits indicate the DS1, DS0 bits in the command phase.
0	DS0	R	-	

7.2.3.10 Digital Input Register (PC-AT Mode) — Base + 7

Bit	Name	R/W	Default	Description
7	DSKCHG	R	-	This bit indicates the complement of DSKCHG# disk interface input.
6-0	Reserved	R	-	Reserved.

7.2.3.11 Digital Input Register (PS/2 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7	DSKCHG	R	-	This bit indicates the complement of DSKCHG# disk interface input.
6-3	Reserved	-	-	Reserved.

2-1	DRATE	R	10	These bits indicate the status of the DRATE programmed through the Data Rate Select Register or Configuration Control Register.
0	HIGHDEN_N	R	1	0: 1Mbps or 500Kbps data rate is chosen. 1: 300Kbps or 250Kbps data rate is chosen.

7.2.3.12 Digital Input Register (Model 30 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7	DSKCHG_N	R	-	This bit indicates the state of DSKCHG# disk interface input.
6-4	Reserved	-	-	Reserved.
3	DMAEN	R	0	This bit reflects the DMA bit in Digital Output Register.
2	NOPRE	R	0	This bit reflects the NOPRE bit in Configuration Control Register.
1-0	DRATE	R	10	These bits indicate the status of DRATE programmed through the Data Rate Select Register or Configuration Control Register.

7.2.3.13 Configuration Control Register (PC-AT and PS/2 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	DRATE	W	10	These bit determine the data rate of the floppy controller. See DRATE bits in Data Rate Select Register.

7.2.3.14 Configuration Control Register (Model 30 Mode) — Base + 7

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2	NOPRE	W	0	This bit could be programmed through Configuration Control Register and be read through the bit 2 in Digital Input Register in Model 30 Mode. But it has no functionality.
1-0	DRATE	W	10	These bit determine the data rate of the floppy controller. See DRATE bits in Data Rate Select Register.

7.2.3.15 FDC Commands

Terminology:

C	Cylinder Number 0 -256
D	Data Pattern
DIR	Step Direction 0: step out 1: step in
DS0	Drive Select 0
DS1	Drive Select 1
DTL	Data Length

EC	Enable Count
EOT	End of Track
EFIFO	Enable FIFO 0: FIFO is enabled. 1: FIFO is disabled.
EIS	Enable Implied Seek
FIFOTHR	FIFO Threshold
GAP	Alters Gap Length
GPL	Gap Length
H/HDS	Head Address
HLT	Head Load Time
HUT	Head Unload Time
LOCK	Lock EFIFO, FIFOTHR, PTRTRK bits. Prevent these bits from being affected by software reset.
MFM	MFM or FM mode 0: FM 1: MFM
MT	Multi-Track
N	Sector Size Code. All values up to 07h are allowable. 00: 128 bytes 01: 256 bytes .. .. 07 16 Kbytes
NCN	New Cylinder Number
ND	Non-DMA Mode
OW	Overwritten
PCN	Present Cylinder Number
POLL	Polling disable 0: polling is enabled. 1: polling is disabled.
PRETRK	Precompensation Start Track Number
R	Sector address
RCN	Relative Cylinder Number
SC	Sector per Cylinder
SK	Skip deleted data address mark
SRT	Step Rate Time
ST0	Status Register 0
ST1	Status Register 1
ST2	Status Register 2
ST3	Status Register 3
WGATE	Write Gate alters timing of WE.

Read Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	SK	0	0	1	1	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								

	W	---------- N ----------
	W	---------- EOT ----------
	W	---------- GPL ----------
	W	---------- DTL ----------
Execution		Data transfer between the FDD and system
Result	R	---------- ST0 ----------
	R	---------- ST1 ----------
	R	---------- ST2 ----------
	R	---------- C ----------
	R	---------- H ----------
	R	---------- R ----------
	R	---------- N ----------

Status information after command execution.

Sector ID information after command execution.

Read Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	SK	0	1	1	0	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Read A Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	MFM	0	0	0	0	1	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system. FDD reads contents of all cylinders from index hole to EOT.
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Read ID

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	MFM	0	0	1	0	1	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register.
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								

	R	---------- C ----------	Disk status after the command has been completed.
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

Verify

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	SK	1	0	1	1	0	Command code
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL/SC ----------								
Execution										No data transfer
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Version

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

Write Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark

Command	W	MT	MFM	0	0	0	1	0	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system.
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution.
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

Write Deleted Data

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	MT	MFM	0	0	1	0	0	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system.
Result	R	---------- ST0 ----------								Status information after command
	R	---------- ST1 ----------								

	R	---------- ST2 ----------	execution.
	R	---------- C ----------	Sector ID information after command execution.
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

Format A Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	MFM	0	0	1	1	0	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes/Sector
	W	---------- SC ----------								Sectors/Cylinder
	W	---------- GPL ----------								Gap 3 Length
	W	---------- D ----------								Data Pattern
Execution for each sector (repeat)	W	---------- C ----------								Input sector parameter.
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution.
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

Recalibrate

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	0	1	1	1	Command code
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to track 0

Sense Interrupt Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								
	R	---------- PCN ----------								

Specify

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	0	0	1	1	Command code
	W	|---------- SRT ----------|				|---------- HUT ----------|			
	W	|---------- SRT ----------|						ND	

Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	1	1	1	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution										Head positioned over proper cylinder on diskette

Configure

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	1	0	0	1	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	0	EIS	EFIFO	POLL	|---------- FIFOTHR ----------|				
	W	---------- PRETRK ----------								
Execution										Internal registers written

Relative Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	1	DIR	0	0	1	1	1	1	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	

	W	---------- RCN ----------	

Perpendicular Mode

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	1	0	0	1	0	Command code
	W	OW	0	D3	D2	D1	D0	GAP	WGATE	

Lock

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	LOCK	0	0	1	0	1	0	0	Command code
Result	R	0	0	0	LOCK	0	0	0	0	

Dumpreg

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	1	1	1	0	Command code
Result	R	---------- PCN (Drive 0) ----------								
	R	---------- PCN (Drive 0) ----------								
	R	---------- PCN (Drive 0) ----------								
	R	---------- PCN (Drive 0) ----------								
	R	|---------- SRT ----------|				|---------- HUT ----------|		
	R	|---------- SRT ----------|						ND	
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	|---------- FIFOTHR ----------|				
	R	---------- PRETRK ----------								

Sense Drive Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	0	0	0	0	0	1	0	0	Command code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information abut disk drive

Invalid

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remark
Command	W	---------- Invalid Codes ----------								FDC goes to standby state.
Result	R	---------- ST0 ----------								ST0 = 80h

7.3 UART1 Registers

7.3.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.3.2 UART 1 Configuration Registers

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR1_EN	R/W	1	0: disable UART 1. 1: enable UART 1.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 1 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 1 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR1IRQ	R/W	4h	Select the IRQ channel for UART 1.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# low when transmitting data.
3-0	Reserved	-	-	Reserved.

7.3.3 Device Registers

7.3.3.1 Receiver Buffer Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	RBR	R	00h	The data received. Read only when LCR[7] is 0

7.3.3.2 Transmitter Holding Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	THR	W	00h	Data to be transmitted. Write only when LCR[7] is 0

7.3.3.3 Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Default	Description
7-0	DLL	R/W	01h	Baud generator divisor low byte. Access only when LCR[7] is 1.

7.3.3.4 Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Default	Description
7-0	DLM	R/W	00h	Baud generator divisor high byte. Access only when LCR[7] is 1.

7.3.3.5 Interrupt Enable Register — Base + 1

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	EDSSI	R/W	0	Enable Modem Status Interrupt. Access only when LCR[7] is 0.
2	ELSI	R/W	0	Enable Line Status Error Interrupt. Access only when LCR[7] is 0.
1	ETBFI	R/W	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR[7] is 0.
0	ERBFI	R/W	0	Enable Received Data Available Interrupt. Access only when LCR[7] is 0.

7.3.3.6 Interrupt Identification Register — Base + 2

Bit	Name	R/W	Default	Description
7	FIFO_EN	R	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	-	Reserved.
3-1	IRQ_ID	R	000	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	1	1: Interrupt is not pending. 0: Interrupt is pending.

7.3.3.7 FIFO Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	RCV_TRIG	W	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	-	Reserved.
2	CLRTX	R	0	Reset the transmitter FIFO.
1	CLRRX	R	0	Reset the receiver FIFO.

0	FIFO_EN	R	0	0: Disable FIFO. 1: Enable FIFO.

7.3.3.8 Line Control Register — Base + 3

Bit	Name	R/W	Default	Description
7	DLAB	R/W	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	0	
3	PEN	R/W	0	
2	STB	R/W	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

7.3.3.9 MODEM Control Register — Base + 4

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	LOOP	R/W	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	0	Read from MSR[6] is loop back mode
1	RTS	R/W	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

7.3.3.10 Line Status Register — Base + 5

Bit	Name	R/W	Default	Description
7	RCR_ERR	R	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.
6	TEMT	R	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.
4	BI	R	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	0	0: Data received has no parity error. 1: Data received has parity error.

1	OE	R	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	0	0: No data is ready for read. 1: Data is received.

7.3.3.11 MODEM Status Register — Base + 6

Bit	Name	R/W	Default	Description
7	DCD	R	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	0	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	0	0: No state changed at CTS#. 1: State changed at CTS#.

7.3.3.12 Scratch Register — Base + 7

Bit	Name	R/W	Default	Description
7-0	SCR	R/W	00h	Scratch register.

7.4 UART 2 Registers

7.4.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description

7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.4.2 UART 2 Configuration Registers

UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR2_EN	R/W	1	0: disable UART 2. 1: enable UART 2.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of UART 2 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 2 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR2IRQ	R/W	3h	Select the IRQ channel for UART 2.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# low when transmitting data.
3	RXW4C_IR	R/W	0	0: No reception delay when SIR is changed form TX to RX. 1: Reception delays 4 characters time when SIR is changed form TX to RX.
2	TXW4C_IR	R/W	0	0: No transmission delay when SIR is changed form RX to TX. 1: Transmission delays 4 characters time when SIR is changed form RX to TX.
1-0	Reserved	-	-	Reserved.

SIR Mode Control Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	Reserved	-	-	Reserved.
5	Reserved	-	-	Reserved.
4-3	IRMODE	R/W	00	00: disable IR function. 01: disable IR function. 10: IrDA function, active pulse is 1.6uS. 11: IrDA function, active pulse is 3/16 bit time.
2	HDUPLX	R/W	1	0: SIR is in full duplex mode for loopbak test. TXW4C_IR and RXW4C_IR are of no use. 1: SIR is in half duplex mode.
1	TXINV_IR	R/W	0	0: IRTX is in normal condition. 1: inverse the IRTX.
0	RXINV_IR	R/W	0	0: IRRX is in normal condition. 1: inverse the IRRX.

7.4.3 Device Registers

7.4.3.1 Receiver Buffer Register — Base + 0

Bit	Name	R/W	Default	Description

7-0	RBR	R	00h	The data received. Read only when LCR[7] is 0

7.4.3.2 Transmitter Holding Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	THR	W	00h	Data to be transmitted. Write only when LCR[7] is 0

7.4.3.3 Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Default	Description
7-0	DLL	R/W	01h	Baud generator divisor low byte. Access only when LCR[7] is 1.

7.4.3.4 Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Default	Description
7-0	DLM	R/W	00h	Baud generator divisor high byte. Access only when LCR[7] is 1.

7.4.3.5 Interrupt Enable Register — Base + 1

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3	EDSSI	R/W	0	Enable Modem Status Interrupt. Access only when LCR[7] is 0.
2	ELSI	R/W	0	Enable Line Status Error Interrupt. Access only when LCR[7] is 0.
1	ETBFI	R/W	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR[7] is 0.
0	ERBFI	R/W	0	Enable Received Data Available Interrupt. Access only when LCR[7] is 0.

7.4.3.6 Interrupt Identification Register — Base + 2

Bit	Name	R/W	Default	Description
7	FIFO_EN	R	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	-	Reserved.
3-1	IRQ_ID	R	000	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	1	1: Interrupt is not pending. 0: Interrupt is pending.

7.4.3.7 FIFO Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	RCV_TRIG	W	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	-	Reserved.
2	CLRTX	R	0	Reset the transmitter FIFO.
1	CLRRX	R	0	Reset the receiver FIFO.
0	FIFO_EN	R	0	0: Disable FIFO. 1: Enable FIFO.

7.4.3.8 Line Control Register — Base + 3

Bit	Name	R/W	Default	Description
7	DLAB	R/W	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	0	
3	PEN	R/W	0	
2	STB	R/W	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

7.4.3.9 MODEM Control Register — Base + 4

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	LOOP	R/W	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	0	Read from MSR[6] is loop back mode
1	RTS	R/W	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

7.4.3.10 Line Status Register — Base + 5

Bit	Name	R/W	Default	Description
7	RCR_ERR	R	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.

6	TEMT	R	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.
4	BI	R	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	0	0: Data received has no parity error. 1: Data received has parity error.
1	OE	R	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	0	0: No data is ready for read. 1: Data is received.

7.4.3.11 MODEM Status Register — Base + 6

Bit	Name	R/W	Default	Description
7	DCD	R	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR
3	DDCD	R	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	0	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	0	0: No state changed at CTS#. 1: State changed at CTS#.

7.4.3.12 Scratch Register — Base + 7

Bit	Name	R/W	Default	Description
7-0	SCR	R/W	00h	Scratch register.

7.5 Parallel Port Registers

7.5.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.5.2 Parallel Port Configuration Register

Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PRT_EN	R/W	1	0: disable Parallel Port. 1: enable Parallel Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of Parallel Port base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	78h	The LSB of Parallel Port base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELPRTIRQ	R/W	7h	Select the IRQ channel for Parallel Port.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	ECP_DMA_MODE	R/W	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	Reserved.
2-0	SELPRTDMA	R/W	011	Select the DMA channel for Parallel Port.

PRT Mode Select Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6-3	ECP_FIFO_THR	R/W	1000	ECP FIFO threshold.
2-0	PRT_MODE	R/W	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

7.5.3 Device Registers

7.5.3.1 Parallel Port Data Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	DATA	R/W	00h	The output data to drive the parallel port data lines.

7.5.3.2 ECP Address FIFO Register — Base + 0

Bit	Name	R/W	Default	Description

7-0	ECP_AFIFO	R/W	00h	Access only in ECP Parallel Port Mode and the ECP_MODE programmed in the Extended Control Register is 011. The data written to this register is placed in the FIFO and tagged as an Address/RLE. It is auto transmitted by the hardware. The operation is only defined for forward direction. It divide into two parts : Bit 7 : 0: bits 6-0 are run length, indicating how many times the next byte to appear (0 = 1time, 1 = 2times, 2 = 3times and so on). 1: bits 6-0 are a ECP address. Bit 6-0 : Address or RLE depends on bit 7.

7.5.3.3 Device Status Register — Base + 1

Bit	Name	R/W	Default	Description
7	BUSY_N	R	-	Inverted version of parallel port signal BUSY.
6	ACK_N	R	-	Version of parallel port signal ACK#.
5	PERROR	R	-	Version of parallel port signal PE.
4	SELECT	R	-	Version of parallel port signal SLCT.
3	ERR_N	R	-	Version of parallel port signal ERR#.
2-1	Reserved	R	11	Reserved. Return 11b when read.
0	TMOUT	R	-	This bit is valid only in EPP mode. Return 1 when in other modes. It indicates that a 10uS time out has occurred on the EPP bus. 0: no time out error. 1: time out error occurred, write 1 to clear.

7.5.3.4 Device Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	Reserved	-	11	Reserved. Return 11b when read.
5	DIR	R/W	0	0: the parallel port is in output mode. 1: the parallel port is in input mode. It is auto reset to 0 when in SPP mode.
4	ACKIRQ_EN	R/W	0	Enable an interrupt at the rising edge of ACK#.
3	SLIN	R/W	0	Inverted and then drives the parallel port signal SLIN#. When read, the status of inverted SLIN# is return.
2	INIT_N	R/W	0	Drives the parallel port signal INIT#. When read, the status of INIT# is return.
1	AFD	R/W	0	Inverted and then drives the parallel port signal AFD#. When read, the status of inverted AFD# is return.
0	STB	R/W	0	Inverted and then drives the parallel port signal STB#. When read, the status of inverted STB# is return.

7.5.3.5 EPP Address Register — Base + 3

Bit	Name	R/W	Default	Description
7-0	EPP_ADDR	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Address Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Address Read protocol.

7.5.3.6 EPP Data Register — Base + 4 – Base + 7

Bit	Name	R/W	Default	Description
7-0	EPP_DATA	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Data Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Data Read protocol.

7.5.3.7 Parallel Port Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	C_FIFO	R/W	00h	Data written to this FIFO is auto transmitted by the hardware to the device by using standard parallel port protocol. It is only valid in ECP and the ECP_MODE is 010b.The operation is only for forward direction.

7.5.3.8 ECP Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	ECP_DFIFO	R/W	00h	Data written to this FIFO when DIR is 0 is auto transmitted by the hardware to the device by using ECP parallel port protocol. Data is auto read from device into the FIFO when DIR is 1 by the hardware by using ECP parallel port protocol. Read the FIFO will return the content to the system. It is only valid in ECP and the ECP_MODE is 011b.

7.5.3.9 ECP Test FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	T_FIFO	R/W	00h	Data may be read, written from system to the FIFO in any Direction. But no hardware handshake occurred on the parallel port lines. It could be used to test the empty, full and threshold of the FIFO. It is only valid in ECP and the ECP_MODE is 110b.

7.5.3.10 ECP Configuration Register A — Base + 400h

Bit	Name	R/W	Default	Description

7	IRQ_MODE	R	0	0: interrupt is ISA pulse. 1: interrupt is ISA level. Only valid in ECP and ECP_MODE is 111b.
6-4	IMPID	R	001	000: the design is 16-bit implementation. 001: the design is 8-bit implementation (default). 010: the design is 32-bit implementation. 011-111: Reserved. Only valid in ECP and ECP_MODE is 111b.
3	Reserved	-	-	Reserved.
2	BYTETRAN_N	R	1	0: when transmitting there is 1 byte waiting in the transceiver that does not affect the FIFO full condition. 1: when transmitting the state of the full bit includes the byte being transmitted. Only valid in ECP and ECP_MODE is 111b.
1-0	Reserved	R	00	Return 00 when read. Only valid in ECP and ECP_MODE is 111b.

7.5.3.11 ECP Configuration Register B — Base + 401h

Bit	Name	R/W	Default	Description
7	COMP	R	0	0: only send uncompressed data. 1: compress data before sending. Only valid in ECP and ECP_MODE is 111b.
6	Reserved	R	1	Reserved. Return 1 when read. Only valid in ECP and ECP_MODE is 111b.
5-3	ECP_IRQ_CH	R	001	000: the interrupt selected with jumper. 001: select IRQ 7 (default). 010: select IRQ 9. 011: select IRQ 10. 100: select IRQ 11. 101: select IRQ 14. 110: select IRQ 15. 111: select IRQ 5. Only valid in ECP and ECP_MODE is 111b.
2-0	ECP_DMA_CH	R	011	Return the DMA channel of ECP parallel port. Only valid in ECP and ECP_MODE is 111b.

7.5.3.12 Extended Control Register — Base + 402h

Bit	Name	R/W	Default	Description

7-5	ECP_MODE	R/W	000	000: SPP Mode. 001: PS/2 Parallel Port Mode. 010: Parallel Port Data FIFO Mode. 011: ECP Parallel Port Mode. 100: EPP Mode. 101: Reserved. 110: Test Mode. 111: Configuration Mode. Only valid in ECP.
4	ERRINTR_EN	R/W	0	0: disable the interrupt generated on the falling edge of ERR#. 1: enable the interrupt generated on the falling edge of ERR#.
3	DAMEN	R/W	0	0: disable DMA. 1: enable DMA. DMA starts when SERVICEINTR is 0.
2	SERVICEINTR	R/W	1	0: enable the following case of interrupt. DMAEN = 1: DMA mode. DMAEN = 0, DIR = 0: set to 1 whenever there are writeIntrThreshold or more bytes are free in the FIFO. DMAEN = 0, DIR = 0: set to 1 whenever there are readIntrThreshold or more bytes are valid to be read in the FIFO.
1	FIFOFULL	R	0	0: The FIFO has at least 1 free byte. 1: The FIFO is completely full.
0	FIFOEMPTY	R	0	0: The FIFO contains at least 1 byte. 1: The FIFO is completely empty.

7.6 Hardware Monitor Registers

7.6.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description

7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.6.2 Hardware Monitor Configuration Registers

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	0	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

7.6.3 Device Registers

7.6.3.1 START_STOP Control Register — Index 00h

Bit	Name	R/W	Default	Description
7	INIT	R/W	0	Set one restores power on default value to all registers. This bit clears itself since the power on default is zero.
6	SOFT_PWDN	R/W	0	Set this bit to 1 will power down A/D converter circuit. Default is 0.
5-1	Reserved	-	-	Reserved
0	START	R/W	1	A one enables startup of monitoring operations; a zero puts the part in standby mode.

7.6.3.2 Temperature Mode Control Register — Index 01h

Bit	Name	R/W	Default	Description
7-6	Temperature Fault Queue	R/W	00	This value stands for how many times of successive temperature fault can be tolerated. 00: 1 times. 01: 2 times. 10: 4 times. 11: 8 times.
5-4	Reserved	-	-	Reserved
3	COMB_LEVEL	R/W	1	Set to 1, enable COMB filter. Set to 0, disable COMB filter. COMB filter is only applied to BJT thermal diode mode. If temperature select thermistor mode, the COMB filter will not work on it.
2	T3_MODE	R/W	1	Set to 1, select T3 as connected to a BJT thermal diode. At this mode, T3 detected temperature ranges from 0°C ~ 140°C, not considering the T3OFFSET(index 92h) effect. Set to 0, select T3 as connected to a thermistor. At this mode, T3 detected temperature ranges from 0°C ~ 127°C, not considering the T3OFFSET(index 92h) effect.
1	T2_MODE	R/W	1	Set to 1, select T2 as connected to a BJT thermal diode. At this mode, T2 detected temperature ranges from 0°C ~ 140°C, not considering the T2OFFSET(index 91h) effect. Set to 0, select T2 as connected to a thermistor. At this mode, T2 detected temperature ranges from 0°C ~ 127°C, not considering the T2OFFSET(index 91h) effect.
0	T1_MODE	R/W	1	Set to 1, select T1 as connected to a BJT thermal diode. At this mode, T1 detected temperature ranges from 0°C ~ 140°C, not considering the T1OFFSET(index 90h) effect. Set to 0, select T1 as connected to a thermistor. At this mode, T1 detected temperature ranges from 0°C ~ 127°C, not considering the T1OFFSET(index 90h) effect.

7.6.3.3 ADC_CLK Frequency Control Register — Index 02h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved

1-0	ADC_CLK_SEL	R/W	00	Select ADC clock frequency. 00 : 12.8K(Default) 01 : 6.4K 10 : 3.2K 11 : 1.6K

7.6.3.4 External BJT Offset Register — Index 09h

Bit	Name	R/W	Default	Description
7-0	Reserved	R/W	37h	

7.6.3.5 FAN1 Full Speed Count Register 0 — Index 0Ah

Bit	Name	R/W	Default	Description
7-0	F1_FULL(MSB)	R	00h	When power on, the FANPWM1 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN after power on, the PWMOUT1 will keep outputting FFh duty cycle.

7.6.3.6 FAN1 Full speed Count Register 1— Index 0Bh

Bit	Name	R/W	Default	Description
7-0	F1_FULL(LSB)	R	FFh	When power on, the FANPWM1 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN after power on, the PWMOUT1 will keep outputting FFh duty cycle.

7.6.3.7 FAN2 Full Speed Count Register 0 — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	F2_FULL(MSB)	R	0Fh	When power on, the FANPWM2 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN2 after power on, the PWMOUT2 will keep outputting FFh duty cycle.

7.6.3.8 FAN2 Full speed Count Register 1— Index 0Dh

Bit	Name	R/W	Default	Description
7-0	F2_FULL(LSB)	R	FFh	When power on, the FANPWM2 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN1 after power on, the PWMOUT2 will keep outputting FFh duty cycle.

7.6.3.9 FAN3 Full Speed Count Register 0 — Index 0Eh

Bit	Name	R/W	Default	Description
7-0	F3_FULL(MSB)	R	0Fh	When power on, the FANPWM3 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN2 after power on, the PWMOUT3 will keep outputting FFh duty cycle.

7.6.3.10 FAN3 Full speed Count Register 1— Index 0Fh

Bit	Name	R/W	Default	Description
7-0	F3_FULL(LSB)	R	FFh	When power on, the FANPWM3 will output full duty cycle (FFh) to enable system FAN. After 10 seconds **when detecting FANIN signal**, assuming the fan has been fully turned on, the fan speed count detected will be recorded in the register. If there is no signal on FANIN3 after power on, the PWMOUT3 will keep outputting FFh duty cycle.

7.6.3.11 Value RAM — Index 10h - 2Fh, 40h - 59h

In the following table, the unit of voltage reading/limit is 8mV. The unit of temperature reading/limit is 1°C.

Address 10-3F	R/W	Description
0Ah	RO	FAN1 full speed count reading [11:8]
0Bh	RO	FAN1 full speed count reading [7:0]
0Ch	RO	FAN2 full speed count reading [11:8]
0Dh	RO	FAN2 full speed count reading [7:0]
0Eh	RO	FAN3 full speed count reading [11:8]
0Fh	RO	FAN3 full speed count reading [7:0]
10h	RO	VCC reading. This reading is the divided voltage of VCC inside the chip.
11h	RO	VIN1 reading.
12h	RO	VIN2 reading.
13h	RO	VIN3 reading.
14h	RO	VIN4 reading.
15h	RO	VIN5 reading.
16h	RO	VIN6 reading.
17h	RO	VIN7 reading.
18h	RO	VIN8 reading.
19h	RO	VSB reading. This reading is the divided voltage of VSB inside the chip.
1Ah	RO	VBAT reading. This reading is the divided voltage of VBAT inside the chip.
1Bh	RO	T1 temperature reading.
1Ch	RO	T2 temperature reading.
1Dh	RO	T3 temperature reading.
1Eh		Reserved
20h	RO	FAN1 count reading (MSB)
21h	RO	FAN1 count reading (LSB)
22h	RO	FAN2 count reading (MSB)
23h	RO	FAN2 count reading (LSB)
24h	RO	FAN3 count reading (MSB)
25h	RO	FAN3 count reading (LSB)
26h ~ 27h		Reserved

28h	R/W	FAN1 count limit. (MSB)
29h	R/W	FAN1 count limit. (LSB)
2Ah	R/W	FAN2 count limit. (MSB)
2Bh	R/W	FAN2 count limit. (LSB).
2Ch	R/W	FAN3 count limit. (MSB)
2Dh	R/W	FAN3 count limit. (LSB)
2Eh	R/W	VBAT high limit. This limit should correspond to the divided voltage.
2Fh	R/W	VBAT low limit. This limit should correspond to the divided voltage.
40h	R/W	VCC high limit. This limit should correspond to the divided voltage.
41h	R/W	VCC low limit. This limit should correspond to the divided voltage.
42h	R/W	VIN1 high limit.
43h	R/W	VIN1 low limit.
44h	R/W	VIN2 high limit.
45h	R/W	VIN2 low limit.
46h	R/W	VIN3 high limit.
47h	R/W	VIN3 low limit.
48h	R/W	VIN4 high limit.
49h	R/W	VIN4 low limit.
4Ah	R/W	VIN5 high limit.
4Bh	R/W	VIN5 low limit.
4Ch	R/W	VIN6 high limit.
4Dh	R/W	VIN6 low limit.
4Eh	R/W	VIN7 high limit.
4Fh	R/W	VIN7 low limit.
50h	R/W	VIN8 high limit.
51h	R/W	VIN8 low limit.
52h	R/W	VSB high limit. This limit should correspond to the divided voltage.
53h	R/W	VSB low limit. This limit should correspond to the divided voltage.
54h	R/W	T1 high limit.
55h	R/W	T1 low limit.
56h	R/W	T2 high limit.
57h	R/W	T2 low limit.
58h	R/W	T3 high limit.
59h	R/W	T3 low limit.

7.6.3.12 INTERRUPT ENABLE Control Register 1 — Index 30h

Bit	Name	R/W	Default	Description
7	EN_VIN7	R/W	0	Set to 1, enables VIN7 abnormal interrupt.
6	EN_VIN6	R/W	0	Set to 1, enables VIN6 abnormal interrupt.
5	EN_VIN5	R/W	0	Set to 1, enables VIN5 abnormal interrupt.
4	EN_VIN4	R/W	0	Set to 1, enables VIN4 abnormal interrupt.
3	EN_VIN3	R/W	0	Set to 1, enables VIN3 abnormal interrupt.
2	EN_VIN2	R/W	0	Set to 1, enables VIN2 abnormal interrupt.
1	EN_VIN1	R/W	0	Set to 1, enables VIN1 abnormal interrupt.
0	EN_3VDD	R/W	0	Set to 1, enables 3VDD abnormal interrupt.

7.6.3.13 INTERRUPT ENABLE Control Register 2 — Index 31h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	
5	EN_T3	R/W	0	Set to 1, enables T3 abnormal interrupt.
4	EN_T2	R/W	0	Set to 1, enables T2 abnormal interrupt.
3	EN_T1	R/W	0	Set to 1, enables T1 abnormal interrupt.
2	EN_VBAT	R/W	0	Set to 1, enables VBAT abnormal interrupt.
1	EN_VSB	R/W	0	Set to 1, enables VSB abnormal interrupt.
0	EN_VIN8	R/W	0	Set to 1, enables VIN8 abnormal interrupt.

7.6.3.14 INTERRUPT ENABLE Control Register 3 — Index 32h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	
6	EN_CASE	R/W	0	Set to 1, enables Chassis Open interrupt.
5	EN_FAN3_TAR	R/W	0	Set to 1, enables FAN3 target speed mismatched interrupt when FANPWM3 duty-cycle is 100%.
4	EN_FAN2_TAR	R/W	0	Set to 1, enables FAN2 target speed mismatched interrupt when FANPWM2 duty-cycle is 100%.
3	EN_FAN1_TAR	R/W	0	Set to 1, enables FAN1 target speed mismatched interrupt when FANPWM1 duty-cycle is 100%.
2	EN_FAN3_LMT	R/W	0	Set to 1, enables FAN3 abnormal interrupt.
1	EN_FAN2_LMT	R/W	0	Set to 1, enables FAN2 abnormal interrupt.
0	EN_FAN1_LMT	R/W	0	Set to 1, enables FAN1 abnormal interrupt.

7.6.3.15 INTERRUPT STATUS Register 1 — Index 33h

Bit	Name	R/W	Default	Description
7	VIN7_STS	R/W	0	A one indicates VIN7 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
6	VIN6_STS	R/W	0	A one indicates VIN6 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
5	VIN5_STS	R/W	0	A one indicates VIN5 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
4	VIN4_STS	R/W	0	A one indicates VIN4 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
3	VIN3_STS	R/W	0	A one indicates VIN3 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
2	VIN2_STS	R/W	0	A one indicates VIN2 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
1	VIN1_STS	R/W	0	A one indicates VIN1 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
0	3VDD_STS	R/W	0	A one indicates 3VDD reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.

7.6.3.16 INTERRUPT STATUS Register 2 — Index 34h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	
5	T3_STS	R/W	0	A one indicates T3 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
4	T2_STS	R/W	0	A one indicates T2 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
3	T1_STS	R/W	0	A one indicates T1 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
2	VBAT_STS	R/W	0	A one indicates VBAT reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
1	VSB_STS	R/W	0	A one indicates VSB reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
0	VIN8_STS	R/W	0	A one indicates VIN8 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.

7.6.3.17 INTERRUPT STATUS Register 3 — Index 35h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	
6	CASEOPEN		0	A one indicates that Chassis has been opened.
5	FAN3_TAR_STS	R/W	0	A one indicates FAN3 can not reach the expect count in time. The time is defined by FAN3 Fault Time registers.
4	FAN2_TAR_STS	R/W	0	A one indicates FAN2 can not reach the expect count in time. The time is defined by FAN2 Fault Time registers.
3	FAN1_TAR_STS	R/W	0	A one indicates FAN1 can not reach the expect count in time. The time is defined by FAN1 Fault Time registers.
2	FAN3_STS	R/W	0	A one indicates FAN3 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	0	A one indicates FAN2 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	0	A one indicates FAN1 reaches its high or low limit. Write 1 to clear this bit, write 0 will be ignored.

7.6.3.18 REAL_TIME STATUS Register 1 — Index 36h

Bit	Name	R/W	Default	Description
7	VIN7_RT	R	0	A one indicates VIN7 is at abnormal range.
6	VIN6_RT	R	0	A one indicates VIN6 is at abnormal range.
5	VIN5_RT	R	0	A one indicates VIN5 is at abnormal range.
4	VIN4_RT	R	0	A one indicates VIN4 is at abnormal range.
3	VIN3_RT	R	0	A one indicates VIN3 is at abnormal range.
2	VIN2_RT	R	0	A one indicates VIN2 is at abnormal range.
1	VIN1_RT	R	0	A one indicates VIN1 is at abnormal range.

0	3VDD_RT	R	0	A one indicates 3VDD is at abnormal range.

7.6.3.19 REAL_TIME STATUS Register 2 — Index 37h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	
5	T3_RT	R	0	A one indicates T3 exceeds its high limit.
4	T2_RT	R	0	A one indicates T2 exceeds its high limit.
3	T1_RT	R	0	A one indicates VBAT exceeds its high limit.
2	VBAT_RT	R	0	A one indicates VBAT exceeds its high limit.
1	VSB_RT	R	0	A one indicates VSB exceeds its high limit.
0	VIN8_RT	R	0	A one indicates VIN8 exceeds its high limit.

7.6.3.20 REAL_TIME STATUS Register 3 — Index 38h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	
6	CASEOPEN	R	0	A one indicates that chassis is opened.
5	FAN3_TAR_RT	R	0	A one indicates FAN3 can not reach the expect count in time when FANPWM3 duty-cycle is 100%. The time is defined by FAN3 Fault Time registers. After FAN3 reaches the expect count, the bit will be set to 0.
4	FAN2_TAR_RT	R	0	A one indicates FAN2 can not reach the expect count in time when FANPWM2 duty-cycle is 100%. The time is defined by FAN2 Fault Time registers. After FAN2 reaches the expect count, the bit will be set to 0.
3	FAN1_TAR_RT	R	0	A one indicates FAN1 can not reach the expect count in time when FANPWM1 duty-cycle is 100%. The time is defined by FAN1 Fault Time registers. After FAN1 reaches the expect count, the bit will be set to 0.
2	FAN3_RT	R	0	A one indicates FAN3 is at abnormal range.
1	FAN2_RT	R	0	A one indicates FAN2 is at abnormal range.
0	FAN1_RT	R	0	A one indicates FAN1 is at abnormal range.

7.6.3.21 VIN_FAULT Mode Register 3 — Index 39h

Bit	Name	R/W	Default	Description
7	VIN7F_SEL	R/W	0	Set to 1, VIN7_ID value will not change until REG 3Ah Bit7 is cleared if that bit is set. Set to 0, Reserved.
6-4	Reserved	-	-	
3	VIN4F_SEL	R	0	Set to 1, once VIN4_FAULT is asserted, it will not be de-asserted when VIN4 is back to normal range. Set to 0, VIN4_FAULT is asserted/de-asserted according to its value whether is out of high/low limit.
2	VIN3F_SEL	R	0	Set to 1, once VIN3_FAULT is asserted, it will not be de-asserted when VIN4 is back to normal range. Set to 0, VIN3_FAULT is asserted/de-asserted according to its value whether is out of high/low limit.

1	VIN2F_SEL	R	0	Set to 1, once VIN2_FAULT is asserted, it will not be de-asserted when VIN4 is back to normal range. Set to 0, VIN2_FAULT is asserted/de-asserted according to its value whether is out of high/low limit.
0	VIN1F_SEL	R	0	Set to 1, once VIN1_FAULT is asserted, it will not be de-asserted when VIN4 is back to normal range. Set to 0, VIN1_FAULT is asserted/de-asserted according to its value whether is out of high/low limit.

7.6.3.22 VIN_FAULT STATUS Register — Index 3Ah

Bit	Name	R/W	Default	Description
7	STS_VIN7_CHG	R/W	0	Reserved
6-4	Reserved	-	-	
3	STS_VIN4_FAULT	R/W	0	Read one indicates that VIN4 is out of its high/low limit. Write 1 to clear this status.
2	STS_VIN3_FAULT	R/W	0	Read one indicates that VIN3 is out of its high/low limit. Write 1 to clear this status.
1	STS_VIN2FAULT	R/W	0	Read one indicates that VIN2 is out of its high/low limit. Write 1 to clear this status.
0	STS_VIN1_FAULT	R/W	0	Read one indicates that VIN1 is out of its high/low limit. Write 1 to clear this status.

7.6.3.23 T_FAULT Control Register — Index 3Bh

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	
2	EN_T3_FAULT	R/W	0	Set to 1, enable temperature 3(VT3)fault through pin OVT_N.
1	EN_T2_FAULT	R/W	0	Set to 1, enable temperature 2(VT2) fault through pin OVT_N.
0	EN_T1_FAULT	R/W	1	Set to 1, enable temperature 1(VT1) fault through pin OVT_N.

7.6.3.24 Case Open Status Clear Register — Index 3Ch

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	
0	CLR_INTRUDE	W	0	Write 1 to clear the latched CASEOPEN event status.

7.6.3.25 BEEP Control Register 1 — Index 3Dh

Bit	Name	R/W	Default	Description
7	EN_VIN7_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN7 abnormal event. Write 0 to disable it.
6	EN_VIN6_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN6 abnormal event. Write 0 to disable it.
5	EN_VIN5_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN5 abnormal event. Write 0 to disable it.
4	EN_VIN4_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN4 abnormal event. Write 0 to disable it.

3	EN_VIN3_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN3 abnormal event. Write 0 to disable it.
2	EN_VIN2_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN2 abnormal event. Write 0 to disable it.
1	EN_VIN1_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN1 abnormal event. Write 0 to disable it.
0	EN_VCC_BEEP	R/W	0	Write 1 to enable the beep alarm for 3VDD abnormal event. Write 0 to disable it.

7.6.3.26 BEEP Control Register 2 — Index 3Eh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	
5	EN_T3_BEEP	R/W	0	Write 1 to enable the beep alarm for T3 abnormal event. Write 0 to disable it
4	EN_T2_BEEP	R/W	0	Write 1 to enable the beep alarm for T2 abnormal event. Write 0 to disable it
3	EN_T1_BEEP	R/W	0	Write 1 to enable the beep alarm for T1 abnormal event. Write 0 to disable it
2	EN_VBAT_BEEP	R/W	0	Write 1 to enable the beep alarm for VBAT abnormal event. Write 0 to disable it
1	EN_VIN7_BEEP	R/W	0	Write 1 to enable the beep alarm for VSB abnormal event. Write 0 to disable it
0	EN_VIN8_BEEP	R/W	0	Write 1 to enable the beep alarm for VIN8 abnormal event. Write 0 to disable it

7.6.3.27 BEEP Control Register 3 — Index 3Fh

Bit	Name	R/W	Default	Description
7	Reserved	-	-	
6	EN_CASE_BEEP	R/W	0	Write 1 to enable the beep alarm for CASEOPEN abnormal event. Write 0 to disable it
5	EN_FAN3_TAR_ BEEP	R/W	0	Write 1 to enable the beep alarm for FAN3 target-not-reached event. Write 0 to disable it
4	EN_FAN2_TAR_ BEEP	R/W	0	Write 1 to enable the beep alarm for FAN2 target-not-reached event. Write 0 to disable it
3	EN_FAN1_TAR_BEE P	R/W	0	Write 1 to enable the beep alarm for FAN1 target-not-reached event. Write 0 to disable it
2	EN_FAN3_LMT_BEE P	R/W	0	Write 1 to enable the beep alarm for FAN3 under-limit event. Write 0 to disable it
1	EN_FAN2_LMT_BEE P	R/W	0	Write 1 to enable the beep alarm for FAN2 under-limit event. Write 0 to disable it
0	EN_FAN1_LMT_BEE P	R/W	0	Write 1 to enable the beep alarm for FAN1 under-limit event. Write 0 to disable it

7.6.3.28 FAN1 OPERATING Control Register -- Index 60h

Bit	Name	R/W	Default	Description
7	FAN1_SKIP	R	-	When this bit is set to 1, FAN1 is not monitored. When this bit is set to 0, FAN1 is monitored.
6	Reserved	-	-	
5	FAN1_FORCE_MONI TOR	R/W	0	Set to 1, FAN1 speed is monitored every monitor cycle even the fan is stopped. Set to 0, FAN1 speed will not be monitored at the next monitor cycle if the fan is stopped.

4	FAN1_DC_MODE	R/W	0	Set to 1, FAN1 control is set to DC mode. Set to 0, FAN1 control is set to PWM duty-cycle mode.
3	F1_LATCH_FULL	R/W	0	Set to 1, current FAN1 COUNT will be bypass to FAN1_FULL_SPEED.
2	F1_KEEP_STOP	R/W	0	Set to 1, keep FANPWM1 duty-cycle decrease to STOP DUTY and hold.
1-0	F1_MODE	R/W	00	**00:** FAN1 operates in **SPEED** mode. FANPWM duty-cycle is automatically adjusted according to FAN EXPECT register. **01:** FAN1 operates in **TEMPERATURE** mode. FANPWM duty-cycle is automatically adjusted according to current temperature, **1x:** FAN1 operates in **MANUAL** mode. Software set the FANPWM duty-cycle directly.

7.6.3.29 FANPWM1 START UP DUTY-CYCLE — Index 61h

Bit	Name	R/W	Default	Description
7-0	F1_START_DUTY[9:2]	R/W	30h	FANPWM1 will increasing duty-cycle from 0 to this valuedirectly.

7.6.3.30 FANPWM1 STOP DUTY-CYCLE — Index 62h

Bit	Name	R/W	Default	Description
7-0	F1_STOP_DUTY[9:2]	R/W	25h	FANPWM1 will decreasing duty-cycle to 0 from this value directly or keep duty-cycle in this value when FAN1_KEEP_STOP set to 1.

7.6.3.31 FANPWM1 Output Frequency Control — Index 63h

Bit	Name	R/W	Default	Description
7	PWM1_DIV[7]	R/W	80h	Set to 1, PRECLK(Pre-Clock) = 48M Hz ; Set to 0, PRECLK = 1M Hz .
6-0	PWM1_DIV[6:0]	R/W		Pre-divisor of PRECLK.

FANPWM1 output frequency = $\frac{PRECLK}{(\Pr e\text{-}divisor) * 256}$

So, PWM frequency ranges from 30.5Hz~187.5KHz

7.6.3.32 FANPWM1 STEP Control Register -- Index 64h

Bit	Name	R/W	Default	Description
7-4	F1_UP_STEP	R/W	00h	This value determines the increasing speed of PWM1_DUTY.
3-0	F1_DOWN_STEP	R/W		This value determines the decreasing speed of PWM1_DUTY.

7.6.3.33 FAN1_FAULT TIME Register — Index 65h

Bit	Name	R/W	Default	Description

7-0	F1_FAULT_TIME	R/W	03h	This register determines the time for fan to chase to the expect speed. Two conditions cause fan fault event: (1). When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in the time. (2). When PWM_Duty reaches 00h, if the fan speed count can't reach the fan expect count in the time. The unit of this register is 1 second. The default value is 3 seconds.

7.6.3.34 FAN1 Expect count Register---Index 69h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	00h	
3-0	F1_EXPECT (MSB)	R		User expect fan1 count value, program this register to control the expect fan1 speed

7.6.3.35 FAN1 Expect count Register-- Index 6Ah

PBit	Name	R/W	Default	Description
7-0	F1_EXPECT (LSB)	R	00h	User expect fan1 count value, program this register to control the expect fan1 speed.

7.6.3.36 FAN1 PWM_DUTY -- Index 6Bh

Bit	Name	R/W	Default	Description
7-0	PWM_DUTY1	R/W	FFh	When FAN1 control is at PWM Duty-cycle mode, this value represents the duty-cycle. When FAN1 control is at DC mode, this value represents the DC voltage output. Each step (LSB) is VCC / 256. This register is programmable at Manual mode. At SPEED or TEMPERATURE mode, this register reflects current FANPWM1 duty-cycle.

7.6.3.37 FAN2 OPERATING Control Register -- Index 70h

Bit	Name	R/W	Default	Description
7	FAN2_SKIP	R	-	When this bit is set to 1, FAN2 is not monitored. When this bit is set to 0, FAN2 is monitored.
6	Reserved	-	-	Reserved.
5	FAN2_FORCE_MONITOR	R/W	0	Set to 1, FAN2 speed is monitored every monitor cycle even the fan is stopped. Set to 0, FAN2 speed will not be monitored at the next monitor cycle if the fan is stopped.
4	FAN2_DC_MODE	R/W	0	Set to 1, FAN2 control is set to DC mode. Set to 0, FAN2 control is set to PWM duty-cycle mode.
3	F2_LATCH_FULL	R/W	0	Set to 1, current FAN2 COUNT will be bypass to F2_FULL_SPEED.
2	F2_KEEP_STOP	R/W	0	Set to 1, keep FANPWM2 duty-cycle decrease to STOP DUTY and hold.

1-0	F2_MODE	R/W	00	**00:** FAN2 operates in **SPEED** mode. FANPWM duty-cycle is automatically adjusted according to FAN EXPECT register. **01:** FAN2 operates in **TEMPERATURE** mode. FANPWM duty-cycle is automatically adjusted according to current temperature, **1x:** FAN2 operates in **MANUAL** mode. Software set the FANPWM duty-cycle directly.

7.6.3.38 FANPWM2 START UP DUTY-CYCLE — Index 71h

Bit	Name	R/W	Default	Description
7-0	F2_START_DUTY	R/W	30h	FANPWM2 will increase duty-cycle from 0 to this value directly.

7.6.3.39 FANPWM2 STOP DUTY-CYCLE — Index 72h

Bit	Name	R/W	Default	Description
7-0	F2_STOP_DUTY	R/W	25h	FANPWM2 will decreasing duty-cycle to 0 from this value directly or keep duty-cycle in this value when F2_KEEP_STOP set to 1.

7.6.3.40 FANPWM2 Output Frequency Control — Index 73h

Bit	Name	R/W	Default	Description
7	PWM2_DIV[7]	R/W	80h	Set to 1, PRECLK(Pre-Clock) = 48M Hz ; Set to 0, PRECLK = 1M Hz .
6-0	PWM2_DIV[6:0]	R/W		Pre-divisor of PRECLK.

FANPWM2 output frequency = $\frac{PRECLK}{(\Pr e - divisor) * 256}$

So, PWM frequency ranges from 30.5Hz~187.5KHz

7.6.3.41 FANPWM2 STEP Control Register -- Index 74h

Bit	Name	R/W	Default	Description
7-4	F2_UP_STEP	R/W	00h	This value determines the increasing speed of PWM2_DUTY.
3-0	F2_DOWN_STEP	R/W		This value determines the decreasing speed of PWM2_DUTY

7.6.3.42 FAN2_FAULT TIME Register — Index 75h

Bit	Name	R/W	Default	Description
7-0	F2_FAULT_TIME	R/W	03h	This register determines the time for fan to chase to the expect speed. Two conditions cause fan fault event: (1). When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in the time. (2). When PWM_Duty reaches 00h, if the fan speed count can't reach the fan expect count in the time. The unit of this register is 1 second. The default value is 180 seconds.

7.6.3.43 FAN2 Expect count Register-- Index 79h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	00h	
3-0	F2_EXPECT (MSB)	R		User expect fan2 count value, program this register to control the expect fan2 speed

7.6.3.44 FAN2 Expect count Register-- Index 7Ah

Bit	Name	R/W	Default	Description
7-0	F2_EXPECT (LSB)	R	00h	User expect fan2 count value, program this register to control the expect fan2 speed.

7.6.3.45 FAN2 PWM_DUTY -- Index 7Bh

Bit	Name	R/W	Default	Description
7-0	PWM_DUTY2	R/W	FFh	When FAN2 control is at PWM Duty-cycle mode, this value represents the duty-cycle. When FAN2 control is at DC mode, this value represents the DC voltage output. Each step (LSB) is VCC / 256. This register is programmable at Manual mode. At SPEED or TEMPERATURE mode, this register reflects current FANPWM1 duty-cycle.

7.6.3.46 FAN3 OPERATING Control Register -- Index 80h

Bit	Name	R/W	Default	Description
7	FAN3_SKIP	R	-	When this bit is set to 1, FAN3 is not monitored. When this bit is set to 0, FAN3 is monitored.
6	Reserved	-	-	
5	FAN3_FORCE_MONITOR	R/W	0	Set to 1, FAN3 speed is monitored every monitor cycle even the fan is stopped. Set to 0, FAN3 speed will not be monitored at the next monitor cycle if the fan is stopped.
4	FAN3_DC_MODE	R/W	0	Set to 1, FAN3 control is set to DC mode. Set to 0, FAN3 control is set to PWM duty-cycle mode.
3	F3_LATCH_FULL	R/W	0	Set to 1, current FAN3 COUNT will be bypass to F3_FULL_SPEED.
2	F3_KEEP_STOP	R/W	0	Set to 1, keep FANPWM3 duty-cycle decrease to STOP DUTY and hold.
1-0	F3_MODE	R/W	00	**00:** FAN3 operates in **SPEED** mode. FANPWM3 duty-cycle is automatically adjusted according to FAN EXPECT register. **01:** FAN3 operates in **TEMPERATURE** mode. FANPWM3 duty-cycle is automatically adjusted according to current temperature, **1x:** FAN3 operates in **MANUAL** mode. Software set the FANPWM3 duty-cycle directly.

7.6.3.47 FANPWM3 START UP DUTY-CYCLE — Index 81h

Bit	Name	R/W	Default	Description
7-0	F3_START_DUTY	R/W	30h	FANPWM3 will increase duty-cycle from 0 to this value directly.

7.6.3.48 FANPWM3 STOP DUTY-CYCLE — Index 82h

Bit	Name	R/W	Default	Description
7-0	F3_STOP_DUTY	R/W	25h	FANPWM3 will decreasing duty-cycle to 0 from this value directly or keep duty-cycle in this value when F3_KEEP_STOP set to 1.

7.6.3.49 FANPWM3 Output Frequency Control — Index 83h

Bit	Name	R/W	Default	Description
7	PWM3_DIV[7]	R/W	80h	Set to 1, PRECLK(Pre-Clock) = 48M Hz ; Set to 0, PRECLK = 1M Hz .
6-0	PWM3_DIV[6:0]	R/W		Pre-divisor of PRECLK.

FANPWM3 output frequency = $\frac{PRECLK}{(\Pr e - divisor) * 256}$

So, PWM frequency ranges from 30.5Hz~187.5KHz

7.6.3.50 FANPWM3 STEP Control Register -- Index 84h

Bit	Name	R/W	Default	Description
7-4	F3_UP_STEP	R/W	00h	This value determines the increasing speed of PWM3_DUTY.
3-0	F3_DOWN_STEP	R/W		This value determines the decreasing speed of PWM3_DUTY

7.6.3.51 FAN3_FAULT TIME Register — Index 85h

Bit	Name	R/W	Default	Description
7-0	F3_FAULT_TIME	R/W	03h	This register determines the time for fan to chase to the expect speed. Two conditions cause fan fault event: (1). When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in the time. (2). When PWM_Duty reaches 00h, if the fan speed count can't reach the fan expect count in the time. The unit of this register is 1 second. The default value is 180 seconds.

7.6.3.52 FAN3 Expect count Register-- Index 89h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	00h	
3-0	F3_EXPECT (MSB)	R		User expect fan3 count value, program this register to control the expect fan3 speed

7.6.3.53 FAN3 Expect count Register-- Index 8Ah

Bit	Name	R/W	Default	Description

7-0	F3_EXPECT (LSB)	R	00h	User expect fan3 count value, program this register to control the expect fan3 speed.

7.6.3.54 FAN3 PWM_DUTY -- Index 8Bh

Bit	Name	R/W	Default	Description
7-0	PWM_DUTY3	R/W	FFh	When FAN3 control is at PWM Duty-cycle mode, this value represents the duty-cycle. When FAN3 control is at DC mode, this value represents the DC voltage output. Each step (LSB) is VCC / 256. This register is programmable at Manual mode. At SPEED or TEMPERATURE mode, this register reflects current FANPWM1 duty-cycle

7.6.3.55 T1 OFFSET Register -- Index 90h

Bit	Name	R/W	Default	Description
7	Reserved	-	00h	
6-0	T1OFFSET	R/W		T1 temperature offset register. The real temperature value will be added by this offset and then will be put into temperature reading (Value RAM 1Bh). The offset ranges from -64ºC to 63ºC. 3Fh : +63ºC. 01h : +1ºC. 00h : +0ºC. 7Fh: -1ºC 7Eh: -2ºC 40h: -64ºC

7.6.3.56 T2 OFFSET Register -- Index 91h

Bit	Name	R/W	Default	Description
7	Reserved	-	00h	
6-0	T2OFFSET	R/W		T2 temperature offset register. The real temperature value will be added by this offset and then will be put into temperature reading (Value RAM 1Ch). The offset ranges from -64ºC to 63ºC. 3Fh : +63ºC. 01h : +1ºC. 00h : +0ºC. 7Fh: -1ºC 7Eh: -2ºC 40h: -64ºC

7.6.3.57 T3 OFFSET Register -- Index 92h

Bit	Name	R/W	Default	Description
7	Reserved	-	00h	

6-0	T3OFFSET	R/W		T3 temperature offset register. The real temperature value will be added by this offset and then will be put into temperature reading (Value RAM 1Dh). The offset ranges from -64ºC to 63ºC. 3Fh : +63ºC. 01h : +1ºC. 00h : +0ºC. 7Fh: -1ºC 7Eh: -2ºC 40h: -64ºC

7.6.3.58 FAN1 CONTROL v.s. TEMPERATURE 1 (INDEX A0 -- AD registers)

T1 BOUNDARY 1 TEMPERATURE – Index A0h

Bit	Name	R/W	Default	Description
7-0	T1_TP_1	R/W	00h	The 1st BOUNDARY temperature for T1 in temperature mode. When T1 temperature is **exceed** this boundary, FAN1 segment **1** speed count registers will be loaded into FAN1 expect count registers. When T1 temperature is **below** this boundary, FAN1 segment **2** speed count registers will be loaded into FAN1 expect count registers.

T1 BOUNDARY 5 TEMPERATURE – Index A1h

Bit	Name	R/W	Default	Description
7-0	T1_TP_5	R/W	00h	The 5th BOUNDARY temperature for T1 in temperature mode. When T1 temperature is **exceed** this boundary, FAN1 segment 5 speed count registers will be loaded into FAN1 expect count registers. When T1 temperature is **below** this boundary, FAN1 segment 6 speed count registers will be loaded into FAN1 expect count registers.

T1 BOUNDARY 9 TEMPERATURE – Index A2h

Bit	Name	R/W	Default	Description
7-0	T1_TP_9	R/W	00h	The 9th BOUNDARY temperature for T1 in temperature mode. When T1 temperature is **exceed** this boundary, FAN1 segment 9 speed count registers will be loaded into FAN1 expect count registers. When T1 temperature is **below** this boundary, FAN1 segment 10 speed count registers will be loaded into FAN1 expect count registers.

FAN1 SEGMENT 1 SPEED COUNT (MSB) – Index A4h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T1_SP_1_MSB	R/W		The MSB of 1st expected fan speed for FAN1 in temperature mode.

FAN1 SEGMENT 1 SPEED COUNT (LSB) – Index A5h

Bit	Name	R/W	Default	Description
7-0	T1_SP_1_LSB	R/W	FFh	The LSB of 1st expected fan speed for FAN1 in temperature mode.

FAN1 SEGMENT 5 SPEED COUNT (MSB) – Index A6h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T1_SP_5_MSB	R/W		The MSB of 5th expected fan speed for FAN1 in temperature mode.

FAN1 SEGMENT 5 SPEED COUNT (LSB) – Index A7h

Bit	Name	R/W	Default	Description
7-0	T1_SP_5_LSB	R/W	FFh	The LSB of 5th expected fan speed for FAN1 in temperature mode.

FAN1 SEGMENT 9 SPEED COUNT (MSB) – Index A8h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T1_SP_9_MSB	R/W		The MSB of 9th expected fan speed for FAN1 in temperature mode.

FAN1 SEGMENT 9 SPEED COUNT (LSB) – Index A9h

Bit	Name	R/W	Default	Description
7-0	T1_SP_9_LSB	R/W	FFh	The LSB of 9th expected fan speed for FAN1 in temperature mode.

7.6.3.59 FAN2 CONTROL v.s. TEMPERATURE 2 (INDEX B0 -- BD registers)

T2 BOUNDARY 1 TEMPERATURE – Index B0h

Bit	Name	R/W	Default	Description
7-0	T2_TP_1	R/W	00h	The 1st BOUNDARY temperature for T2 in temperature mode. When T2 temperature is **exceed** this boundary, FAN2 segment **1** speed count registers will be loaded into FAN2 expect count registers. When T2 temperature is **below** this boundary, FAN2 segment **2** speed count registers will be loaded into FAN2 expect count registers.

T2 BOUNDARY 5 TEMPERATURE – Index B1h

Bit	Name	R/W	Default	Description
7-0	T2_TP_5	R/W	002h	The 5th BOUNDARY temperature for T2 in temperature mode. When T2 temperature is **exceed** this boundary, FAN2 segment 5 speed count registers will be loaded into FAN2 expect count registers. When T2 temperature is **below** this boundary, FAN2 segment 6 speed count registers will be loaded into FAN2 expect count registers.

T2 BOUNDARY 9 TEMPERATURE – Index B2h

Bit	Name	R/W	Default	Description
7-0	T2_TP_9	R/W	00h	The 9th BOUNDARY temperature for T2 in temperature mode. When T2 temperature is **exceed** this boundary, FAN2 segment 9 speed count registers will be loaded into FAN2 expect count registers. When T2 temperature is **below** this boundary, FAN2 segment 10 speed count registers will be loaded into FAN2 expect count registers.

FAN2 SEGMENT 1 SPEED COUNT (MSB) – Index B4h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T2_SP_1_MSB	R/W		The MSB of 1st expected fan speed for FAN2 in temperature mode.

FAN2 SEGMENT 1 SPEED COUNT (LSB) – Index B5h

Bit	Name	R/W	Default	Description
7-0	T2_SP_1_LSB	R/W	FFh	The LSB of 1st expected fan speed for FAN2 in temperature mode.

FAN2 SEGMENT 5 SPEED COUNT (MSB) – Index B6h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T2_SP_5_MSB	R/W		The MSB of 5th expected fan speed for FAN2 in temperature mode.

FAN2 SEGMENT 5 SPEED COUNT (LSB) – Index B7h

Bit	Name	R/W	Default	Description
7-0	T2_SP_5_LSB	R/W	FFh	The LSB of 5th expected fan speed for FAN2 in temperature mode.

FAN2 SEGMENT 9 SPEED COUNT (MSB) – Index B8h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T2_SP_9_MSB	R/W		The MSB of 9th expected fan speed for FAN2 in temperature mode.

FAN2 SEGMENT 9 SPEED COUNT (LSB) – Index B9h

Bit	Name	R/W	Default	Description
7-0	T2_SP_9_LSB	R/W	FFh	The LSB of 9th expected fan speed for FAN2 in temperature mode.

7.6.3.60 FAN3 CONTROL v.s. TEMPERATURE 3 (INDEX C0 -- CD registers)

T3 BOUNDARY 1 TEMPERATURE – Index C0h

Bit	Name	R/W	Default	Description
7-0	T3_TP_1	R/W	00h	The 1st BOUNDARY temperature for T3 in temperature mode. When T3 temperature is **exceed** this boundary, FAN3 segment **1** speed count registers will be loaded into FAN3 expect count registers. When T3 temperature is **below** this boundary, FAN3 segment **2** speed count registers will be loaded into FAN3 expect count registers.

T3 BOUNDARY 5 TEMPERATURE – Index C1h

Bit	Name	R/W	Default	Description
7-0	T3_TP_5	R/W	00h	The 5th BOUNDARY temperature for T3 in temperature mode. When T3 temperature is **exceed** this boundary, FAN3 segment 5 speed count registers will be loaded into FAN3 expect count registers. When T3 temperature is **below** this boundary, FAN3 segment 6 speed count registers will be loaded into FAN3 expect count registers.

T3 BOUNDARY 9 TEMPERATURE – Index C2h

Bit	Name	R/W	Default	Description
7-0	T3_TP_9	R/W	00h	The 9th BOUNDARY temperature for T3 in temperature mode. When T3 temperature is **exceed** this boundary, FAN3 segment 9 speed count registers will be loaded into FAN3 expect count registers. When T3 temperature is **below** this boundary, FAN3 segment 10 speed count registers will be loaded into FAN3 expect count registers.

FAN3 SEGMENT 1 SPEED COUNT (MSB) – Index C4h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T3_SP_1_MSB	R/W		The MSB of 1st expected fan speed for FAN3 in temperature mode.

FAN3 SEGMENT 1 SPEED COUNT (LSB) – Index C5h

Bit	Name	R/W	Default	Description
7-0	T3_SP_1_LSB	R/W	FFh	The LSB of 1st expected fan speed for FAN3 in temperature mode.

FAN3 SEGMENT 5 SPEED COUNT (MSB) – Index C6h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T3_SP_5_MSB	R/W		The MSB of 5th expected fan speed for FAN3 in temperature mode.

FAN3 SEGMENT 5 SPEED COUNT (LSB) – Index C7h

Bit	Name	R/W	Default	Description
7-0	T3_SP_5_LSB	R/W	FFh	The LSB of 5th expected fan speed for FAN1 in temperature mode.

FAN3 SEGMENT 9 SPEED COUNT (MSB) – Index C8h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	0Fh	
3-0	T3_SP_9_MSB	R/W		The MSB of 9th expected fan speed for FAN3 in temperature mode.

FAN3 SEGMENT 9 SPEED COUNT (LSB) – Index C9h

Bit	Name	R/W	Default	Description
7-0	T3_SP_9_LSB	R/W	FFh	The LSB of 9th expected fan speed for FAN3 in temperature mode.

7.7 Keyboard Register

7.7.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.7.2 KBC Configuration Registers

KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC. When the DTR1# is pulled down. KBC_EN is reset to 0.DTR1# is internal pull up.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4;

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	0h	Select the IRQ channel for keyboard interrupt.

Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	0h	Select the IRQ channel for PS/2 mouse interrupt.

Clock Select Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	SELCLK_KBC	R/W	10	00: select 6MHz clock as KBC clock input. 01: select 8MHz clock as KBC clock input. 10: select 12MHz clock as KBC clock input (default). 11: select 16MHz clock as KBC clock input.
5-2	Reserved	-	-	Reserved.
1	GA20_EN	R/W	1	0: GATE20# software control. 1: GATE20# hardware speed up.
0	HKBRST	R/W	1	0: KBRST# software control. 1: KBRST# hardware speed up.

KBC Test Mode Register — Index F1h

Bit	Name	R/W	Default	Description
7-0	TEST_MODE_KBC	-	00h	Reserved for Fintek test mode only.

7.7.3 Device Registers

7.7.3.1 Status Register

The status register is an 8 bits register at I/O address 64h that provides information about the status of the KBC

Bit	Name	R/W	Default	Description
7	Parity error	R	0	0:odd parity 1:even parity
6	Time out	R	0	0:no time out error 1:time out error
5	Auxiliary device OBF	R	0	0: Auxiliary output buffer empty 1: Auxiliary output buffer full
4	Inhinit	R	0	0:keyboard is inhibited 1: keyboard is not inhibited
3	Command/data	R	0	0:data byte 1:command byte
2	SYSTEM_FLAG	R	0	This bit is set or clear by command byte of KBC
1	IBF	R	0	0:input buffer empty 1: input buffer full
0	OBF	R	0	0:output buffer empty 1: output buffer full

7.7.3.2 Command register

The internal KBC operation is controlled by the KBC command byte (KCCB). The KCCB resides in I/O address 64h that is read with a 20h command and written with a 60h command data.

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	Translate code	R/W	1	0: Pass un-translated scan code. 1: Translate scan code to IBM PC standard.
5	Disable Auxiliary Device	R/W	0	1: Disable Auxiliary inhibit function.
4	Disable Keyboard	R/W	0	1: Disable keyboard inhibit function.
3	Reserved	-	-	Reserved
2	System flag	R/W	1	0: The system is executing POST as a result of a cold boot. 1: The system is executing POST as a result of a shutdown or warm boot.
1	Enable Auxiliary Interrupt	R/W	1	0: Ao interrupt 1: A system interrupt is generated when a byte is placed in output buffer (IRQ12).
0	Enable keyboard Interrupt	R/W	1	0:No interrupt 1: A system interrupt is generated when a byte is placed in output buffer (IRQ1).

7.7.3.3 DATA register

The DATA register is an 8 bits register at I/O address 60h. the KBC used the output buffer to send the scan code received from keyboard and data byte replay by command to the system.

Power on default <7:0> = 00000000 binary

7.8 GPIO Registers

7.8.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description

7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.8.2 Configuration Registers

7.8.2.1 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELGIOIRQ	R/W	0h	Select the IRQ channel for GPIO[6:0] interrupt.

7.8.2.2 GPIO Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO6_OE	R/W	0	0: GPIO6 is in input mode. 1: GPIO6 is in output mode.
5	GPIO5_OE	R/W	0	0: GPIO5 is in input mode. 1: GPIO5 is in output mode.
4	GPIO4_OE	R/W	0	0: GPIO4 is in input mode. 1: GPIO4 is in output mode.
3	GPIO3_OE	R/W	0	0: GPIO3 is in input mode. 1: GPIO3 is in output mode.
2	GPIO2_OE	R/W	0	0: GPIO2 is in input mode. 1: GPIO2 is in output mode.
1	GPIO1_OE	R/W	0	0: GPIO1 is in input mode. 1: GPIO1 is in output mode.
0	GPIO0_OE	R/W	0	0: GPIO0 is in input mode. 1: GPIO0 is in output mode.

7.8.2.3 GPIO Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.

6	GPIO6_VAL	R/W	0	0: GPIO6 outputs 0 when in output mode. 1: GPIO6 outputs1 when in output mode and GPIO6_MODE is 0. GPIO6 outputs a pulse when in output mode and GPIO6_MODE is 1. Auto clear after the pulse.
5	GPIO5_VAL	R/W	0	0: GPIO5 outputs 0 when in output mode. 1: GPIO5 outputs 1 when in output mode and GPIO5_MODE is 0. GPIO5 outputs a pulse when in output mode and GPIO5_MODE is 1. Auto clear after the pulse.
4	GPIO4_VAL	R/W	0	0: GPIO4 outputs 0 when in output mode. 1: GPIO4 outputs 1 when in output mode and GPIO4_MODE is 0. GPIO4 outputs a pulse when in output mode and GPIO4_MODE is 1. Auto clear after the pulse.
3	GPIO3_VAL	R/W	0	0: GPIO3 outputs 0 when in output mode. 1: GPIO3 outputs 1 when in output mode and GPIO3_MODE is 0. GPIO3 outputs a pulse when in output mode and GPIO3_MODE is 1. Auto clear after the pulse.
2	GPIO2_VAL	R/W	0	0: GPIO2 outputs 0 when in output mode. 1: GPIO2 outputs 1 when in output mode and GPIO2_MODE is 0. GPIO2 outputs a pulse when in output mode and GPIO2_MODE is 1. Auto clear after the pulse.
1	GPIO1_VAL	R/W	0	0: GPIO1 outputs 0 when in output mode. 1: GPIO1 outputs 1 when in output mode and GPIO1_MODE is 0. GPIO1 outputs a pulse when in output mode and GPIO1_MODE is 1. Auto clear after the pulse.
0	GPIO0_VAL	R/W	0	0: GPIO0 outputs 0 when in output mode. 1: GPIO0 outputs 1 when in output mode and GPIO0_MODE is 0. GPIO0 outputs a pulse when in output mode and GPIO0_MODE is 1. Auto clear after the pulse.

7.8.2.4 GPIO Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO6_IN	R	-	The pin status of GPIO6/Voltage_fault4#/WDTRST1#.
5	GPIO5_IN	R	-	The pin status of GPIO5/Voltage_fault3#.
4	GPIO4_IN	R	-	The pin status of GPIO4/Voltage_fault2#.
3	GPIO3_IN	R	-	The pin status of GPIO3/Voltage_fault1#.
2	GPIO2_IN	R	-	The pin status of GPIO2.
1	GPIO1_IN	R	-	The pin status of GPIO1.
0	GPIO0_IN	R	-	The pin status of GPIO0.

7.8.2.5 GPIO Output Mode Register — Index E3h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO6_MODE	R/W	0	0: level mode, GPIO6 output is controlled by GPIO6_VAL. 1: pulse mode, write GPIO6_VAL 1 to generate a pulse via GPIO6.

5	GPIO5_MODE	R/W	0	0: level mode, GPIO5 output is controlled by GPIO5_VAL. 1: pulse mode, write GPIO5_VAL 1 to generate a pulse via GPIO5.
4	GPIO4_MODE	R/W	0	0: level mode, GPIO4 output is controlled by GPIO4_VAL. 1: pulse mode, write GPIO4_VAL 1 to generate a pulse via GPIO4.
3	GPIO3_MODE	R/W	0	0: level mode, GPIO3 output is controlled by GPIO3_VAL. 1: pulse mode, write GPIO3_VAL 1 to generate a pulse via GPIO3.
2	GPIO2_MODE	R/W	0	0: level mode, GPIO2 output is controlled by GPIO2_VAL. 1: pulse mode, write GPIO2_VAL 1 to generate a pulse via GPIO2.
1	GPIO1_MODE	R/W	0	0: level mode, GPIO1 output is controlled by GPIO1_VAL. 1: pulse mode, write GPIO1_VAL 1 to generate a pulse via GPIO1.
0	GPIO0_MODE	R/W	0	0: level mode, GPIO0 output is controlled by GPIO0_VAL. 1: pulse mode, write GPIO0_VAL 1 to generate a pulse via GPIO0.

7.8.2.6 GPIO Pulse Width Select 1 Register — Index E4h

Bit	Name	R/W	Default	Description
7-6	GPIO3_PW_SEL	R/W	00	GPIO3 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.
5-4	GPIO2_PW_SEL	R/W	00	GPIO2 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.
3-2	GPIO1_PW_SEL	R/W	00	GPIO1 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO0_PW_SEL	R/W	00	GPIO0 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.

7.8.2.7 GPIO Pulse Width Select 2 Register — Index E5h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	GPIO6_PW_SEL	R/W	00	GPIO6 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.

3-2	GPIO5_PW_SEL	R/W	00	GPIO5 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.
1-0	GPIO4_PW_SEL	R/W	00	GPIO4 pulse width select: 00: 500us (default). 01: 1ms. 10: 20ms. 11: 100ms.

7.8.2.8 GPIO Pulse Mode Register — Index E6h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO6_PUL_MODE	R/W	0	GPIO6 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.
5	GPIO5_PUL_MODE	R/W	0	GPIO5 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.
4	GPIO4_PUL_MODE	R/W	0	GPIO4 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.
3	GPIO3_PUL_MODE	R/W	0	GPIO3 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.
2	GPIO2_PUL_MODE	R/W	0	GPIO2 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.
1	GPIO1_PUL_MODE	R/W	0	GPIO1 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.
0	GPIO0_PUL_MODE	R/W	0	GPIO0 pulse mode: 0: output low pulse when in pulse mode. 1: output high pulse when in pulse mode.

7.8.2.9 GPIO Pad Type Register — Index E7h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO6_DRV_EN	R/W	0	GPIO6 pad type: 0: open drain. 1: push-pull.
5	GPIO5_DRV_EN	R/W	0	GPIO5 pad type: 0: open drain. 1: push-pull.

4	GPIO4_DRV_EN	R/W	0	GPIO4 pad type: 0: open drain. 1: push-pull.
3	GPIO3_DRV_EN	R/W	0	GPIO3 pad type: 0: open drain. 1: push-pull.
2	GPIO2_DRV_EN	R/W	0	GPIO2 pad type: 0: open drain. 1: push-pull.
1	GPIO1_DRV_EN	R/W	0	GPIO1 pad type: 0: open drain. 1: push-pull.
0	GPIO0_DRV_EN	R/W	0	GPIO0 pad type: 0: open drain. 1: push-pull.

7.8.2.10 GPIO IRQ Enable Register — Index E8h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO6_IRQ_EN	R/W	0	GPIO6 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO6 changed in input mode.
5	GPIO5_IRQ_EN	R/W	0	GPIO5 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO5 changed in input mode.
4	GPIO4_IRQ_EN	R/W	0	GPIO4 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO4 changed in input mode.
3	GPIO3_IRQ_EN	R/W	0	GPIO3 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO3 changed in input mode.
2	GPIO2_IRQ_EN	R/W	0	GPIO2 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO2 changed in input mode.
1	GPIO1_IRQ_EN	R/W	0	GPIO1 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO1 changed in input mode.
0	GPIO0_IRQ_EN	R/W	0	GPIO0 interrupt enable: 0: disable interrupt. 1: assert an interrupt when GPIO0 changed in input mode.

7.8.2.11 GPIO Edge Detect Register — Index E9h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.

6	GPIO6_EDG	R/W	1	GPIO6 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.
5	GPIO5_EDG	R/W	1	GPIO5 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.
4	GPIO4_EDG	R/W	1	GPIO4 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.
3	GPIO3_EDG	R/W	1	GPIO3 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.
2	GPIO2_EDG	R/W	1	GPIO2 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.
1	GPIO1_EDG	R/W	1	GPIO1 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.
0	GPIO0_EDG	R/W	1	GPIO0 edge detect: 0: input data does not change. 1: input data changes. Write 1 to clear.

7.8.2.12 GPIO1 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_OE	R/W	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

7.8.2.13 GPIO1 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_VAL	R/W	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.

5	GPIO15_VAL	R/W	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

7.8.2.14 GPIO1 Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_IN	R	-	The pin status of IRTX/GPIO16.
5	GPIO15_IN	R	-	The pin status of PCIRST5#/GPIO15.
4	GPIO14_IN	R	-	The pin status of PCIRST3#/GPIO14.
3	GPIO13_IN	R	-	The pin status of PCIRST2#/GPIO13.
2	GPIO12_IN	R	-	The pin status of PWROK1/GPIO12.
1	GPIO11_IN	R	-	The pin status of PCIRST1#/GPIO11.
0	GPIO10_IN	R	-	The pin status of RSTCON#/GPIO10.

7.8.2.15 GPIO2 Output Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

7.8.2.16 GPIO2 Output Data Register — Index F4h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs1 when in output mode.
6	GPIO26_VAL	R/W	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs1 when in output mode.
5	GPIO25_VAL	R/W	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

7.8.2.17 GPIO2 Pin Status Register — Index F5h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of RSMRST#/GPIO27.
6	GPIO26_IN	R	-	The pin status of PCIRST4#/GPIO26.
5	GPIO25_IN	R	-	The pin status of PWROK2/GPIO25.
4	GPIO24_IN	R	-	The pin status of GPIO24/OVT#/WDTRST2#.
3	GPIO23_IN	R	-	The pin status of PSON#/GPIO23.
2	GPIO22_IN	R	-	The pin status of PWSWIN#/GPIO22.
1	GPIO21_IN	R	-	The pin status of PME#/GPIO21.
0	GPIO20_IN	R	-	The pin status of PWSWOUT#/GPIO20.

7.8.2.18 GPIO3 Output Enable Register — Index F6h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1	GPIO31_OE	R/W	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode.
0	GPIO30_OE	R/W	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode.

7.8.2.19 GPIO3 Output Data Register — Index F7h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.

1	GPIO31_VAL	R/W	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

7.8.2.20 GPIO3 Pin Status Register — Index F8h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1	GPIO31_IN	R	-	The pin status of S3#/GPIO31.
0	GPIO30_IN	R	-	The pin status of IRRX/GPIO30.

7.9 VID Register

7.9.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.9.2 VID Configuration Registers

VID Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	VID_EN	R/W	0	0: disable VID. 1: enable VID.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of VID base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of VID base address.

7.9.3 Device Registers

7.9.3.1 VID Control Register — Index 00h

Bit	Name	R/W	Default	Description
7	CLK_SEL	R/W	0	Select Watchdog Timer clock, set to 1 will use external clock source (power by Vcc), else will use internal OSC 2MHz clock (power by VSB3V).
6-4	Reserved	-	-	Reserved
3	EN_GP_OTF	R/W	0	Set this bit 1 to control GPIO4/Voltage_fault2/BEEP/VID_OTF# to enable VID on the fly function. To function correctly, the EN_OTF should be programmed to 0 first.
2	CPU_SEL	R/W	0	CPU select, if set this bit to 1 will select AMD CPU, else if set to 0 is Intel CPU(default), (This bit will auto clear by SLOTOCC# or Watchdog timer, and protect write command by VID_KEY REG 0x30.)
1	EN_OTF	R/W	0	If set this bit to 1 will enable VID on the fly mode, user can change new VID value by program the REG 0x01 VID_OFFSET, else if set to 0, VID will in programming mode, user can program REG 0x02 to decide VID output data. (This bit will auto clear by SLOTOCC# or Watchdog timer, and protect write command by VID_KEY REG 0x03.)
0	VID_EXTEND	R/W	1	Set this bit to 1 to enable Intel VRM10 mode, this bit default is enable, (This bit will auto clear by SLOTOCC# or Watchdog timer, and protect write command by VID_KEY REG 0x03.)

7.9.3.2 VID on the fly offset Register — Index 01h

Bit	Name	R/W	Default	Description

7-6	Reserved	-	-	Reserved
5-0	VID_OFFSET	R/W	00h	VID offset register. The offset value is representative in 2's complement. The real VID value will be added by this offset and then will be put into VID_OUT (when EN_OTF is set). The offset ranges from -16 to +31. 1Fh : +31. 01h : +1. 00h : +0. 3Fh : -1. 30h : -16.

7.9.3.3 VID Output Data Register — Index 02h

Bit	Name	R/W	Default	Description
7	EN_VIDOUT	R/W	0	Enable VIDOUT. If set to one and VID output key is asserted referred as VIDKEY, the VIDOUT_DATA will output to these pins of VIDOUT. This bit is supplied by VSB3V and reset by the VSB3V power good or Watchdog timer is asserted or SLOTOCC# is asserted.
6	VIDKEY_OK	RO	0	When the sequential key is programmed to register 22H. this bit will set to 1. if program exit sequential key to register 22H, this bit read back will be 0
5-0	VIDOUT_DATA	R/W	00h	VIDOUT Data. These bits is mapping to VIDOUT[5:0] if EN_VIDOUT is enable. These bits power is supplied by VSB3V for keeping data when VDD3V power is lose.

7.9.3.4 VIDKEY Protection — Index 03h

Bit	Name	R/W	Default	Description
7-0	VIDKEY	R/W	00h	VID Key for protection the VIDOUT. If would like to program VID Output Data Register, the sequential key should be programmed first. The VID Output Register is disable in the default (VSB3V power on). The sequential keys are defined as 0x32, 0x5d, 0x42, 0xac. And the exit key is 0x35.

7.9.3.5 VID Input Data Register — Index 04h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-0	VID_IN	R	XXh	VID Input data.

7.9.3.6 Watchdog Timer Control Register — Index 05h

Bit	Name	R/W	Default	Description

7	Reserved	R	0	Reserved. Read will return 0.
6	STS_WD_TMOUT	R/W	0	Watchdog is timeout. When the watchdog is timeout, this bit will be set to one. If set to 1, write 1 will clear this bit. Write 0, no effect.
5	WD_ENABLE	R/W	0	Enable watchdog timer.
4	WD_PULSE	R/W	0	Watchdog output level or pulse. If set 0 (default), the pin of watchdog is level output. If write 1, the pin will output with a pulse.
3	WD_UNIT	R/W	0	Watchdog unit select. Default 0 is select second. Write 1 to select minute.
2	WD_HACTIVE	R/W	0	Program WD output level. If set to 1 and watchdog asserted, the pin will be high. If set to 0 and watchdog asserted, this pin will drive low (default).
1-0	WD_PSWIDTH	R/W	00	Watchdog pulse width selection. If the pin output is selected to pulse mode. The pulse width can be choice. 00b – 1m second. 01b – 25m second. 10b – 125m second 11b – 5 second

7.9.3.7 Watchdog Timer Range Register — Index 05h

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	00h	Watchdog timing range from 0 ~ 255. The unit is either second or minute programmed by the watchdog timer control register bit3.

7.10 ACPI and PME Registers

7.10.1 Logic Device Number Register

Logic Device Number Register — Index 07H

Bit	Name	R/W	Default	Description

7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 0ah: Select PME & ACPI device configuration registers.

7.10.2 ACPI and PME Configuration Registers

Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

PME Event Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	MS_PME_EN	R/W	0	PS/2 mouse PME event enable. 0: disable PS/2 mouse PME event. 1: enable PS/2 mouse PME event.
5	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3	PRT_PME_EN	R/W	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
2	UR2_PME_EN	R/W	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
1	UR1_PME_EN	R/W	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.

0	FDC_PME_EN	R/W	0	FDC PME event enable. 0: disable FDC PME event. 1: enable FDC PME event.

PME Event Status Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	MS_PME_ST	R/W	1	PS/2 mouse PME event status. 0: PS/2 mouse has no PME event. 1: PS/2 mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/W	1	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/W	0	Hardware monitor PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	PRT_PME_ST	R/W	0	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UR2_PME_ST	R/W	0	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UR1_PME_ST	R/W	0	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	FDC_PME_ST	R/W	1	FDC PME event status. 0: FDC has no PME event. 1: FDC has a PME event to assert. Write 1 to clear to be ready for next PME event.

ACPI Control Register — Index F4h

Bit	Name	R/W	Default	Description
7	TS3	R/W	0	Set to 1 to enable keyboard or mouse can wakeup from S1 state, It must also set EN_KBCWAKEUP and EN_MOWAKEUP register.
6	Reserved	-	-	Reserved
5	Reserved	-	-	Reserved
4	EN_KBCWAKEUP	R/W	0	Set to 1 to enable the Keyboard to wakeup system.
3	EN_MOWAKEUP	R/W	0	Set to 1 to enable the mouse to wakeup system.

2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Reserved (always on) 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

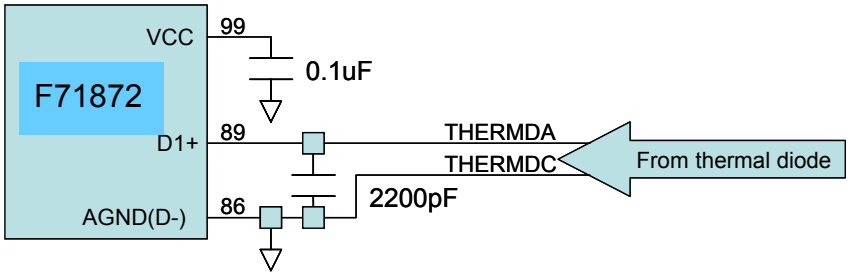
ACPI Control Register — Index F5h

Bit	Name	R/W	Default	Description
7	SOFT_RST_ACPI	R/W	0	Software Reset to ACPI (auto clear after reset)
6	Reserved	-	-	Reserved
5	RSTCON_EN	R/W	1	Set to 1 to enable RSTCON_EN to PCIRST, set to 0 to enable RSTCON_EN to PWOKIN1 and PWOKIN2
4-3	DELAY	R/W	11	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms
2	VINDB_EN	R/W	1	Enable the PCIRSTIN_N and ATXPWGD debounce
1	Reserved	-	-	Reserved.
0	Reserved	-	-	Reserved.

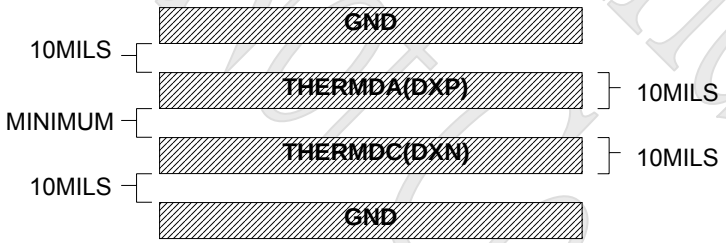
8 PCB Layout Guide

F71872 adopts **Current Mode** measure method to do temperature detected. The measure data will not be affected by different process of CPU due to use current mode technology. This technology measures mini-voltage from the remote sensor so a good PCB layout must be cared about noise minimizing. The noises often come from circuit trace which is a track from remote sensor (CPU side) to detect circuit input (F71872 side). The signal on this track will be inducted mini-noises when it passes through a high electromagnetic area. Those effects will result in the mini-noises and show in the detected side. It will be reported a wrong data which you want to measure. Please pay attention and follow up the check list below in order to get an actual and real temperature inside the chip.

1. The D1+/D2+/D3+ and AGND (D-) tracks **Must Not** pass through/by PWM POWER-MOS. Keep as far as possible from POWER MOS.
2. Place a 0.1μF bypass capacitor close to the V_{CC} pin (Pin# 99). Place an external 2200pF input filter capacitors across D+, D- and close to the F71872. Near the pin AGND (D-) **Must Be** placed a through hole into the GND Plane before connect to the external 2200pF capacitor.



3. Place the F71872 as close as practical to the remote sensor diode. In noisy environments, such as a computer main-board, the distance can be 4 to 8 inches. (typ). This length can be increased if the worst noise sources are avoided. Noise sources generally include clock generators, CRTs, memory buses and PCI/ISA bus etc.
4. Separated route the D1+, D2+ or D3+ with AGND (D-) tracks close together and in parallel after adding external 2200pF capacitor. For more reliable, it had better with grounded guard tracks on each side. Provide a ground plane under the tracks if possible. Do not route D+ & D- lines next to the deflection coil of the CRT. And also don't route the trace across fast digital signals which can easily induce bigger error.



5. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.
6. Try to minimize the number of component/solder joints, called through hole, which can cause thermocouple effects. Where through holes are used, make sure that they are in both the D+ and D- path and at the same temperature. Thermocouple effects should not be a major problem as 1℃ corresponds to about 200μV. It means that a copper-solder thermocouple exhibits 3μV/℃, and takes about 200μV of the voltage error at D+ & D- to cause a 1℃ measurement error. Adding a few thermocouples causes a negligible error.
7. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. It will work up to around 6 to 12 feet.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance will affect the measurement accuracy. When using long cables, the filter capacitor should be reduced or removed. Cable resistance can also induce errors. For example: 1 Ω series resistance introduces about 0.5℃ error.

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V) (Note)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{16ts} - TTL level bi-directional pin, can select to OD by register, with 16 mA source-sink capability						
Input Low Threshold Voltage	Vt-				V	VDD = 3.3 V
Input High Threshold Voltage	Vt+				V	VDD = 3.3 V
Output Low Current	IOL				mA	VOL = 0.4 V
Input High Leakage	ILIH				μA	VIN = VDD
Input Low Leakage	ILIL				μA	VIN = 0V
I/OD_{12ts} - TTL level bi-directional pin, can select to OD by register, with 12 mA source-sink capability						
Input Low Threshold Voltage	Vt-				V	VDD = 3.3 V
Input High Threshold Voltage	Vt+				V	VDD = 3.3 V
Output Low Current	IOL				mA	VOL = 0.4 V
Input High Leakage	ILIH				μA	VIN = VDD
Input Low Leakage	ILIL				μA	VIN = 0V

9.3 AC Characteristics

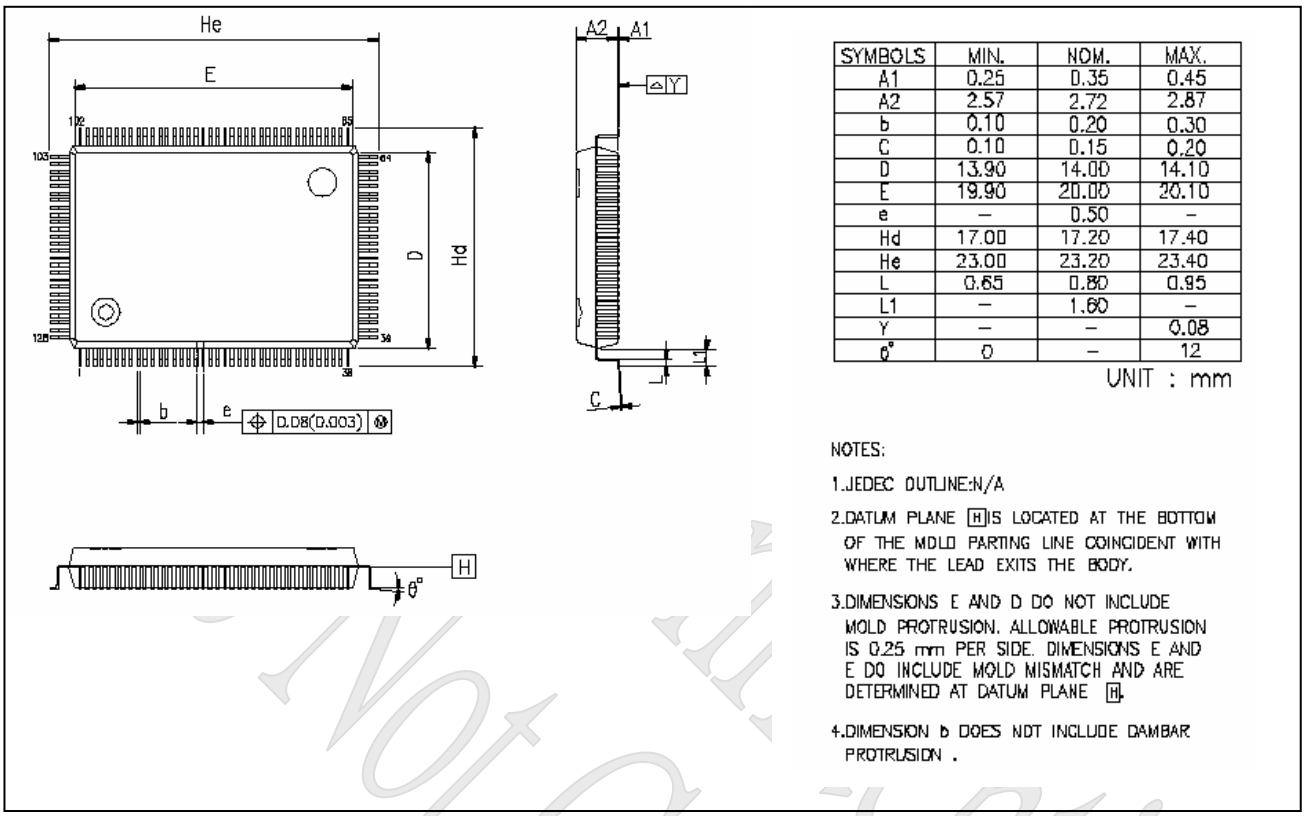
Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}			uS
Start condition hold time	$t_{HD;SDA}$			uS
Stop condition setup-up time	$t_{SU;STO}$			uS
DATA to SCL setup time	$t_{SU;DAT}$			nS
DATA to SCL hold time	$t_{HD;DAT}$			nS
SCL and SDA rise time	t_R			uS
SCL and SDA fall time	t_F			nS

10 Ordering Information

Part Number	Package Type	Production Flow
F71872F	128-QFP (Normal)	Commercial, 0°C to +70°C
F71872FG	128-QFP (Green Package)	Commercial, 0°C to +70°C

11 Package Dimensions



SYMBOLS	MIN.	NOM.	MAX.
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	–	0.50	–
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	–	1.60	–
Y	–	–	0.08
θ°	0	–	12

UNIT : mm

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12 F71872 Demo Circuit