

## FM3540/60

# 4/5 Bit Multiplexed, 1 Bit Latched Port with Standard 2-Wire Bus Interface and Non-Volatile Latches

### General Description

The FM3540/60 multiplexes the I-port input signals with two internal non-volatile registers that can be loaded through the serial port. The multiplexer is selected via the serial port and defaults to the I-Port upon power-up. Pull-up resistors are provided on the input port to accommodate connections to open drain outputs and to eliminate the need for external resistors. The device supports a choice of either 2.5V output or Open Drain Outputs for easy interface to devices with different VDD Levels.

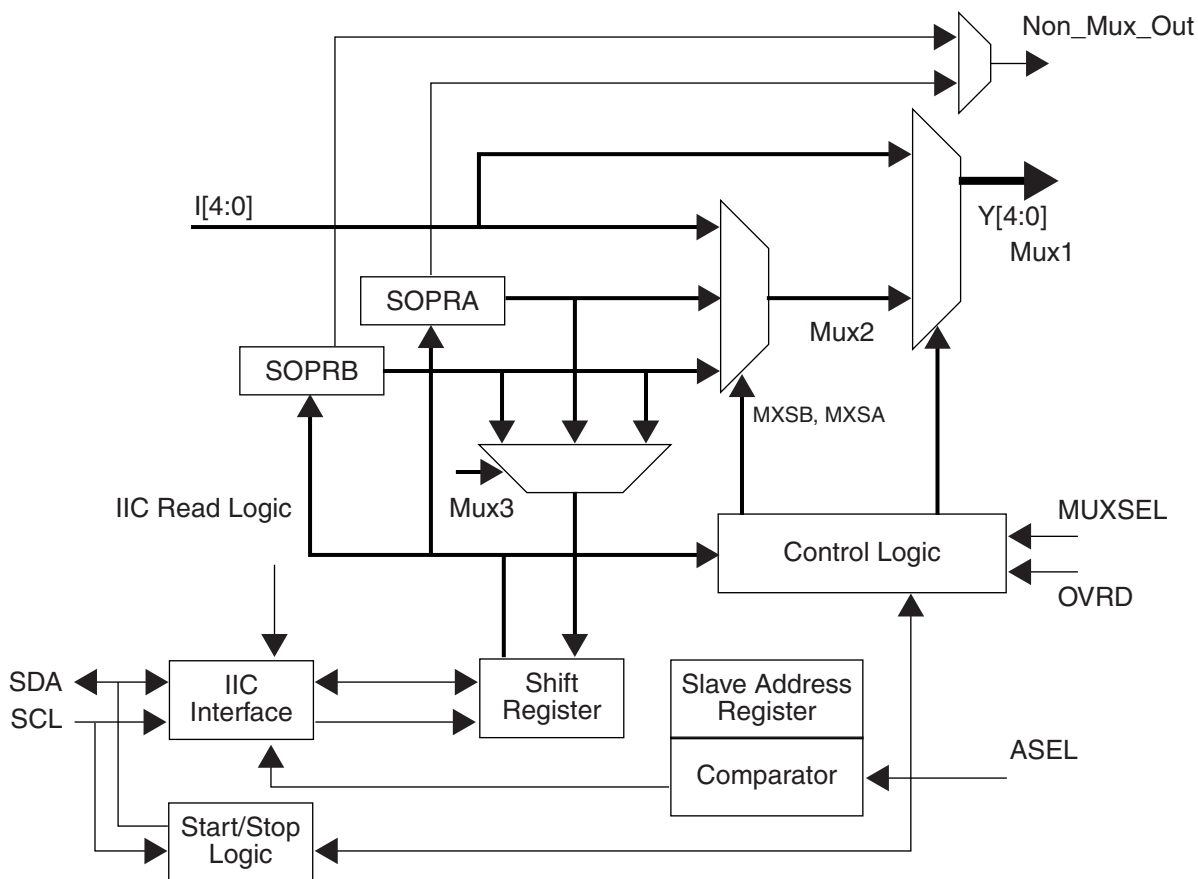
The serial port is an IIC compatible slave only interface and supports both 100kbps and 400kbps modes of operation. The port is used to read the I-Port, Write Data to the internal non-volatile

registers and select whether the I-Port or one of the internal non-volatile registers is output to the Y-port. The FM3540/60 is fabricated with an advanced CMOS technology to achieve high density and low power.

### Features

- Extended Operating Voltage Range 3.0V-5.5V
- IIC Compatible Slave Interface.
- ESD performance: Human body model > 2000V
- Choice of 2.5V outputs or Open-Drain Outputs

### Block Diagram



## Ordering Information

| Order Number | Package Number | Package Description | Packing | Y-Port Output Type | Device Address   |
|--------------|----------------|---------------------|---------|--------------------|------------------|
| FM3540CM14   | M14A           | 14-Pin SO           | T&R     | Open-Collector     | 1001110          |
| FM3540CMT14  | MTC14          | 14-Pin TSSOP        | T&R     | Open-Collector     | 1001110          |
| FM3540SM14   | M14A           | 14-Pin SO           | T&R     | Fixed 2.5V         | 1001110          |
| FM3540SMT14  | MTC14          | 14-Pin TSSOP        | T&R     | Fixed 2.5V         | 1001110          |
| FM3560M20    | M20B           | 20-Pin SO           | T&R     | (See Note below)   | (See Note below) |
| FM3560MT20   | MTC20          | 20-Pin TSSOP        | T&R     | (See Note below)   | (See Note below) |

### Note About Y-Port Output Type:

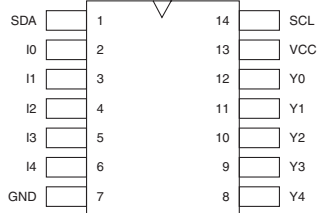
FM3560 device has a dedicated input pin (LEVEL) to select either "Fixed 2.5Volts" or "Open-Collector" Y-Port output type.

### Note About Device Address:

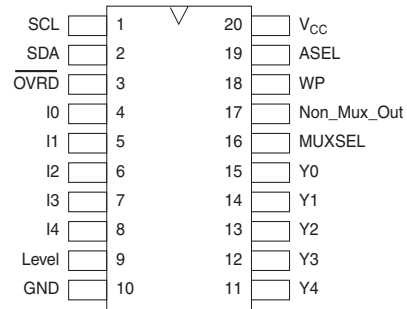
- For FM3540 with an alternate device address of 0110111, contact Fairchild Marketing/Sales.
- FM3560 device has a dedicated input pin (ASEL) to select either "1001110" or "0110111" as device address.

## Pin Connection Diagrams

**14-Pin Packages  
FM3540**



**20-Pin Packages  
FM3560**



## Pin Description

| Pin Name    | Description                           |
|-------------|---------------------------------------|
| I[0:4]      | Data Inputs w/Pullups (10K-40K)       |
| Y[0:4]      | O/D Data Outputs                      |
| SCL         | Serial Port Clock Input (120K pullup) |
| Override#   | Override Input, sets all outputs to 0 |
| WP          | Write Protect Input                   |
| Non_Mux_Out | Non-Multiplexed Output                |
| Mux_Sel     | Mux. Select Input                     |
| Level       | Level Select Input                    |
| ASEL        | Address Select Input                  |
| SDA         | Serial Port Data I/O (120K pullup)    |

## Functional Description

The FM3540/60 has two primary functional modes of operation and an additional mode for programming the device.

### Operational Modes

During standard operation the device will either pass an address to the Y-Port from the I-Port or from an internally programmed value. At power up the device will default to passing the I-Port value to the Y-Port.

The I-port values are generated from the motherboard of the system and may be hardwired or driven by another device. Pull-up resistors are provided on the device to accommodate this device being driven by open drain output drivers. The device expects standard CMOS input signals. The level of the output signal is determined by the Level input. If this input is connected to Vss/Ground, the output is at 2.5V on the multiplexed outputs (Y0-Y4). The non-multiplexed output is always at CMOS levels. The Level input, if left unconnected (it has an internal pullup), will cause the Y0-Y4 outputs to operate as open-drain outputs. The override# input, when set to 0, will cause all the outputs to be set to 0. The WP signal, if set to logic 1, will prevent data from being written to the non-volatile register.

The mux\_sel input, when set to logic 0, will select the data from the non-volatile register to drive on the Y0-4 outputs. If set to logic 1, the data from the inputs are selected instead. The non\_mux\_out latch is transparent when the mux\_sel signal is at logic 0, and will latch data when the mux\_select is in a logic 1 state.

### Output Port: Y0-Y4

The output port is an open drain output to allow for easy connection to devices running at different voltage levels. The port is always active and either passes the value on the I-Port or the value in the Serial output port Register (SOPR). Changing the Mux Path is accomplished by writing to b7, b6 of the Serial Input Port Register. SOPR-b7, b6 defaults to a value of "10" at power up and the default path is from the I-Port through to the output port. The multiplexer only updates when an IIC stop condition is observed.

### Register Description

The FM3540/60 has 3 registers in total. These registers are made up of a combination of read only, write only and read write bits. The two registers are listed below.

*Serial Output Port Register A(SOPRA) Address: 00H - A read/write register that contains the new value to be written to output Port-Y and the multiplexer select bit.*

*Serial Output Port Register B(SOPRB) Address: 01H - A read/write register that contains the new value to be written to output Port-Y and the multiplexer select bit.*

*Parallel Input Port Register (PIPR) Address: 02H - A read only register that is loaded with the 5 bit value of the I-Port.*

## Serial Output Port Register (SOPR)

(Address 000b and 001b)

| MXSB | MXSA | Data Field |     |    |    |    |    |
|------|------|------------|-----|----|----|----|----|
| 0    | 0    | I5         | NMO | I3 | I2 | I1 | I0 |
| b7   | b6   | b5         | b4  | b3 | b2 | B1 | b0 |

b7-b6 - Multiplexer Select Bits (MXSB,MXSA)

00 - Multiplexer passes the SOPR(A).

01 - Multiplexer passes the SOPR(B).

10 - Multiplexer defaults to passing the I-Port Value.

b5, b3-b0 - Data Field. New value to be output through the multiplexer.

nmo - Non multiplexed output from internal non-volatile bit

## Parallel Input Port Register (PIPR)

(Address 002b)

| Address Field |    |    | Data Field |    |    |    |    |
|---------------|----|----|------------|----|----|----|----|
| 0             | 0  | 0  | I4         | I3 | I2 | I1 | I0 |
| b7            | b6 | b5 | b4         | b3 | b2 | B1 | b0 |

b7-b5 - Address field. Value is always 000

b4-b0 - Data Field. Value is equal to the value on the I-Port.

The external Port Register captures the value on the I-Port. Data is latched into this register on the first clock after a start condition is seen. This insures that a valid value will always be in this register if it is read. This register is a read only register with respect to the IIC port.

| Over-ride# | mux_sel | MXSB   | MXSA   | mux_outputs                        | Non_mux_output                              |
|------------|---------|--------|--------|------------------------------------|---|
| 0          | 0       | X      | X      | all 0's                            | all 0's                                     |
| 0          | 1       | X      | X      | Mux_inputs (see note 1)            | latched NMO                                 |
| 1          | 0       | 1      | 0      | Mux_inputs (see note 1)            | latched NMO                                 |
| 1          | 0       | 0      | 0      | From Non-volatile register (SOPRA) | From non-volatile register (SOPRA)          |
| 1          | 0       | 1      | 1      | Do not use this combination        |   |
| 1          | 0       | 0      | 1      | From Non-volatile register (SOPRB) | From non-volatile register (SOPRB)          |
| 1          | 1       | Note 2 | Note 1 | Mux_inputs                         | From Non-volatile register (SOPRA or SOPRB) |

**Note 1:** Latched NMO state will be the value present on the NMO output at the time of the mux\_sel input transitioning from logic 0 to logic 1 state.

**Note 2:** Output depends on previously selected state of MXSB and MXSA bits written to device.

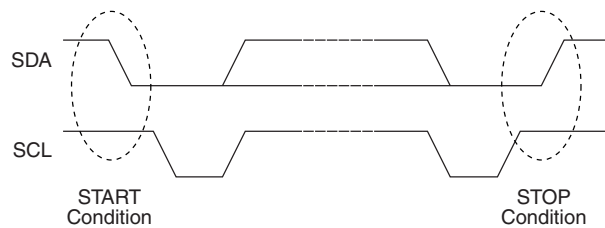
## Multiplexer Logic

The output multiplexer logic determines what value is actually output to the Y-port. The value that is output is dependent upon b7-b6 of the SOPRA and SOPRB registers, as well as the external mux\_sel and override# inputs. There is only one set of MXS bits in the SOPRA and SOPRB registers. Regardless of whether one writes to SOPRA or SOPRB register for setting the MXS bits, the result is the same. These same bits appear in both the registers. If the mux\_sel is logic 0 and OVRD is logic 1, then, if b7,b6 is "10" then the value on the I-port is passed. When b7 is "00" the value of the SOPRA register is passed on the next IIC stop condition, and .When b7 is "01" the value of the SOPRB register is passed on the next IIC stop condition. If mux\_sel is logic 1 and OVRD is logic 1, the input lines I0-4 are used to drive the outputs. The above table describes all the combinations.

## IIC Interface

The IIC Interface is a standard slave interface. As a slave interface the device will not generate its own clock. Data can be read from and written into the device. Commands for reading and writing the registers are generated by the IIC Master.

## START and STOP Conditions



The IIC protocol uniquely defines START and STOP conditions. A START condition is defined as a HIGH to LOW transition of the SDA signal while SCL is HIGH. A STOP condition is defined as a LOW to HIGH transition of the SDA signal while SCL is HIGH. These are shown in Figure 2.

## Device Addressing

The device uses 7 bit IIC addressing. The address has been defined as 1001 110 if the ASEL input is '1' and 0110 111 if the ASEL input is '0'. The address byte is the first byte of data sent after a start condition. This is the only address that this device will respond to. The device will not respond to the general call address 0000 000.

## Reading from the Registers

Data can be read from both of the internal registers. All reads are non-destructive and do not change the value in the register or the internal state of the device. When a start condition is received with a read request both registers can be read out in the following sequence.

- (1) SOPRA - Serial Output Port Register A
- (2) SPORB - Serial Output Port Register B
- (3) PIPR - PORT-I Value

If so desired only the SOPRA register can be read. This is accomplished by issuing a stop command after acknowledge bit for the first byte read. If no stop is issued, the device will output the registers in the above sequence.

## Writing to the Registers

Data is written to the SOPR registers through the serial port interface. When a write request is received with the Start Address it is assumed that the intent is to write the SOPR registers. The value placed in the least 6 significant bits of the register contain the new code to be placed in the SOPR A/B registers. The value of the two most significant bits must contain the address of the destination register SOPRA or SOPRB.

The internal non-volatile latch takes about 10 ms to update its data. The new data is reflected on the outputs after the internal non-volatile latch is updated, if the corresponding select bits (MXSx, OVRD and mux\_sel) are set to reflect the state of the non-volatile register

## Register Read Sequence

| S | Slave Address | R | A | SOPRA Register | A | SOPRB Register | A | PIPR Register | A | P |
|---|---------------|---|---|----------------|---|----------------|---|---------------|---|---|
| S | 1001110       | 1 | A | 00bbbbbb       | A | 00bbbbbb       | A | 00bbbbbb      | A | P |

## Register Write Sequence

| S | Slave Address | W | A | SOPRx Register | A | S |
|---|---------------|---|---|----------------|---|---|
| S | 1001110       | 0 | A | xxbbbbbb       | A | S |

xx = Register Selection bits (MXSB and MXSA) xx = 00 selects SOPRA, 01 selects SOPRB

## Register Write Sequence using Repeated Start Condition

| S | Slave Address | R | A | SOPRA Register | A | S | Slave Address | W | A | SOPRx Register | A | P |
|---|---------------|---|---|----------------|---|---|---------------|---|---|----------------|---|---|
| S | 1001110       | 1 | A | 00bbbbbb       | A | S | 1001110       | 0 | A | xxbbbbbb       | A | P |

Figure 4

### Absolute Maximum Ratings (Note 1)

|  |                       |
|--|-----------------------|
| Supply Voltage ( $V_{CC}$ )  | -0.5V to +6.5V        |
| DC Input Voltage ( $V_I$ )   | -0.5V to +6.5V        |
| Output Voltage ( $V_O$ )   |                       |
| Outputs 3-STATED   | -0.5V to +6.5V        |
| Outputs Active (Note 2)  | -0.5 to $V_{CC}+0.5V$ |
| DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$                     | -50mA                 |
| DC Output Diode Current (IOK)                                      |                       |
| $V_O < 0V$   | -50mA                 |
| $V_O > V_{CC}$   | +50mA                 |
| DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )                  | $\pm 50mA$            |
| DC $V_{CC}$ or Ground Current per Supply Pin ( $I_{CC}$ or Ground) | $\pm 100mA$           |
| Storage Temperature Range ( $T_{STG}$ )                            | -65°C to +150°C       |

### Recommended Operating Conditions (Note 3)

|  |                |
|--|----------------|
| Power Supply   | 3.0V to 5.5V   |
| Input Voltage  | -0.3V to 5.5V  |
| Output Voltage ( $V_O$ )   | 0V TO $V_{CC}$ |
| Output Current $I_{OL}$  | 3mA            |
| Free Air Operating Temperature(TA)   | -0°C to +70°C  |
| Minimum Input Edge Rate ( $d_T/d_V$ )<br>$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$ | 10nS/V         |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** IO Absolute Maximum Rating must be observed.

**Note 3:** Floating or unused pins (inputs or I/O's) must be held HIGH or LOW.

### DC Electrical Characteristics (4.5V < $V_{CC}$ ≤ 5.5V)

| Symbol   | Parameter                | Conditions   | $V_{CC}$ (V) | Min                 | Max                 | Units   |
|----------|--------------------------|--|--------------|---------------------|---------------------|---------|
| $V_{IH}$ | High Level Input Voltage |  | 4.5 - 5.5    | $V_{CC} \times 0.7$ |                     | V       |
| $V_{IL}$ | Low Level Input Voltage  |  | 4.5 - 5.5    |                     | $V_{CC} \times 0.3$ | V       |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL} = 100\mu A$<br>$I_{OL} = 3mA$                            | 4.5 - 5.5    |                     | 0.2<br>0.4          | V       |
| $I_{IR}$ | Input Leakage Current    | $V_I = V_{IL}$   | 5.5          | -10                 | +10                 | $\mu A$ |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND<br>$V_{CC} \leq (V_{Ii}, V_{O}) \leq 3.6V$ | 4.5 - 5.5    | 300                 | 975                 | $\mu A$ |

### DC Electrical Characteristics Extended (3.0V ≤ $V_{CC}$ ≤ 5.5V)

| Symbol   | Parameter                | Conditions  | $V_{CC}$ (V) | Min                 | Max                 | Units   |
|----------|--------------------------|---|--------------|---------------------|---------------------|---------|
| $V_{IH}$ | High Level Input Voltage |   | 3.0 - 5.5    | $V_{CC} \times 0.7$ |                     | V       |
| $V_{IL}$ | Low Level Input Voltage  |   | 3.0 - 5.5    |                     | $V_{CC} \times 0.3$ | V       |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL} = 100\mu A$<br>$I_{OL} = 3mA$   | 3.0 - 5.5    |                     | 0.2<br>0.4          | V       |
| $V_{OH}$ | Output High Voltage      | Fixed output mode, ('s' grade samples, or FM3560 with LEVEL input = logical '0') 1 TTL load, 50pf capacitance | 3.0 - 5.5    | 2.3                 | 2.5                 | V       |
| $I_{IR}$ | Input Leakage Current    | $V_I = V_{IL}$  | 5.5          | -10                 | +10                 | $\mu A$ |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND<br>$V_{CC} \leq (V_I, V_O) \leq 3.6V$   | 3.0 - 5.5    | 300                 | 975                 | $\mu A$ |

### AC Characteristics

| Symbol    | Parameter                               | $T_A = 0^\circ\text{C to } +70^\circ\text{C}, C_L = 30\text{pF}, R_L = 500\Omega$ |     |                                |     | Units |
|-----------|---|---|-----|--------------------------------|-----|-------|
|           |   | $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$  |     | $V_{CC} = 3.3 \pm 0.3\text{V}$ |     |       |
|           |   | Min   | Max | Min                            | Max |       |
| $t_{PHL}$ | Prop Delay I to Y                       |   | 50  |                                | 50  | ns    |
| $T_{PLH}$ | Prop Delay I to Y                       |   | 50  |                                | 50  | ns    |
| $t_{PHL}$ | Prop Delay to Y (from OVRD' or Mux_Sel) |   | 50  |                                | 50  | ns    |
| $T_{PLH}$ | Prop Delay to Y (from OVRD' or Mux_Sel) |   | 50  |                                | 50  | ns    |

### IIC AC Characteristics

| Symbol       | Parameter   | $T_A = 0^\circ\text{C to } +70^\circ\text{C}, C_L = 30\text{pF}, R_L = 500\Omega$ |      |        |     | Units         |
|--------------|---|---|------|--------|-----|---------------|
|              |   | 100kHz  |      | 400kHz |     |               |
|              |   | Min   | Max  | Min    | Max |               |
| $f_{SCL}$    | SCL Clock Frequency   |   | 100  |        | 400 | kHz           |
| $T_1$        | Noise Supression Time Constant                                |   | 100  |        | 50  | nS            |
| $t_{AA}$     | SCL Low to SDA Data Out Valid                                 | 0.3   | 3.5  | 0.1    | 0.9 | $\mu\text{S}$ |
| $t_{BUF}$    | Time the Bus must be free before a new Transmission can start | 4.7   |      | 1.3    |     | $\mu\text{S}$ |
| $t_{HD:STA}$ | Start Condition Hold Time                                     | 4.0   |      | 0.6    |     | $\mu\text{S}$ |
| $t_{LOW}$    | Clock Low Period  | 4.7   |      | 0.6    |     | $\mu\text{S}$ |
| $t_{HIGH}$   | Clock High Period   | 4.0   |      | 0.6    |     | $\mu\text{S}$ |
| $t_{SU:STA}$ | Start Condition Setup Time (For a repeated Start Condition)   | 4.7   |      | 0.6    |     |               |
| $t_{HD:DAT}$ | Data in Hold Time   | 0   |      | 0      |     | $\mu\text{S}$ |
| $t_{SU:DAT}$ | Data in Setup Time  | 250   |      | 100    |     | nS            |
| $t_R$        | SDA and SCL Rise Time   |   | 1000 |        | 300 | nS            |
| $t_F$        | SDA and SCL Fall Time   |   | 300  |        | 300 | nS            |
| $t_{SU:STO}$ | Stop Condition Setup Time                                     | 4.7   |      | 0.6    |     | $\mu\text{S}$ |

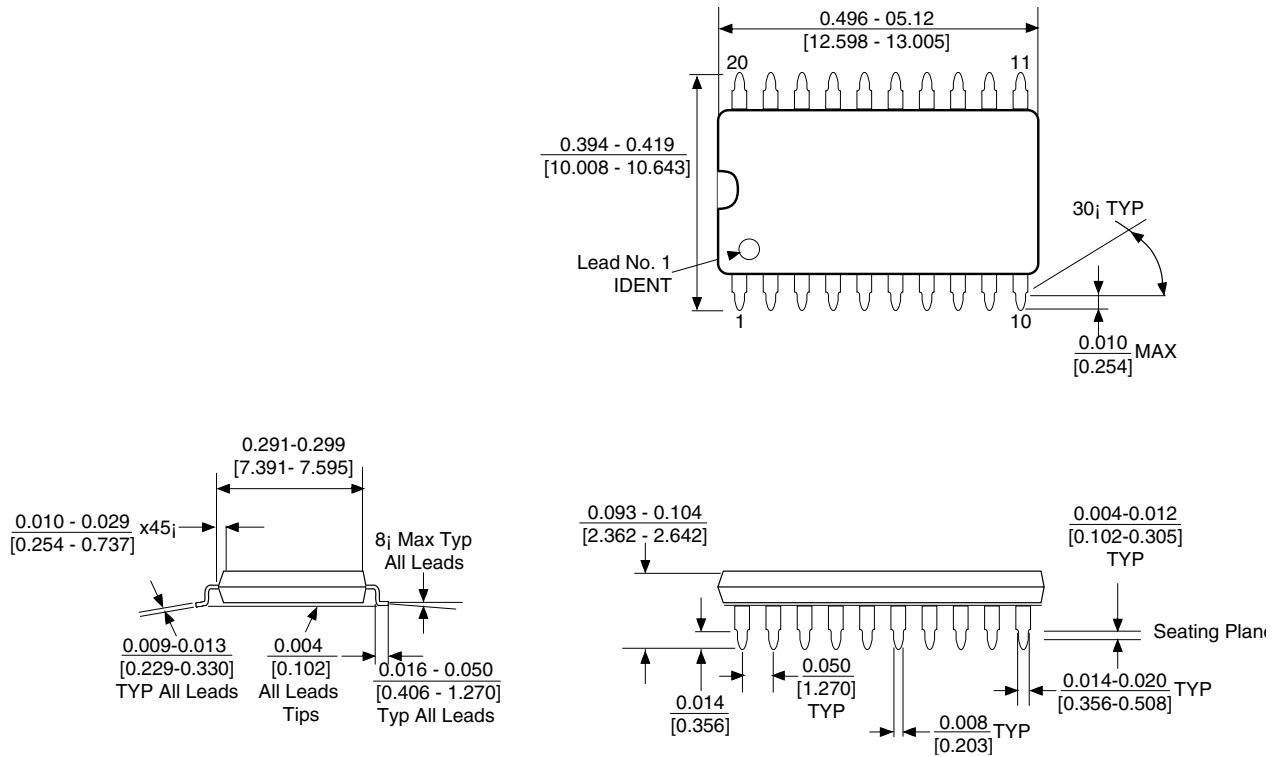
### Capacitance

| Symbol    | Parameter                      | Conditions   | $T_A = +25^\circ\text{C}$ Typical | Units |
|-----------|--------------------------------|--|-----------------------------------|-------|
| $C_{in}$  | Input Capacitance (I4-I0)      | $V_I = 0\text{V or } V_{CC}, V_{CC} = 3.3 \text{ or } 5.0$ | 6                                 | PF    |
| $C_{I/O}$ | Input/Output Capacitance (SDA) | $V_I = 0\text{V or } V_{CC}, V_{CC} = 3.3 \text{ or } 5.0$ | 7                                 | PF    |
| $C_{OUT}$ | Output Capacitance (Y4-Y0)     |  | 7                                 | PF    |

### Non-Volatile Memory Characteristics

| Parameter        | Specification    |
|------------------|------------------|
| Data Retention   | 10 years minimum |
| Number of writes | 1,000,000 cycles |

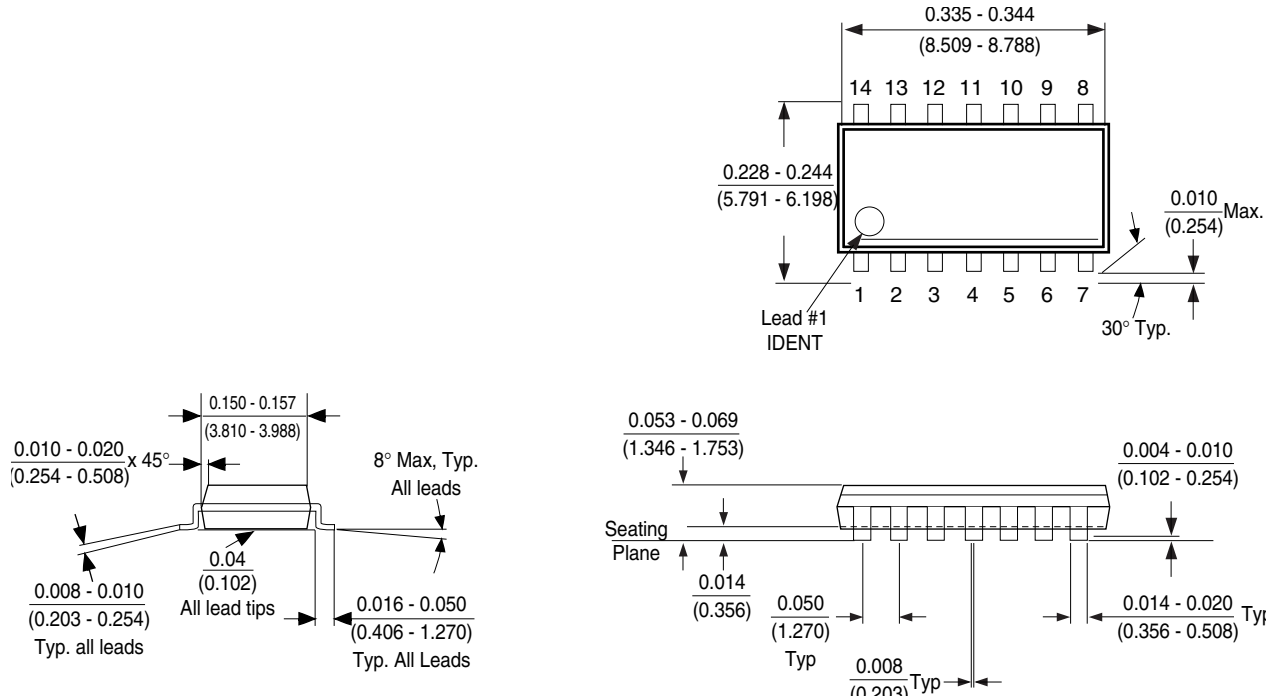
**Physical Dimensions** inches (millimeters) unless otherwise noted



**Molded Small Outline Package (M)**  
**Order Number FM3560XM**  
**Package Number M20B**

X = C for open collector  
 and X = S for 2.5V

**Physical Dimensions** inches (millimeters) unless otherwise noted

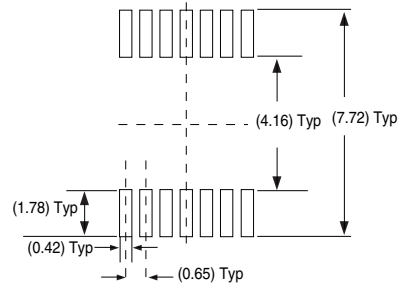
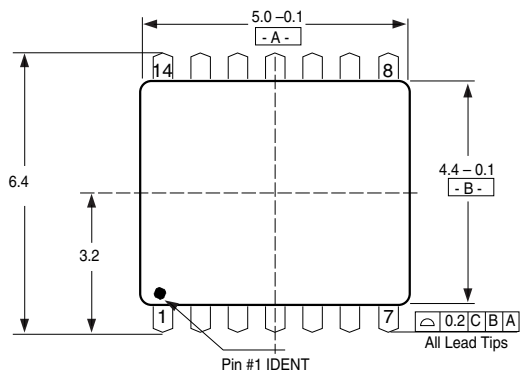


**Molded Small Outline Package (M)**  
**Order Number FM3540XM**  
**Package Number M14A**

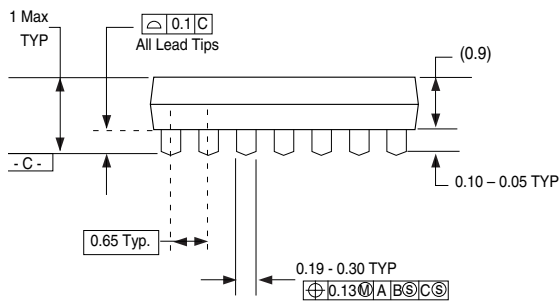
X = C for open collector  
 and X = S for 2.5V



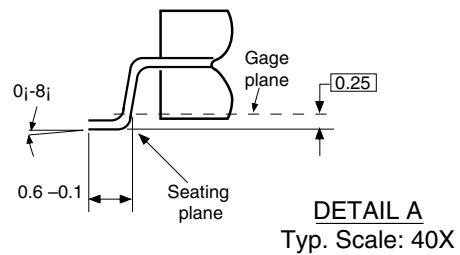
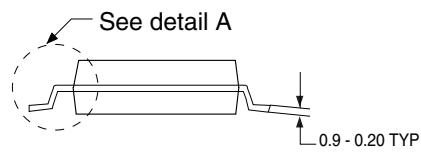
**Physical Dimensions** inches (millimeters) unless otherwise noted



Land pattern recommendation



Dimensions are in millimeters



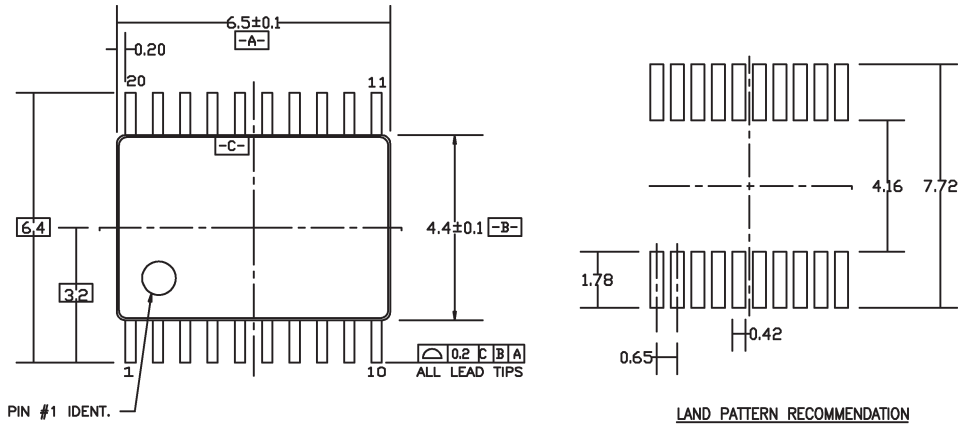
Notes: Unless otherwise specified

1. Reference JEDED registration MO153. Variation AB.  
Ref. Note 6, dated 7/93

**Order Number FM3540XMT**  
**Package Number MTC14**

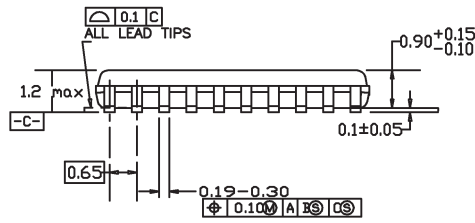
X = C for open collector  
and X = S for 2.5V

**Physical Dimensions** inches (millimeters) unless otherwise noted

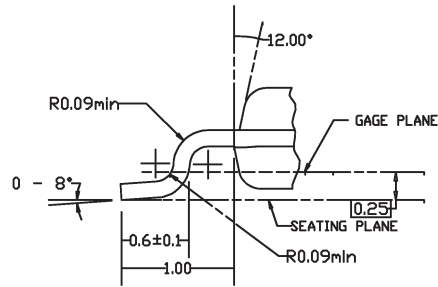
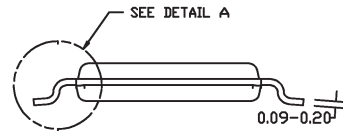


PIN #1 IDENT.

**LAND PATTERN RECOMMENDATION**



DIMENSIONS ARE IN MILLIMETERS



**DETAIL A**

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**Order Number FM3560MT**  
**Package Number MTC20**

**Life Support Policy**

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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