

**PCB STACK UP**

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

**Cable Docking**

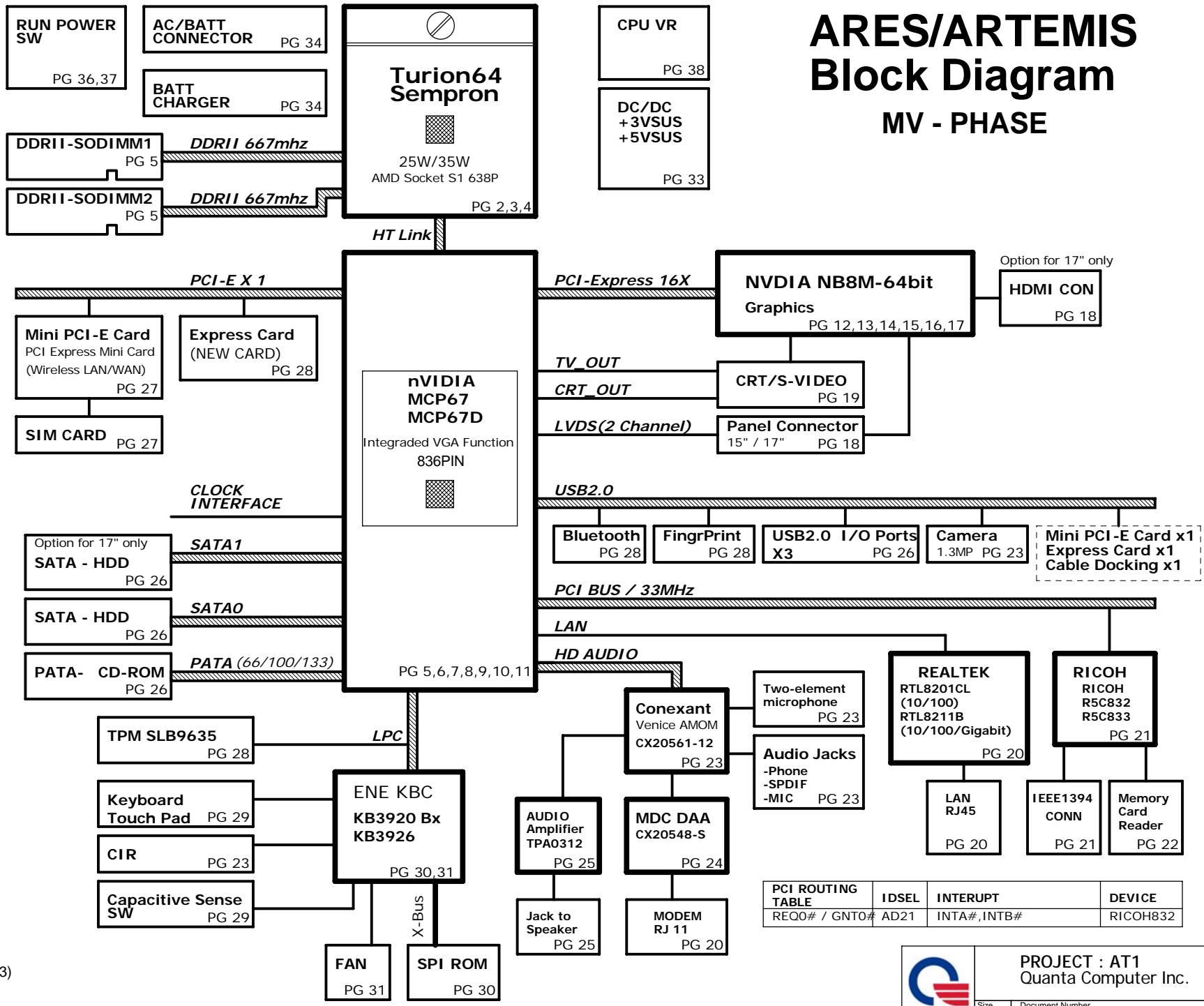
- TV\_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PG 31

# ARES/ARTEMIS

## Block Diagram

### MV - PHASE



**VAULE DEFINE**  
 A=0603,B=0805,C=1206,F=1%,  
 OTHER IS 0402  
 V=Y5V,U=Y5U,R=X5R,S=X6S,  
 X=X7R,G=COG,O=NPO

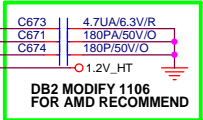
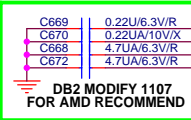
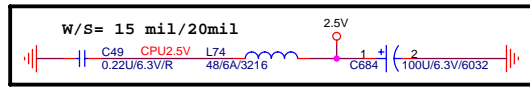
**EXAMPLE**  
 10R=10ohm(0402)  
 10A=10ohm(0603)  
 10B=10ohm(0805)  
 10C=10ohm(1206)  
 10/F=10ohm(0402 and 1%)

**EXAMPLE**  
 0.1U/16V/R=0.1U/16V/X5R(0402)  
 0.47UA/10V/X=0.47U/10V/X7R(0603)  
 10UB/10V/U=10U/10V/Y5U(0805)

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

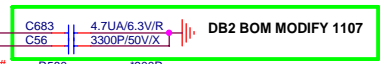
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number BLOCK DIAGRAM	Rev MV
Date: Tuesday, August 21, 2007		Sheet 1 of 40

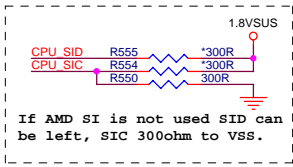


TEST PU/PL MUST FOLLOW ERRATUM 133 REVISION GUIDE FROM AMD NPT 0Ph CPU

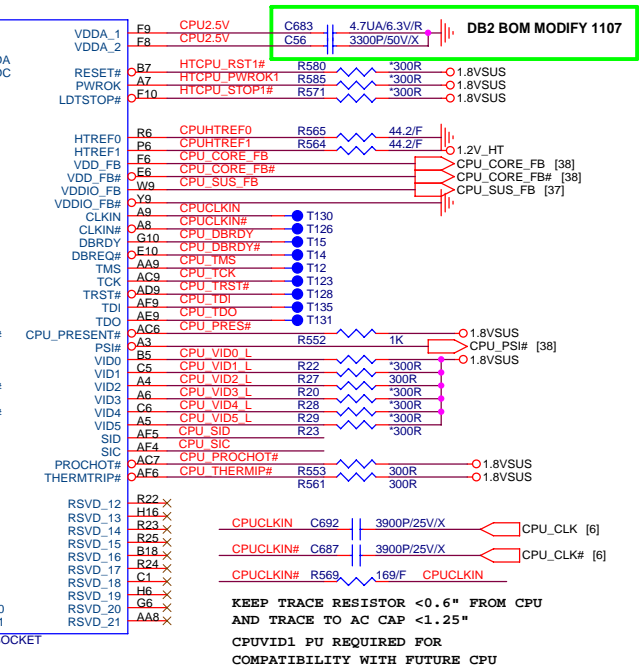
DB2 MODIFY 1107 FOR AMD RECOMMEND REMOVE TEST POINTS FOR AMD RECOMMEND



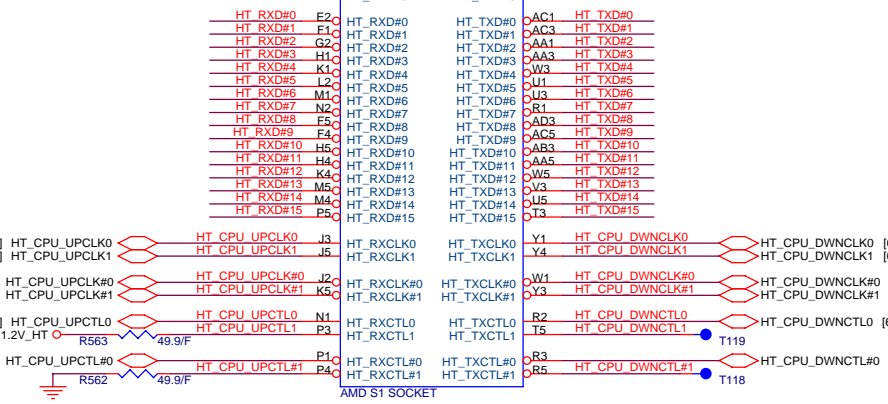
ROUTE TRACES 80ohm DIFF IMPEDENCE 8/5/20 SPACING



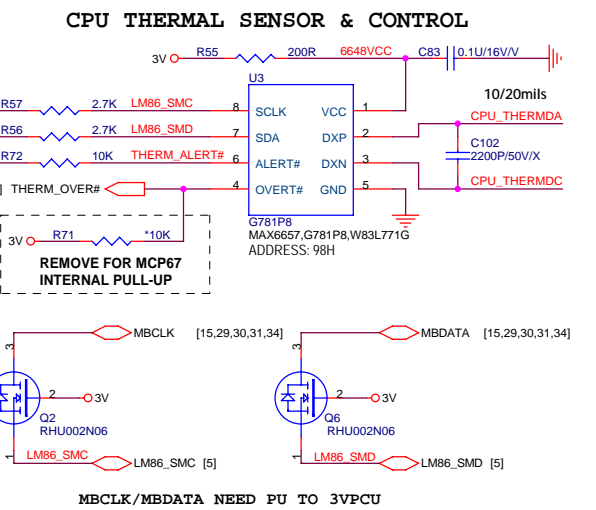
If AMD SI is not used SID can be left, SIC 300ohm to VSS.



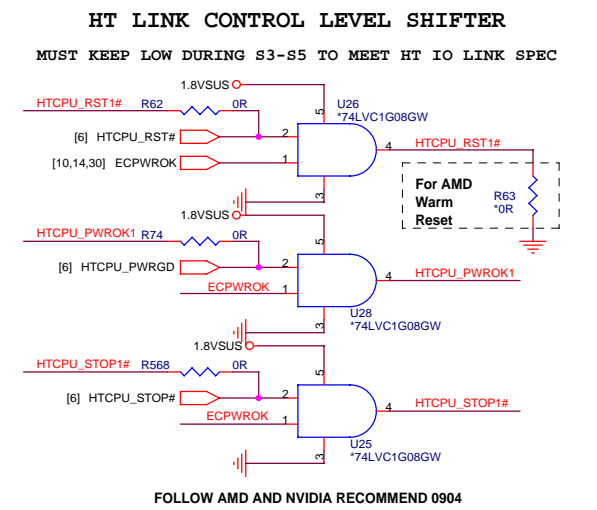
KEEP TRACE RESISTOR <0.6" FROM CPU AND TRACE TO AC CAP <1.25" CPUVID1 PU REQUIRED FOR COMPATIBILITY WITH FUTURE CPU



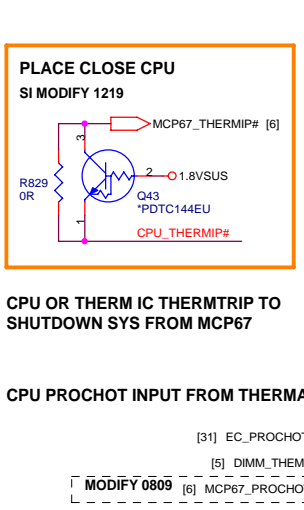
HT\_RXCTL1/HT\_RXCLR#1 MUST <1.5" FROM CPU PIN



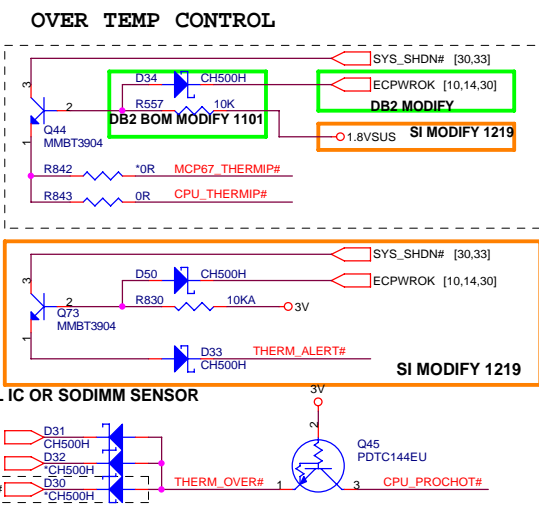
MBCLK/MBDATA NEED PU TO 3VPCU



FOLLOW AMD AND NVIDIA RECOMMEND 0904



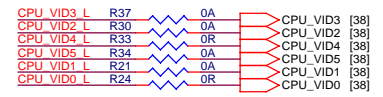
CPU OR THERM IC THERMTRIP TO SHUTDOWN SYS FROM MCP67



CPU PROCHOT INPUT FROM THERMAL IC OR SODIMM SENSOR



NEED TO CONFIRM NVIDIA FOR THE USAGE CONNECTION TO SB



PROJECT : AT1 Quanta Computer Inc. NBS/RD2/HW1. Document Number: CPU (HT\_IF\_CTL). Date: Tuesday, August 21, 2007. Sheet 2 of 40. Rev MV.

U27B

M A DQ63	AA12	MA_DATA[63]
M A DQ62	AB12	MA_DATA[62]
M A DQ61	AA14	MA_DATA[61]
M A DQ60	AB14	MA_DATA[60]
M A DQ59	Y11	MA_DATA[59]
M A DQ58	Y12	MA_DATA[58]
M A DQ57	AD13	MA_DATA[57]
M A DQ56	AB13	MA_DATA[56]
M A DQ55	AD15	MA_DATA[55]
M A DQ54	AB15	MA_DATA[54]
M A DQ53	AB17	MA_DATA[53]
M A DQ52	Y17	MA_DATA[52]
M A DQ51	Y14	MA_DATA[51]
M A DQ50	W14	MA_DATA[50]
M A DQ49	W16	MA_DATA[49]
M A DQ48	AD17	MA_DATA[48]
M A DQ47	Y18	MA_DATA[47]
M A DQ46	AD19	MA_DATA[46]
M A DQ45	AD21	MA_DATA[45]
M A DQ44	AB21	MA_DATA[44]
M A DQ43	AB18	MA_DATA[43]
M A DQ42	AA18	MA_DATA[42]
M A DQ41	AA20	MA_DATA[41]
M A DQ40	Y20	MA_DATA[40]
M A DQ39	AA22	MA_DATA[39]
M A DQ38	Y22	MA_DATA[38]
M A DQ37	W21	MA_DATA[37]
M A DQ36	W22	MA_DATA[36]
M A DQ35	AA21	MA_DATA[35]
M A DQ34	AB22	MA_DATA[34]
M A DQ33	AB24	MA_DATA[33]
M A DQ32	Y24	MA_DATA[32]
M A DQ31	H22	MA_DATA[31]
M A DQ30	H20	MA_DATA[30]
M A DQ29	E22	MA_DATA[29]
M A DQ28	E21	MA_DATA[28]
M A DQ27	J19	MA_DATA[27]
M A DQ26	H24	MA_DATA[26]
M A DQ25	F22	MA_DATA[25]
M A DQ24	F20	MA_DATA[24]
M A DQ23	C23	MA_DATA[23]
M A DQ22	B22	MA_DATA[22]
M A DQ21	F18	MA_DATA[21]
M A DQ20	E18	MA_DATA[20]
M A DQ19	E20	MA_DATA[19]
M A DQ18	D22	MA_DATA[18]
M A DQ17	C19	MA_DATA[17]
M A DQ16	G18	MA_DATA[16]
M A DQ15	G17	MA_DATA[15]
M A DQ14	C17	MA_DATA[14]
M A DQ13	F14	MA_DATA[13]
M A DQ12	E14	MA_DATA[12]
M A DQ11	H17	MA_DATA[11]
M A DQ10	E17	MA_DATA[10]
M A DQ9	E15	MA_DATA[9]
M A DQ8	H15	MA_DATA[8]
M A DQ7	E13	MA_DATA[7]
M A DQ6	C13	MA_DATA[6]
M A DQ5	H12	MA_DATA[5]
M A DQ4	H11	MA_DATA[4]
M A DQ3	G14	MA_DATA[3]
M A DQ2	H14	MA_DATA[2]
M A DQ1	F12	MA_DATA[1]
M A DQ0	G12	MA_DATA[0]

Y13	M A DQM7
AB16	M A DQM6
Y19	M A DQM5
AC24	M A DQM4
F24	M A DQM3
E19	M A DQM2
C15	M A DQM1
E12	M A DQM0

W12	M A DQS7
Y15	M A DQS6
AB19	M A DQS5
AD23	M A DQS4
G22	M A DQS3
G16	M A DQS1
G13	M A DQS0

W13	M A DQS#7
W15	M A DQS#6
AB20	M A DQS#5
AC23	M A DQS#4
G21	M A DQS#3
C21	M A DQS#2
G15	M A DQS#1
H13	M A DQS#0

E16	M A CLK1
F16	M A CLK1#

Y16	M A CLK2
AA16	M A CLK2#

K22	M A BA2
R20	M A BA1
T22	M A BA0

T20	M A RAS#
U20	M A CAS#
U21	M A WE#

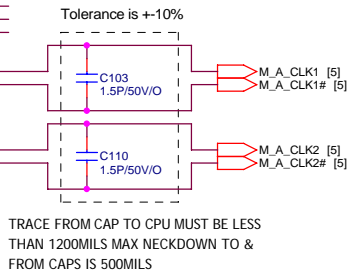
V19	M A CS#3
J22	M A CS#2
V22	M A CS#1
T19	M A CS#0

J20	M A CKE1
J21	M A CKE0

V20	M A ODT1
U19	M A ODT0



U27C

M B DQ63	AD11	MB_DATA[63]
M B DQ62	AE11	MB_DATA[62]
M B DQ61	AE14	MB_DATA[61]
M B DQ60	AE14	MB_DATA[60]
M B DQ59	Y11	MB_DATA[59]
M B DQ58	AB11	MB_DATA[58]
M B DQ57	AC12	MB_DATA[57]
M B DQ56	AE13	MB_DATA[56]
M B DQ55	AE15	MB_DATA[55]
M B DQ54	AE16	MB_DATA[54]
M B DQ53	AC18	MB_DATA[53]
M B DQ52	AE19	MB_DATA[52]
M B DQ51	AD14	MB_DATA[51]
M B DQ50	AC14	MB_DATA[50]
M B DQ49	AE18	MB_DATA[49]
M B DQ48	AD18	MB_DATA[48]
M B DQ47	AD20	MB_DATA[47]
M B DQ46	AC20	MB_DATA[46]
M B DQ45	AE23	MB_DATA[45]
M B DQ44	AE24	MB_DATA[44]
M B DQ43	AE20	MB_DATA[43]
M B DQ42	AE20	MB_DATA[42]
M B DQ41	AD22	MB_DATA[41]
M B DQ40	AC22	MB_DATA[40]
M B DQ39	AE25	MB_DATA[39]
M B DQ38	AD26	MB_DATA[38]
M B DQ37	AA25	MB_DATA[37]
M B DQ36	AA26	MB_DATA[36]
M B DQ35	AE24	MB_DATA[35]
M B DQ34	AD24	MB_DATA[34]
M B DQ33	AA23	MB_DATA[33]
M B DQ32	AA24	MB_DATA[32]
M B DQ31	G24	MB_DATA[31]
M B DQ30	G23	MB_DATA[30]
M B DQ29	D26	MB_DATA[29]
M B DQ28	C26	MB_DATA[28]
M B DQ27	G26	MB_DATA[27]
M B DQ26	G25	MB_DATA[26]
M B DQ25	C25	MB_DATA[25]
M B DQ24	E23	MB_DATA[24]
M B DQ23	C24	MB_DATA[23]
M B DQ22	B24	MB_DATA[22]
M B DQ21	C20	MB_DATA[21]
M B DQ20	B20	MB_DATA[20]
M B DQ19	D24	MB_DATA[19]
M B DQ18	D24	MB_DATA[18]
M B DQ17	A21	MB_DATA[17]
M B DQ16	D20	MB_DATA[16]
M B DQ15	D18	MB_DATA[15]
M B DQ14	C18	MB_DATA[14]
M B DQ13	D14	MB_DATA[13]
M B DQ12	C14	MB_DATA[12]
M B DQ11	A20	MB_DATA[11]
M B DQ10	A19	MB_DATA[10]
M B DQ9	A16	MB_DATA[9]
M B DQ8	A15	MB_DATA[8]
M B DQ7	A13	MB_DATA[7]
M B DQ6	D12	MB_DATA[6]
M B DQ5	E11	MB_DATA[5]
M B DQ4	G11	MB_DATA[4]
M B DQ3	B14	MB_DATA[3]
M B DQ2	A14	MB_DATA[2]
M B DQ1	A11	MB_DATA[1]
M B DQ0	C11	MB_DATA[0]

AD12	M B DQM7
AC16	M B DQM6
AE22	M B DQM5
AB26	M B DQM4
E25	M B DQM3
A22	M B DQM2
B16	M B DQM1
A12	M B DQM0

AF12	M B DQS7
AE16	M B DQS6
AF21	M B DQS5
AC25	M B DQS4
F26	M B DQS3
A24	M B DQS2
D16	M B DQS1
C12	M B DQS0

AF12	M B DQS#7
AD16	M B DQS#6
AF22	M B DQS#5
AC26	M B DQS#4
E26	M B DQS#3
A23	M B DQS#2
C16	M B DQS#1
B12	M B DQS#0

A17	M B CLK1
A18	M B CLK1#

AF18	M B CLK2
AF17	M B CLK2#

K26	M B BA2
T26	M B BA1
U26	M B BA0

U24	M B RAS#
V26	M B CAS#
U22	M B WE#

Y26	M B CS#3
J24	M B CS#2
W24	M B CS#1
U23	M B CS#0

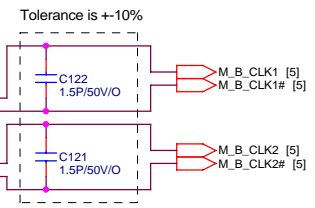
H26	M B CKE1
J23	M B CKE0

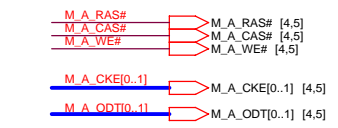
W23	M B ODT1
W26	M B ODT0

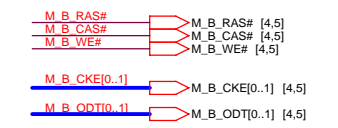
Y10	VTERM_FB
-----	----------



- [5] M\_A\_DQ[0..63] <-> M\_A\_DQ[0..63]
- [4..5] M\_A\_A[0..15] <-> M\_A\_A[0..15]
- [5] M\_A\_DQM[0..7] <-> M\_A\_DQM[0..7]
- [5] M\_A\_DQS[0..7] <-> M\_A\_DQS[0..7]
- [5] M\_A\_DQS#[0..7] <-> M\_A\_DQS#[0..7]
- [4..5] M\_A\_BA[0..2] <-> M\_A\_BA[0..2]
- [4..5] M\_A\_CS#[0..3] <-> M\_A\_CS#[0..3]



- [5] M\_B\_DQ[0..63] <-> M\_B\_DQ[0..63]
- [4..5] M\_B\_A[0..15] <-> M\_B\_A[0..15]
- [5] M\_B\_DQM[0..7] <-> M\_B\_DQM[0..7]
- [5] M\_B\_DQS[0..7] <-> M\_B\_DQS[0..7]
- [5] M\_B\_DQS#[0..7] <-> M\_B\_DQS#[0..7]
- [4..5] M\_B\_BA[0..2] <-> M\_B\_BA[0..2]
- [4..5] M\_B\_CS#[0..3] <-> M\_B\_CS#[0..3]

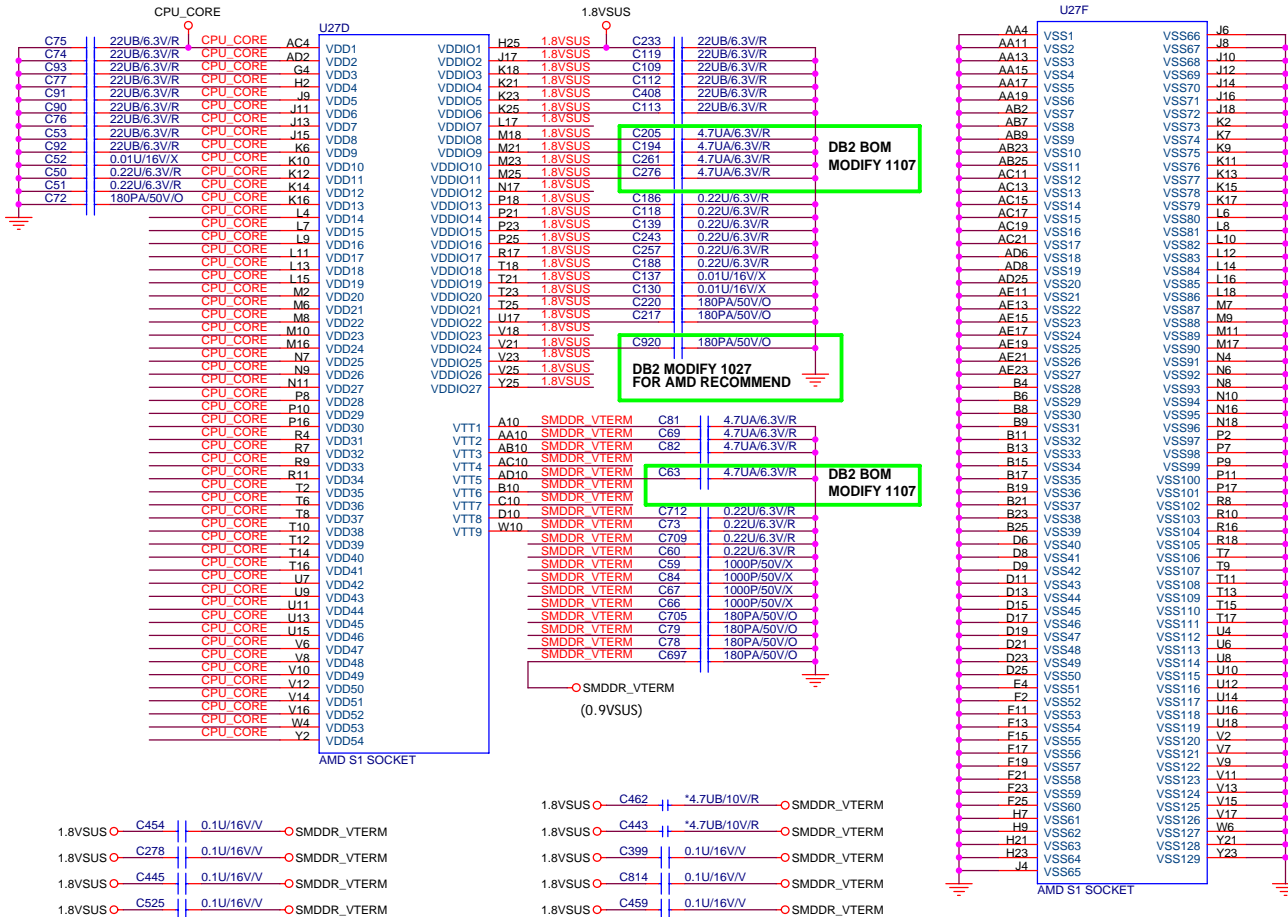


1.8VSUS [2,4,5,6,32,36,37]

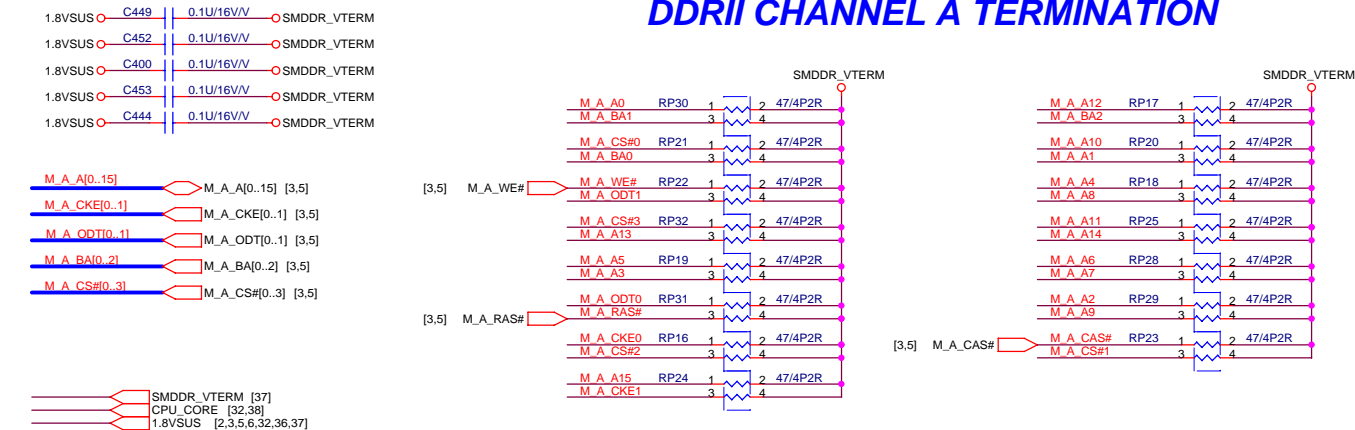
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number CPU (MEM_I/F)	Rev MV
Date: Tuesday, August 21, 2007		
Sheet 3 of 40		

# CPU POWER PLANE AND BY PASS CAP

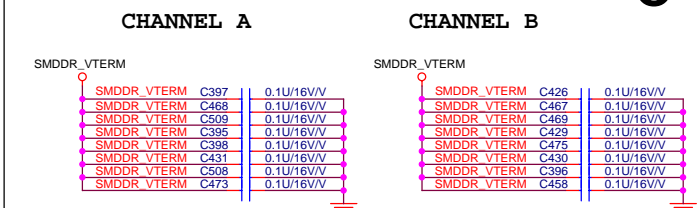


## DDRII CHANNEL A TERMINATION



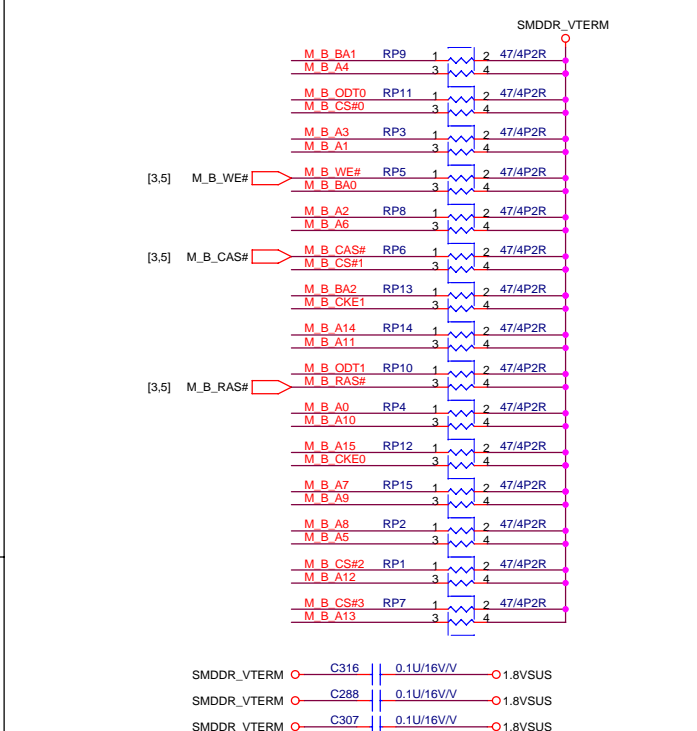
# DDR2 TERMINATION BYPASS CAP

04



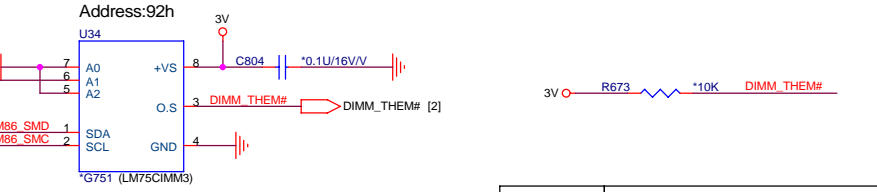
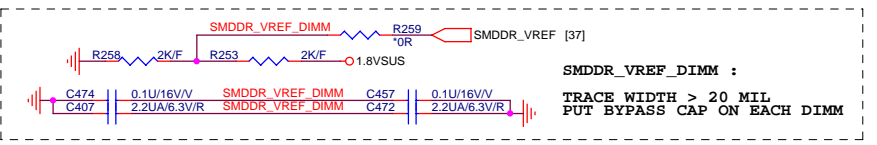
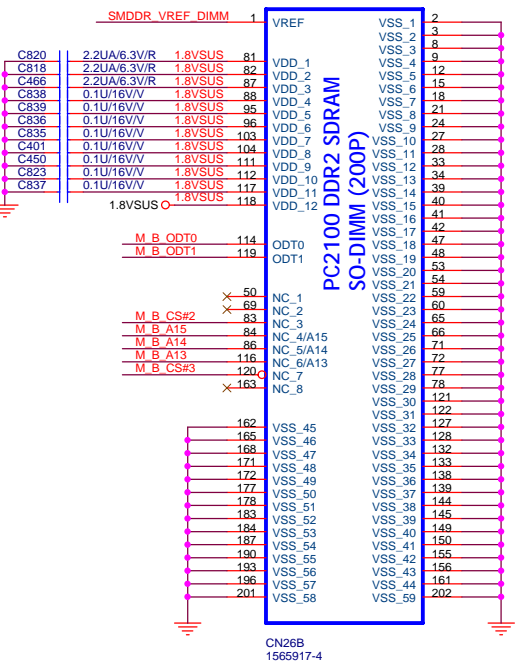
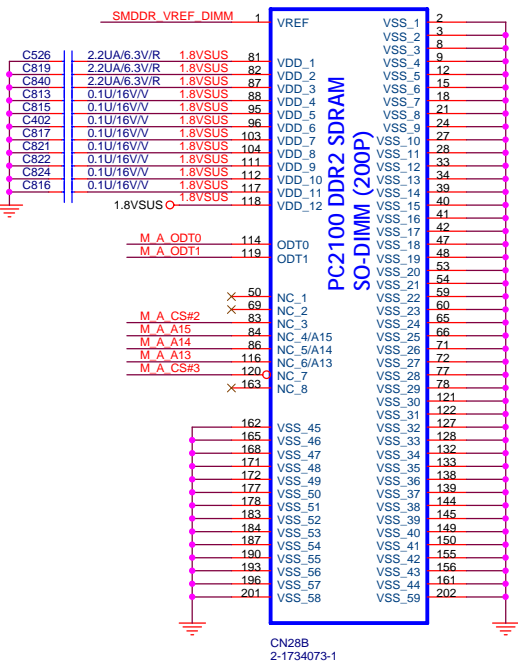
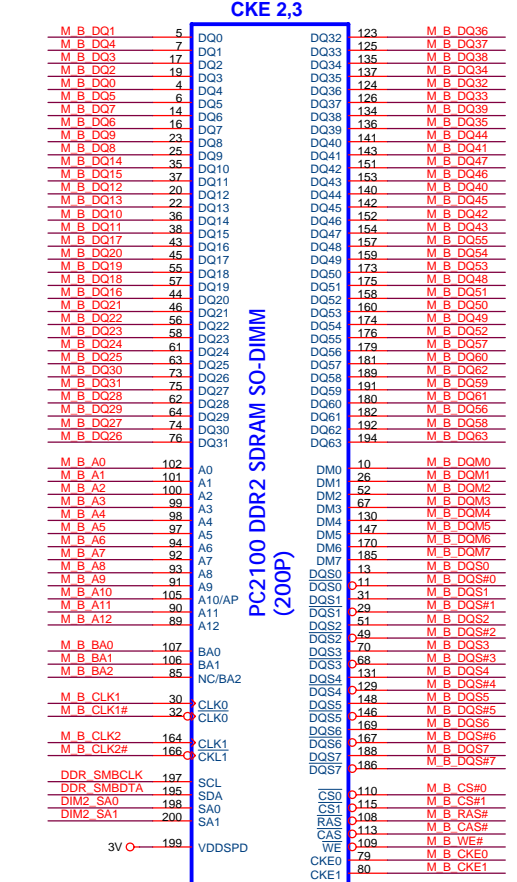
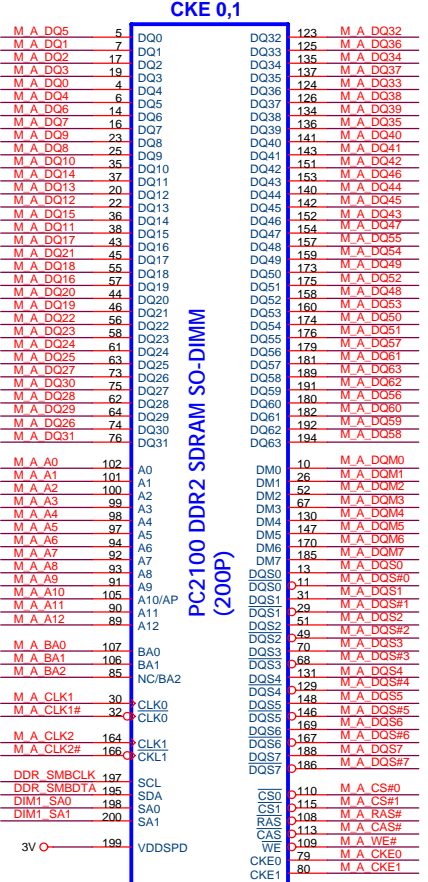
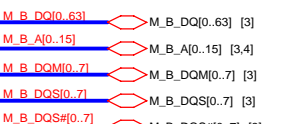
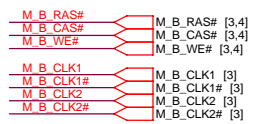
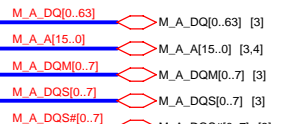
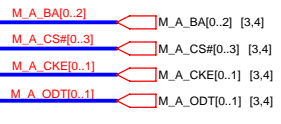
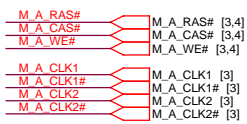
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM

## DDRII CHANNEL B TERMINATION



**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number CPU (POWER,GND),DDR2_TERM	Rev MV
Date: Tuesday, August 21, 2007	Sheet 4 of 40	



CKE 0,1

CKE 2,3

PC2100 DDR2 SDRAM SO-DIMM (200P)

PC2100 DDR2 SDRAM SO-DIMM (200P)

HEIGHT=9.2mm

HEIGHT=5.2mm

SMBus address A0

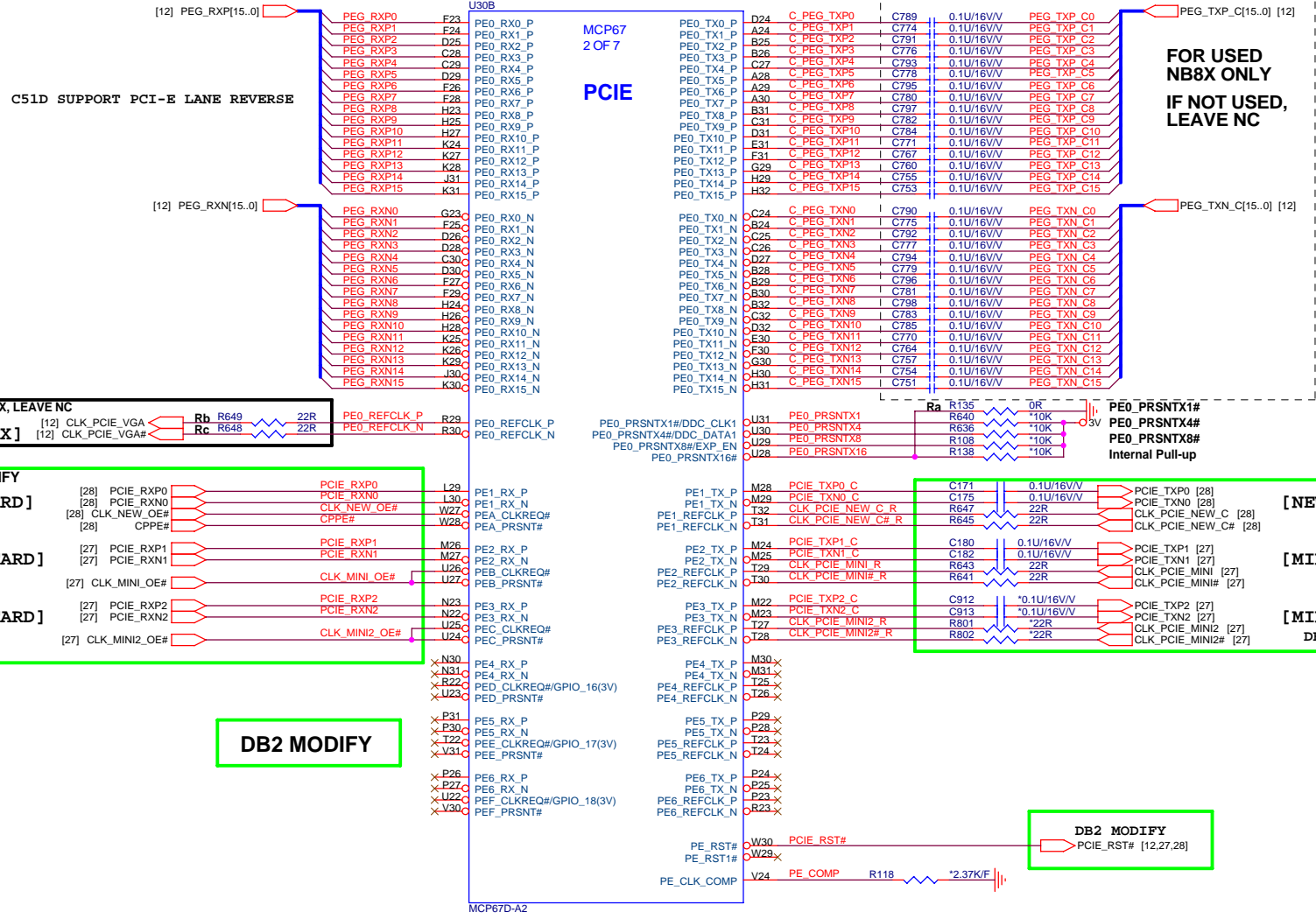
SMBus address A2

TRACE WIDTH > 20 MIL PUT BYPASS CAP ON EACH DIMM

Address:92h

PROJECT : AT1 Quanta Computer Inc. Size Custom Document Number DDR SO-DIMMx2 (200P) Rev MV Date: Tuesday, August 21, 2007 Sheet 5 of 40





**MCP67D & MCP67M DIFFERENCE TABLE**

LOCATION	MCP67M (UMA)	MCP67M (DISCRETE)	MCP67D (DISCRETE)
Ra	NC	0R	0R
Rb Rc	NC NC	22R 22R	22R 22R

NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	NC

IF NOT USED NB8X, LEAVE NC  
 [12] CLK\_PCIE\_VGA# Rb R649 22R PE0\_REFCLK\_P R29  
 [12] CLK\_PCIE\_VGA# Rc R648 22R PE0\_REFCLK\_N R30

**DB2 MODIFY [NEW CARD]**

- [28] PCIE\_RXP0 PCIE\_RXP0 L29 PE1\_RX\_P
- [28] PCIE\_RXN0 PCIE\_RXN0 L30 PE1\_RX\_N
- [28] CLK\_NEW\_OE# CLK\_NEW\_OE# W27 PE1\_CLKREQ#
- [28] CPPE# CPPE# W29 PE1\_PRSNT#

**[MINI CARD]**

- [27] PCIE\_RXP1 PCIE\_RXP1 M26 PE2\_RX\_P
- [27] PCIE\_RXN1 PCIE\_RXN1 M27 PE2\_RX\_N
- [27] CLK\_MINI\_OE# CLK\_MINI\_OE# U26 PE2\_CLKREQ#
- [27] PE2\_PRSNT#

**[MINI CARD]**

- [27] PCIE\_RXP2 PCIE\_RXP2 N23 PE3\_RX\_P
- [27] PCIE\_RXN2 PCIE\_RXN2 N22 PE3\_RX\_N
- [27] CLK\_MINI2\_OE# CLK\_MINI2\_OE# U25 PE3\_CLKREQ#
- [27] PE3\_PRSNT#

**[NEW CARD]**

- C171 0.1U/16V/V PEG\_TXP\_C0 PCIE\_TXP0 [28]
- C175 0.1U/16V/V PEG\_TXN\_C0 PCIE\_TXN0 [28]
- R647 22R CLK\_PCIE\_NEW\_C\_R CLK\_PCIE\_NEW\_C [28]
- R645 22R CLK\_PCIE\_NEW\_C#\_R CLK\_PCIE\_NEW\_C# [28]

**[MINI CARD]**

- C180 0.1U/16V/V PEG\_TXP\_C1 PCIE\_TXP1 [27]
- C182 0.1U/16V/V PEG\_TXN\_C1 PCIE\_TXN1 [27]
- R643 22R CLK\_PCIE\_MINI\_R CLK\_PCIE\_MINI [27]
- R641 22R CLK\_PCIE\_MINI#\_R CLK\_PCIE\_MINI# [27]

**[MINI CARD] DB2 MODIFY**

- C912 \*0.1U/16V/V PEG\_TXP\_C2 PCIE\_TXP2 [27]
- C913 \*0.1U/16V/V PEG\_TXN\_C2 PCIE\_TXN2 [27]
- R801 \*22R CLK\_PCIE\_MINI2\_R CLK\_PCIE\_MINI2 [27]
- R802 \*22R CLK\_PCIE\_MINI2#\_R CLK\_PCIE\_MINI2# [27]

**DB2 MODIFY**

- N30 PE4\_RX\_P
- N31 PE4\_RX\_N
- R22 PE4\_CLKREQ#/GPIO\_16(3V)
- U23 PE4\_PRSNT#
- P31 PE5\_RX\_P
- P30 PE5\_RX\_N
- T22 PE5\_CLKREQ#/GPIO\_17(3V)
- U24 PE5\_PRSNT#
- P28 PE6\_RX\_P
- P27 PE6\_RX\_N
- U22 PE6\_CLKREQ#/GPIO\_18(3V)
- V30 PE6\_PRSNT#

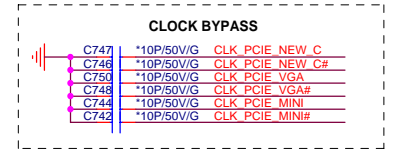
**DB2 MODIFY**

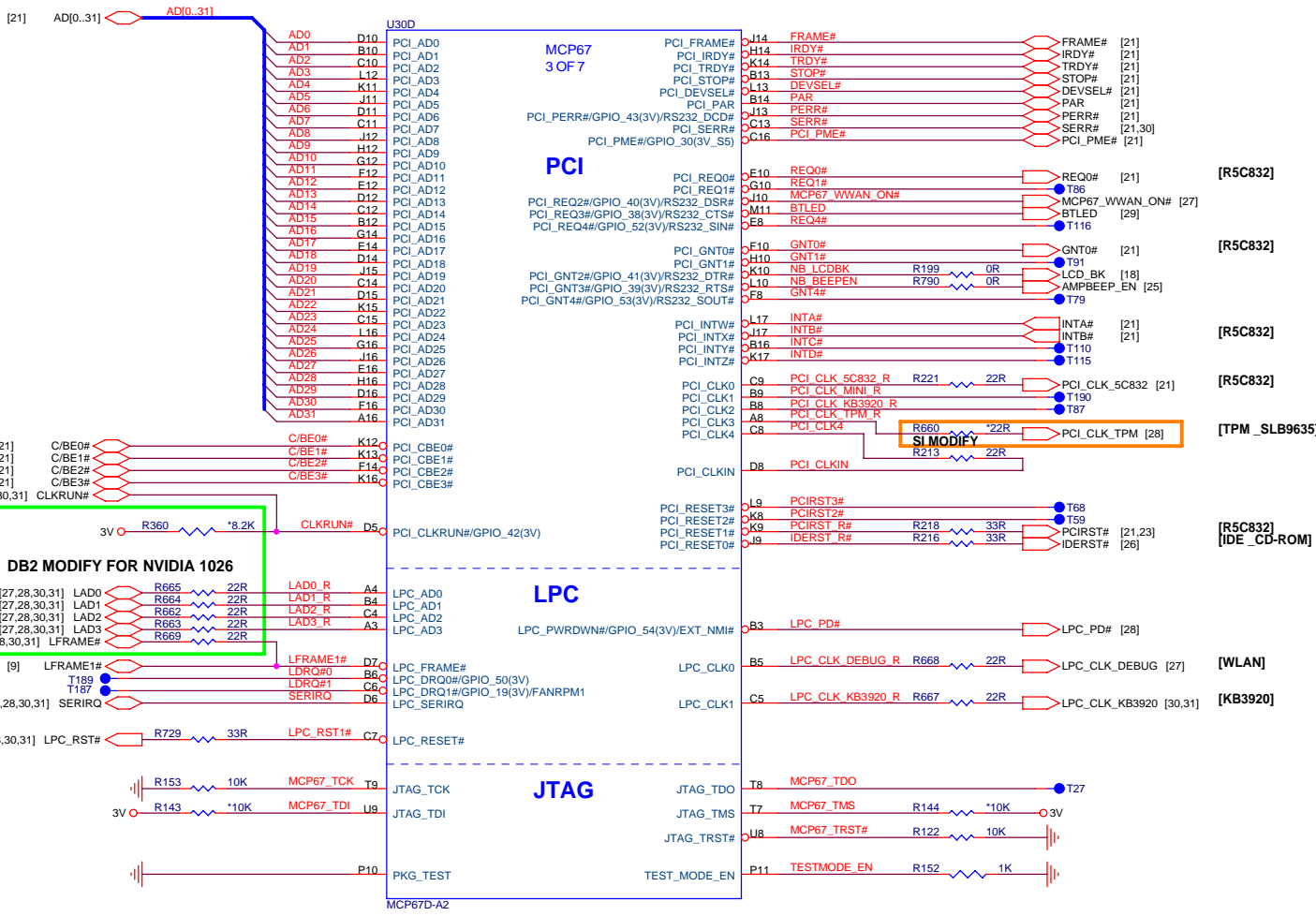
- W30 PCIE\_RST#
- W29 PE\_RST#
- V24 PE\_COMP R118 \*2.37K/F

**MV MODIFY 0423**

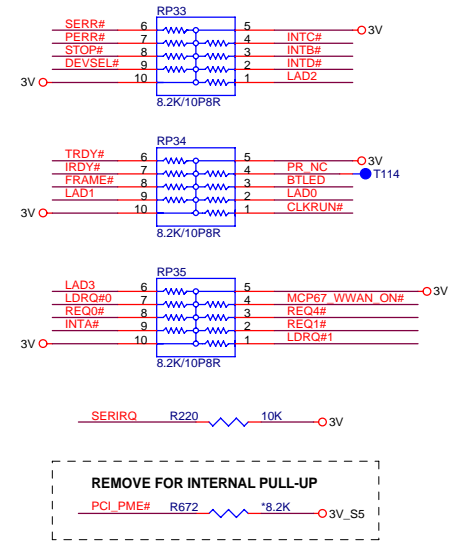
**DB2 MODIFY 1025**  
 Ra,Rb IF NOT USED : LEAVE NC (INTERNAL PU)

- R811 10K
- R812 \*10K
- R813 10K
- R98 \*10K
- R109 \*10K
- R107 \*10K

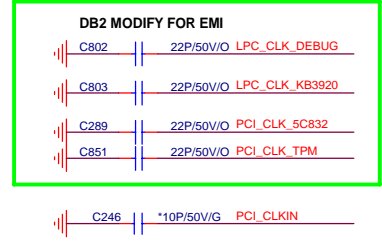




**PCI/LPC PULL-UP**



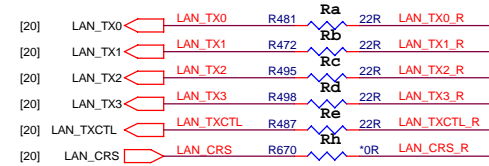
**CLOCK BYPASS**



3V [2,5,6,7,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]  
 3V\_S5 [9,10,11,20,28,30,32,33,37]

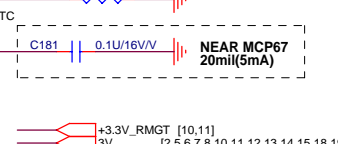
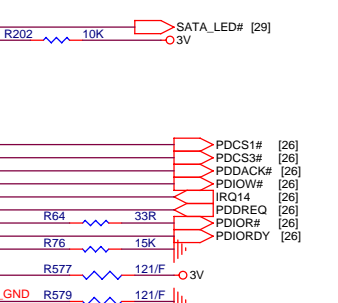
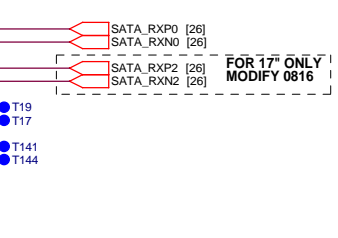
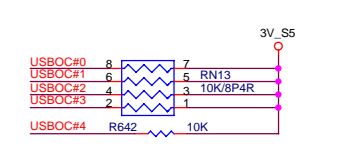
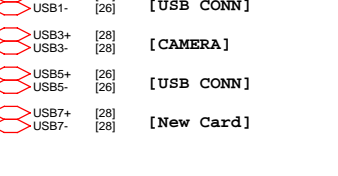
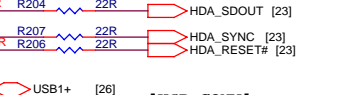
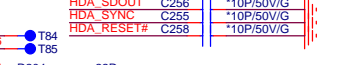
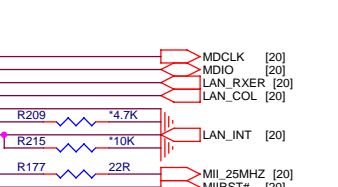
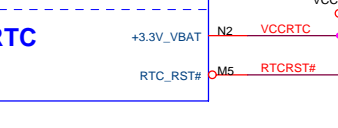
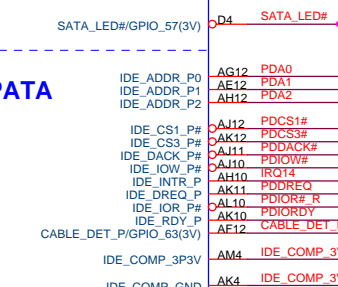
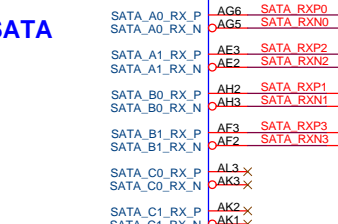
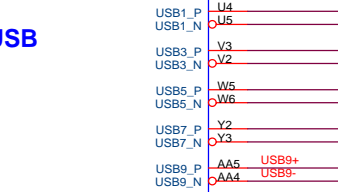
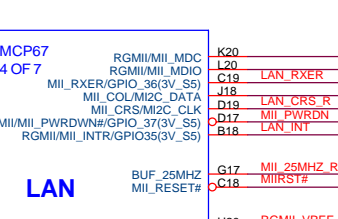
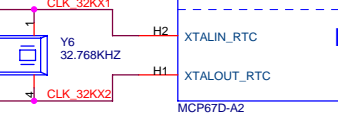
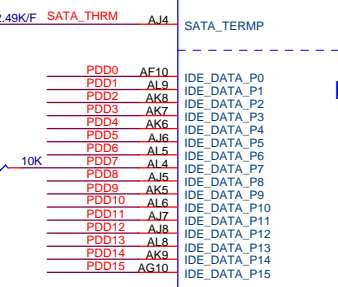
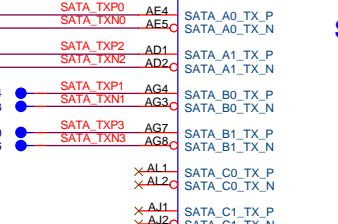
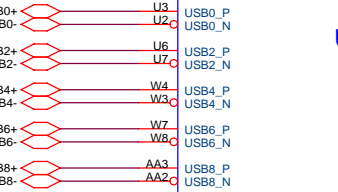
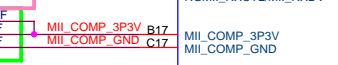
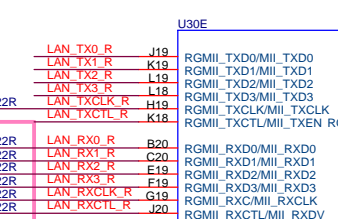
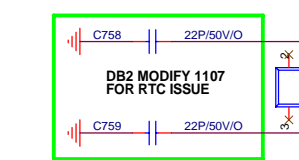
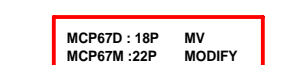
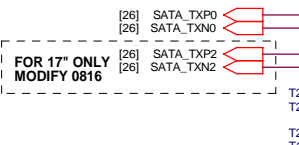
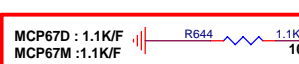
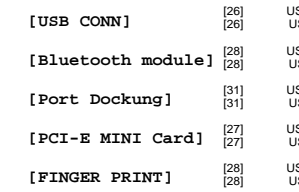
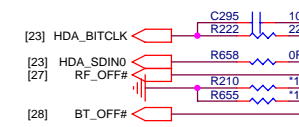
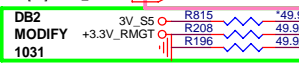
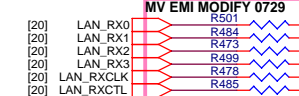
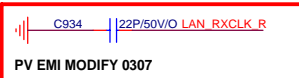
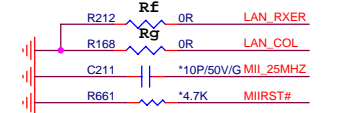


10/100 - GIAG LAN STUFF OPTION

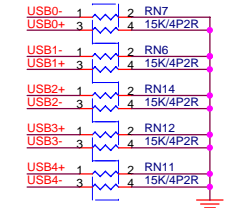


MODIFY 0824

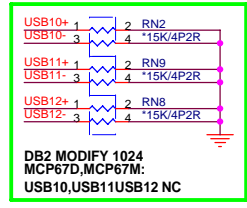
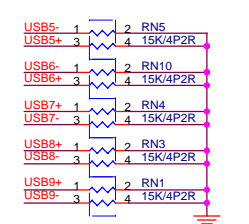
Table with 3 columns: Component, 10/100, GIGA. Rows include Ra, Rb, Rc, Rd, Re, Rf, Rg, Rh.



MODIFY 0823



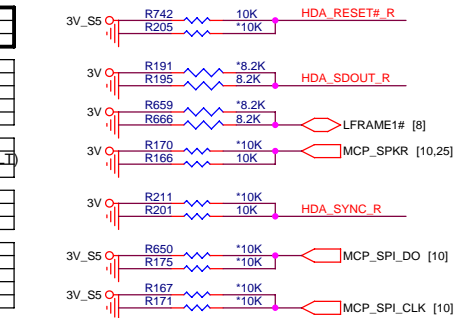
USB PULL-DOWN



MCP67 STRAPPING

Table with 2 columns: Component, Value. Rows include HDA\_RESET# (LAN), HDA\_SDOUT\_R, HDA\_SYNC\_R, MCP\_SPKR, HDA\_SYNC\_R (SIO CLOCK), SPI\_DO, SPI\_CLK (SPI CLOCK).

MODIFY 0824



RTC

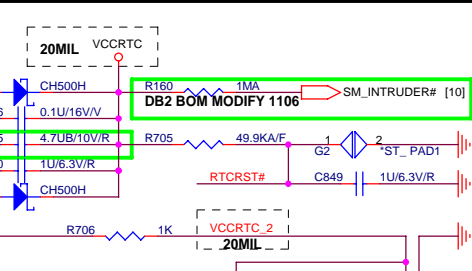
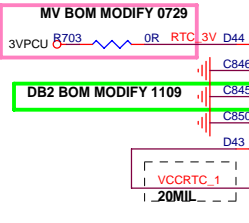
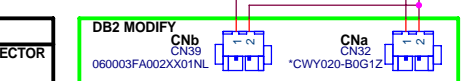


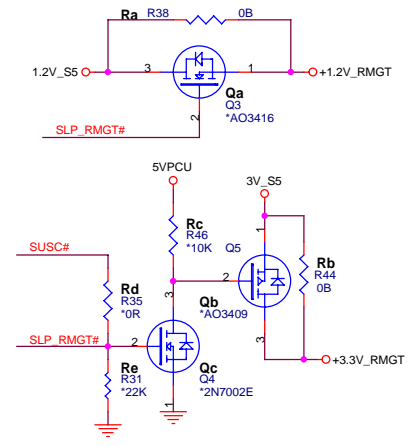
Table with 2 columns: Component, Value. Rows include CNa, CNb, CN32.



PROJECT : AT1 Quanta Computer Inc. Date: Tuesday, August 21, 2007 Sheet 9 of 40

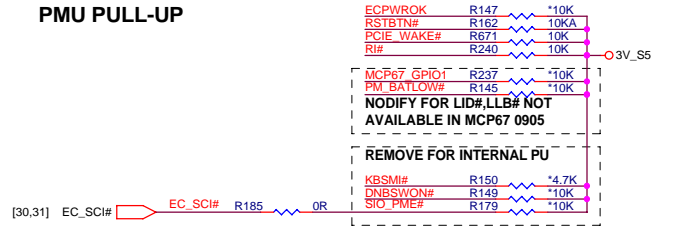
- +3.3V\_RMGTT [10,11]
3V [2,5,6,7,8,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V\_S5 [8,10,11,20,28,30,32,33,37]
3VPCU [14,18,28,29,30,31,33,34,35]

## CORE POWER CIRCUIT FOR SLEEP MODE MCP67M SUPPORT ONLY



	MCP67M UMA	MCP67D DISCRETE
Ra	NC	STUFF
Rb	NC	STUFF
Rc	STUFF	NC
Rd	NC	NC
Re	STUFF	NC
Qa	STUFF	NC
Qb	STUFF	NC
Qc	STUFF	NC

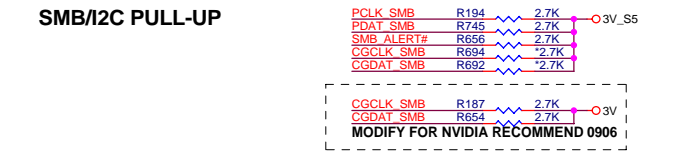
### PMU PULL-UP



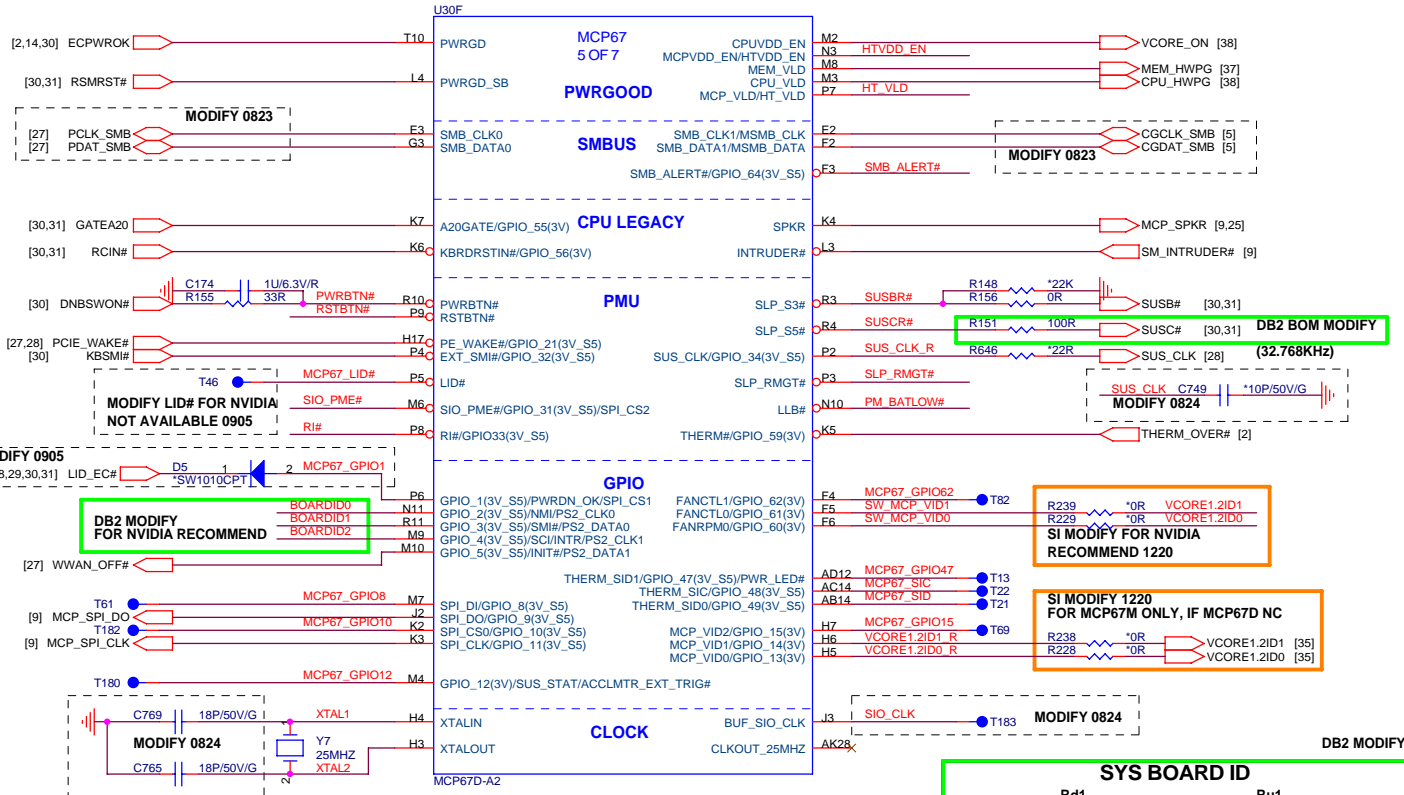
### CPU LEGACY PULL-UP



### SMB/I2C PULL-UP

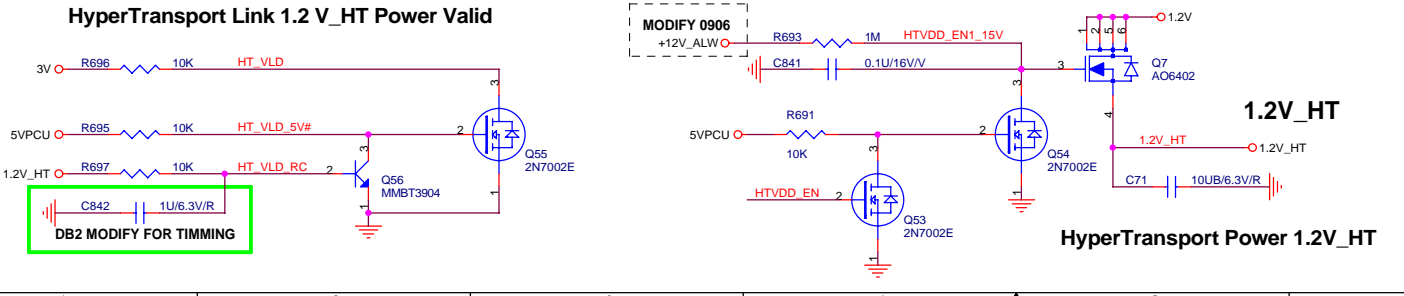


- +1.2V\_RMGT [11]
- 1.2V\_S5 [11,32,35]
- 1.2V\_HT [2,6,11]
- 1.2V [11,12,13,15,36]
- +3.3V\_RMGT [9,11]
- 3V\_S5 [2,5,6,7,8,9,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
- 5VPCU [23,33,34,35,36,37,38]
- +1.2V\_ALW [18,32,33]



Board ID :	0/1	0/1	0/1
DIFINE	RESERVE / RESERVE	UMA / DISCRETE	AT1 / AT2

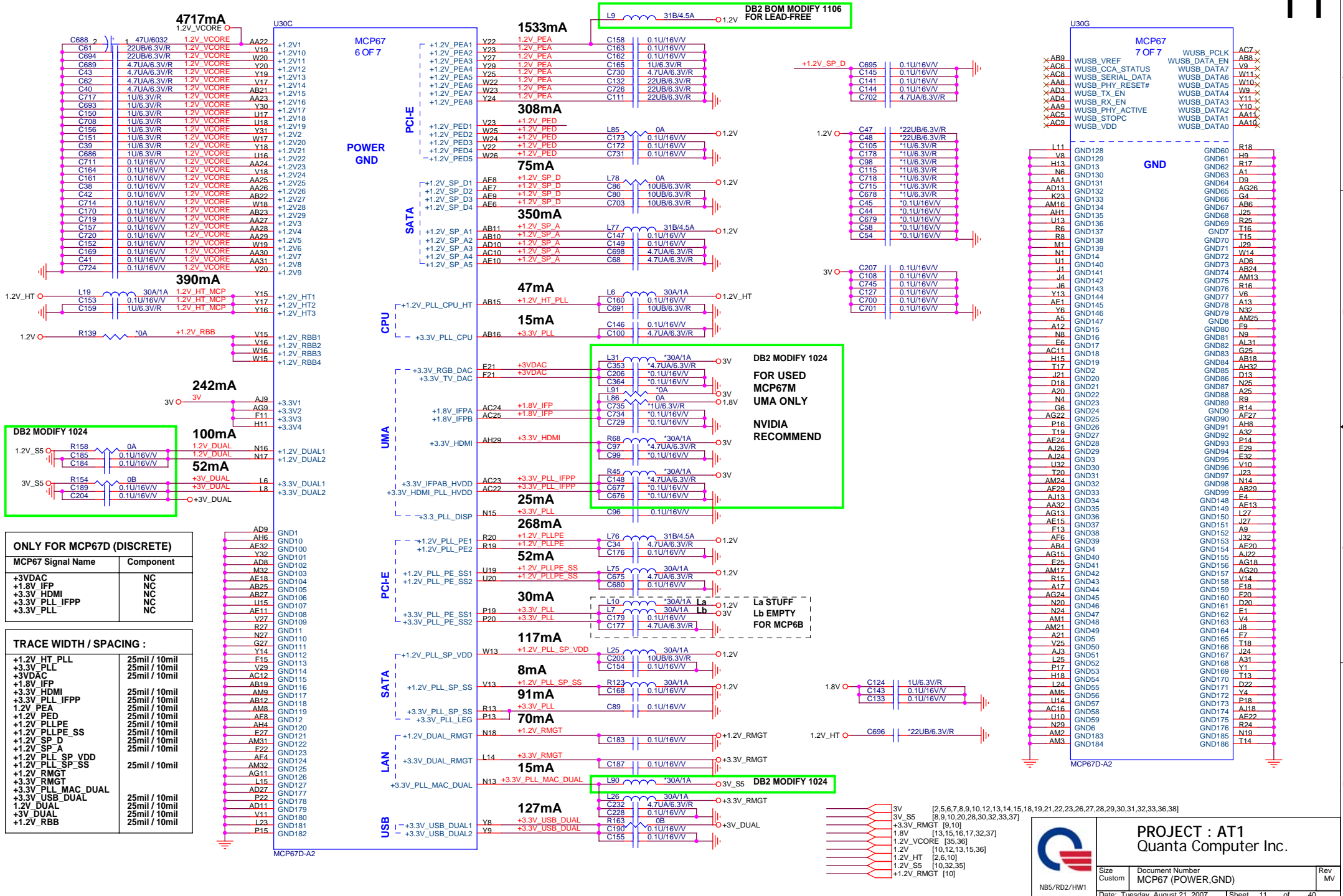
ARES/ARTEMIS 1.0			ARES/ARTEMIS 1.1			SI Setting		PV Setting		ARES/ARTEMIS 1.1	
SKU (BOARD ID)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (UMA)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (UMA)	SKU (BOARD ID)	AT1A (DISCRETE)	AT2A (DISCRETE)	AT1A (DISCRETE)	AT2A (DISCRETE)
Board ID	000	000	001	010	010	011	Board ID	010	111	000	001
ID0 STUFF	Rd1	Rd1	Ru1	Rd1	Rd1	Ru1	ID0 STUFF	Rd1	Ru1	Rd1	Ru1
ID1 STUFF	Rd2	Rd2	Rd2	Ru2	Ru2	Ru2	ID1 STUFF	Ru2	Ru2	Rd2	Rd2
ID2 STUFF	Rd3	Rd3	Rd3	Rd3	Rd3	Rd3	ID2 STUFF	Rd3	Ru3	Rd3	Rd3



**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number MCP67 (PG,SMB,PMU,GPIO,CLK)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 10	of 40

MCP67 POWER PLANE/GND & BYPASS



**ONLY FOR MCP67D (DISCRETE)**

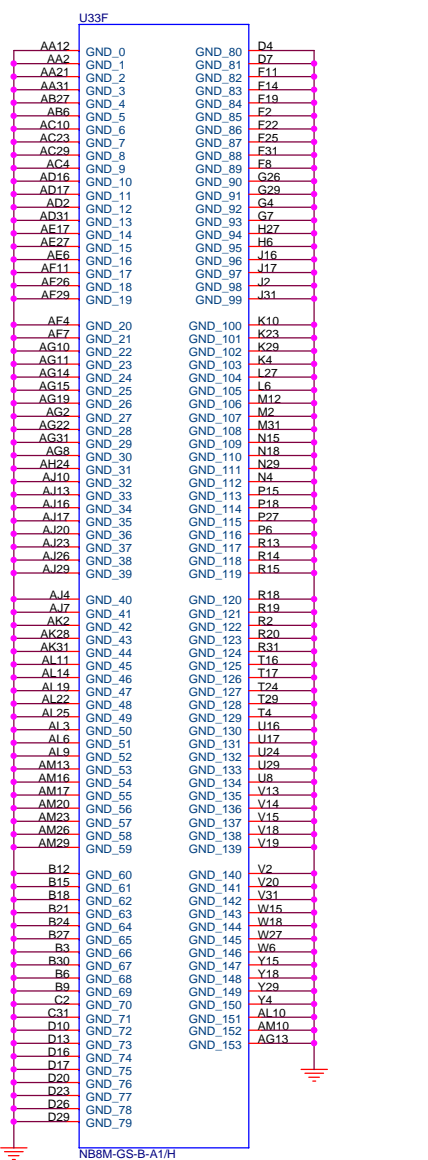
MCP67 Signal Name	Component
+3VDAC	NC
+1.8V_IFP	NC
+3.3V_HDMI	NC
+3.3V_PLL_IFPP	NC
+3.3V_PLL	NC

**TRACE WIDTH / SPACING :**

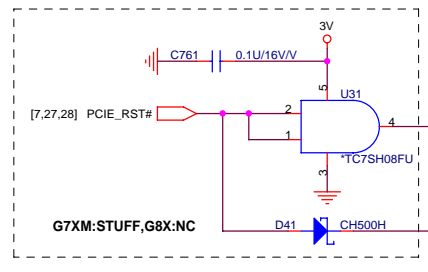
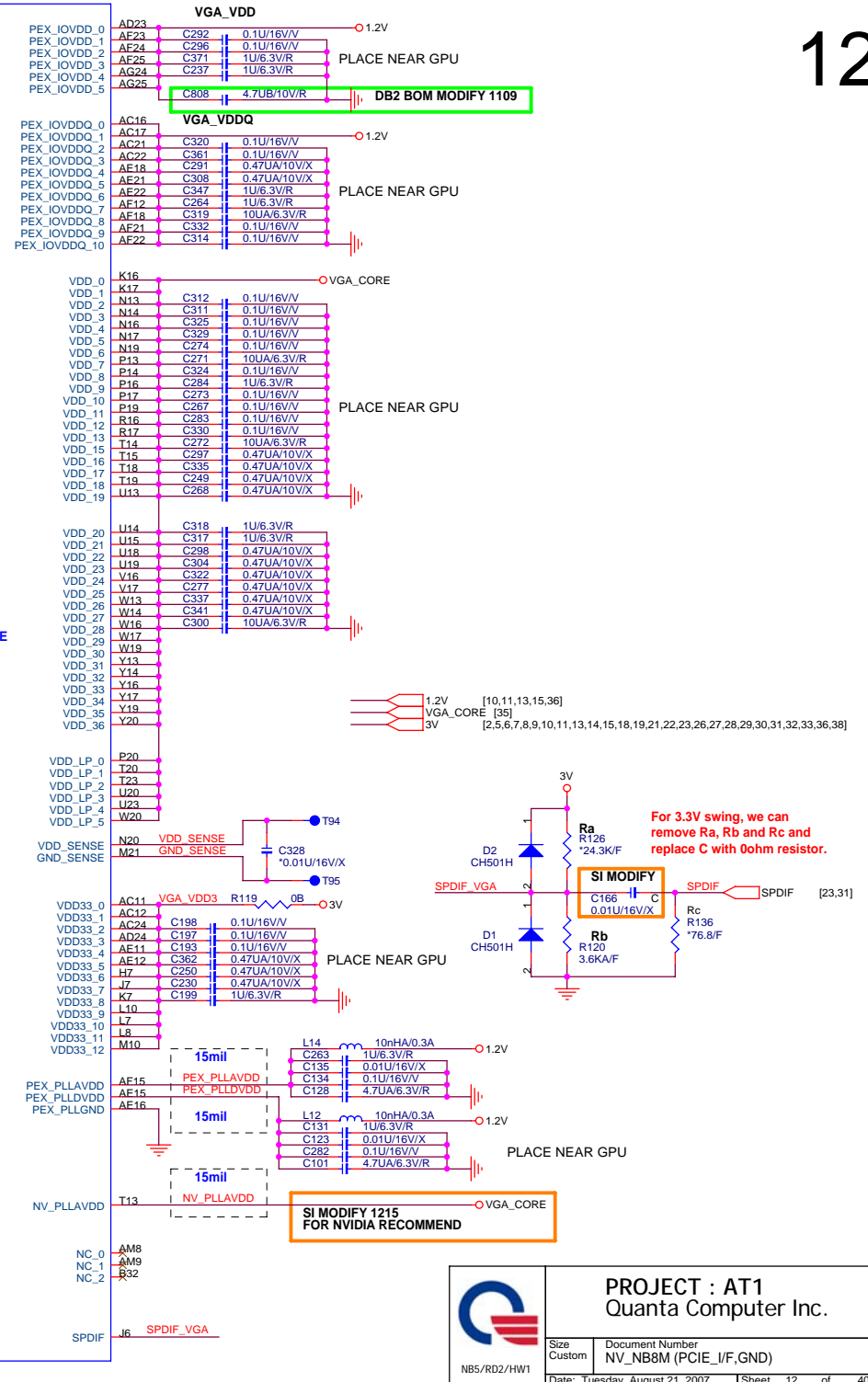
+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFP	25mil / 10mil
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
+1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	25mil / 10mil
+1.2V_PLL_SP_SS	25mil / 10mil
+1.2V_RMGT	25mil / 10mil
+3.3V_RMGT	25mil / 10mil
+3.3V_PLL_MAC_DUAL	25mil / 10mil
+3.3V_USB_DUAL	25mil / 10mil
+1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil

**PROJECT : AT1**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (POWER,GND)	MV
Date: Tuesday, August 21, 2007	Sheet 11 of 40	

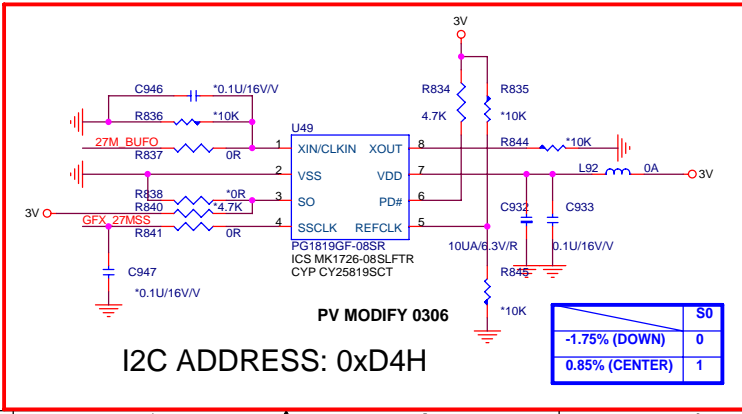
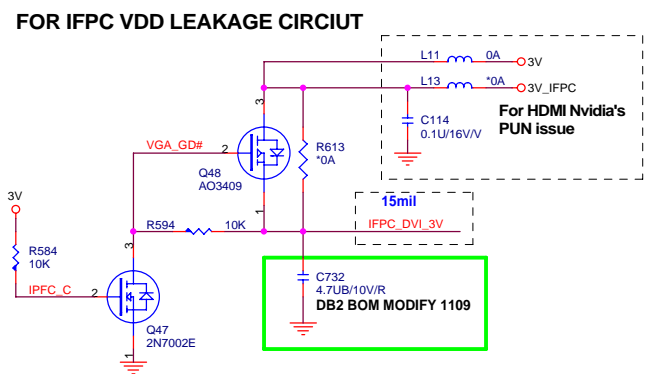
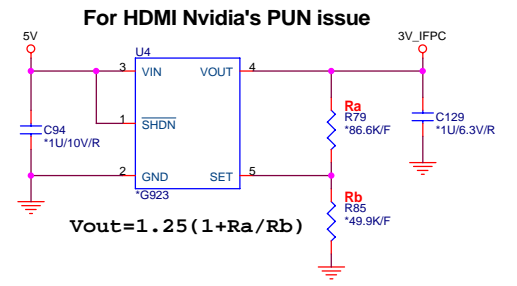
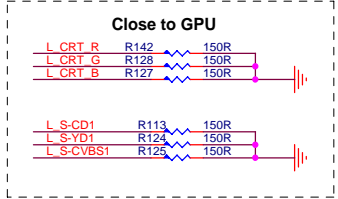
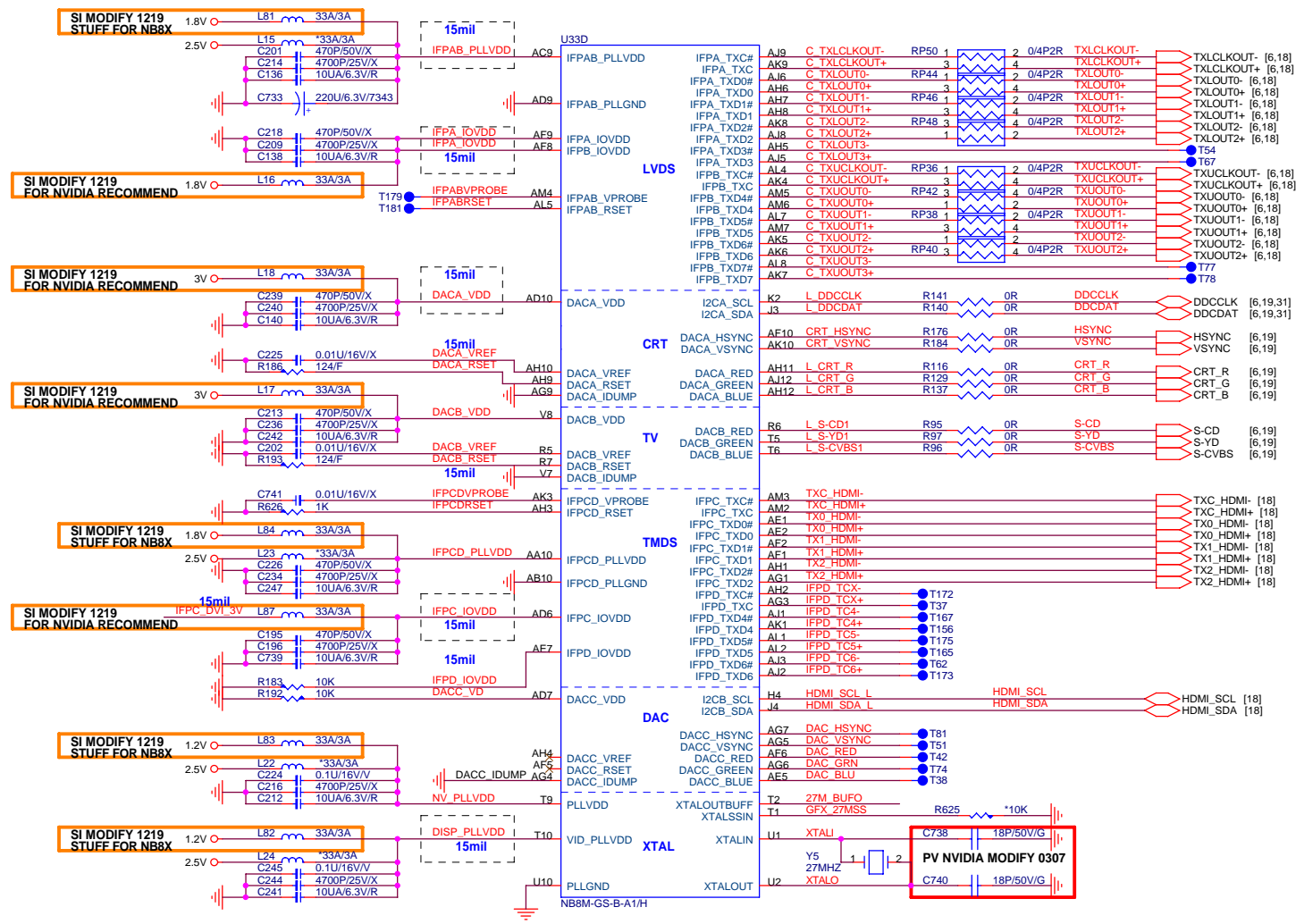


[7]	PEG_RXP0	PEG_RXN0	PEG_RXP0	C215	0.1U/16V/V	C PEG_RXP0	AJ15	PEX_TX0	U33A	PEX_IOVDD_0	AD23	0.1U/16V/V	1.2V	
[7]	PEG_RXP1	PEG_RXN1	PEG_RXP1	C222	0.1U/16V/V	C PEG_RXP1	AH16	PEX_TX1		PEX_IOVDD_1	AE23	0.1U/16V/V		
[7]	PEG_RXP2	PEG_RXN2	PEG_RXP2	C238	0.1U/16V/V	C PEG_RXP2	AG17	PEX_TX2		PEX_IOVDD_2	AE24	0.1U/16V/V		
[7]	PEG_RXP3	PEG_RXN3	PEG_RXP3	C252	0.1U/16V/V	C PEG_RXP3	AG18	PEX_TX3		PEX_IOVDD_3	AE25	1U/6.3V/R		
[7]	PEG_RXP4	PEG_RXN4	PEG_RXP4	C269	0.1U/16V/V	C PEG_RXP4	AJ18	PEX_TX4		PEX_IOVDD_4	AG24	1U/6.3V/R		
[7]	PEG_RXP5	PEG_RXN5	PEG_RXP5	C275	0.1U/16V/V	C PEG_RXP5	AJ19	PEX_TX5		PEX_IOVDD_5	AG25	4.7U/10V/R	DB2 BOM MODIFY 1109	
[7]	PEG_RXP6	PEG_RXN6	PEG_RXP6	C310	0.1U/16V/V	C PEG_RXP6	AG20	PEX_TX6		PEX_IOVDD_6	AC16	0.1U/16V/V		
[7]	PEG_RXP7	PEG_RXN7	PEG_RXP7	C285	0.1U/16V/V	C PEG_RXP7	AG21	PEX_TX7		PEX_IOVDD_7	AC17	0.1U/16V/V	1.2V	
[7]	PEG_RXP8	PEG_RXN8	PEG_RXP8	C309	0.1U/16V/V	C PEG_RXP8	AK21	PEX_TX8		PEX_IOVDD_8	AC21	C320	0.1U/16V/V	
[7]	PEG_RXP9	PEG_RXN9	PEG_RXP9	C326	0.1U/16V/V	C PEG_RXP9	AJ22	PEX_TX9		PEX_IOVDD_9	AC22	C361	0.1U/16V/V	
[7]	PEG_RXP10	PEG_RXN10	PEG_RXP10	C334	0.1U/16V/V	C PEG_RXP10	AH22	PEX_TX10		PEX_IOVDD_10	AC24	C291	0.47U/10V/X	
[7]	PEG_RXP11	PEG_RXN11	PEG_RXP11	C346	0.1U/16V/V	C PEG_RXP11	AK24	PEX_TX11		PEX_IOVDD_11	AE12	C308	0.47U/10V/X	
[7]	PEG_RXP12	PEG_RXN12	PEG_RXP12	C359	0.1U/16V/V	C PEG_RXP12	AJ25	PEX_TX12		PEX_IOVDD_12	AE22	C347	1U/6.3V/R	
[7]	PEG_RXP13	PEG_RXN13	PEG_RXP13	C373	0.1U/16V/V	C PEG_RXP13	AH26	PEX_TX13		PEX_IOVDD_13	AE12	C264	1U/6.3V/R	
[7]	PEG_RXP14	PEG_RXN14	PEG_RXP14	C367	0.1U/16V/V	C PEG_RXP14	AK27	PEX_TX14		PEX_IOVDD_14	AE18	C319	10U/6.3V/R	
[7]	PEG_RXP15	PEG_RXN15	PEG_RXP15	C375	0.1U/16V/V	C PEG_RXP15	AJ28	PEX_TX15		PEX_IOVDD_15	AE21	C332	0.1U/16V/V	
[7]	PEG_TXP_C0	PEG_TXN_C0	PEG_TXP_C0	AK13				PEX_RX0		VDD_0	K16	0.1U/16V/V	VGA_CORE	
[7]	PEG_TXP_C1	PEG_TXN_C1	PEG_TXP_C1	AM14				PEX_RX1		VDD_1	N13	0.1U/16V/V		
[7]	PEG_TXP_C2	PEG_TXN_C2	PEG_TXP_C2	AL15				PEX_RX2		VDD_2	N14	0.1U/16V/V		
[7]	PEG_TXP_C3	PEG_TXN_C3	PEG_TXP_C3	AK16				PEX_RX3		VDD_3	N16	0.1U/16V/V		
[7]	PEG_TXP_C4	PEG_TXN_C4	PEG_TXP_C4	AL17				PEX_RX4		VDD_4	N17	0.1U/16V/V		
[7]	PEG_TXP_C5	PEG_TXN_C5	PEG_TXP_C5	AM18				PEX_RX5		VDD_5	N19	0.1U/16V/V		
[7]	PEG_TXP_C6	PEG_TXN_C6	PEG_TXP_C6	AK19				PEX_RX6		VDD_6	N19	10U/6.3V/R		
[7]	PEG_TXP_C7	PEG_TXN_C7	PEG_TXP_C7	AL20				PEX_RX7		VDD_7	P14	0.1U/16V/V		
[7]	PEG_TXP_C8	PEG_TXN_C8	PEG_TXP_C8	AM21				PEX_RX8		VDD_8	P16	1U/6.3V/R		
[7]	PEG_TXP_C9	PEG_TXN_C9	PEG_TXP_C9	AK22				PEX_RX9		VDD_9	P17	0.1U/16V/V		
[7]	PEG_TXP_C10	PEG_TXN_C10	PEG_TXP_C10	AL23				PEX_RX10		VDD_10	P17	0.1U/16V/V		
[7]	PEG_TXP_C11	PEG_TXN_C11	PEG_TXP_C11	AM24				PEX_RX11		VDD_11	P19	0.1U/16V/V		
[7]	PEG_TXP_C12	PEG_TXN_C12	PEG_TXP_C12	AK25				PEX_RX12		VDD_12	R16	C283	0.1U/16V/V	
[7]	PEG_TXP_C13	PEG_TXN_C13	PEG_TXP_C13	AL26				PEX_RX13		VDD_13	R17	C330	0.1U/16V/V	
[7]	PEG_TXP_C14	PEG_TXN_C14	PEG_TXP_C14	AM27				PEX_RX14		VDD_14	T18	C335	0.47U/10V/X	
[7]	PEG_TXP_C15	PEG_TXN_C15	PEG_TXP_C15	AL28				PEX_RX15		VDD_15	T19	C249	0.47U/10V/X	
[7]	CLK_PCIE_VGA	CLK_PCIE_VGA#	CLK_PCIE_VGA	AH14				PEX_REFCLK		VDD_16	U13	C268	0.47U/10V/X	



**PROJECT : AT1**  
Quanta Computer Inc.

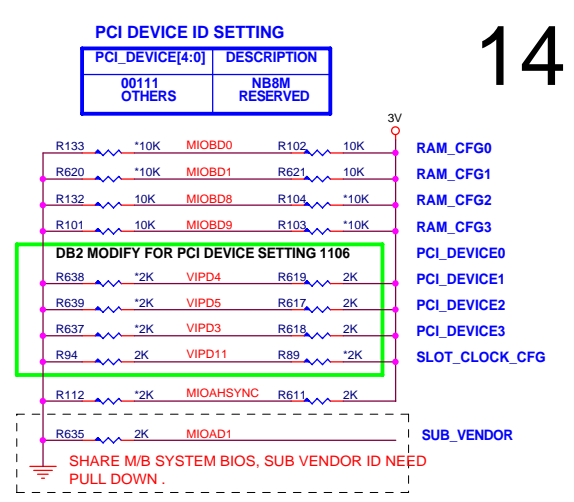
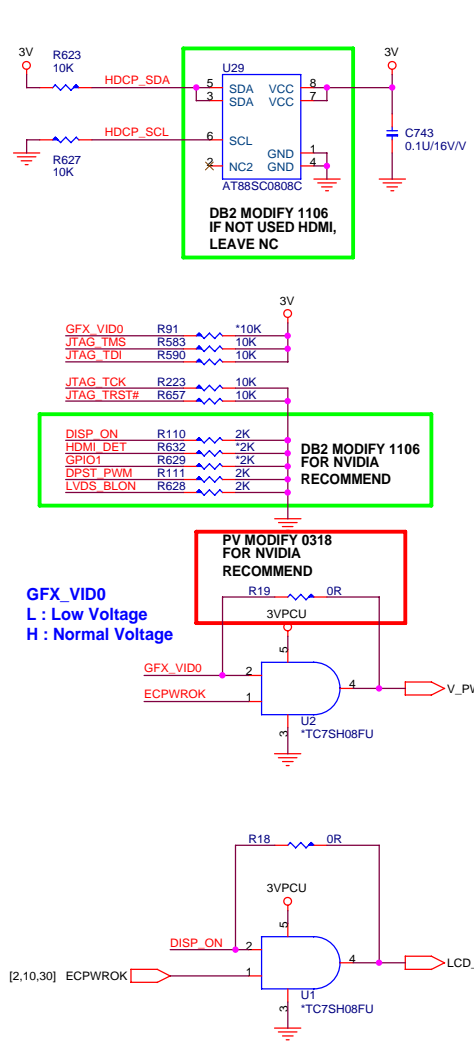
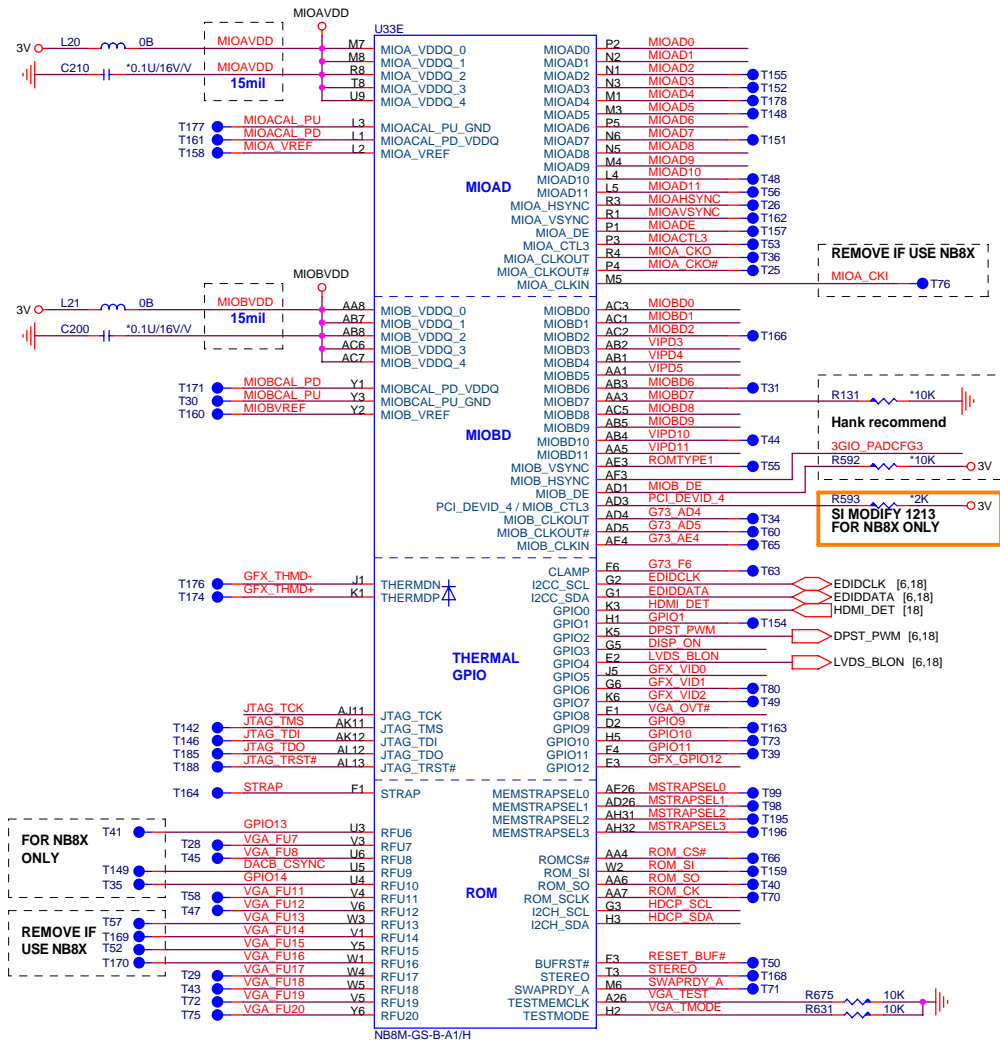
Size Custom Document Number NV\_NB8M (PCIE\_I/F,GND) Rev MV  
Date: Tuesday, August 21, 2007 Sheet 12 of 40



- 1.2V [10,11,12,15,36]
- 1.8V [11,15,16,17,32,37]
- 2.5V [2,32,36]
- 3V [2,5,6,7,8,9,10,11,12,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
- 5V [18,19,22,23,25,26,27,28,29,31,32,33,36,38]

**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number NV_NB8M (LVDS,CRT,TV,HDMI)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 13	of 40

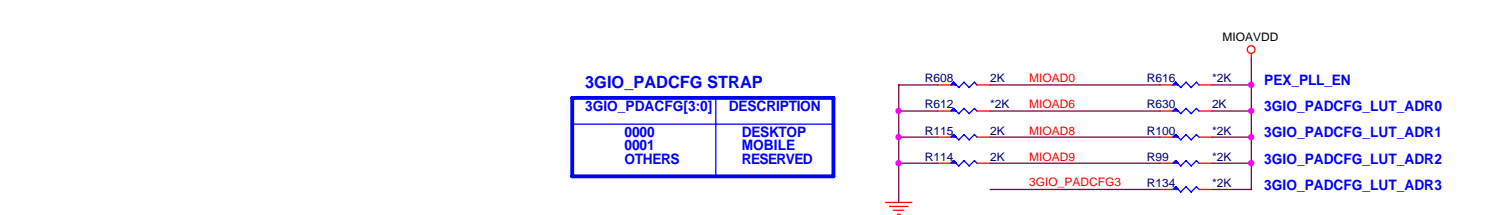
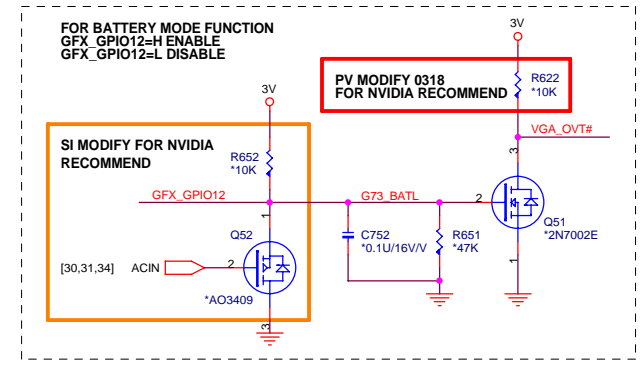


**NB8X 64bit VRAM Configuration Table**

RAM_CFG3[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infinion
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Hynix
0111	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infinion
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

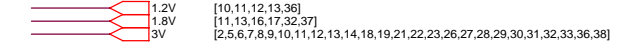
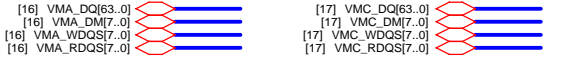
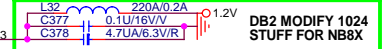
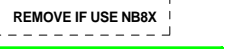
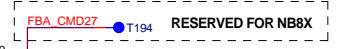
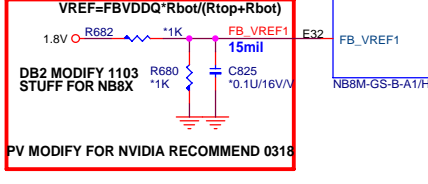
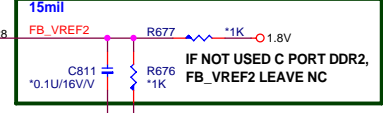
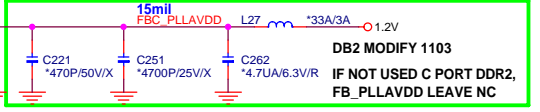
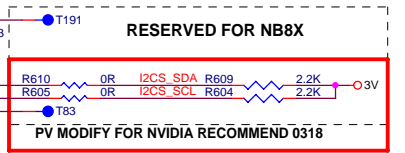
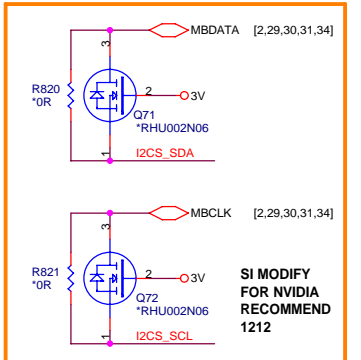
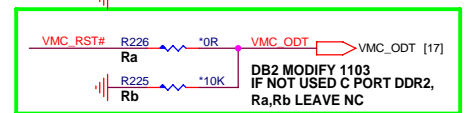
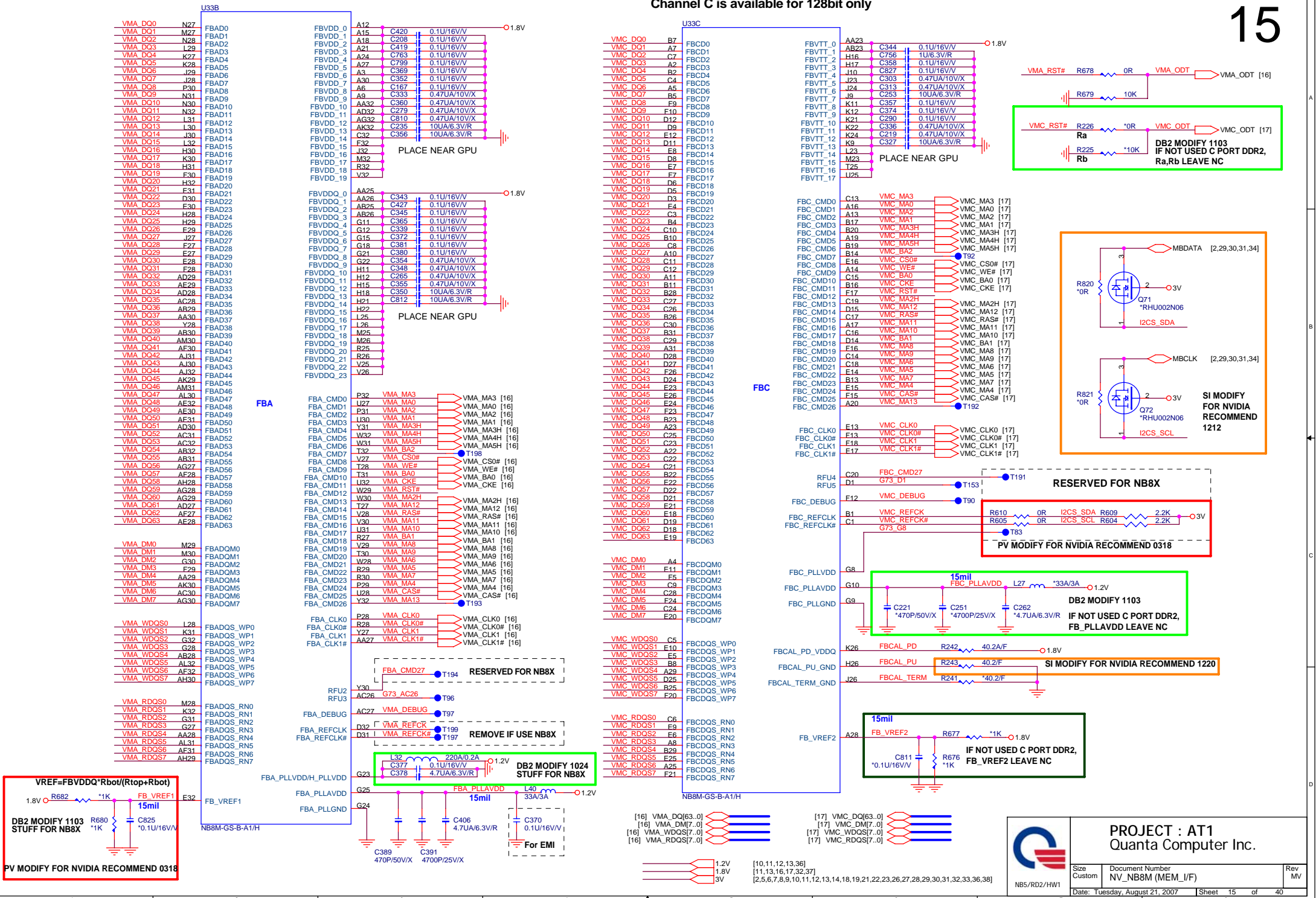
**NB8X 128bit VRAM Configuration Table**

RAM_CFG3[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infinion
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Hynix
0111	DDR2 32Mx16x8, 128bit, 512MB	Samsung
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infinion
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infinion
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



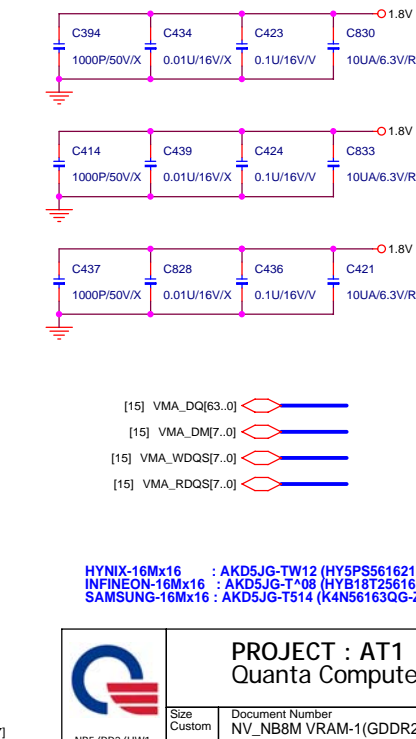
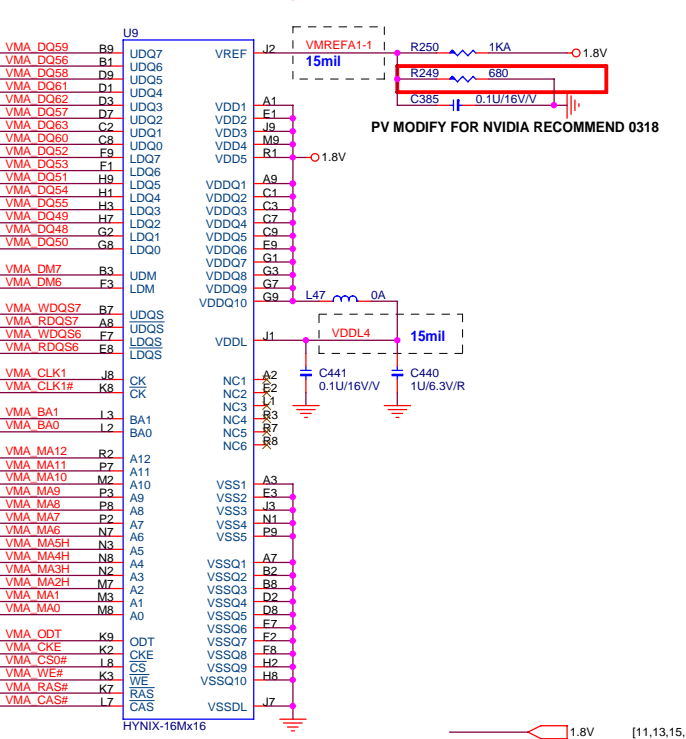
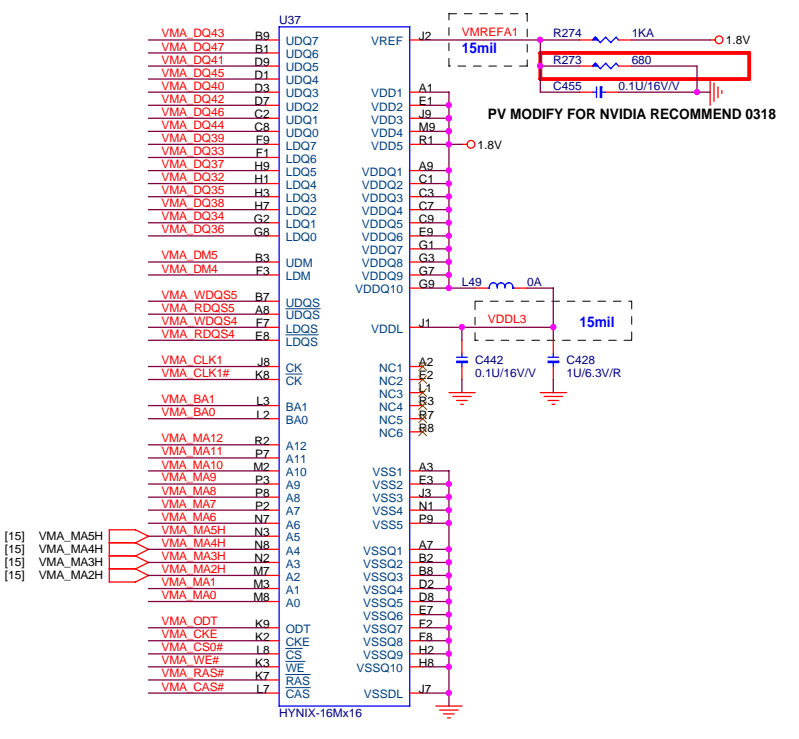
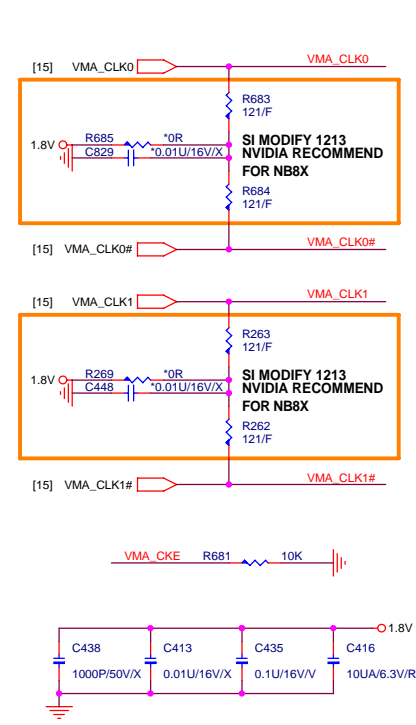
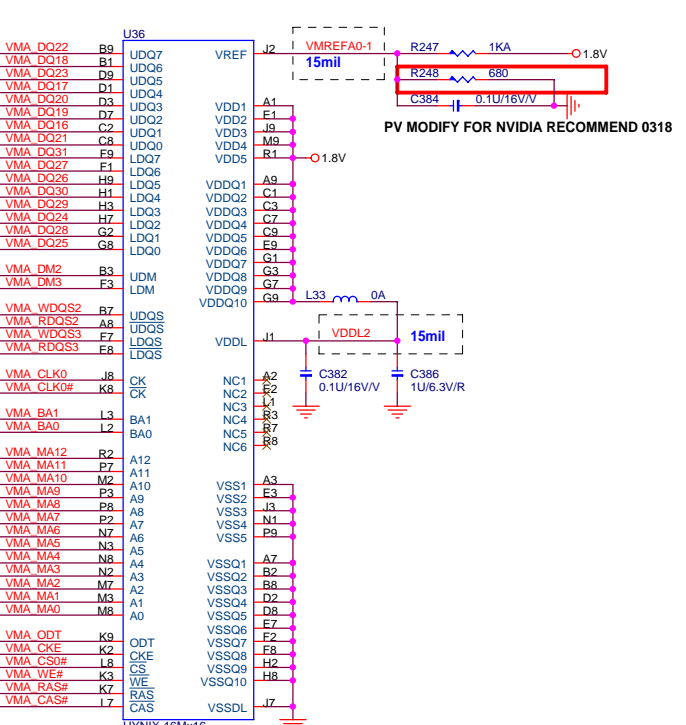
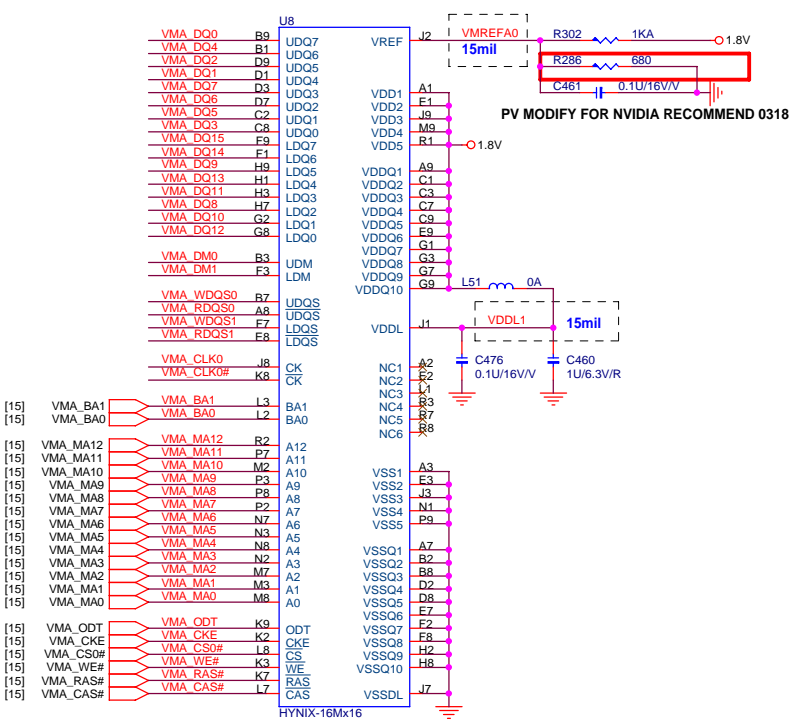
3V [2,5,6,7,8,9,10,11,12,13,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]  
3VPCU [9,18,28,29,30,31,33,34,35]

Channel C is available for 128bit only



**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom Document Number NV\_NB8M (MEM\_I/F) Rev MV  
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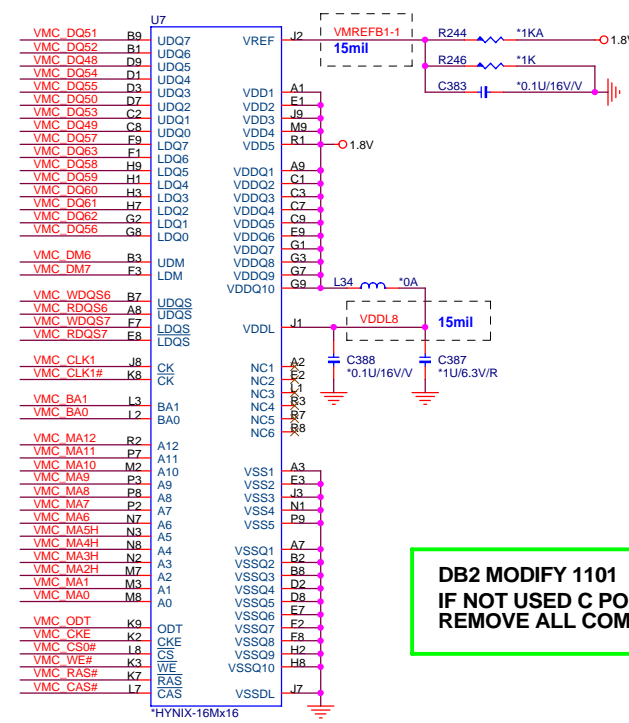
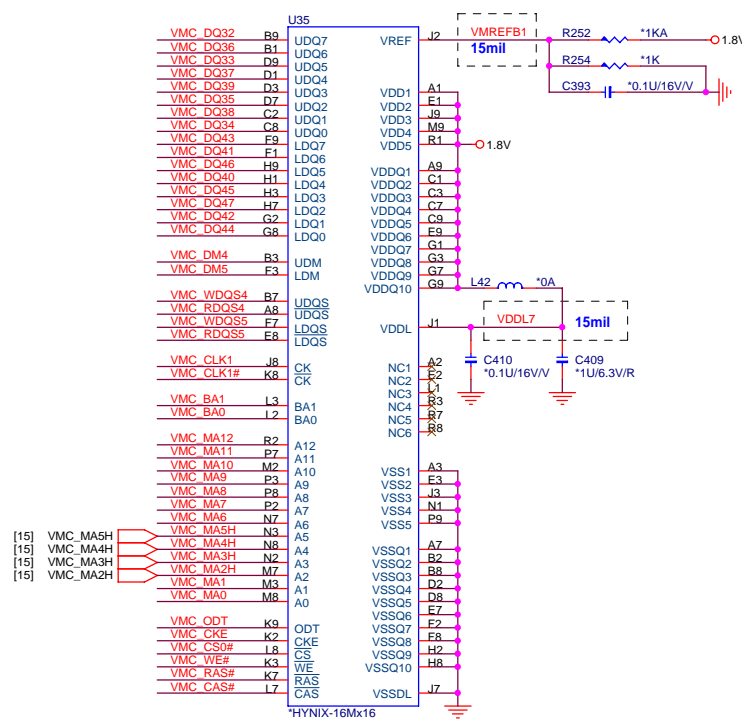
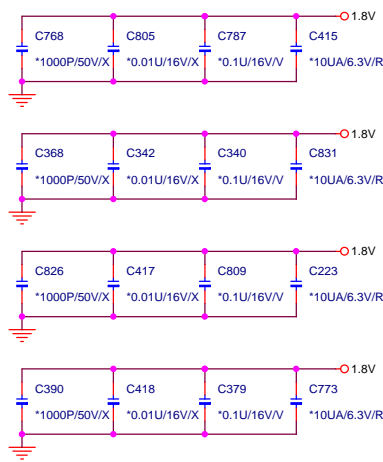
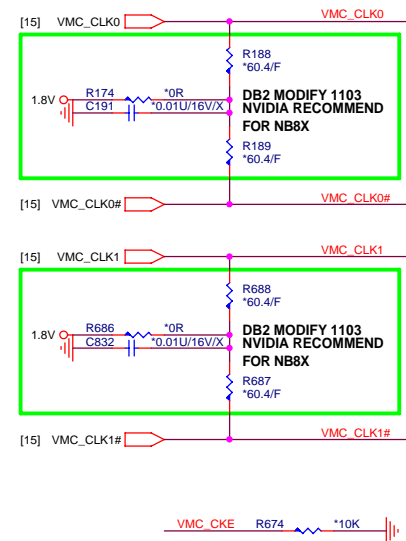
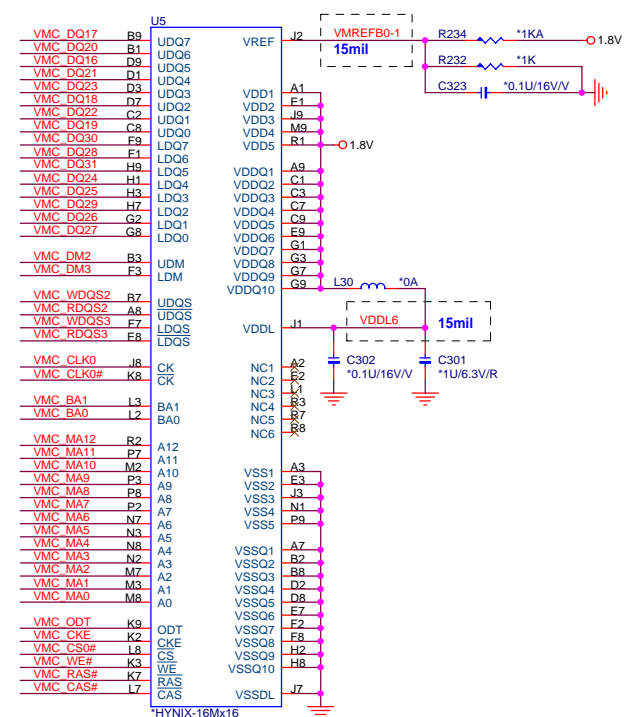
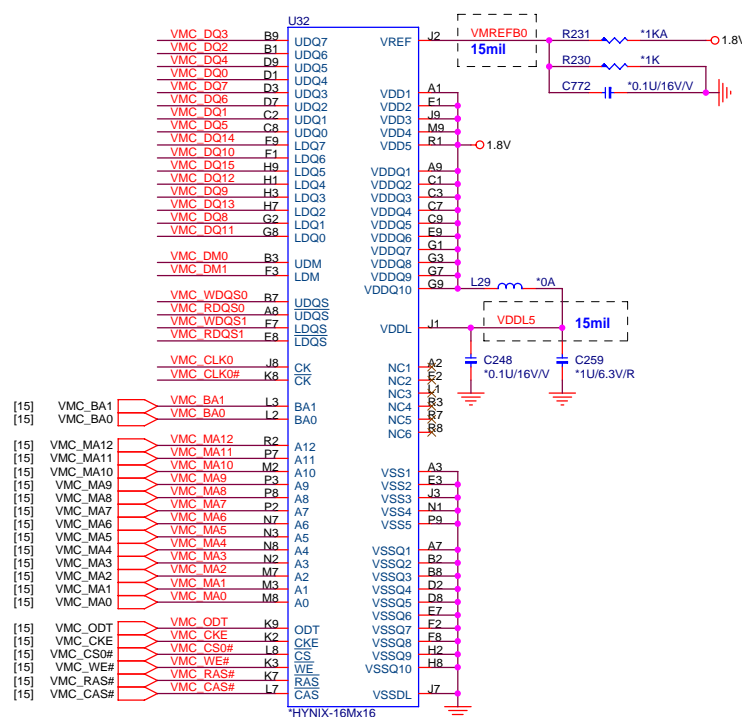


HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25\_1.8V)  
 INFINEON-16Mx16 : AKD5JG-T\*08 (HYB18T256161AFL25)  
 SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25\_1.8V)

**PROJECT : AT1**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev MV
	NV_NB8M VRAM-1(GDDR2 BGA84)	
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- [15] VMC\_DQ[63..0]
- [15] VMC\_DM[7..0]
- [15] VMC\_WDQS[7..0]
- [15] VMC\_RDQS[7..0]

**DB2 MODIFY 1101  
IF NOT USED C PORT DDR2,  
REMOVE ALL COMPONENTS**

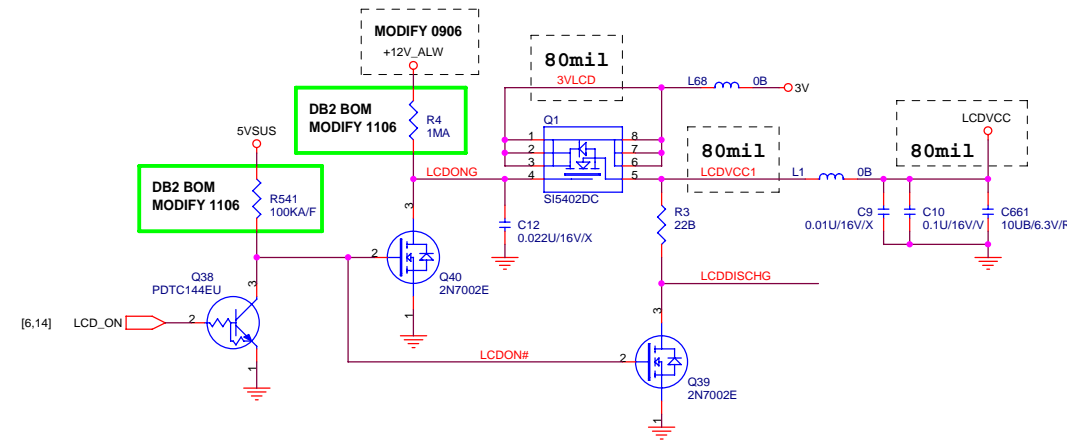
HYNIX-16Mx16 : AKD5JG-TW12 (HYSP561621AFP-25\_1.8V)  
INFINEON-16Mx16 : AKD5JG-T\*08 (HYB18T256161AFL25)  
SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25\_1.8V)



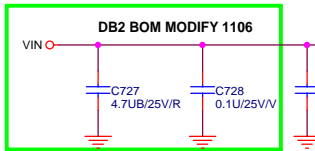
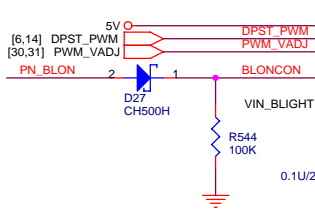
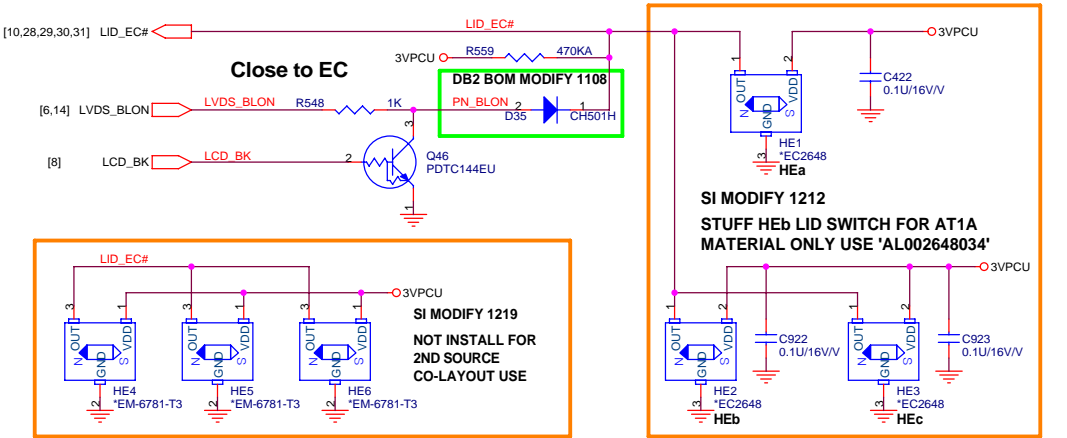
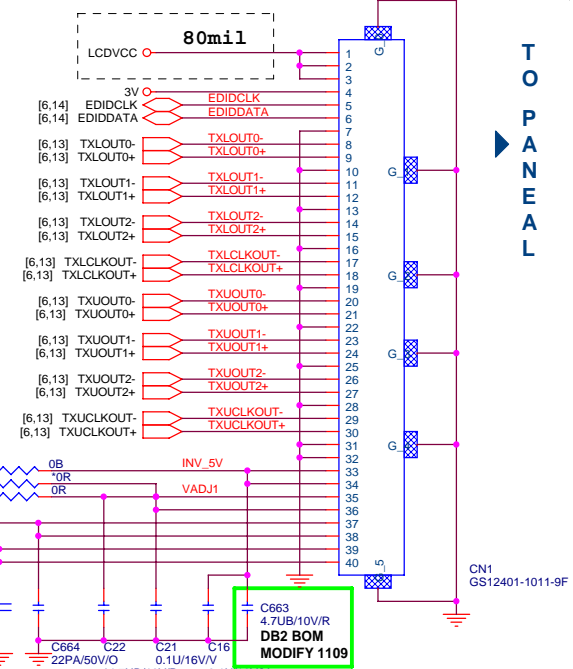
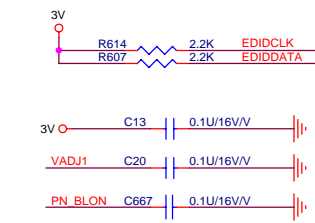
**PROJECT : AT1  
Quanta Computer Inc.**

Size Custom	Document Number NV_NB8M VRAM-2(GDDR2 BGA84)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 17 of 40	

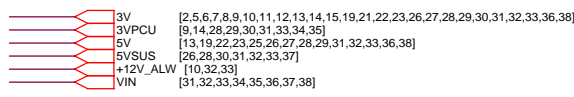
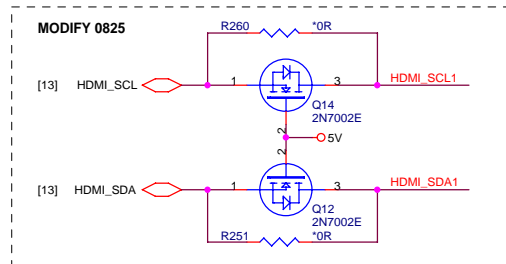
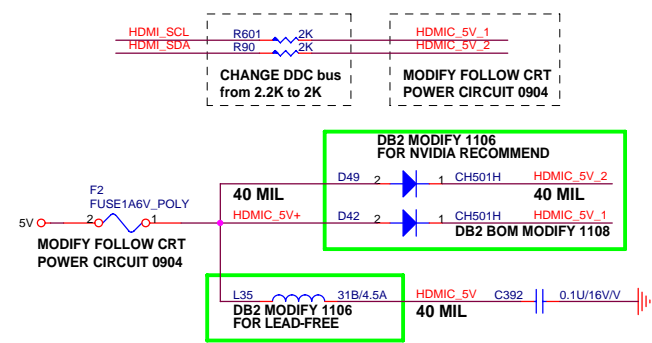
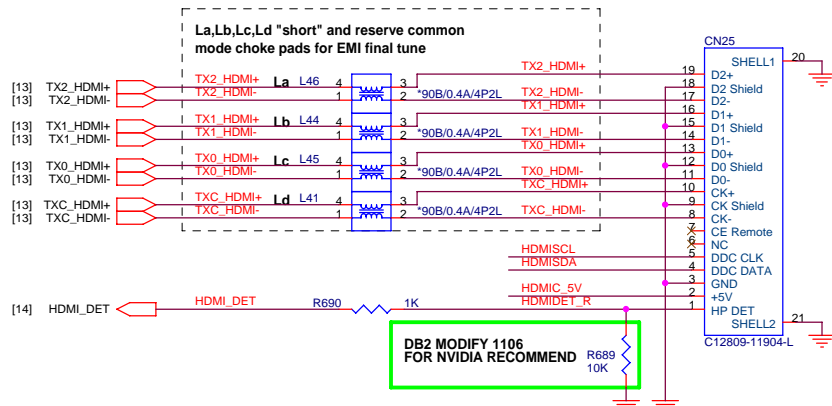
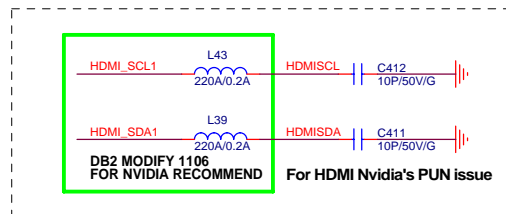
1.8V [11,13,15,16,32,37]



### LCD CONNECTOR



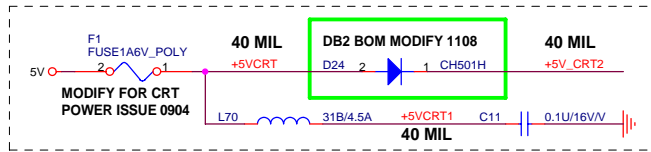
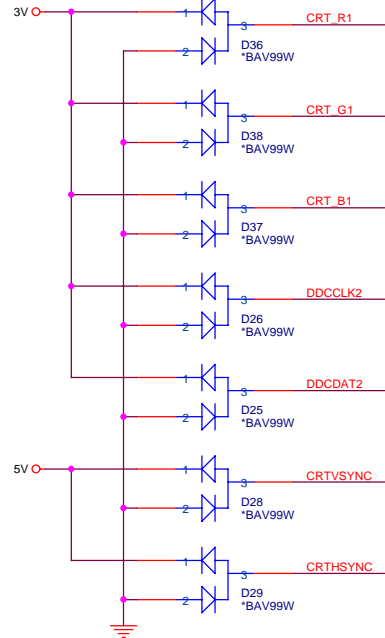
### HDMI PORT



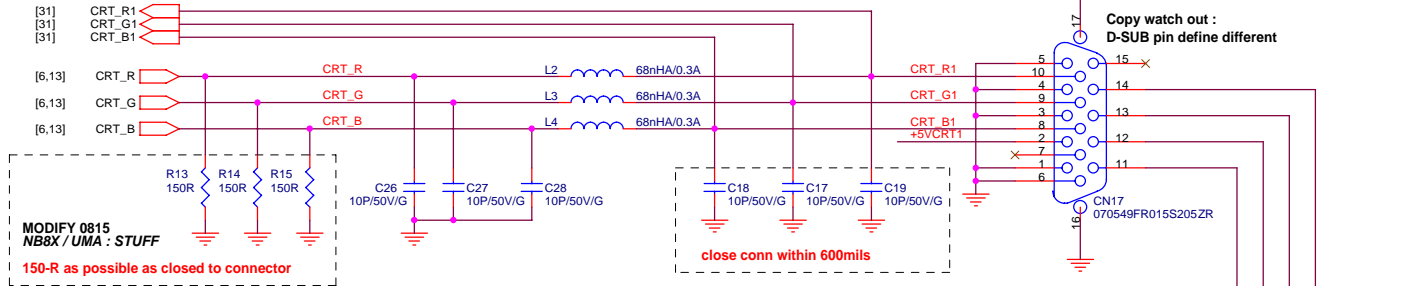
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number LCD,HDMI,LID_SW	Rev MV
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NBS/RD2/HW1

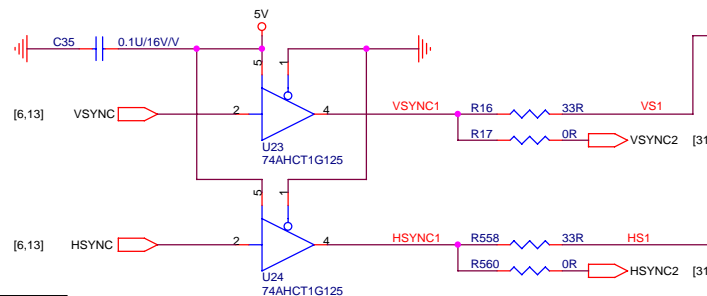


**CRT PORT**

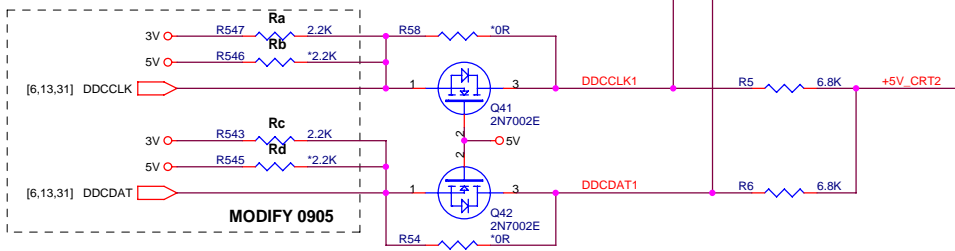


**MODIFY 0815**  
NB8X / UMA : STUFF  
150-R as possible as closed to connector

close conn within 600mils

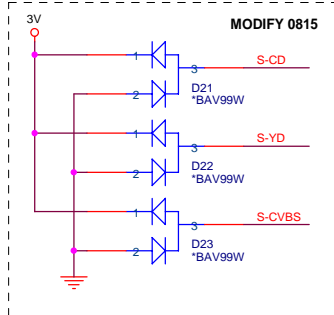


NB8X & MCP67M DIFFERENCE		
LOCATION	NB8X (DISCRETE)	MCP67M (UMA)
Ra	2.2K	NC
Rb	NC	2.2K
Rc	2.2K	NC
Rd	NC	2.2K

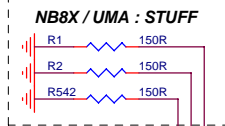


**MODIFY 0905**

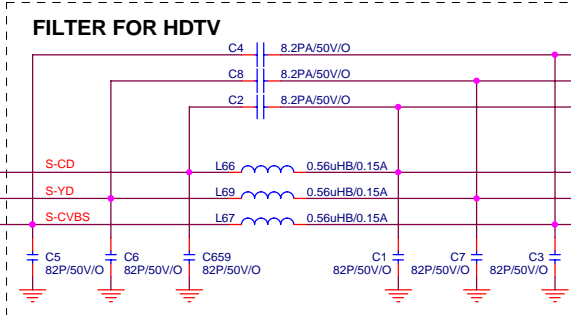
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,21,22,23,26,27,28,29,30,31,32,33,36,38]  
5V [13,18,22,23,25,26,27,28,29,31,32,33,36,38]



**MODIFY 0815**

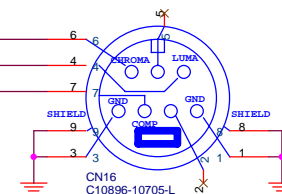
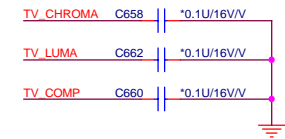


[6,13] S-CD  
[6,13] S-YD  
[6,13] S-CVBS



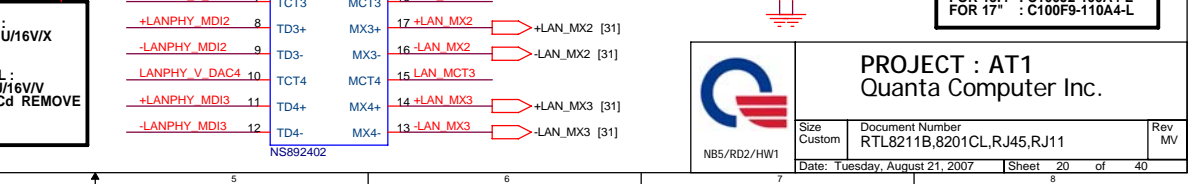
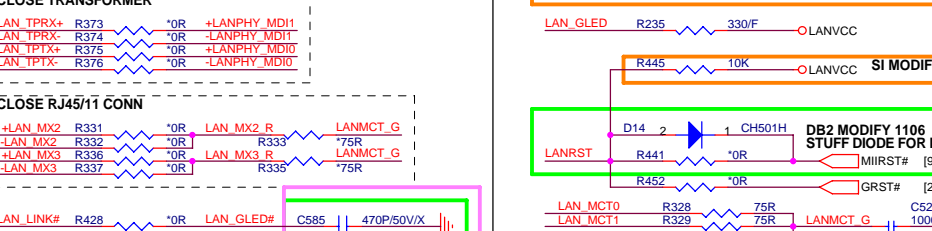
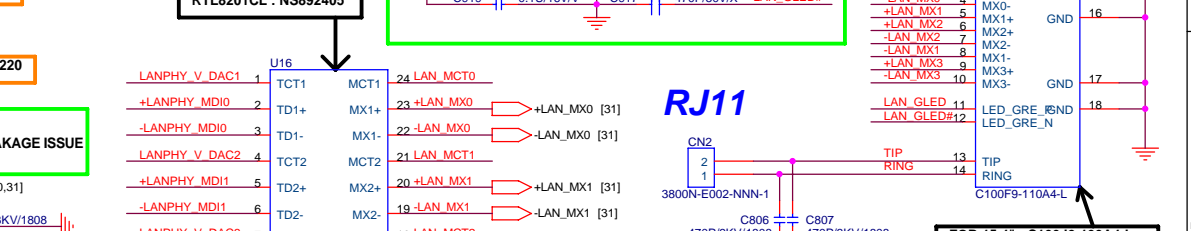
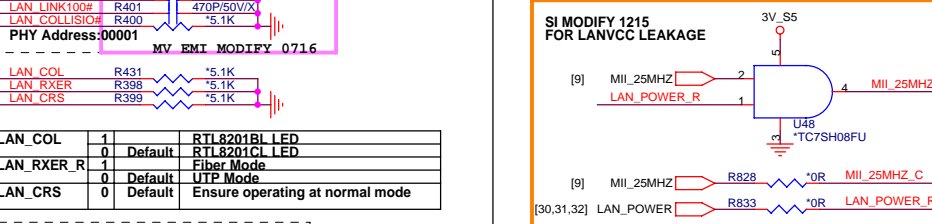
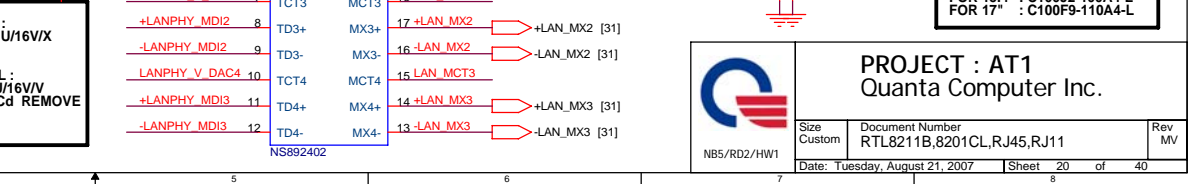
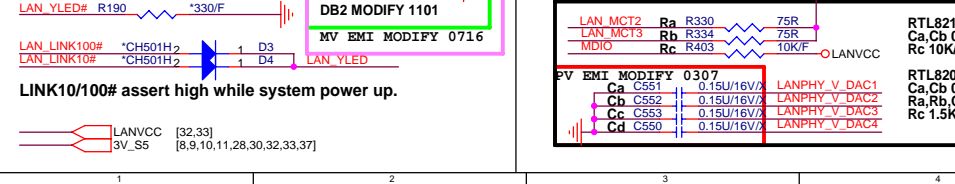
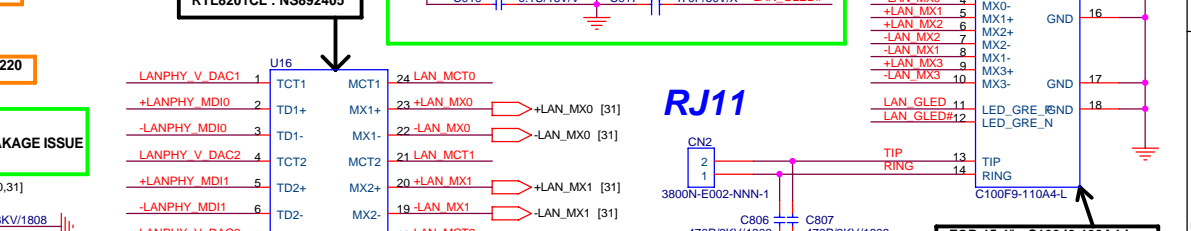
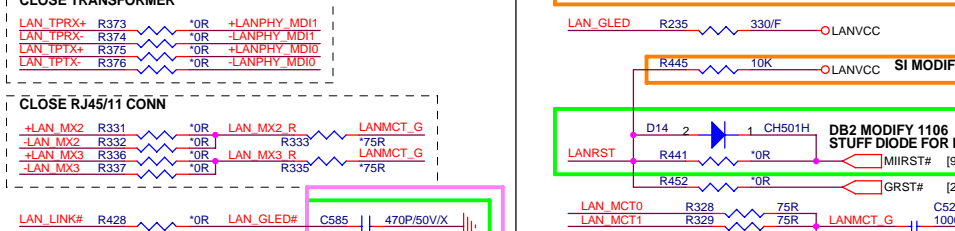
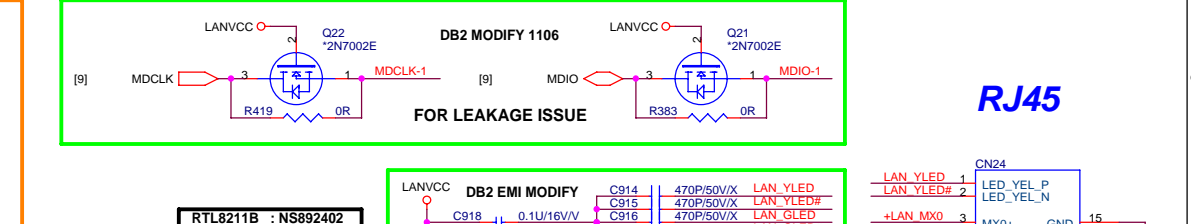
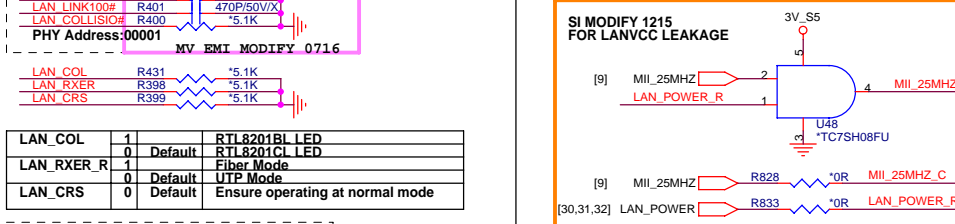
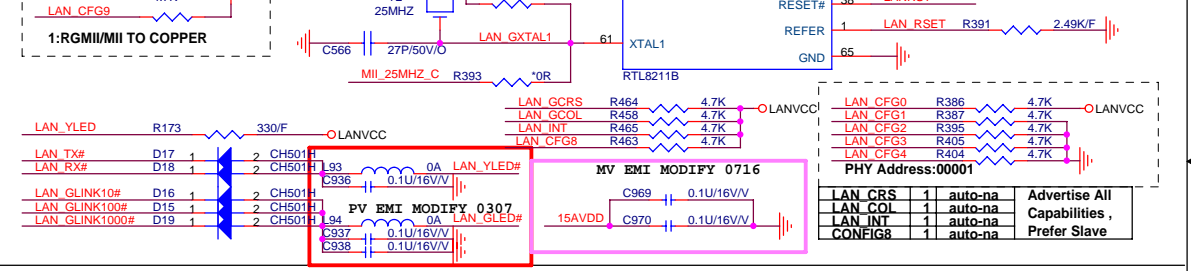
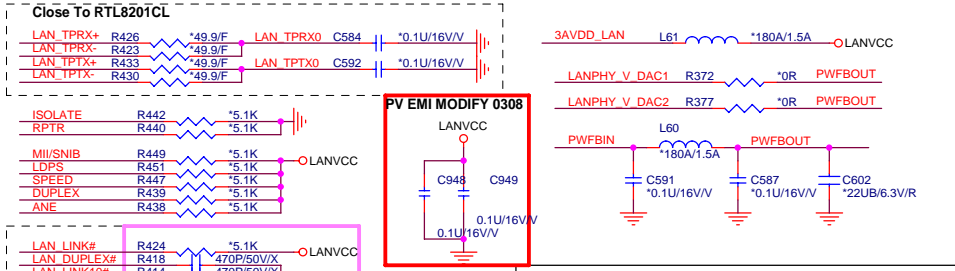
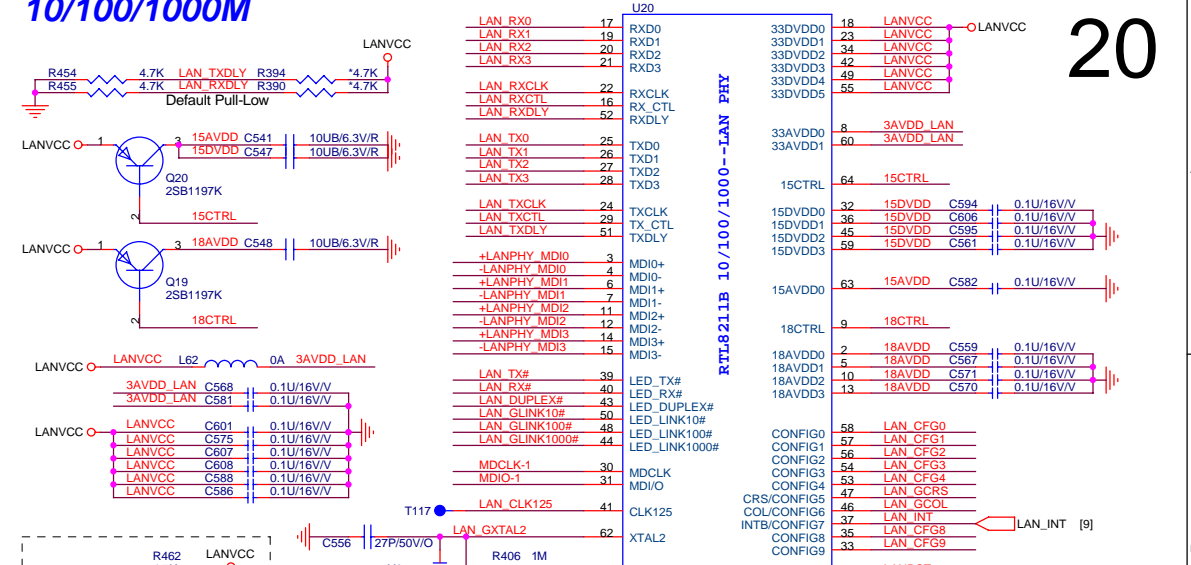
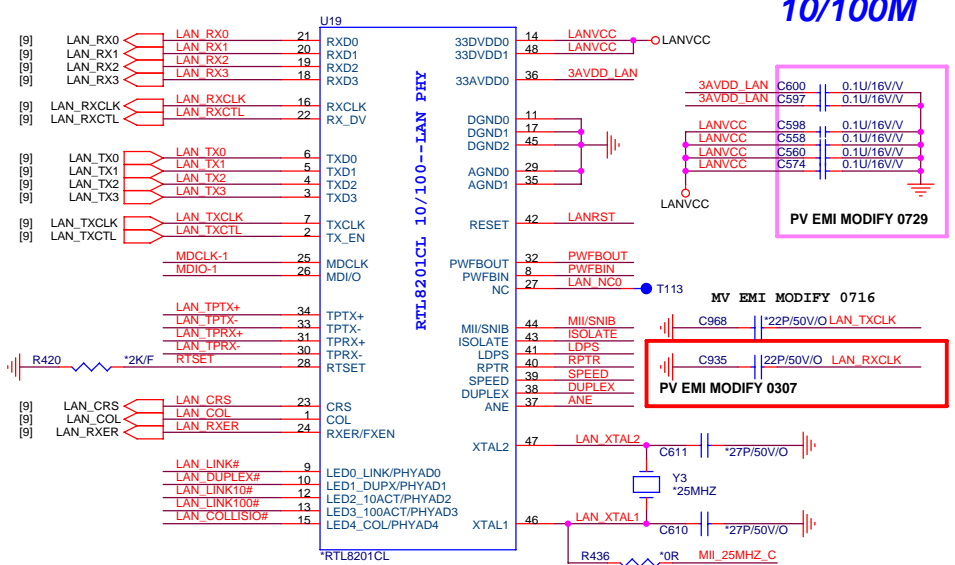
**FILTER FOR HDTV**

**TV\_OUT**



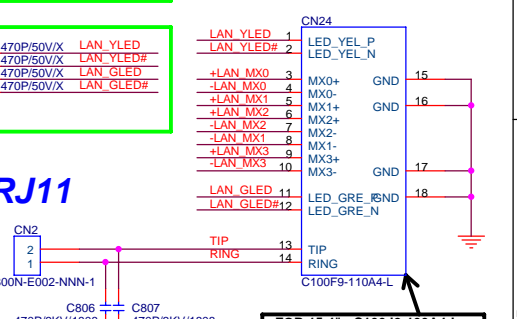
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number CRT_TV_OUT	Rev MV
Date: Tuesday, August 21, 2007		Sheet 19 of 40



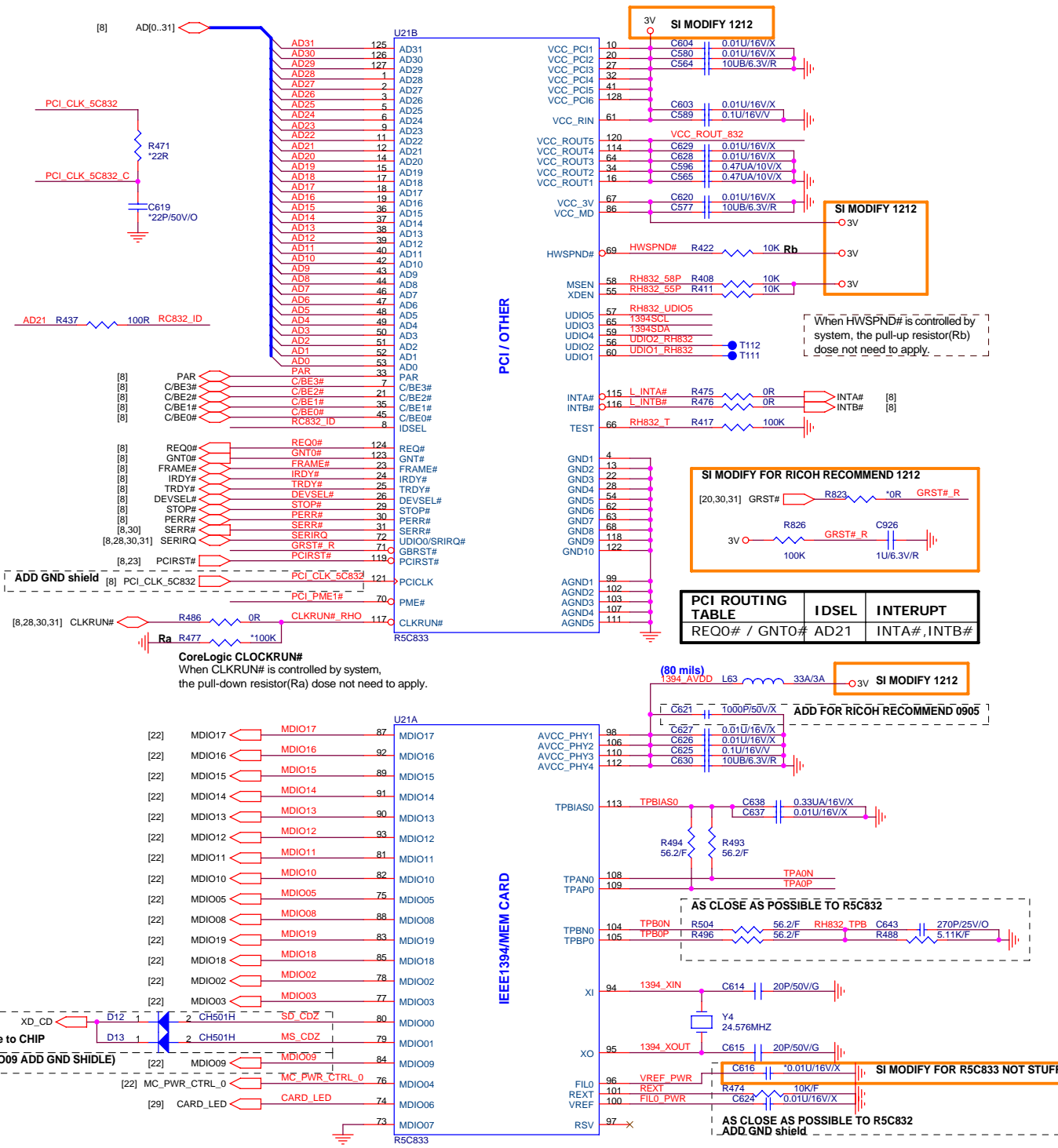
LAN CRS	1	auto-na	Advertise All Capabilities, Prefer Slave
LAN COL	1	auto-na	
LAN INT	1	auto-na	
LAN CFG8	1	auto-na	

PHY Address:0001

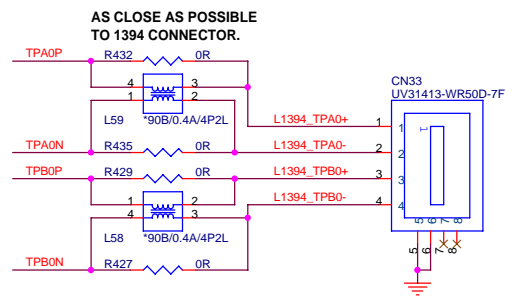
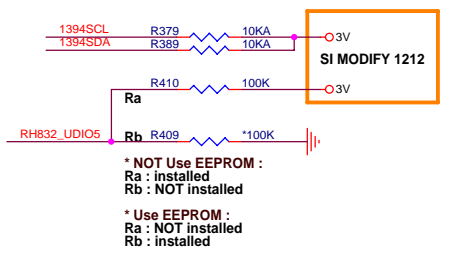


**RJ11**

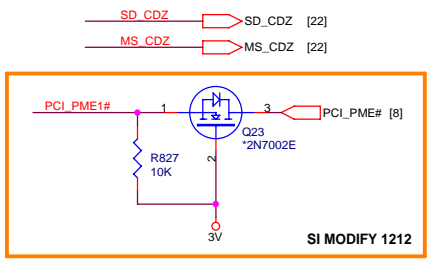
**FOR 15.4" : C100J2-100A4-L**  
**FOR 17" : C100F9-110A4-L**



Serial EEPROM



\*TPA/TPA#,TPB/TPB# pair trace : As close as possible.  
\*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layout with shields.  
\*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

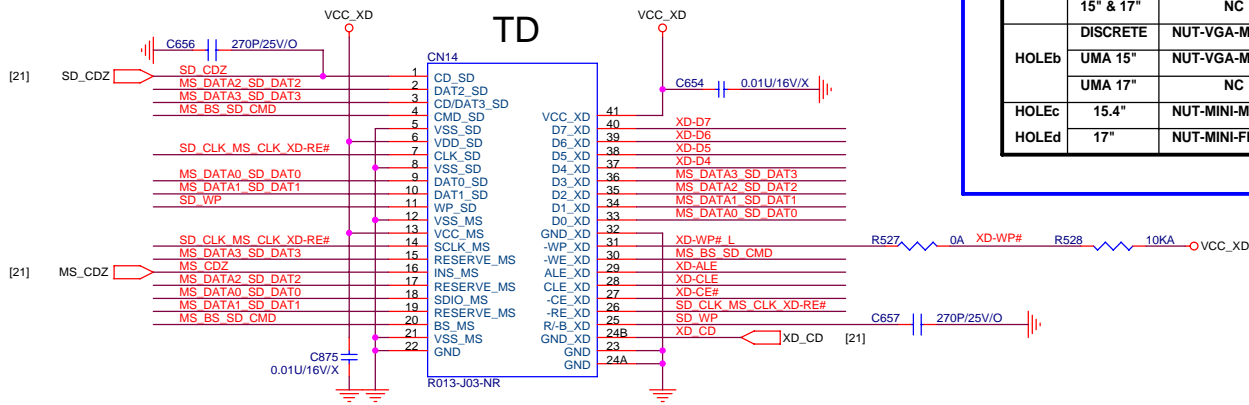


**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number R5C832V00, 1394 PORT	Rev MV
Date: Tuesday, August 21, 2007	Sheet 21 of 40	

NBS/RD2/HW1

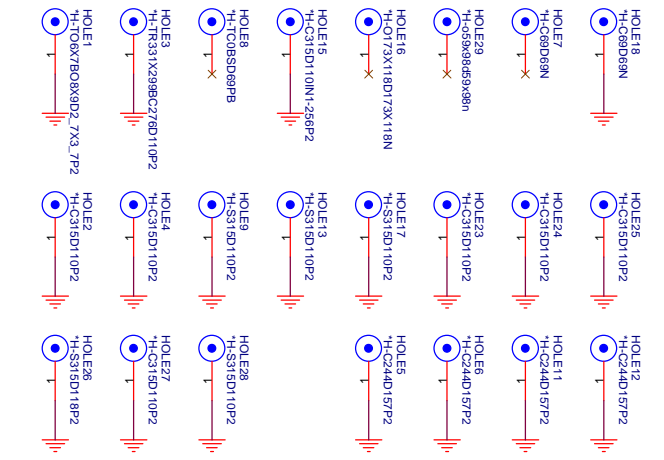
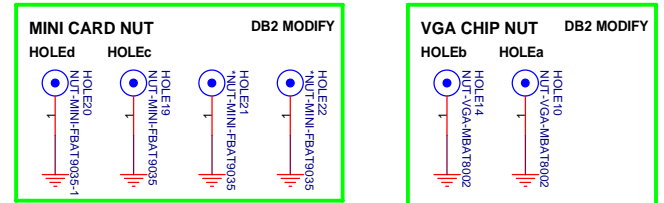
### 4 IN1 CARD READER XD,MMC/SD,MS/MP



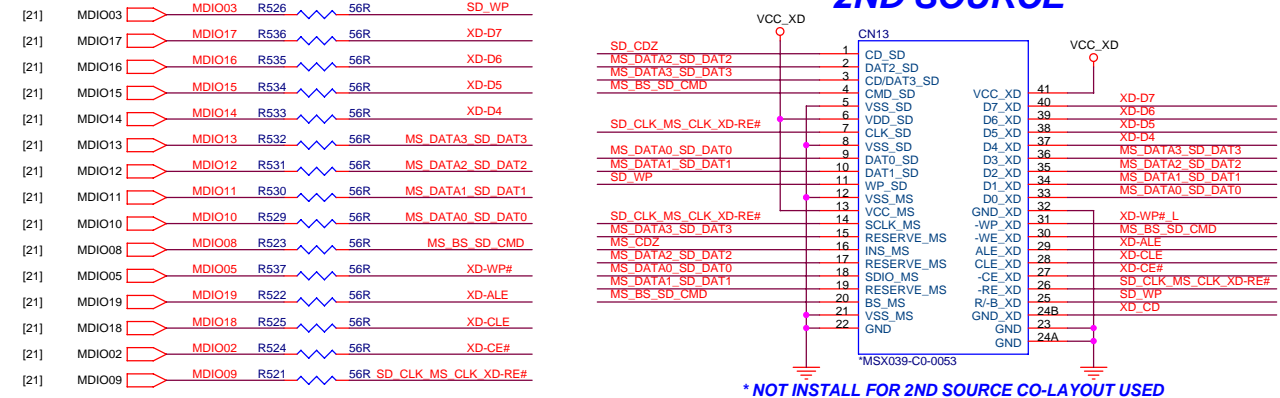
Note: Need to add WP# and CD# pad for Proconn

15.4" & 17" AND DISCRETE & UMA		
HOLE	STATUS	NUT
HOLEa	DISCRETE	NUT-VGA-MBAT8002
	15" & 17"	NC
	DISCRETE	NUT-VGA-MBAT8002
HOLEb	UMA 15"	NUT-VGA-MBAT8002
	UMA 17"	NC
HOLEc	15.4"	NUT-MINI-MBAT8004
HOLEd	17"	NUT-MINI-FBAT9035

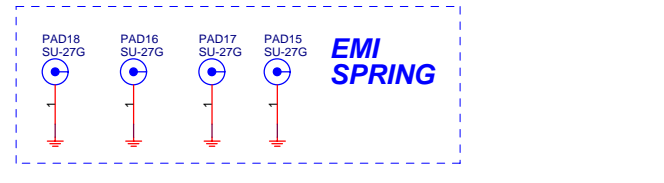
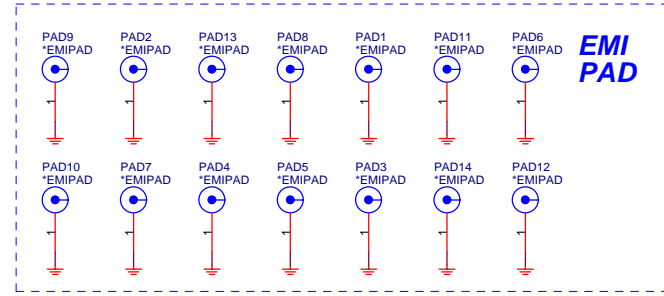
### SCREW HOLE



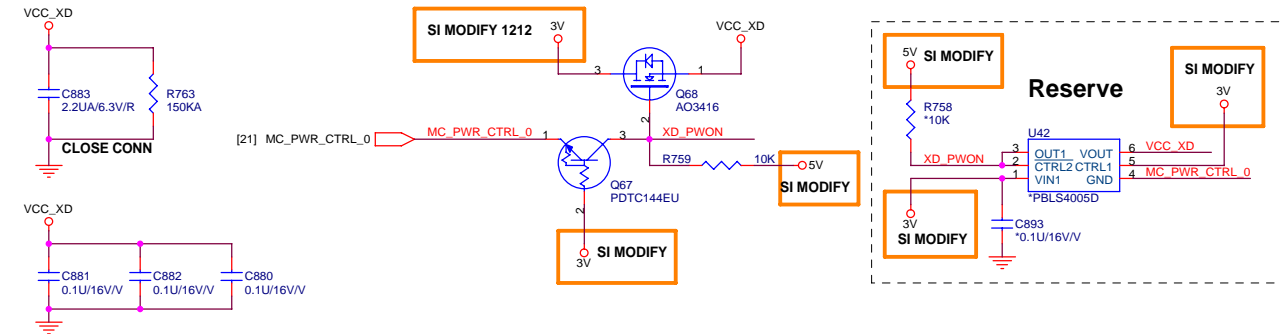
### 2ND SOURCE



\* NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED



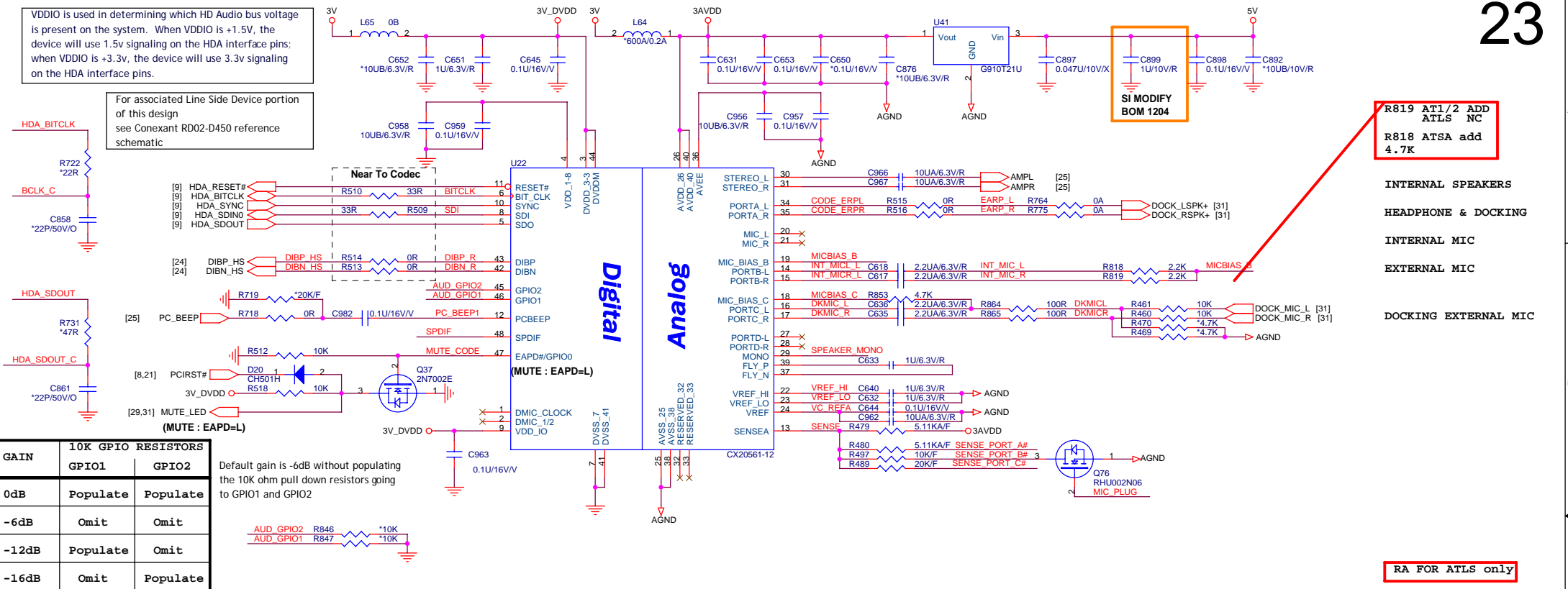
[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,23,26,27,28,29,30,31,32,33,36,38]  
[13,18,19,23,25,26,27,28,29,31,32,33,36,38]



	<b>PROJECT : AT1</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number CARD_READER,HOLE,NUT,SPRING
Date: Tuesday, August 21, 2007		Sheet 22 of 40

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic



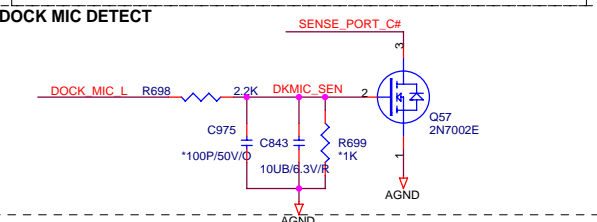
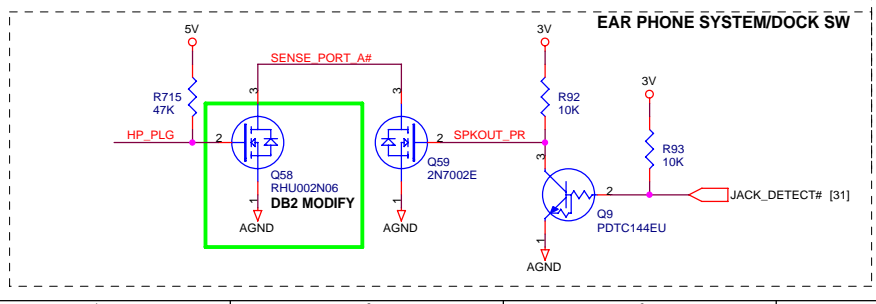
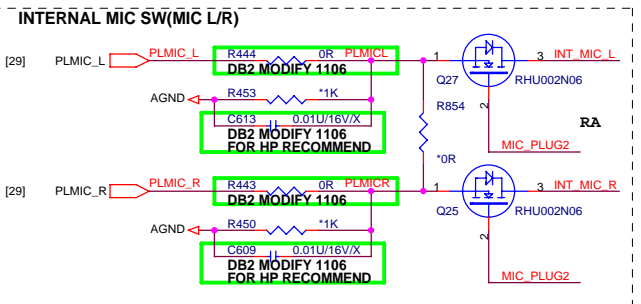
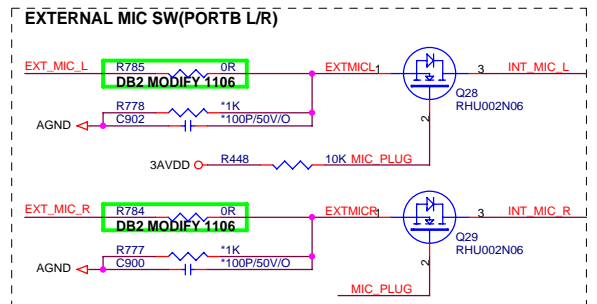
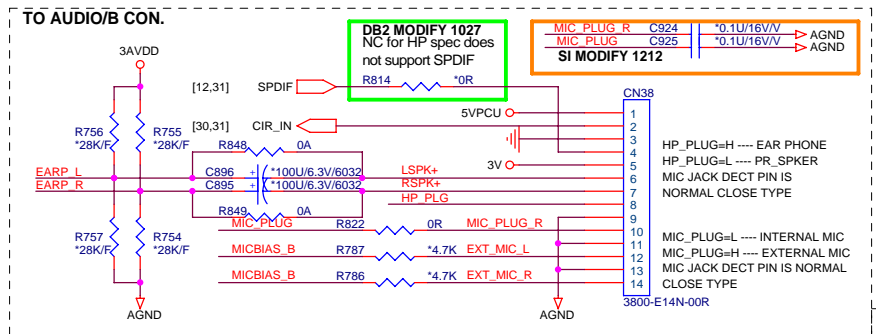
R819 AT1/2 ADD ATLS NC  
R818 ATSA add 4.7K

- INTERNAL SPEAKERS
- HEADPHONE & DOCKING
- INTERNAL MIC
- EXTERNAL MIC
- DOCKING EXTERNAL MIC

GAIN	10K GPIO RESISTORS	
	GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

RA FOR ATLS only



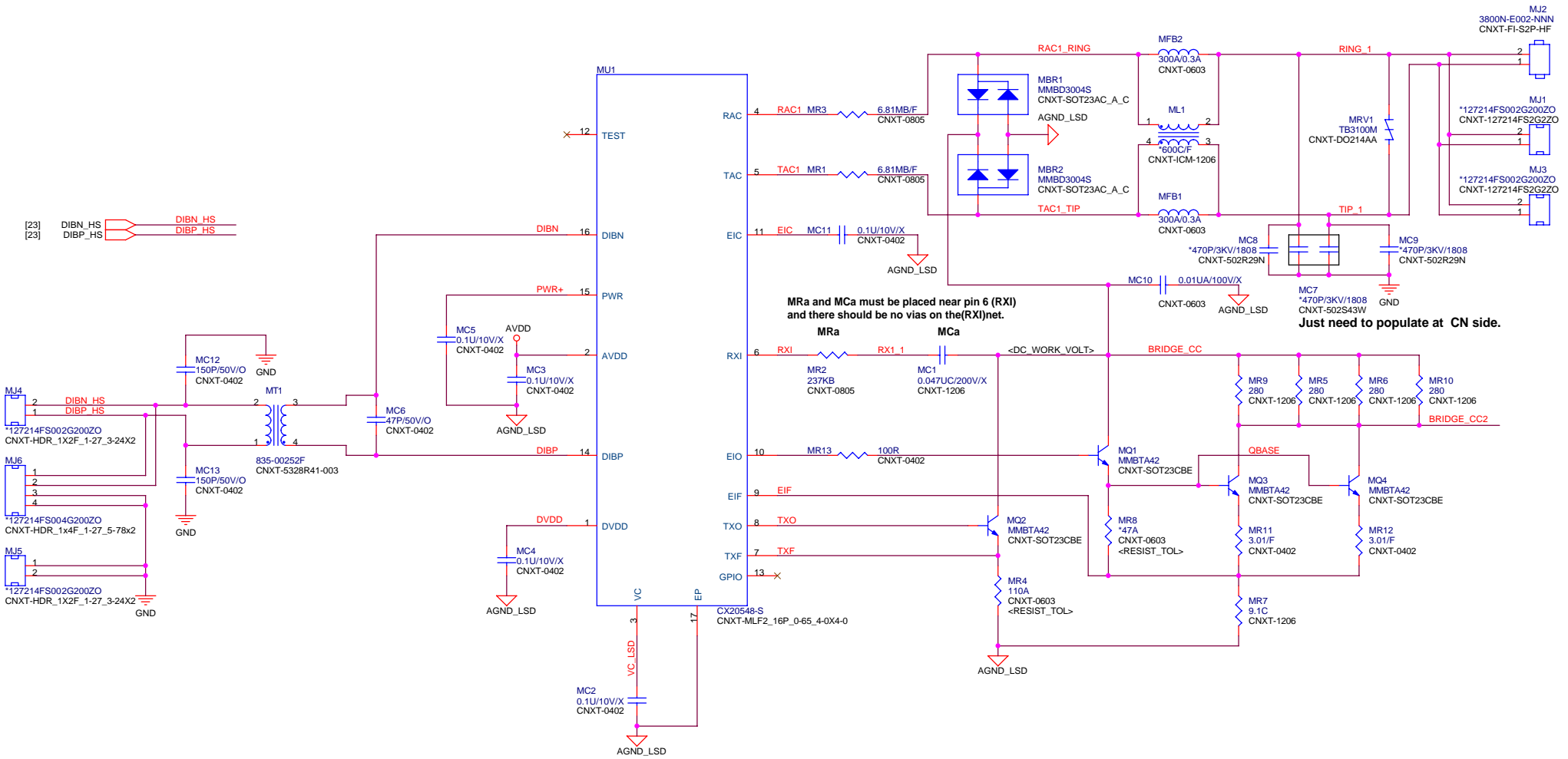
- 3AVDD [25]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,26,27,28,29,30,31,32,33,36,38]
- 5V [13,18,19,22,25,26,27,28,29,31,32,33,36,38]
- 5VPCU [10,33,34,35,36,37,38]

**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number HDA_CX20561-12,AUDIO_BOARD	Rev MV
Date: Tuesday, August 21, 2007	Sheet 23	of 40

NBS/RD2/HW1

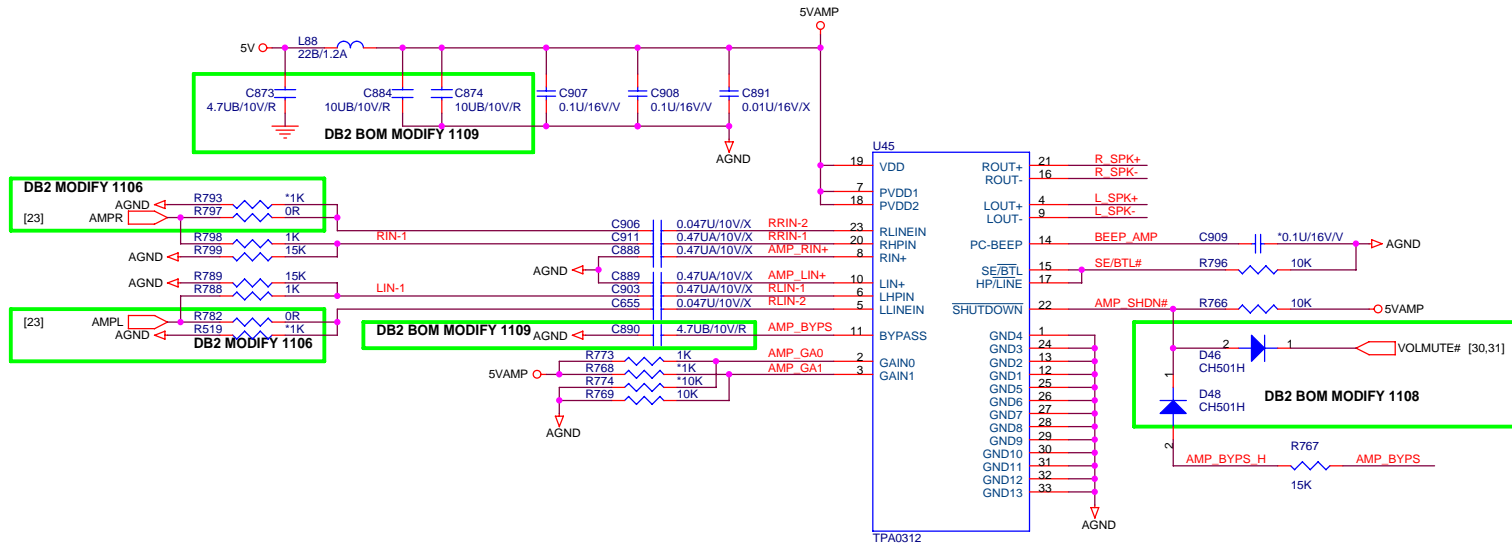
Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		



<p>NBS/RD2/HW1</p>	<p><b>PROJECT : AT1</b> Quanta Computer Inc.</p>	
	<p>Size Custom</p>	<p>Document Number MODEM(DAA)_CX20548-S</p>
<p>Date: Tuesday, August 21, 2007</p>		<p>Sheet 24 of 40</p>

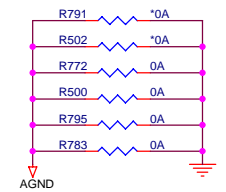


AUDIO AMPLIFIER

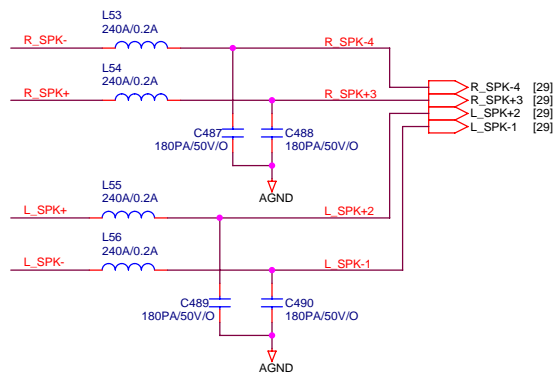


0312 Gain Table

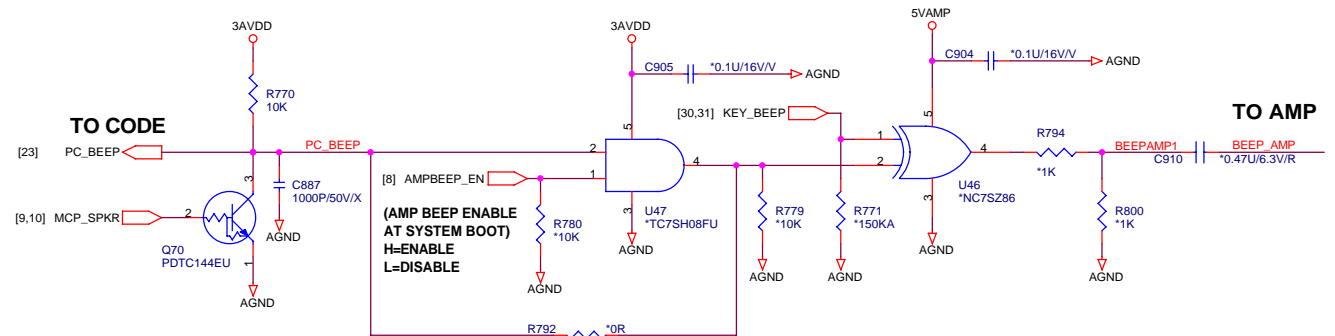
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER



PCSPK BEEP

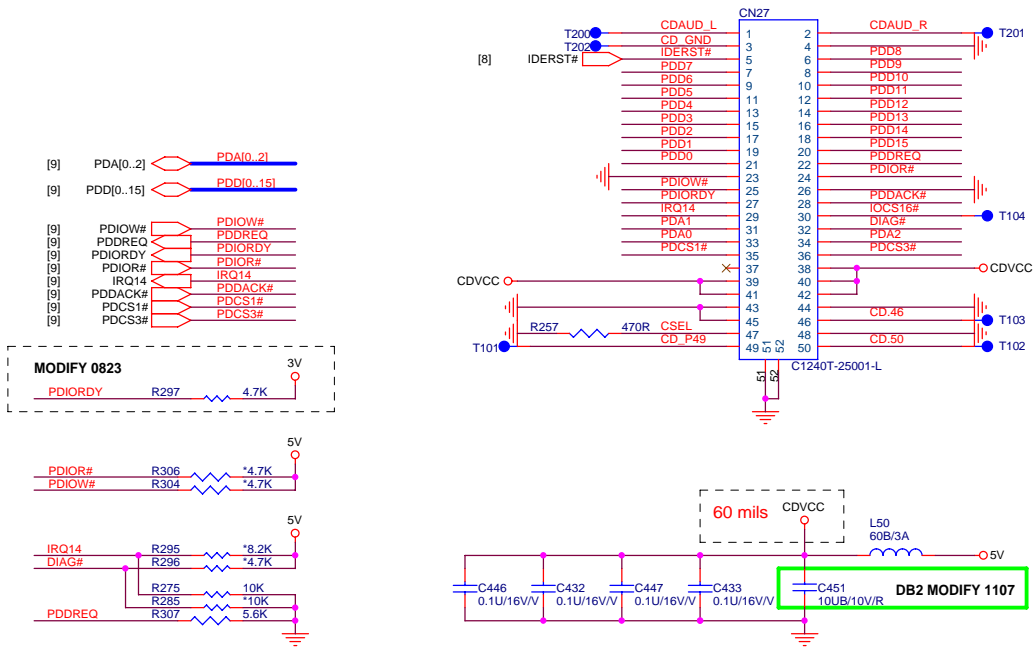


3AVDD [23] (13,18,19,22,23,26,27,28,29,31,32,33,36,38)  
5V

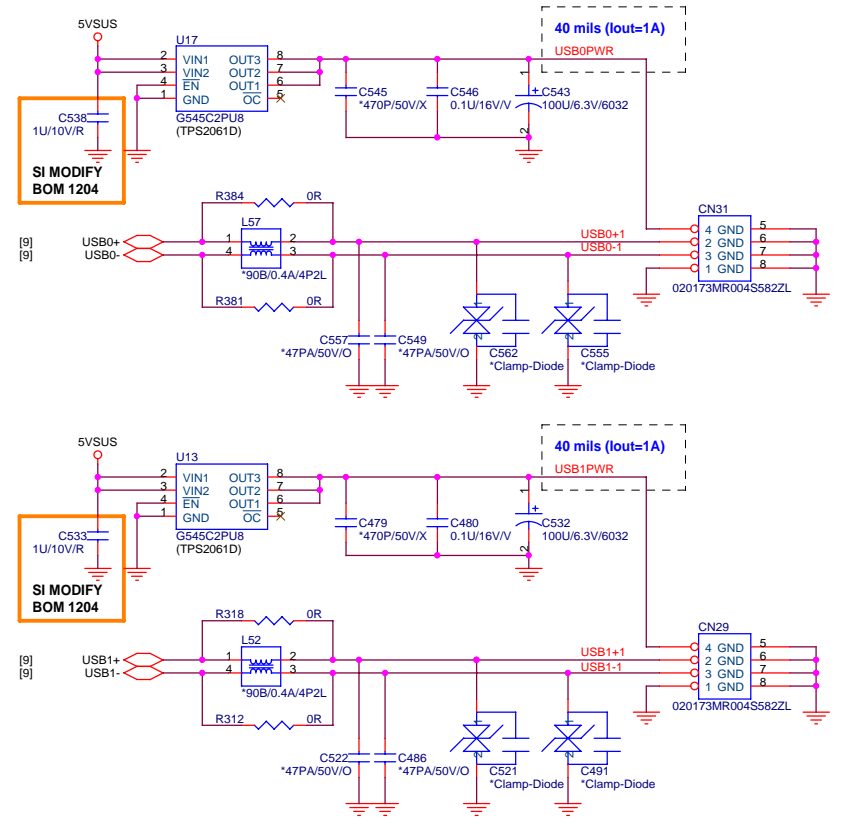
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA0312	Rev MV
Date: Tuesday, August 21, 2007		Sheet 25 of 40

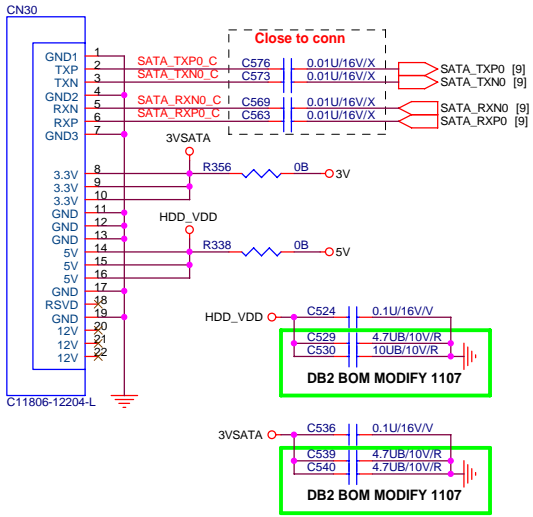
### CD-ROM



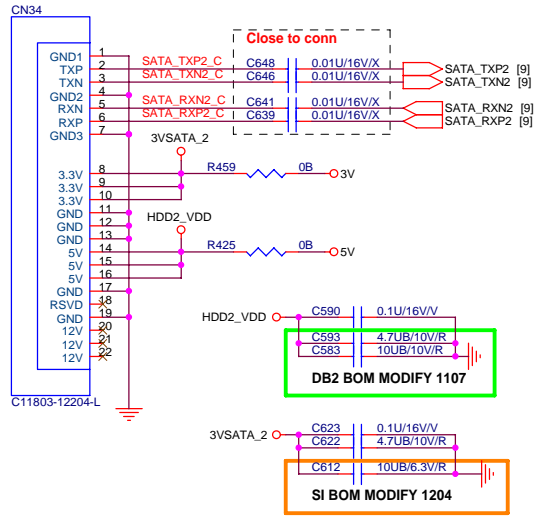
### USB DIP CONNECTOR X 2



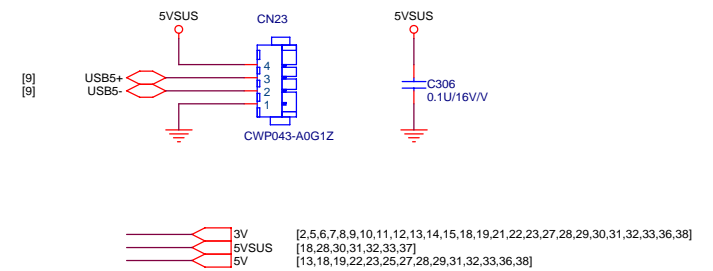
### SATA\_1 CONNECTOR



### For 17"W Second HDD SATA\_2 CONNECTOR



### USB WIRE TO DC BOARD X 1

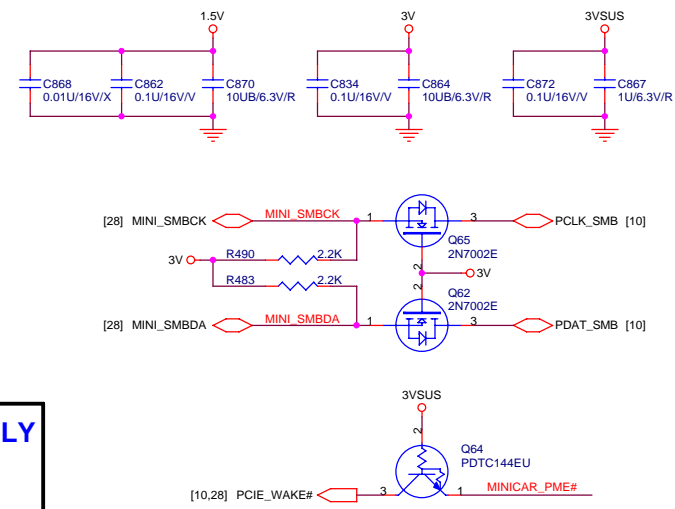
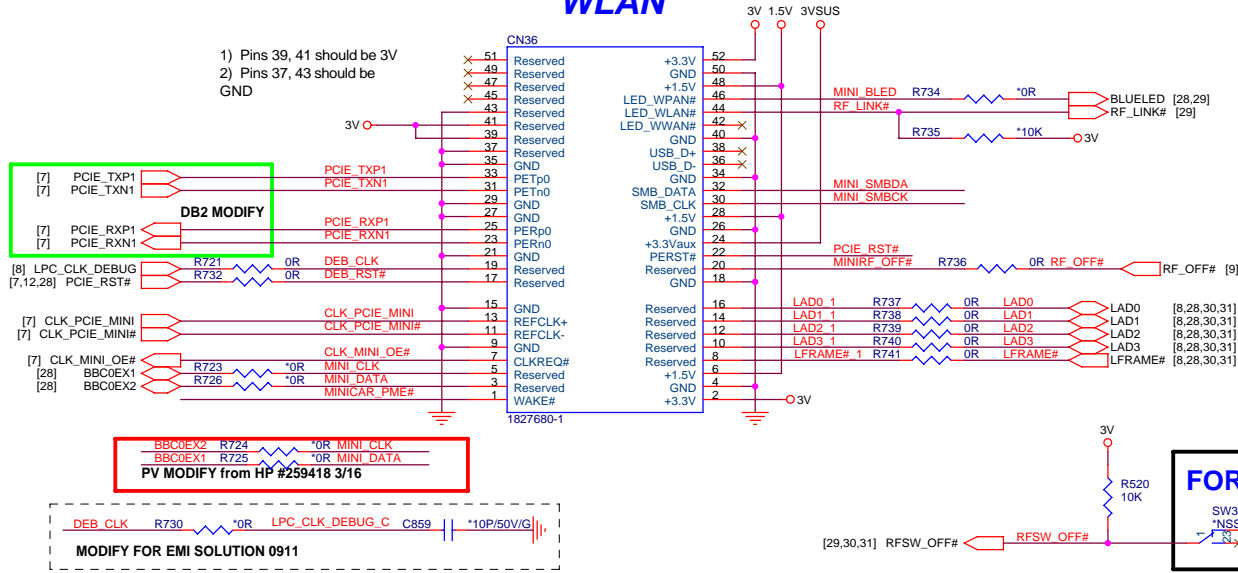


**PROJECT : AT1**  
Quanta Computer Inc.

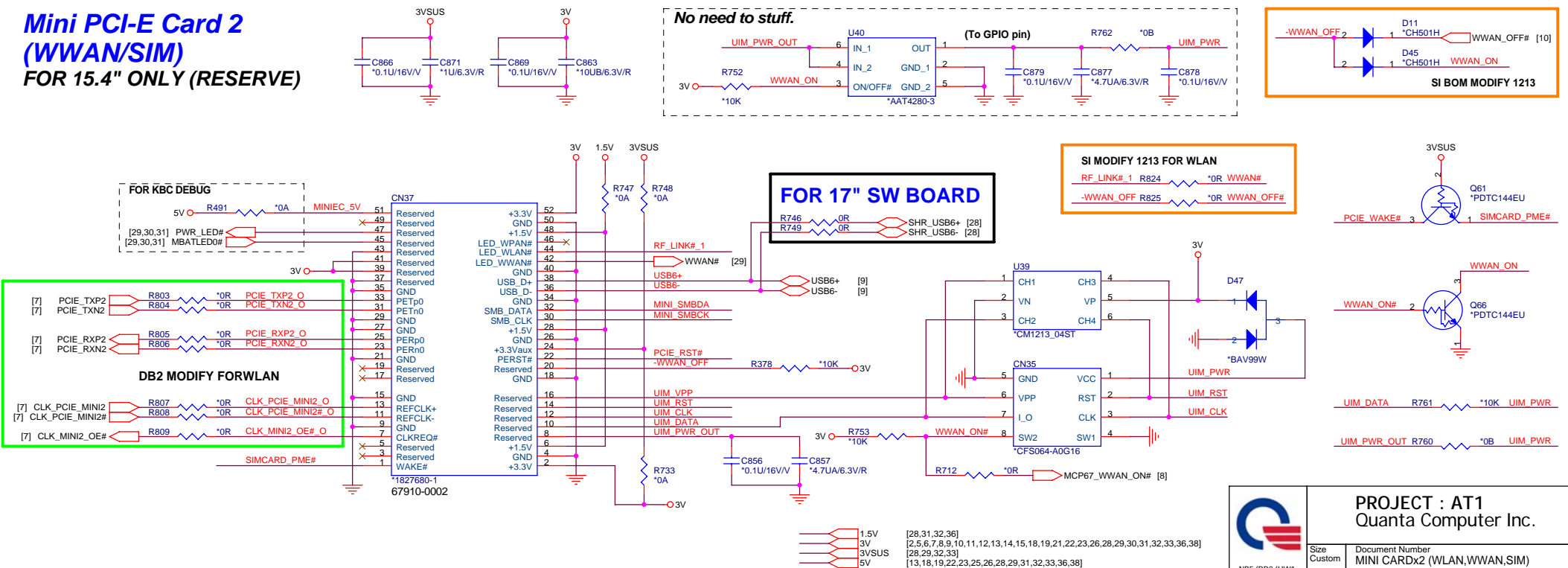
Size Custom	Document Number SATA HDDx2,CD-ROM,USBx3	Rev MV
Date: Tuesday, August 21, 2007	Sheet 26	of 40

NBS/RD2/HW1

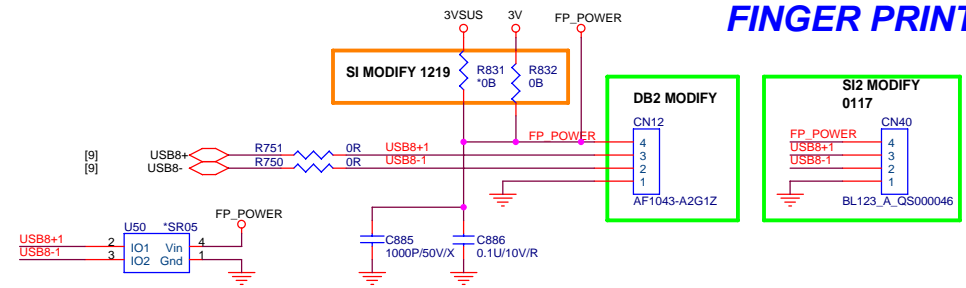
### Mini PCI-E Card 1 WLAN



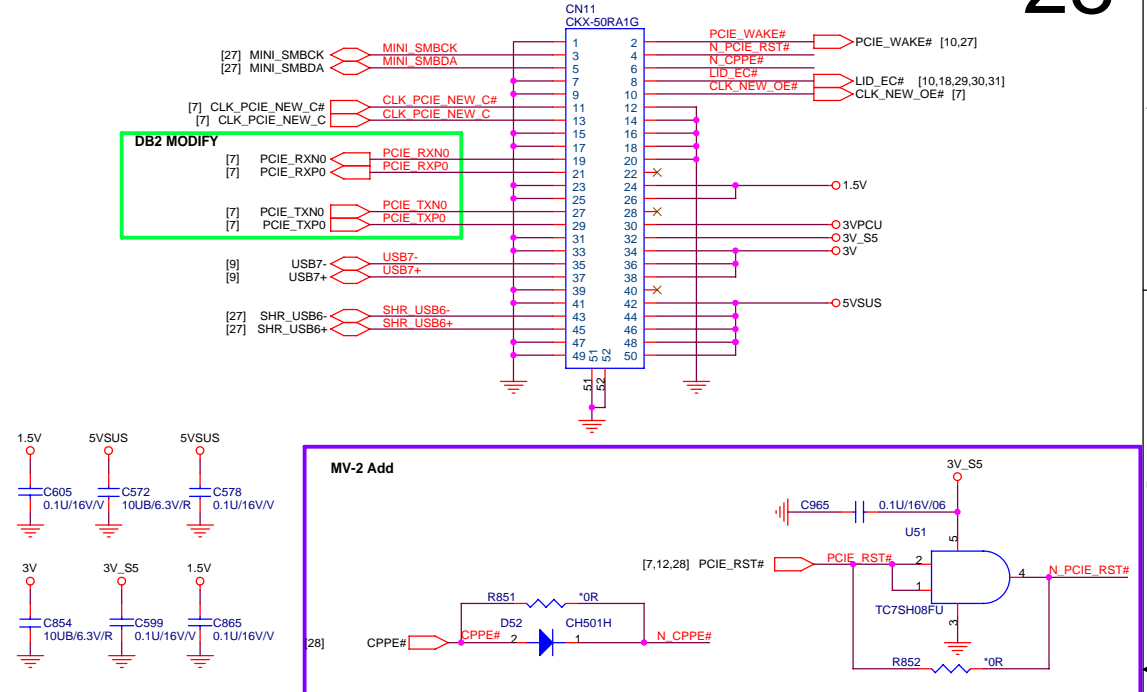
### Mini PCI-E Card 2 (WWAN/SIM) FOR 15.4" ONLY (RESERVE)



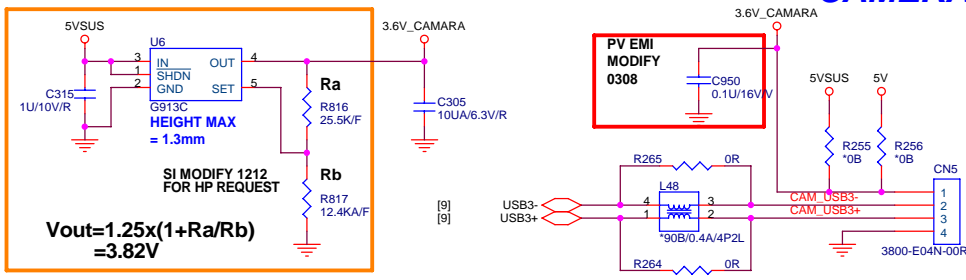
### FINGER PRINT



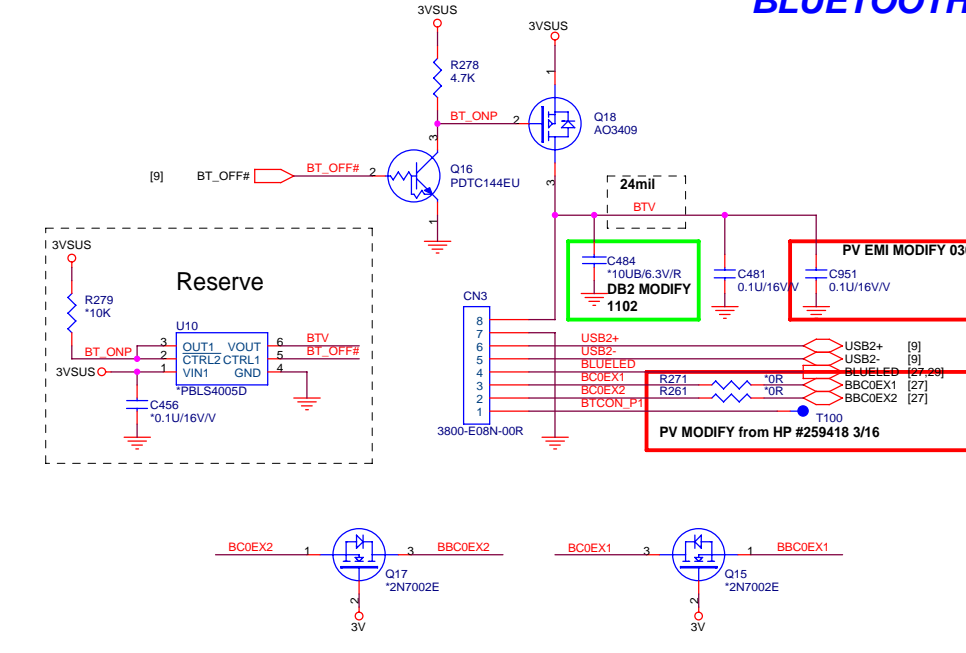
### NEW CARD



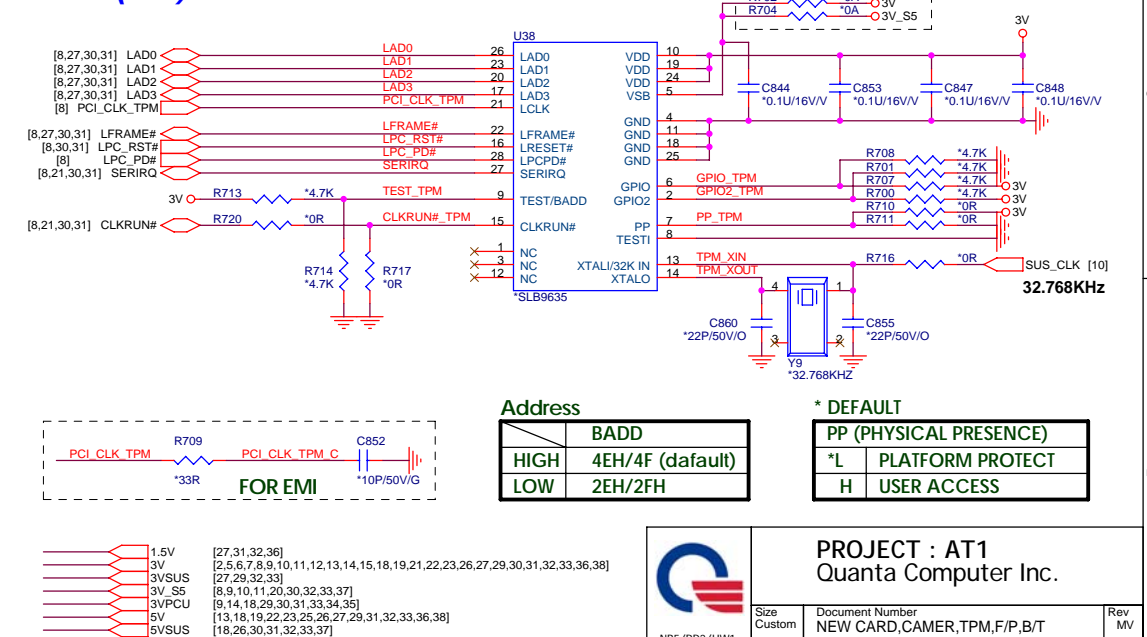
### CAMERA



### BLUETOOTH



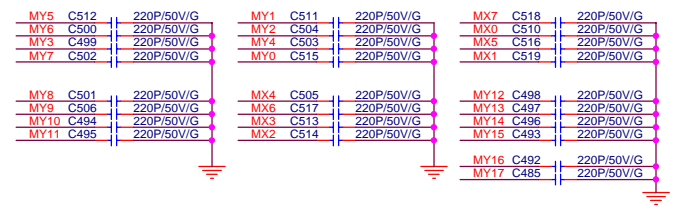
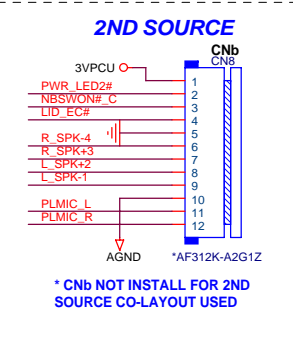
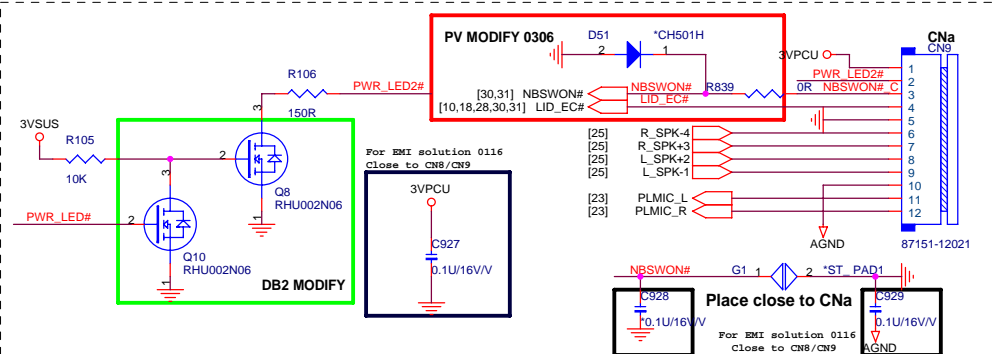
### TPM (1.2)



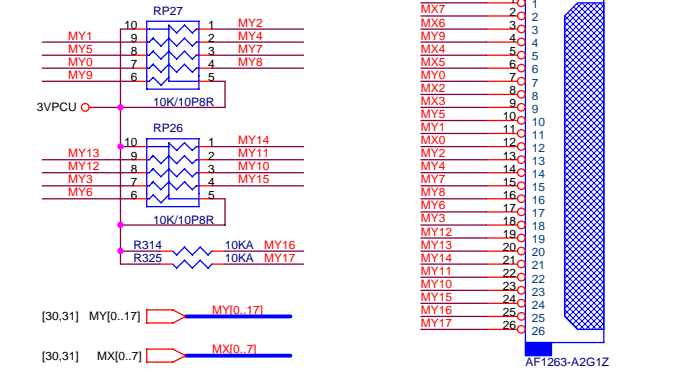
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number NEW_CARD,CAMER,TPM,F/P,B/T	Rev MV
Date: Tuesday, August 21, 2007	Sheet 28	of 40

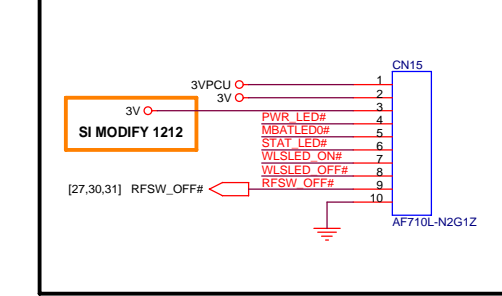
FOR POWER ON AND INTERNAL SPK / MIC SW BOARD



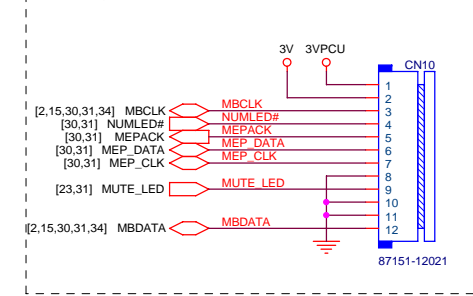
KEYBOARD PULL-UP



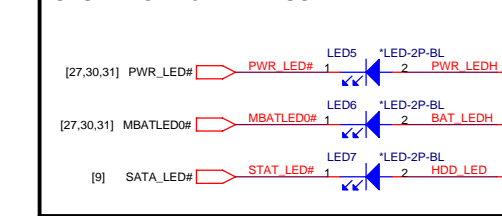
FOR 17" LED AND WIRLESS SW BOARD



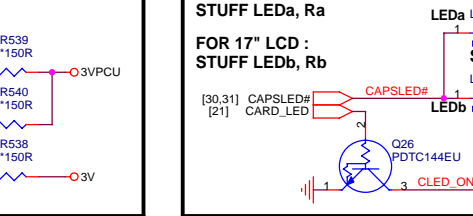
FOR QLB SW BOARD



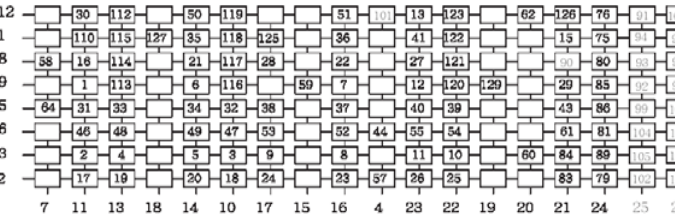
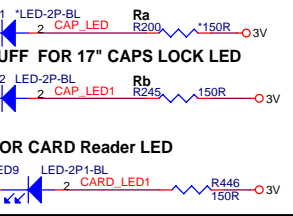
STUFF FOR 15.4" LED USED



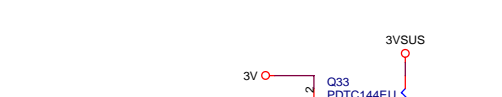
FOR 15.4" LCD : STUFF LEDa, Ra



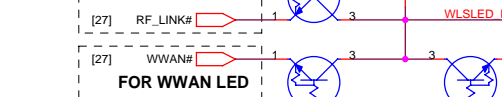
STUFF FOR 15.4" CAPS LOCK LED



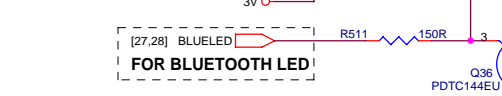
FOR WLAN LED



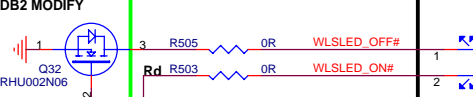
FOR WWAN LED



FOR BLUETOOTH LED



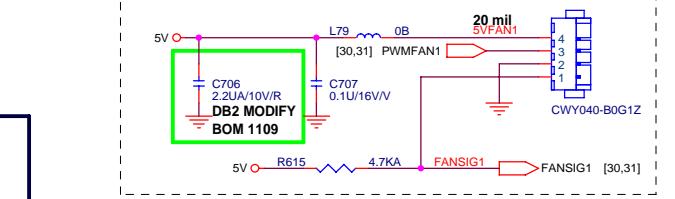
STUFF FOR 15.4" LED



FOR LED DRIVING ISSUE



FAN CONNECTOR

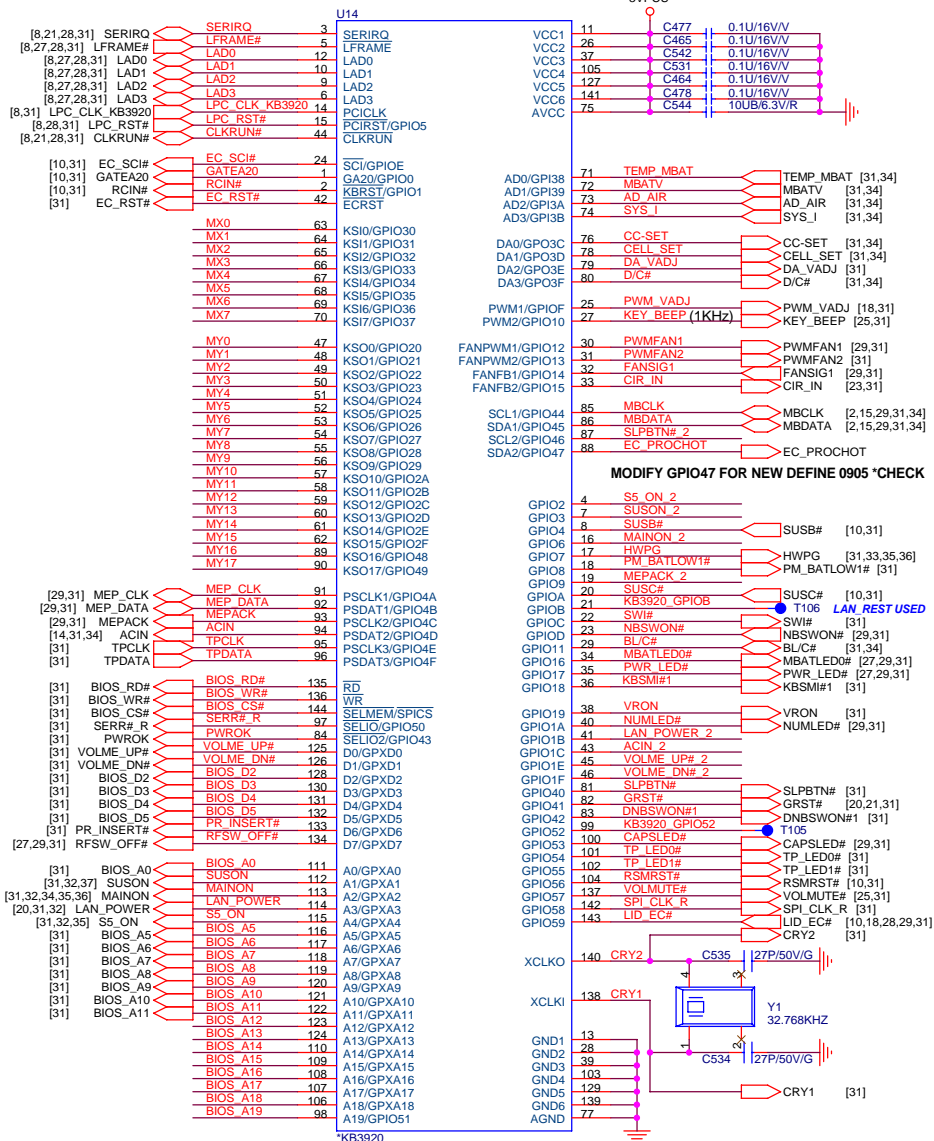


**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number KB.FAN.LED.SW (PWR,QLB,LED)	Rev MV
Date: Tuesday, August 21, 2007	Sheet 29	of 40

- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,30,31,32,33,36,38]
- 3VSUS [27,28,32,33]
- 3VPCU [9,14,18,28,30,31,33,34,35]
- 5V [13,18,19,22,23,25,26,27,28,31,32,33,36,38]

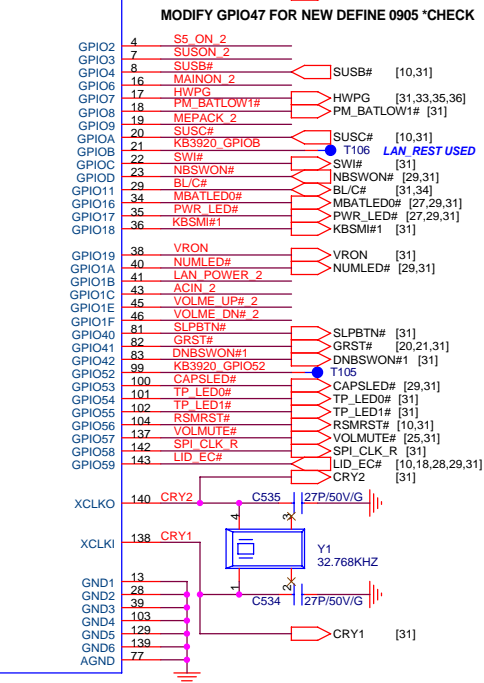
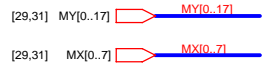
# EC - KB3920



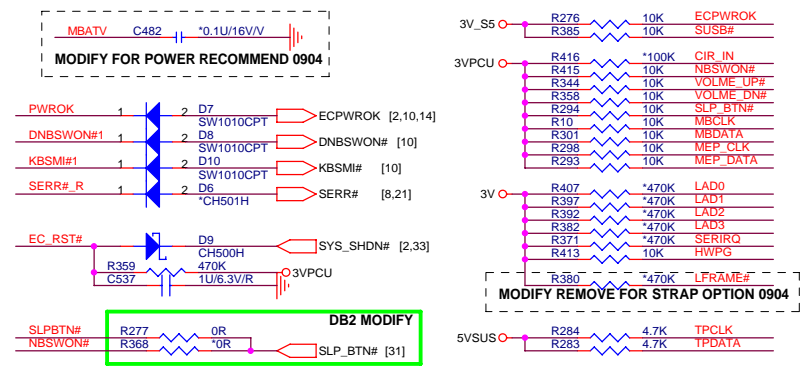
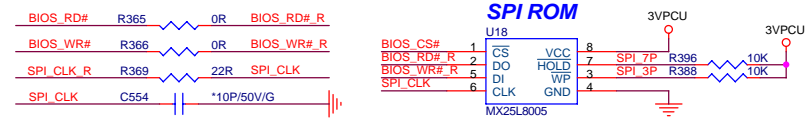
**IF USED KB3920 : Ra stuff 0 ohm**

**IF USED KB3920 : Ra leave NC**

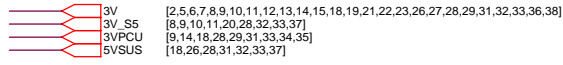
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: *32kHz clock in normal training	MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: *Boot from ISA flash part
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: *Normal operation	MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: *Normal Mode



### SI STUFF SPI ROM



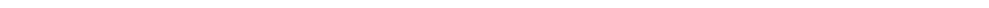
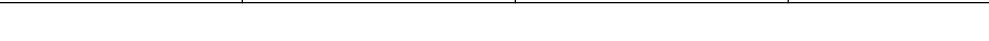
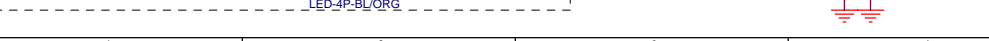
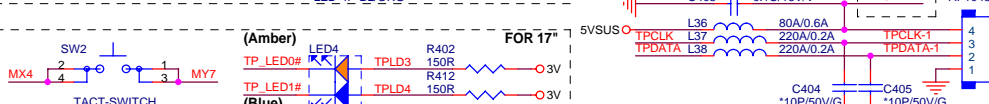
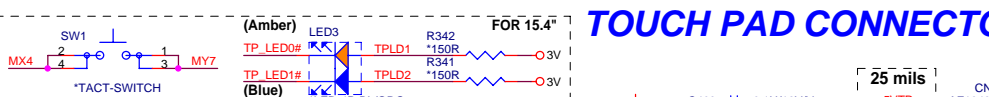
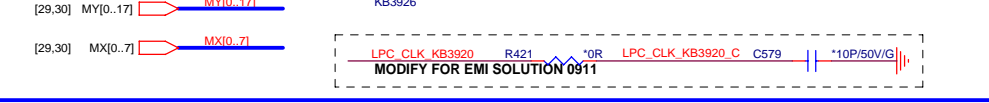
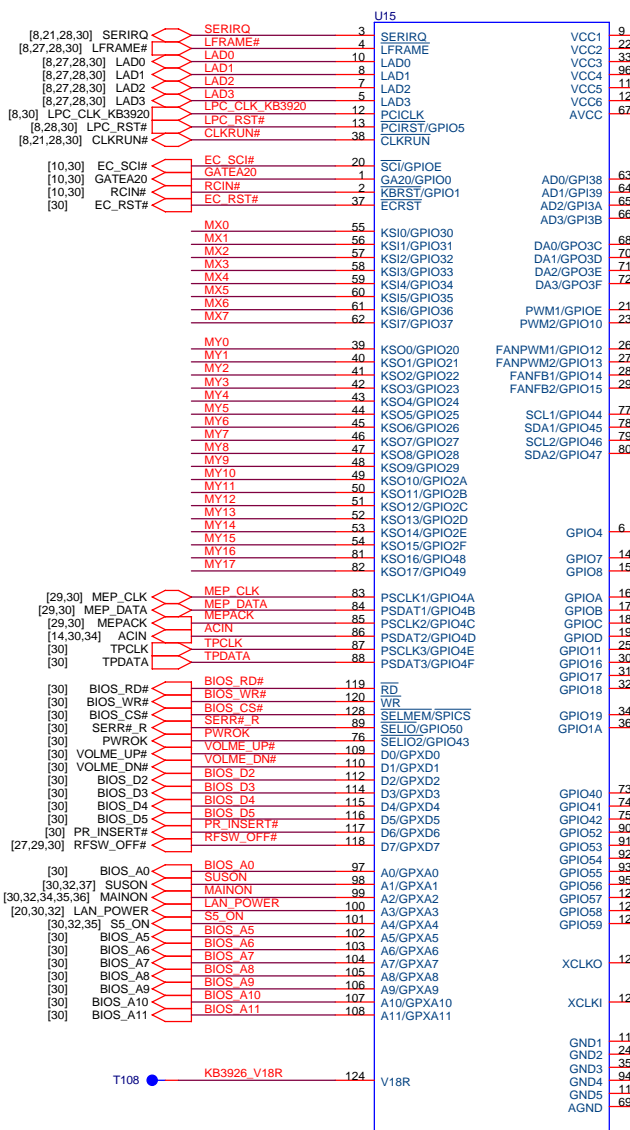
### DB2 MODIFY



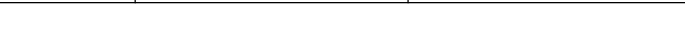
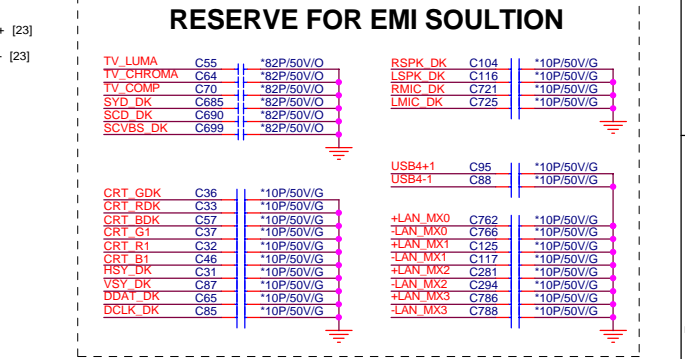
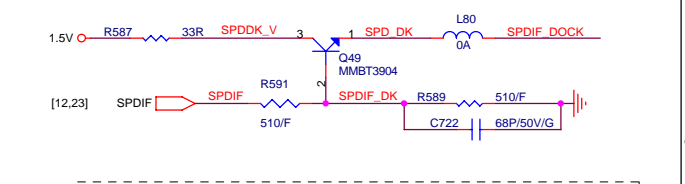
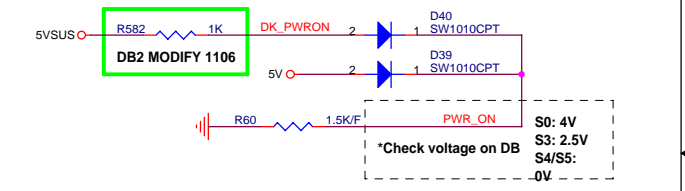
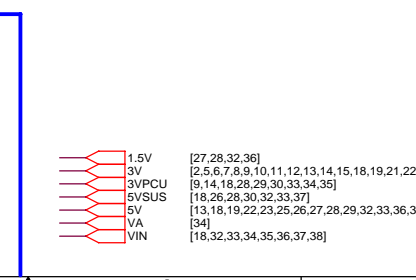
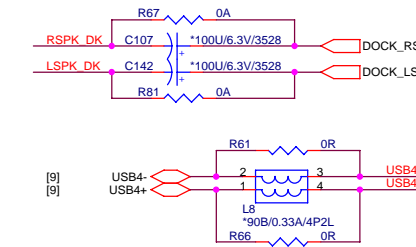
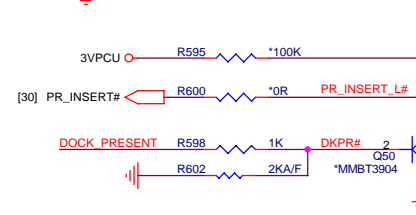
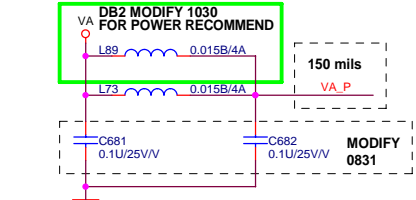
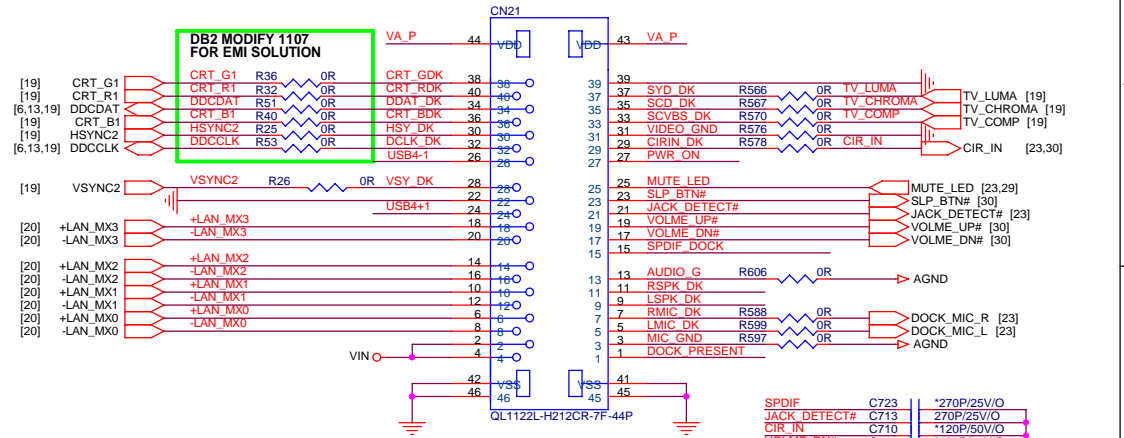
**PROJECT : AT1**  
**Quanta Computer Inc.**

Size Custom	Document Number KB3920_SPI_ROM	Rev MV
Date: Tuesday, August 21, 2007		
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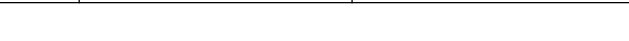
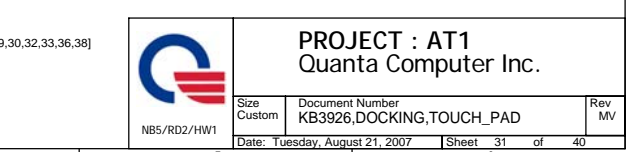
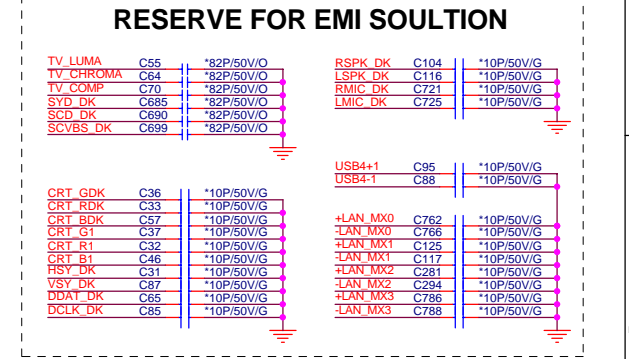
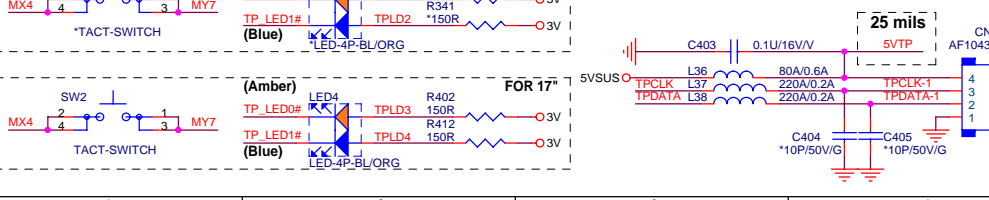
# EC - KB3926



# CABLE DOCK



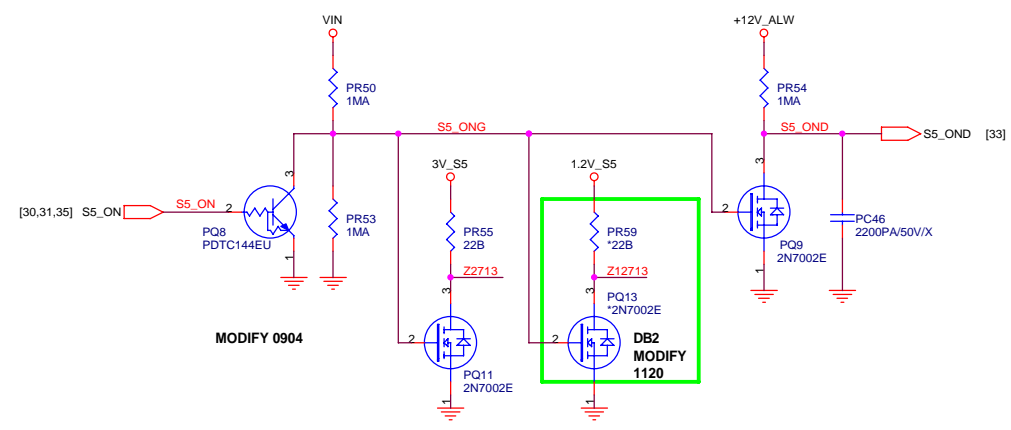
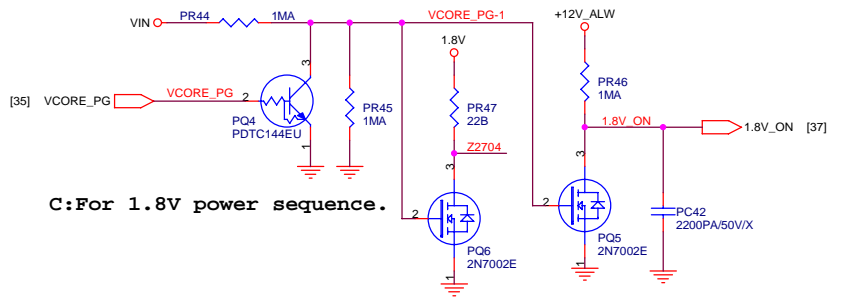
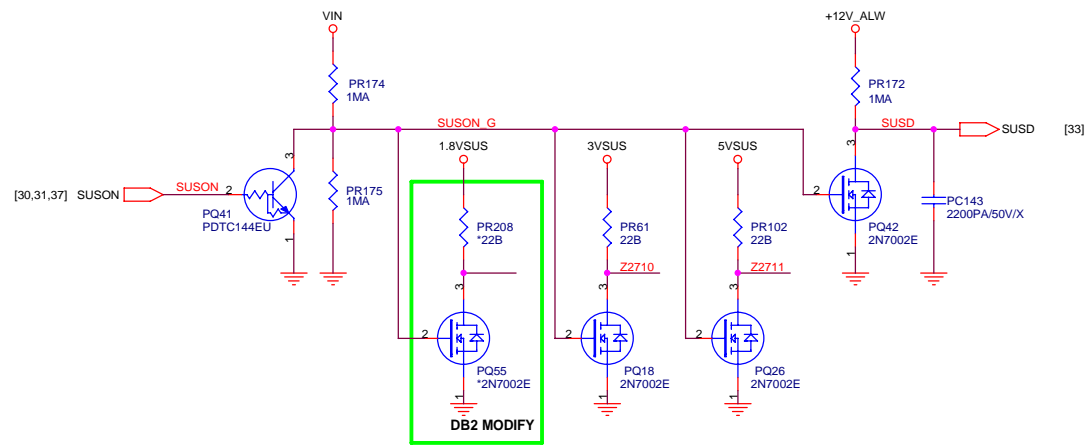
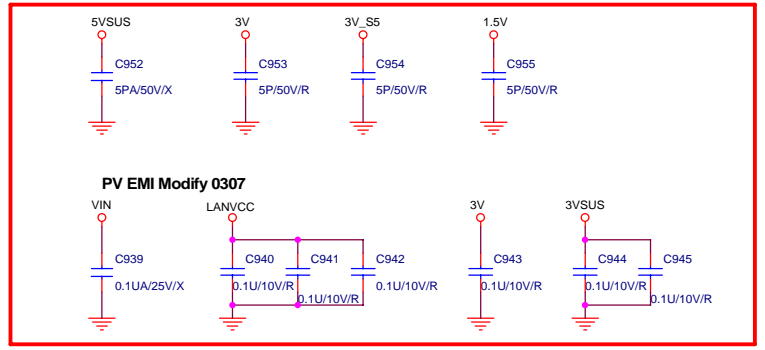
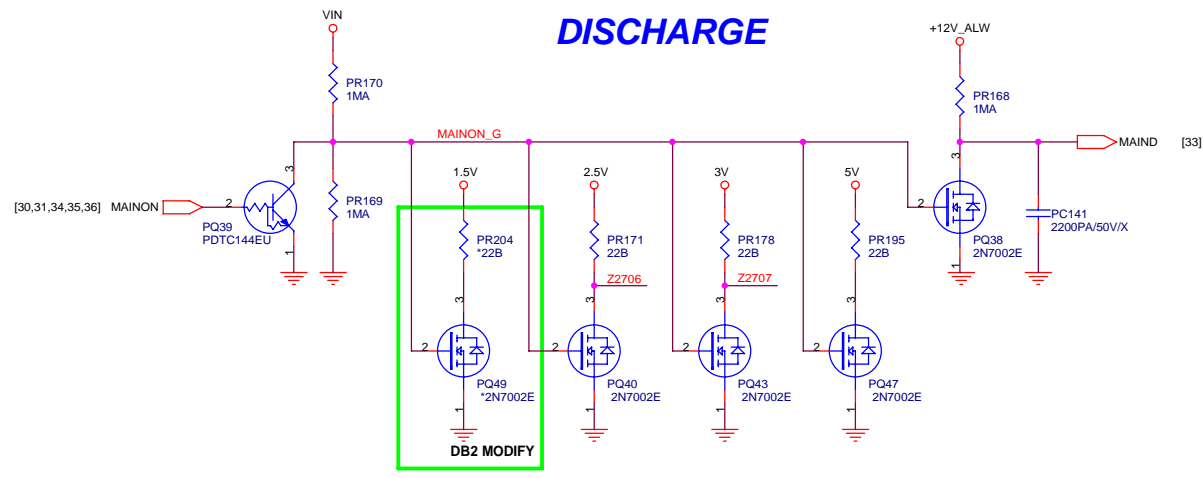
## TOUCH PAD CONNECTOR



			<p><b>PROJECT : AT1</b> Quanta Computer Inc.</p>
<p>Size Custom</p>	<p>Document Number KB3926.DOCKING, TOUCH_PAD</p>	<p>Rev MV</p>	
<p>Date: Tuesday, August 21, 2007</p>		<p>Sheet 31 of 40</p>	

**DISCHARGE**

**SI POWER MODIFY**



**LAN\_POWER (WOL FUNCTION)**

POWER STATES	AC MODE	DC MODE
S4 / S5	OFF	OFF
S3	ON	OFF
S0	ON	ON

- CPU\_CORE [4,38]
- 1.2V\_S5 [10,11,35]
- 1.5V [27,28,31,36]
- 1.8V [11,13,15,16,17,37]
- 1.8VSUS [2,3,4,5,6,36,37]
- 2.5V [2,13,36]
- LANVCC [20,33]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,33,36,38]
- 3VSUS [27,28,29,33]
- 3V\_S5 [8,9,10,11,20,28,30,33,37]
- 5V [13,18,19,22,23,25,26,27,28,29,31,33,36,38]
- 5VSUS [18,26,28,30,31,33,37]
- +12V\_ALW [10,18,33]
- VIN [18,31,33,34,35,36,37,38]

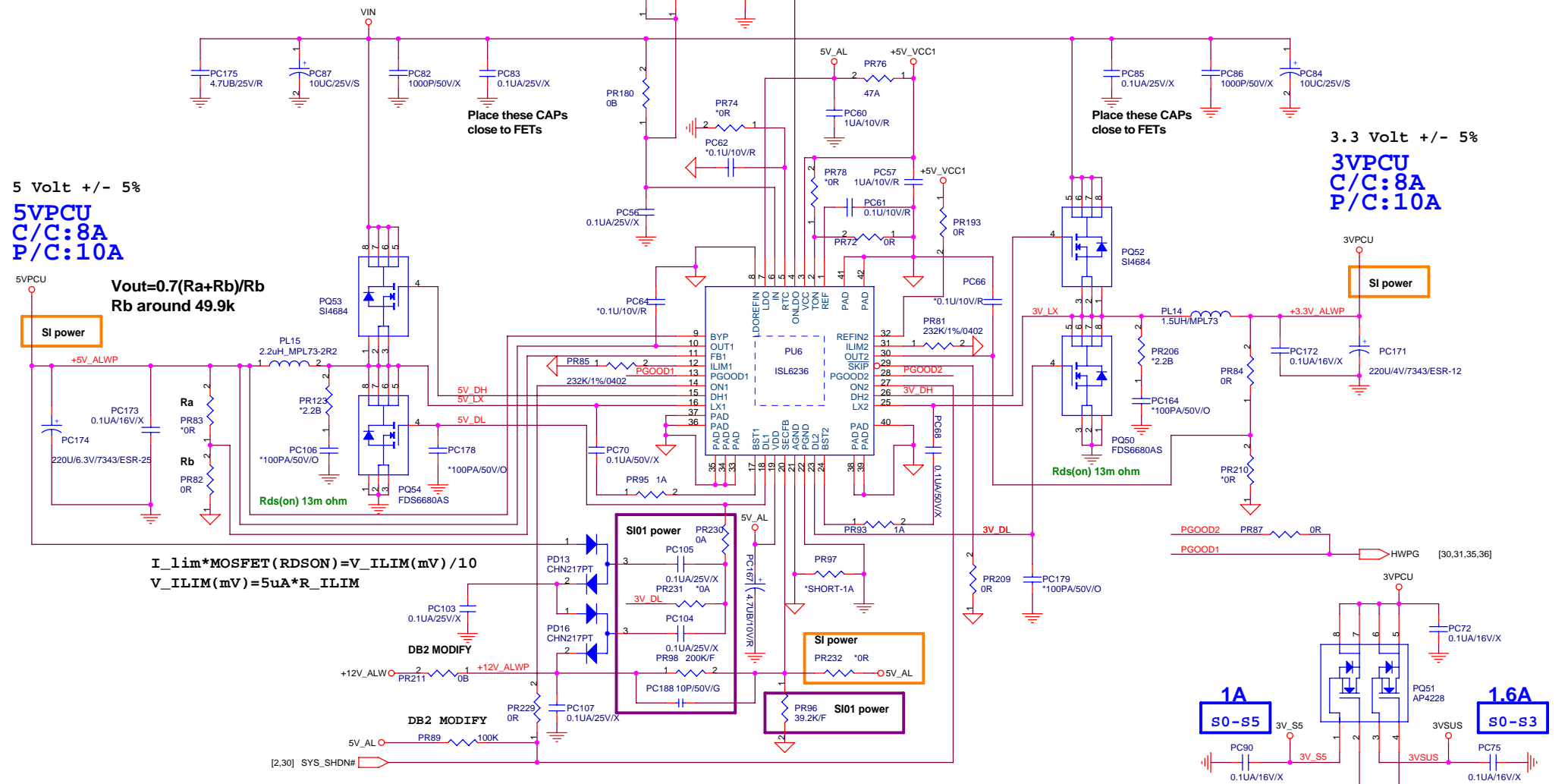
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom	Document Number <b>DISCHARGE</b>	Rev MV
Date: Tuesday, August 21, 2007		Sheet 32 of 40



# DC/DC 3VPCU/ 5VPCU/ +12V\_ALW

TOPN: OUT1/OUT2  
 GND=400KHz/500KHz  
 REF = 400KHz/300KHz  
 VCC5=200KHz/300KHz

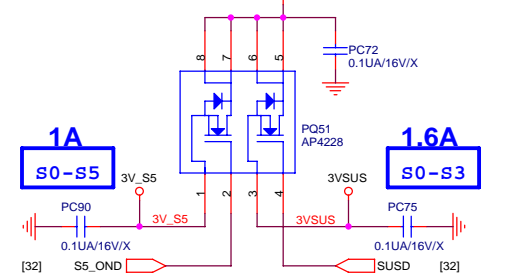
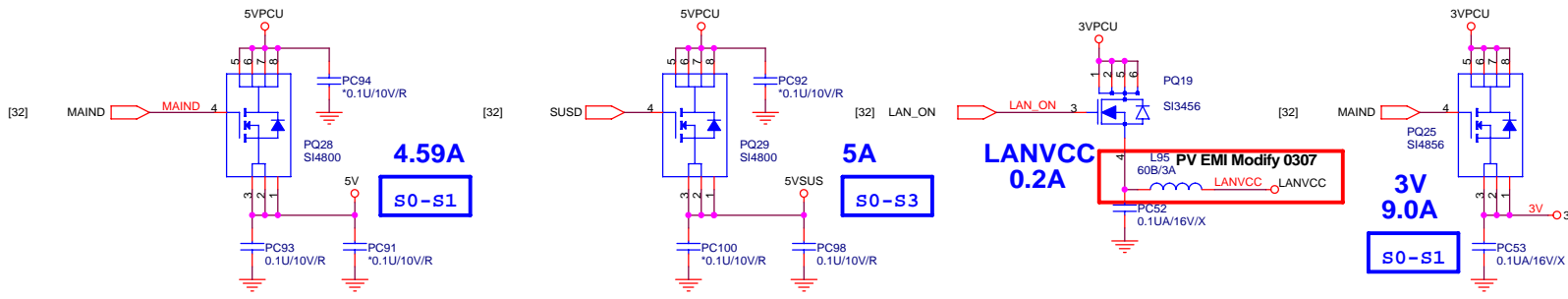


5 Volt +/- 5%  
**5VPCU**  
 C/C:8A  
 P/C:10A

3.3 Volt +/- 5%  
**3VPCU**  
 C/C:8A  
 P/C:10A

$V_{out} = 0.7(Ra + Rb) / Rb$   
 Rb around 49.9k

$I_{lim} * MOSFET (RDSON) = V_{ILIM} (mV) / 10$   
 $V_{ILIM} (mV) = 5uA * R_{ILIM}$



+12V_ALW	[10,18,32]
LANVCC	[20,32]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,36,38]
3VSUS	[27,28,29,32]
3V_S5	[8,9,10,11,20,28,30,32,37]
3VPCU	[9,14,18,28,29,30,31,34,35]
5V	[13,18,19,22,23,25,26,27,28,29,31,32,36,38]
5VSUS	[18,26,28,30,31,32,37]
5VPCU	[10,23,34,35,36,37,38]
VIN	[18,31,32,34,35,36,37,38]

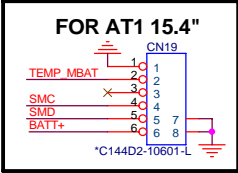
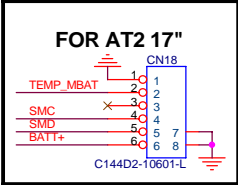
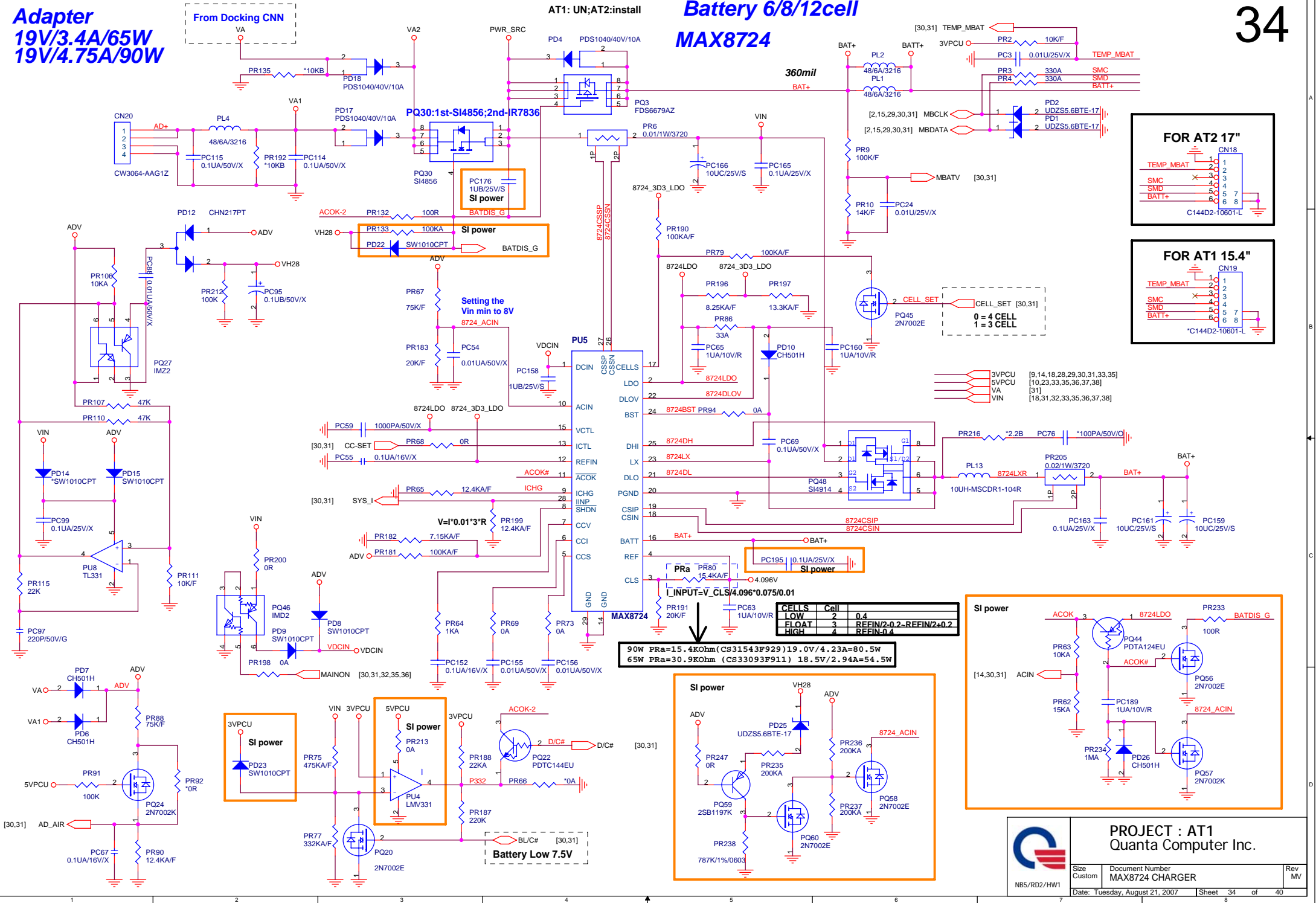


PROJECT : AT1  
 Quanta Computer Inc.

Size Custom	Document Number ISL6236 (5VPCU,3VPCU)	Rev MV
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**Adapter**  
**19V/3.4A/65W**  
**19V/4.75A/90W**

**Battery 6/8/12cell**  
**MAX8724**

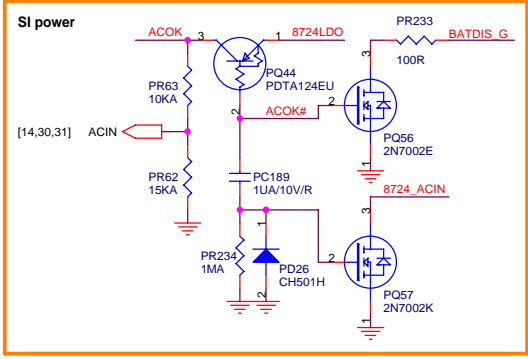
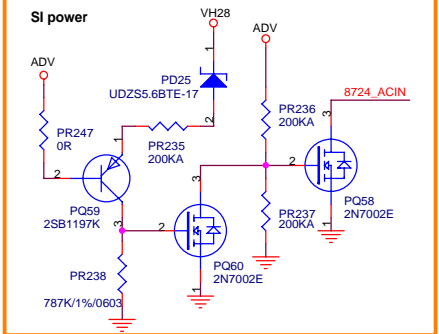


3VPCU [9,14,18,28,29,30,31,33,35]  
 5VPCU [10,23,33,35,36,37,38]  
 VA [31]  
 VIN [18,31,32,33,35,36,37,38]

CELLS	Cell
LOW	2
FLOAT	3
HIGH	4

REFIN/2.0 2-REFIN/2.0 2  
 REFIN-0.4

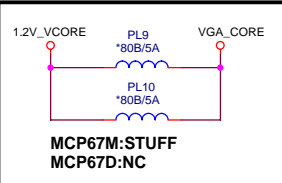
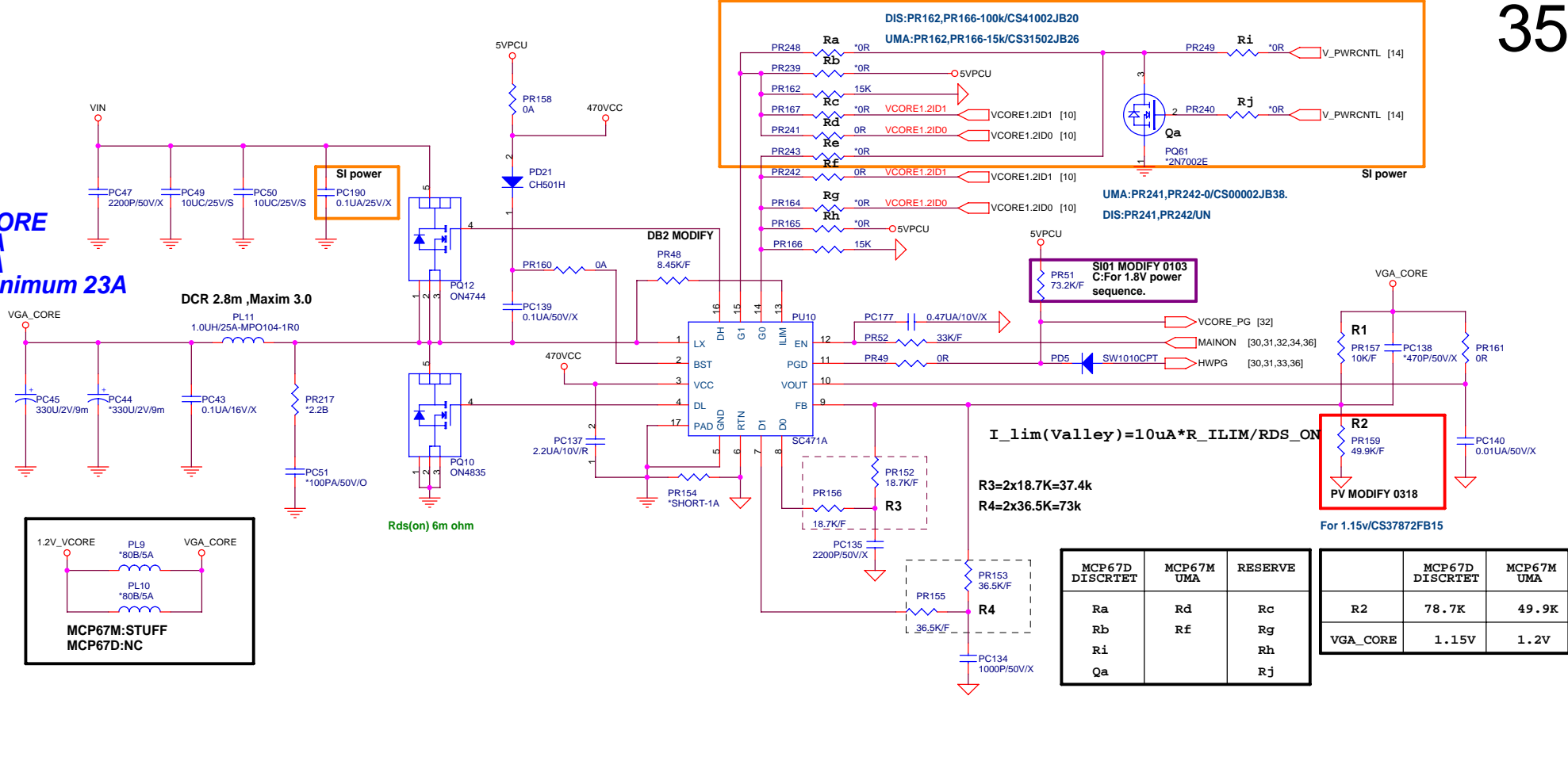
90W P<sub>ra</sub>=15.4Kohm (CS31543F929) 19.0V/4.23A=80.5W  
 65W P<sub>ra</sub>=30.9Kohm (CS33093F911) 18.5V/2.94A=54.5W



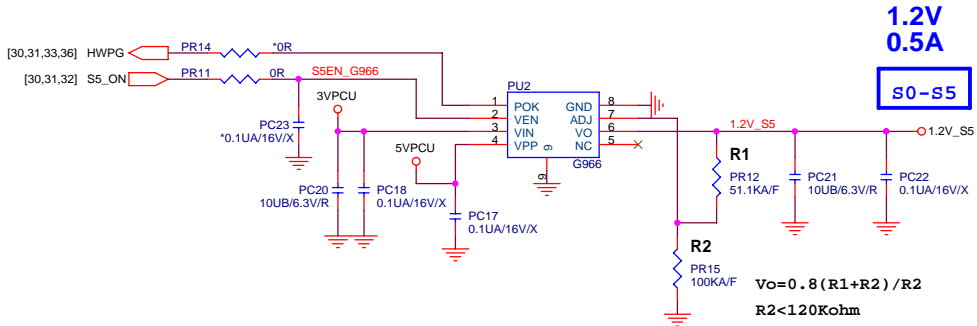
**PROJECT : AT1**  
**Quanta Computer Inc.**

Size Custom	Document Number MAX8724 CHARGER	Rev MV
Date: Tuesday, August 21, 2007	Sheet 34 of 40	

VGA\_CORE  
C/C:12A  
P/C:15A  
OCP minimum 23A



INPUTS					
VCORE1.2ID1	VCORE1.2ID0	OUTPUTS			VGA_CORE
G0	G1	OD1	OD2	OD3	
0	0	$0.75x(1+R1/R2+R1/R3+R1/R4)$			1.2V
0	1	$0.75x(1+R1/R2+R1/R3)$			1.1V
1	0	$0.75x(1+R1/R2+R1/R4)$			1.0V
1	1	$0.75x(1+R1/R2)$			0.9V



MCP67D DISCRETET	MCP67M UMA	RESERVE
Ra	Rd	Rc
Rb	Rf	Rg
Ri	Rh	Rj
Qa		

	MCP67D DISCRETET	MCP67M UMA
R2	78.7K	49.9K
VGA_CORE	1.15V	1.2V

- 1.2V\_S5 [10,11,32]
- 1.2V\_VCORE [11,36]
- VGA\_CORE [12]
- 3VPCU [9,14,18,28,29,30,31,33,34]
- 5VPCU [10,23,33,34,36,37,38]
- VIN [18,31,32,33,34,36,37,38]



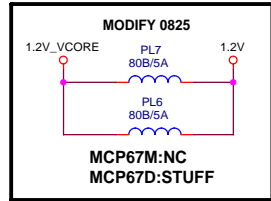
PROJECT : AT1  
Quanta Computer Inc.

Size Custom	Document Number SC471A (VGA_CORE), 1.2V_S5	Rev MV
Date: Tuesday, August 21, 2007	Sheet 35	of 40

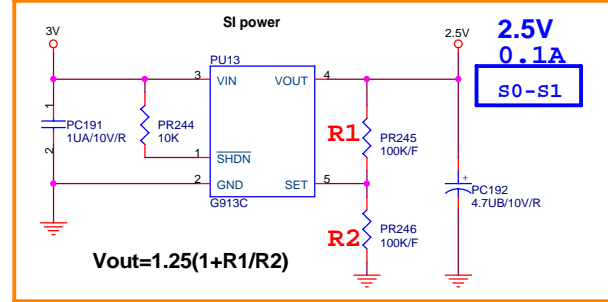
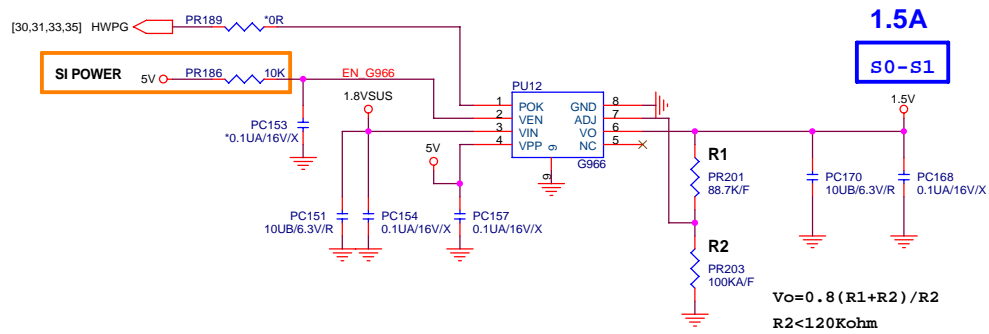
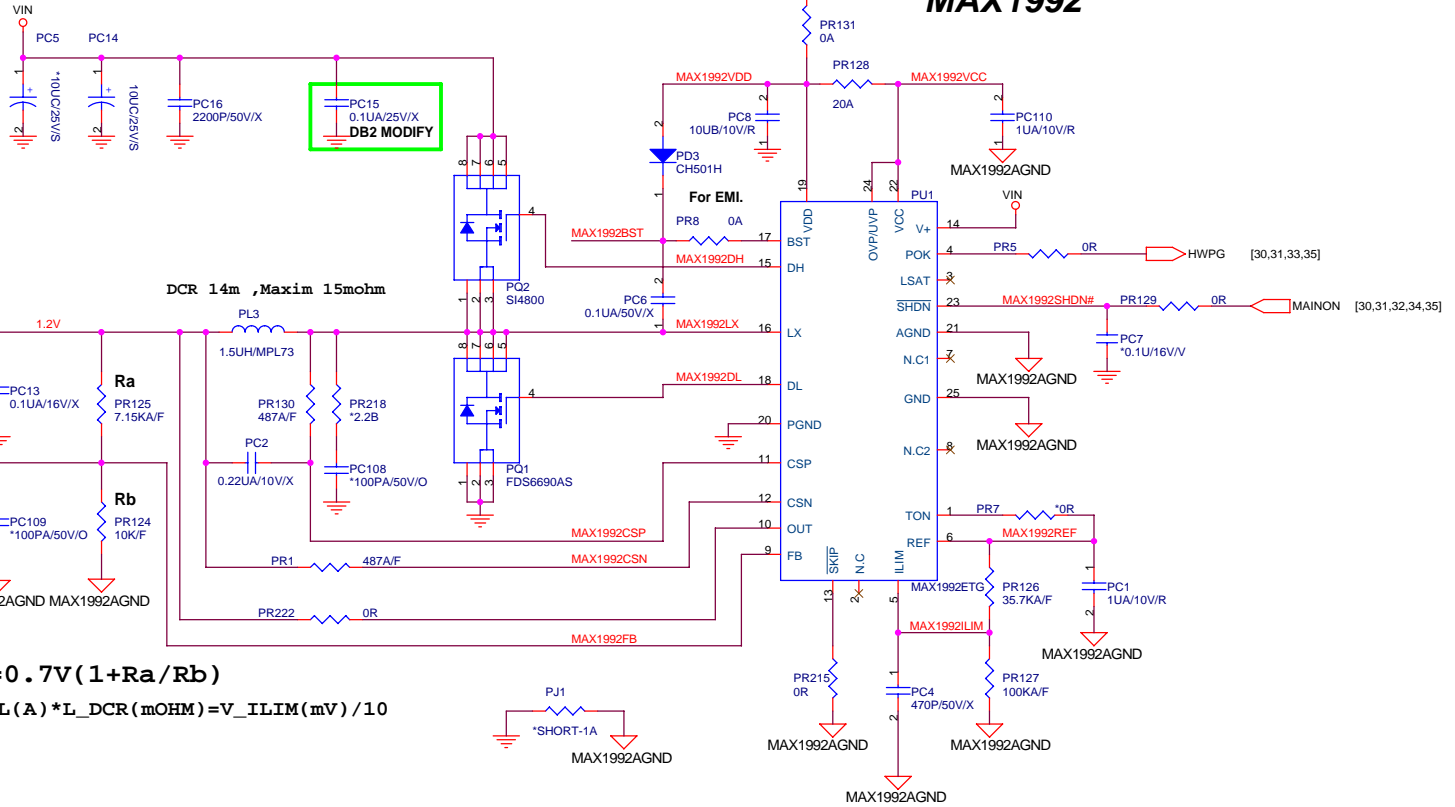
MAX1992

S0-S1

1.2V  
C/C:6A  
P/C:8A  
OCP minimum 10A



$V_{out} = 0.7V(1 + R_a/R_b)$   
 $V_{cs} = I_L(A) * L_{DCR}(mOHM) = V_{ILIM}(mV) / 10$

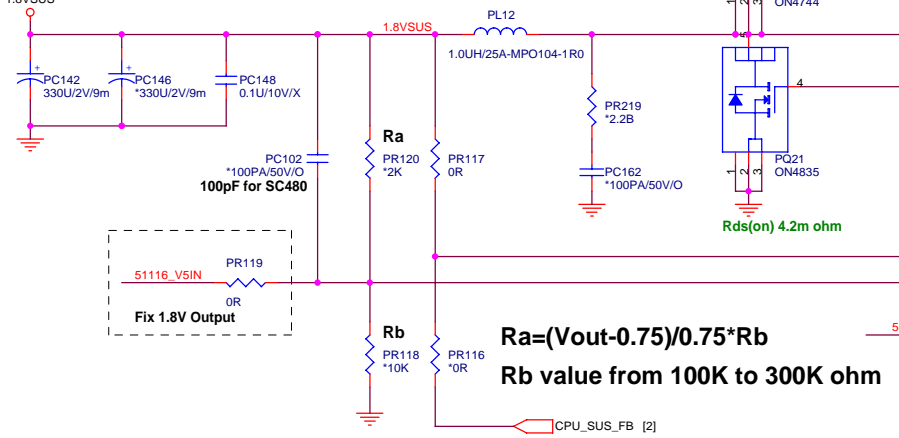


- 1.2V\_VCORE [11,35]
- 1.2V [10,11,12,13,15]
- 1.5V [27,28,31,32]
- 1.8V\_SUS [2,3,4,5,6,32,37]
- 2.5V [2,13,32]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,38]
- 5V [13,18,19,22,23,25,26,27,28,29,31,32,33,38]
- 5VPCU [10,23,33,34,35,37,38]
- VIN [18,31,32,33,34,35,37,38]

S0-S3

1.8VSUS  
C/C:12A  
P/C:15.2A  
OCP minimum 25A

1.8 Volt +/-5%



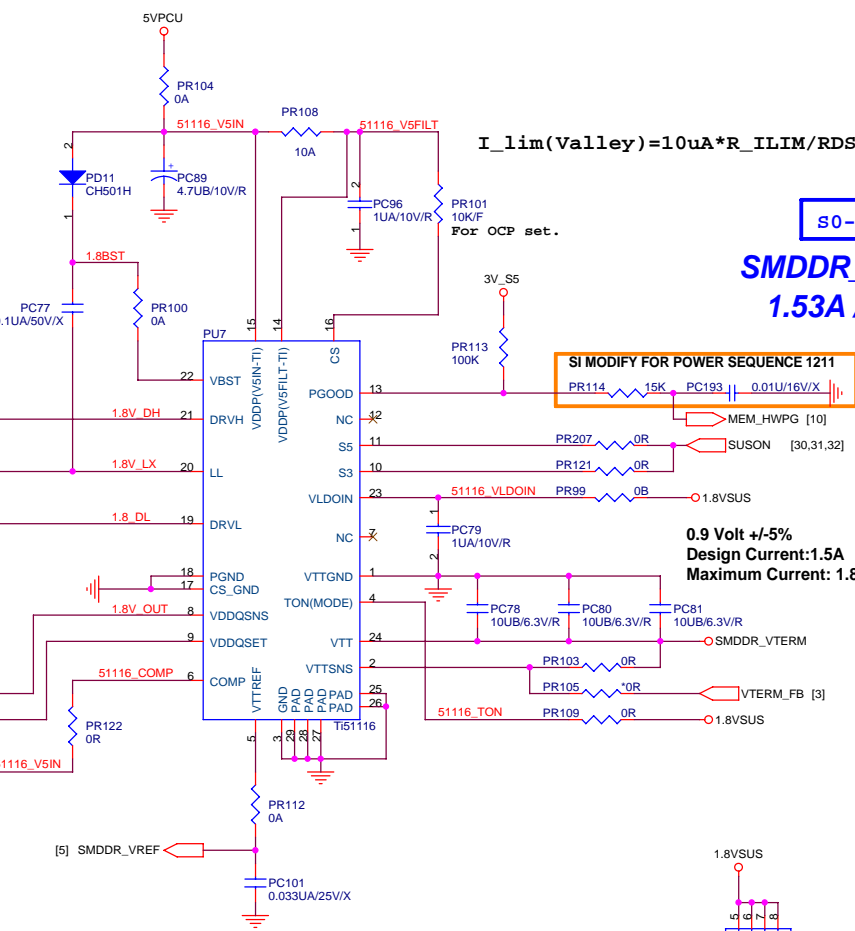
$I_{lim}(Valley) = 10\mu A * R_{ILIM} / RDS_{ON}$

S0-S3

SMDDR\_VTERM  
1.53A / 0.9V

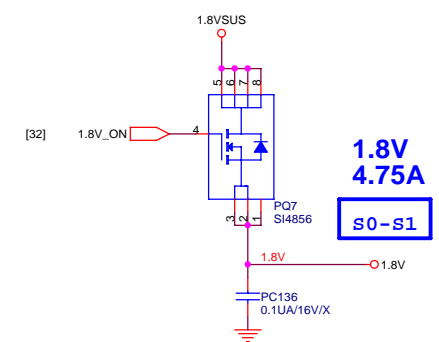
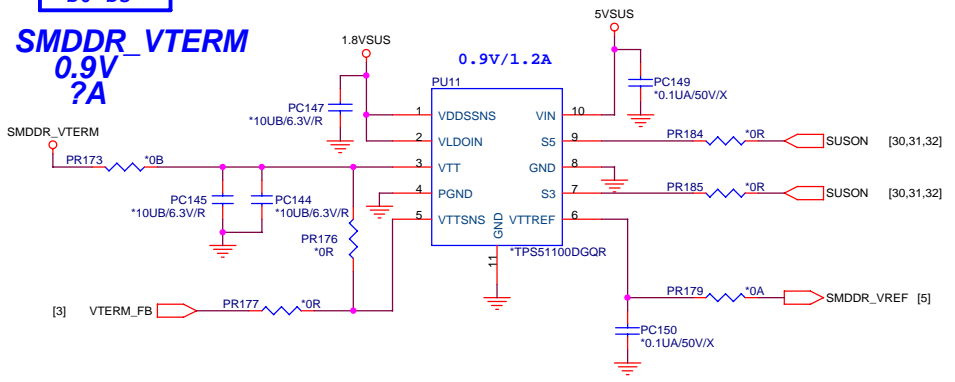
SI MODIFY FOR POWER SEQUENCE 1211

0.9 Volt +/-5%  
Design Current:1.5A  
Maximum Current: 1.8A



S0-S3

SMDDR\_VTERM  
0.9V  
?A



Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(\mu A)$

$I_{OCP} = V_{trip} / Rds_{on} + I_{Ripple} / 2$

VDDQSET	VDDQ(V)	VTREF and Vtt	Note
GND	2.5	V_vddqsns/2	DDR
V5IN	1.8	V_vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V < VDDQ < 3V

- SMDDR\_VTERM [4]
- 1.8V [11,13,15,16,17,32]
- 1.8VSUS [2,3,4,5,6,32,36]
- 3V\_S5 [8,9,10,11,20,28,30,32,33]
- 5VSUS [18,26,28,30,31,32,33]
- 5VPCU [10,23,33,34,35,36,38]
- VIN [18,31,32,33,34,35,36,38]

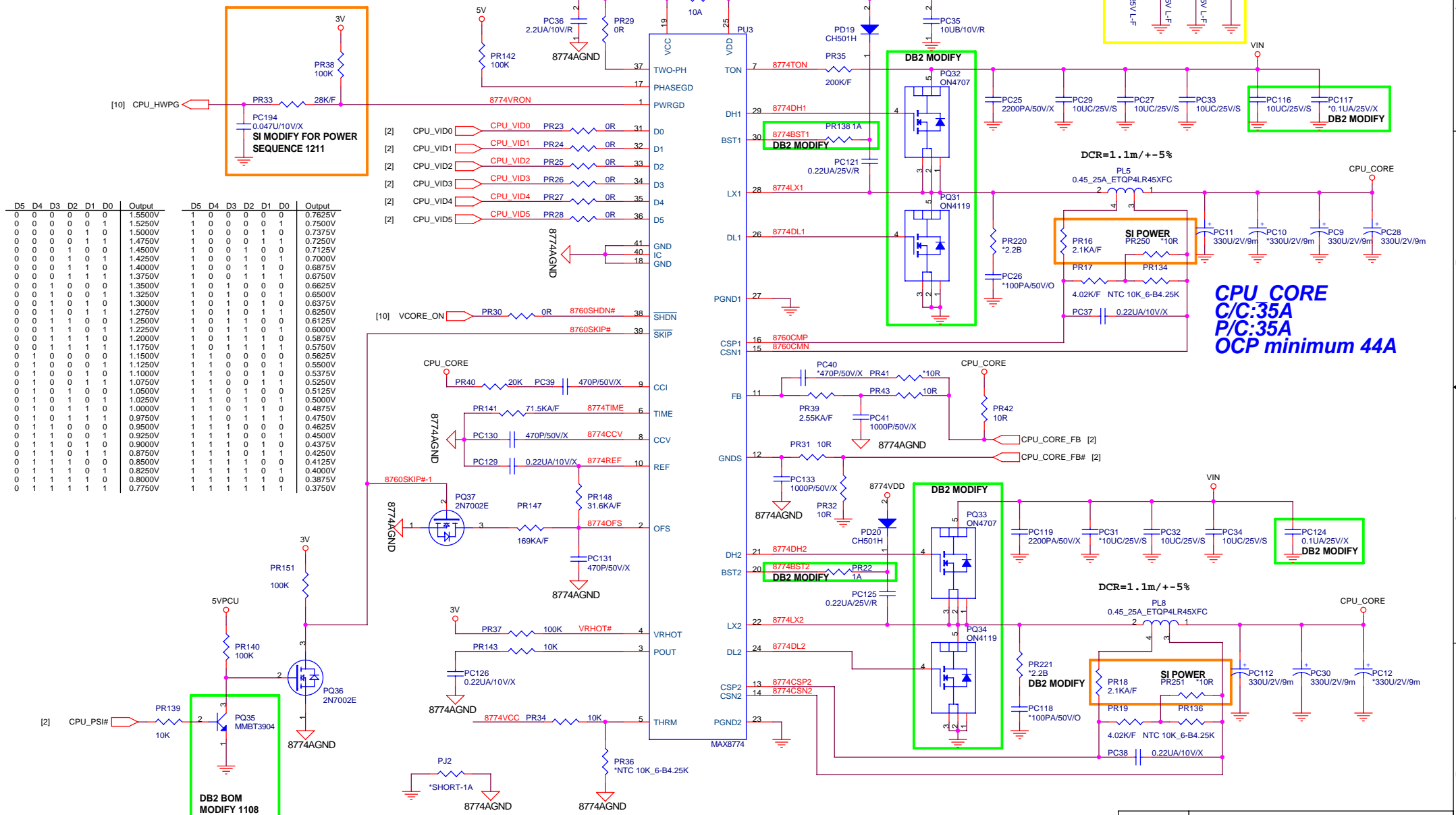
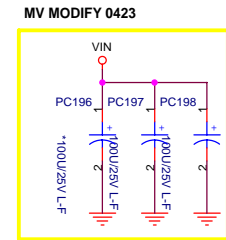
**PROJECT : AT1**  
Quanta Computer Inc.

Size Custom Document Number T151116 (1.8VSUS,VTER),1.8V Rev MV

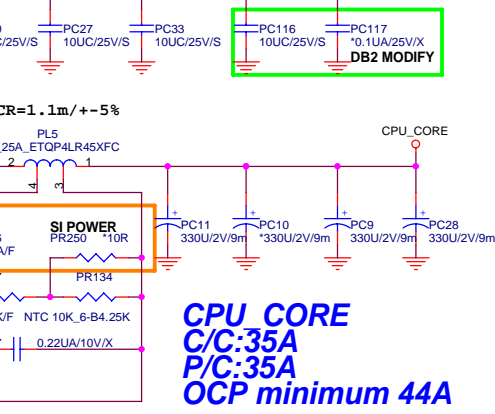
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Slew rate=(12.5mVus)\*(71.5K/R\_TIME)  
 VFB=V\_VID+0.125(VREF-VOFS)  
 VRHOT is low when VTHRM below 1.5V  
 Tsw=16.26pF(R\_TON+6.5K)ohm  
 CCV CAP=470pF\*(2/total phase)\*300KHz/fsw

# CPU\_CORE MAX8774



D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7500V
0	0	0	0	0	1	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	0	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	0	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9250V	1	1	1	0	1	0	0.4500V
0	1	1	0	1	0	0.9000V	1	1	1	0	1	1	0.4375V
0	1	1	0	1	1	0.8750V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8500V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8250V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.8000V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	1	0.3750V



**CPU\_CORE**  
 C/C:35A  
 P/C:35A  
 OCP minimum 44A

- CPU\_CORE [4,32]
- 3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36]
- 5V [13,18,19,22,23,25,26,27,28,29,31,32,33,36]
- 5VPCU [10,23,33,34,35,36,37]
- VIN [18,31,32,33,34,35,36,37]

**PROJECT : AT1**  
 Quanta Computer Inc.

Size Custom	Document Number MAX8774 (CPU_CORE)	Rev MV
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