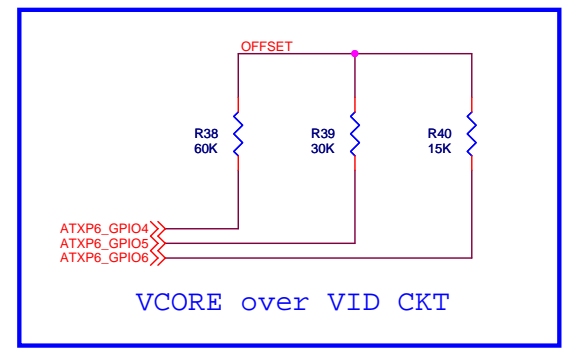
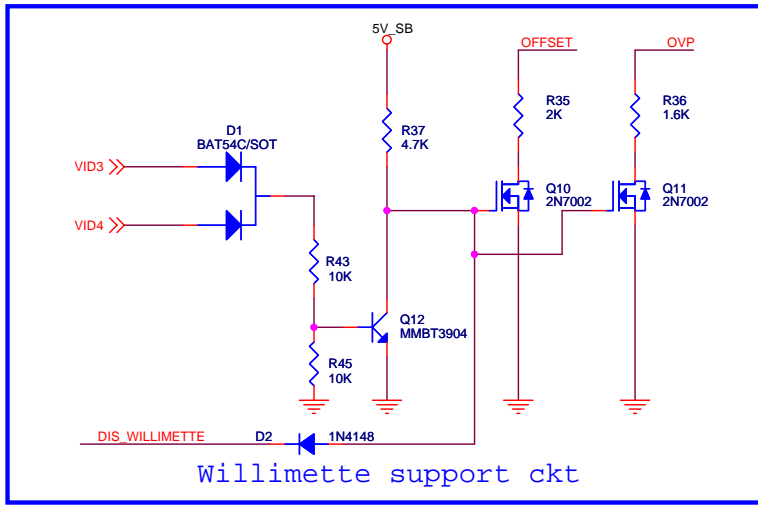
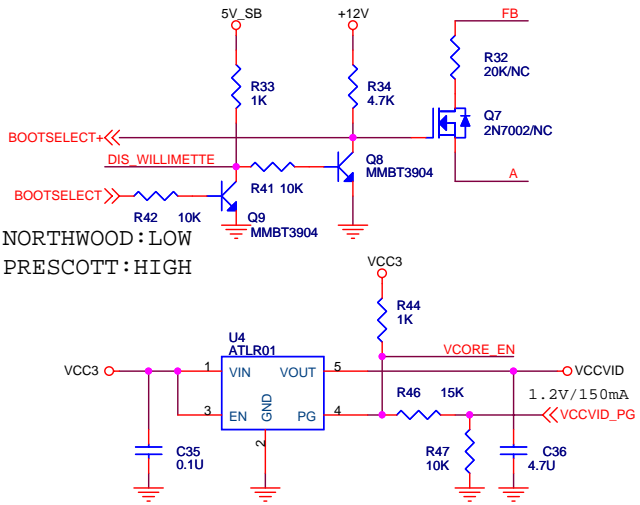
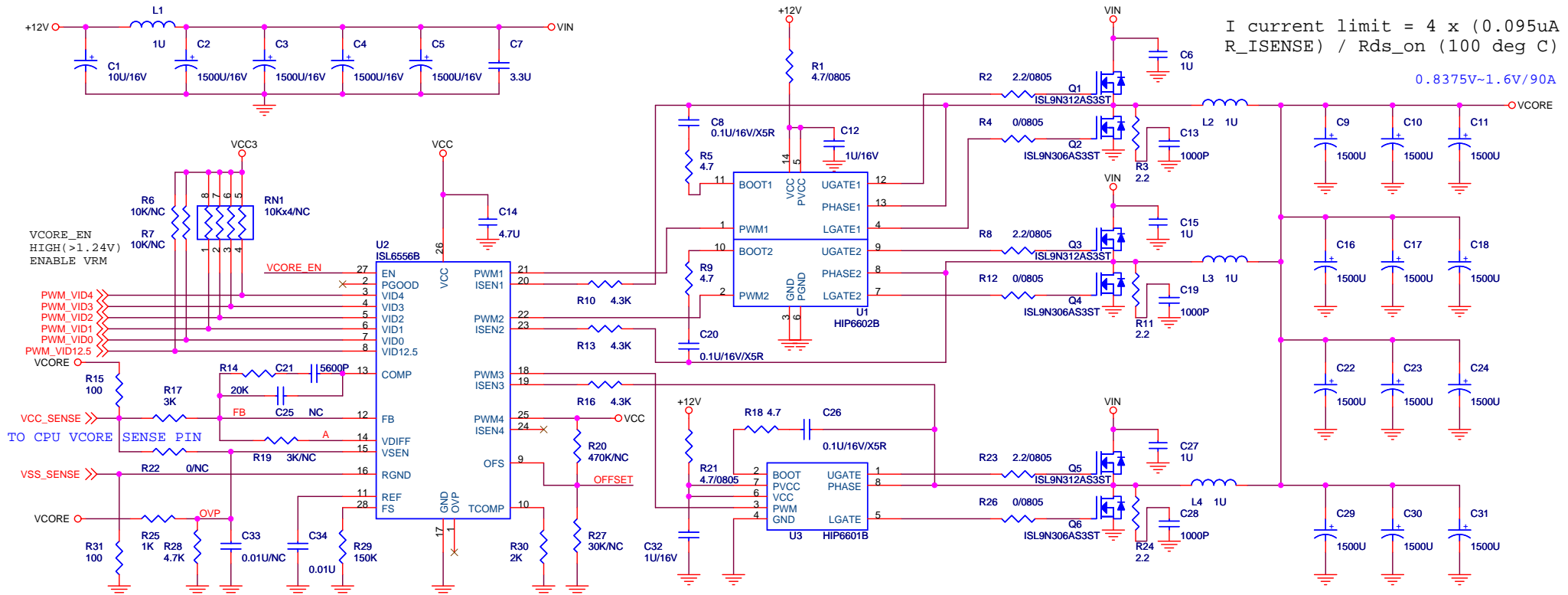


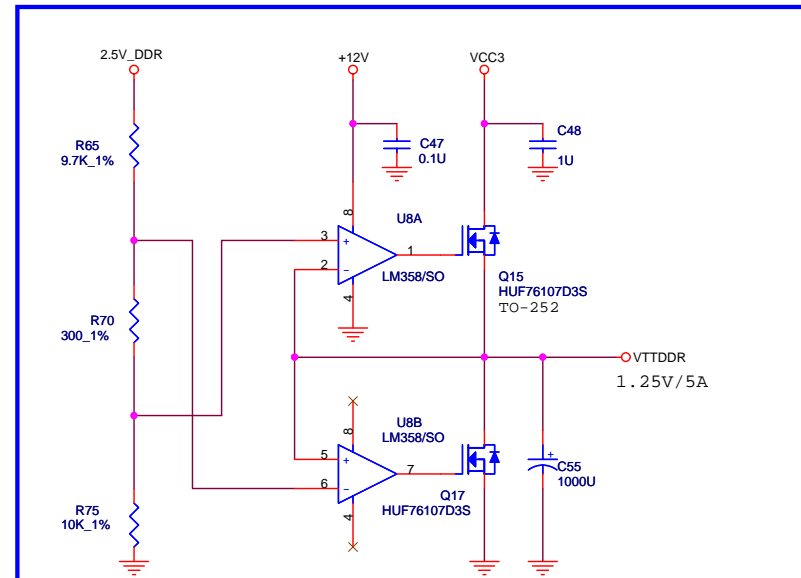
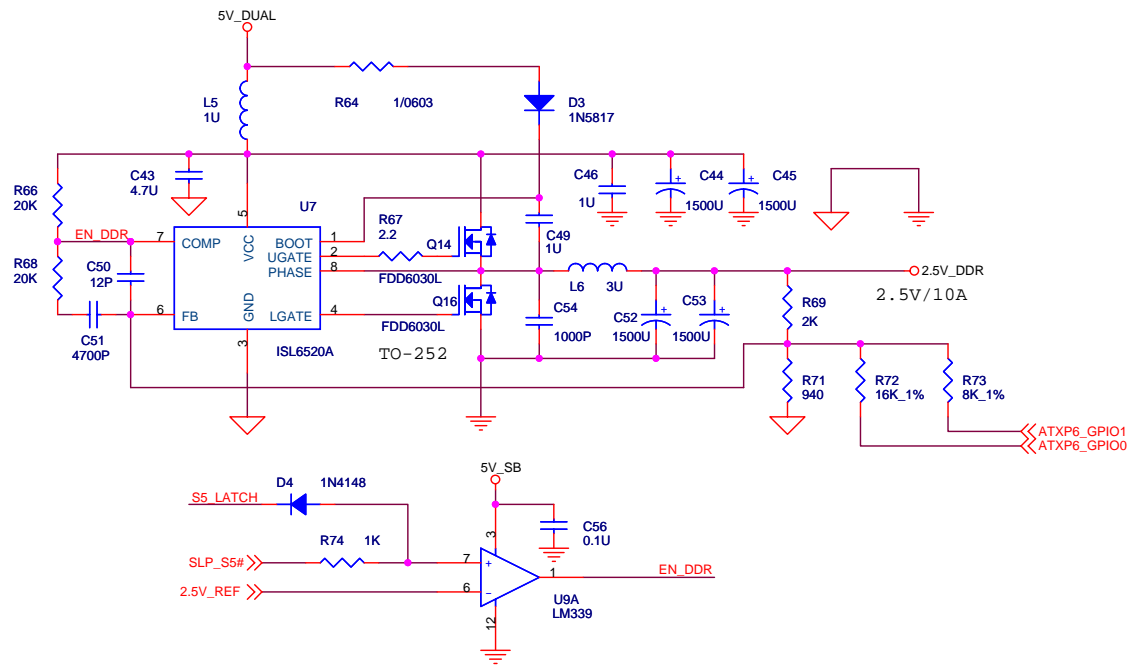
ISL6556B FOR INTEL P4 VRM10 POWER CKT

I current limit = $4 \times (0.095\mu A \times R_{I_SENSE}) / R_{ds_on} (100 \text{ deg C})$

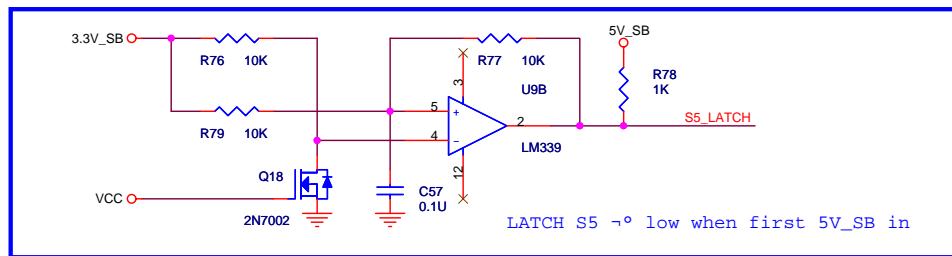
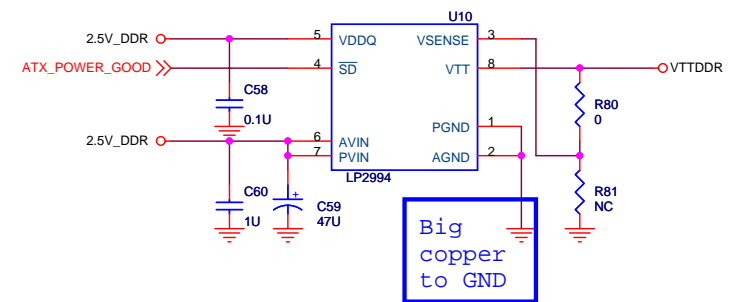
0.8375V~1.6V/90A



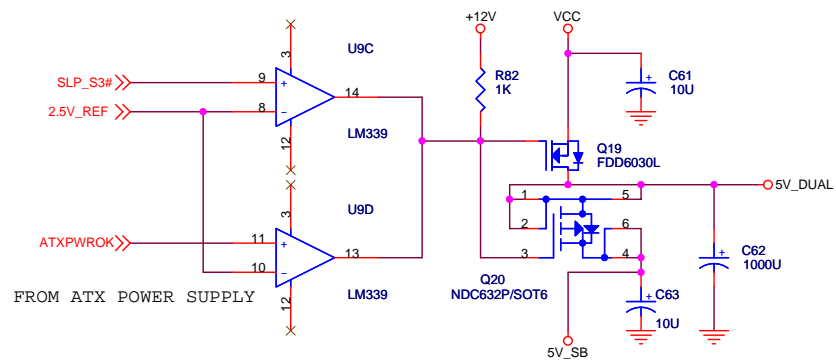
Title		
ISL6556B Springdale power ckt - 3 phase, support Willimette		
Size	Document Number	Rev
	ISL6556B_Springdale_Willimette.DSN	04
Date:	Sunday, January 27, 2008	Sheet 1 of 4



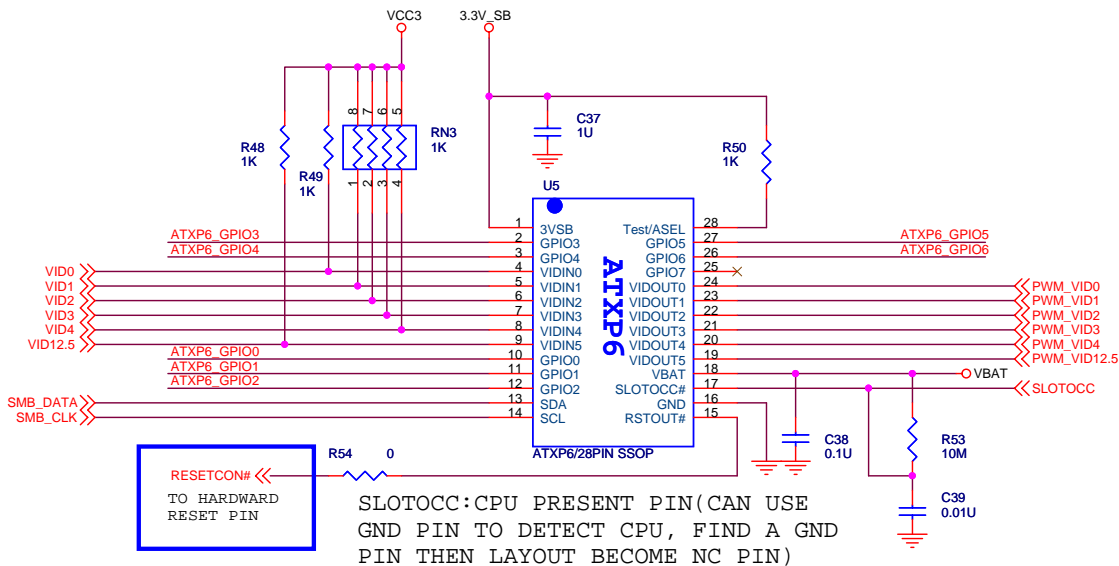
CO-LAYOUT



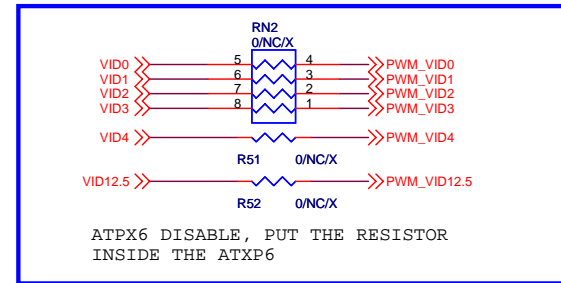
LATCH S5 → low when first 5V_SB in



Title		
ISL6556B Springdale power ckt - 3 phase, support Willimette		
Size	Document Number	Rev
	ISL6556B_Springdale_Willimette.DSN	01
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SLOTOCC: CPU PRESENT PIN (CAN USE GND PIN TO DETECT CPU, FIND A GND PIN THEN LAYOUT BECOME NC PIN)

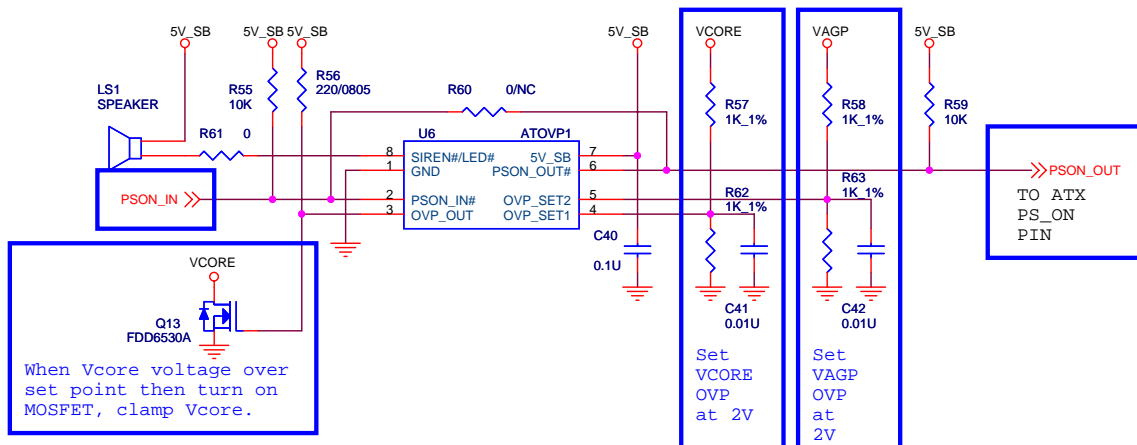


ATXP6 DISABLE, PUT THE RESISTOR INSIDE THE ATXP6

ATXP6_GPIO0	ATXP6_GPIO1	2.5V_DDR
1	1	2.5V
0	1	2.6V
1	0	2.7V
0	0	2.8V

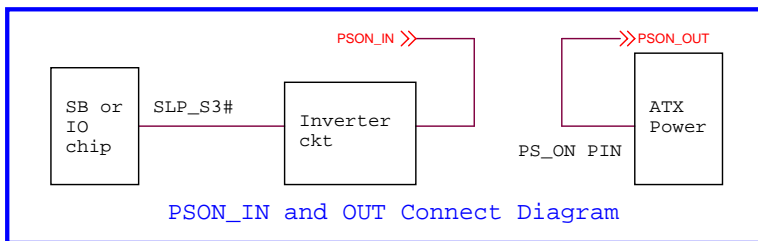
ATXP6_GPIO2	ATXP6_GPIO3	VDD_1.5V
1	1	1.5V
0	1	1.6V
1	0	1.7V
0	0	1.8V

NOTE: 1-OPEN DRAIN, 0-LOW



ATXP6_GPIO4	ATXP6_GPIO5	ATXP6_GPIO6	Vcore+Voffset
1	1	1	1.6V (DEFAULT)
0	1	1	1.625V
1	0	1	1.65V
0	0	1	1.675V
1	1	0	1.7V
0	1	0	1.725V
1	0	0	1.75V
0	0	0	1.775V

NOTE: SET 010101 to PWM_VID (1.6V), then use ATXP6_GPIO4,5,6 to set Vcore to 1.775V
0:LOW 0V
1:OPEN



Title		
ISL6556B Springdale power ckt - 3 phase, support Willimette		
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