

IT8281M

K8 Power Sequence Controller

Preliminary Specification V0.1

INTEGRATED TECHNOLOGY EXPRESS, INC.

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Additional copies of this manual or other ITE literature may be obtained from:

ITE, Inc.
Marketing Department
8F, No. 233-1, Bao Chiao Rd., Hsin Tien,
Taipei County 231, Taiwan, R.O.C.

Phone: (02) 2912-6889
Fax: (02) 2910-2551, 2910-2552

ITE (USA) Inc.
Marketing Department
1235 Midas Way
Sunnyvale, CA 94086
U.S.A.

Phone: (408) 530-8860
Fax: (408) 530-8861

ITE (USA) Inc.
Eastern U.S.A. Sales Office
896 Summit St., #105
Round Rock, TX 78664
U.S.A.

Phone: (512) 388-7880
Fax: (512) 388-3108

If you have any marketing or sales questions, please contact:

Lawrence Liu, at ITE Taiwan: E-mail: lawrence.liu@ite.com.tw, Tel: 886-2-2912-6889 X6071,
Fax: 886-2-26578561

David Lin, at ITE U.S.A.: E-mail: david.lin@iteusa.com, Tel: (408) 530-8860 X238,
Fax: (408) 530-8861

Don Gardenhire, at ITE Eastern USA Office: E-mail: don.gardenhire@iteusa.com
Tel: (512) 388-7880, Fax: (512) 388-3108

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<http://www.iteusa.com>

Or e-mail itesupport@ite.com.tw for more product information/services.

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1. Features

- **K8 Power Sequence Controller**
 - Built-in enhanced voltage comparator
- **System Power-Good Generation**
 - Built-in power-good glue logic
- **Single 5VSB Power Supply**
- **16-pin SOP**

2. General Description

The IT8281M incorporates glue logics for AMD K8 CPU power sequence application and provides the system power-good request.

Outstanding features of this controller IC include special voltage comparators for VLDT, VDDA and VDIMM_STR power detected without the need of any external components. All power-good generation circuits support AMD K8 main board design for saving glue logics cost.

The following figure is the application hint.

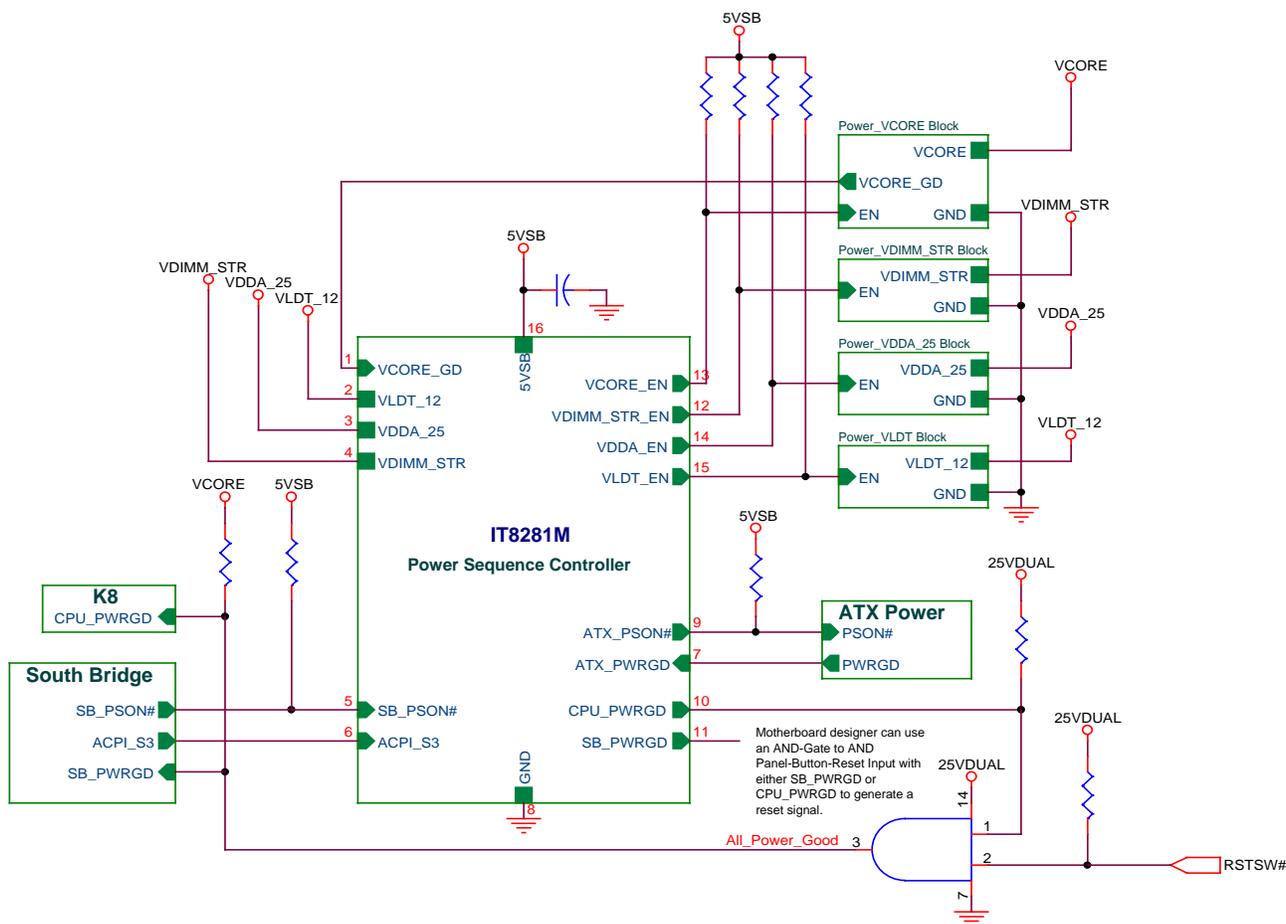
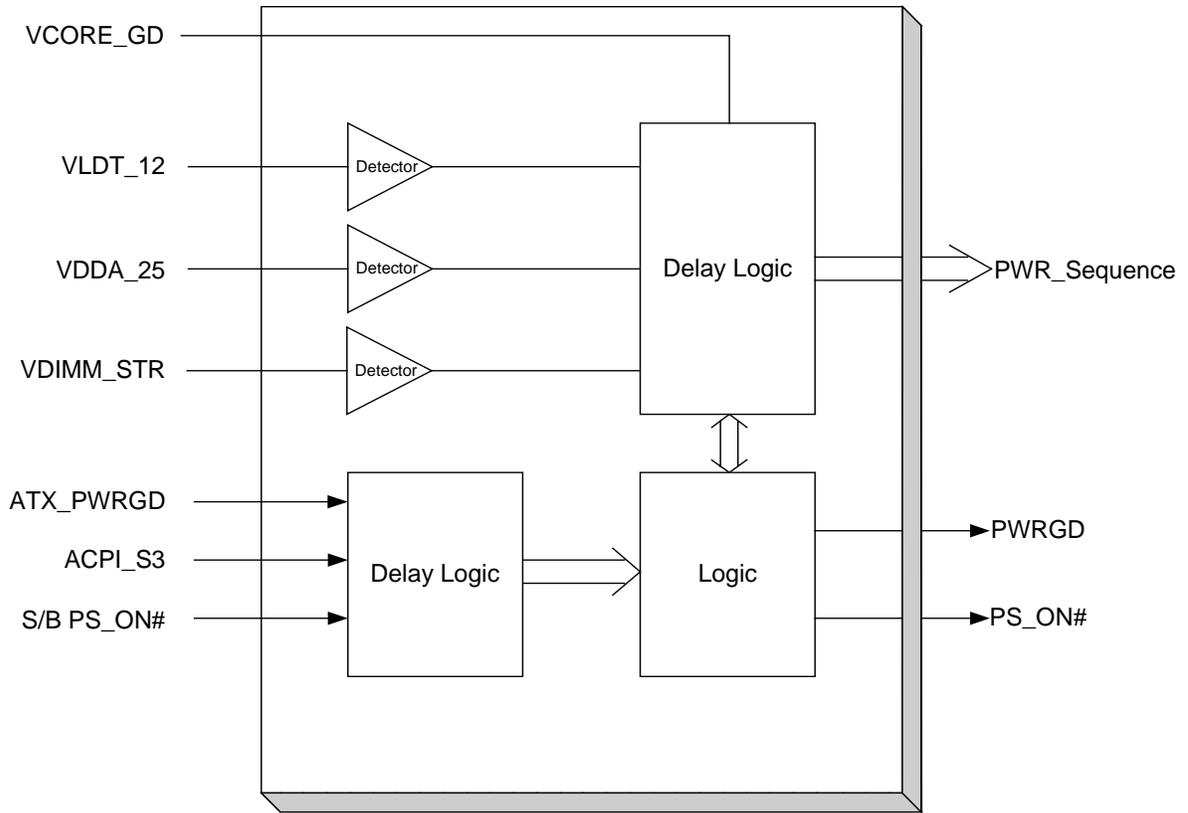


Figure 2-1. Application Circuit

3. Block Diagram



4. Pin Configuration

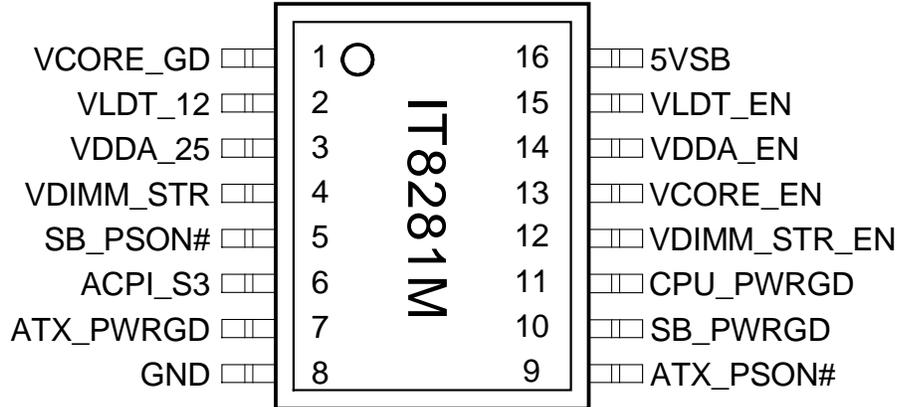


Table 4-1. Pins Listed in Numeric Order

| Pin | Signal | Pin | Signal |
|-----|-----------|-----|--------------|
| 1 | VCORE_GD | 9 | ATX_PSON# |
| 2 | VLDT_12 | 10 | SB_PWRGD |
| 3 | VDDA_25 | 11 | CPU_PWRGD |
| 4 | VDIMM_STR | 12 | VDIMM_STR_EN |
| 5 | SB_PSON# | 13 | VCORE_EN |
| 6 | ACPI_S3 | 14 | VDDA_EN |
| 7 | ATX_PWRGD | 15 | VLDT_EN |
| 8 | GND | 16 | 5VSB |

5. IT8281M Pin Descriptions

Table 5-1. Pin Descriptions of Power Sequence

| Pin(s) No. | Symbol | Attribute | Description |
|------------|--------------|-----------|---|
| 1 | VCORE_GD | DI | VCORE Power-Good. Active high. This pin indicates that the power-good signal from the PWM controller for CPU core voltage. |
| 2 | VLDT_12 | AI | VLDT (1.2V) analog inputs. |
| 3 | VDDA_25 | AI | VDDA (2.5V) analog inputs. |
| 4 | VDIMM_STR | AI | VDIMM DUAL STR (2.5V) analog inputs. |
| 5 | SB_PSON# | DI | South Bridge PSON#. Active low. This signal is connected to the PSON# signal from the south bridge or Super I/O to control the on/off of ATX power supply. |
| 6 | ACPI_S3 | DI | A GPIO pin from S/B. Active high. This pin indicates that the system is in ACPI S3 state. |
| 9 | ATX_PSON# | DOD8 | ATX Power PSON#. Active low. The function of this pin is ATX Power Supply On-Off. |
| 12 | VDIMM_STR_EN | DOD8 | VDIMM STR Enable. Active high. The function of this pin is to enable the PWM for VDIMM_STR dual voltage. |
| 13 | VCORE_EN | DOD8 | VCORE Enable. Active high. The function of this pin is to enable the PWM for CPU VCORE. |
| 14 | VDDA_EN | DOD8 | VDDA Enable. Active high. The function of this pin is to enable the VDDA power for K8 CPU. |
| 15 | VLDT_EN | DOD8 | VLDT Enable. Active high. The function of this pin is to enable the VLDT voltage. |

Table 5-2. Pin Descriptions of Power-Good Generation

| Pin(s) No. | Symbol | Attribute | Description |
|------------|-----------|-----------|--|
| 7 | ATX_PWRGD | DI | ATX Power-Good. Active high. Input indicates that ATX power supply power-good is ready. |
| 10 | SB_PWRGD | DOD8 | South Bridge Power-Good. Active high. Output indicates that the south bridge power-good is ready. |
| 11 | CPU_PWRGD | DOD8 | CPU Power-Good. Active high. Output indicates that CPU power-good is ready. |

Table 5-3. Pin Descriptions of Power/Ground Signals

| Pin(s) No. | Symbol | Attribute | Description |
|------------|--------|-----------|---------------------------------|
| 8 | GND | PWR | Ground |
| 16 | 5VSB | PWR | +5V Standby Power Supply |

IO Cell:

DOD8: 8mA Digital Open-Drain Output buffer

AI: Analog input

DI: Digital Input

6. DC Characteristics (VCC = 5.0V±5%. Ta=0°C to 70°C)

Absolute Maximum Ratings

| | |
|--------------------------------------|---------------------|
| Power Supply (V _{CC})..... | -0.5V to 7.0V |
| Input Voltage..... | -0.5V to VCC + 0.5V |
| Output Voltage..... | -0.5V to VCC + 0.5V |
| Storage Temperature..... | -55°C to 125°C |

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=5V ± 5%, Ta = 0°C to + 70°C)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------------------------|---|----------------------|------|------|------|------|
| AI Type Buffer | | | | | | |
| V _{trig} | Trigger point for VDDA_25 and VDIMM_STR | VCC=5V | - | 2.25 | - | V |
| V _{trig} | Trigger point for VLDT_12 | VCC=5V | - | 1.0 | - | V |
| DOD8 Type Buffer | | | | | | |
| V _{OL} | Output Low Voltage | I _{OL} =8mA | - | - | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} =8mA | 2.4 | - | - | V |
| DIOD8 Type Buffer | | | | | | |
| V _{IL} | Input Low Voltage | | - | - | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.2 | - | - | V |
| V _{OL} | Output Low Voltage | I _{OL} =8mA | - | - | 0.4 | V |
| I _{IL} | Low Input Leakage current | V _{IN} =0 | - | 10 | | uA |
| I _{IH} | High Input Leakage current | V _{IN} =VCC | - | - | -10 | uA |
| I _{OZ} | Tri-state leakage current | | - | - | 20 | uA |
| DI Type Buffer | | | | | | |
| V _{IL} | Input Low Voltage | | - | - | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.2 | - | - | V |
| I _{IL} | Input Leakage current | V _{IN} =0 | - | 10 | - | uA |
| I _{IH} | High Input Leakage current | V _{IN} =VCC | - | - | -10 | uA |

7. AC Characteristics

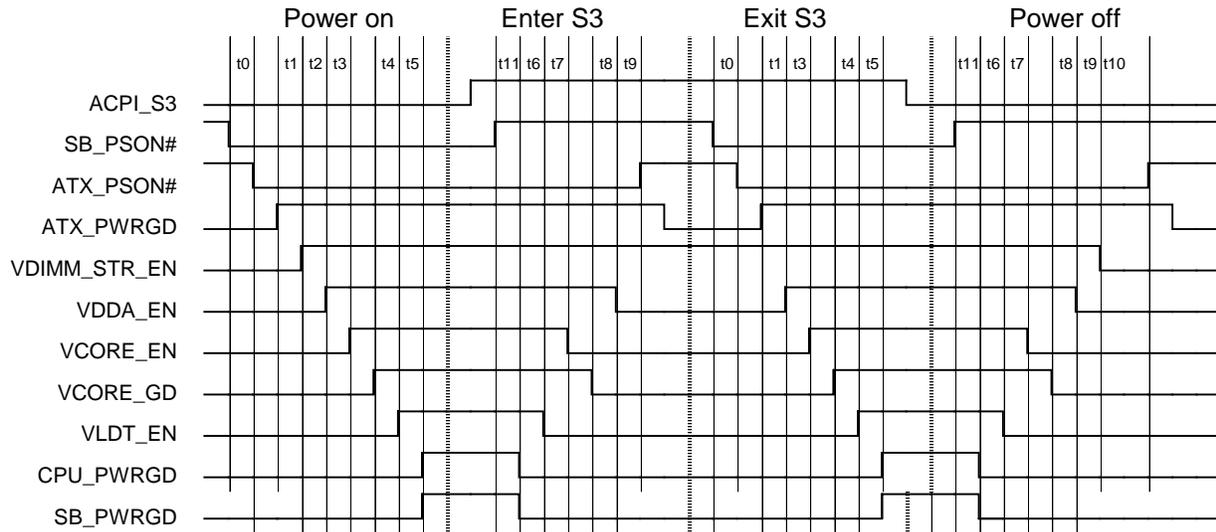


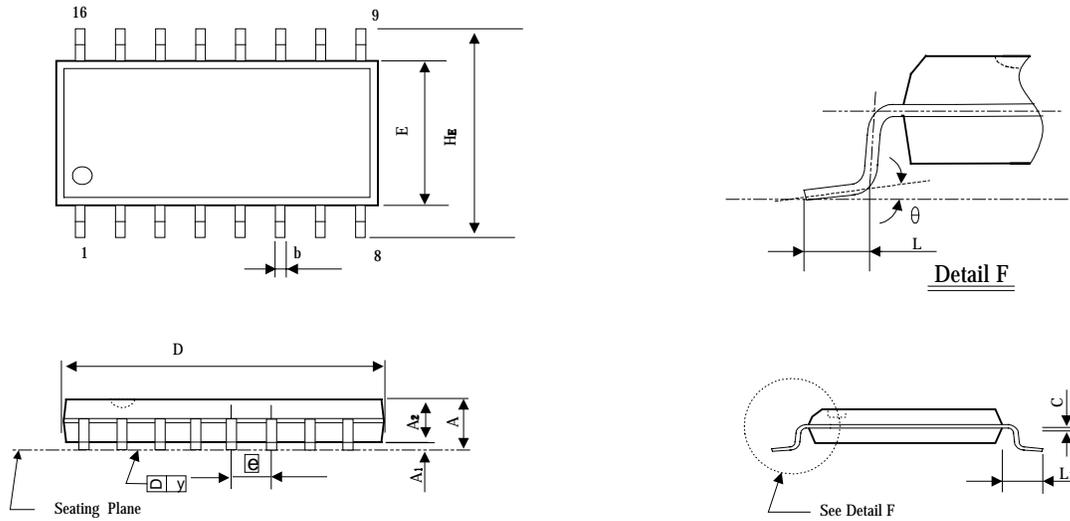
Table 7-1. AC Timing Parameter

| Item | Max | Typ | Min | Description |
|------|----------------------|------|------|---|
| t0 | | 1us | 0 | The falling edge of SB_PSON# to the assertion of ATX_PSON#. |
| t1 | | 50us | | The rising edge of ATX_PWRGD to the assertion of VDIMM_STR_EN |
| t2 | 50us + t_vdimm_gd | | 50us | The assertion of VDIMM_STR_EN to the assertion of VDDA_EN. The t_vdimm_gd is the rise time of the VDIMM_STR_EN voltage from 0V to 2.25V. |
| t3 | 50us + t_vdda_gd | | 50us | The assertion of VDDA_EN to the assertion of VCORE_EN. The t_vdda_gd is the rise time of the VDDA voltage from 0V to 2.25V. |
| t4 | | 50us | | The rising edge of VCORE_GD to the assertion of VLDT_EN. |
| t5 | 50us + t_vldt_gd | | 50us | The assertion of VLDT_EN to the assertion of CPU_PWRGD and SB_PWRGD. The t_vldt_gd is the rise time of the vldt voltage from 0V to 1.0V. |
| t6 | | 50us | | The de-assertion of CPU_PWRGD and SB_PWRGD to the de-assertion of VLDT_EN. |
| t7 | | 10ms | | The de-assertion of VLDT_EN to the de-assertion of VCORE_EN. |
| t8 | | 10ms | | The falling edge of VCORE_GD to the de-assertion of VDDA_EN. |
| t9 | | 10ms | | The de-assertion of VDDA_EN to the de-assertion of VDIMM_STR_EN or ATX_PSON#. |
| t10 | | 50ms | | The de-assertion of VDIMM_STR_EN to the de-assertion of ATX_PSON#. |
| t11 | | 50us | | The rising edge of SB_PSON# to the de-assertion of CPU_PWRGD and SB_PWRGD. |

8. Package Information

SOP16L Outline Dimensions

unit: inches/mm



| Symbol | Dimension in inches | | | Dimension in mm | | |
|----------|---------------------|-------|-------|-----------------|------|-------|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.053 | 0.064 | 0.069 | 1.35 | 1.63 | 1.75 |
| A1 | 0.004 | 0.006 | 0.010 | 0.10 | 0.15 | 0.25 |
| A2 | 0.051 | 0.055 | 0.059 | 1.30 | 1.40 | 1.50 |
| b | 0.013 | 0.016 | 0.020 | 0.33 | 0.41 | 0.51 |
| C | 0.007 | - | 0.010 | 0.19 | - | 0.25 |
| D | 0.386 | 0.390 | 0.394 | 9.80 | 9.91 | 10.01 |
| E | 0.150 | 0.154 | 0.157 | 3.80 | 3.90 | 4.00 |
| e | 0.050BSC | | | 1.27BSC | | |
| HE | 0.228 | 0.236 | 0.244 | 5.80 | 6.00 | 6.20 |
| L | 0.016 | 0.025 | 0.050 | 0.40 | 0.64 | 1.27 |
| L1 | 0.042REF. | | | 1.07REF. | | |
| y | - | - | 0.004 | - | - | 0.10 |
| θ | 0° | - | 8° | 0° | - | 8° |

9. Ordering Information

| Part No. | Package |
|----------|---------|
| IT8281M | 16 SOP |