First International Computer,Inc

Protable Computer Group HW Department

Board name : Mother Board Schematic

Project : MB02

Version : 0.2A

Initial Date : September/20 2002

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Manager Sign by : Eric_Yang

Drawing by : Steven Hsu

Total confirm by :Adam Cho

LAN Circuit check by : Vivian Chen

Audio Circuit check by : Annie Wang

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7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

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1. Schematic Page Description :

Carmel (FIC MB02) Schematic Ver : 0.2A

1. TITLE
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43. DCIN
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45. BATTERY SELECT
46. CHARGE CIRCUIT
47. Battery Voltage Sense
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50. Power (3VDDM / 5VDDM)
51. AC97 CODEC(ALC202)
52. CD SOUND & MICIN
53. AUDIO POWER
54. AMP TPA2020
55. DIP SW & LID SW
56. MDC/Blue Tooth CNN
57. Calexico MINI PCI

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI Wireless LAN
AD23	R5C551(1394&CardBus)
AD24	ICH4-M Embeded Lan/ Intel 82540EM

PCIINT	CHIP
IRQA	MiniPCI / CardBus
IRQB	MiniPCI / / IEEE1394/ AC97
IRQC	Intel 82540EM
IRQD	ICH4-M Embeded USB2.0

BUSMASTER

REQ	CHIP
REQ0 / GNT0	Mini PCI Lan
REQ1 / GNT1	R5C551(1394&CardBus)
REQ2 / GNT2	Mini PCI Modem
REQ3 / GNT3	
REQ4 / GNT4	Intel 82540EM

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	FLOPPY DISK
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

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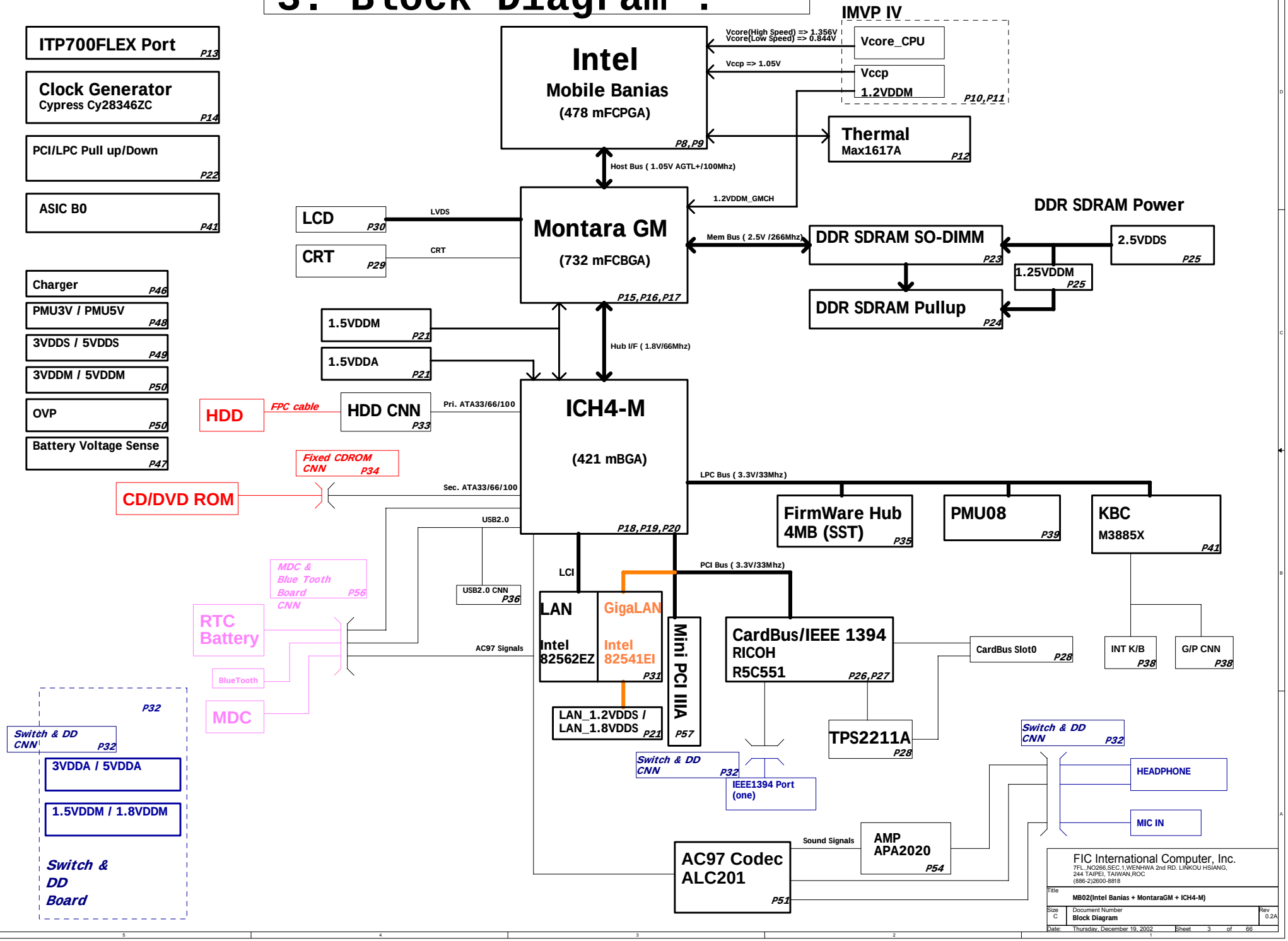
3. Block Diagram :



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244 TAIPEI, TAIWAN,ROC
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4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
3VDDA	3V always on power rail by DCON from PMU08
5VDDA	5V always on power rail by DCON from PMU08
1.5VDDA	1.5V always on power rail from 3VDDA
3VDDS	3V switched power rail by PSUSC0, and exist at STR
5VDDS	5V switched power rail by PSUSC0, and exist at STR
2.5VDDS	2.5V power rail controlled by PSUSC0, and exist at STR
1.5VDDS	1.5V power rail controlled by PSUSC0, and exist at STR
LAN_1.2VDDS	1.2V power rail from 3VDDS by LDO, and exist at STR
LAN 1.8VDDS	1.8V power rail from 3VDDS by LDO, and exist at STR
12VDDM	12V power rail controlled by SUSTAT_B0
3VDDM	3.3V switched power rail by SUSTAT_B0
5VDDM	5.0V switched power rail by SUSTAT_B0
2.5VDDM	2.5V switched power rail by SUSTAT_B0
1.5VDDM	1.5V switched power rail by SUSTAT_B0
1.8VDDM	1.8V power rail controlled by SUSTAT_B0
VCCP	0.9V-1.105V power rail for CPU controlled by SYS_PWROK
Vcore_CPU	0.7V~1.708V power rail for CPU controlled by VR_ON
1.2VDDM	1.2V power rail controlled by SYS_PWROK

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal

Signal Conditioning

_D_	=	Damped (by a resistor)
_Q_	=	Isolated (by a Q-switch)
_L_	=	Filtered (by an inductor or bead)

5.Board Stack up Description :

PCB Layers

Trace Impedence: 55ohm+_15%

Copper	Trace Width	Layer No	Dielectric	Layer Type	Layer Signals	Thickness
1/2oz	5mil	Layer 1		TOP(MicroStrip)		0.7mil
			(2116)4mil			4mil
1oz		Layer 2		GND		1.4mil
			(1506)6mil			6mil
1oz	4mil	Layer 3		IN1(StripLine)(High Speed)	AGTL+, CLK, SDRAM, HUB_LINK, LVDS,	1.4mil
			(1506)6mil			6mil
1oz	4mil	Layer 4		IN2(StripLine)(High Speed)	USB2.0, FWH, AC97	1.4mil
			(1506)6mil			6mil
1oz		Layer 5		GND		1.4mil
			(1506)6mil			6mil
1oz	4mil	Layer 6		IN3(StripLine)(Others)	PCI, IDE	1.4mil
			(1506)6mil			6mil
1oz		Layer 7		VCC		1.4mil
			(2116)4mil			4mil
1/2oz	5mil	Layer 8		BOTTOM(MicroStrip)		0.7mil
						1.214mm

POWER RAIL	DESTINATION	VOLTAGE	S0 CURRENT
VCORE_CPU	Banias	0.7-1.708V	32A
VCCP	Banias	0.9-1.105V	2.5A
	MontaraGM		0.72A
1.8VDDM	Banias (PLL)	1.8V	0.3A
	ICH4M (PLL)		0.099A
1.2VDDM	MontaraGM	1.2V	1.89A
	(CORE, HUB, DDRDDL)		(1.4A, 0.09A, 0.4A)
1.5VDDM	MontaraGM	1.5V	0.23A
	(LVDS, DAC, DVO)		(0.07A, 0.07A, 0.09A)
	ICH4M (CORE)		0.5A
2.5VDDS	MontaraGM	2.5V	2.12A
	(DDR, LVDSIO)		(2.07A, 0.05A)
	DDR RAM		1.046A(Idle) 1.692A (Run 3DMark)
	R5C551		0.13A
1.8VDDS	82541EI		0.22A
1.25VDDM	DDR RAM	1.25V	0.0769A
1.5VDDS	ICH4M (LAN)	1.5V	0.0155A
1.2VDDS	82541EI	1.2V	0.47A
1.5VDDA	ICH4M (SUS)	1.5V	0.0675A
3VDDM	ICH4M (IO)	3.3V	0.528A
	R5C551		0.13A
	MiniPCI		
	FWH BIOS		
	LPC KBC		0.0308A (Idle)
	AC97 CODEC		0.0461A (Idle)
	CLK GEN		0.36A
	LVDS		0.246A
3VDDS	ICH4M (LAN)	3.3V	0.0092A
	R5C551		
	MiniPCI		
	82540EM		0.15A
	PCMCIA VCCA		
3VDDA	ICH4M (SUS)	3.3V	0.165A
5VDDM	AMP2020		0.0615A (Idle) 0.338A (Run)
	CDROM		0.0461A (Idle) 0.677~0.8A(Run)
	HDD		0.0461A (Idle) 0.492A (Run)
	INT KB/ INT MS		
	INVERTER		0.0615A (Idle) 0.569A (Run)
5VDDS	PCMCIA VCCA		
5VDDA	ICH4M		10UA
	USB		
PMU3V	PMU08		0.0615A
PMU5V	ASIC_B0		0.0615A

VCORE_CPU	highest frequency mode	1.356V
	lowest frequency mode	0.844V
	deeper sleep	0.748V

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6.Schematic modify Item and History :

Modify item description

Version B change to Version C

1. In GMCH, For easy layout, we can put high. HUB_PSWING and HUB_HLVREF to 1.2VDDM and fine tune resistors.
2. Decoupling Capacitors C206, C207, C215, C216. Please use X5R to instead of Y5V.
3. Using 0 ohm to connect PCI_RST0 and BUFF_PCIRST0 and unmount U15, U16.
4. Using S4 to instead of DC_SLP_S50 to control Power switch
5. change Q21 SI3442 to AO4402
6. Provide PCMCIA Card List
7. Stuff C455 and C456
8. Provide MDC daughter board schematic
9. Vcore PWR U2 pin9, connect VRON_VCCP instead of VR_ON.
10. Add ITP700FLEX Port

Version C change to Version D

1. Mother Board and DD board join to one PCB board.
2. P.6 Add Timing of Adaptor & Battery only power on and S4 resume.
3. P.7 Add Switch setting.
4. P.7 Add DDR layout Command Signal Topology1.
5. P.8 R102 change size.
6. P.9 Bypass Caps. Change to Option2(NT80) from Option4(NT130)/ Option5(NT100). Because this will save more money.
7. P.9 U1 pinB1,N1,AC26 add 0 ohm to update Banias verB0.
8. P.9 modify FAN_PWM only from FIC_ASIC.
9. P.10 Max1987 pin 49 add to GND
10. P.10 Max1987 pin16 modify resistor to 2.7kΩ.
11. P.11 Change PWM controller from MAX1715($1.45) to MAX1845($1.25).
12. P.11 Max1845 pin 28 & pin 16 connection to pin 27 & pin 17.
13. P.11.Max1845 pin output VCCP & 1.2VDDM add serial 20 mΩ.
14. P.11 max1845 pin 8 add 0Ω to GND.
15. P.11 Max1845 pin2 modify resistor value.
16. P.12 Delete THRM_PROCHOT0 circuit to ICH4.
17. P.14 Combine U11(AND logic) to FIC_ASIC.
18. P.14 Change U70 from SMBus to Hardware strap setting
19. P.14 Combine U10 pin37 to 3VDDM_CLKSTRAP and delete some Bypass Caps.
20. P.15 Delete BDG_PILOT0 and BDG_RCOMP2 unmount circuit.
21. P.17 Montara 1.2VDDM_GMCH 150uF change to NU.
22. P.17 Montara connection pin A6 &B16 220uF change to NU.
23. P.18 Modify U13 pin M23, R22 HUB_VREF and HUB_VSWING circuit.
24. P.19 Simplify SYS_PWROK circuit.
25. P.19 Add D87 to reduce RTC_VCC voltage.
26. P.19 Delete U17.
27. P.19 Add Net CDROM_OFF0 & IDEQEN0.
28. P.20 Simplify VCCLAN1.5 and VCCLAN3.3 power source.
29. P.21 U77 from MAX8888($0.8) change to SI9182($0.3). and Delete 1.5VDDS power good circuit.
30. P.21 Simplify SUSTAT_B0 to SUSTATB to control 1.5VDDM.
31. P.23 Change DDR Connector to support separable MAA bus. And use Command Signal Topology1 to layout.
32. P.25 DDR power ,DDR2.5V &DDR1.25V PWM IC change from MAX1714 ($1.5) and MAX1809 ($0.9) to ISL6225 ($1.2).
33. P.26 Delete C645, C646, C647, C648, C649.
34. P.27 Delete C439.
35. P.28 Remove 12VDDM from U29 pin9.
36. P.29 Modify HSYNC and VSYNC circuit.
37. P.29 Modify CRT5VS output capacity quantity (delete C450).
38. P.30 Modify pin out of CN2.
39. P.30 LED_G with LED_A 0Ω cancel
40. P.31 change R431, R436, R441, R446 to C854, C855, C856, C857.
41. P.31 Add C858, C859, C860, C861 and R1087.
42. P.32 Modify pin out of CN12 and cancel all of 12V voltage and modify all of correlate component.
43. P.33 Cancel HDD connector input fuse(F6) and Capacitor(C500).
44. P.34 Add CD_ROM can power off on O.S not used.
45. P.35 Modify FWH 3VDDM input capacity quantity and add PLCC 32 pin socket for easy debug.
46. P.37 Modify K/B pin 24 reserve pull high for ENE LPC K/B control.
47. P.38 Cancel Glide Pad 5VDDM serial 10Ω.
48. P.38 Modify INT KB Connector pin out.
49. P.39 cancel PMU08 flash component.
50. P.40 Delete Q43 and connect IDE_RST0 to PCI_RST0.
51. P.41 To use FIC ASIC to reduce logic components including of U45, Q44, U11.
52. P.42 Modify adaptor connector EMI and ESD solution.
53. P.44 Modify Batt connector pin2 to EPROM VCC change to PMU3V.
54. P.44, P46 Modify Batt connector pin1 for battery 6 cell or 8 cell select
55. P.46 cancel second battery select circuit.
56. P.48 Modify battery only power on circuit.
57. P.49 Simplify 3VDDS and 5VDDS power circuit.
58. P.50 Cancel over voltage protect circuit.
59. P.50 Simplify 3VDDM and 5VDDM power circuit.
60. P.51 Add R188, R189, C156, R186, R187 for supporting ALC202 codec.
61. P.53 Delete U60 to save layout space.
62. P.53 Modify AMP_MUTE and AMP_SD circuit.
63. P.54 Cancel SPDIF feature and modify with SPDIF correlate pin.
64. P.55 Modify Dip switch to move KBSEL1 and KBSEL2 to DD board and move LID switch to DD board.
65. P.21 Add GigaLAN 82541EI power source(LAN_1.2VDDS, LAN_1.8VDDS).
66. P.31 Modify to match GigaLAN 82541EI circuit and add R1096.
67. P.26 Modify U26 pinE1 to add SB_GPIO25 to control and delete R992
68. P.29 Return HSYNC and VSYNC circuit back, because 1.5V is hard to open 2N7002
69. P.35 R511,R512,R513,R514,R515 from 10Kohm to 100ohm(Intel recommend).
70. P.28 Add C869 at CN5 pin58 to reduce noise.
71. P.9 Change Option2 to Option5.
72. P.26 Add R1117 and C905 to delay PCIREST to meet spec.
73. P.14 Add R1116 to make SSCLK frequency selection which sets 48M or 66M.
74. P.15, P.23, P.24 Del R319, RP74, R357, R347 and disconnect CLK2 and CLK5 to meet No ECC signals spec.
75. P.23, P.24 Change Topology1 to Topology2 at DDR command signals
76. P.41 Disconnect U46 pin94 and pin93.
77. P.40 Unmount Q42 and R599.
78. P.29 Change D75 from 2A component to 1A component.
79. P.56, P.37, P.19, P.30 modify Blue tooth signals.
80. P.9 Change C27 from 150UF to 100UF.
81. P.11 Add R37, R74, R77, R78, C70, C71.
82. P.17 Change value of C192, C193, C230, C203.
83. P.45 Add R1118 to protect Q51.
84. P.32 Connector Pin25 from 5VDDM change to 5VDDS; Pin20 NU.
85. P.62 Connector Pin25 from D5VDDM change to D5VDDS; Pin20 NU.
86. P.56 Add Tri-State Buffer on coexistence signals.
87. P.30 For easy layout, we change the pins of CN2
88. P.23, P.24 For easy layout, we modify series resistors and pull high resistors.

Version 0.1 change to 0.2

1. Page17,33 Not stuff C312, C669
2. Page50 R372 changes from 4.7Kohm to 1Kohm
3. Page21 Q10 pin 2 connect to 1.5VDDM from Q10 pin4.
4. Page30 Not stuff R28, R27, R26, R25, R24, R23, R22, R21 and stuff R301, R302, R303, R304, R305, R306, R307, R308.
5. Page51 Not stuff R575
6. Page10 Not stuff C443, and change R169 to 470ohm, R172 to 3.75Kohm.
7. Page13 Delete ITP700FLEX.
8. Page25 U30 power source from 5VDDM to 5VDDS and unmount C603, C590.
9. Page56 Add R809 at AC97_BITCLK before CN15
10. Page12 Add R810 between OVER_TEMP0 and delete R528
11. Page37 Add Test Pointer(CN44) for PS2 KB/MS interface.
12. Page19 Delete D30 to keep RTC_VCC at 3V~3.3V
13. Page30 Delete Q22 and R323 to change RFON from Active High to Active LOW
14. Page11 Add D59, U47, U48, R811, C674, C673, R812 circuit to create VR_ON signal and clarify when SYS_PWROK assert, PCICLK and 1.5VDDM is stable over 3ms for test.
15. Page55,32,19 Add CRISIS0 Signal to provide BIOS to recover the destroy.
16. Page10,62 L11, L12, DSW4 dual layout change to single layout.
17. Page46 R768 change to 51Kohm and cancel R247
18. Page11 Change R191 and R173 to 68Kohm and stuff C60 and C78 and F2 change to 3A fuse
19. Change Vendor source at C331, C25, C510, C387, C431, C168, C221, C332, C605, C604, C63, C79, C80, DC32, DC33, DC34, DC35, DC24, DC25.
20. Page64 DR13 change to 33Kohm, and DR19 change to 47Kohm, and unmount DC27.
21. Page63 DR32 change to 0 ohm and unmount DR31, DR3, DR2, DC7, DC8, DR6, DR5.
22. Change DC37, DC38, DC39, DC36, DC41, DC21, DC22 to 4.7uF/X5R
23. Page63 Cancel DC43 and only use DC42 at DUP, and DD11 change to RB751, and DC42, DC55 change to 0.1uF 50V, and DR9 change to 1Kohm, and DD13 change to ISS355, and DR7, DR4 change to 0ohm, and DC5, DC6 change to 0.1uF/X7R/0805 to fine tune 3VDDA/5VDDA.
24. Page54 R482, R493 change to 10Kohm to fine turn audio amplifier.

BUG LIST:

ROOT CAUSE	SOLUTION	PHASE IN PLAN

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244 TAIPEI, TAIWAN,ROC
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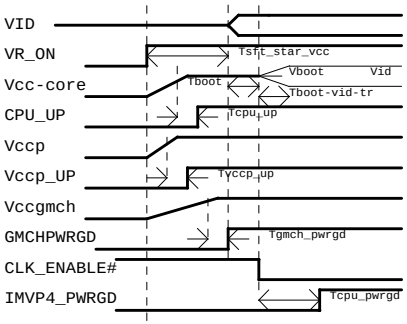
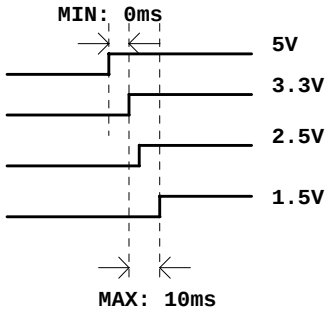
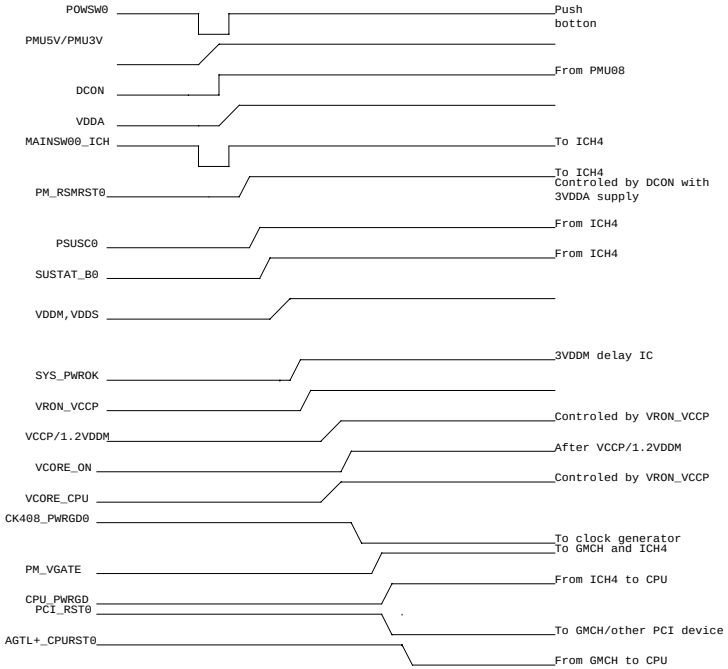
Power On Sequencing Timing Diagram

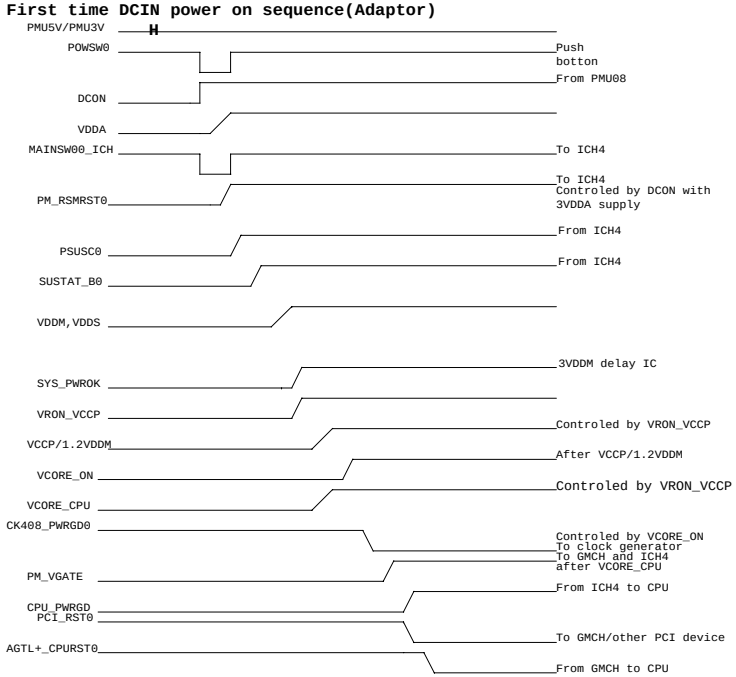




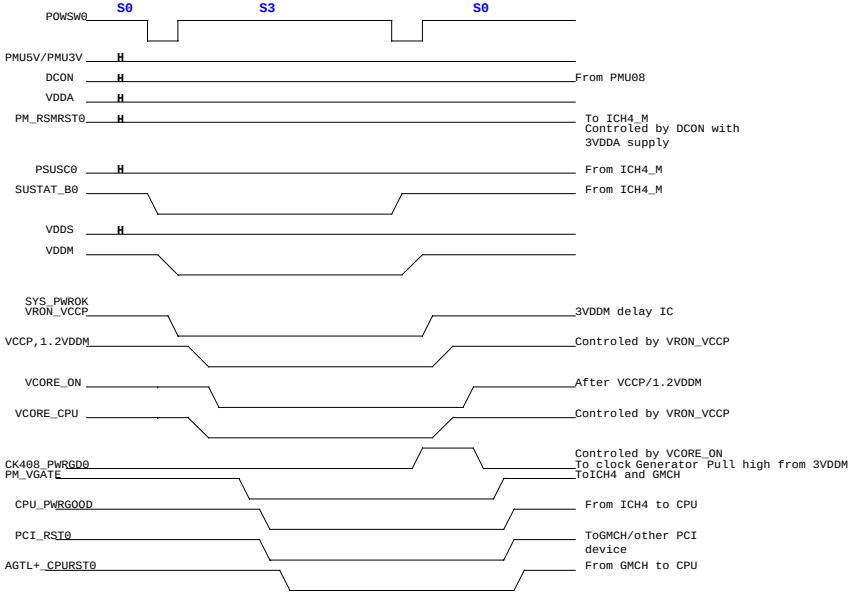
BATTERY ONLY POWER ON TIMING



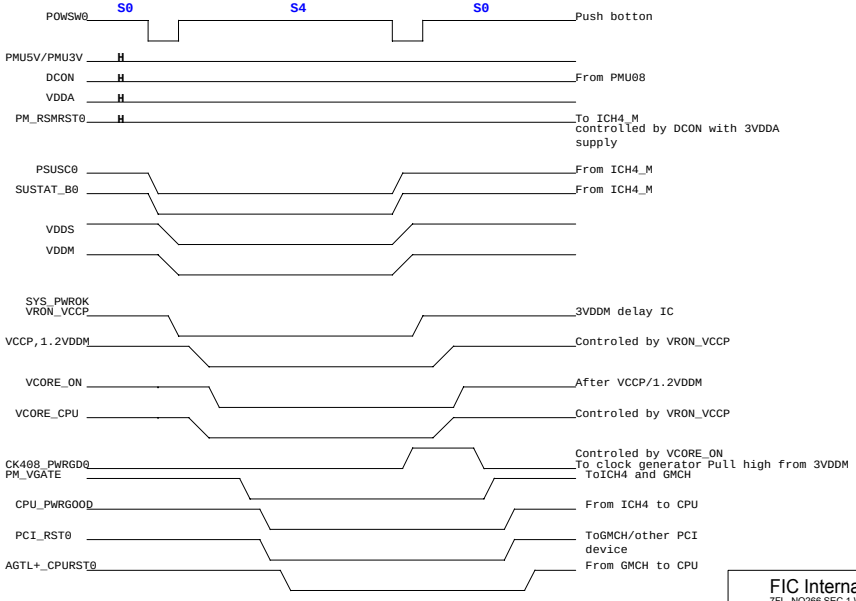
First time DCIN power on sequence(Adaptor)



MB02 S3 SUSPEND AND RESUME TIMING



MB02 S4 SUSPEND AND RESUME TIMING



FIC International Computer, Inc.
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244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

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8. Layout Guideline :

Montara-GM DDR Layout Guidelines

Note that all length matching formulas are based on GMCH die-pad to SO-DIMM pin total length

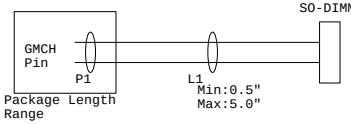
DDR Signal Groups

Group	Signal Name
Clocks	SCK[5:0] SCK#[5:0]
Data	SDQ[71:0] SDQS[8:0] SDM[8:0]
Control	SCKE[3:0] SCS#[3:0]
Command	SMA[12:6,3:0] SBA[1:0] SRAS# SCAS# SWE#
CPC	SMA[5,4,2,1] SMAB[5,4,2,1]
Feedback	RCVENOUT# RCVENIN#

Length Matching Formulas

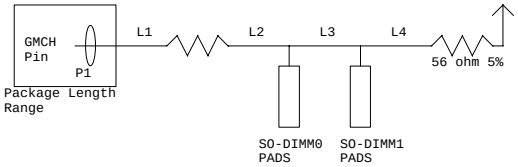
Signal Group	Minimum Length	Maximum Length
Control to Clock	Clock - 1.0"	Clock + 0.5"
Command to Clock	Clock - 1.0"	Clock + 2.0"
CPC to Clock	Clock - 1.0"	Clock + 0.5"
Strobe to Clock	Clock - 1.0"	Clock + 0.5"
Data to Strobe	Strobe - 25 mils	Strobe + 25 mils

Clock Signals Topologies and Routing Guidelines



7 mil trace, 4 mil pair space
Clock length tolerehve within the pair : +/- 10 mil
Clock to Clock Length Matching : +/- 25 mils
Minimum Pair to Pair Spacing : 20 mils
Minimum Spacing to other Signals : 20 mils

Data Signals Topologies and Routing Guidelines

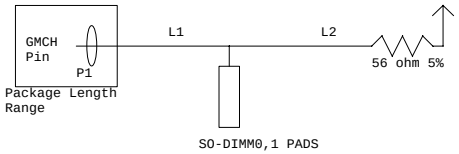


Minimun Spacing to Trace Width Ratio, SDQ/SDM : 2 to 1
SDQS : 3 to1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5", Max 3.75"
L2 : Max 0.75"
L3 : Min 0.25" , Max 1.0"
L4 : Max 1.0"
Length Matching : SDQS to SCK/SCK#
SDQS , SODIMM0 P1+L1+L2
SDQS , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" Max : Clock + 0.5"
SDQ/SDM to SDQS : +/-'25 mils

SDQ/SDM to SDQS Mapping

Signal	Mask	Relative To	Mismatching
SDQ[7..0]	SDM[0]	SDQS[0]	+/- 25 mil
SDQ[15..8]	SDM[1]	SDQS[1]	+/- 25 mil
SDQ[23..16]	SDM[2]	SDQS[2]	+/- 25 mil
SDQ[31..24]	SDM[3]	SDQS[3]	+/- 25 mil
SDQ[39..32]	SDM[4]	SDQS[4]	+/- 25 mil
SDQ[56..40]	SDM[5]	SDQS[5]	+/- 25 mil
SDQ[55..48]	SDM[6]	SDQS[6]	+/- 25 mil
SDQ[63..56]	SDM[7]	SDQS[7]	+/- 25 mil
SDQ[71..64]	SDM[8]	SDQS[8]	+/- 25 mil

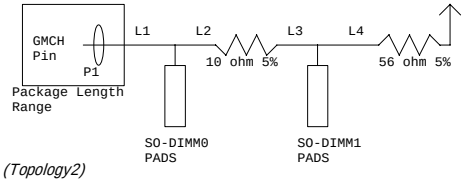
Control Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CTRL(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

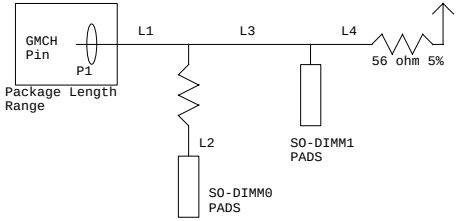
Command Signals Topologies and Routing Guidelines

(Topology1)



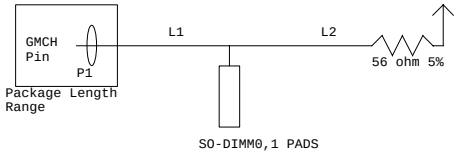
Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1.5"
L3 : Max 1.5"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1
CMD , SODIMM1 P1+L1+L2+L3
Min : Clock - 1.0" , Max : Clock + 2.0"

(Topology2)



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 4.0"
L2 : Max 1"
L3 : Max 2"
L2+L3 : Max 3.0"
L4 : Max 1.0"
Length Matching : CMD to SCK/SCK#
CMD , SODIMM0 P1+L1+L2
CMD , SODIMM1 P1+L1+L3
Min : Clock - 1.0" , Max : Clock + 2.0"
10 ohm 5%

CPC Signals Topologies and Routing Guidelines



Trace spacing to trace width ratio : 2 to 1
Minimum Spacing to other Signals : 20 mils
Trace Length L1 : Min 0.5" , Max 5.5"
L2 : Max 2.0"
Length Matching : CPC(P1+L1) to SCK/SCK#
Min : Clock - 1.0" , Max : Clock + 0.5"

9. Switch Setting :

SW1 on Mother Board

SW1 setting Pin1

SW1-1	DVDSEL
OFF	CDROM enable
ON	DVDROM enable

SW1 setting Pin2

SW1-2	CMOS CLEAR
OFF	NORMAL
ON	CLEAR

DSW1 on DD Board

DSW1 setting Pin1& Pin2

SW1-1	SW1-2	Keyboard Select
OFF	OFF	US Keyboard
OFF	ON	Reverse
ON	OFF	JP Keyboard
ON	ON	UK Keyboard

DSW1 setting Pin4

SW1-2	BIOS Crisis
OFF	NORMAL
ON	Enable

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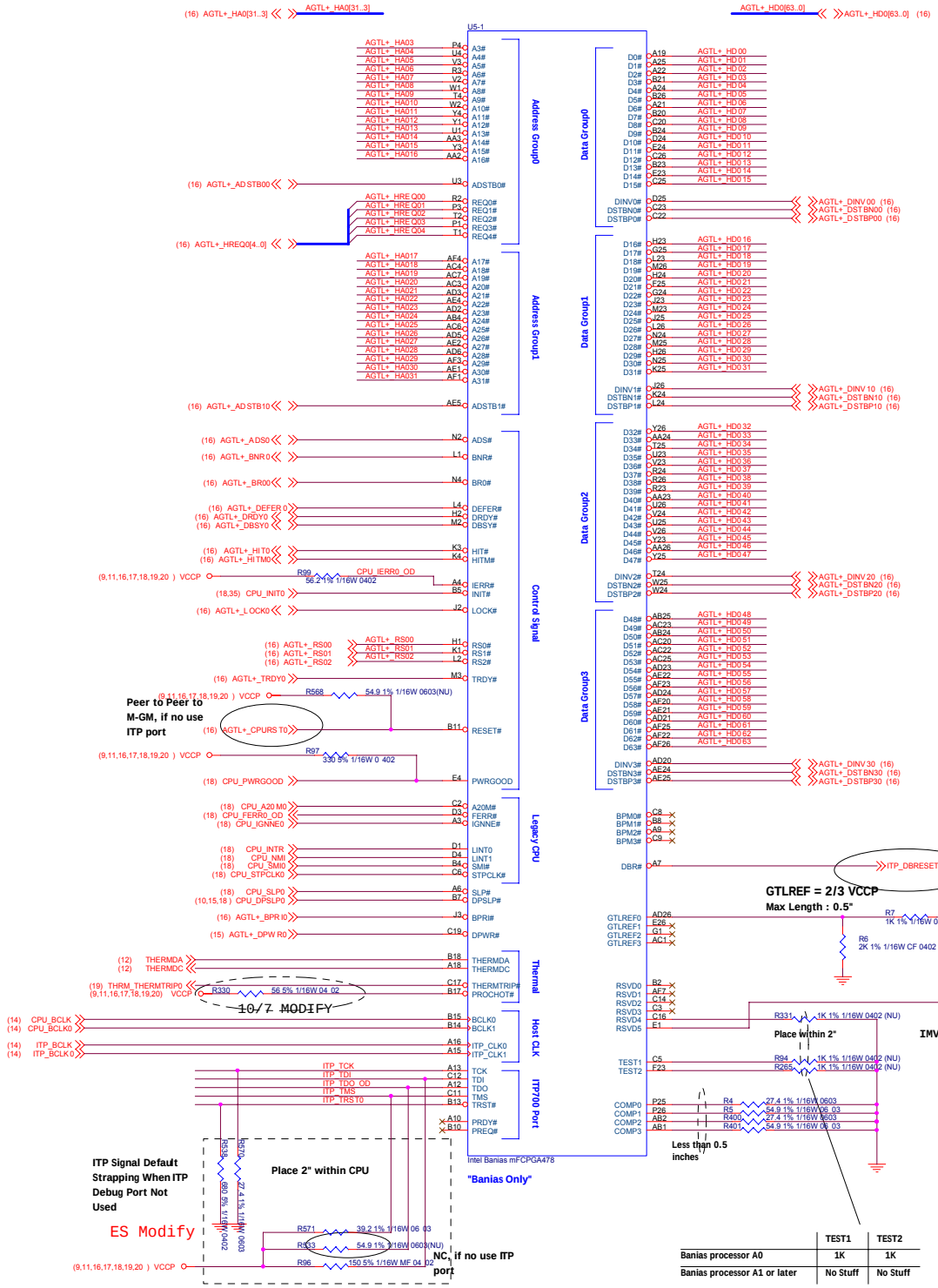
Title: MB02(Intel Banias + MontaraGM + ICH4-M)

Size: C | Document Number: Montara GM DDR Layout Guideline | Rev: 0.2A

Date: Thursday, December 19, 2002 | Sheet 7 of 66



	TEST1	TEST2
Banias processor A0	1K	1K
Banias processor A1 or later	No Stuff	No Stuff

System Bus Common Clock Signal Layout Guide :

ADS# , BNR# , BPRI# , BR0# , DBSY# , DEFER# , DPWR# , DRDY# , HIT# , HITM# , LOCK# , RS[2..0]# , TRDY# , RESET#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer) Micro-strip(Ext. Layer)	1.0 ~ 6.5 inch	55+/-10%	4 & 8(Int. Layer) 5 & 10(Ext. Layer)

Source Synchronous DATA :

DATA#[63..0] , DINV#[3..0] , DSTBN#[3.0] , DSTBP#[3..0]

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	0.5 ~ 5.5 inch	55+/-10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
DATA#[15..0] , DINV0#	+/- 100 mils	DSTBP0#,DSTBN0#	+/- 25 mils
DATA#[31..16] , DINV1#	+/- 100 mils	DSTBP1#,DSTBN1#	+/- 25 mils
DATA#[47..32] , DINV2#	+/- 100 mils	DSTBP2#,DSTBN2#	+/- 25 mils
DATA#[63..48] , DINV3#	+/- 100 mils	DSTBP3#,DSTBN3#	+/- 25 mils

Strobes of the same group should be trace length matched to each other within +-25mil and to the average length of their associated data signal group

Source Synchronous ADDRESS :

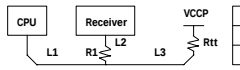
Address#[31..3] , REQ#[4..0] ,ADSTB#[1..0]

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line	0.5 ~ 6.5 inch	55+/-10%	4 & 12

Signals Name	Signals Matching	Strobes associated with the group	Strobe Matching
A#[16..3] , REQ#[4..0]	+/- 200 mils	ADSTB0#	+/- 25 mils
A#[31..17	+/- 200 mils	ADSTB1#	+/- 25 mils

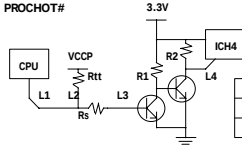
Strobes of the same group should be trace length matched to each other within +-25mil and to the average length of their associated data signal group

Topology : IERR# , FERR# , THERMTRIP#



L1	L2	L3	R1	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	56 +/-5%	56 +/-5%	Strip-line

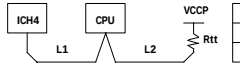
Topology : PROCHOT#



Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

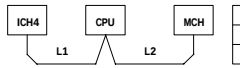
L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	0" - 3.0"	0.5" - 12"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	0" - 3.0"	0.5" - 12"	56 +/-5%	Strip-line

Topology : PWRGOOD



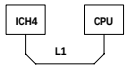
L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	330 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	330 +/-5%	Strip-line

Topology : DPSLP#



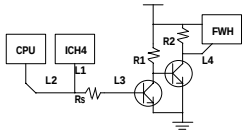
L1	L2	Transmission Line
0.5" - 12"	0.5" - 6.5"	Micro-strip
0.5" - 12"	0.5" - 6.5"	Strip-line

Topology : LINT1 , LINT0 , A20M# , IGNNE# , SLP# , SMI# , STPCLK#



L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

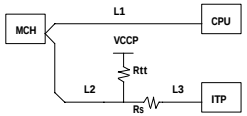
Topology : INIT# driven CH4



Rs : 330 +/-5%
R1 : 1.3K +/-5%
R2 : 330 +/-5%

L1 + L2	L3	L4	Transmission Line
0.5" - 12"	0" - 3.0"	0.5" - 6.0"	Micro-strip
0.5" - 12"	0" - 3.0"	0.5" - 6.0"	Strip-line

Topology : CPU RESET#



L1	L2 + L3	L3	Rs	Rtt
1.0" - 6.0"	12.0" max	0.5" max	22.6 +/-1%	54.9 +/-1%

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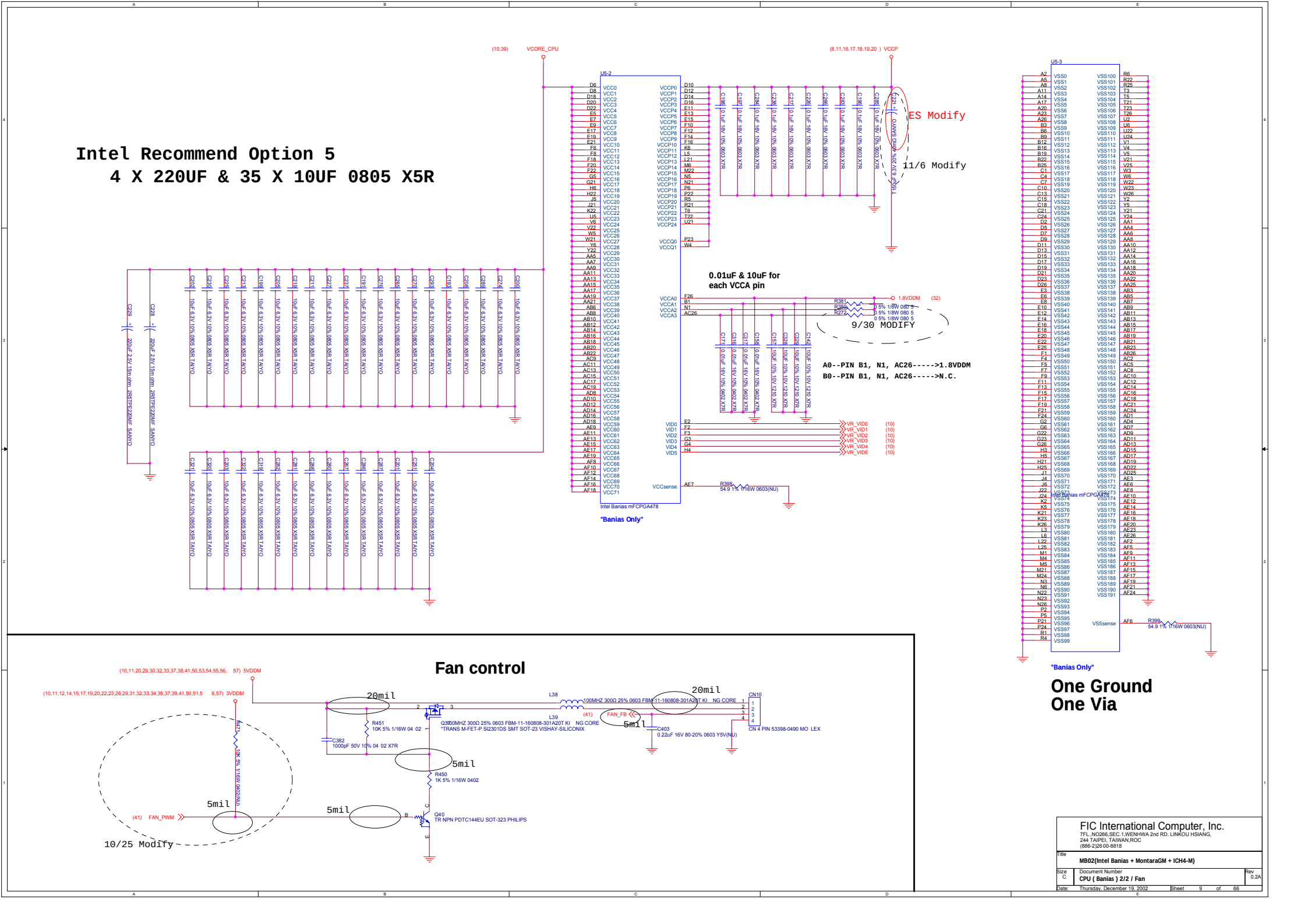
Title: MB02(Intel Banias + MontaraGM + ICH4-M)

Size: C | Document Number: CPU (Banias) 1/2 | Rev: 0.2A

Date: Thursday, December 19, 2002 | Sheet 8 of 66


Intel Recommend Option 5
4 X 220UF & 35 X 10UF 0805 X5R
(10,39) VCORE_CPU
(8,11,16,17,18,19,20) VCCP
U5-2
Intel Banias mFCPGA478
"Banias Only"
ES Modify
11/6 Modify
0.01uF & 10uF for each VCCA pin
1.8VDDM (32)
9/30 MODIFY
A0--PIN B1, N1, AC26----->1.8VDDM
B0--PIN B1, N1, AC26----->N.C.
VR_VID0 (10)
VR_VID1 (10)
VR_VID2 (10)
VR_VID3 (10)
VR_VID4 (10)
VR_VID5 (10)
R398 54.9 1% 1/16W 0603(NU)
U5-3
VSSsense
R399 54.9 1% 1/16W 0603(NU)
"Banias Only"
One Ground
One Via
Fan control
(10,11,20,29,30,32,33,37,38,41,50,53,54,55,56, 57) 5VDDM
(10,11,12,14,15,17,19,20,22,23,26,29,31,32,33,34,35,37,39,41,50,51,5 6,57) 3VDDM
20mil
5mil
L38 100MHZ 300Ω 25% 0603 FBM-11-160808-301A20T KI NG CORE
L39 Q300MHZ 300Ω 25% 0603 FBM-11-160808-301A20T KI NG CORE
*TRANS M-FET-P SI2301DS SMT SOT-23 VISHAY-SILICONIX
R451 10K 5% 1/16W 04 02
C382 1000pF 50V 10% 04 02 X7R
R450 1K 5% 1/16W 0402
R447 10K 5% 1/16W 0402(NU)
C403 0.22uF 16V 80-20% 0603 Y5V(NU)
CN10 CN 4 PIN 53398-0490 MO LEX
(41) FAN_PWM
(41) FAN_FB
Q40 TR NPN PDTC144EU SOT-323 PHILIPS
10/25 Modify
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(886-2)26 00-8818
Title
MB02(Intel Banias + MontaraGM + ICH4-M)
Size C
Document Number
CPU (Banias) 2/2 / Fan
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Date: Thursday, December 19, 2002
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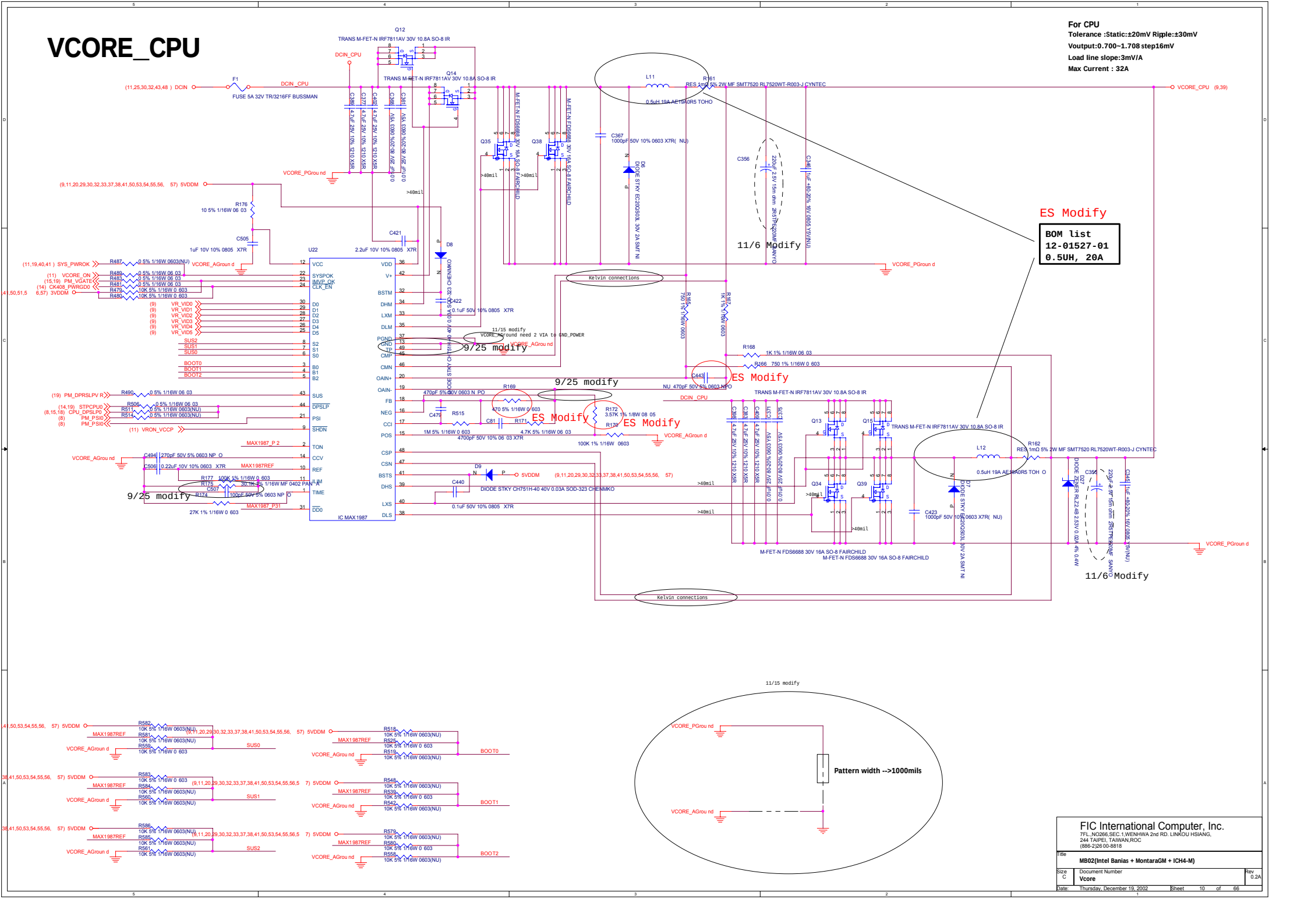
VCORE_CPU

For CPU
Tolerance :Static:±20mV Ripple:±30mV
Voutput:0.700~1.708 step16mV
Load line slope:3mV/A
Max Current : 32A



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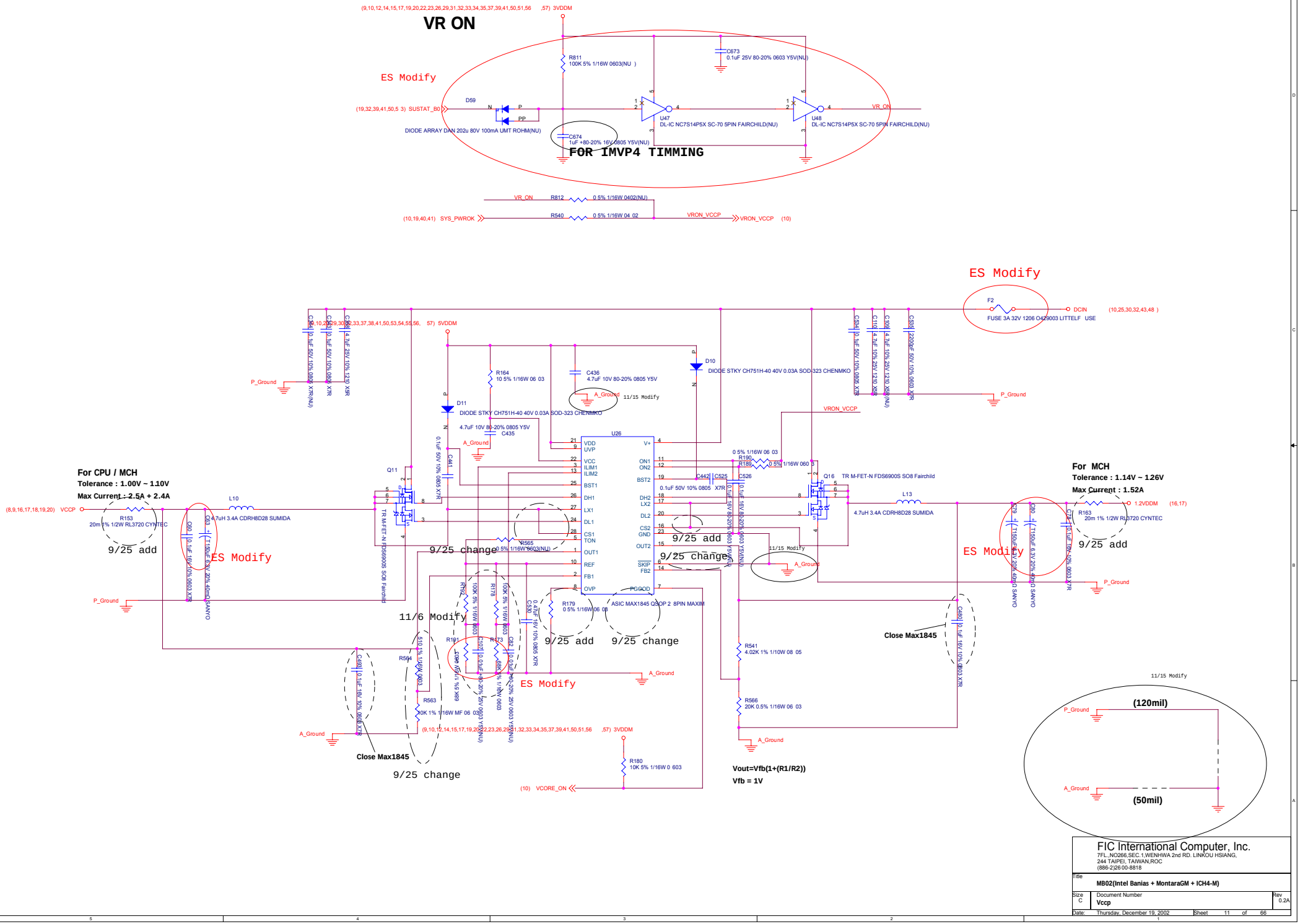
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Vcore	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 10 of 66	



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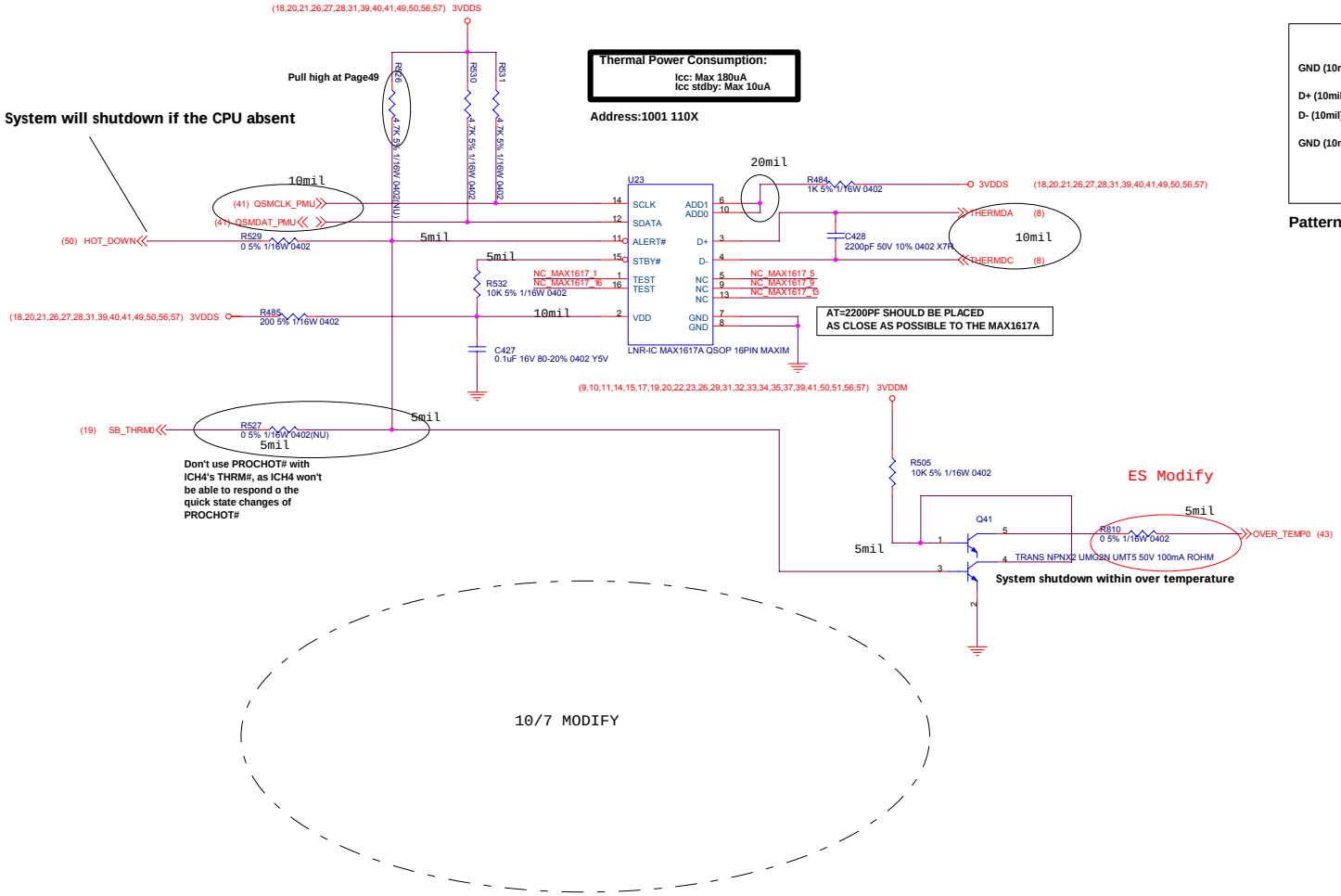
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Vccp	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 11 of 66	

Thermal Sensor



Layout Guide:

GND (10mil)
Spacing: 10mil
D+ (10mil)
D- (10mil)
Spacing: 10mil
GND (10mil)

Differential Pair:
Signals Parallel,Trace Length Equal,as short as possible

Patterns of D+/D- should be minimized via

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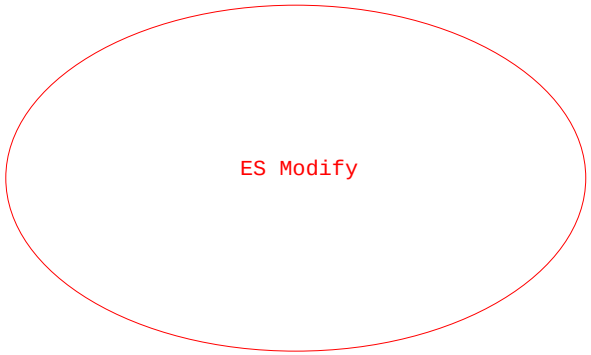
Title	**MB02(Intel Banias + MontaraGM + ICH4-M)**	
Size C	Document Number **Thermal Sensor (Max1617A)**	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 12 of 66	

ITP700FLEX I/F



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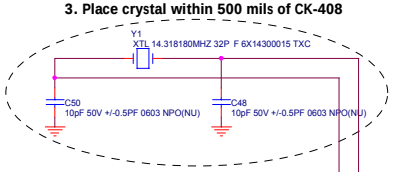
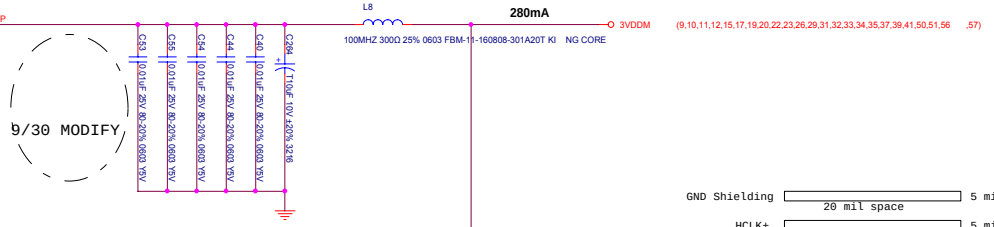
Title	**MB02(Intel Banias + MontaraGM + ICH4-M)**	
Size C	Document Number **ITP700**	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 13 of 66	

Clock Layout :

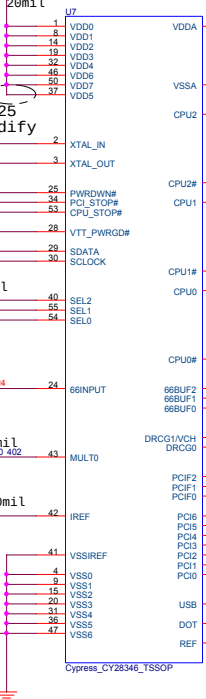
1. Close to Clock generator
2. Trace as short as possible and use 12 mil
3. Place crystal within 500 mils of CK-408





power plate 20mil

10mil



9/25 modify

9/25 Modify

(9,10,11,12,15,17,19,20,22,23,26,29,31,32,33,34,35,37,39,41,50,51,56 ,57) 3VDDM

R355 10K 5% 1/16W 0 402

(39,41) DC_SLP_S1 0 — DC_SLP_S 10 — C292 1uF 10V +80/-20% 0603 Y5V — D26 DIODE STKY CH751H-40 40V 0.03A SOD-323 CHENMKO

(19) STPPCI0
(10,19) STPCPU0
(10) GH406_PWRGD 0
(41) CLK_SMBD ATA
(41) CLK_SMB CLK

5mil / 10mil / 5mil

3VDDM_CLKSTRA P — R115 330 5% 1/16W 0402(NU) — R114 1K 5% 1/16W 0402

S2 S1 S0
0 0 1

R374 1K 5% 1/16W 0402 — R113 0 5% 1/16W 0402(NU)

R111 1K 5% 1/16W 0402

NC_CLKGEN_24

3VDDM_CLKSTRA P — R112 10K 5% 1/16W 0 402

R366 475 1% 1/16W 0603

Under 500mil / Under 200mil / Under 500mil / Under 500mil

R156 49.9 1% 1/16W 0603 — R155 49.9 1% 1/16W 0603
R146 33 1% 1/16W 06 03 — R145 33 1% 1/16W 06 03 — CPU_BCLK (8) — CPU_BCLK0 (8)
R158 49.9 1% 1/16W 0603 — R157 49.9 1% 1/16W 0603
R148 33 1% 1/16W 06 03 — R147 33 1% 1/16W 06 03 — MCH_BCLK (16) — MCH_BCLK0 (16)
R391 49.9 1% 1/16W 0603(NU) — R390 49.9 1% 1/16W 0603(NU)
R119 33 1% 1/16W 0603(NU) — R118 33 1% 1/16W 0603(NU) — ITP_BCLK (8) — ITP_BCLK 0 (8)

ES Modify

L9
100MHZ 300Ω 25% 0603 FBM-11-160808-301A20T KI NG CORE

C43 0.01uF 25V 80-20% 0603 Y5 V
C262 T10uF 10V ±20% 3 216

GND Shielding — 20 mil space — 5 mil space
HCLK+ — 5 mil space
HCLK- — 20 mil space
GND Shielding — 5 mil space
(5 mil width for differential signals and GND shiekding)

FOR ITP700 FLEX

FOR INTERPOSER BOARD

NC_CLKGEN_23 — R76 33 1% 1/16W 06 03 — R77 33 1% 1/16W 06 03 — CLK_MCH66 (15) — CLK_ICH66 (18)

R142 33 1% 1/16W 06 03 SSCLKIN — NC_CLKGEN_22

PCIF2 Should be free-running PCI clock.

R88 33 1% 1/16W 06 03 — CLK_ICHPCI (18)
NC_CLKGEN_6
NC_CLKGEN_5
R78 33 1% 1/16W 06 03 — NC_CLKGEN_17 — CLK_LANPCI (31)
R79 33 1% 1/16W 06 03 — CLK_CBPCI (26)
R84 33 1% 1/16W 06 03 — CLK_KBCPCI (37)
R85 33 1% 1/16W 06 03 — CLK_FWHPCI (35)
R86 33 1% 1/16W 06 03 — CLK_MINIPCI (57)
R87 33 1% 1/16W 06 03 — CLK_PMU08PCI (39)
R144 33 1% 1/16W 06 03 — CLK_ICH48 (19)
R143 33 1% 1/16W 06 03 — CLK_MCH48 (15)
R117 22 1% 1/16W 06 03 — 14MCLK_A C97 (51)
R116 22 1% 1/16W 06 03 — CLK_ICH14 (19)
R394 33 1% 1/16W 0603(NU) SSCLKIN

1178 Modify

C261 5pF 50V +/-0.5PF 0402(NU)
C262 5pF 50V +/-0.5PF 0402(NU)
C265 5pF 50V +/-0.5PF 0402(NU)
C98 5pF 50V +/-0.5PF 0402(NU)
C258 5pF 50V +/-0.5PF 0402(NU)
C259 5pF 50V +/-0.5PF 0402(NU)
C260 5pF 50V +/-0.5PF 0402(NU)
C257 5pF 50V +/-0.5PF 0402(NU)
C256 5pF 50V +/-0.5PF 0402(NU)
C234 5pF 50V +/-0.5PF 0402(NU)
C255 5pF 50V +/-0.5PF 0402(NU)
C236 5pF 50V +/-0.5PF 0402(NU)
C238 5pF 50V +/-0.5PF 0402(NU)

Thermal Power Consumption:
Icc: Max 280mA

Address:1101 001X

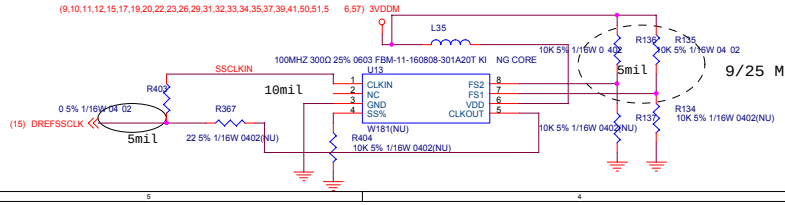
Clock Latout Guideline

	CLOCKS	LENGTH	TRACE / SPACE	NOTES
HOST Clock	CPU_BCLK[1..0] MCH_BCLK[1..0] ITP_BCLK[1..0]	2" ~ 8 "	5 / 20 mils (5 mil space between 1 & 0)	1.Differentials pairs with the same length (within 10 mil) 2. CPU & NB trace mismatch within 20 mil
CLK66 Clock	CLK_ICH66 CLK_MCH66	4.5" ~ 9.0 "	5 / 20 mils	Length mismatch within 100 mils
	CLK_AGP	MAX : 8.5"		
CLK33 Clock	CLK_ICHPCI CLK_SIOPCI CLK_FWHPCI	4.5" ~ 9.0 "	5 / 20 mils	Length same as CLK66 Clock Length mismatch within 100mils
PCI Clock	CLK_MINIPCI CLK_1394PCI CLK_PMU08PCI CLK_CBPCI	4.5"~9.0"	5 / 20 mils	1.Making PCI length with minimum various 2. Length Require CLK33-2.5" 3. Length mismatch +/- 2.0"
CLK14 Clock	CLK_SIO14 CLK_ICH14 CLK_TV14	2.0"~9.0"	5 / 20 mils	1. Length mismatch +/- 500 mils
	CLK_ICH48 CLK_MCH48	3.5" ~ 12.5"	5 / 20 mils	

Clock Package Length

Banais Processor Package Length 485mils
Montara-GM GMCH Package Length 1142 mils
CPU Socket Equivalent Length 157 mils

GND Shielding — 10 mil space — 5 mil space
DREFSSCLK — 10 mil space — 5 mil space
GND Shielding — 10 mil space — 5 mil space



S2	S1	S0	CPU	3V66	66BUFF	66INPUT	PCI_F	REF	USB
1	0	0	66M	66M	66IN	66M CKIN	66IN/2	14.318M	48M
1	0	1	100M	66M	66IN	66M CKIN	66IN/2	14.318M	48M
1	1	0	200M	66M	66IN	66M CKIN	66IN/2	14.318M	48M
1	1	1	133M	66M	66IN	66M CKIN	66IN/2	14.318M	48M
0	0	0	66M	66M	66M	66M	33M	14.318M	48M
0	0	1	100M	66M	66M	66M	33M	14.318M	48M
0	1	0	200M	66M	66M	66M	33M	14.318M	48M
0	1	1	133M	66M	66M	66M	33M	14.318M	48M
M	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	0	1	Tclk/2	Tclk/4	Tclk/4	Tclk/4	Tclk/8	Tclk	Tclk/2

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Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Clock Generator (Cypress CY28346ZC)	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 14 of 66	

Layout Notes (DVO):

Spacing to Trace Width ratio : 2 to 1
Minimum spacing to non-DVO signals: 20 mils
Minimum spacing to other DVO signals: 12 mils
Trace Length : Max 6.0"

DVO Interface Trace Length Requirements:

Data Group	Signal Matching to Strobe Clock	DVO Clock Strobes Associated with the Group	Clock Strobe Matching
DVOBD[11:0]	+/- 100 mils	DVOBCLK[1:0]	+/- 10 mils
DVOCD[11:0]	+/- 100 mils	DVOCCLK[1:0]	+/- 10 mils

Layout Notes (LVDS):

Differential Mode Impedance: 100ohm+-15%
Nominal Trace Width :4 mil
Nominal PairSpacing (edge to edge); 7mil
Minimum Pair to Pair Spacing; 20mil
Minimum Serpentine Spacing: 20mil
Minimum Spacing to Other LVDS Signals: 20mil
Minimum Isolation Spacing to non-LVDS Signals: 20mil
Max Via Count: 2
Package Length Range: 550mil+-150mil
Total Length: Max 10inch
Clock Length Matching: Match all segment to +-20mil
Clock to Clock Length Matching (Total Length): Match Clocks to +-20mil

5 mil GND
10 mil RED
10 mil
10 mil GREEN
10 mil
10 mil BLUE
5 mil GND

U1B

DDR SYSTEM MEMORY

MONTARA-GM_GMCH

No support DDR ECC

No support DDR ECC

No support DDR ECC

No support DDR ECC

U1A

DVO

DAC

LVDS

CLKS

MISC

NC

MONTARA-GM_GMCH

Low is for DVO use(Default)

High is for P4M

Trace should be 10 mil wide with 20 mil spacing

Communicate with VBIOS to know DVO Devices

ADDID7~ADDID4 ADDID3~ADDID0

0 1 1 1--->7 1 1 1 1--->F

9/30 MODIFY

RVSD7	ST0	Clock Configuration Straps	0	1	0
RVSD6	ST1		0	0	1
RVSD5	ST2				
FSB			400	400	400
DDR			266	200	200
Gfx			133~200 Default	100~200	100~133 no UXGA

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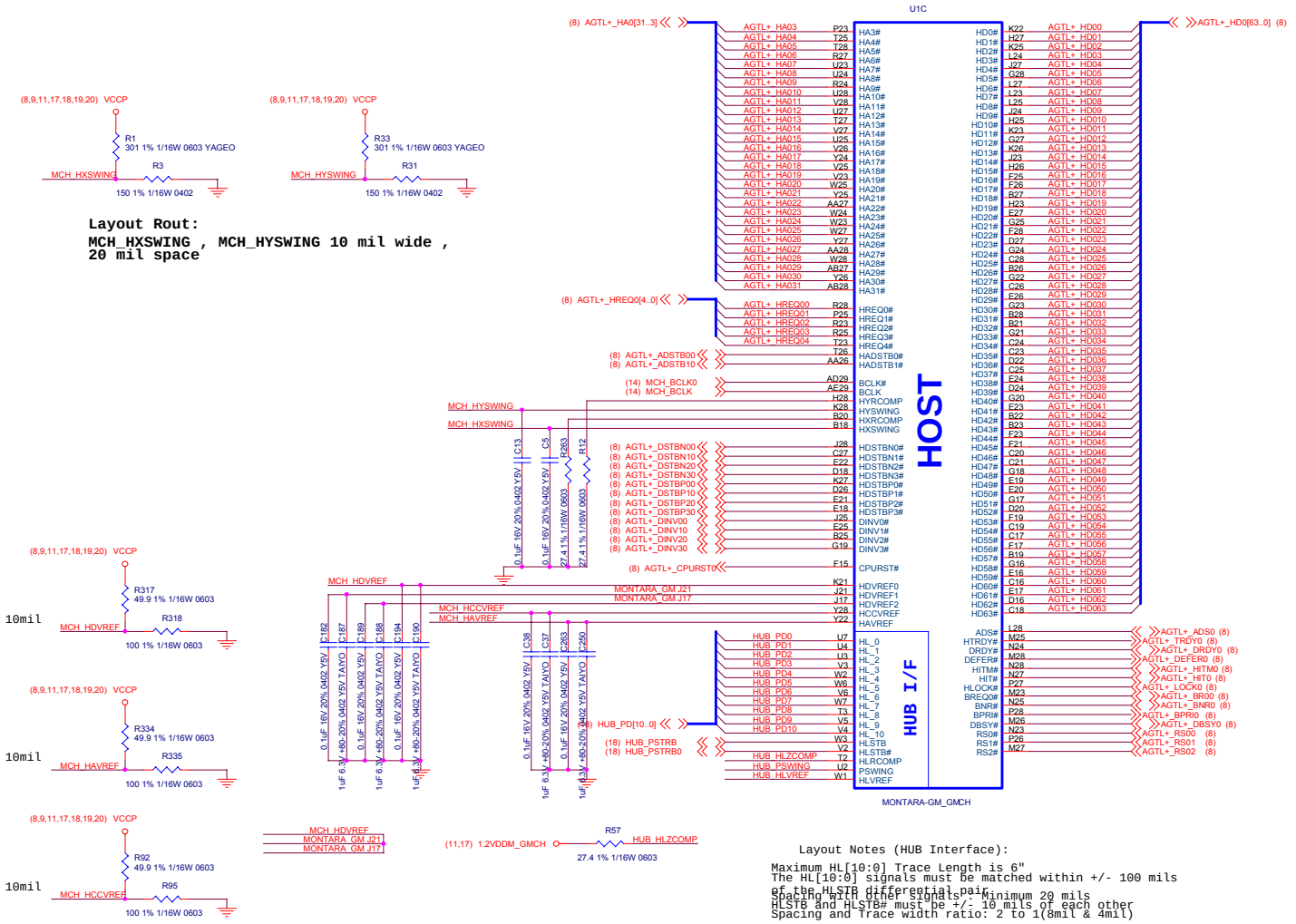
Title: MB02(Intel Banias + MontaraGM + ICH4-M)

Size C | Document Number Montara-GM 1/3 | Rev 0.2A

Date: Thursday, December 19, 2002 | Sheet 15 of 66

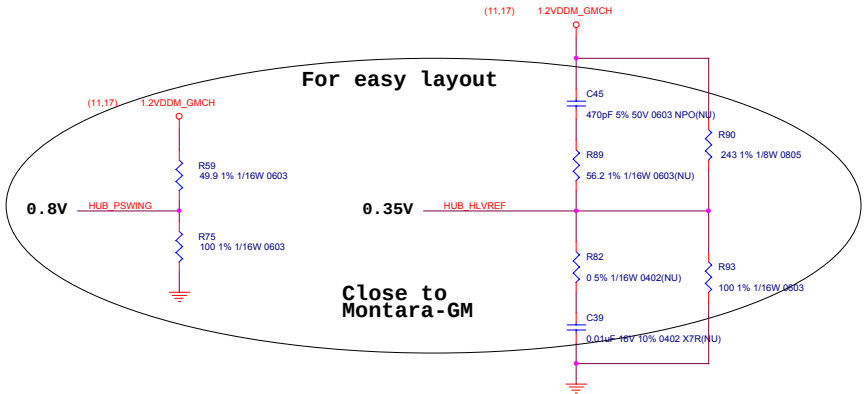


Layout Rout:
MCH_HXSWING , MCH_HYSWING 10 mil wide , 20 mil space

Layout Rout:
Maximum length from pin to voltage divider for MCH_HDVREF,MCH_HCCVREF,MCH_HAVREF should be less than 0.5 inches.

Layout Notes (HUB Interface):

Maximum HL[10:0] Trace Length is 6"
The HL[10:0] signals must be matched within +/- 100 mils of the HLSTB differential pair.
Spacing with other signals: Minimum 20 mils
HLSTB and HLSTB# must be +/- 10 mils of each other
Spacing and Trace width ratio: 2 to 1(8mil & 4mil)



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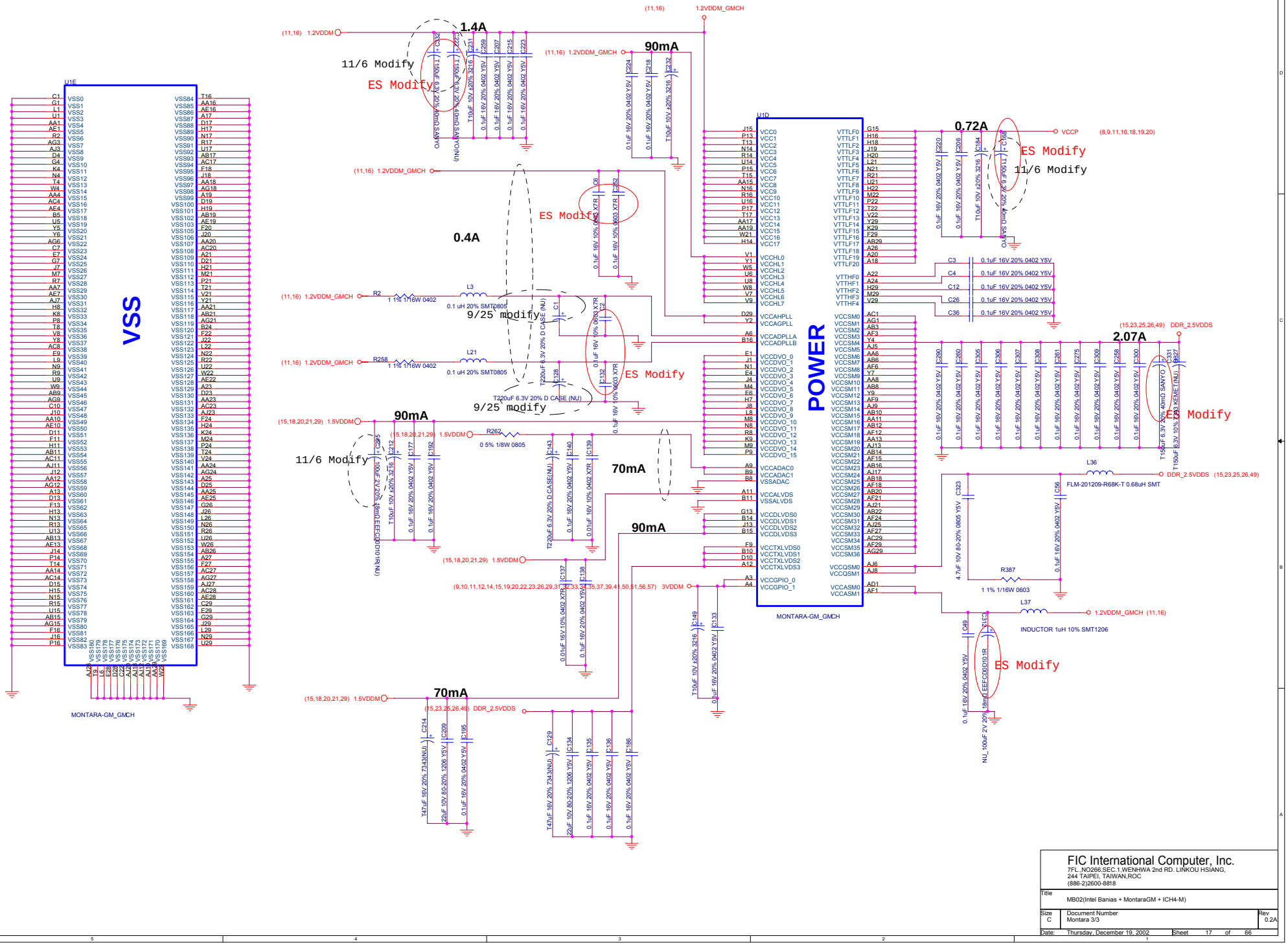
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Montara GM 2/3	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 16 of 66	



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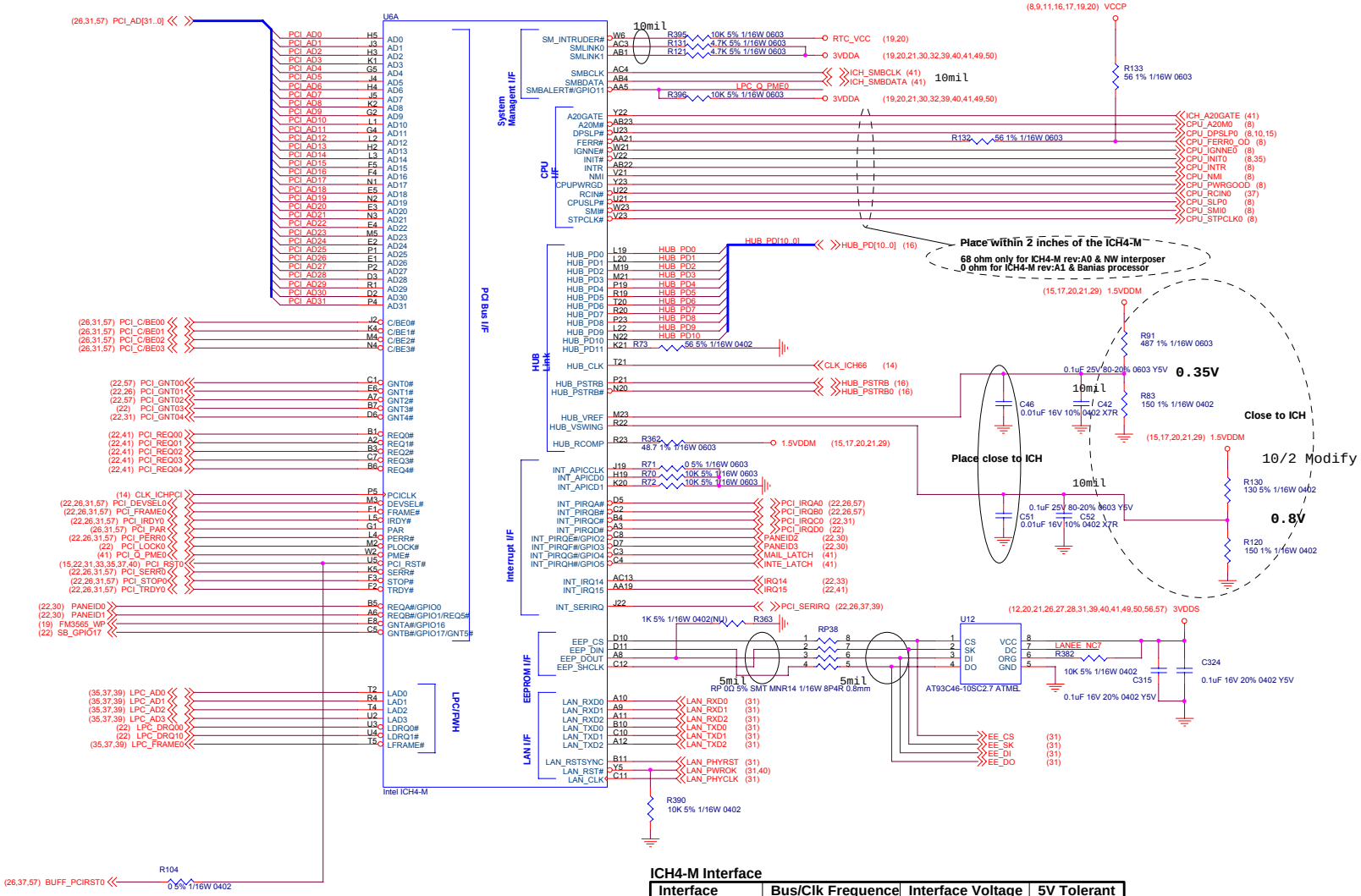
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Montara 3/3	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 17 of 66	



ICH4-M Bandwidth

Interface	Clk Speed (MHz)	Sample Per Clk	Data Rate (Mega-sample/S)	Data Width (Bytes)	Bandwidth (MB/S)
Hub Interface	66MHz	4	266MHz	1	266MHz
PCI 2.2	33MHz	1	33MHz	4	133MHz

ICH4-M Interface

Interface	Bus/Clk Frequence	Interface Voltage	5V Tolerant
CPU (Sideband)	N/A	1.5V	
Hub Interface	66MHz	1.8V	
PCI	33MHz	3.3V	Yes
LPC	33MHz	3.3V	
FWH	33MHz	3.3V	
USB	48MHz	3.3V	
IDE	[ATA 33/66/100]	3.3V	Yes
AC97	12.288MHz	3.3V	
LAN-D100 MAC	Up to 50 MHz	3.3V I/O 1.8V Core	
SMBus	N/A	3.3V	
Interrupt	N/A	3.3V	Yes
RTC	N/A	3.3V	
Resume Well	N/A	3.3V I/O 1.8V Core	
GPIO	N/A	3.3V	Yes

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Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number ICH4 (PCI / Hub Link / CPU / IRQ / Lan) 1/3	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 18 of 66	

IDE Layout Giude:

Trace:5 mil, Spacing: 7mil
Must be less than 8 inch
The maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch

USB 2.0 Trace Length Guide

Low-Speed Signal	DP1	DM1	DP2	DM2	Clock/ High Speed Signal
20 mil	4 mil	4.5 mil	4 mil	4.5 mil	4 mil	50 mil
20 mil					

Signals Reference	Signal Mismatch	MB Trace Length
Ground	The max mismatch between data pairs should not be greater than 150mils	17 inches

USBRBIAS/USBRBIAS# Routing Requirements	Maximum Trace Length
5 on 5	500 mil

USBRBIAS
USBRBIAS#
500 mil

Pull high to 3VDDA, when ITP Debug Port Not Used

R123 10K 5% 1/16W 0402

U6B

Power Management
IST
AC97 I/F
USB I/F
Unmuxed GPIOs
GPIOs
Clocks
Misc
Primary IDE
Secondary IDE

Intel ICH4-M

Power Strap Pin

R298 10K 5% 1/16W 0402(NU) — Stuff for safe mode
R347 1K 5% 1/16W 0402(NU) — StuffF for No Reboot
R300 1K 5% 1/16W 0402(NU) — Stuff for A16 swap override

11/8 Modify
Route USB_RBIAS/RBIAS# differentially
11/8 Modify
ES Modify
11/8 Modify

5V tolerant
GPIO6 input (3VDDM) Not implemented
GPIO7 & GPIO[5:0] input (3VDDM)
GPIO8 & GPIO[13:11] input (3VDDA) GPIO9,10 not implemented
GPIO[17:16] output (3VDDM)
GPIO[24:18] output/input (3VDDM) Not implemented
GPIO[28:25] output/input (default:output) (3VDDA) GPIO26 not implemented
GPIO[31:29] output (3VDDM) Not implemented
GPIO[47:44] output/input (3VDDM) Not implemented

not 5V tolerant
GPIO[43:32] output/input (default:output) (3VDDM)

PowerOK
LNR-IC PST9228 SOT-25A 5PIN MITSUMI
10/2 Modify

TR PNP 2SB1132T100 -1A -32V MPT3 SC-62 ROHM
DIODE ISS355 SOD-323 CHENMKO
DIODE STKY CH751-40 SOD-323 CHENMKO
DIODE ISS355 SOD-323 CHENMKO
9/30 MODIFY
10/2 Modify
ES Modify
3V~3.3V

RTC Layout Giude:
1. Keep the lead lengths as short as possible, around 1/4 inch is sufficient
2. Minimize the capacitance between Xin and Xout component
3. Put a ground plane under the Xtal component
4. Do not route any switching signals under the external component (unless separated by a ground plane)
5. The Oscillator VCC should be clean, use a filter, such as an RC low pass or a ferrite inductor
6. The Oscillator VCC should be clean, use a filter, such as an RC low pass or a ferrite inductor

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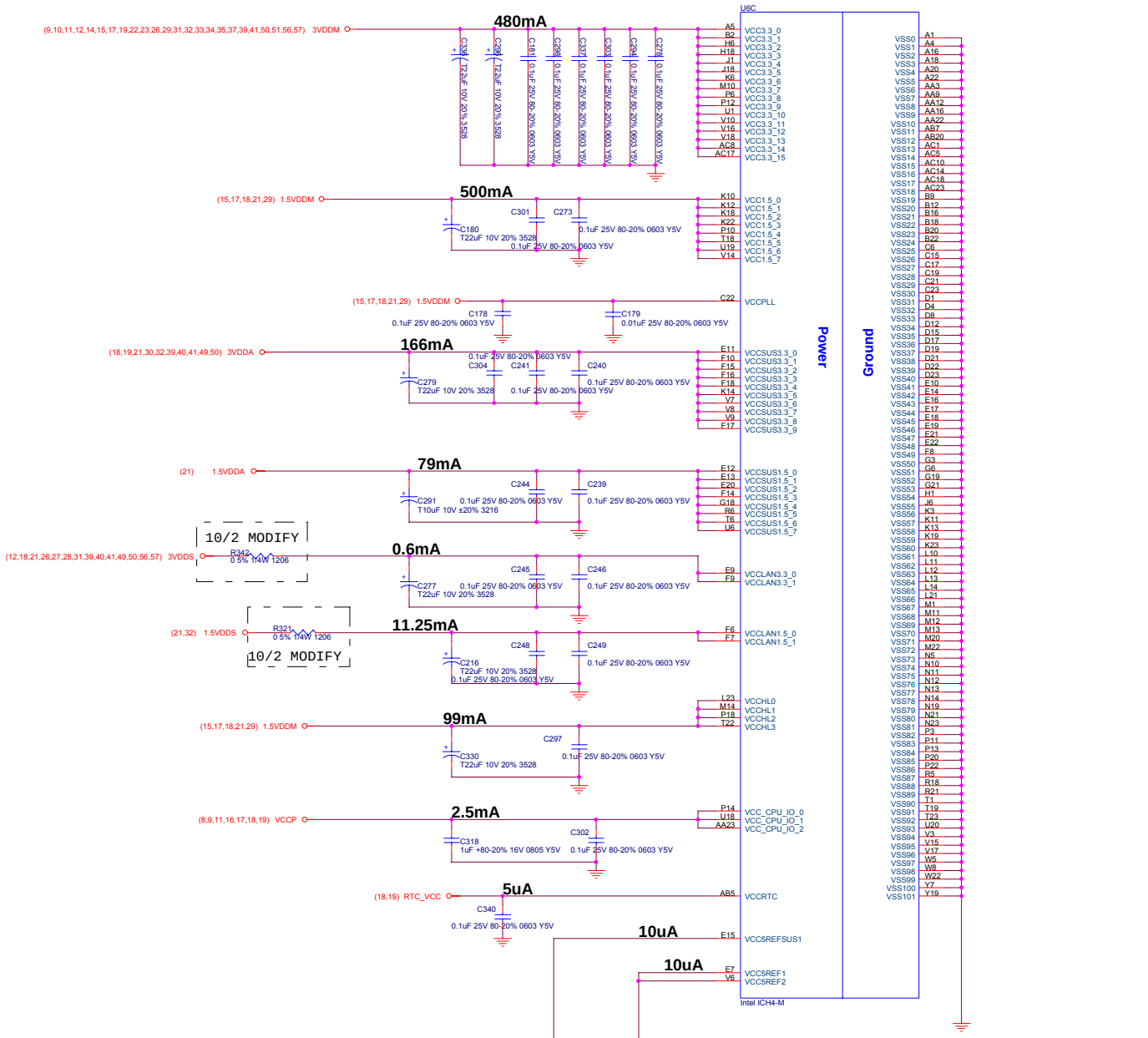
Title		
MB02(Intel Banias + MontaraGM + ICH4-M)		
Size C	Document Number ICH4 (IDE / AC97 / USB2 / PMU / GPIO) 2/3	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 19 of 66	



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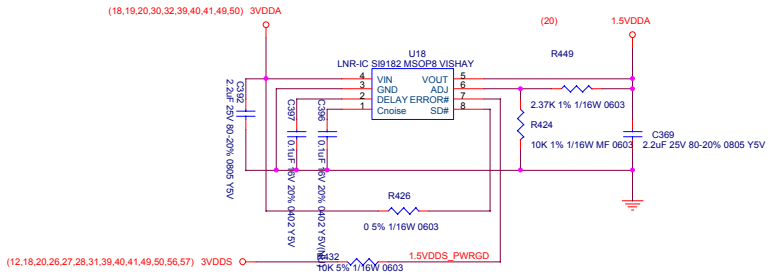
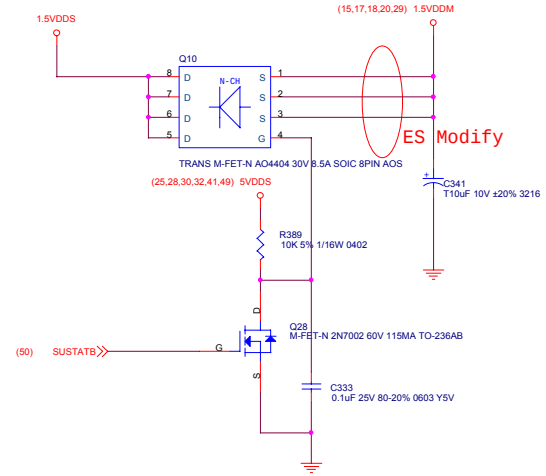
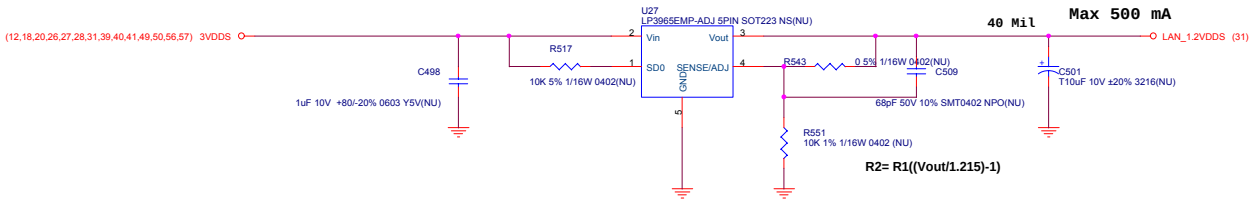
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number ICH4 (Power / Ground) 3/3	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 20 of 66	

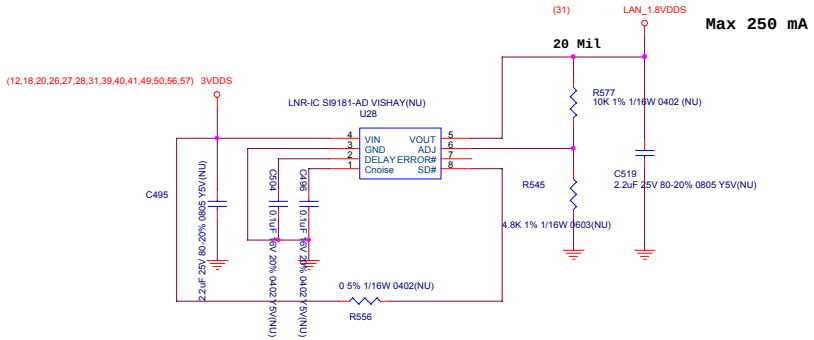
1.5VDDA / 1.5VDDM





LAN_1.2VDDS / LAN_1.8VDDS





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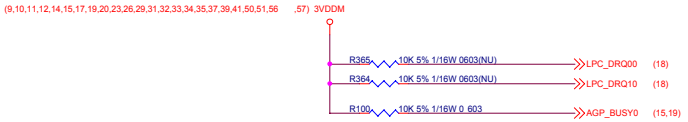
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Power (1.5VDDA / 1.5VDDM/ GigaLAN Power)	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 21 of 66	

PCI Pull Up/Down

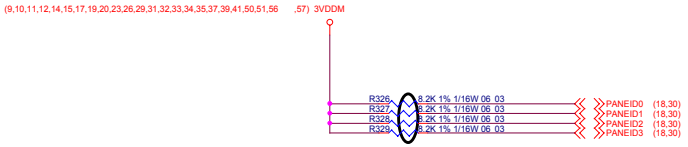
LPC Pull Up

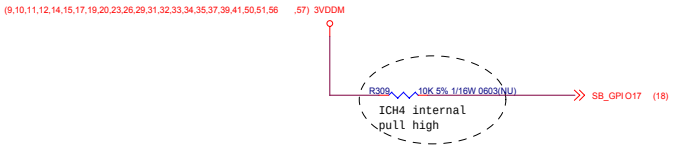


PCI PMU Pull Up

AC97 Pull Down

GPIO Pull Up





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Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number PCI / LPC / GPIO Pull Up/Down	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 22 of 66	

Command Signals use Topology 2

10/25 Modify

(15) SM_DATA[63..0]

RP17 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA0 SM_DATA1 SM_DATA2 SM_DATA3 — SM_R_DATA0 SM_R_DATA1 SM_R_DATA2 SM_R_DATA3

RP3 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA4 SM_DATA5 SM_DATA6 SM_DATA7 — SM_R_DATA4 SM_R_DATA5 SM_R_DATA6 SM_R_DATA7

RP18 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA8 SM_DATA9 SM_DATA10 SM_DATA11 — SM_R_DATA8 SM_R_DATA9 SM_R_DATA10 SM_R_DATA11

RP4 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA12 SM_DATA13 SM_DATA14 SM_DATA15 — SM_R_DATA12 SM_R_DATA13 SM_R_DATA14 SM_R_DATA15

RP19 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA16 SM_DATA17 SM_DATA18 SM_DATA19 — SM_R_DATA16 SM_R_DATA17 SM_R_DATA18 SM_R_DATA19

RP5 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA20 SM_DATA21 SM_DATA22 SM_DATA23 — SM_R_DATA20 SM_R_DATA21 SM_R_DATA22 SM_R_DATA23

RP20 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA24 SM_DATA25 SM_DATA26 SM_DATA27 — SM_R_DATA24 SM_R_DATA25 SM_R_DATA26 SM_R_DATA27

RP6 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA28 SM_DATA29 SM_DATA30 SM_DATA31 — SM_R_DATA28 SM_R_DATA29 SM_R_DATA30 SM_R_DATA31

RP21 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA32 SM_DATA33 SM_DATA34 SM_DATA35 — SM_R_DATA32 SM_R_DATA33 SM_R_DATA34 SM_R_DATA35

RP7 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA36 SM_DATA37 SM_DATA38 SM_DATA39 — SM_R_DATA36 SM_R_DATA37 SM_R_DATA38 SM_R_DATA39

RP22 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA40 SM_DATA41 SM_DATA42 SM_DATA43 — SM_R_DATA40 SM_R_DATA41 SM_R_DATA42 SM_R_DATA43

RP8 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA44 SM_DATA45 SM_DATA46 SM_DATA47 — SM_R_DATA44 SM_R_DATA45 SM_R_DATA46 SM_R_DATA47

RP23 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA48 SM_DATA49 SM_DATA50 SM_DATA51 — SM_R_DATA48 SM_R_DATA49 SM_R_DATA50 SM_R_DATA51

RP9 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA52 SM_DATA53 SM_DATA54 SM_DATA55 — SM_R_DATA52 SM_R_DATA53 SM_R_DATA54 SM_R_DATA55

RP24 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA56 SM_DATA57 SM_DATA58 SM_DATA59 — SM_R_DATA56 SM_R_DATA57 SM_R_DATA58 SM_R_DATA59

RP10 RP 10 5% 0402*4 1/16W 8P4R
SM_DATA60 SM_DATA61 SM_DATA62 SM_DATA63 — SM_R_DATA60 SM_R_DATA61 SM_R_DATA62 SM_R_DATA63

>>SM_R_DATA[63..0] (24)

RP41 RP 10 5% 0402*4 1/16W 8P4R
RP42 RP 10 5% 0402*4 1/16W 8P4R 0.5mm
RP43 RP 10 5% 0402*2 1/16W 4P2R 0.65mm

(15,24) SM_MA[12..0]

SM_MA1 SM_MA2 SM_MA4 SM_MA5 SM_MA0 SM_MA3 SM_MA10 SM_SBS1 SM_MA11 SM_MA8 SM_MA6 SM_MA7 SM_MA9 SM_MA12
SM_R_MA0 SM_R_MA3 SM_R_MA10 SM_R_SBS1 SM_R_MA11 SM_R_MA8 SM_R_MA6 SM_R_MA7 SM_R_MA9 SM_R_MA12

(15,24) SM_SBS1
SM_SBS1 M_AB1 M_AB2 M_AB4 M_AB5

RP40 RP 10 5% 0402*4 1/16W 8P4R
(15,24) SM_SRAS0 (15,24) SM_SBS0 (15,24) SM_SCAS0 (15,24) SM_SWE0
SM_SRAS0 SM_SBS0 SM_SCAS0 SM_SWE0
SM_R_SRAS0 SM_R_SBS0 SM_R_SCAS0 SM_R_SWE0

11/11 Modify

11/5 Modify

(24) SM_R_DATA[63..0]

CN11A

SM_R_MA0	112A	A_A0	DQ0	5	SM_R_DATA0
SM_MA1	111A	A_A1	DQ1	7	SM_R_DATA1
SM_MA2	110A	A_A2	DQ2	13	SM_R_DATA2
SM_R_MA3	109A	A_A3	DQ3	17	SM_R_DATA3
SM_MA4	108A	A_A4	DQ4	6	SM_R_DATA4
SM_MA5	107A	A_A5	DQ5	8	SM_R_DATA5
SM_R_MA6	106A	A_A6	DQ6	14	SM_R_DATA6
SM_R_MA7	105A	A_A7	DQ7	18	SM_R_DATA7
SM_R_MA8	102A	A_A8	DQ8	19	SM_R_DATA8
SM_R_MA9	101A	A_A9	DQ9	23	SM_R_DATA9
SM_R_MA10	115A	A_A10/AP	DQ10	29	SM_R_DATA10
SM_R_MA11	100A	A_A11	DQ11	31	SM_R_DATA11
SM_R_MA12	99A	A_A12	DQ12	20	SM_R_DATA12
T119 1	97A	A_A13(DU)	DQ13	24	SM_R_DATA13
			DQ14	30	SM_R_DATA14
			DQ15	32	SM_R_DATA15
			DQ16	41	SM_R_DATA16
(15) SMCLK_DDR0	35A	A_CK0	DQ17	43	SM_R_DATA17
(15) SMCLK_DDR00	37A	A_CK0#	DQ18	49	SM_R_DATA18
(15) SMCLK_DDR1	160A	A_CK1	DQ19	53	SM_R_DATA19
(15) SMCLK_DDR10	158A	A_CK1#	DQ20	42	SM_R_DATA20
T112 1	89A	A_CK2	DQ21	44	SM_R_DATA21
T113 1	91A	A_CK2#	DQ22	50	SM_R_DATA22
	96A	A_CKE0	DQ23	54	SM_R_DATA23
(15,24) SM_SCKE0	95A	A_CKE1	DQ24	55	SM_R_DATA24
(15,24) SM_SCKE1	121A	A_S0#	DQ25	59	SM_R_DATA25
(15,24) SM_SCS00	122A	A_S1#	DQ26	65	SM_R_DATA26
(15,24) SM_SCS10	194A	A_SA0	DQ27	67	SM_R_DATA27
	196A	A_SA1	DQ28	57	SM_R_DATA28
	198A	A_SA2	DQ29	60	SM_R_DATA29
			DQ30	66	SM_R_DATA30
SM_R_SBS0	117A	A_BA0	DQ31	68	SM_R_DATA31
SM_R_SBS1	116A	A_BA1	DQ32	127	SM_R_DATA32
			DQ33	129	SM_R_DATA33
SM_R_SCAS0	120A	A_CAS#	DQ34	135	SM_R_DATA34
SM_R_SRAS0	118A	A_RAS#	DQ35	139	SM_R_DATA35
SM_R_SWE0	119A	A_WE#	DQ36	128	SM_R_DATA36
			DQ37	130	SM_R_DATA37
			DQ38	136	SM_R_DATA38
			DQ39	140	SM_R_DATA39
			DQ40	141	SM_R_DATA40
			DQ41	145	SM_R_DATA41
SM_MA0	112B	B_A0	DQ42	151	SM_R_DATA42
M_AB1	111B	B_A1	DQ43	153	SM_R_DATA43
M_AB2	110B	B_A2	DQ44	142	SM_R_DATA44
SM_MA3	109B	B_A3	DQ45	146	SM_R_DATA45
M_AB4	108B	B_A4	DQ46	152	SM_R_DATA46
M_AB5	107B	B_A5	DQ47	154	SM_R_DATA47
SM_MA6	106B	B_A6	DQ48	163	SM_R_DATA48
SM_MA7	105B	B_A7	DQ49	165	SM_R_DATA49
SM_MA8	102B	B_A8	DQ50	171	SM_R_DATA50
SM_MA9	101B	B_A9	DQ51	175	SM_R_DATA51
SM_MA10	115B	B_A10/AP	DQ52	164	SM_R_DATA52
SM_MA11	100B	B_A11	DQ53	166	SM_R_DATA53
SM_MA12	99B	B_A12	DQ54	172	SM_R_DATA54
T114 1	97B	B_A13(DU)	DQ55	176	SM_R_DATA55
			DQ56	177	SM_R_DATA56
			DQ57	181	SM_R_DATA57
			DQ58	187	SM_R_DATA58
(15) SMCLK_DDR3	35B	B_CK0	DQ59	189	SM_R_DATA59
(15) SMCLK_DDR30	37B	B_CK0#	DQ60	178	SM_R_DATA60
(15) SMCLK_DDR4	160B	B_CK1	DQ61	182	SM_R_DATA61
(15) SMCLK_DDR40	158B	B_CK1#	DQ62	188	SM_R_DATA62
T115 1	89B	B_CK2	DQ63	190	SM_R_DATA63
T116 1	91B	B_CK2#			
(15,24) SM_SCKE2	96B	B_CKE0			
(15,24) SM_SCKE3	95B	B_CKE1	DM0	12	M_R_DM0
(15,24) SM_SCS20	121B	B_S0#	DM1	28	M_R_DM1
(15,24) SM_SCS30	122B	B_S1#	DM2	48	M_R_DM2
(9,10,11,12,14,15,17,19,20,22,26,29,31,32,33,34,35,37,39,41,50,51,56,57) 3VDDM	194B	B_SA0	DM3	62	M_R_DM3
	196B	B_SA1	DM4	134	M_R_DM4
	198B	B_SA2	DM5	148	M_R_DM5
			DM6	170	M_R_DM6
			DM7	184	M_R_DM7
SM_SBS0	117B	B_BA0			M_R_DM8
SM_SBS1	116B	B_BA1	DQS0	11	SM_R_SDQS0
T58 1	98	BA2(DU)	DQS1	25	SM_R_SDQS1
SM_SCAS0	120B	B_CAS#	DQS2	47	SM_R_SDQS2
SM_SRAS0	118B	B_RAS#	DQS3	61	SM_R_SDQS3
SM_SWE0	119B	B_WE#	DQS4	133	SM_R_SDQS4
	195	SCL	DQS5	147	SM_R_SDQS5
(41) SM_SMBCLK_DIMM0	193	SDA	DQS6	169	SM_R_SDQS6
(41) SM_SMBDATA_DIMM0	86	RESET(DU)	DQS7	183	SM_R_SDQS7
T60 1			DQS8		SM_R_SDQS8

CN 218PIN DUAL DDR SO-DIMM

M_R_DM[8..0] (24)

(15,17,25,26,49) DDR_2.5VDDS

CN11B

	9	VDD1	VSS1	3	
	21	VDD2	VSS2	15	
	33	VDD3	VSS3	27	
	45	VDD4	VSS4	39	
	57	VDD5	VSS5	51	
	69	VDD6	VSS6	63	
	93	VDD8	VSS8	87	
	113	VDD9	VSS9	103	
	131	VDD10	VSS10	125	
	143	VDD11	VSS11	137	
	155	VDD12	VSS12	149	
	157	VDD13	VSS13	159	
	167	VDD14	VSS14	161	
	179	VDD15	VSS15	173	
	191	VDD16	VSS16	185	
	10	VDD17	VSS17	4	
	22	VDD18	VSS18	16	
	34	VDD19	VSS19	28	
	36	VDD20	VSS20	38	
	46	VDD21	VSS21	40	
	58	VDD22	VSS22	52	
	70	VDD23	VSS23	64	
	92	VDD25	VSS25	88	
	94	VDD26	VSS26	90	
	114	VDD27	VSS27	104	
	132	VDD28	VSS28	126	
	144	VDD29	VSS29	138	
	156	VDD30	VSS30	150	
	168	VDD31	VSS31	162	
	180	VDD32	VSS32	174	
	192	VDD33	VSS33	186	
T59 1	199	VDDID	DU1	85	
3VDDM	197	VDDSPD	DU2	123	
(15,25) DDR_VREF	1	VREF1	DU3	124	
	2	VREF2	DU4	200	
			NC1	201	
			NC2	202	
			NC3	203	
			NC4	204	

C83 0.1uF 25V 80-20% 0603 Y5V
C429 0.1uF 25V 80-20% 0603 Y5V

CN 218PIN DUAL DDR SO-DIMM

(15,17,25,26,49) DDR_2.5VDDS

C510 1uF 6.3V 20% SANYO
C414 C485 C417 C412 C488 C484 C410 C485 C411 0.1uF 16V 10% 0603 X7R
C491 C419 C413 C489 C487 C490 C483 C415 C418 0.1uF 16V 10% 0603 X7R
C511 1uF 6.3V 20% SANYO

ES Modify

(15) SM_SDQS[7..0] SM_SDQS[7..0] >> SM_R_SDQS[7..0] (24)
(15) M_DM[7..0] M_DM[7..0] >> M_R_DM[7..0] (24)

SM_SDQS0 M_DM0	R467 R447	10 5% 1/16W 0402	SM_R_SDQS0 M_R_DM0
SM_SDQS1 M_DM1	R466 R446	10 5% 1/16W 0402	SM_R_SDQS1 M_R_DM1
SM_SDQS2 M_DM2	R465 R445	10 5% 1/16W 0402	SM_R_SDQS2 M_R_DM2
SM_SDQS3 M_DM3	R464 R444	10 5% 1/16W 0402	SM_R_SDQS3 M_R_DM3
SM_SDQS4 M_DM4	R463 R440	10 5% 1/16W 0402	SM_R_SDQS4 M_R_DM4
SM_SDQS5 M_DM5	R462 R443	10 5% 1/16W 0402	SM_R_SDQS5 M_R_DM5
SM_SDQS6 M_DM6	R461 R442	10 5% 1/16W 0402	SM_R_SDQS6 M_R_DM6
SM_SDQS7 M_DM7	R460 R441	10 5% 1/16W 0402	SM_R_SDQS7 M_R_DM7

11/5 Modify

FIC International Computer, Inc.
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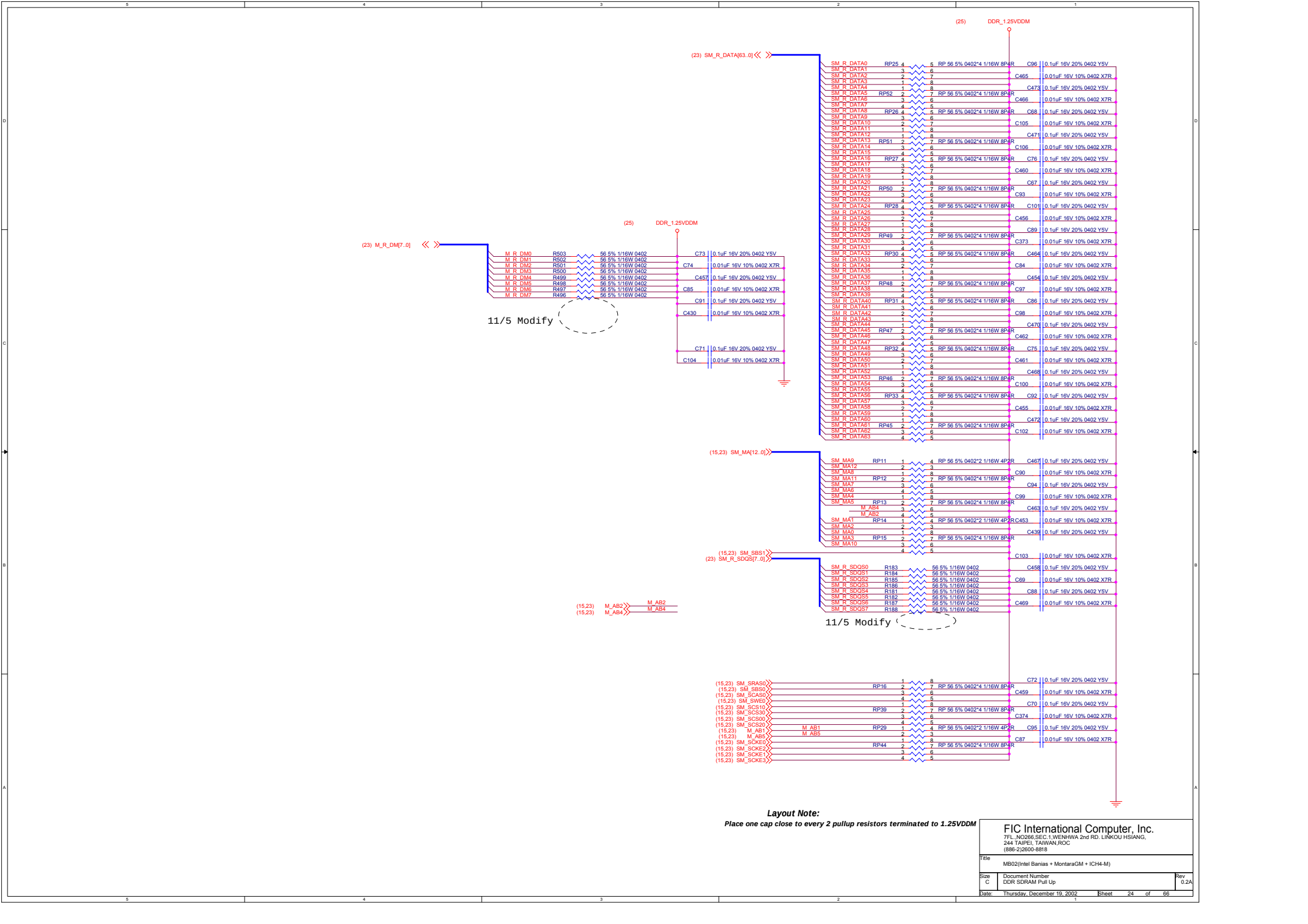
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

Title	MB02(Intel Banias + MontaraGM + ICH4-M)		
Size C	Document Number DDR SDRAM SO-DIMM		Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 23 of 66		

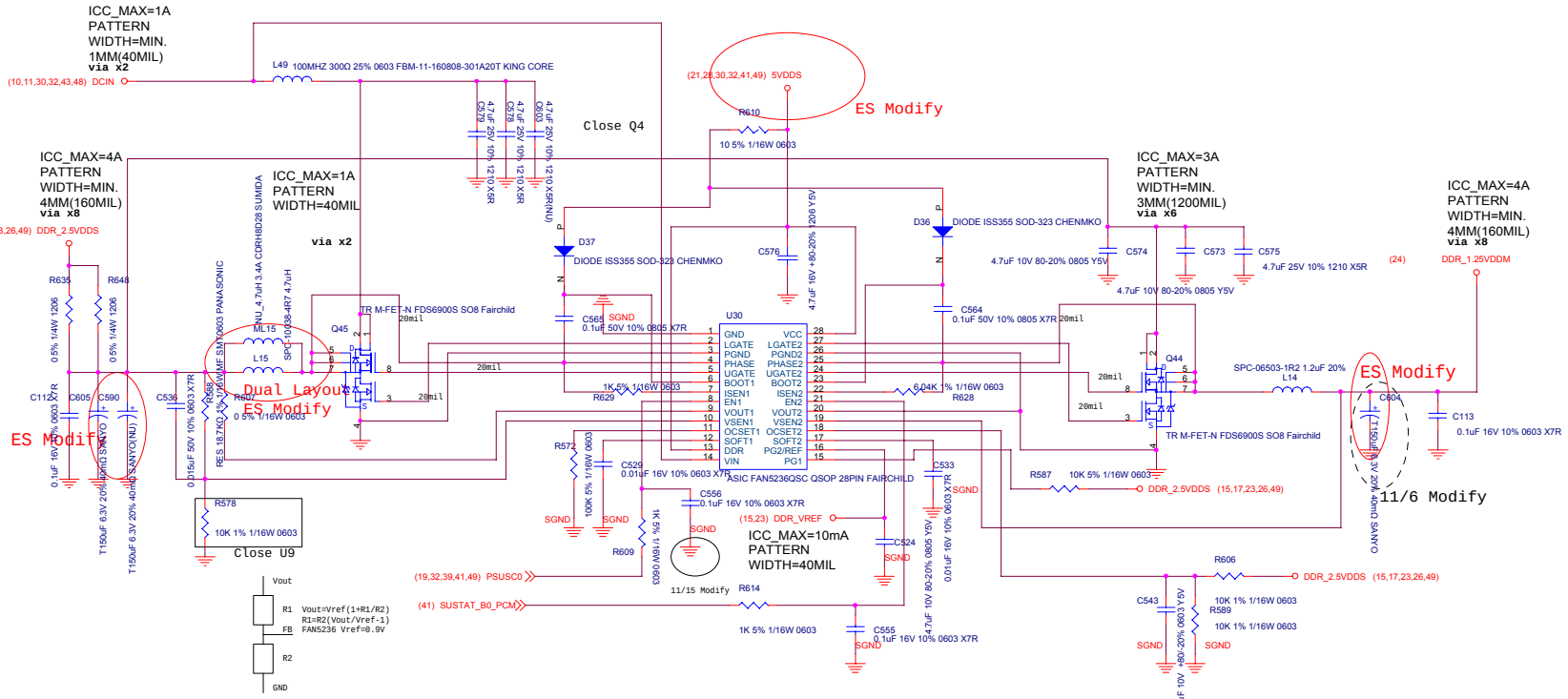


Layout Note:

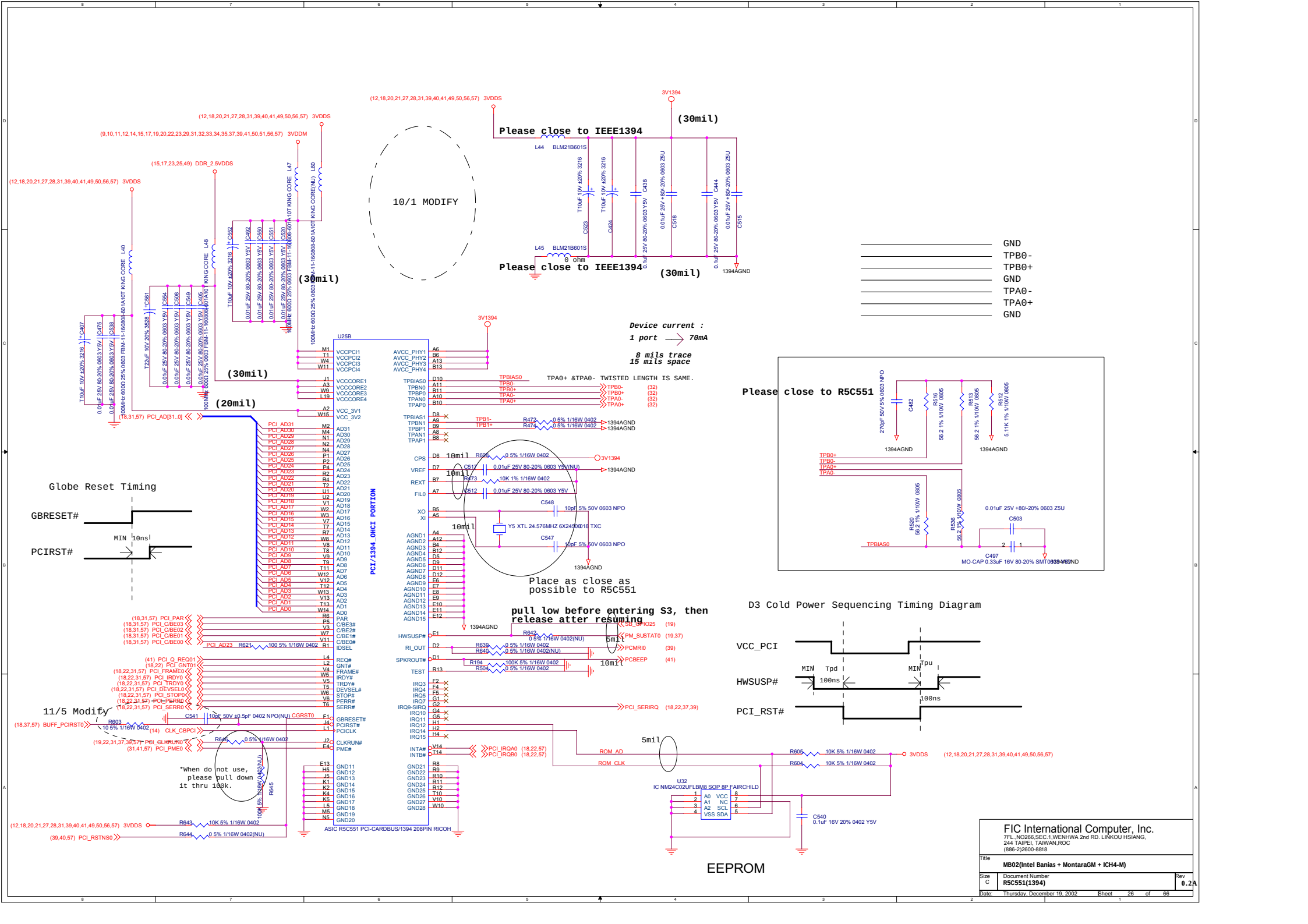
Place one cap close to every 2 pullup resistors terminated to 1.25VDDM

FIC International Computer, Inc.
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number DDR SDRAM Pull Up	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 24 of 66	



FIC International Computer, Inc.		
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC (886-2)2600-8818		
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number DDR SDRAM Power	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 25 of 66	



Title	MB02(Intel Banias + MontaraGM + ICH4-M)
Size	C
Document Number	R5C551(1394)
Rev	0.2A
Date:	Thursday, December 19, 2002
Sheet	26 of 66

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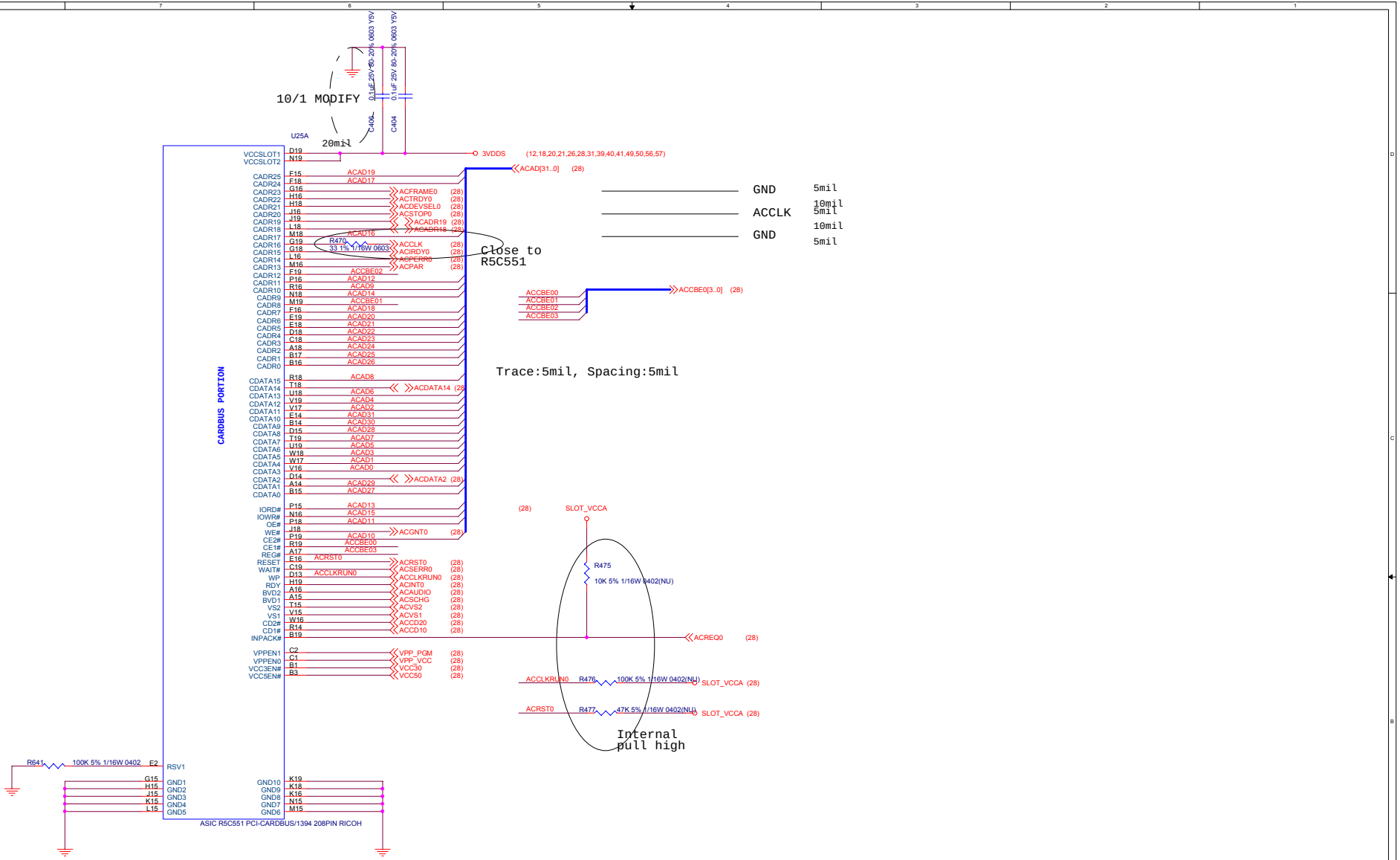

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7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
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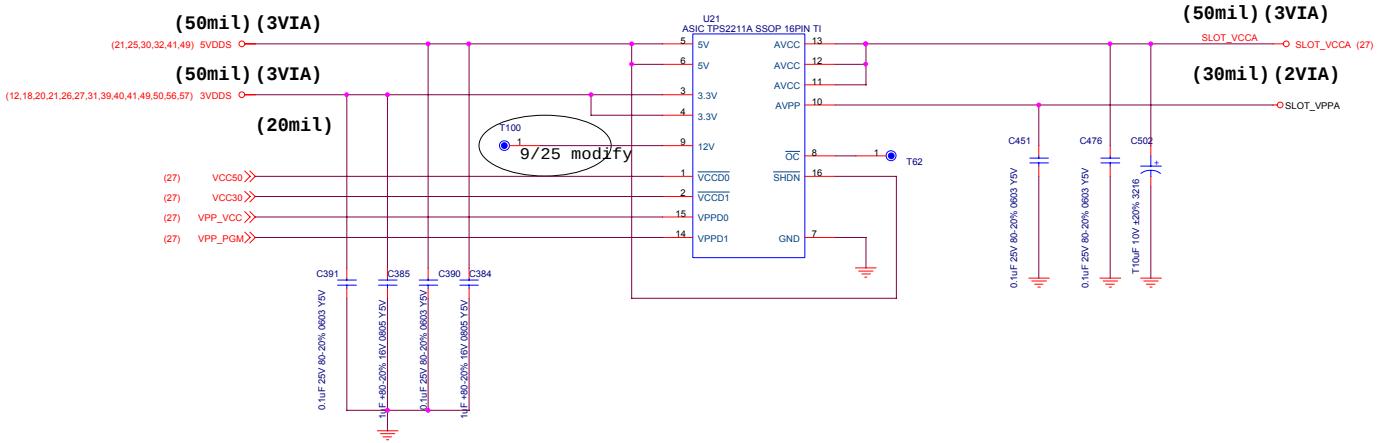
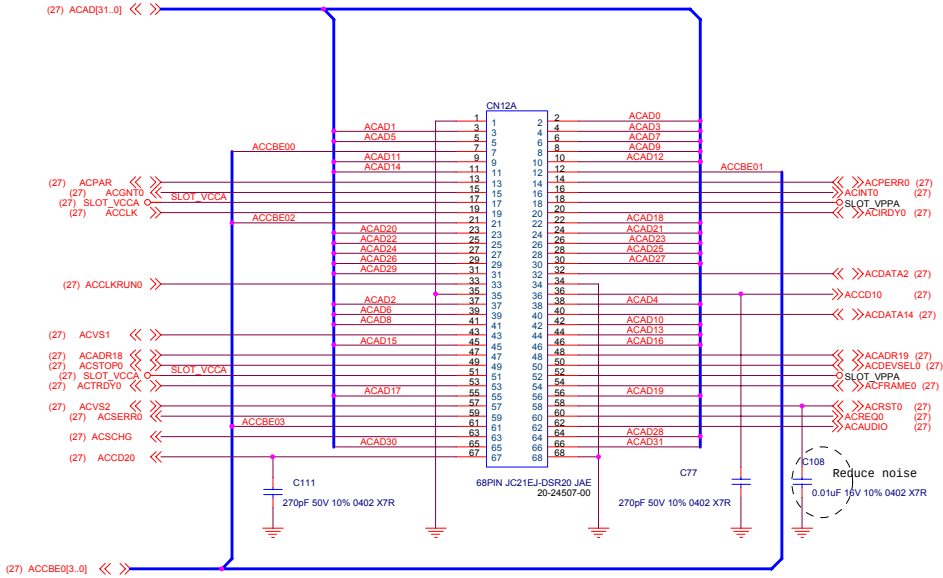
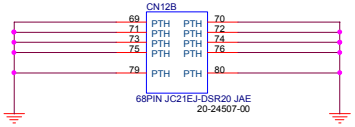
Title: MB02(Intel Banias + MontaraGM + ICH4-M)

Size: C | Document Number: R5C551(CardBus) | Rev: 0.2A

Date: Thursday, December 19, 2002 | Sheet 27 of 66







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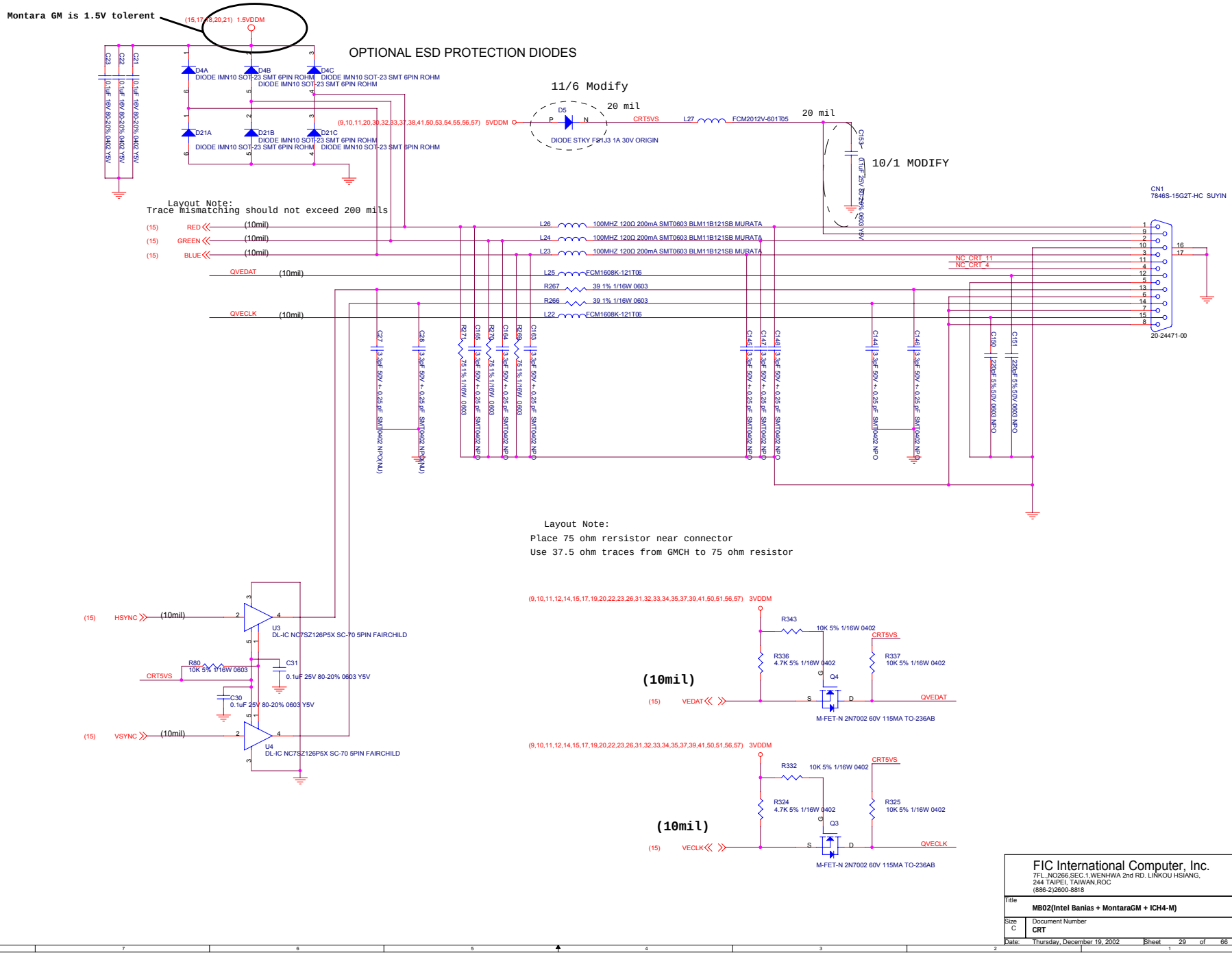
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Cardbus Power/CNN	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 28 of 66	

CRT CIRCUIT



FIC International Computer, Inc.
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
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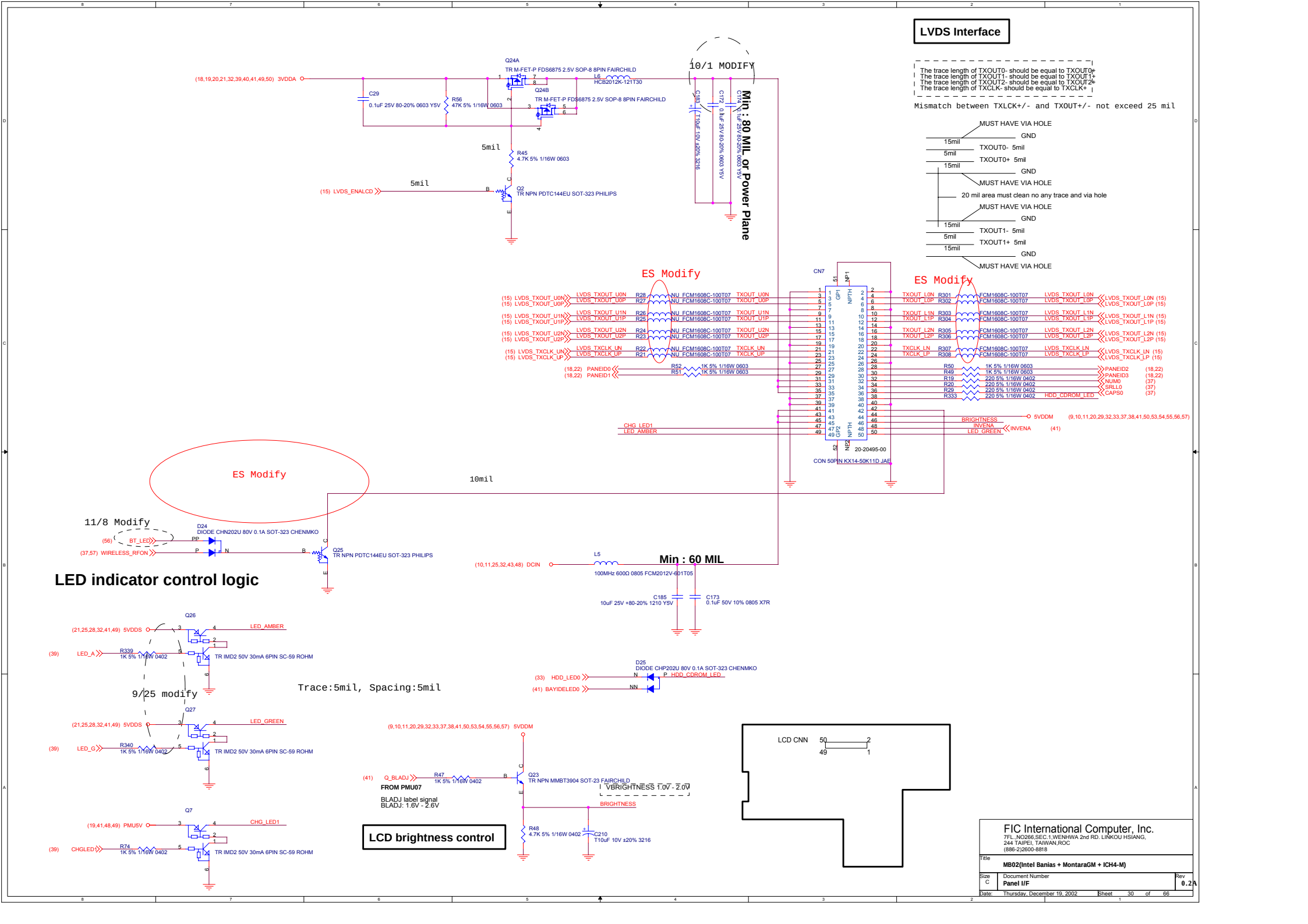
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number CRT	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 29 of 66	

LVDS Interface



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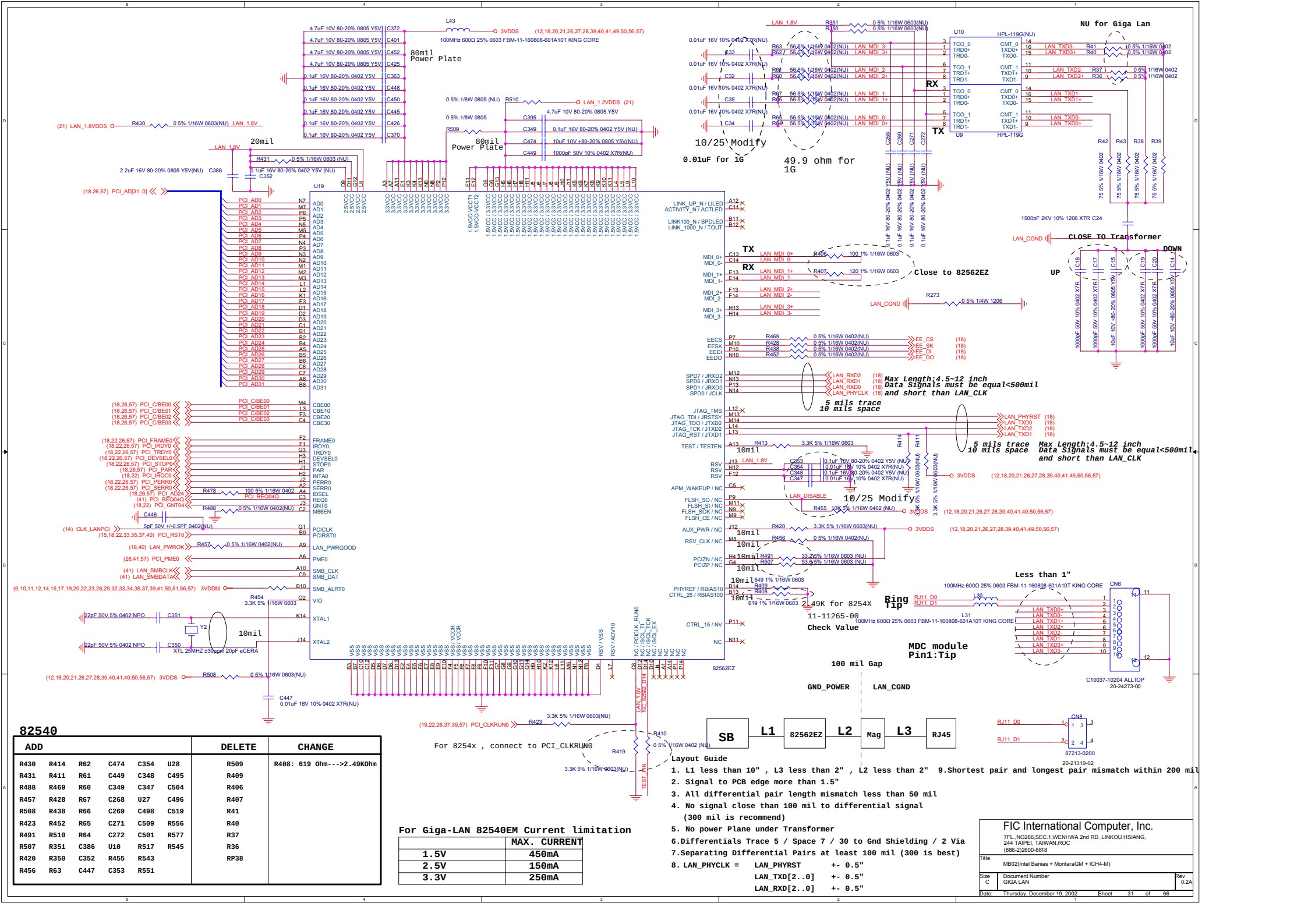
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Panel I/F	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 30 of 66	



ADD						DELETE	CHANGE
R430	R414	R62	C474	C354	U28	R509	R408: 619 Ohm--->2.49KOhm
R431	R411	R61	C449	C348	C495	R409	
R488	R469	R60	C349	C347	C504	R406	
R457	R428	R67	C268	U27	C496	R407	
R508	R438	R66	C269	C498	C519	R41	
R423	R452	R65	C271	C509	R556	R40	
R491	R510	R64	C272	C501	R577	R37	
R507	R351	C386	U10	R517	R545	R36	
R420	R350	C352	R455	R543		RP38	
R456	R63	C447	C353	R551			

	MAX. CURRENT
1.5V	450mA
2.5V	150mA
3.3V	250mA

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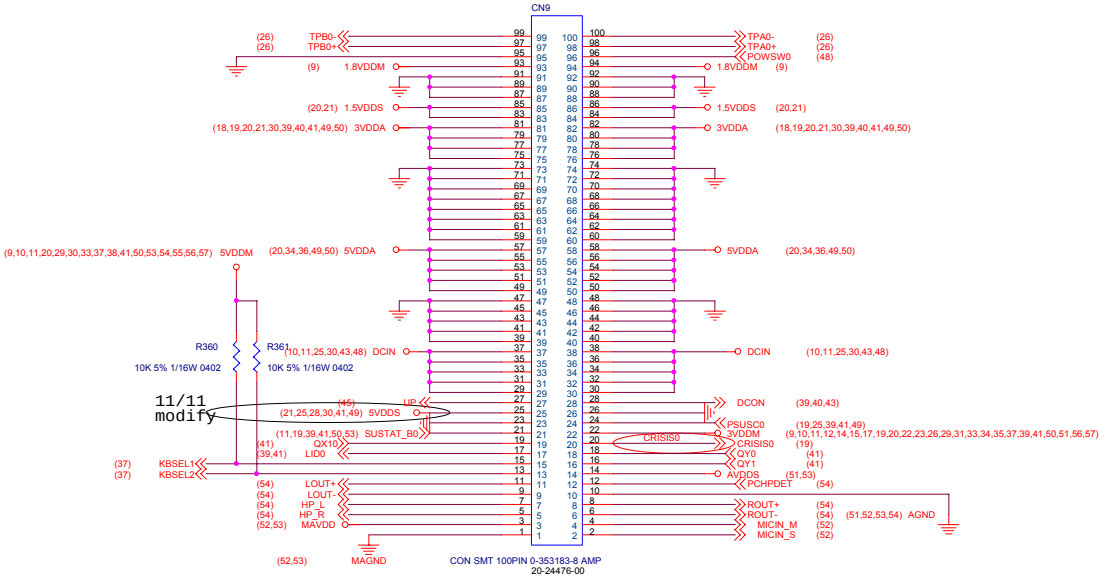
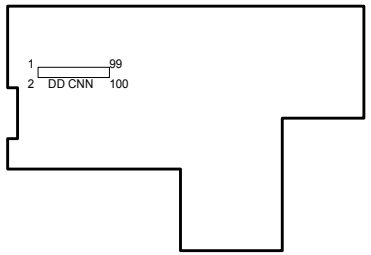
Title	MB02(Intel Banias + MontaraGM + ICH4-M)		
Size C	Document Number GIGA LAN		Rev 0.2A
Date: Thursday, December 19, 2002		Sheet 31 of 66	

Switch & D/D BOARD CNN

(5VDDA, 3VDDA, 1.5VDDS, 1.8VDDM)

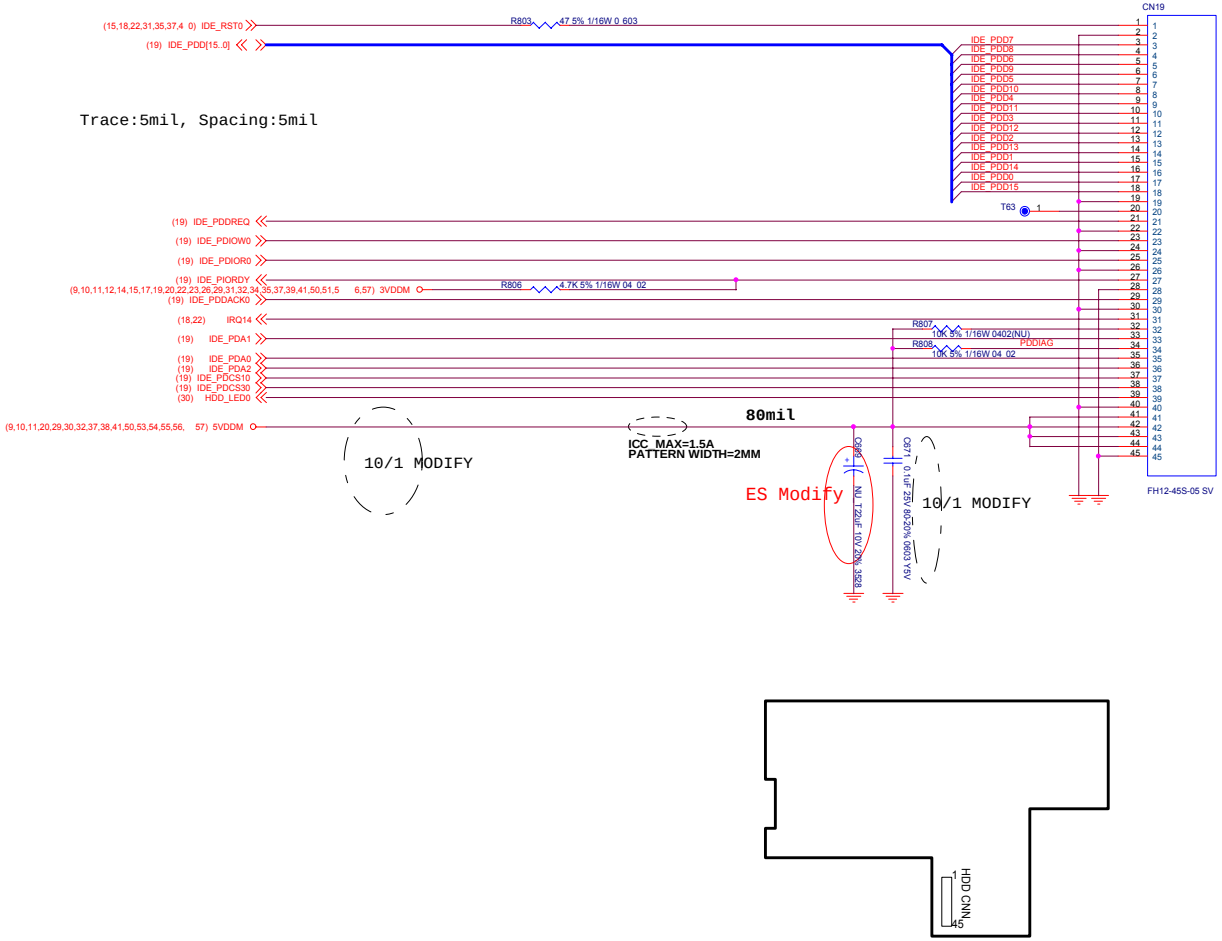
1 PIN 0.5A





FIC International Computer, Inc. 7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC (886-2)2600-8818		
Title: **MB02(Intel Banias + MontaraGM + ICH4-M)**		
Size: C	Document Number: **SW & DD CNN**	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 32 of 66	

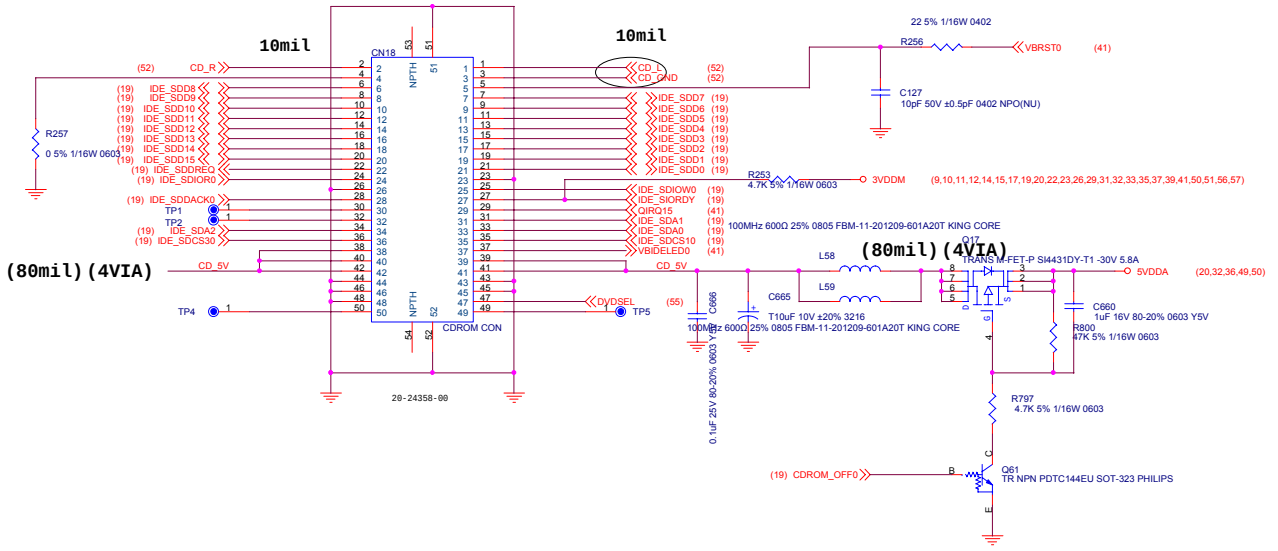
HDD I/F

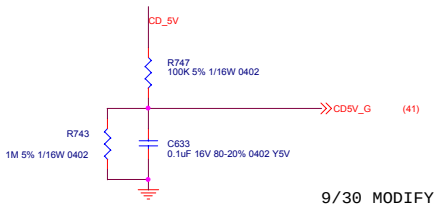


FIC International Computer, Inc. 7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC (886-2)2600-8818		
Title: MB02(Intel Banias + MontaraGM + ICH4-M)		
Size: C	Document Number: Primary IDE (HDD)	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 33 of 66	

CDROM CNN

Trace:5mil, Spacing:5mil





9/30 MODIFY

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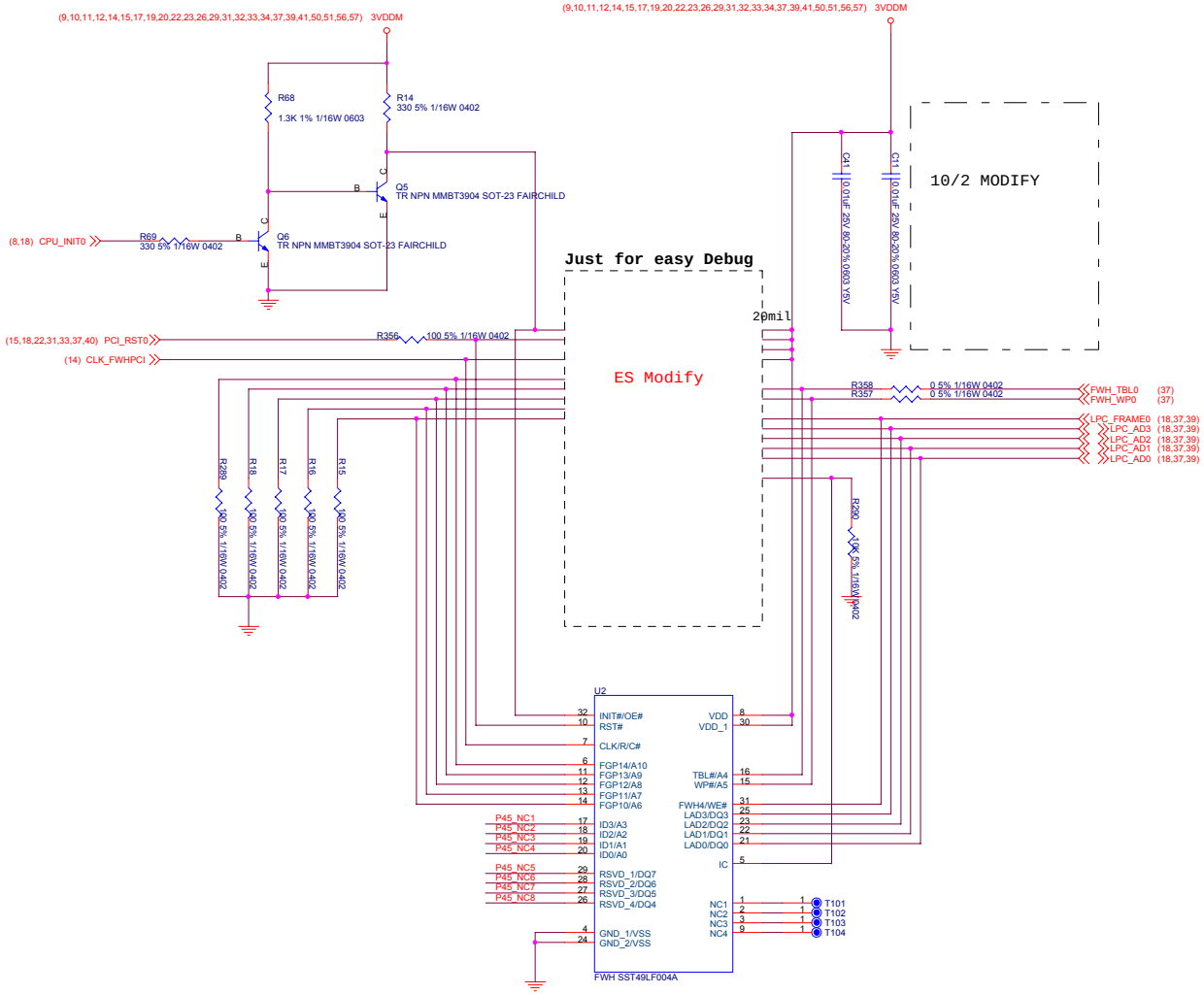
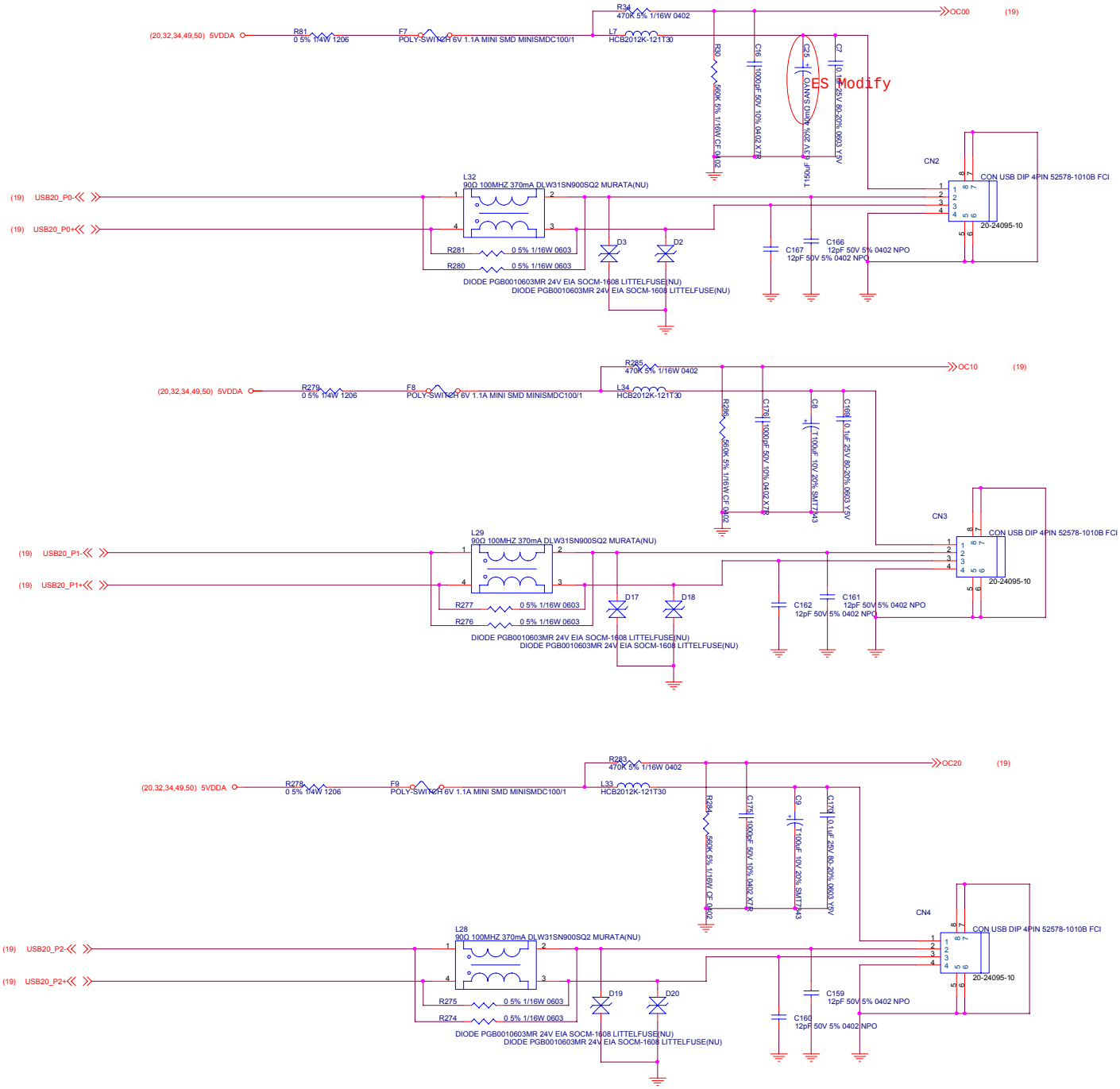
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number CDROM CNN	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 34 of 66	



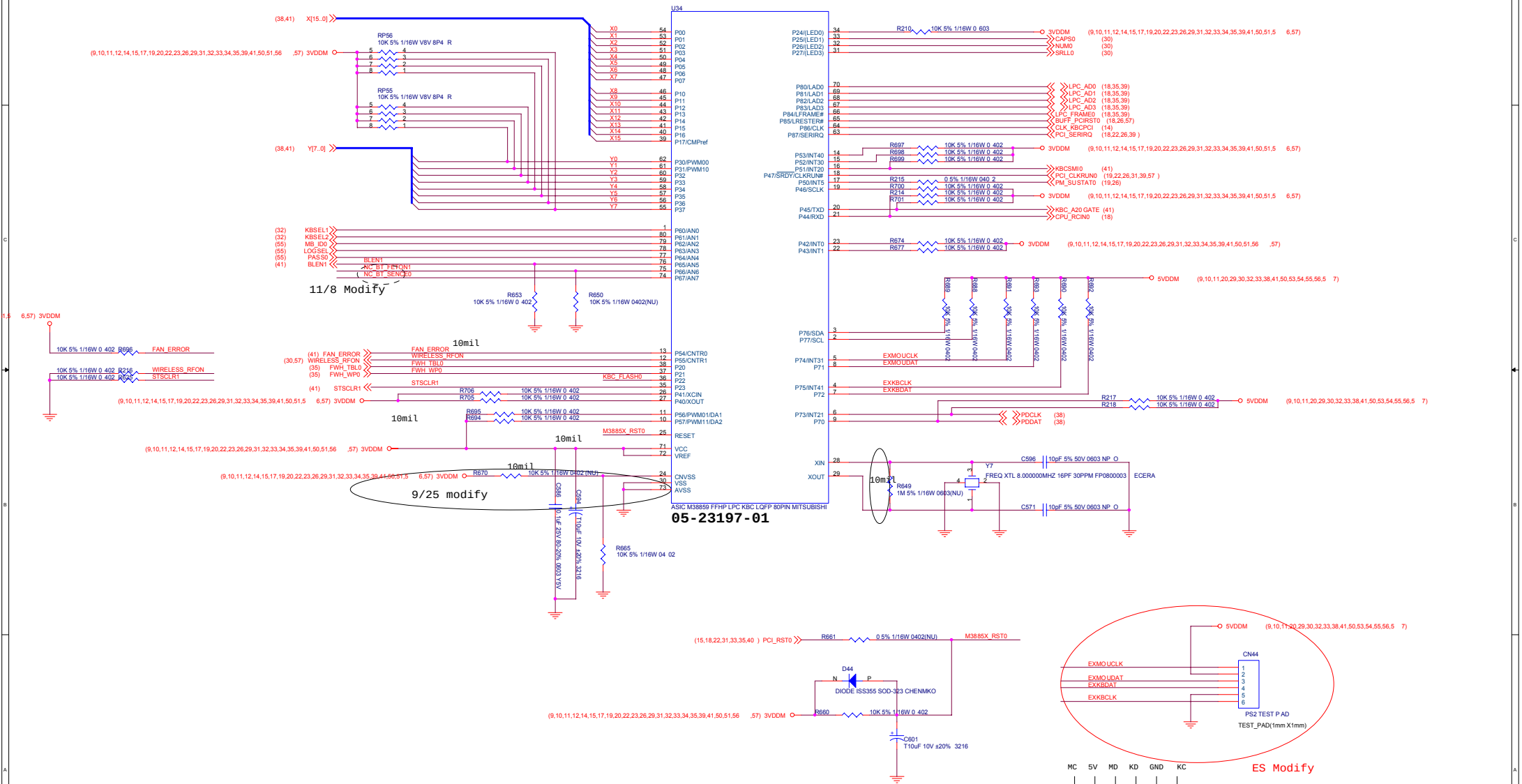
FIC International Computer, Inc. 7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC (886-2)2600-8818		
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number FirmWare Hub	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 35 of 66	



FIC International Computer, Inc.
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

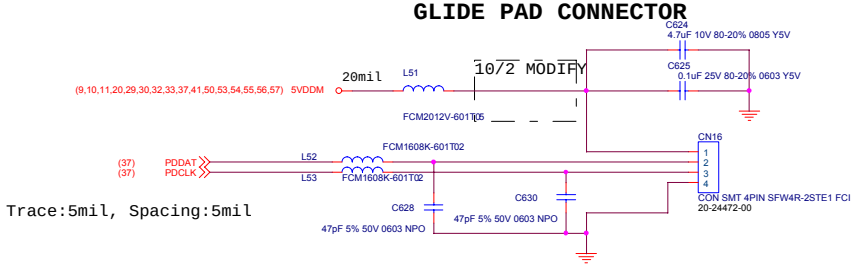
Title	**MB02(Intel Banias + MontaraGM + ICH4-M)**	
Size C	Document Number **USB2.0 CN x 3**	Rev **0.2A**
Date: Thursday, December 19, 2002	Sheet 36 of 66	

Trace:5mil, Spacing:5mil



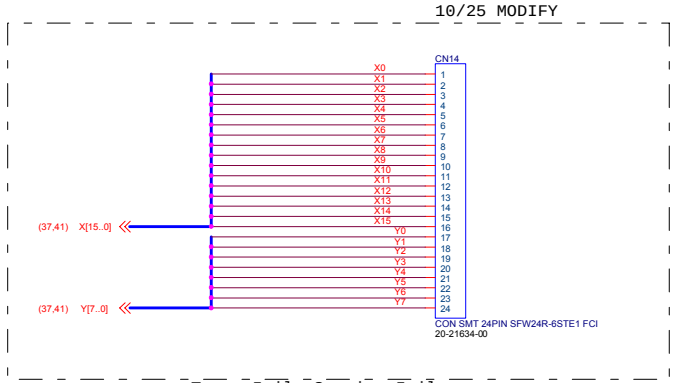
FIC International Computer, Inc.	
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC (886-2)2600-8818	
Title	MB02(Intel Banias + MontaraGM + ICH4-M)
Size C	Document Number KBC M38869
Rev	0.2A
Date: Thursday, December 19, 2002	Sheet 37 of 66

GLIDE PAD CONNECTOR



Trace:5mil, Spacing:5mil

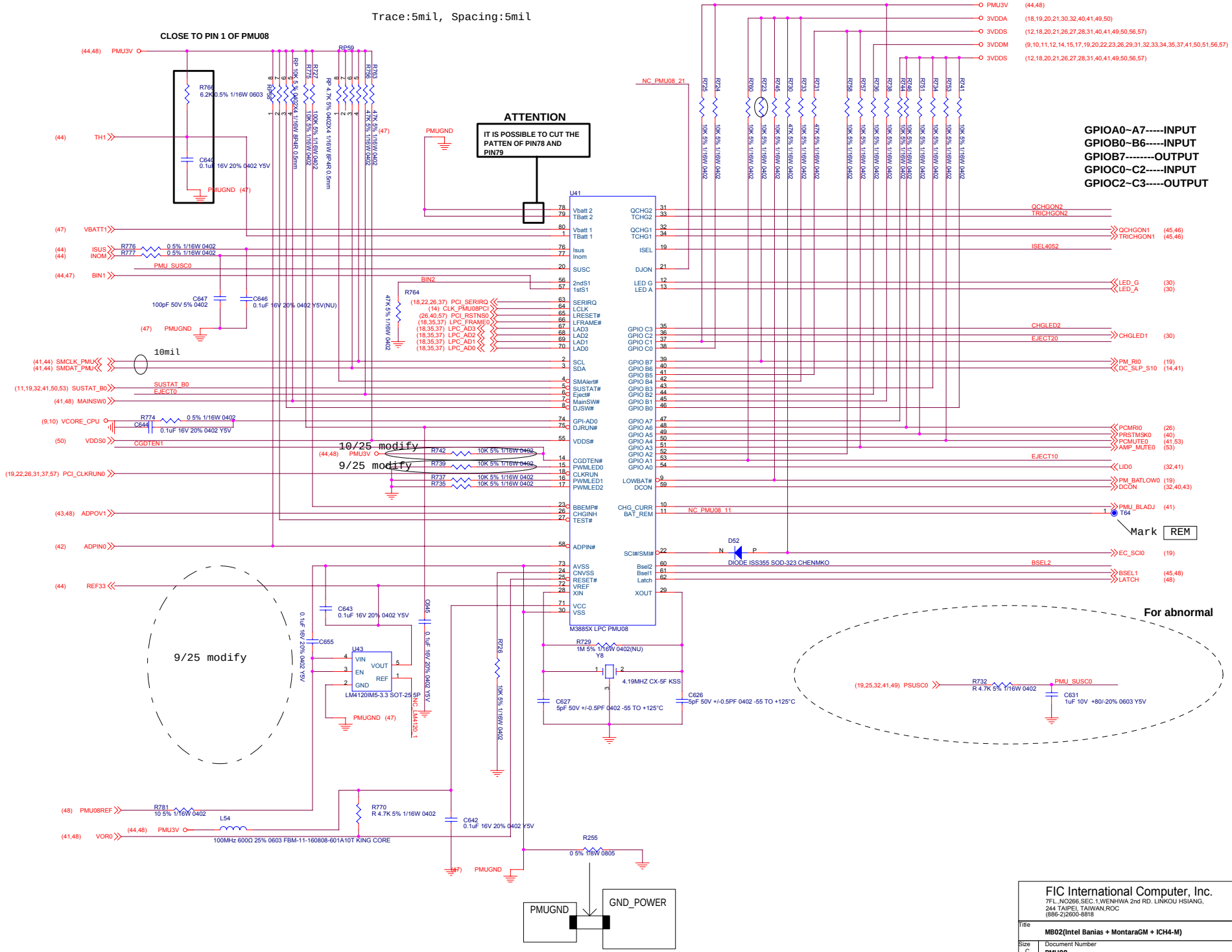
INT KB CNN

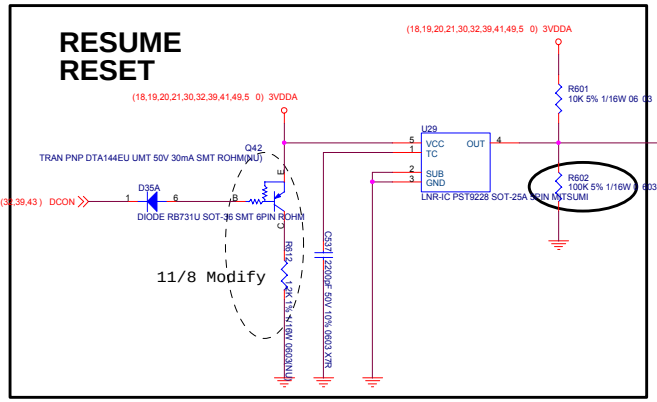


Trace:5mil, Spacing:5mil

FIC International Computer, Inc.
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

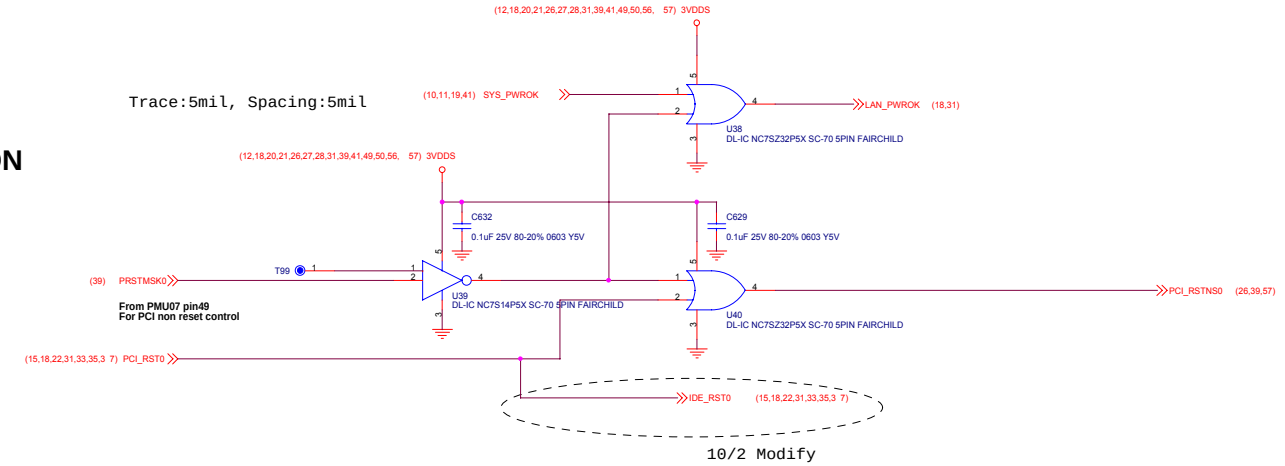
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Glide Pad/INT KB	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 38 of 66	


Trace:5mil, Spacing:5mil
CLOSE TO PIN 1 OF PMU08
ATTENTION
IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79
GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT
U41
M3885X LPC PMU08
10/25 modify
9/25 modify
10mil
For abnormal
Mark REM
D52
DIODE ISS355 SOD-323 CHENMKO
LM4120IM5-3.3 SOT-25 5P
100MHz 600Ω 25% 0603 FBM-11-160808-601A10T KING CORE
4.19MHZ CX-5F KSS
PMUGND
GND_POWER
FIC International Computer, Inc.
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG, 244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818
MB02(Intel Banias + MontaraGM + ICH4-M)
PMU08
0.2A
Thursday, December 19, 2002
Sheet 39 of 66



WORKAROUND FOR POWER CONTROL SIGNAL

PCI RESET & PCI NON RESET



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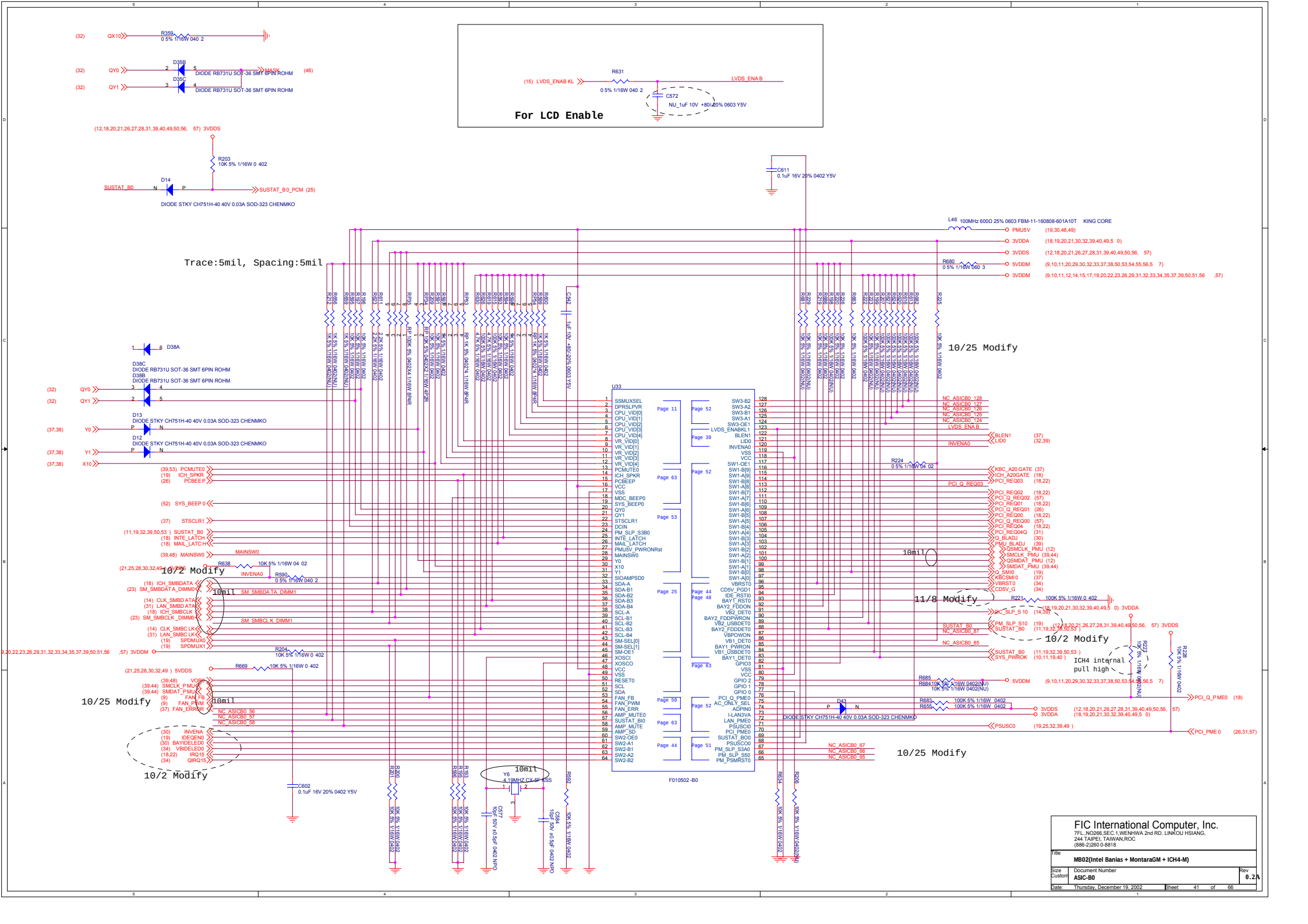
(886-2)260 0-8818

Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Reset Control Logic	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 40 of 66	


For LCD Enable
R631
0 5% 1/16W 040 2
C572
NU_1uF 10V +80/-20% 0603 Y5V
LVDS_ENA B
Trace:5mil, Spacing:5mil
10/25 Modify
10/2 Modify
11/8 Modify
ICH4 internal pull high
U33
F010502-B0
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(886-2)260 0-8818
MB02(Intel Banias + MontaraGM + ICH4-M)
ASIC-B0
0.2A
Thursday, December 19, 2002
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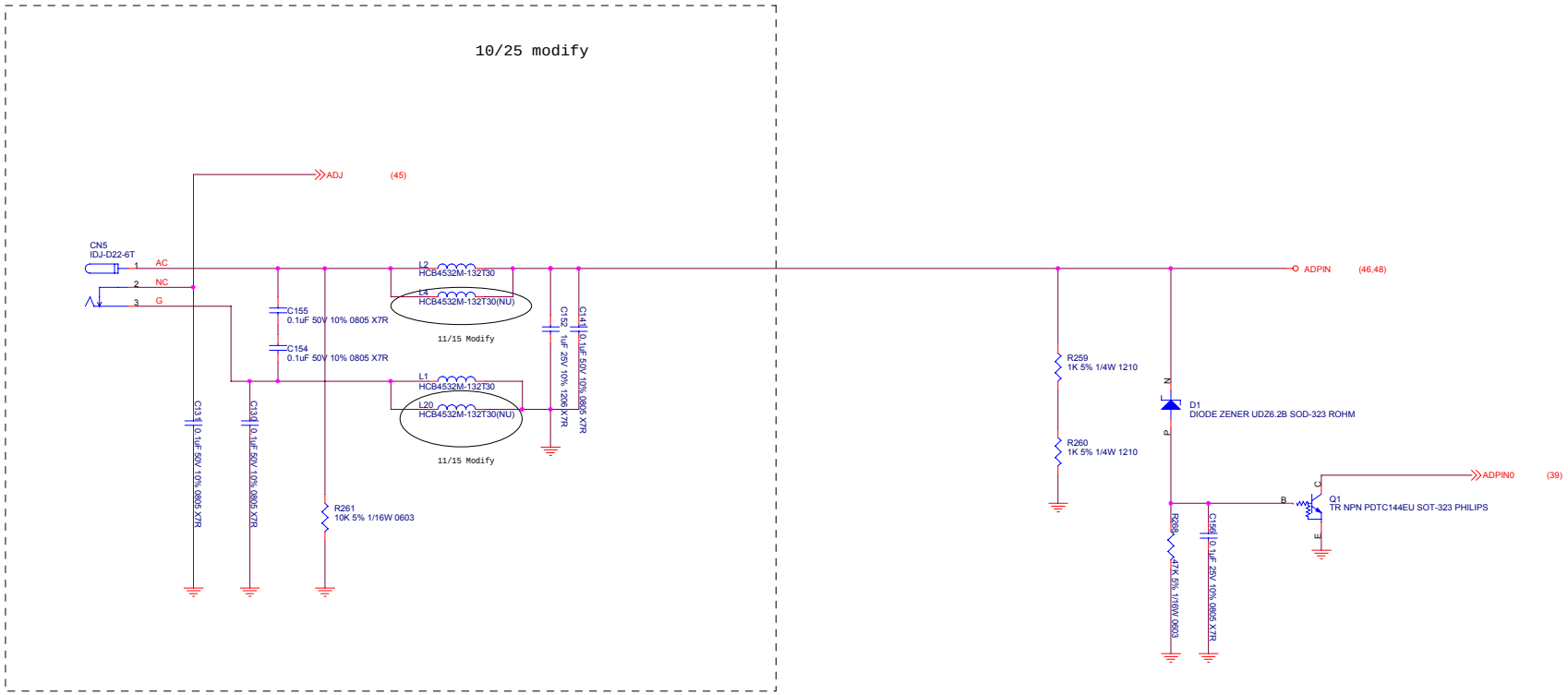

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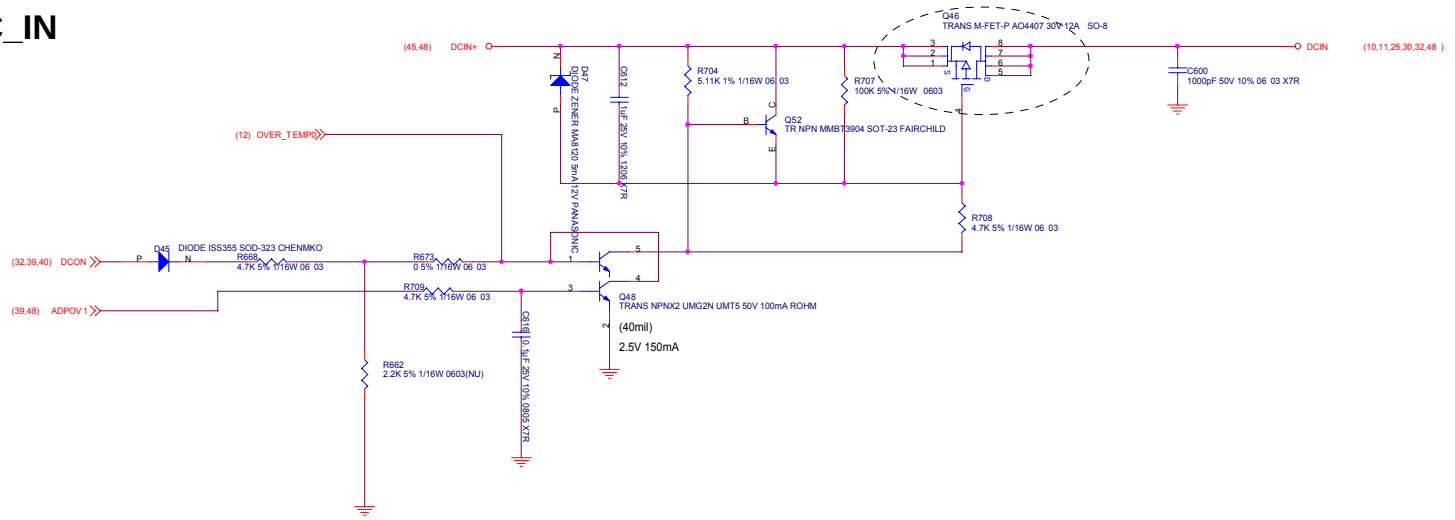
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number ACIN	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 42 of 66	

DC_IN

11/6 Modify



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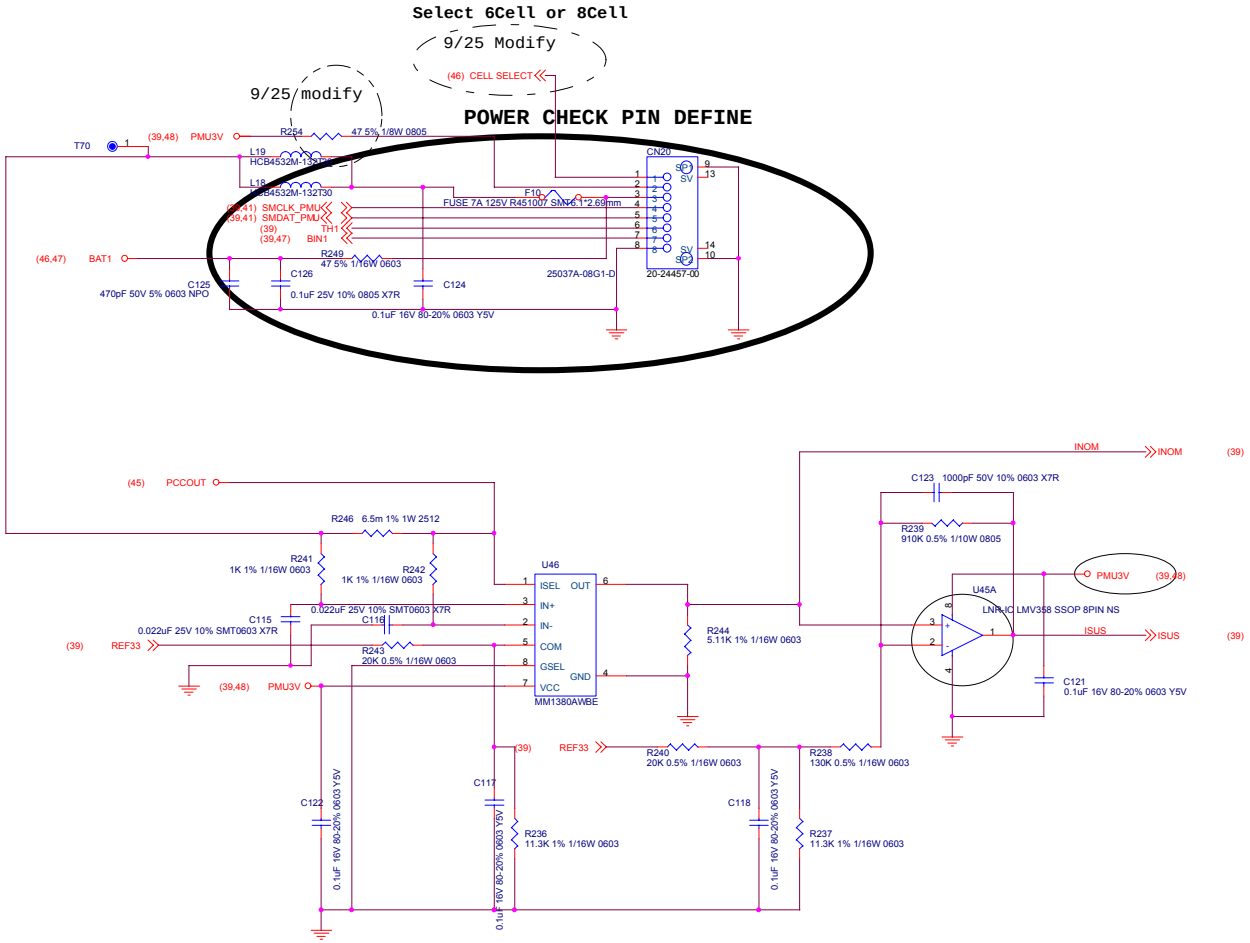
Title: **MB02(Intel Banias + MontaraGM + ICH4-M)**

Size	Document Number	Rev
C	**DCIN**	**0.2A**

Date: Thursday, December 19, 2002 Sheet 43 of 66



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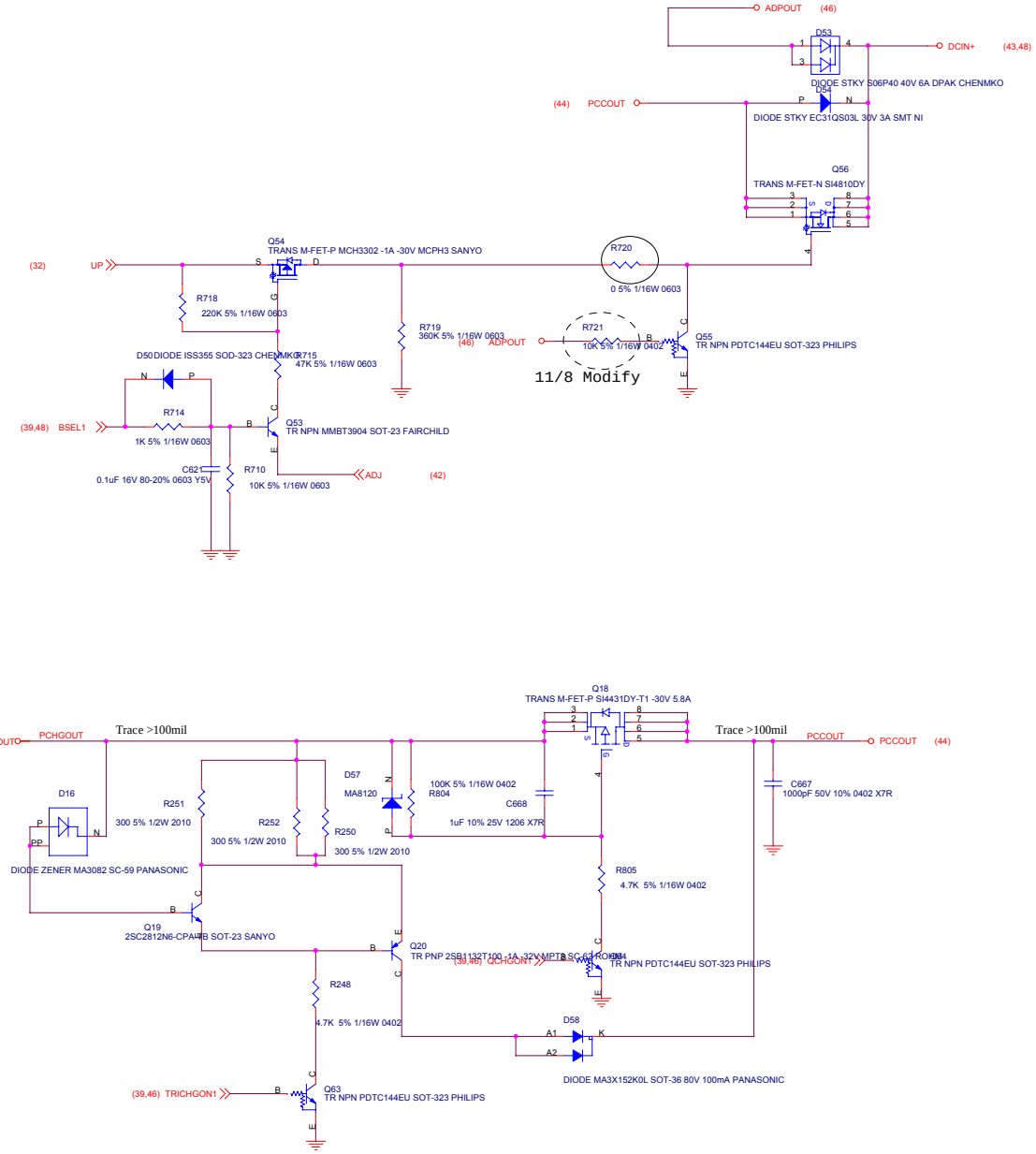
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Main Battery CNN	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 44 of 66	



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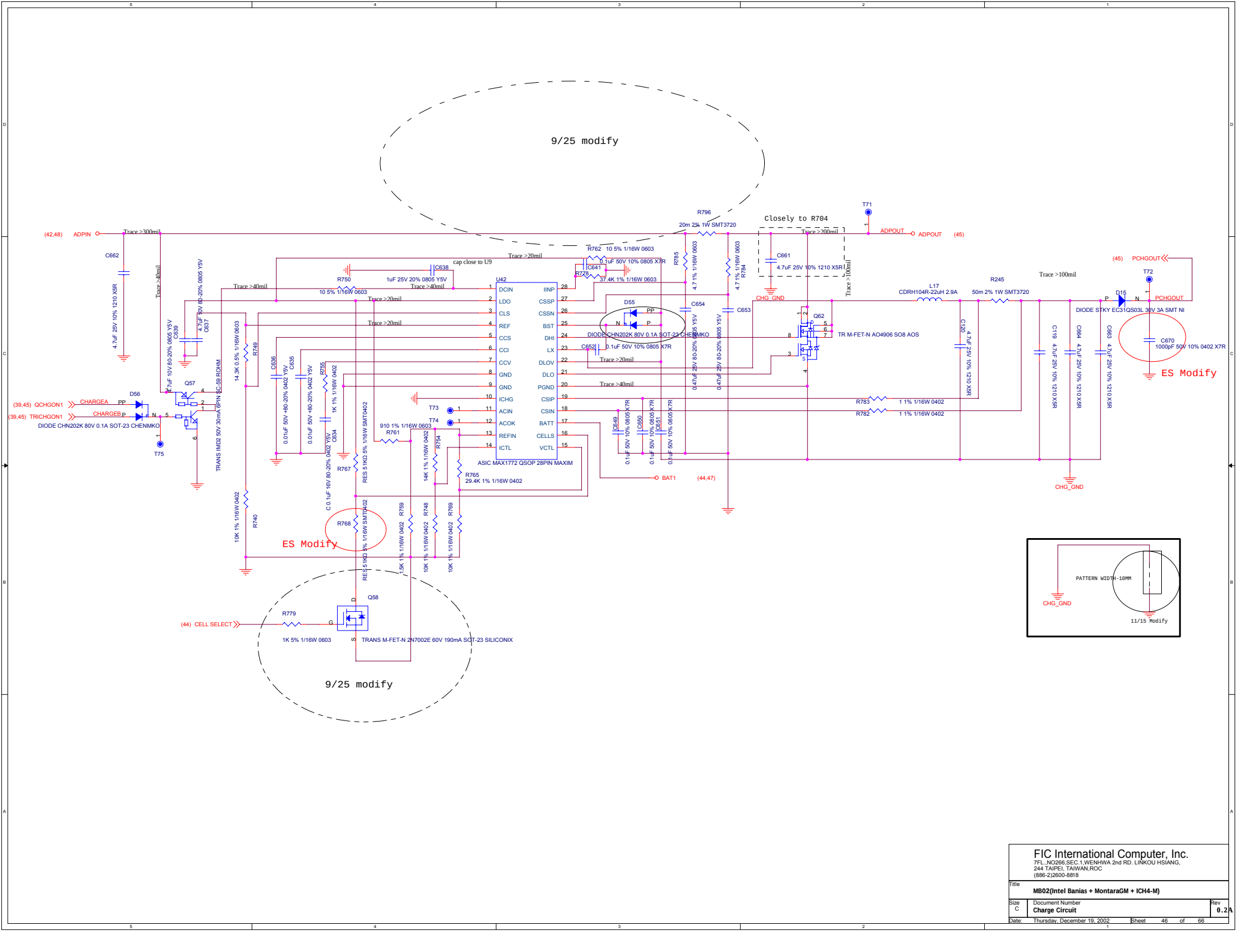
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Battery Select	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 45 of 66	



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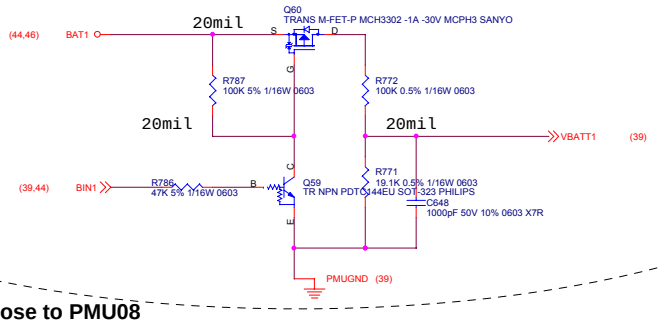
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number Charge Circuit	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 46 of 66	

MAIN BATTERY VOLTAGE SENSE



Close to PMU08

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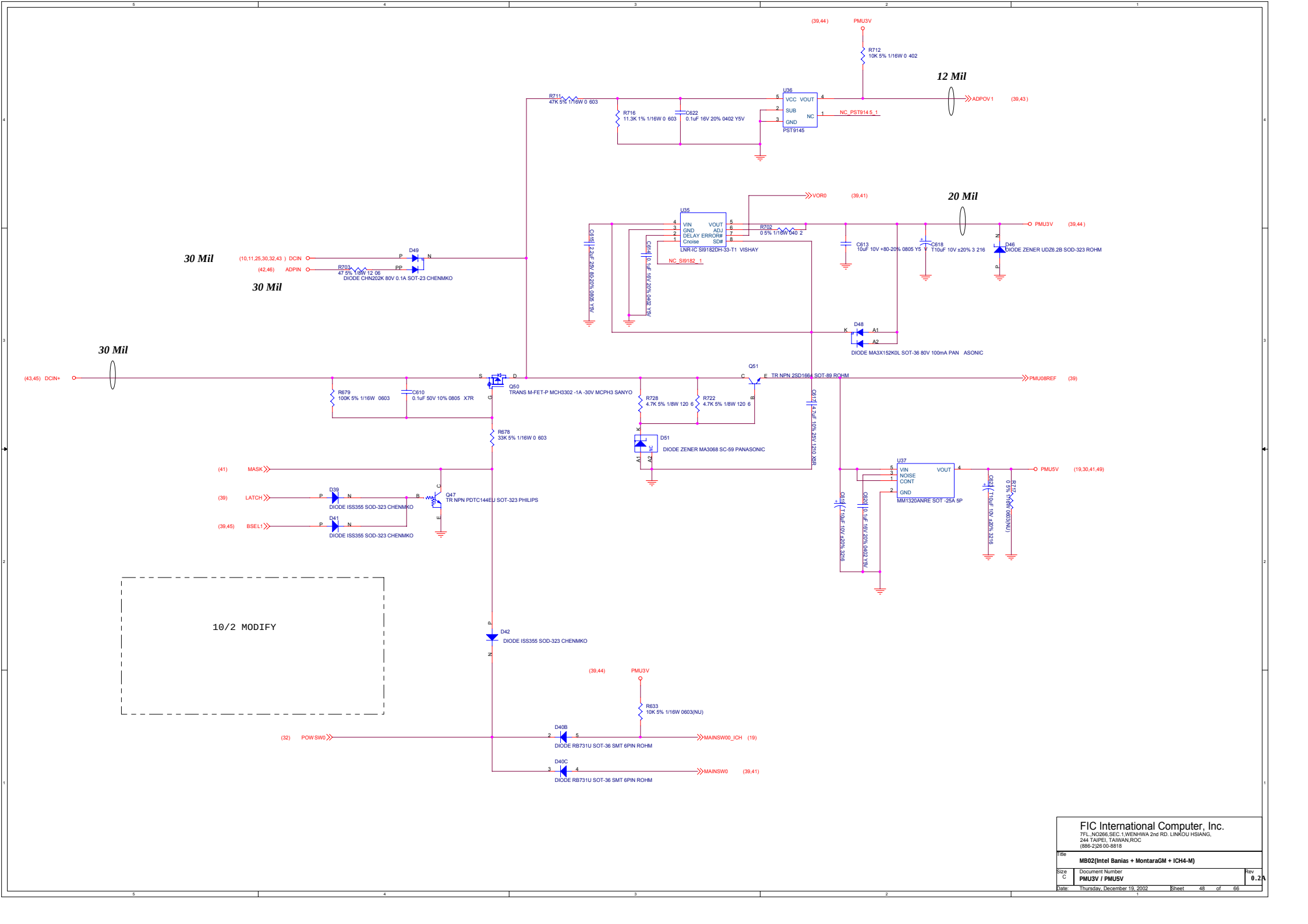
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Battery Voltage Sense	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 47 of 66	



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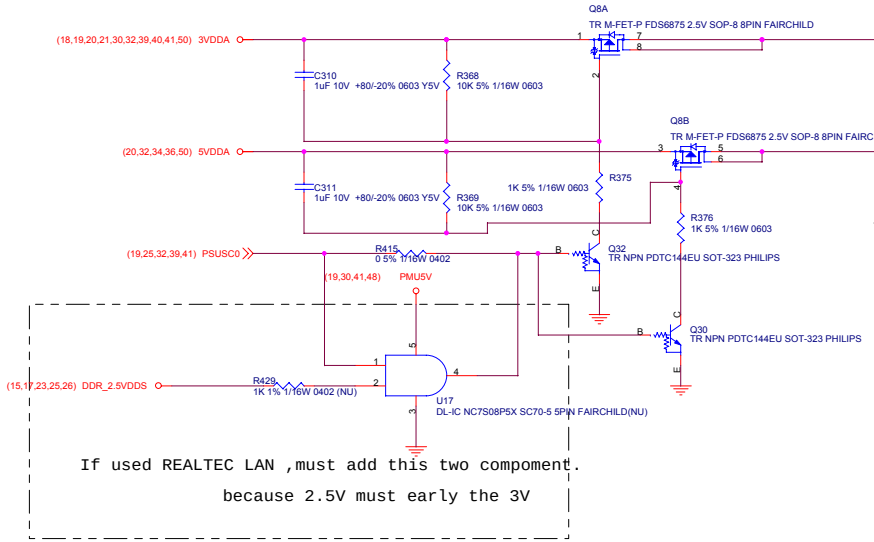
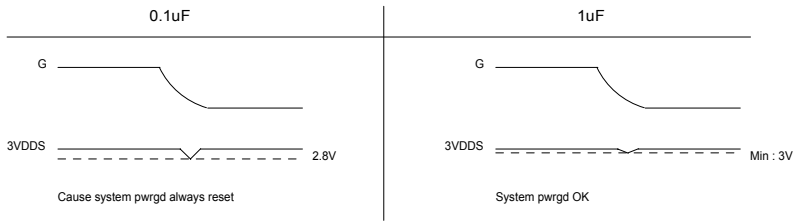
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number PMU3V / PMU5V	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 48 of 66	

3VDDS & 5VDDS

10/12 Modify





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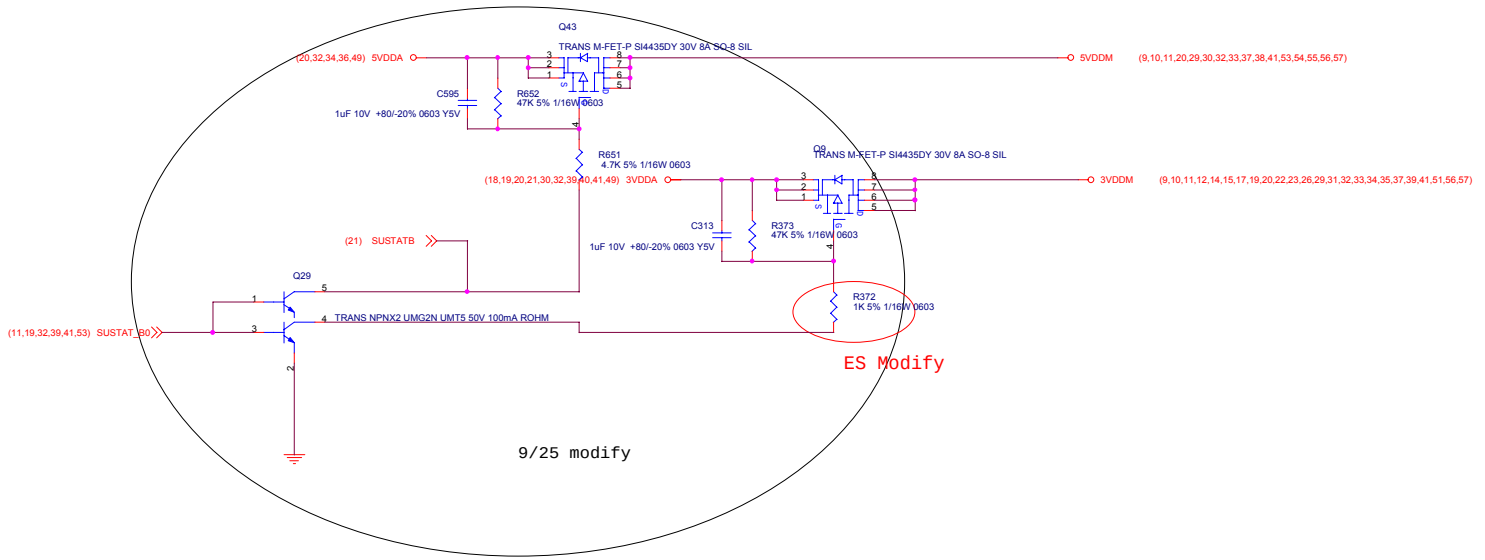
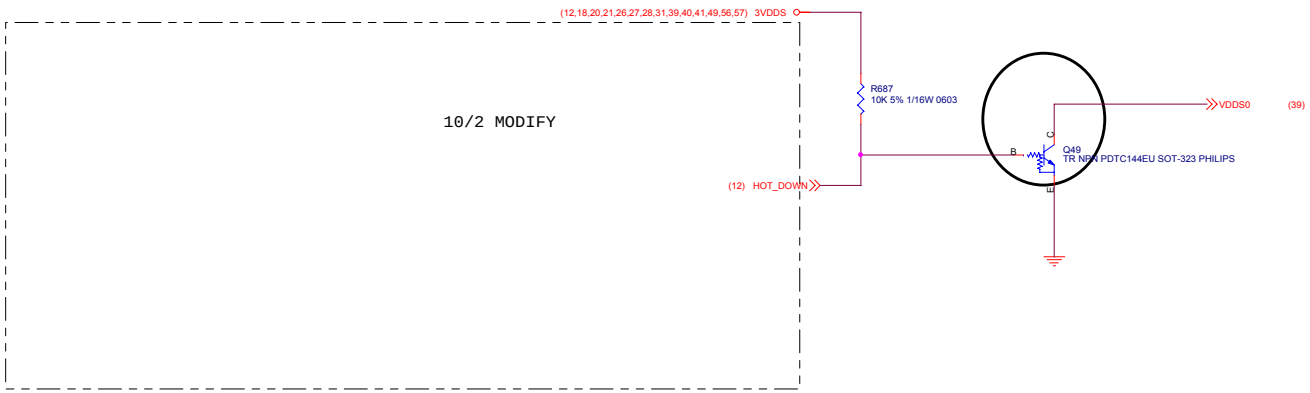
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number: Power (3VDDS / 5VDDS)	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 49 of 66	

3VDDM/5VDDM





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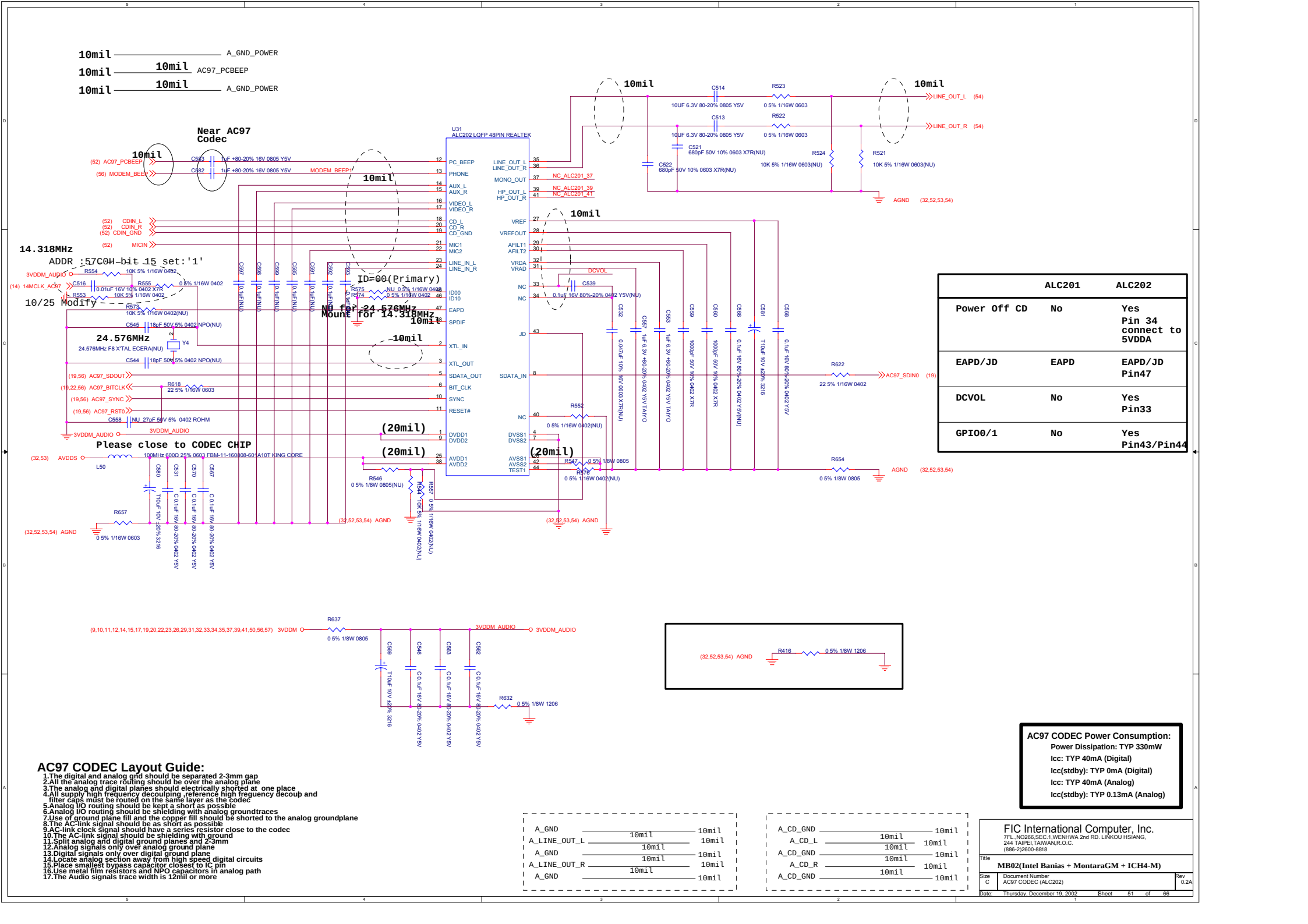
Title: MB02(Intel Banias + MontaraGM + ICH4-M)		
Size: C	Document Number: Power (3VDDM / 5VDDM) & over voltage protect	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 50 of 66	



	ALC201	ALC202
Power Off CD	No	Yes Pin 34 connect to 5VDDA
EAPD/JD	EAPD	EAPD/JD Pin47
DCVOL	No	Yes Pin33
GPIO0/1	No	Yes Pin43/Pin44

AC97 CODEC Layout Guide:

1. The digital and analog gnd should be separated 2-3mm gap
2. All the analog trace routing should be over the analog plane
3. The analog and digital planes should electrically shorted at one place
4. All supply high frequency decoulping ,reference high freguency decoup and filter caps must be routed on the same layer as the codec
5. Analog I/O routing should be kept a short as possible
6. Analog I/O routing should be shielding with analog groundtraces
7. Use of ground plane fill and the copper fill should be shorted to the analog groundplane
8. The AC-link signal should be as short as possible
9. AC-link clock signal should have a series resistor close to the codec
10. The AC-link signal should be shielding with ground
11. Split analog and digital ground planes and 2-3mm
12. Analog signals only over analog ground plane
13. Digital signals only over digital ground plane
14. Locate analog section away from high speed digital circuits
15. Place smallest bypass capacitor closest to IC pin
16. Use metal film resistors and NPO capacitors in analog path
17. The Audio signals trace width is 12mil or more

AC97 CODEC Power Consumption:

- Power Dissipation: TYP 330mW
- Icc: TYP 40mA (Digital)
- Icc(stdby): TYP 0mA (Digital)
- Icc: TYP 40mA (Analog)
- Icc(stdby): TYP 0.13mA (Analog)

A_GND — A_LINE_OUT_L — A_GND — A_LINE_OUT_R — A_GND (10mil)

A_CD_GND — A_CD_L — A_CD_GND — A_CD_R — A_CD_GND (10mil)

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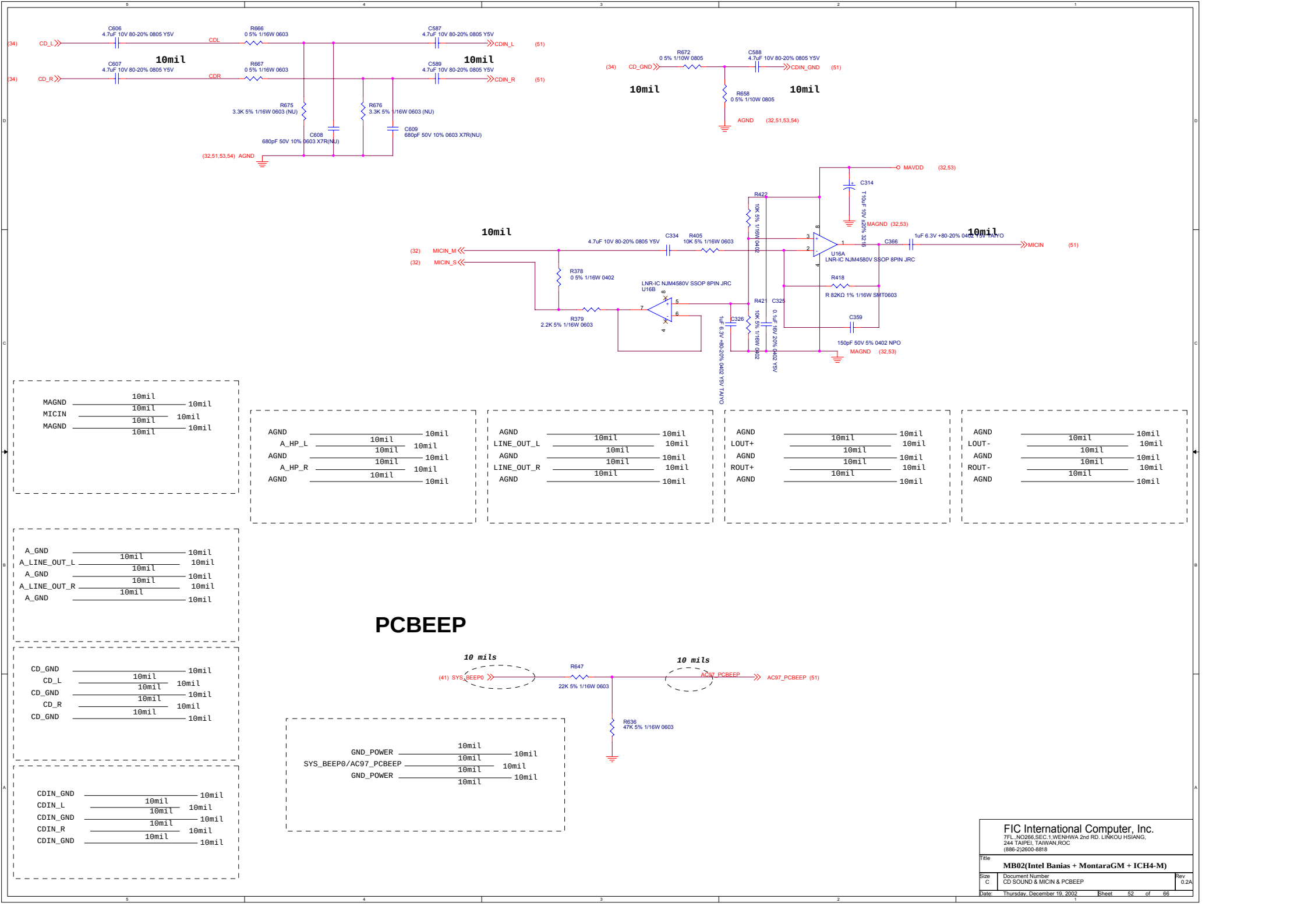
Title: **MB02(Intel Banias + MontaraGM + ICH4-M)**

Size	Document Number	Rev
C	AC97 CODEC (ALC202)	0.2A

Date: Thursday, December 19, 2002 Sheet 51 of 66



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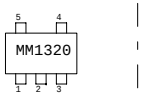
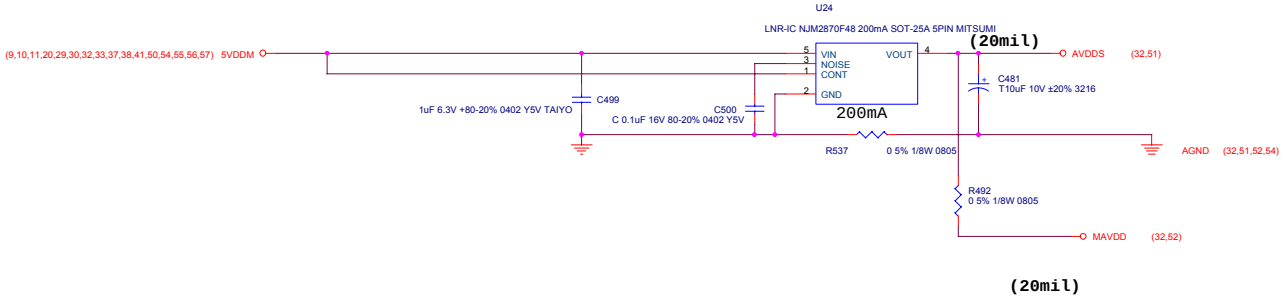
Title: **MB02(Intel Banias + MontaraGM + ICH4-M)**

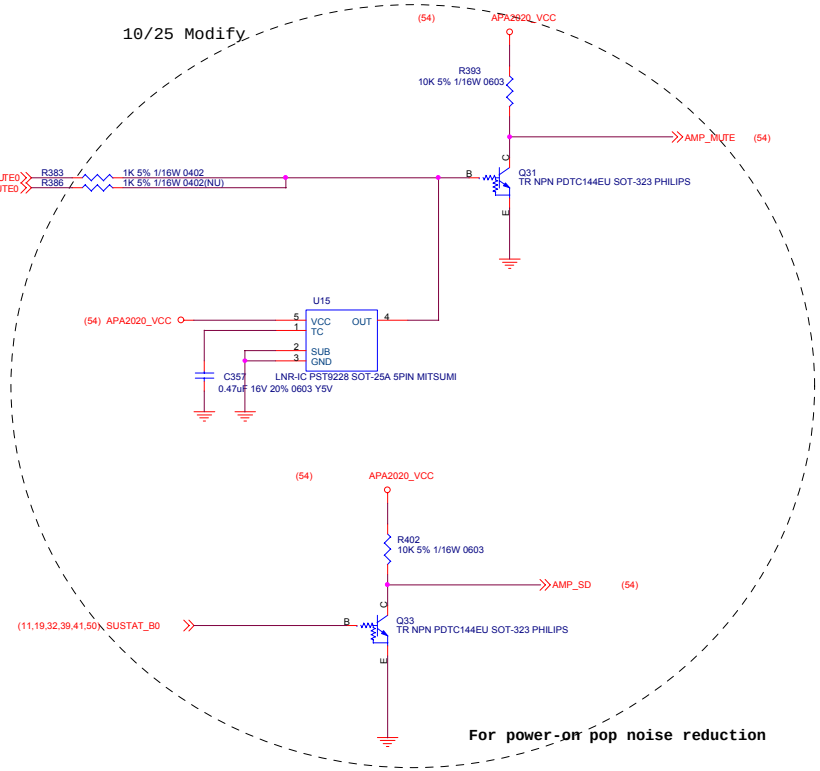
Size	Document Number	Rev
C	CD SOUND & MICIN & PCBEEP	0.2A

Date: Thursday, December 19, 2002 Sheet 52 of 66

Cont	Vont
L	OFF
H	ON







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Title: **MB02(Intel Banias + MontaraGM + ICH4-M)**

Size	Document Number	Rev
C	AUDIO POWER & SD	0.2A

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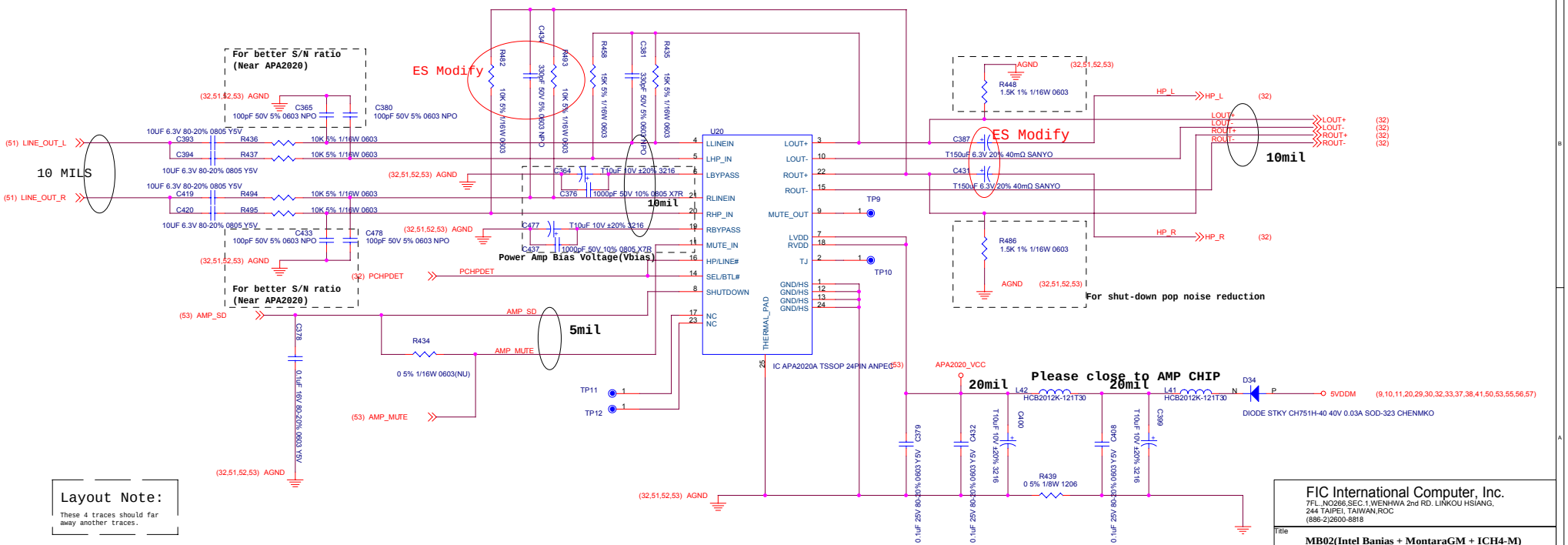
10/2 MODIFY
Delete SPDIF



Layout Note:
These 4 traces should far away another traces.

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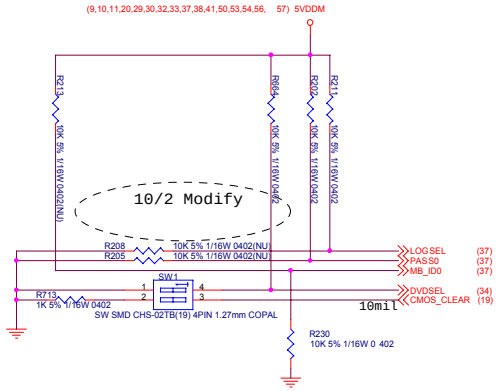
Title: MB02(Intel Banias + MontaraGM + ICH4-M)		
Size: C	Document Number: AMP TPA2020	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 54 of 66	

DIP SWITCH



Trace:5mil, Spacing:5mil

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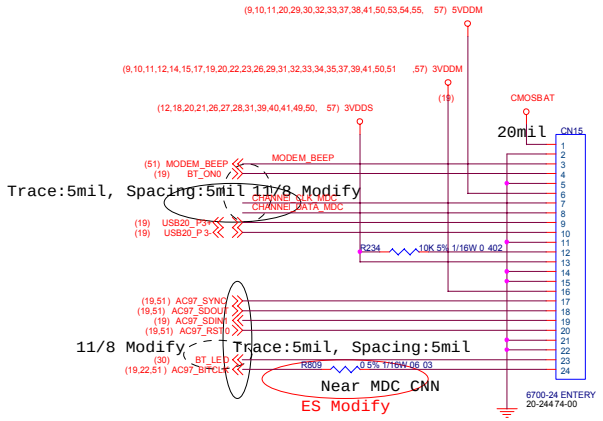
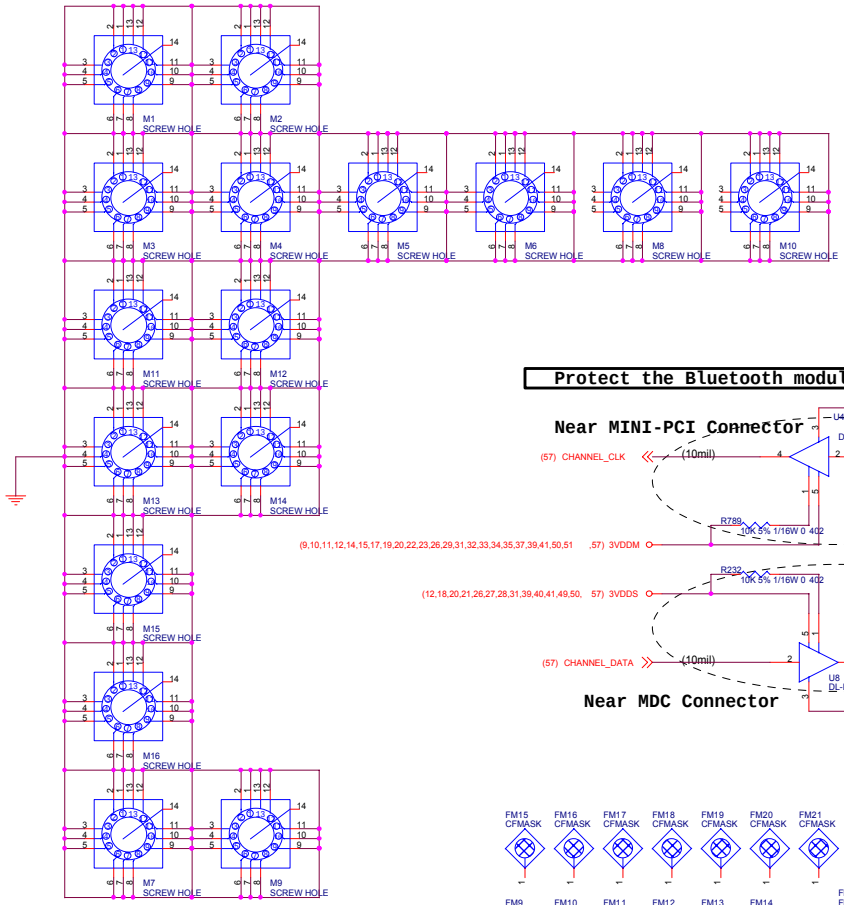
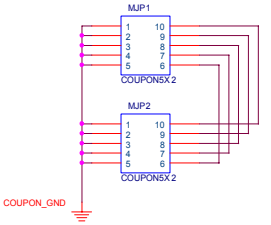
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size: C	Document Number: DIP SW/ LID Switch	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 55 of 66	

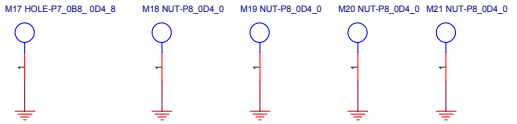


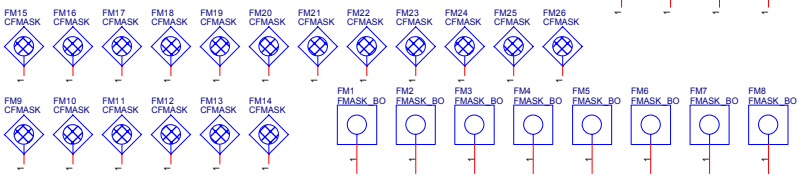


Protect the Bluetooth module and Calexico modules.

COUPON5X2







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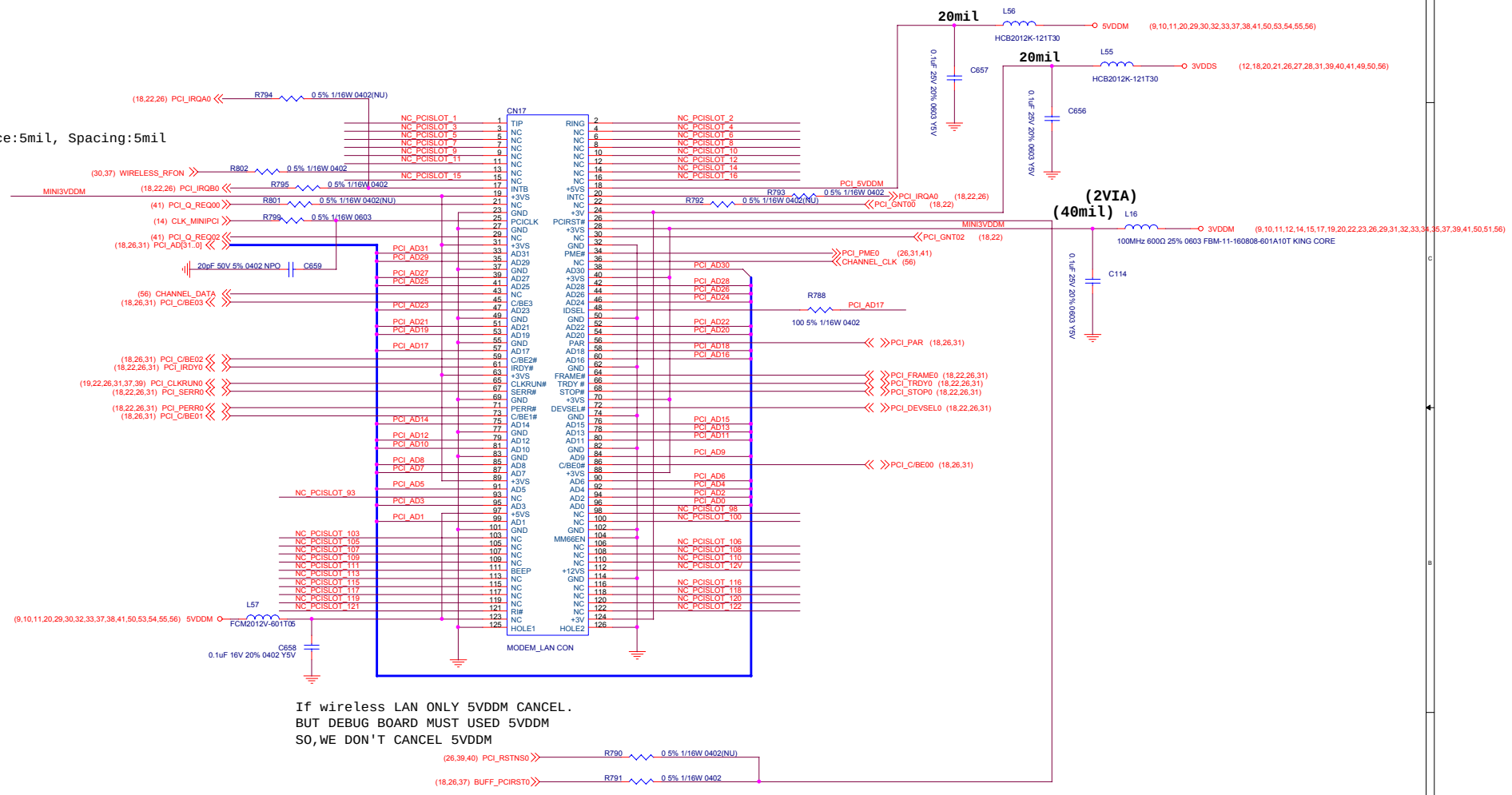
Title	MB02(Intel Banias + MontaraGM + ICH4-M)	
Size C	Document Number MDC CNN/ Blue Tooth CNN	Rev 0.2A
Date: Thursday, December 19, 2002	Sheet 56 of 66	

TYPE III MODEM / LAN CONNECTOR

Nu Parts : R14,R20,R38



Title	MB02(Intel Banias + MontaraGM + ICH4-M)
Size C	Document Number Calexico MINI PCI
Rev	0.2A
Date:	Thursday, December 19, 2002
Sheet	57 of 66

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FIC MB02 DC/DC Board Schematic Ver : 0.1

1. Top Sheet
2. Block Diagram
3. Schematic Modify Version Notice
4. Annotations
5. D/D Board CNN
6. 5VDDS,3VDDA
7. 1.8VDDM,1.5VDDM
8. 1394 CNN & MICIN & SW
9. SPDIF CNN

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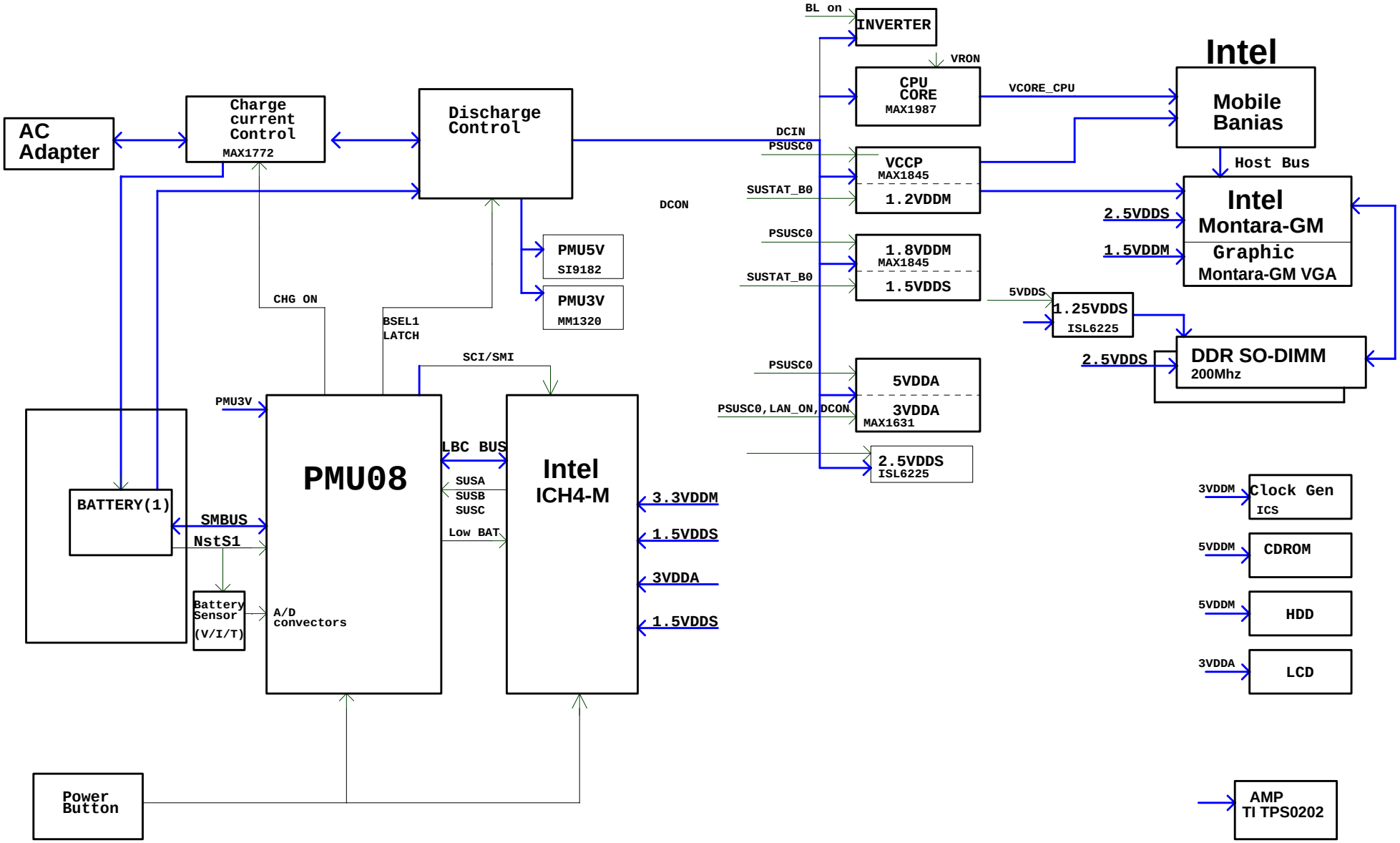
Title	MB02 Intel Banias + Montara-GM + ICH4-M	
Size: C	Document Number: TOP SHEET	Rev: 0.2A
Date: Thursday, December 19, 2002	Sheet 58 of 66	



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Title	MB02 Intel Banias + Montara-GM + ICH4-M	
Size C	Document Number Block Diagram	Rev 0.2A
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Sshematic Modify (Version ii):

BUG LIST:

	BUG	ROOT CAUSE	SOLUTION	PHASE IN
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
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23				
24				

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Title: **MB02 Intel Banias + Montara-GM + ICH4-M**

Size: C | Document Number: **Version Notice** | Rev: **0.2A**

Date: Thursday, December 19, 2002 | Sheet 60 of 66

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by DCON
1.5VDDA	1.5V always on power rail by DCON
5VDDA	5V always on power rail by PWR_CTL or PSUSC0
3VDDA	3.3V power rail by DCON
5VDDS	5.0V power rail by DCON
2.5VDDS	2.5V switched power rail
3VDDM	3.3V switched power rail
5VDDM	5.0V switched power rail
1.5VDDM	1.5V switched power rail
1.8VDDM	1.8V switched power rail
VCCP	1.2V switched power rail for CPU
Vcore_CPU	1.15~1.25V switched power rail for CPU

PCB Layers

Layer 1	TOP
Layer 2	GND
Layer 3	IN1 (HIGH SPEED)
Layer 4	IN2 (HIGH SPEED)
Layer 5	VCC
Layer 6	BOTTOM

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

0 = Active Low signal

Signal Conditioning

_D_ = Damped (by a resistor)
_Q_ = Isolated (by a Q-switch)
_L_ = Filtered (by an inductor or bead)

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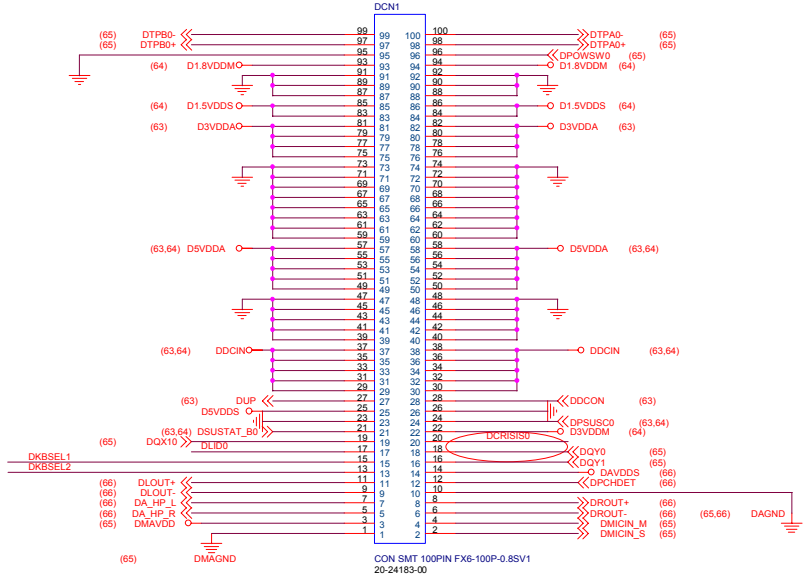
Title: MB02 Intel Banias + Montara-GM + ICH4-M

Size: C | Document Number: Annotations | Rev: 0.2A

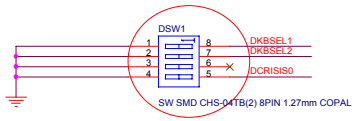
Date: Thursday, December 19, 2002 | Sheet 61 of 66

Switch & D/D BOARD CNN

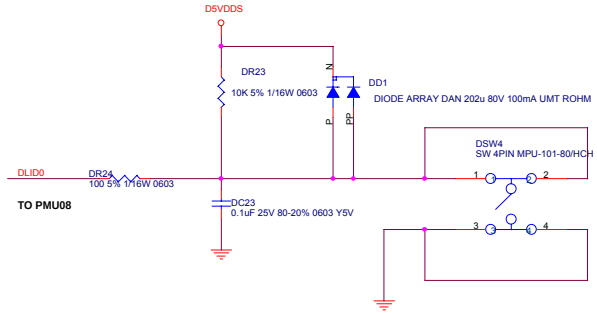
(5VDDA, 3VDDA, 1.5VDDA, 1.8VDDM)

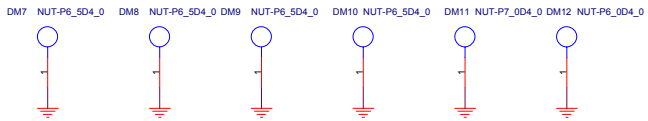


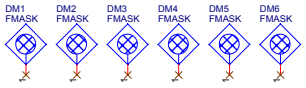
ES Modify



LID Switch







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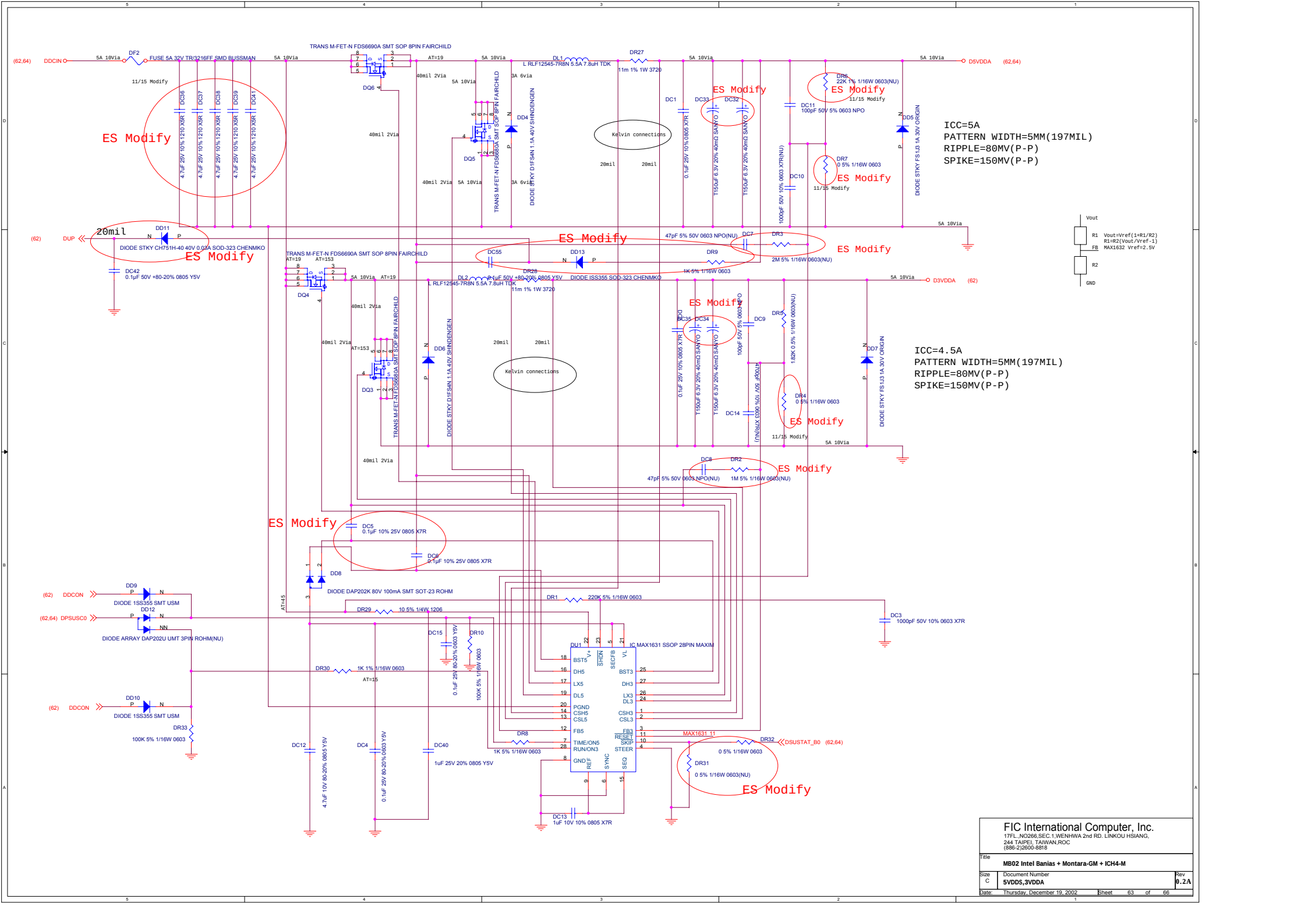

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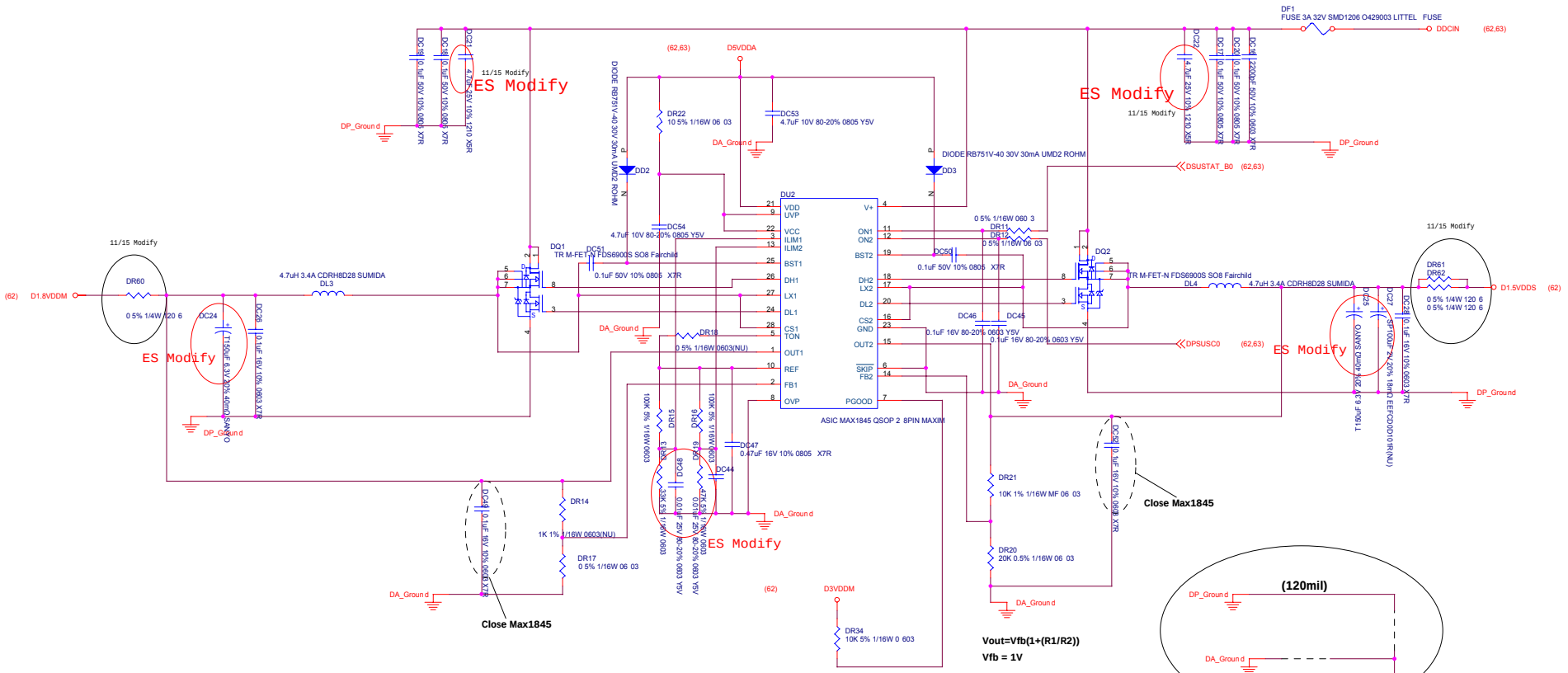

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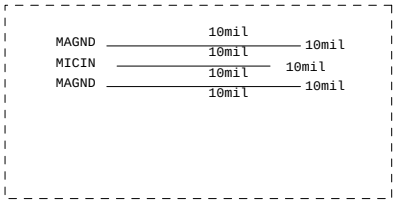

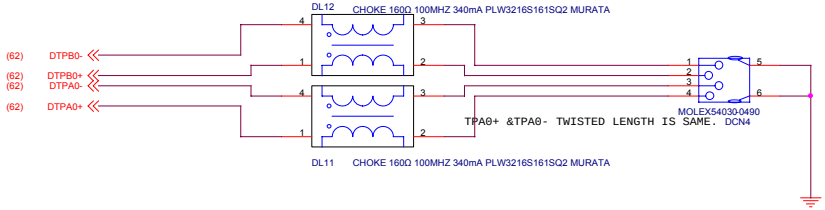

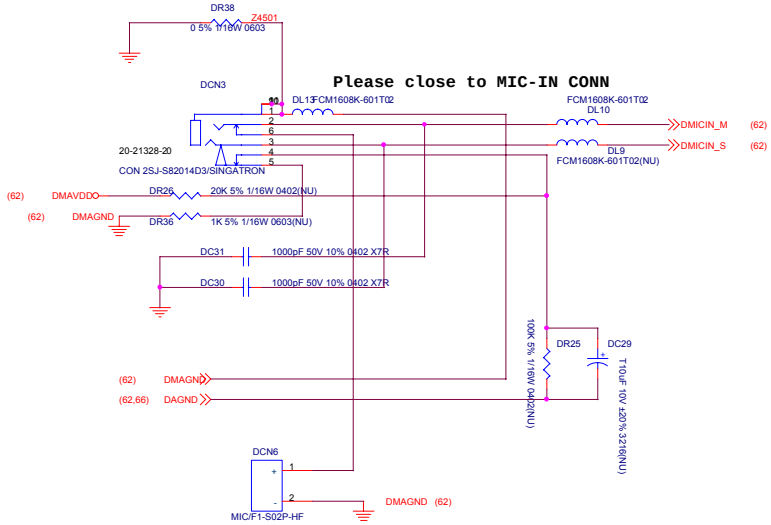

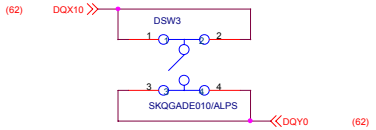

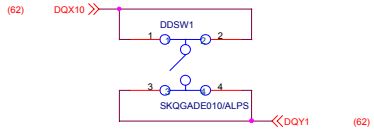

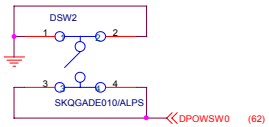

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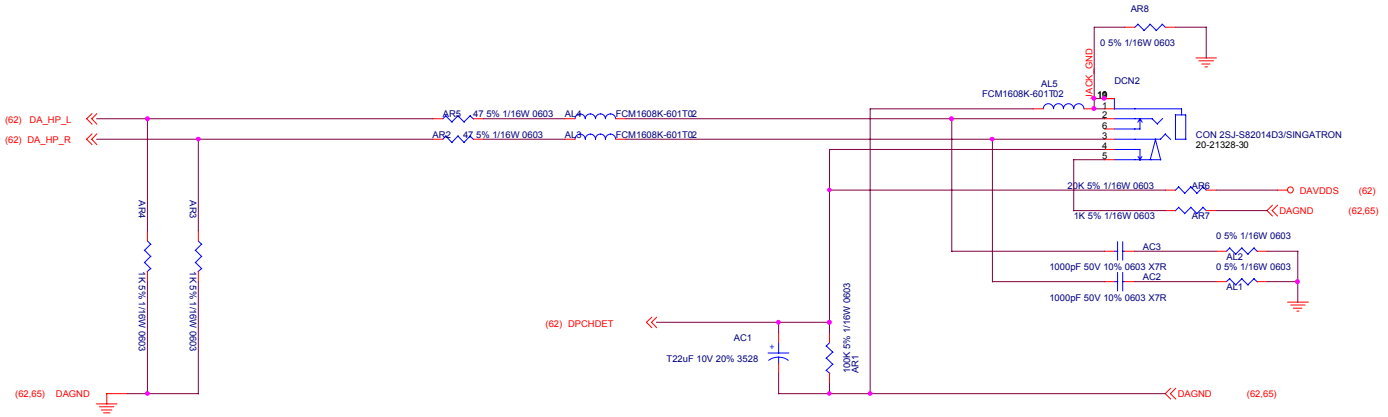

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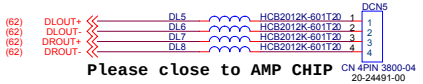

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