MS-6+ Picture

Winbond
N-Channel FET Synchronous Buck Regulator Controller
MS-6^{+} / MS-6^{+}G

MS-6+/MS-6+G
Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1			0.2		Version draft
2		Sep./04	0.21		Add Lead-free part MS-6+G

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

General Description

The MS-6+ is a high-speed, N-Channel synchronous buck regulator controller optimized for wide reference input range. The MS-6+ employs a fixed-frequency voltage-mode PWM control architecture. Both high-side and low-side MOSFETs are lower cost N-Channel type. The regulator is biased from a 5V rail and the power for the high-side MOSFET can be supplied by a separate 12V rail or supplied from a local charge pump.

Current limit is achieved by monitoring the voltage drop across the on resistance of the low-side MOSFET. This method eliminates the requirement of extra current sensing resistor and avoides false trigger of OC protection when Vin varies. The adaptive non-overlapping MOSFET gate drivers help avoid potential shoot-through problems while maintaining high efficiency. All these together with Power-good flag, enable and soft start features make power sequencing easy.

Unique "one wire control" feture make MS6+ easy to cooperate with Winbond's ACPI controller IC to provide proper voltage, timing and protection for motherboard ACPI applications.

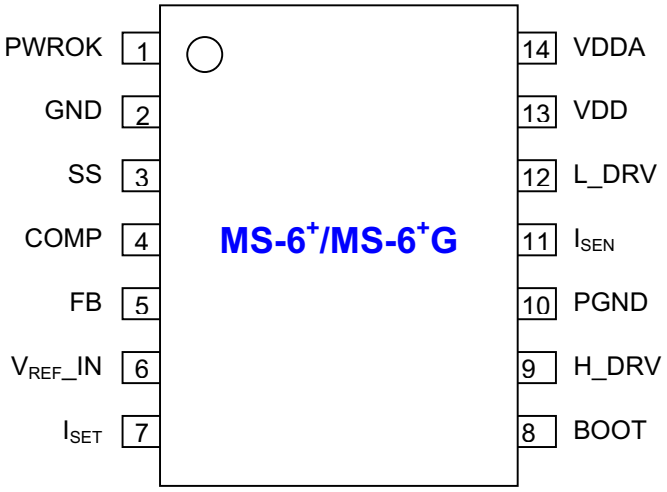
Features

- Input voltage from 3.3V or 5V
- Providing +/-1.5% reference voltage
- Wide reference input range
- Power Good flag
- Current limit without sense resistor
- Soft start
- Switching frequency from 100 kHz to 400 kHz
- Easy to cooperate with Winbond's ACPI controllers
- Tiny plastic SOP-14 package

Applications

- Set-Top Boxes/ Home Gateways
- Core Logic Regulators
- High-Efficiency Buck Regulation

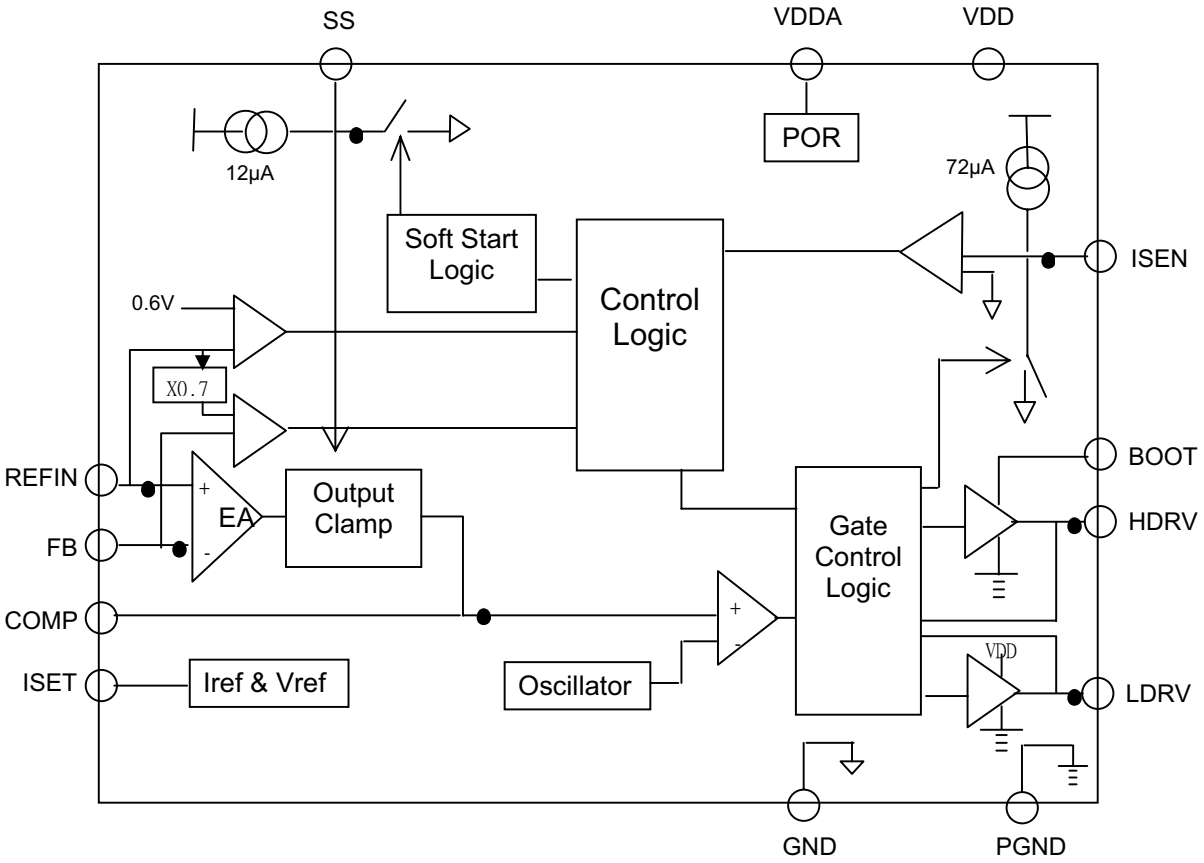
Pin-Out



Pin Description

PIN	NAME	FUNCTION
1	**PWROK**	Power OK. It's an open drain output. This pin will be opened with following conditions: 1. no over-current detected, 2. V_{REF}_IN >0.6V, 3. FB > 75% of V_{REF}_IN, 4. SS >3V.
2	**GND**	Power ground for signal level circuit.
3	**SS**	Soft Start Pin. A capacitor should be attached in this pin to ground for soft start output clamping. This capacitor, along with an internal 12uA current source, set the output clamp ramp up speed.
4	**COMP**	Internal Error Amplifier Output Pin. This pin is available for compensation of the control loop.
5	**FB**	Inverting Input of the Error Amplifier. This pin is available for compensation of the control loop.
6	**V_{REF}_IN**	Non-inverting Input of the Error Amplifier. Voltage on this pin provides reference input to the PWM control loop. When the V_{REF}_IN voltage is less than 0.3V, the PWM is shut-down and the H_DRV and L_DRV are driven low. Due to its wide input range (0 ~ 3.6V), the V_{REF}_IN voltage can be raised slowly to perform the input clamp function. Besides, a special function is implemented in this IC to inform the reference provider of over current alarm. Each time as the OC occurs, V_{REF}_IN will be short to GND (through 170 ohms) for about 5~10uS. The reference provider can be aware of the OC condition by detecting this pulse.
7	**I_{SET}**	This pin outputs a 1.19V reference voltage. Connect a 49.6K ohms resistor between this pin and GND. The Internal circuit will detect current flow out (24uA) for internal reference. In order to avoid high frequency interference, minimize the capacitance seen by this pin. If voltage on this pin is to be used as regulator's reference input, it's better to tap this pin through a nearly placed resistor with large resistance (>50K ohms).
8	**BOOT**	Supply rail for the high-side MOSFET driver. A bootstrap circuit may be used to create a BOOT voltage or a separate 12V supply can be used.
9	**H_DRV**	Gate drive for the high-side N-channel MOSFET. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the high-side MOSFET has turned off.
10	**PGND**	Ground for FET driver circuitry. Connect it to system ground.
11	**I_{SEN}**	Current limit threshold setting. Connect a resistor (R_{OCSET}) between this pin and the drain of the low-side MOSFET. An internal 72uA current source will flow through R_{ISEN} and cause a fixed voltage drop on it while the low-side MOSFET is turned on. In the mean while, the MS-6+ compares the voltage drop with the voltage across the low-side MOSFET and determines whether the current limit has been reached. The equation for over-current limit is: $I_{LIM} = (72uA * R_{ISEN})/R_{DSON}$
12	**L_DRV**	Gate drive for the low-side N-channel MOSFET. This pin is also monitored by the adaptive shoot through protection circuitry to determine when the low-side MOSFET has turned off.
13	**VDD**	+5V supply rail for the lower gate driver and control logic circuit.
14	**VDDA**	VDDA: +5V supply rail for the chip.

Internal Block Diagram



Soft-Start

When Vdda and Vdd exceeds 4.3V and voltage at pin REFIN exceeds 0.27V the soft start capacitor begins charging through an internal 12uA current source. The error amplifier (and the PWM duty) is both output clamped by the voltage on soft-start pin V(SS) and input clamped by the voltage on REFIN. So, there are two ways to soft start: following the rising of the slower one of V(SS) or V(REFIN). during soft-start, PWOK is forced low and Over-Current protection function begin to work. 0.4V to 1.9V of V(SS) is roughly mapping to 0 to 100% pulse-width. Smaller than 0.27V on REFIN will disable the PWM controller and discharge Css.

MOSFET Gate Drivers

Power for the high-side driver is through the BOOT pin. This voltage can be supplied by a separate, higher voltage source, or supplied from a local charge pump structure or even the combination of the two.

Since the voltage of the low-side MOSFET gate and the high-side MOSFET gate are being monitored to determine the state of the MOSFET, it should be considered carefully to add external components between the gate drivers and their respective MOSFET gates. Doing so may interfere with the shoot-through protection.

Current Limit

Current limit is realized by sensing the voltage across the low-side MOSFET while it is on. This method enhances the converter's effeciency and reduces cost by eliminating a current sensing resistor.

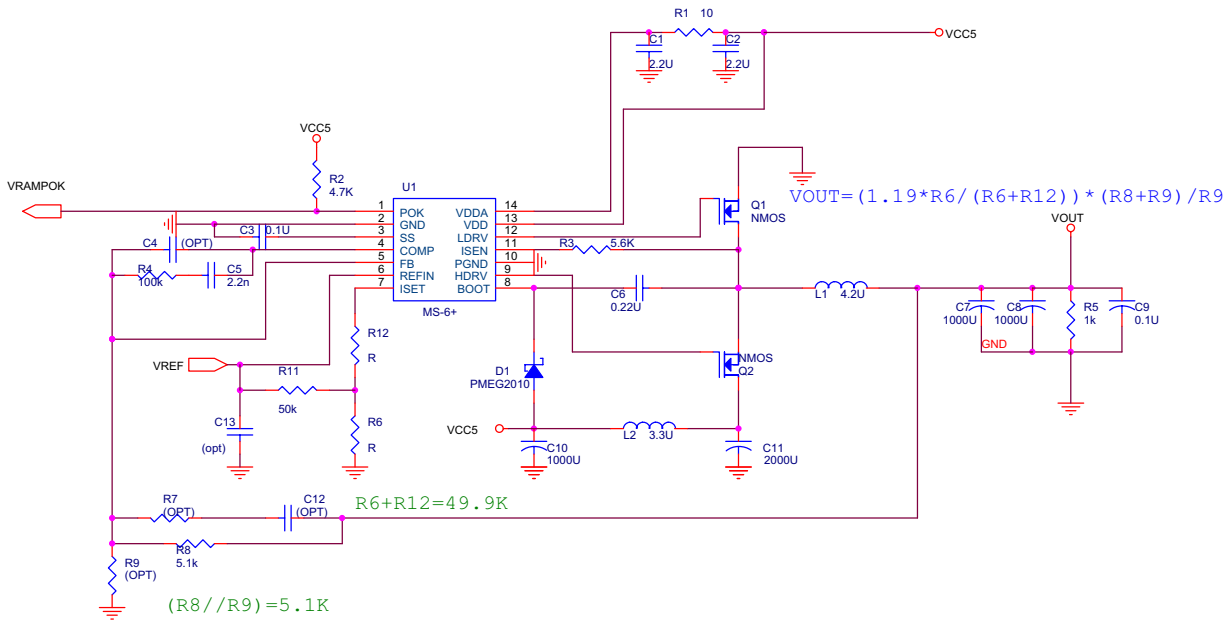
While low-side MOSFET is turned on, a constant current of 72uA is forced through R_{OCSET} which is an external resistor connected between phase and ISEN, causing a fixed voltage drop. This fixed voltage is compared against V_{DS} and if the latter is higher, the chip enters current limit mode. In the current limit mode both the high-side and low-side MOSFETS are turned off and the soft start capacitor C_{SS} will be discharged immediately. The REFIN is shorted to GND for 5~10uS to indicate the over current condition. After a 5mS delay, a soft-start cycle is initiated. If the cause of the overcurrent is still present after the delay interval, the current limit would be triggered again. The shut dowm - delay - soft start cycle will be repeated indefinitely untill the overcurrent event has cleared.

Input Tracking

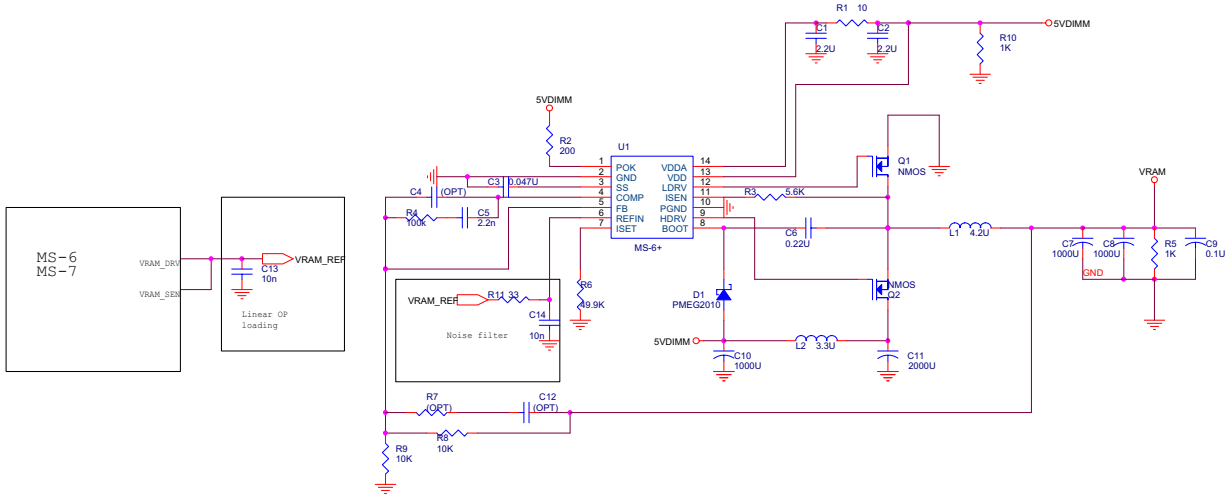
When the V_{REF}_IN voltage is less than 0.3V, the PWM is shut-down and the H_DRV and L_DRV are driven low. Due to its wide input range (0 ~ 3.6V), this chip is suitable for reference input tracking application. But note that the chip will be shut-down when REFIN <0.27V, so a proper setting of C_{SS} is needed to clamp the output at initiation of start up and avoid output voltage step-up (and so a large inrush current).

Application Circuit

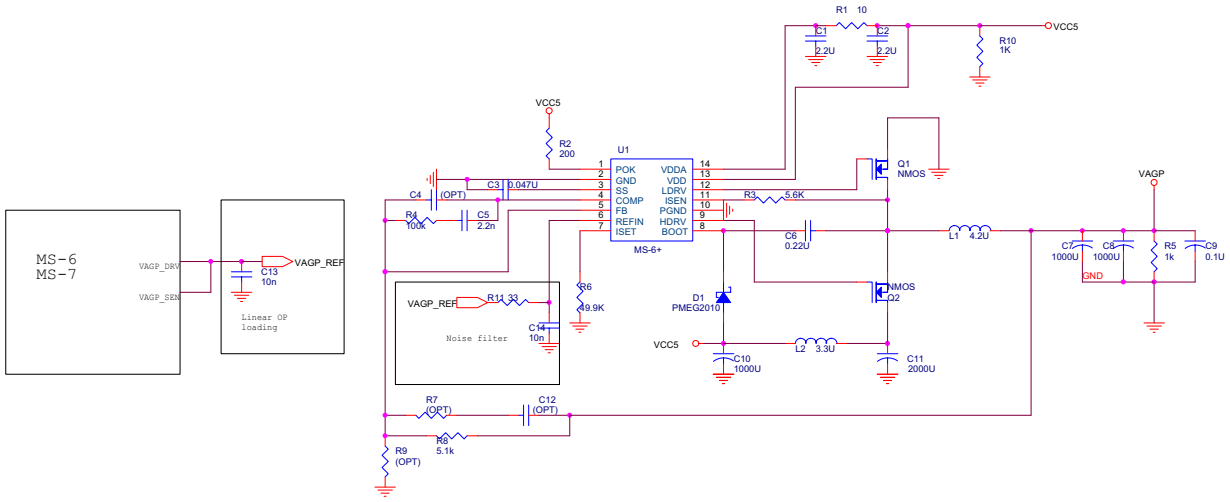
1. Fix



2. VRAM tracking



3. VAGP tracking



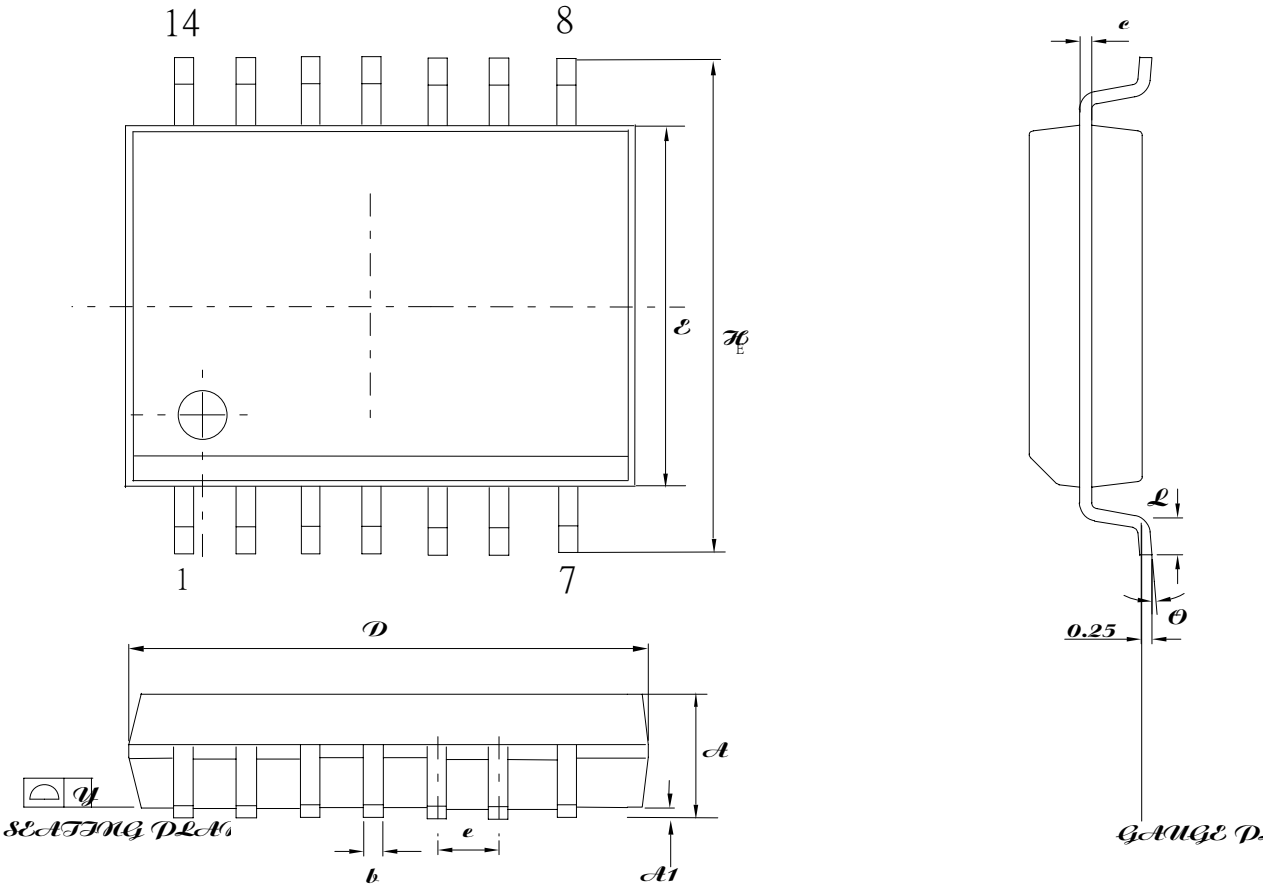
4. Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Nominal Suuply	I_{CC}	EN=V_{CC}; UGATE and LGATE Open	-	5	-	mA
POWER-ON RESET						
Rising V_{DD} Threshold			-	4.3	-	V
Falling V_{DD} Threshold			-	3.7	-	V
REFIN Enable			-	2.7	-	V
OSCILLATOR						
Free Running Frequency		R_{SET}=49.6K	160	200	240	kHz
Ramp Amplitude	ΔV_{OSC}	R_{SET}=49.6K	-	1.5	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance	V_{REF}		-1.5	-	1.5	%
Reference Voltage			-	1.19	-	V
ERROR AMPLIFIER						
DC Gain			-	80	-	dB
Gain-Bandwidth			-	5	-	MHz
Slew Rate			-	4	-	$V/_{\mu S}$
GATE DRIVERS						
High-side Gate Source	$I_{HGATE-SRC}$	V_{BOOT}=12V,V_{UGATE}=6V	250	-	-	mA
High-side Gate Sink	$I_{HGATE-SNK}$	V_{BOOT}=12V,V_{UGATE}=6V	600	-	-	mA
Low-side Gate Source	$I_{LGATE-SRC}$	V_{CC}=5V, V_{LGATE}=2.5V	250	-	-	mA
Low-side Gate Sink	$I_{LGATE-SNK}$	V_{CC}=5V, V_{LGATE}=2.5V	300	-	-	mA
PROTECTION						
ISEN Current Source	I_{SEN}		64	72	80	µA
Soft-Start Current	I_{SS}		10	12	14	µA

Typical Performance Characteristics

Package Dimension Outline

14L SOP (150mil)



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN IN	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC		0.050 BSC	
HE	5.80	6.20	0.228	0.244
y	———	0.10	———	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

Ordering Instruction

PART NO.	PACKAGE	REMARKS
MS-6+	14-pin SOP	Operation - Commercial 0~70℃

How to Read the Top Marking

Left Line: MSI Logo
1st Line: Part No – MS-6+
2nd Line: IC Tracking Code
3rd Line: Manufacturing Date Code (X XX) + Assembly Code (X) + IC Version (X)

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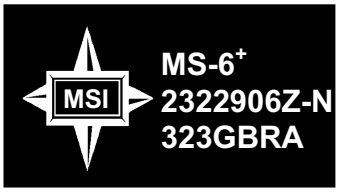
Ordering Instruction

PART NO.	PACKAGE	REMARKS
MS-6+	14-pin SOP	Operation - Commercial 0~70℃
MS-6+G	14-pin SOP	Operation - Commercial 0~70℃ Lead-free

How to Read the Top Marking



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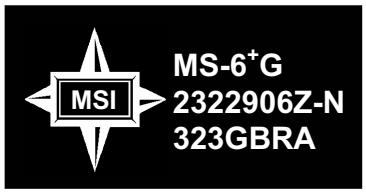
+ Assembly Code (X) + Chip Version (XXX)



Left Line: MSI Logo
1st Line: Part No – MS-6+Lead-free package (G)
2nd Line: IC Tracking Code
3rd Line: Manufacturing Date Code (X XX)
+ Assembly Code (X) + Chip Version (XXX)

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