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MS-7177

Version:21

CPU:

Intel Tejas & Prescott LGA775 Processor

System Chipset:

**Intel Grantsdale: 915GV/915PP/915G/910GL
Intel ICH6**

On Board Chipset:

**BIOS -- FWH EEPROM
AC'97 Codec -- ALC655
LPC Super I/O -- W83627THF Ver:E
LAN --RTL8100C/RTL8110S
CLOCK --Cypress 28416**

Main Memory:

DDRII * 4

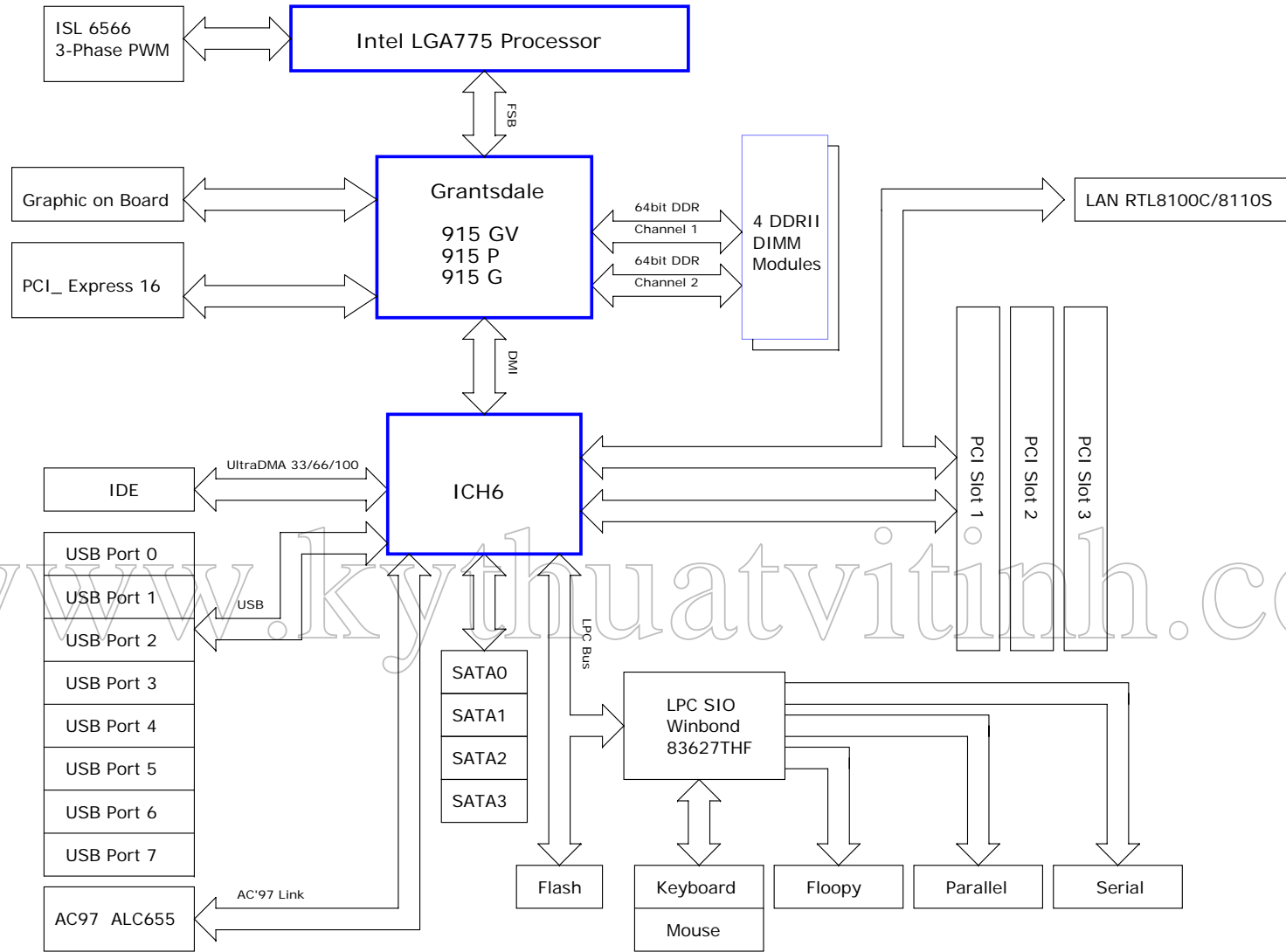
Expansion Slots:

**PCI EXPRESS X16 SLOT
PCI SLOT * 3**

PWM:

Controller: Intersil 6566

Block Diagram



Tejas		
0.8375V - 1.6000V Core	-	95A
1.2V FSB Vtt	-	TBD A

Gransdale GMCH		
1.2V FSB Vtt	-	1.0A
1.8V DDRII I/O (S0,S1)	-	4.7A
1.8V DDRII I/O (S3)	-	25mA
*2.5V DAC	-	0.07A
2.5V HV	-	TBD A
1.5V Core (Integrated)	-	9.7A
1.5V Core (Discrete)	-	7.7A
*1.5V PCI Express	-	1.4A

ICH6		
1.2V VCC_CPU	-	tbdmA
1.5V Core	-	1.88A
*1.5V PCI Express	-	260mA
1.5V SATA	-	430mA
+3.3V VccSus	-	330mA
RTC (G3)	-	5uA
5VRef	-	TBD A
5VrefSus	-	TBD A
+3.3V	-	180mA

FWH		
+3.3V (S0,S1)	-	107mA

ISL6566		
VCCP	VRM 10.1	
0.8375V-1.6000V	95A	
3-Phase Switch		

W83310DS		
VTT_DDR		
1.3V	Linear	1.0A

MS7 Regulator		
V_FSB_VTT		
1.2V	Linear	5.0A
VCC_DDR		
1.8V (S0,S1)	8.0A	
Linear (S3)	570mA	
V_2P5_MCH		
2.5V	Linear	100mA
VCC3_SB		
3.3V	Linear	1.5A
5VDUAL1,2		
5V	Linear	22mA

MS6+ Regulator		
V_1P5_CORE		
1.5V	Switch	14A

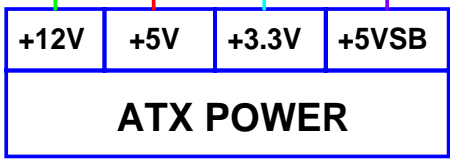
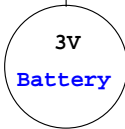
DDR DIMM & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

PCI slot x3		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

USB		
+5V (S0,S1)	-	4A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA



ICH6 Not modify yet

GPIO Pin	Type	Function	Power	Pin
GPIO 0	I	REQ#6 pull-up to VCC5 with 2.7K	5V	B7
GPIO 1	I	REQ#5 pull-up to VCC5 with 2.7K, and connect to RTL8100C	5V	E8
GPIO 2	I	PIRQ#E pull-up to VCC5 with 2.7K	5V	D9
GPIO 3	I	PIRQ#F pull-up to VCC5 with 2.7K	5V	C7
GPIO 4	I	PIRQ#G pull-up to VCC5 with 2.7K	5V	C6
GPIO 5	I	PIRQ#H pull-up to VCC5 with 2.7K	5V	M3
GPIO 6	I	GP16 pull-up to VCC3 with 10K	3.3V	AD19
GPIO 7	I	GP17 pull-up to VCC3 with 10K	3.3V	AE19
GPIO 8	I	GP18 pull-up to VCC3_SB with 10K	3.3V_SB	R1
GPIO 9	I	OC#3_4 connect to USB connector	3.3V_SB	C23
GPIO 10	I	OC#3_4 connect to USB connector	3.3V_SB	D23
GPIO 11	I	SMB_ALERT# pull-up to VCC3_SB with 10K	3.3V_SB	W6
GPIO 12	I	PS_DETECT pull-up to VCC3 with 10K	3.3V	M2
GPIO 13	I	SIO_PME# connect to LPC I/O	3.3V_SB	R6
GPIO 14	I	OC#3_4 connect to USB connector	3.3V_SB	C25
GPIO 15	I	OC#3_4 connect to USB connector	3.3V_SB	C24
GPIO 16	O	NC	3.3V	D8
GPIO 17	O	PGNT#5 connect to RTL8100C	3.3V	F6
GPIO 18	O	NC	3.3V	AC21
GPIO 19	O	BIOS_WP# connect to FWH	3.3V	AB21
GPIO 20	O	NC	3.3V	AD22
GPIO 21	O	NC	3.3V	AD20
GPIO 23	O	GPO23_TBL# connect to FWH	3.3V	AD21
GPIO 24	I/O	GPIO24 connect to Lenovo header	3.3V_SB	V3
GPIO 25	I/O	pull-down to GND with 1K directly (enable internal 2.5V VRM)	3.3V_SB	P5
GPIO 26	I	pull-up to VCC3 with 10K directly	3.3V	AF17
GPIO 27	I/O	GPO27_TBL# connect to ACPI Q87	3.3V_SB	R3
GPIO 28	I/O	NC	3.3V_SB	T3
GPIO 29	I	pull-up to VCC3 with 10K directly	3.3V	AE18
GPIO 30	I	pull-up to VCC3 with 10K directly	3.3V	AF18
GPIO 31	I	pull-up to VCC3 with 10K directly	3.3V	AG18
GPIO 32	I/O	LEO_CLKRUN#	3.3V	AF19
GPIO 33	I/O	NC	3.3V	AF20
GPIO 34	I/O	GPIO34 connect to Lenovo header	3.3V	AC18
GPIO 40	I	PREQ#4 pull-up to VCC5 with 2.7K	5V	F7
GPIO 41	I	NC	3.3V	P4
GPIO 48	O	NC	3.3V	E7
GPIO 49	OD	H_PWRGD pull-up to VTT_OUT_LEFT with 100 ohm, and connect to CPU	VCPU	AG25

FWH

GPIO Pin	Type	Function
GPIO 0	I	PD_DET

PCI Configuration

DEVICE	INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 2	INTB# INTC# INTD# INTA#	PCI_REQ#1 PCI_GNT#1	AD18	PCICLK1
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD19	PCICLK2
PCI Slot 1	INTD# INTA# INTB# INTC#	PCI_REQ#3 PCI_GNT#3	AD20	PCICLK3
LAN	INTH#	PCI_REQ#5 PCI_GNT#5	AD27	LAN_CLK

PCI RESET DEVICE

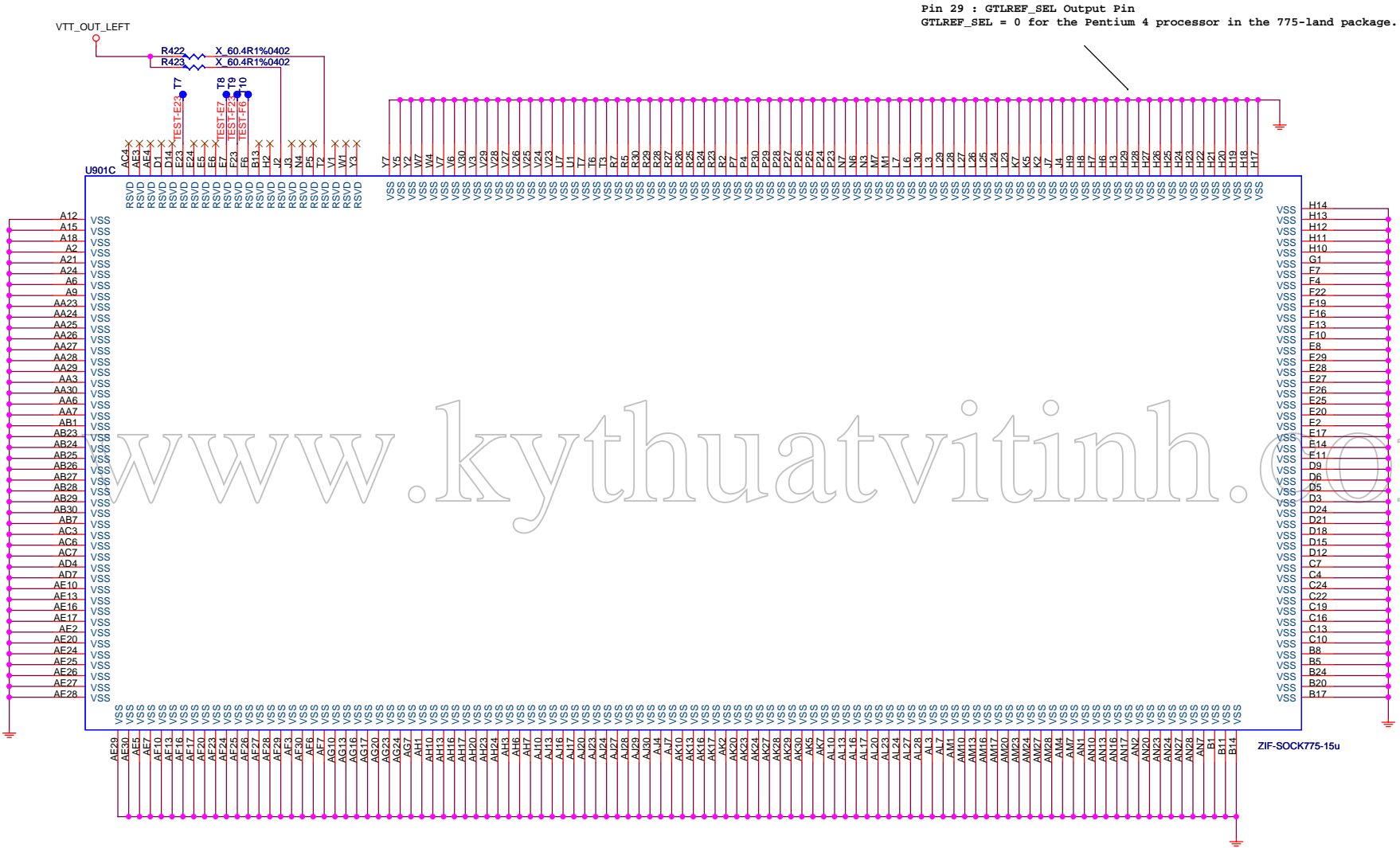
Signals	Target
PLTRST#	Grandstale,MS7
PCIRST_ICH6#	PCIE_16, LAN
PCIRST#1	FWH, SIO, LEO Header
PCIRST#2	PCI Slot 1,2,3
HD_RST#	IDE

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A4H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

JUMPER SETTING

RTCST	(2-3) NORMAL	(1-2) CLEAR
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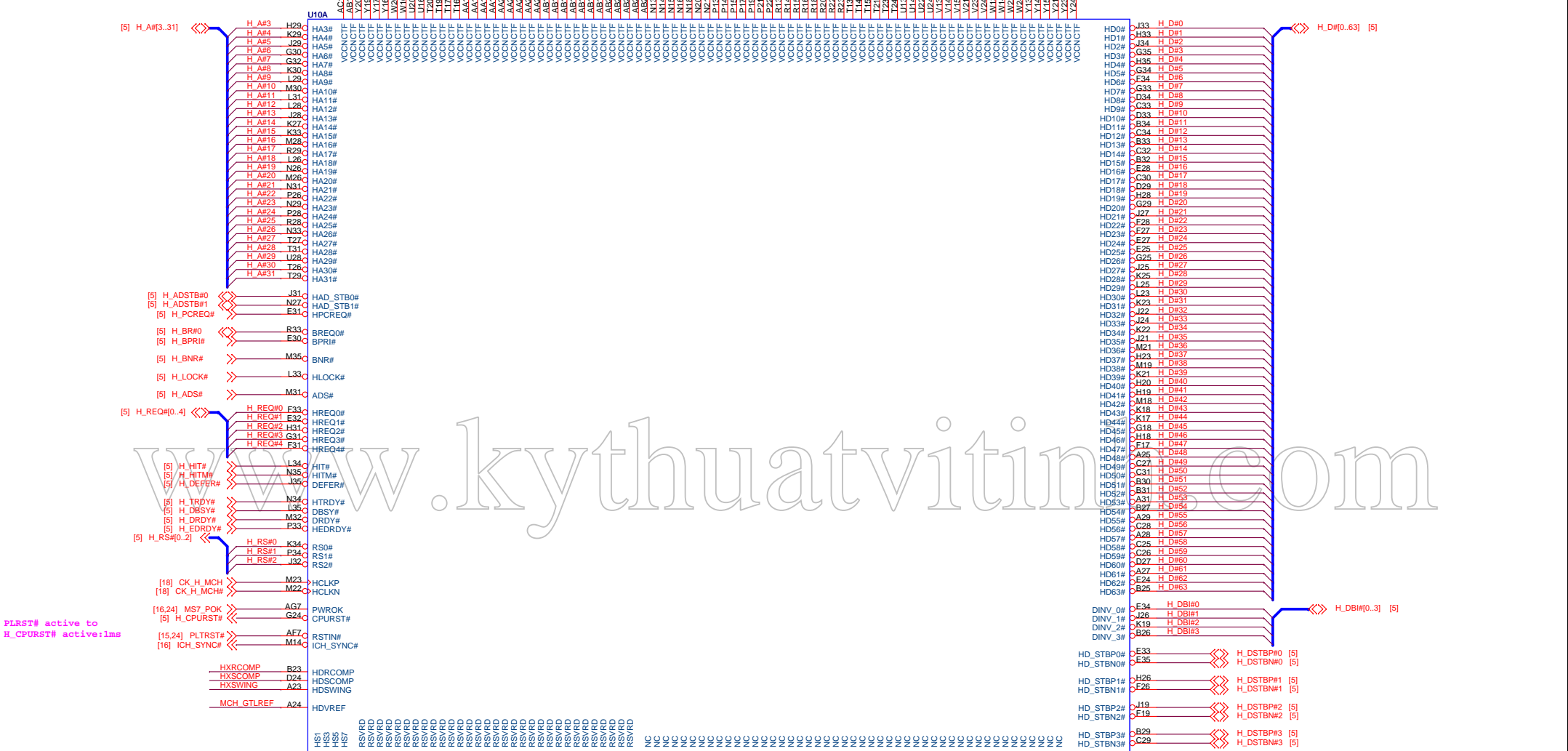
Pin 29 : GTLREF_SEL Output Pin
 GTLREF_SEL = 0 for the Pentium 4 processor in the 775-land package.

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Title: **Intel LG775 - GND**

Size: Custom	Document Number: MS-7177	Rev: 20
Date: Monday, July 11, 2005		Sheet 7 of 33

V_1P5_CORE



PLRST# active to H_CPURST# active:1ms

GTLREF VOLTAGE SHOULD BE 0.67*VTT=0.8V

HD_SWING VOLTAGE *10 MIL TRACE , 7 MIL SPACE* HD_SWING S/B 1/4*VTT +/- 2%

CAPS SHOULD BE PLACED NEAR MCH PIN

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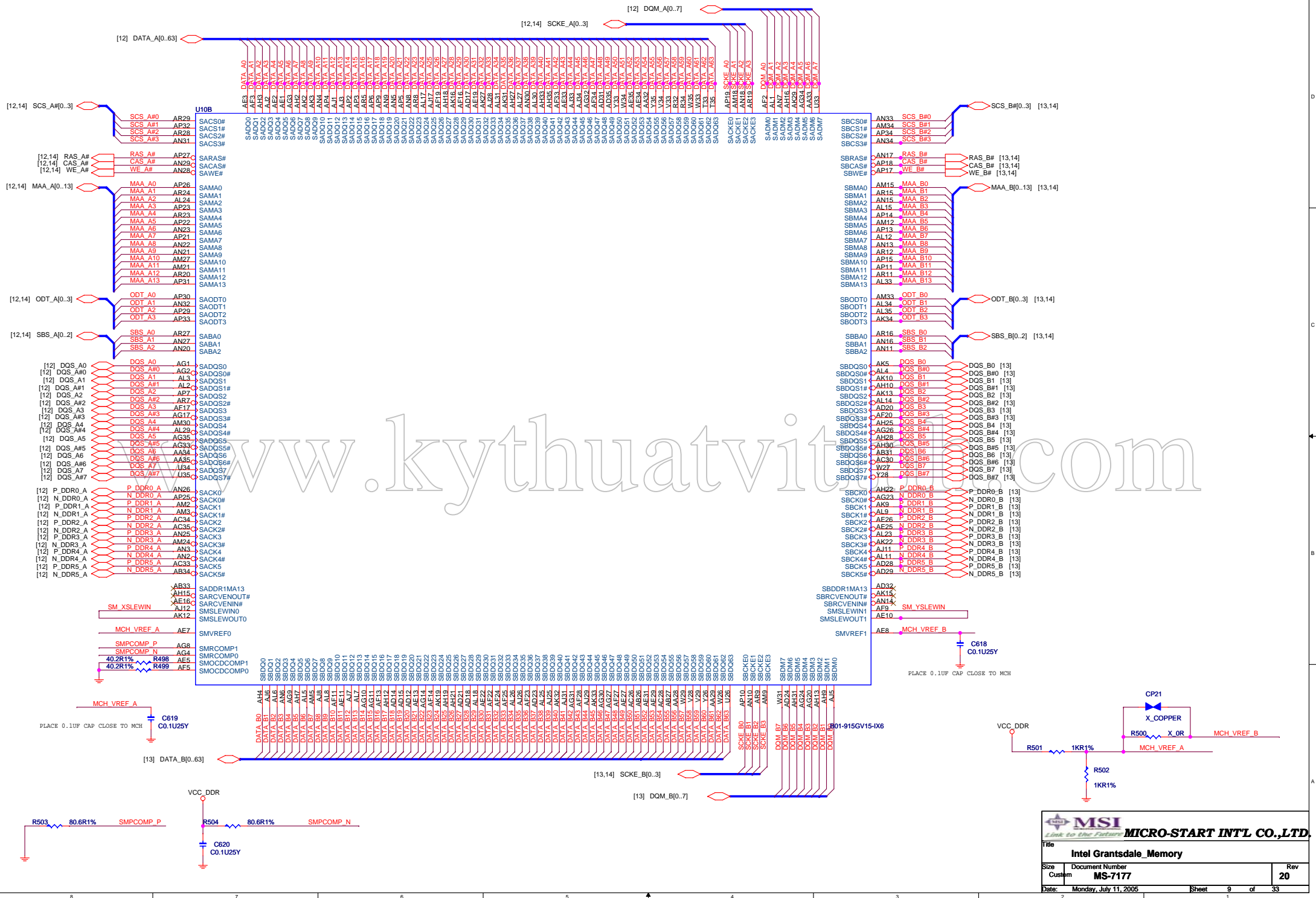
Title: **Intel Grantsdale CPU**

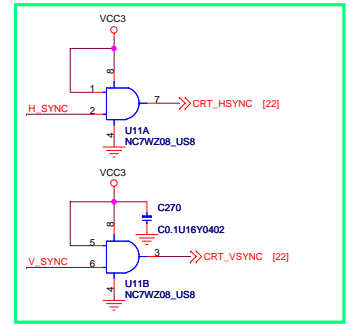
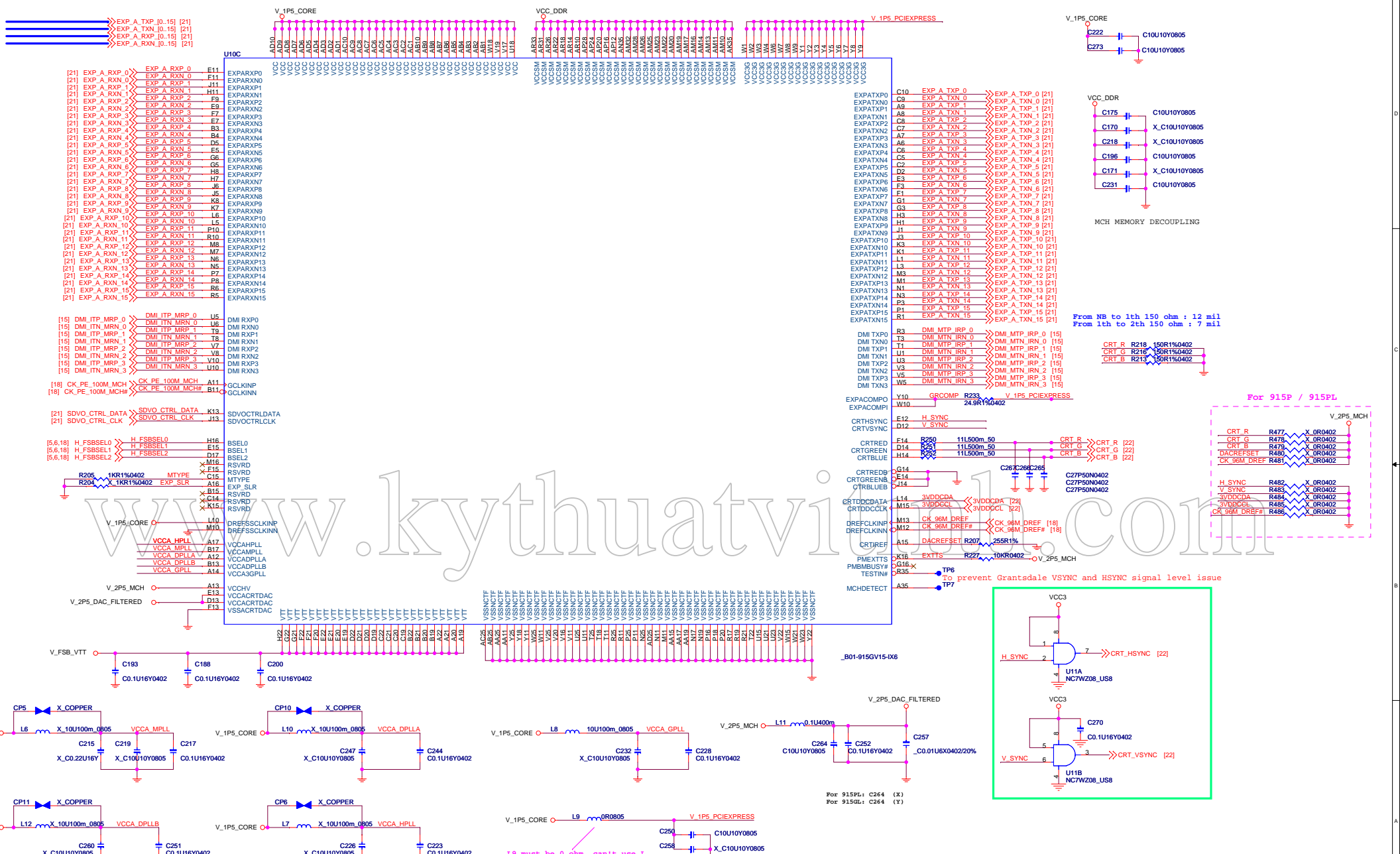
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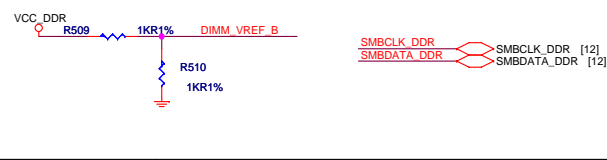
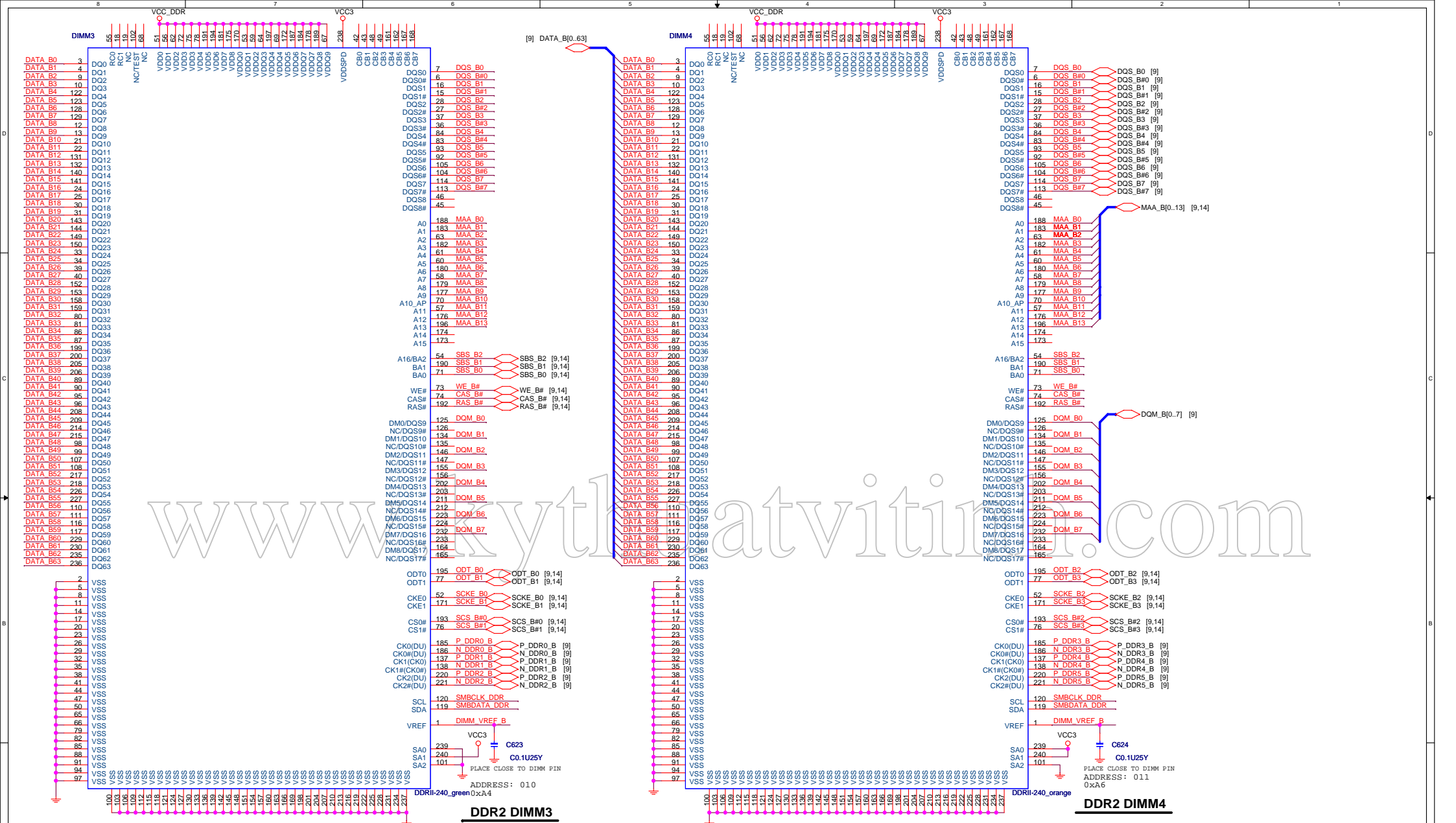
Date: Monday, July 11, 2005

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Rev: **20**







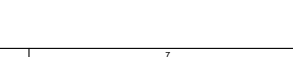
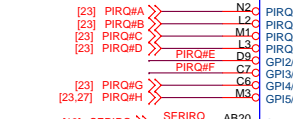
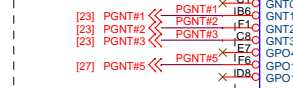
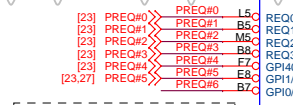
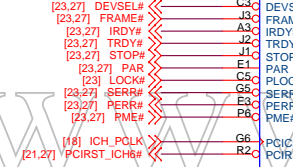
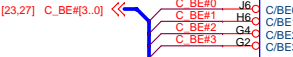
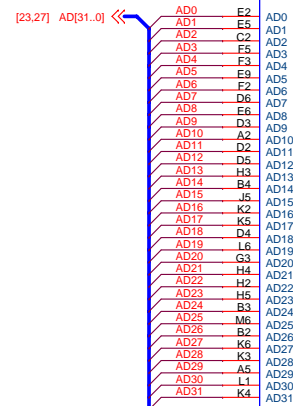
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Title: **DDR2 DIMM 3 & 4**

Size: Custom Document Number: **MS-7177** Rev: **20**

Date: Monday, July 11, 2005 Sheet: 13 of 33

U15A



PCI INTERFACE

ICH 6

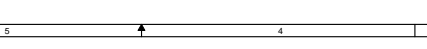
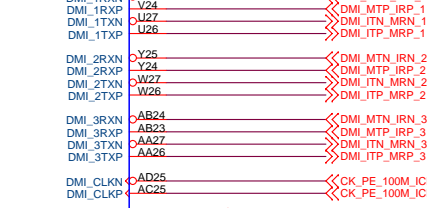
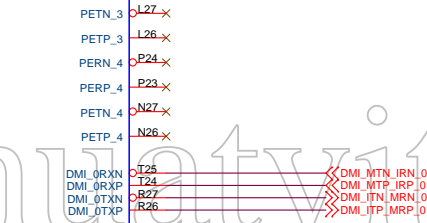
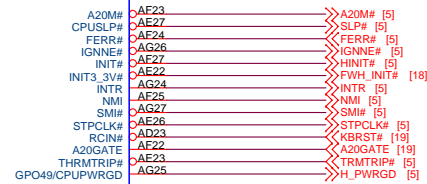
PART 1/3

CPU

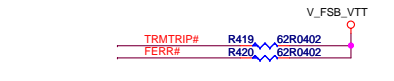
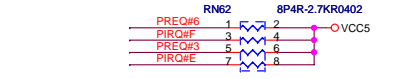
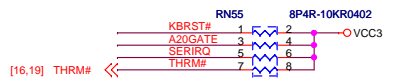
PCI EXPRESS

DIRECT MEDIA

LAN



ICH6 Pull-Up / Down Resistors



DMI Interface
Trace width 5 mils & 7 mils space.
GMCH breakout space 5 mils, length < 250 mils
Length matching < 5 mils
Trace Length 2" to 11"

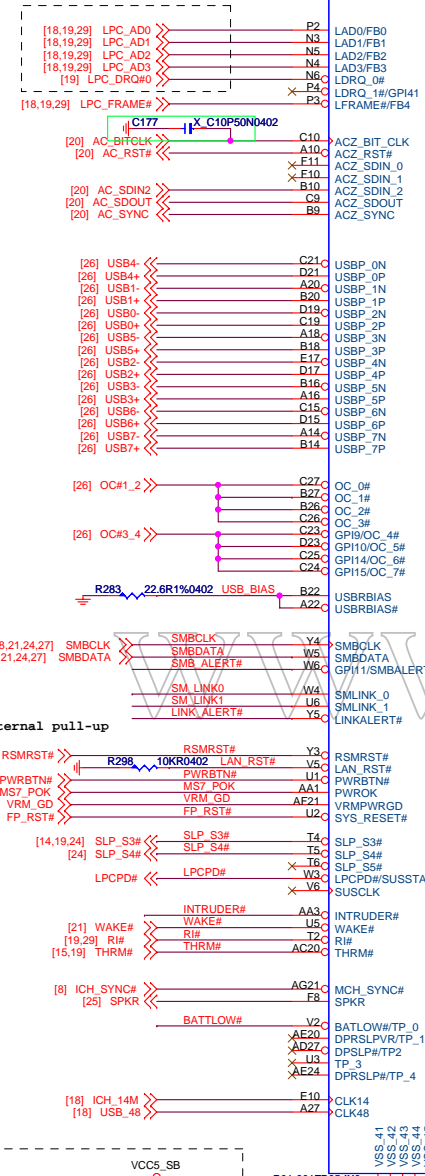
<200mils

These signals have internal pull-ups.

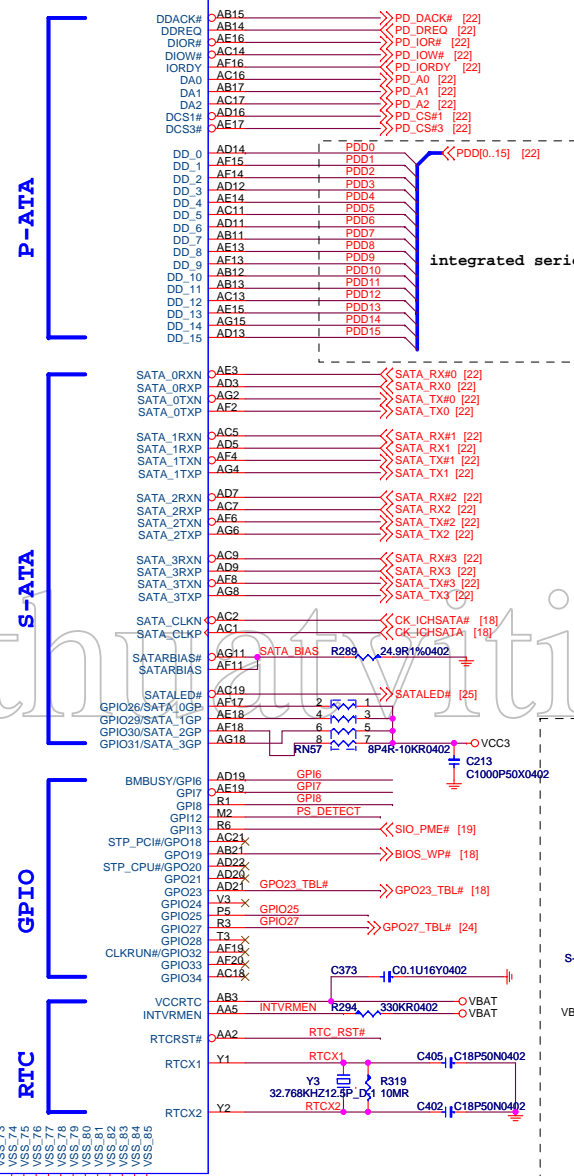
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Title: ICH6_PCI, DMI, CPU, IRQ
Size: Custom
Document Number: MS-7177
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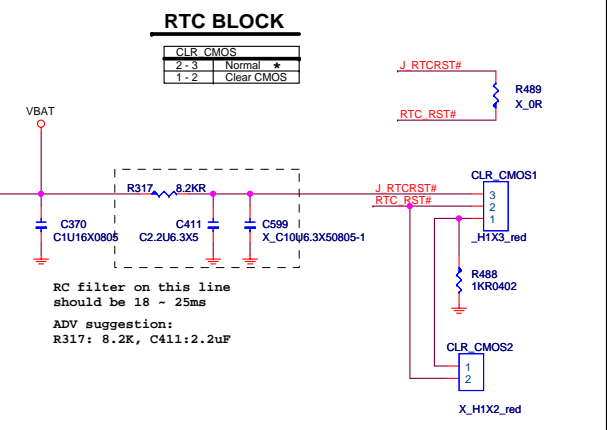
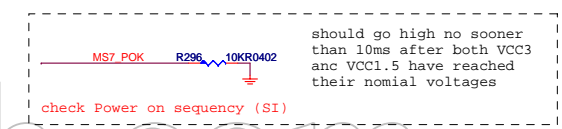
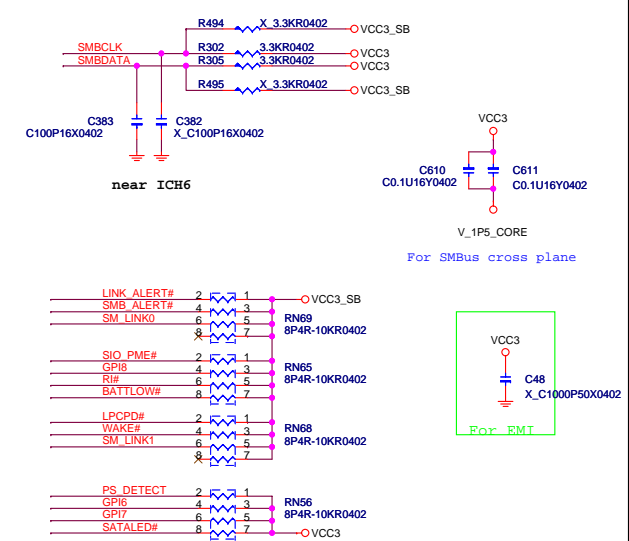
ICH6 integrates 20K ohm nominal pull-up resistors



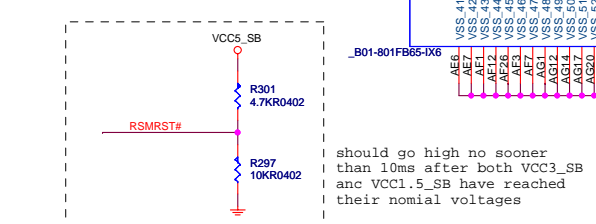
ICH 6 PART 2 / 3



SM BUS Pull-High

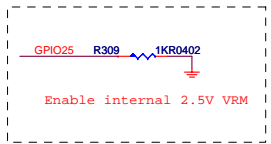


Pin U1 internal pull-up

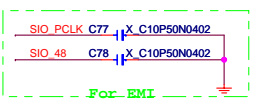


should go high no sooner than 10ms after both VCC3 and VCC1.5 have reached their nominal voltages

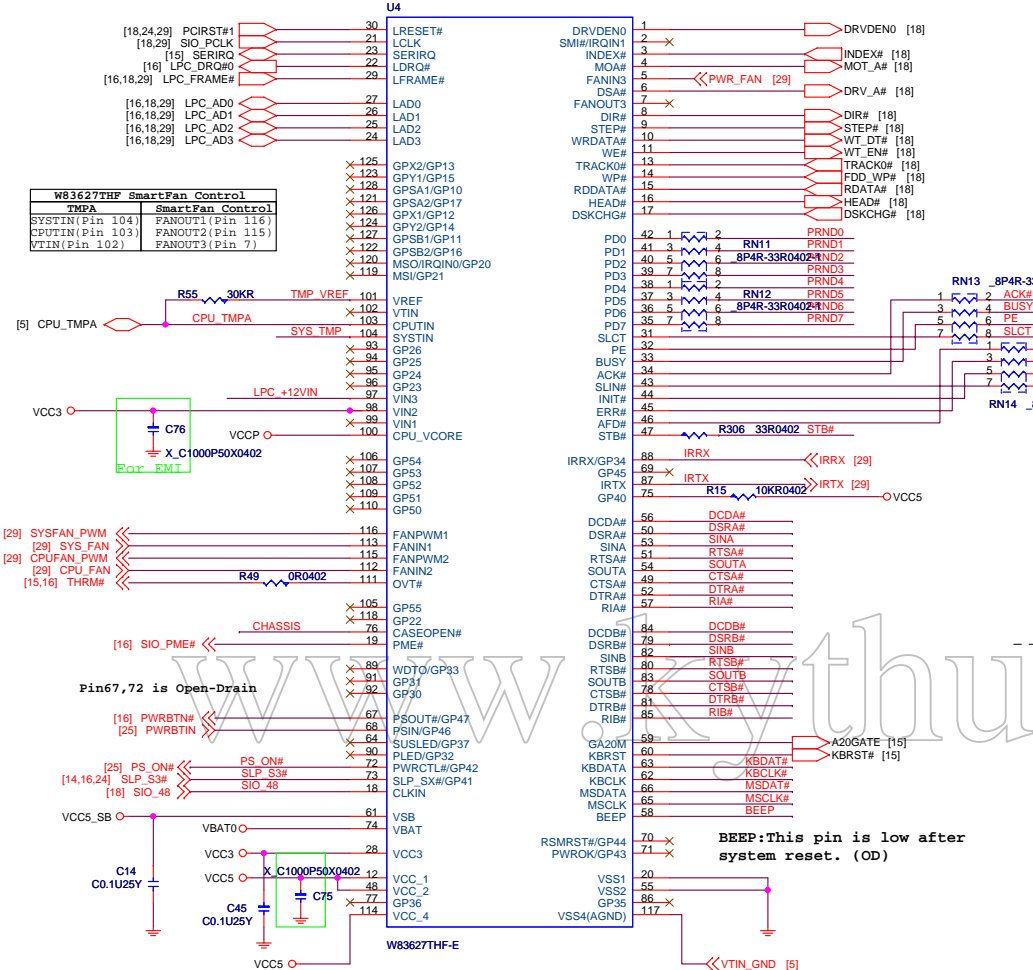
RC filter on this line should be 18 - 25ms
ADV suggestion:
R317: 8.2K, C411: 2.2uF



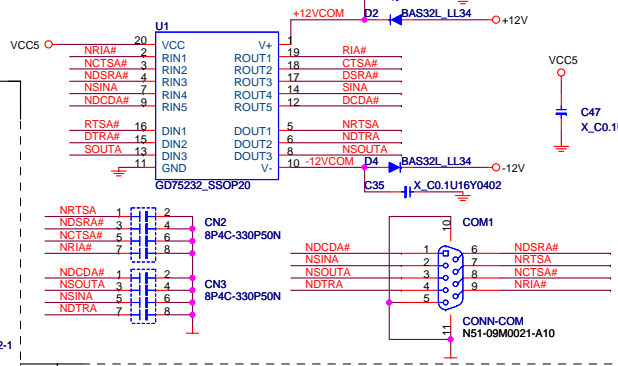
LPC SUPER I/O W83627HF/NHF/THF



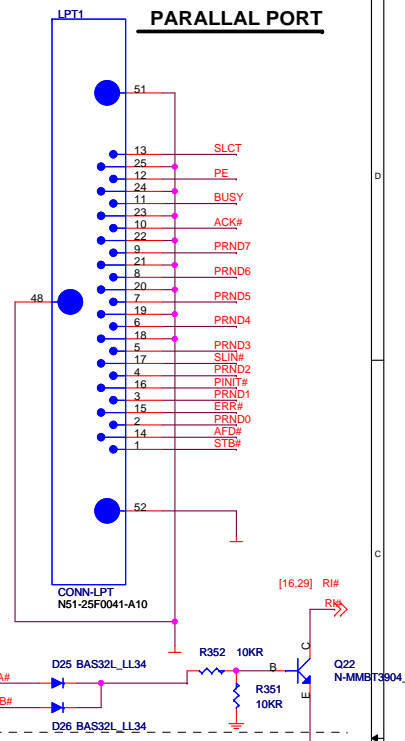
W83627THF SmartFan Control	
TMPA	SmartFan Control
SYSTIN (Pin 104)	FANOUT1 (Pin 116)
CPUTIN (Pin 103)	FANOUT2 (Pin 115)
VTIN (Pin 102)	FANOUT3 (Pin 7)



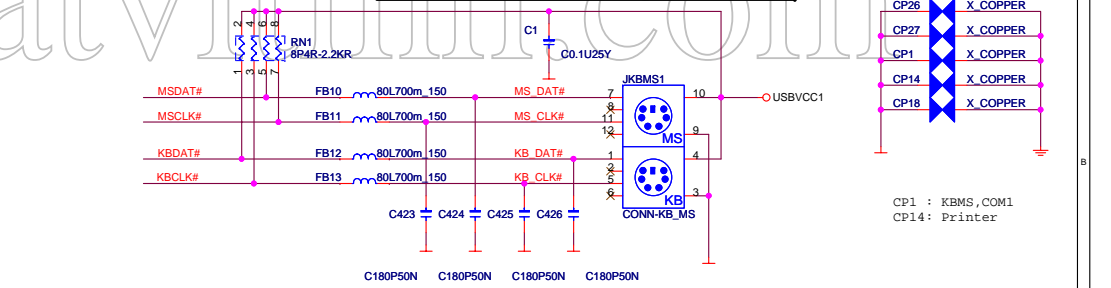
SERIAL PORT 1



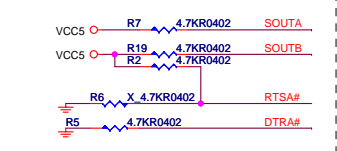
PARALLEL PORT



PS2 KEYBOARD & MOUSE CONNECTOR

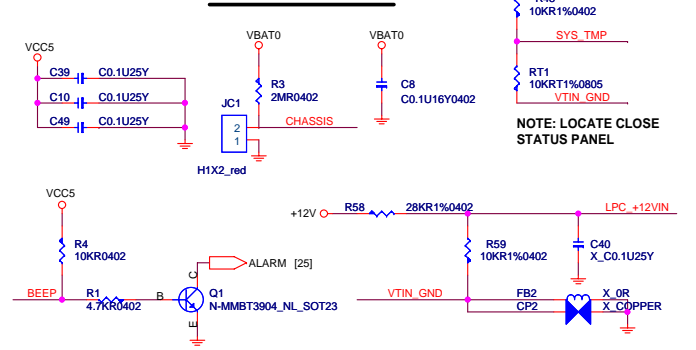


LPC I/O STRAPPING RESISTOR

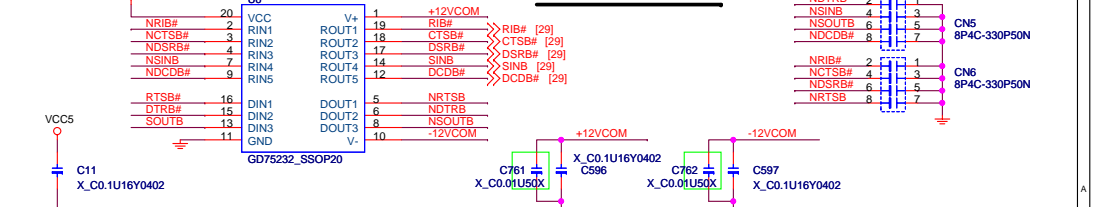


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

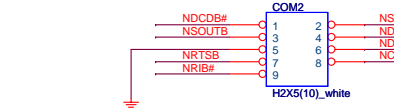
Chassis Intrusion



SERIAL PORT 2



COM2 HEADER



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Title: **SIO, KBMS, COM, Print**

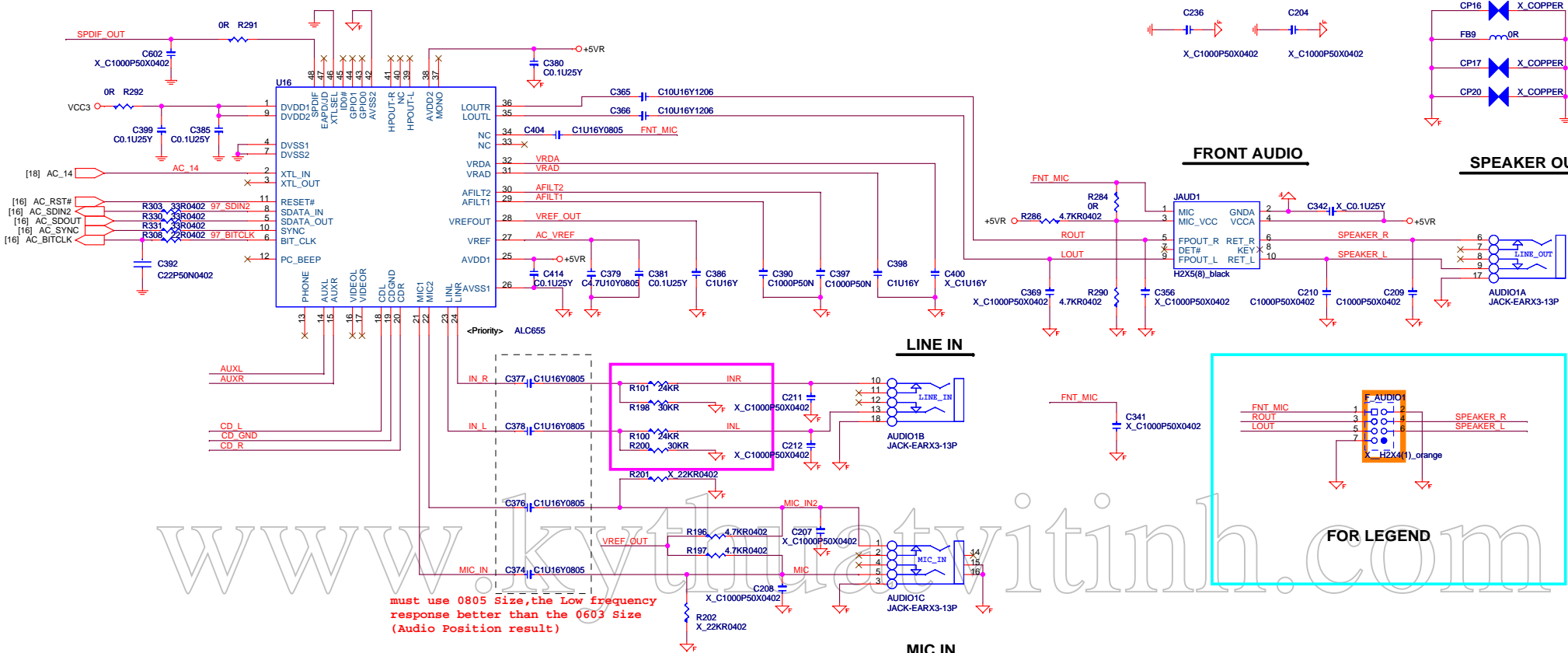
Size: **MS-7177**

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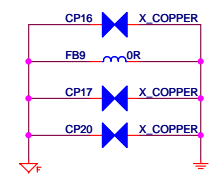
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AC'97 Codec -- ALC655

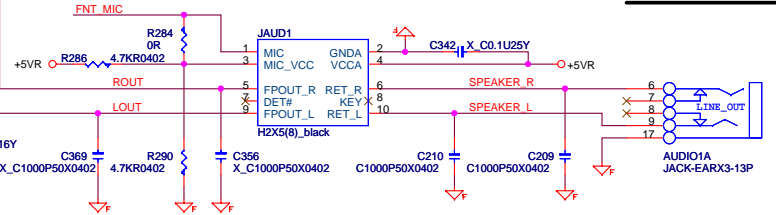


must use 0805 Size, the low frequency response better than the 0603 size (Audio Position result)

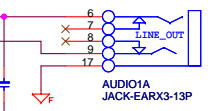
COPPER



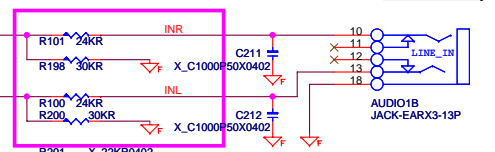
FRONT AUDIO



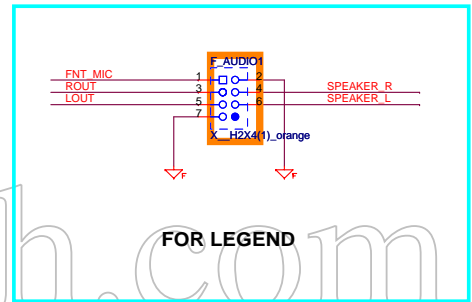
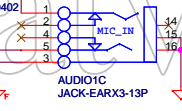
SPEAKER OUT



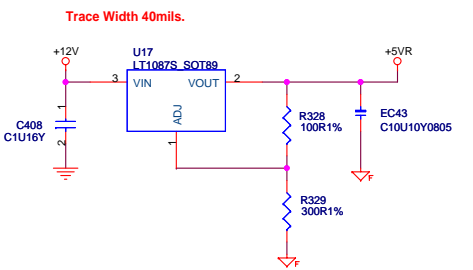
LINE IN



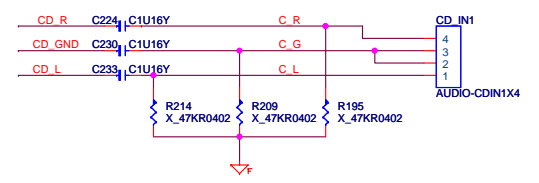
MIC IN



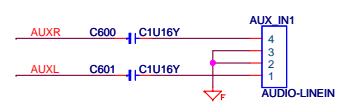
AUDIO CODE REGULATORS



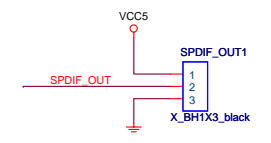
CD IN

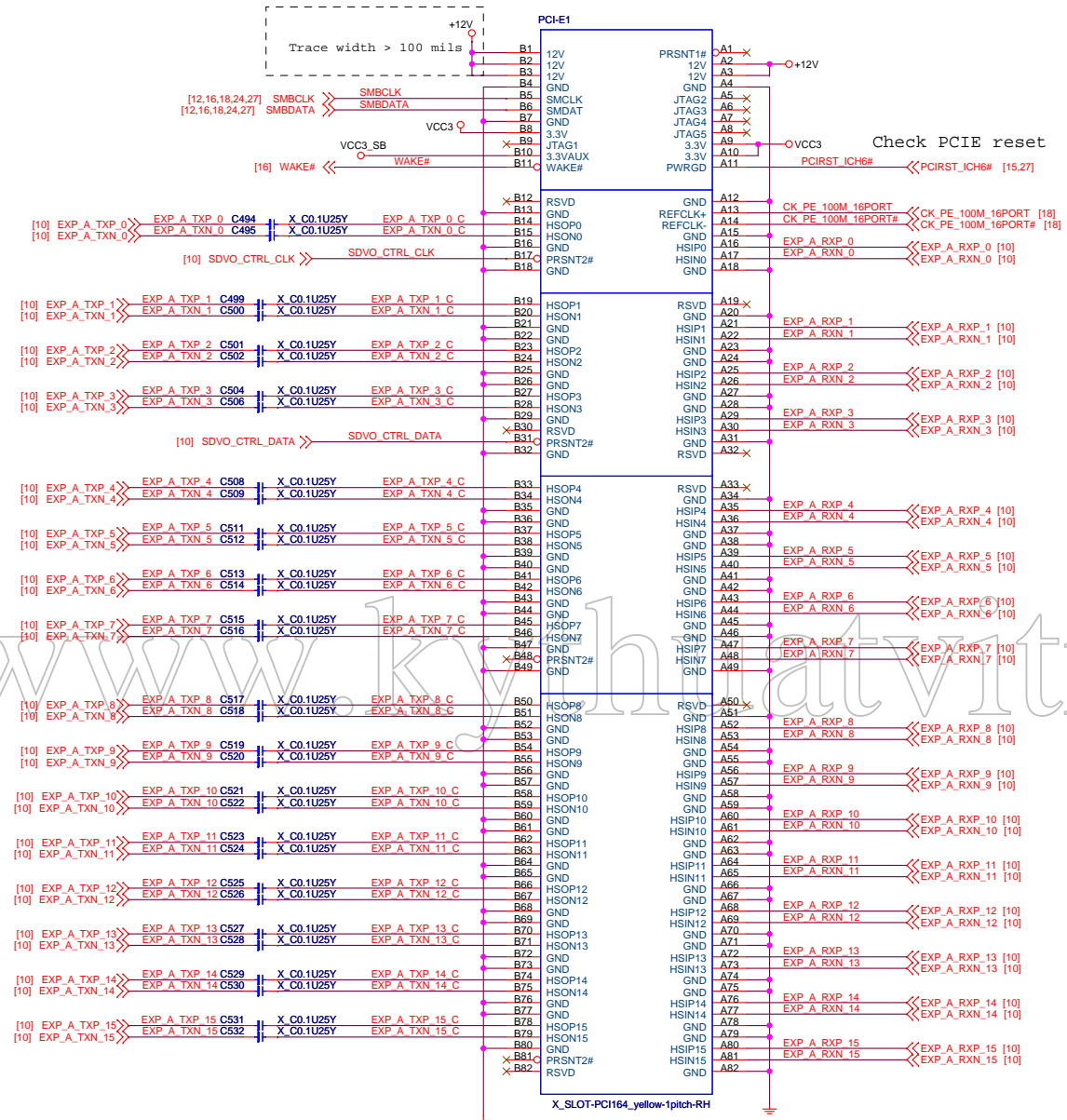


AUX IN

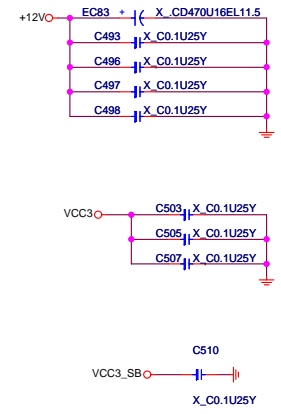


SPDIF Out

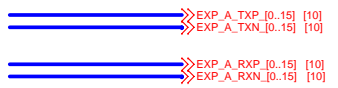




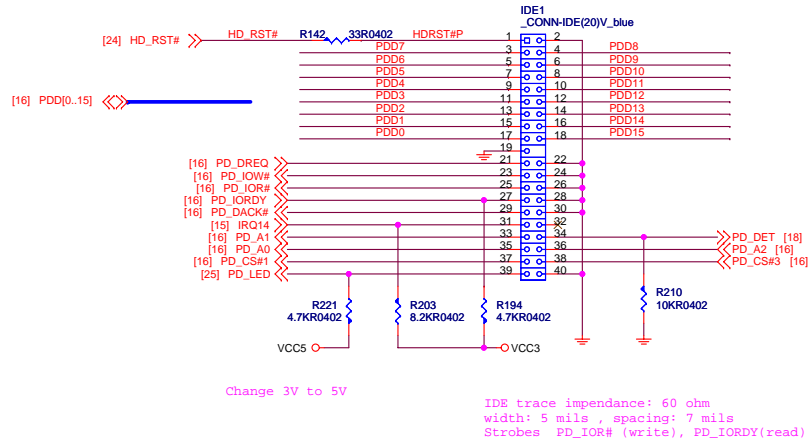
PCI EXPRESS 1-PORT



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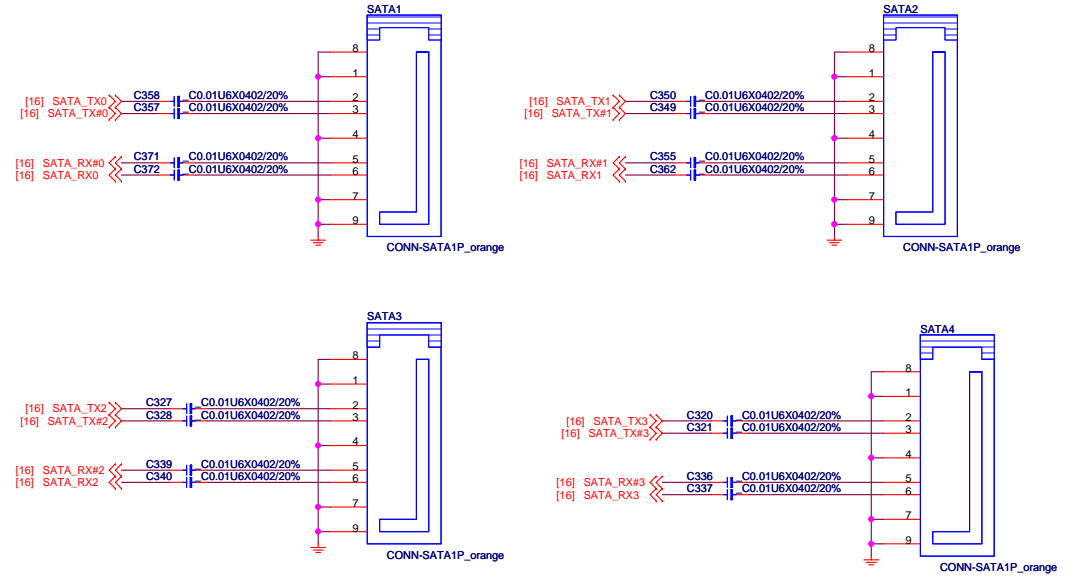


ATA 33/66/100 IDE Connectors

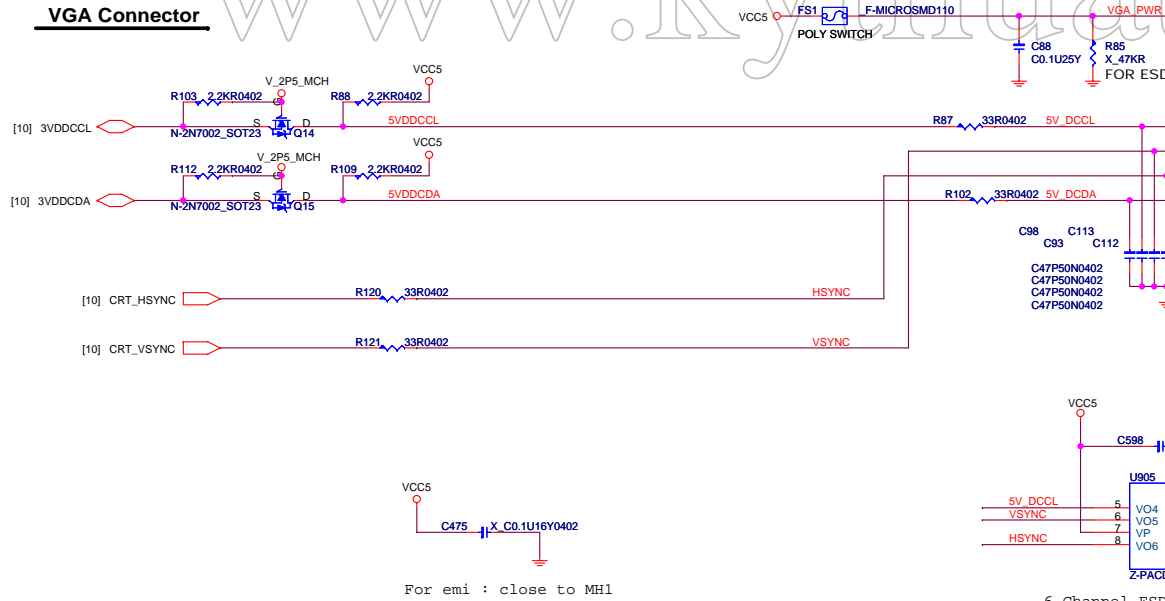


SATA CONNECTOR

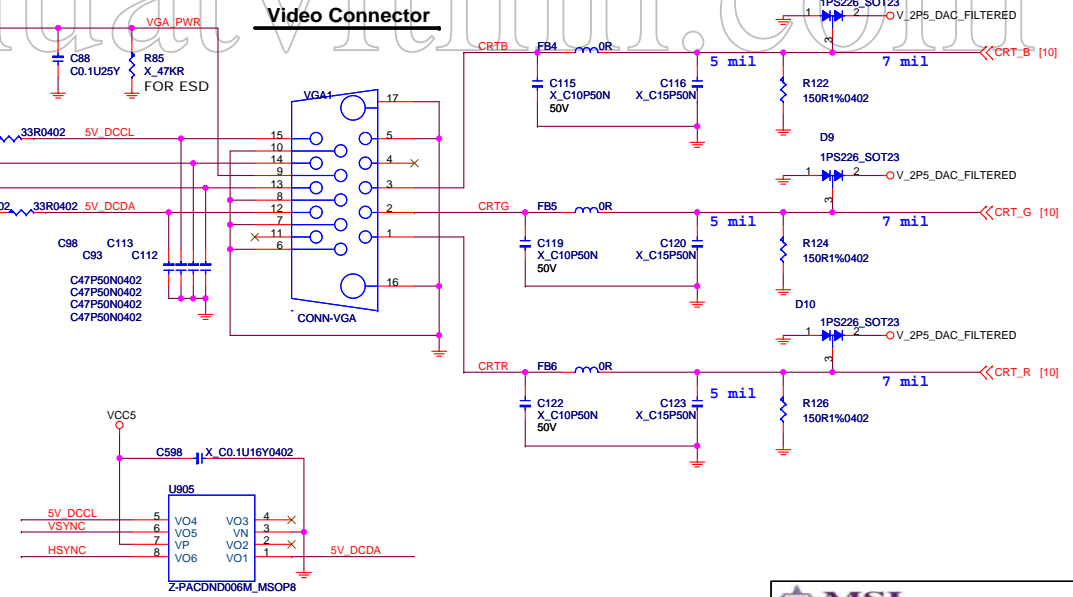
AC coupling Cap: 1nF - 10nF (place anywhere)
 SATA trace impedance: 100 ohm (5/7/5)
 Length mismatch: 20 mils



VGA Connector



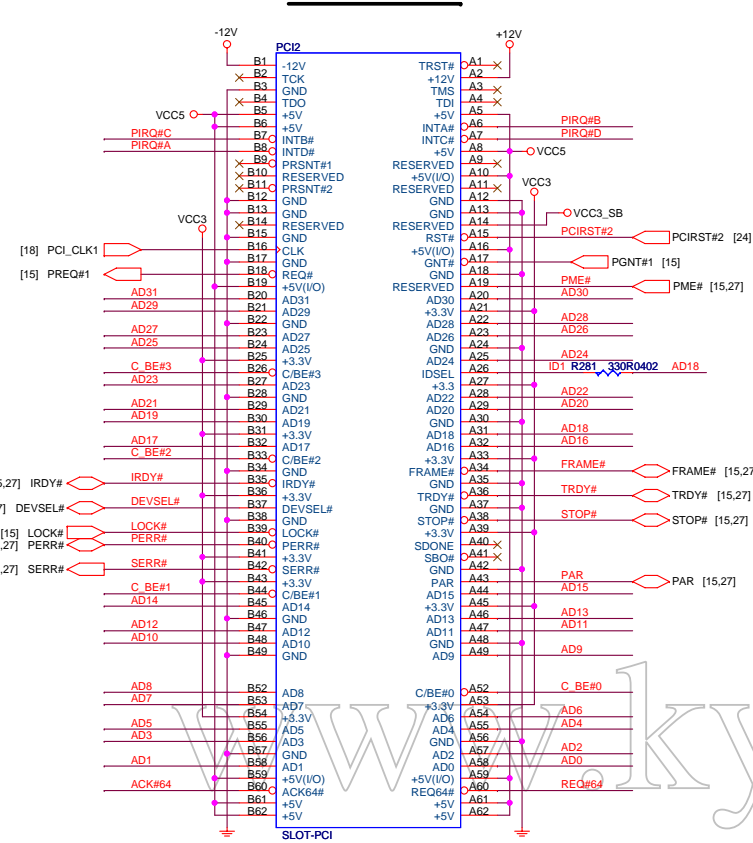
Video Connector



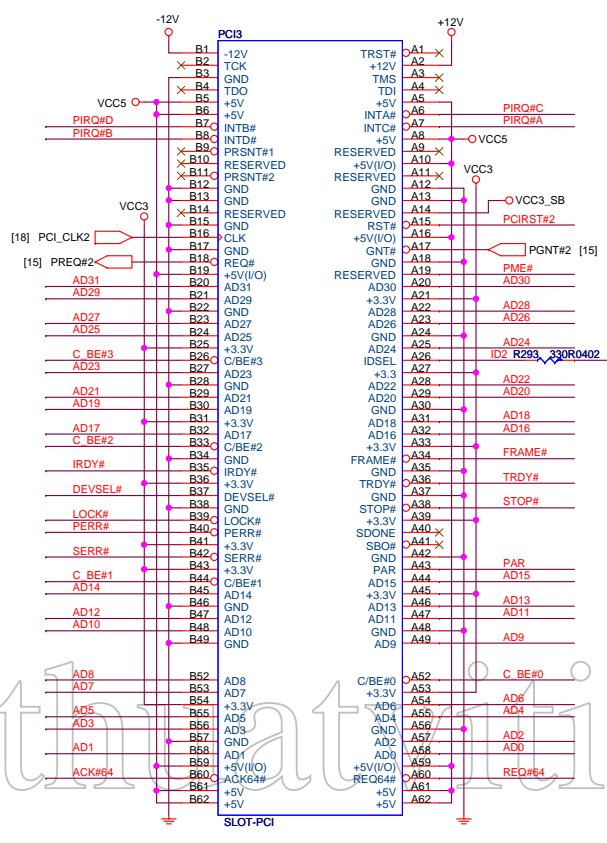
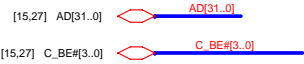
PCI SLOT 2

PCI SLOT 3

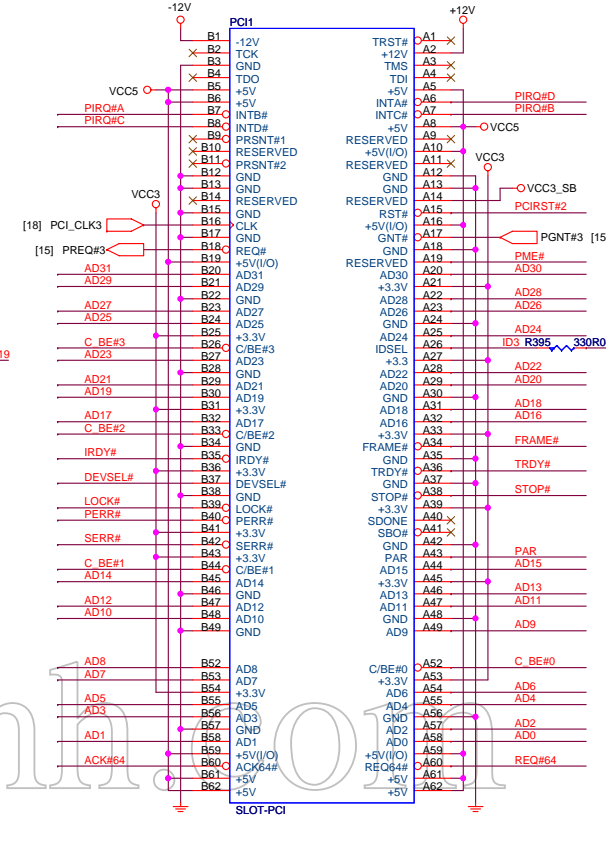
PCI SLOT 1



ISEL = AD18
 MASTER = PREQ#1
 PIRQ#B

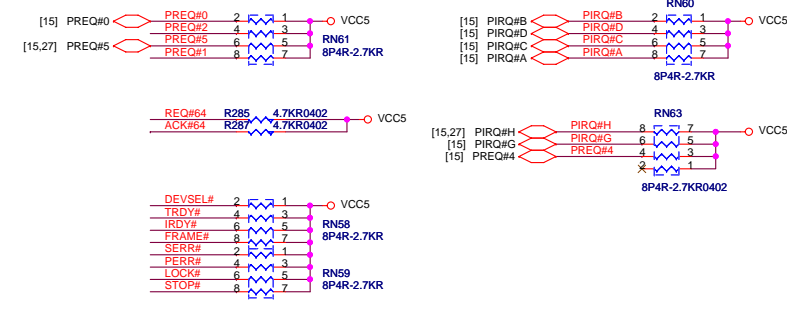


ISEL = AD19
 MASTER = PREQ#2
 PIRQ#C

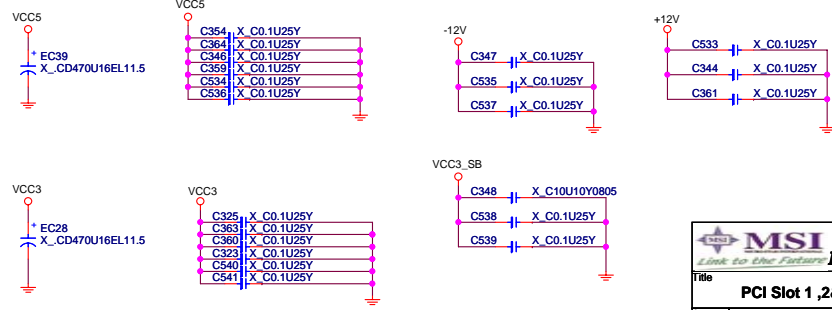


ISEL = AD20
 MASTER = PREQ#3
 PIRQ#D

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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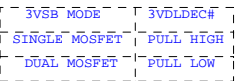
Title: **PCI Slot 1,2&3**

Size: Custom Document Number: **MS-7177** Rev: **20**

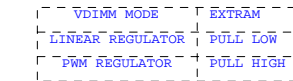
Date: Monday, July 11, 2005 Sheet: 23 of 33

ACPI Controller

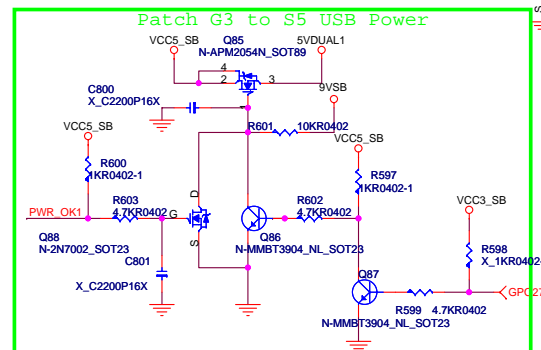
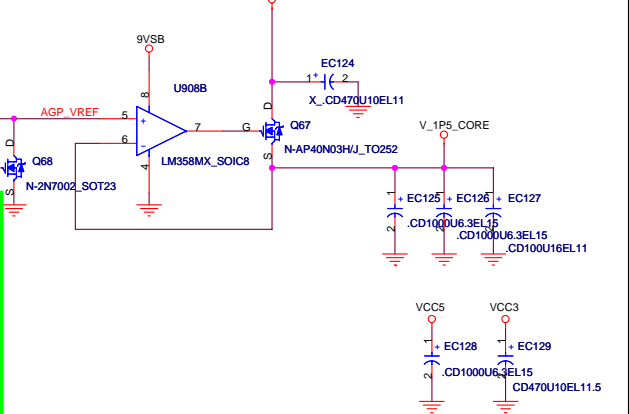
3VSB MODE SELECT



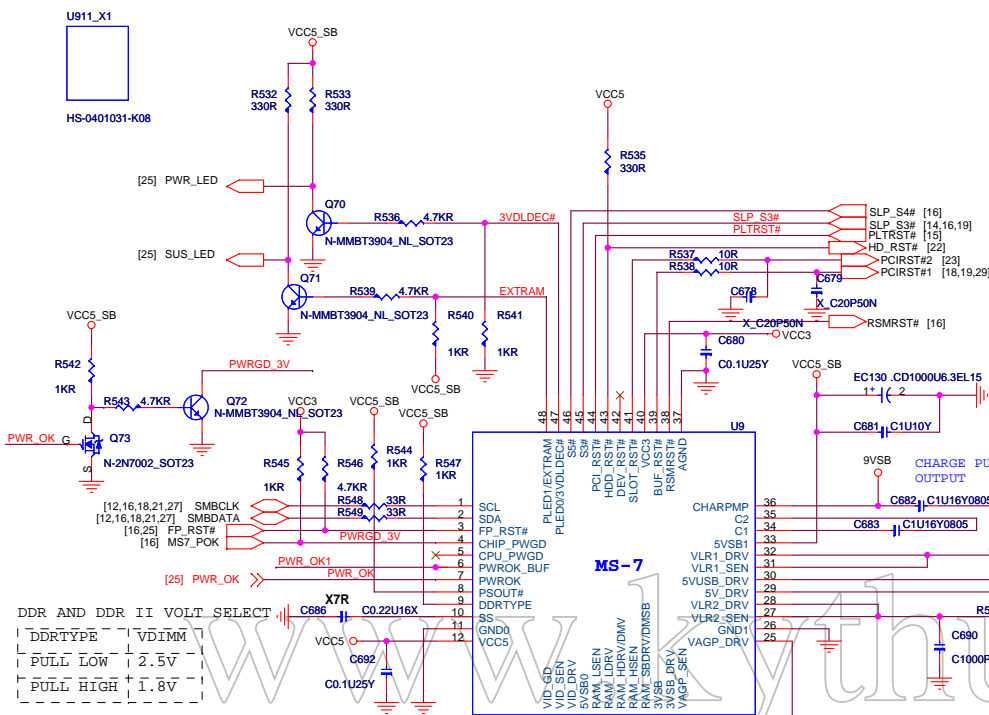
VDIMM LINEAR OR PWM SELECT



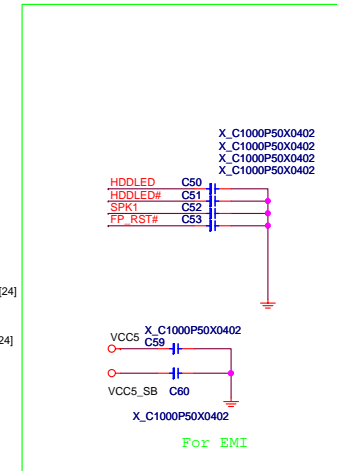
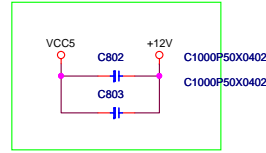
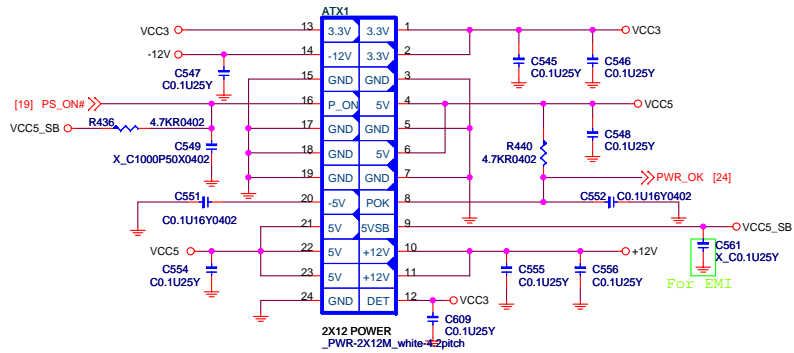
PCI-EX POWER



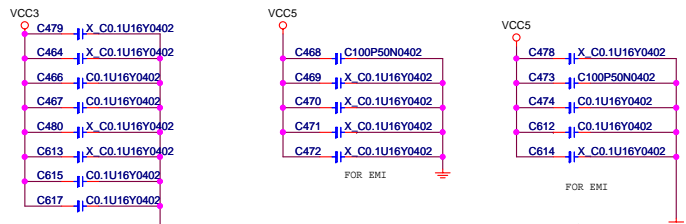
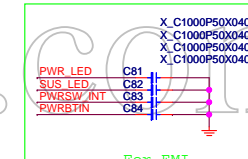
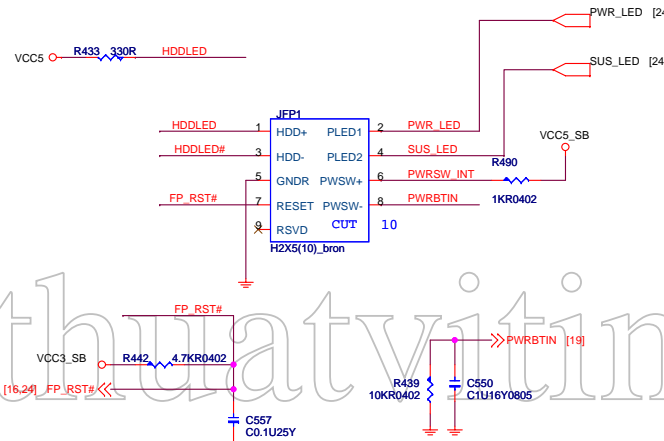
5V DUAL Power



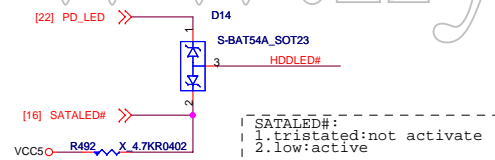
ATX Connector



INTEL/PB Front Panel Connector

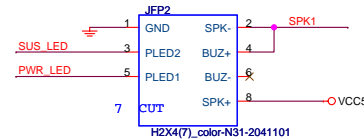
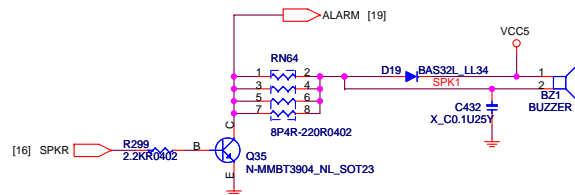


C466, C467, C615, C617, C474, C612 for clock & signal layer jump.



SATALED#:
1. tristated: not activate
2. low: active

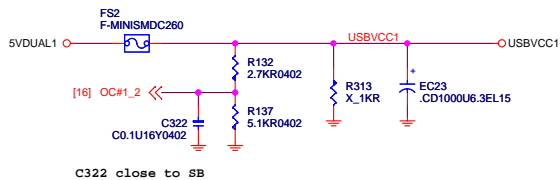
MSI Front Panel Connector



SPKR: ICH6 integrated pull-down, only enable at boot/reset for strapping functions; at other time is disabled.

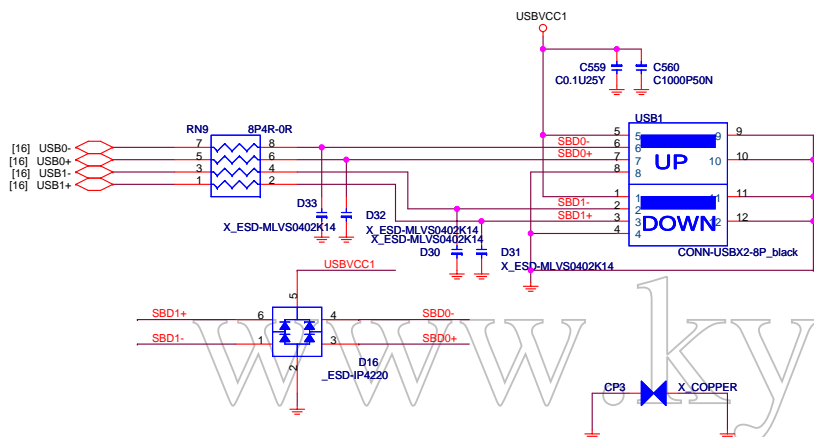
Rear USB

POWER CIRCUIT FOR USB PORT 0,1,2,3

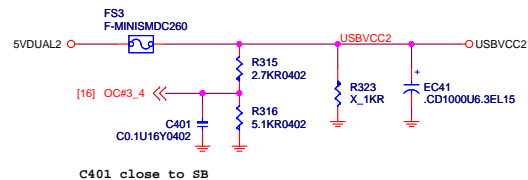


C322,C401 close to SB
 EC23, EC41 close to USB connector
 R313, R323: for ESD
 OC# [7:0] are 3.3V level

REAR PANEL USB CONNECTOR FOR USB PORT 0,1

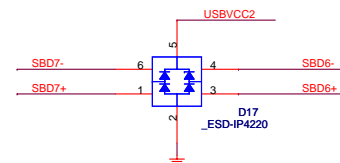
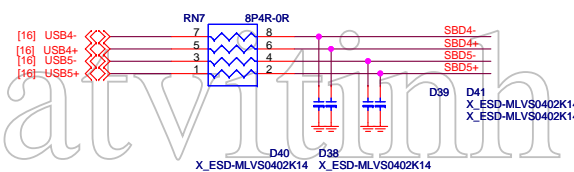


Front USB

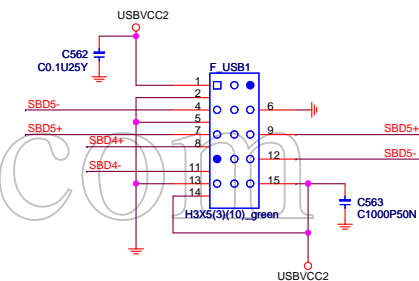


C401 close to SB

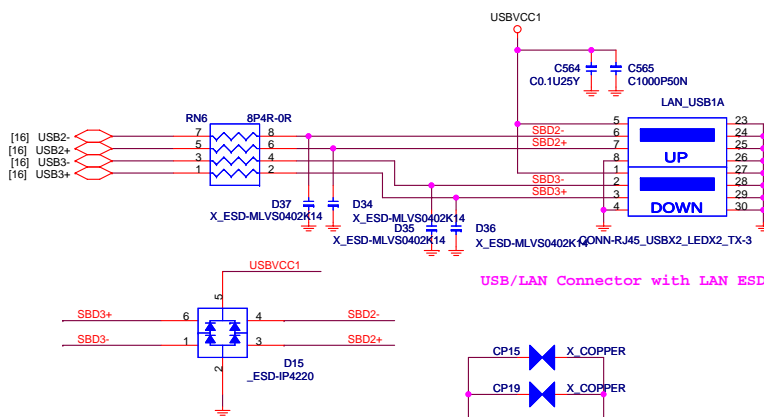
Front PANEL USB CONNECTOR FOR USB PORT 4,5



LENOVO Front USB Header

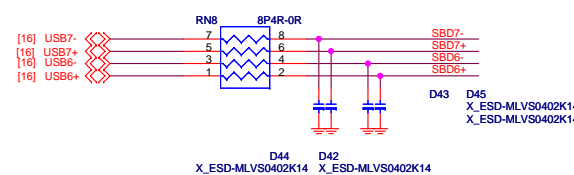


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

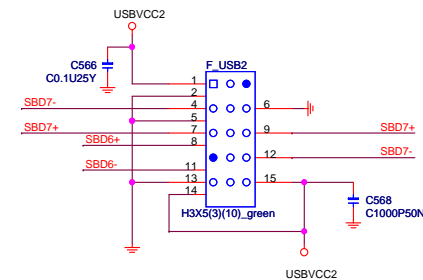


USB/LAN Connector with LAN ESD solution

Front PANEL USB CONNECTOR FOR USB PORT 6,7



LENOVO Front USB Header



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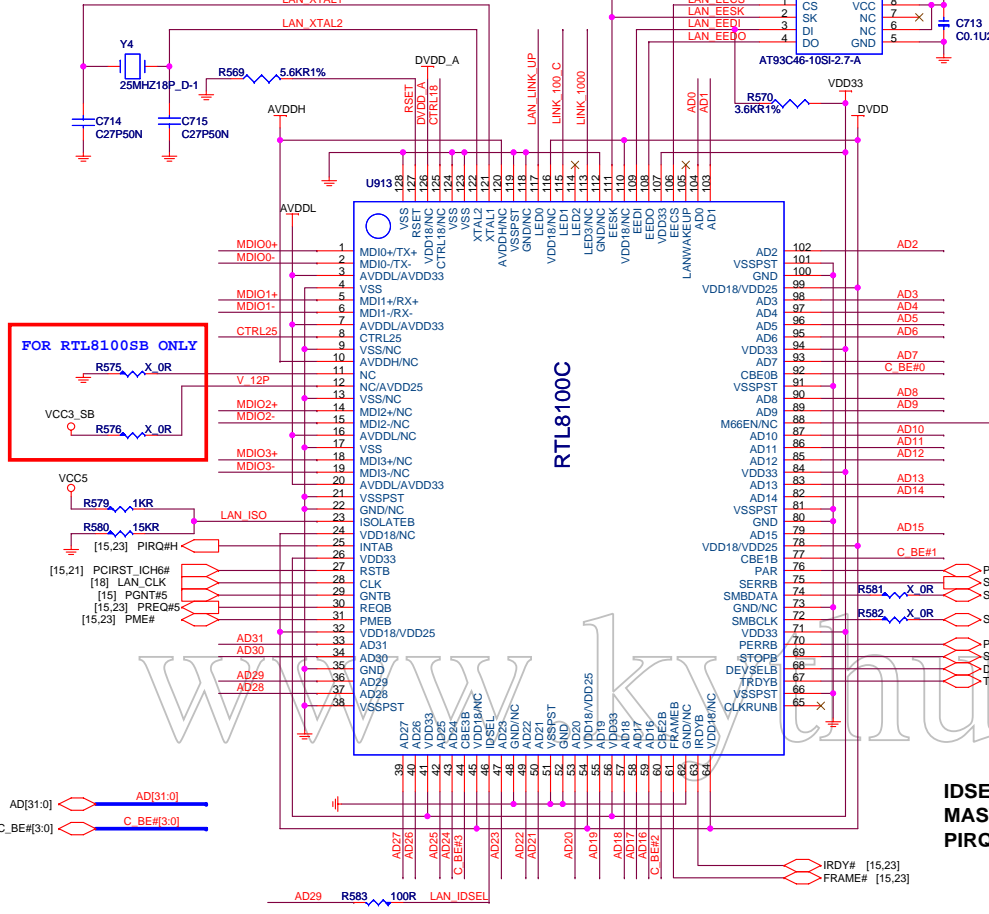
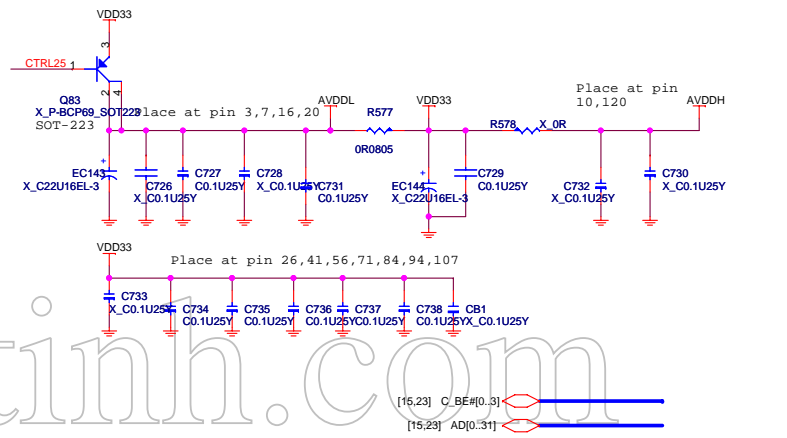
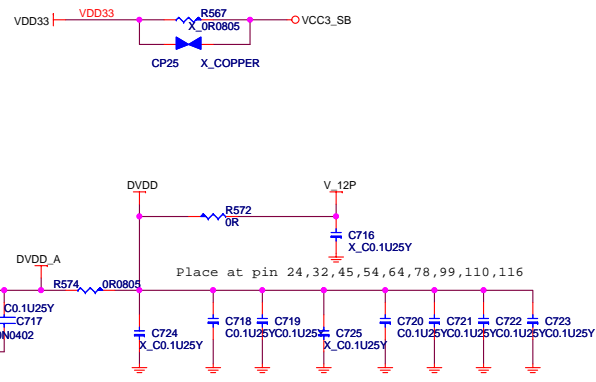
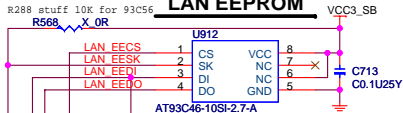
Title: **USB CONNECTORS**

Size	Document Number	Rev
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PCI LAN RTL8110S/8100C

R858[RSET]: 2.49K for 8110S
5.6K for 8100C

LAN EEPROM



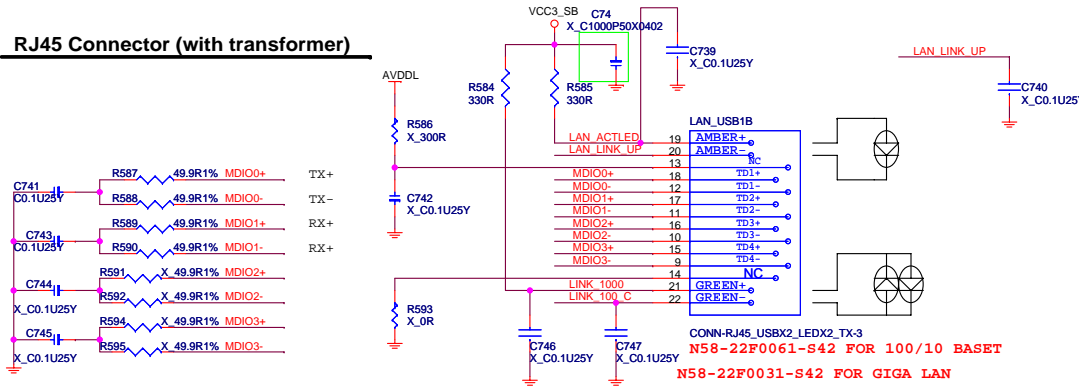
FOR RTL8100SB ONLY

IDSEL = AD29
MASTER = PREQ#6
PIRQ#H

1- MDIO+ & MDIO- pairs should be 100-ohm differential impedance. Route equal length and symmetrically. Separate every pairs.

	DVDD	DVDDA	AVDDL	AVDDH	V-12P	
8100C	2.5V	2.5V	3.3V	X	2.5V	
8110S	1.8V	1.8V	2.5V	3.3V	X	
ADD PIN1,12	8110SB	1.8V	1.8V	2.5V	3.3V	3.3V

RJ45 Connector (with transformer)



Part Value Selection:
GbE: 8110S LAN(1000M)
TE: 8100C LAN(10/100M)
L: With LAN option
X: No Stuff

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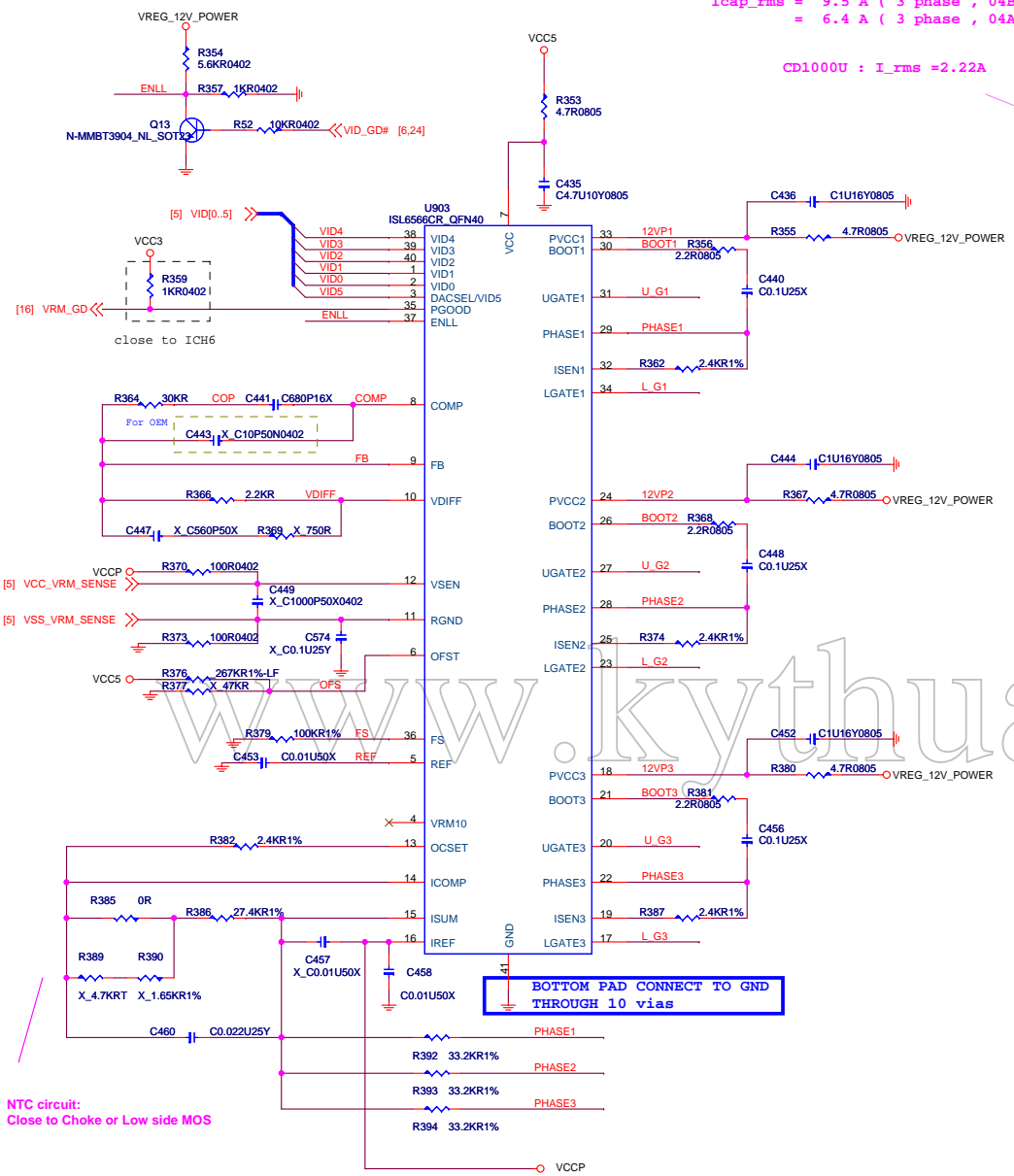
Title: **LAN_RTL8100C/RTL8110S**

Size: Custom Document Number: **MS-7177** Rev: **20**

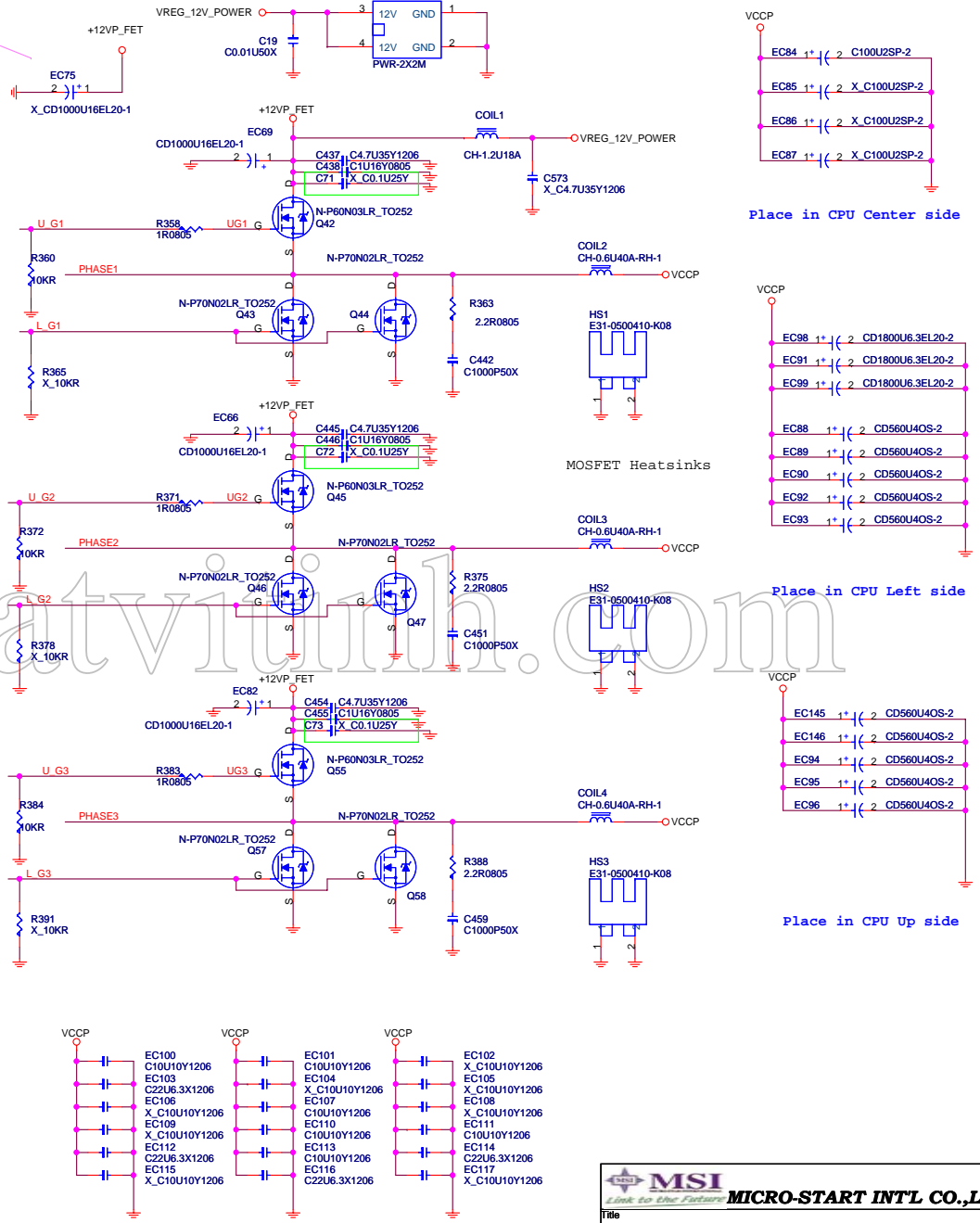
Date: Monday, July 11, 2005 Sheet: 27 of 33

Set at 85 degree :
 $I_{cap_rms} = 9.5 \text{ A (3 phase , 04B spec)} \rightarrow 4 \text{ caps}$
 $= 6.4 \text{ A (3 phase , 04A spec)} \rightarrow 3 \text{ caps}$

CD1000U : $I_{rms} = 2.22\text{A}$



NTC circuit:
 Close to Choke or Low side MOS

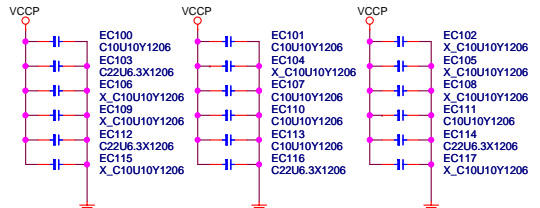


Place in CPU Center side

Place in CPU Left side

Place in CPU Up side

MOSFET Heatsinks

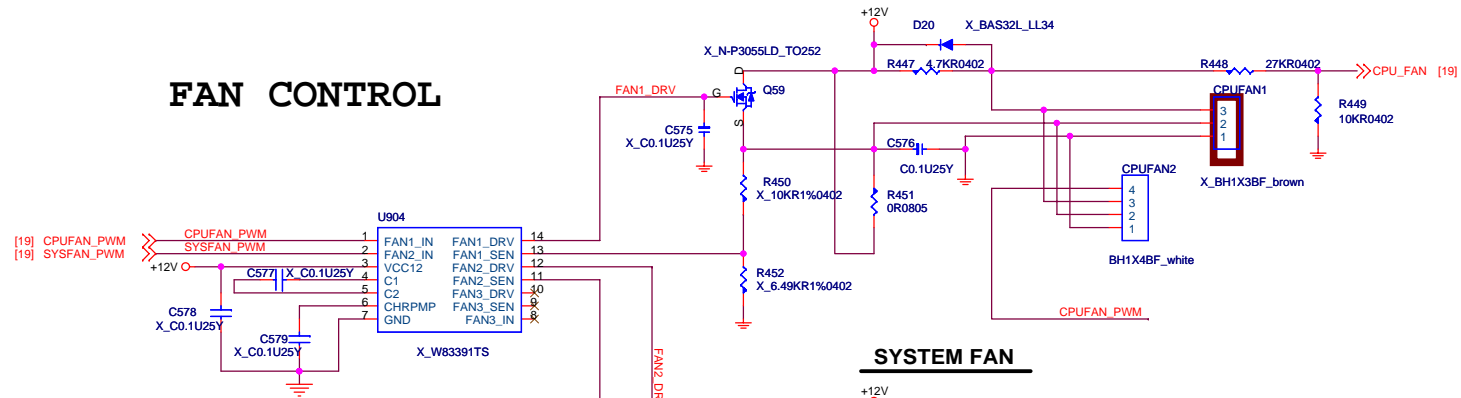


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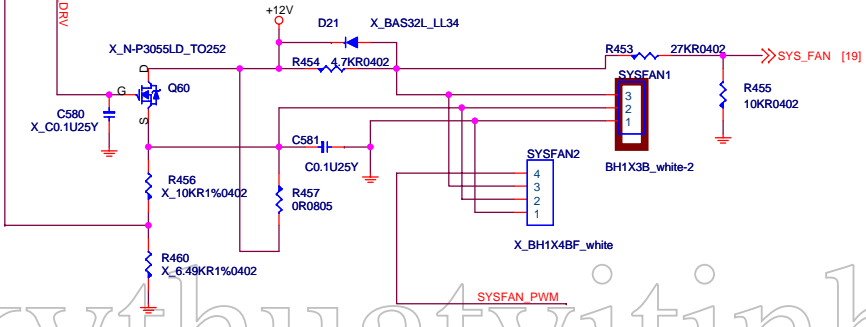
Title: **VRM10 INTERSIL 6566**

Size	Document Number	Rev
Custom	MS-7177	20
Date:	Monday, July 11, 2005	Sheet 28 of 33

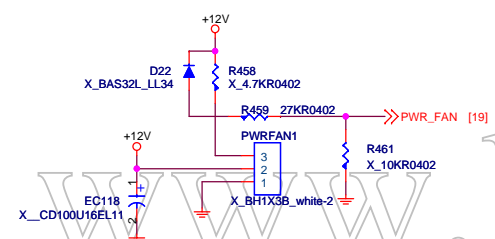
FAN CONTROL



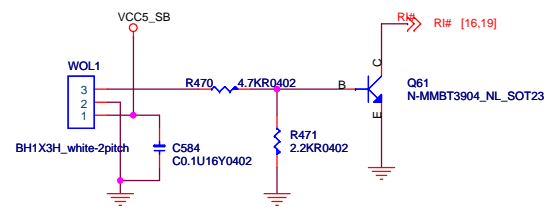
SYSTEM FAN



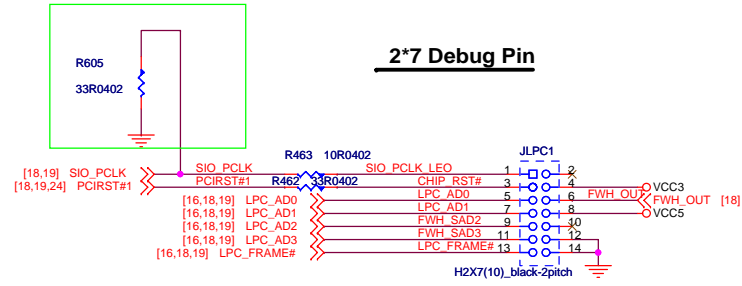
POWER FAN



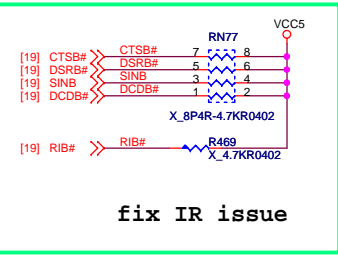
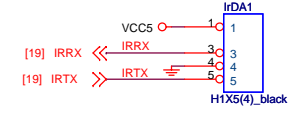
Wake on LAN



2*7 Debug Pin



IR HEADER



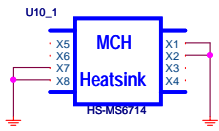
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Title: **FAN**

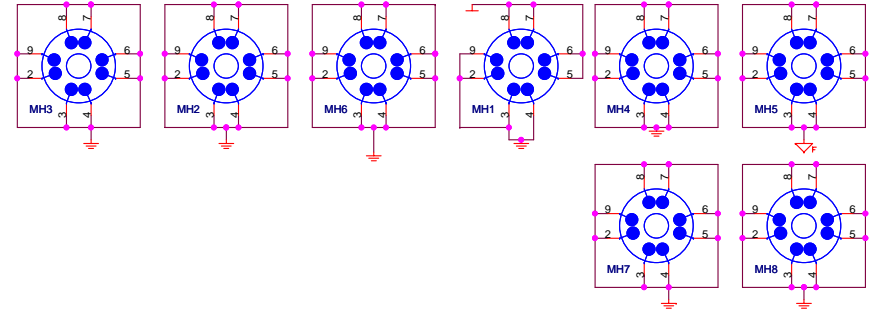
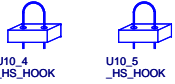
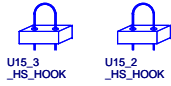
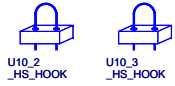
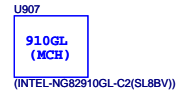
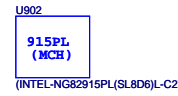
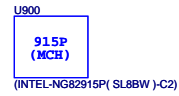
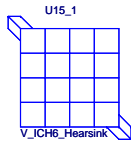
Size: Custom
Document Number: **MS-7177**

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Sheet: 29 of 33

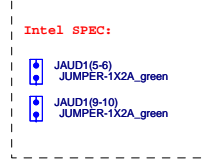
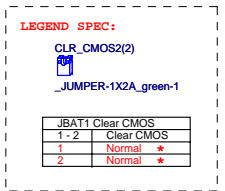
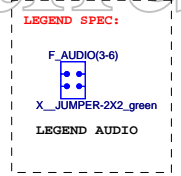
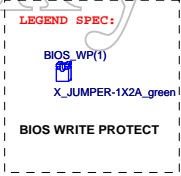
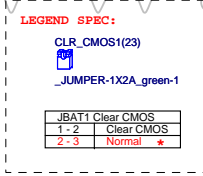
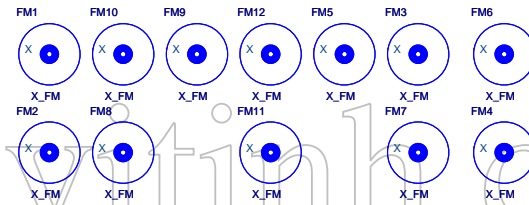
Jumper Setting / Manual Part



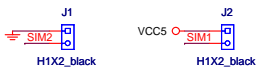
E31-0401101-K08 for 8 pin

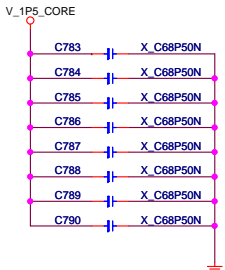
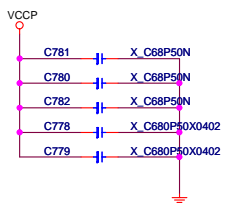
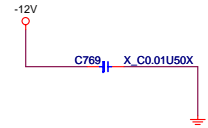
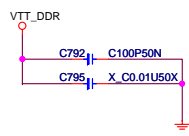
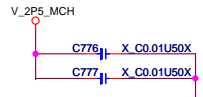
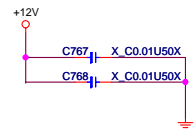
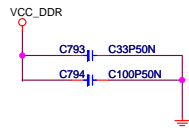
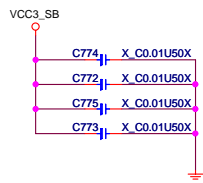
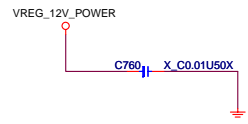
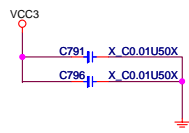
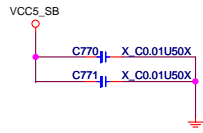
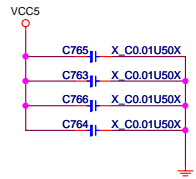


Optics Orientation Holes



Simulation





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Title: **For EMI**

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MS-7177 Config setting:

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