

PRAHA EXT GFX

CPU : Intel Merom (800MHz)
 Chip Set : RS600ME & SB600
 Remarks : Mobility Platform

Model Name : PRAHA EXT GFX
 PBA Name : MAIN
 PCB Code : NANYA:BA41-00806A
 GCE : BA41-00812A
 TPT : BA41-00814A
 Dev. Step : PR2 (8-Layer)
 Revision : 1.0
 T.R. Date : 2007.06.24

DRAW	CHECK	APPROVAL

■ Owner : SEC Mobile R & D Signature : X

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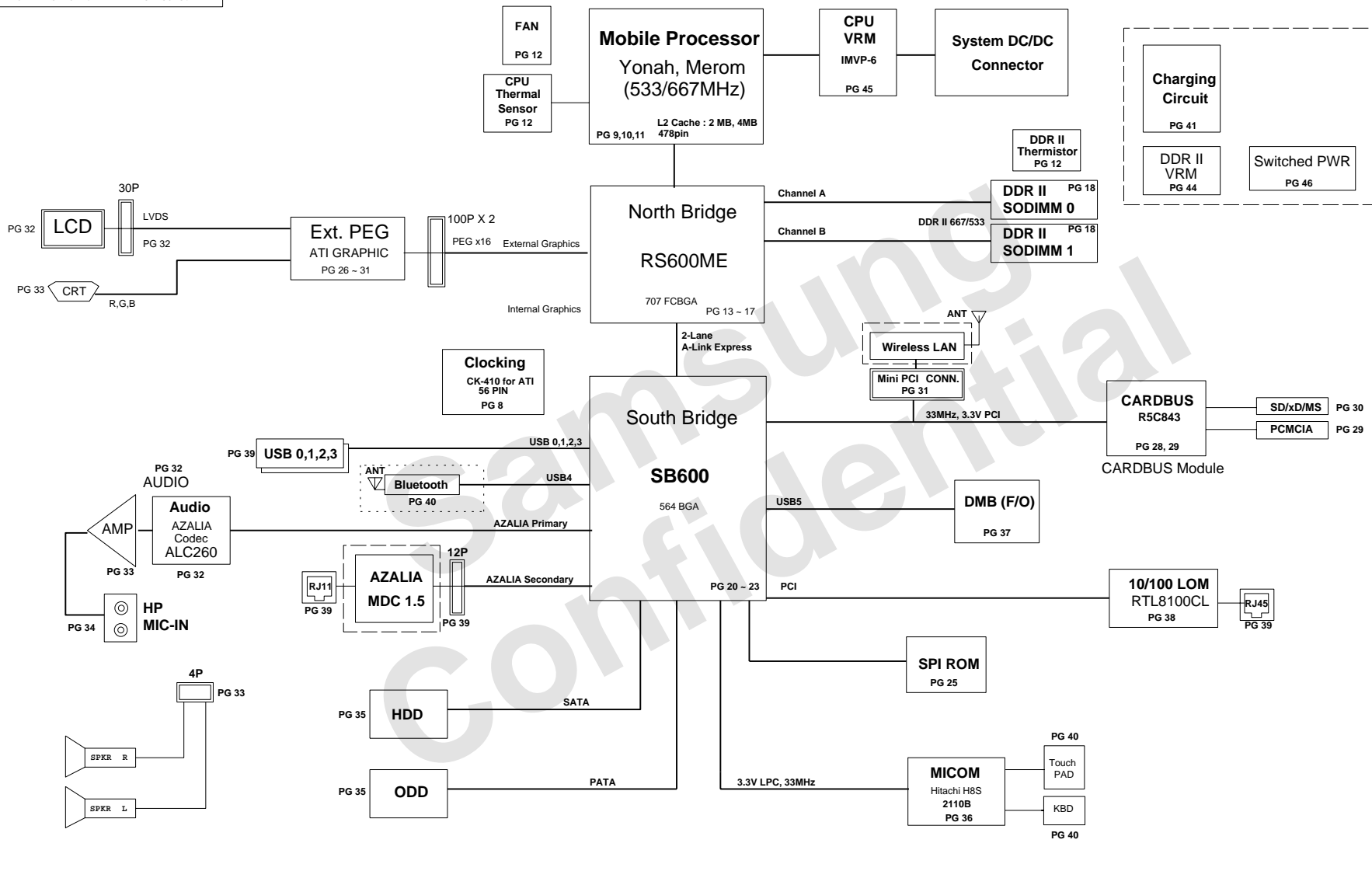
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USE ICT PORT

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	COVER	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-00806A	
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	1 OF 54	

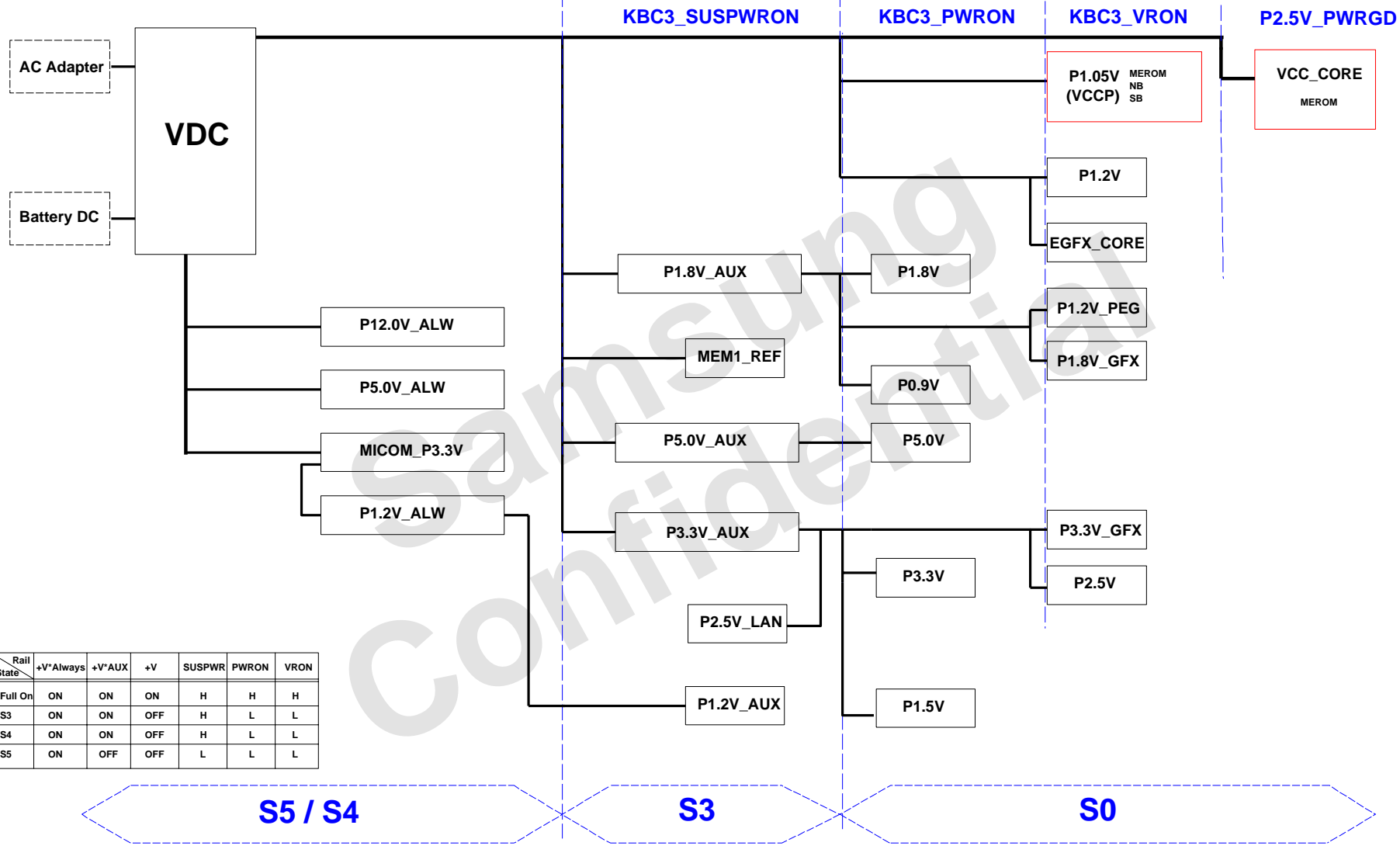
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DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	OPERATION BLOCK DIAGRAM		PART NO. BA41-00806A
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	2	OF 54

Power Diagram

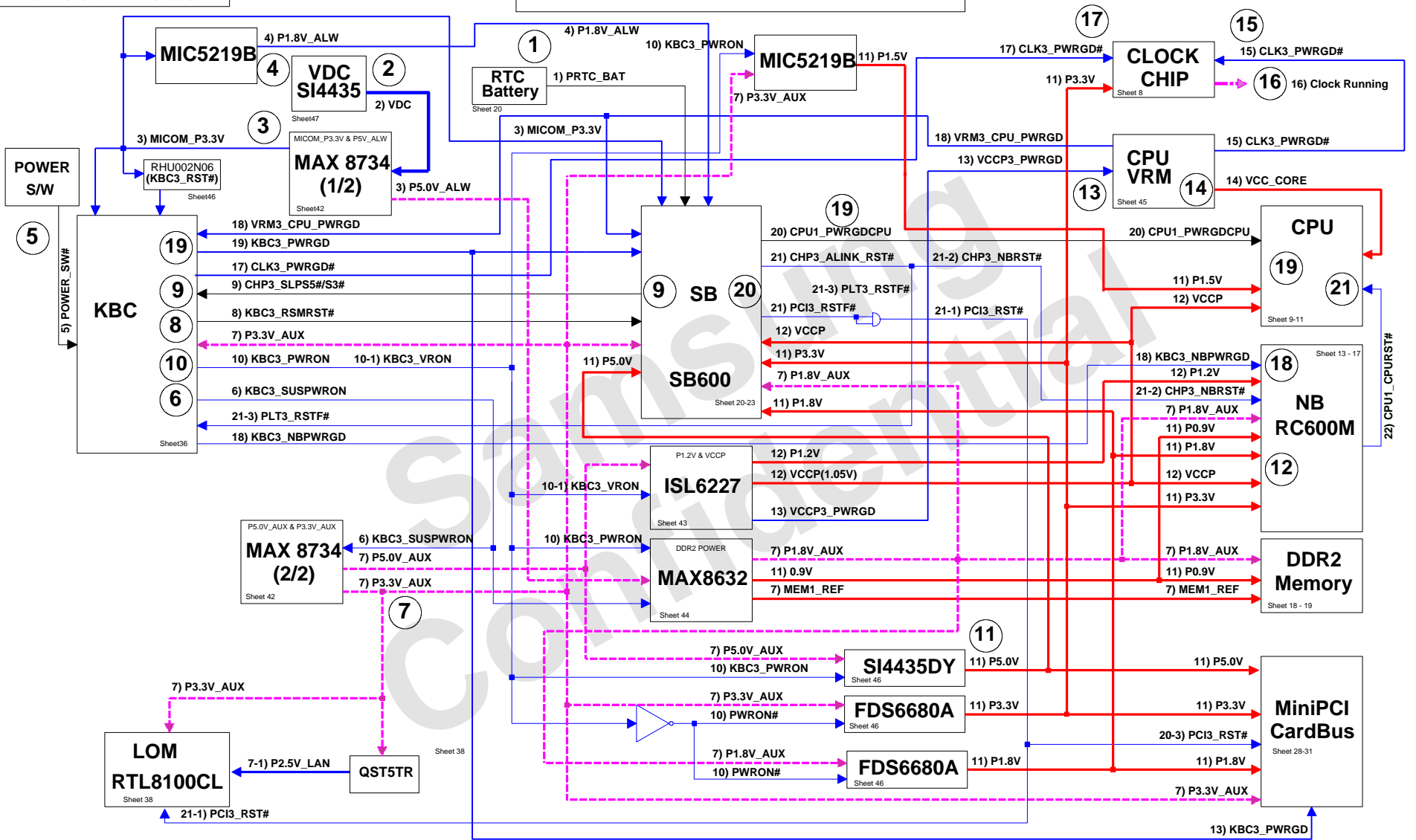


Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	POWER DIAGRAM	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-00806A	
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	3	OF 54

POWER SEQUENCE Rev. 0.1



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0	POWER SEQUENCE		
MODULE CODE		LAST EDIT				
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DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT CLOCK DIAGRAM	SAMSUNG ELECTRONICS	
CHECK	SS BAIK	DEV. STEP	PR	PART NO.			BA41-00806A
APPROVAL	KK BIN	REV	1.0				
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE			5 OF 54

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A, B, C
LAN	AD21	1	D
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (0-1.5V)
VCCP	YONAH Processor System Bus(PSB) Termination (1.05V)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P1.8V_ALWS	1.8V power rail (Always On)
P2.5V_LAN	2.5V power rail (off in S4-S5)
MICOM_P3.3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P5.0V_ALWS	5.0V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I²C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
SODIMM0	1010 0100	A4h	-
SODIMM1	1010 0110	A6h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	HBS-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table IMVP-6

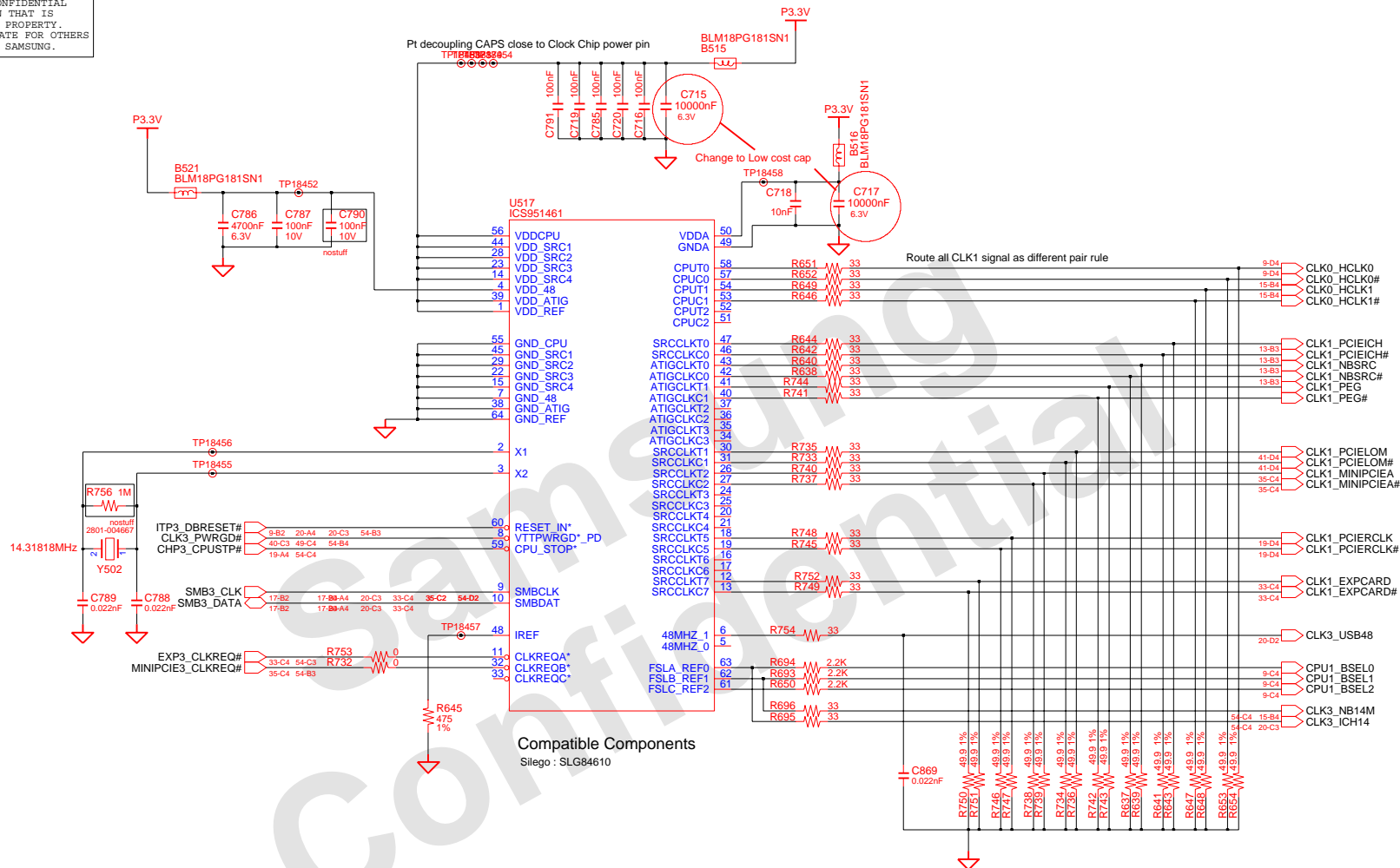
Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 1 0 0 0	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 1	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 1 0	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 1	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 1 0 0	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 1	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 1 0	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 1	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 1 0 0 0 0	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 1	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 1 0	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 1	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 1 0 0	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 1	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 1 0	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 1	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP* 1, PSI2* 0 or 1
Deeper Slp: DPRSLPVR 1, DPRSTP* 0, PSI2* 0 or 1

11111111 : OV power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAH_A_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0	BOARD INFORMATION		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		May 28, 2007 10:24:00 AM	PAGE	6 OF 54



Compatible Components
Silego : SLG84610

Place all te serias termination resistor as close as Clock Chip as possible

FSA, FSB, FSC of Clock chip are low threshold inputs
Vih_fs_min = 0.7V
Vil_fs_max = 0.35V

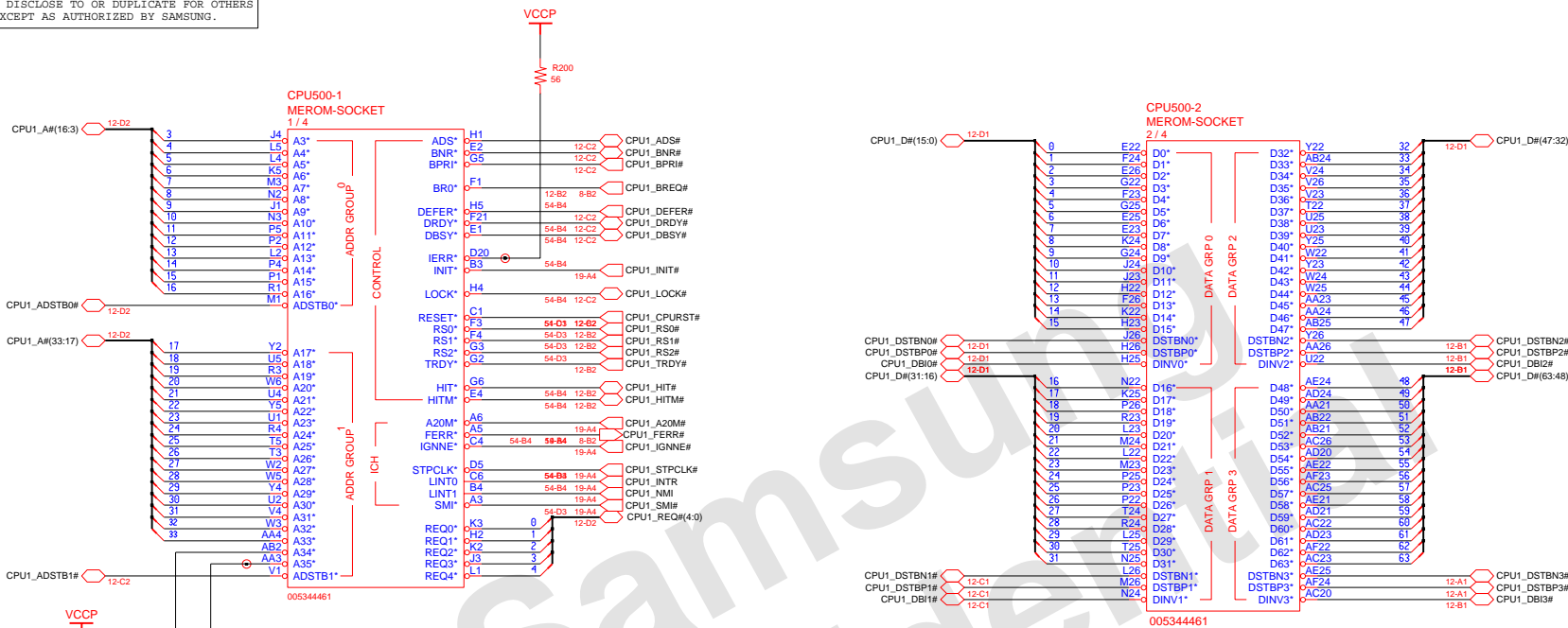
CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

Celeron 533MHz
Yonah 667MHz

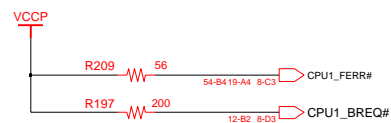
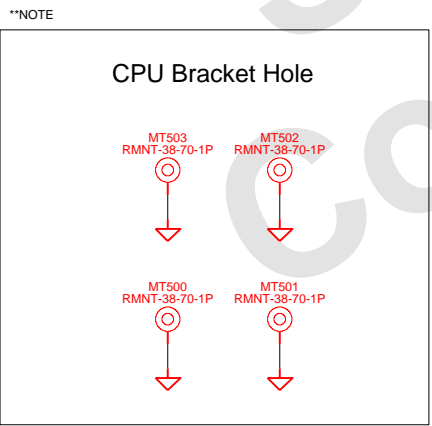
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CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		CLOCK GENERATOR	PART NO. BA41-00806A
MODULE CODE		LAST EDIT				

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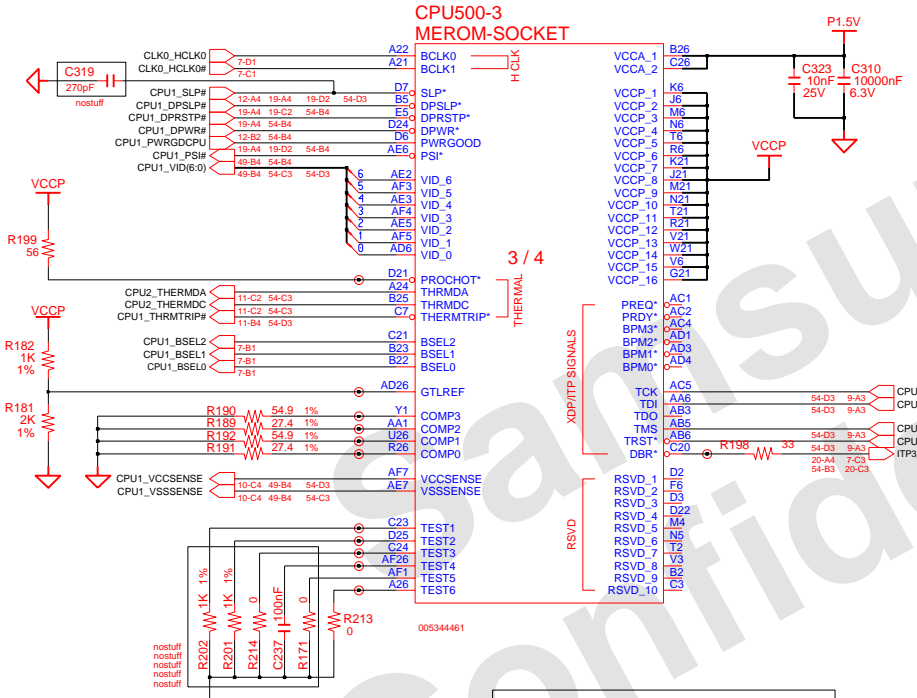


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DRAW	KI IM	DATE	5/28/2007	FILE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	MEROM CPU (1/3)		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		May 28, 2007 10:24:00 AM	PAGE	8 OF 54

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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	0 1 0 1 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 1 0 0 0 0	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 1	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 0 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 0 1 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 0	1.0125 V	1 0 0 1 1 1 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP* 1, PSI2* 0 or 1
 Deeper Slp: DPRSLPVR 1, DPRSTP* 0, PSI2* 0 or 1

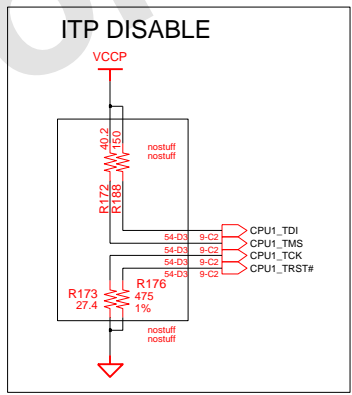
***"1111111": 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

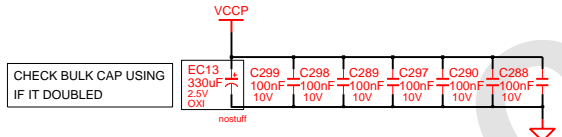
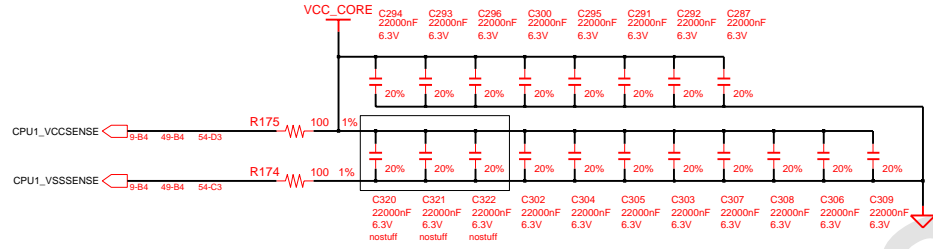
GND test points within 100mil of the VCC/VSSense at the end of the line. Route the VCC/VSSense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.



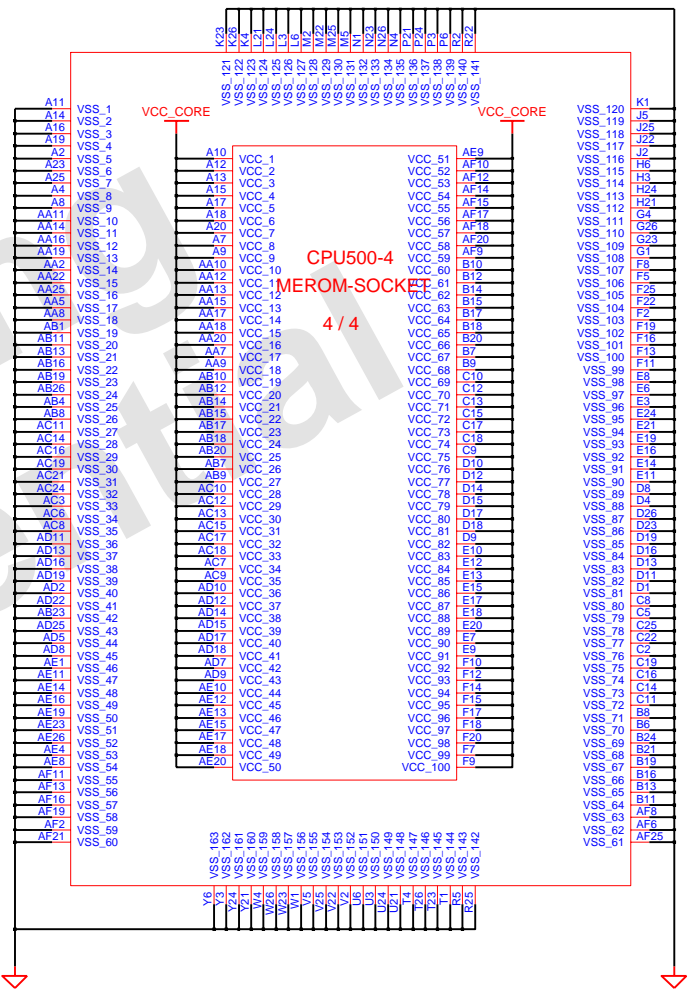
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CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		MEROM CPU(2/3)	PART NO. BA41-00806A
MODULE CODE		LAST EDIT				

May 28, 2007 10:24:00 AM PAGE 9 OF 54

Deleted 13 De-cap (Only use 19pcs out of 32)

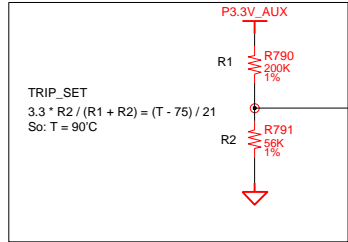
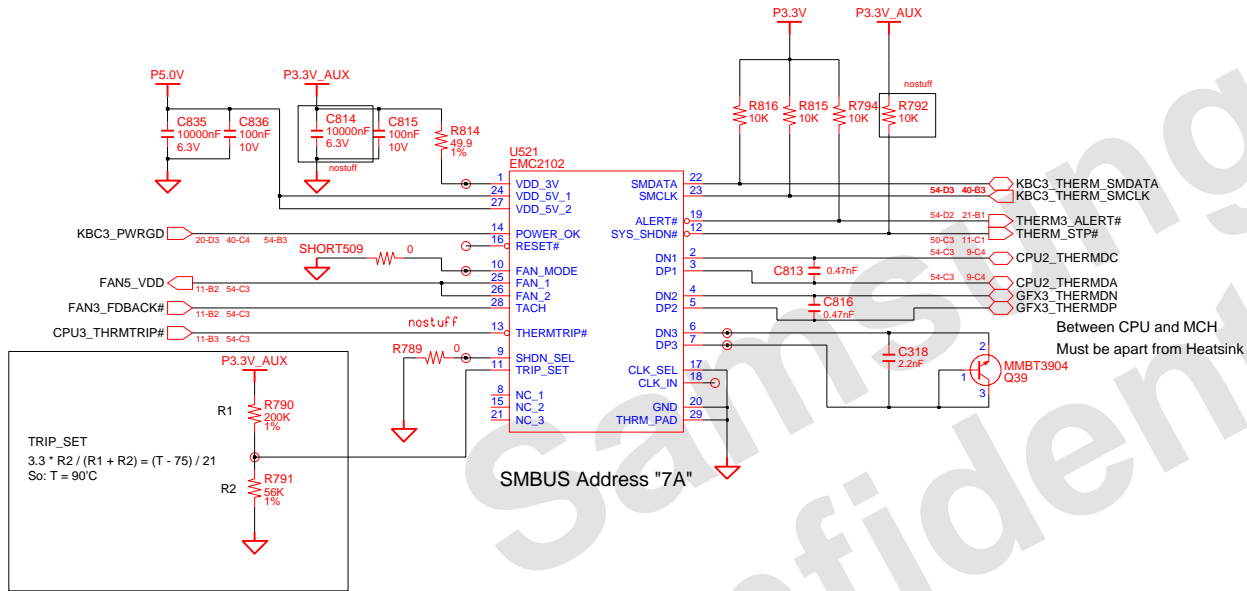


CHECK BULK CAP USING
IF IT DOUBLED

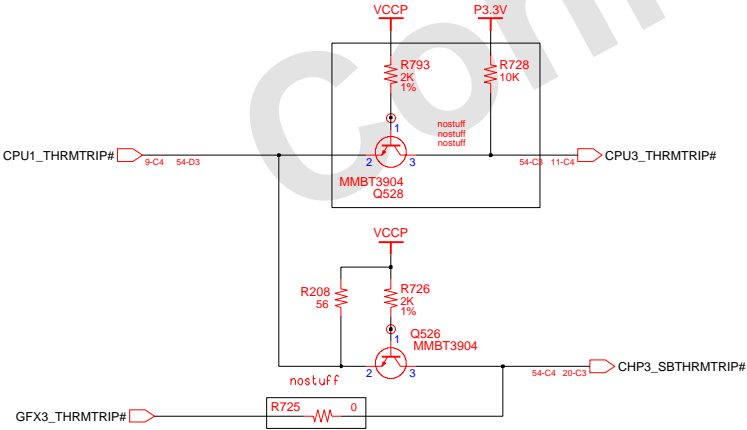


DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	MEROM CPU(3/3)		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		May 28, 2007 10:24:00 AM	PAGE	10 OF 54

Thermal Monitor

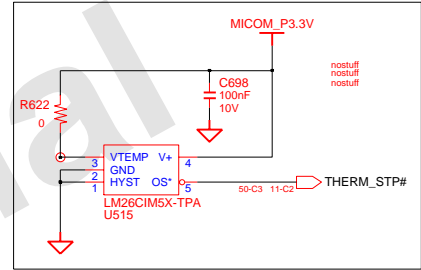


SMBUS Address "7A"

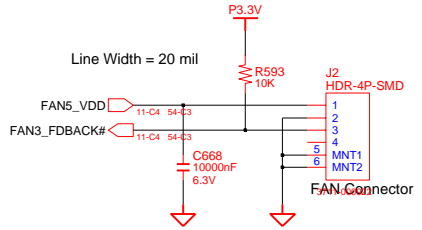


- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V) bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND

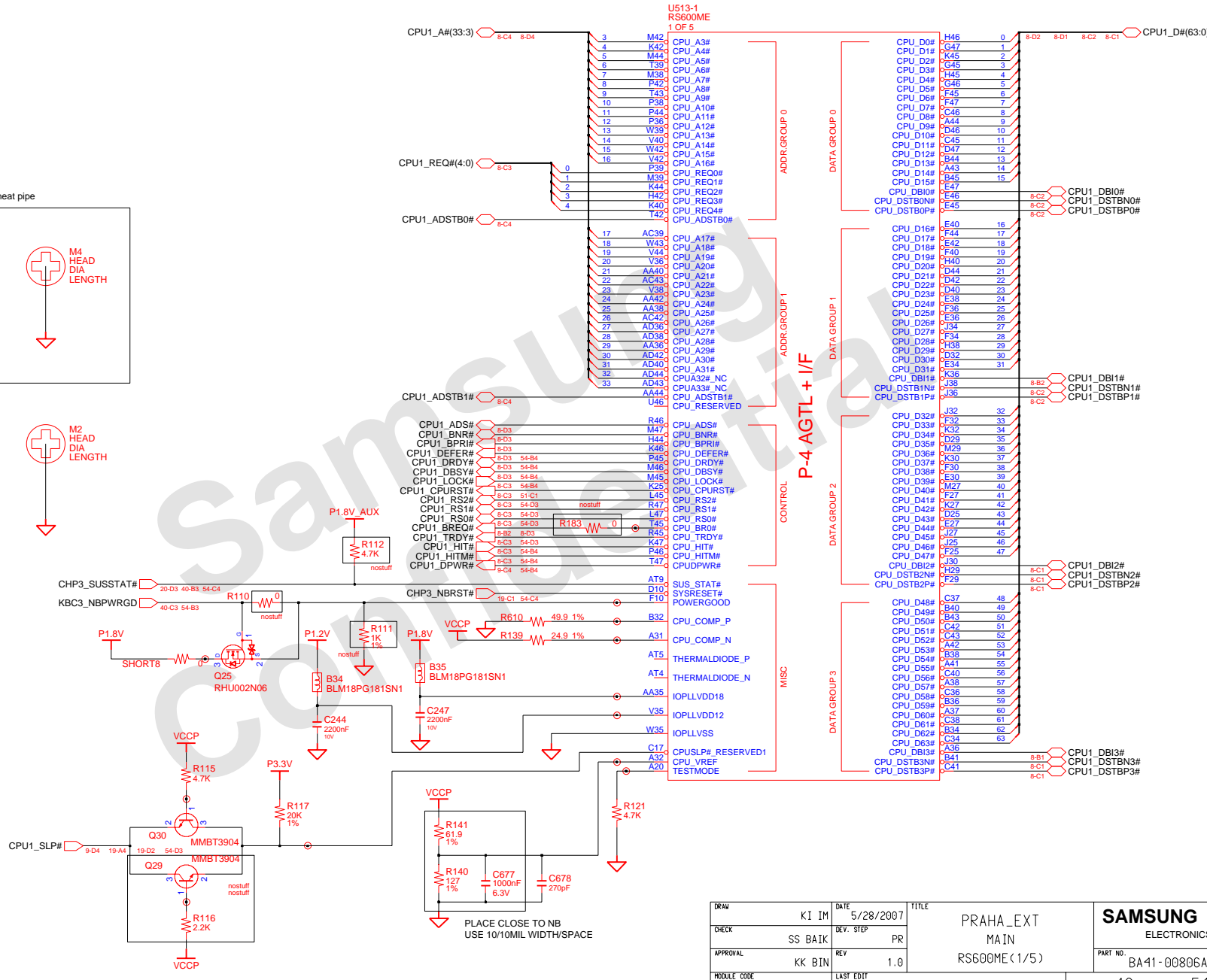
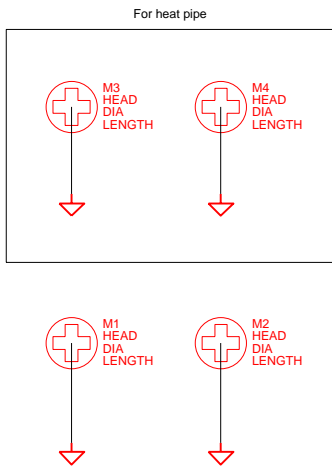
OTP (NOSTUFF)



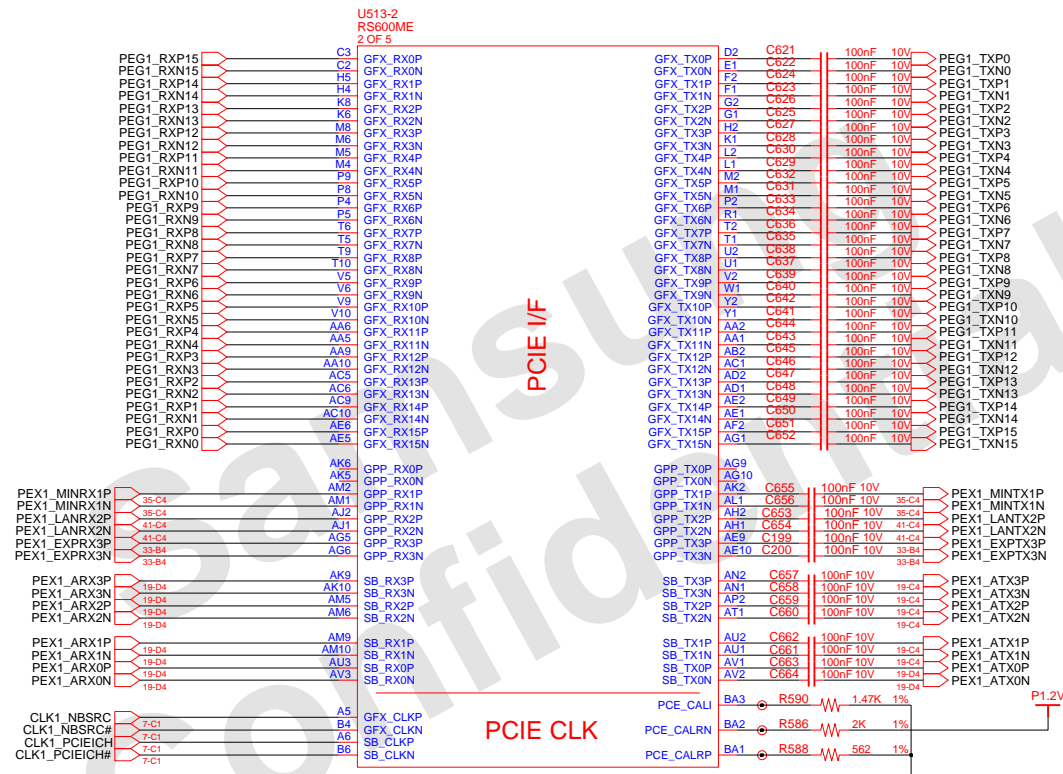
FAN Control



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	KK BIN	REV	1.0	THERMAL SENSOR/FAN CNTRL	BA41-00806A	
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	11 OF 54	



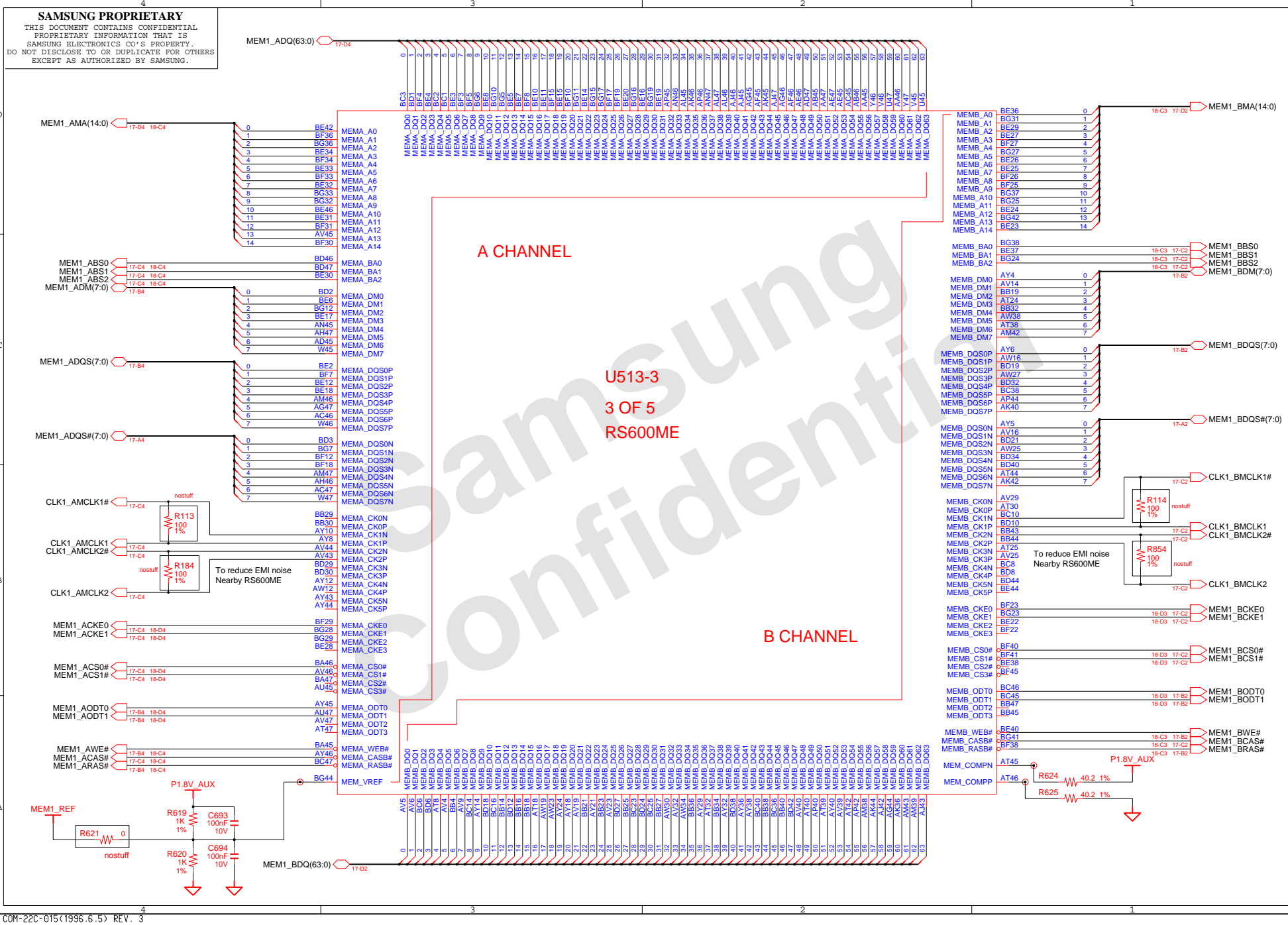
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CHECK	SS BAIK	DEV. STEP	PR	REV	RS600ME(1/5)	
APPROVAL	KK BIN	REV	1.0	LAST EDIT		
MODULE CODE						



PEX1_MIN Mini Card I/F
 PEX1_LAN LOM I/F
 PEX1_EXP Express Card I/F

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	REV	RS600ME(2/5)	
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-00806A
MODULE CODE		LAST EDIT				
				May 28, 2007 10:24:00 AM	PAGE 13	OF 54

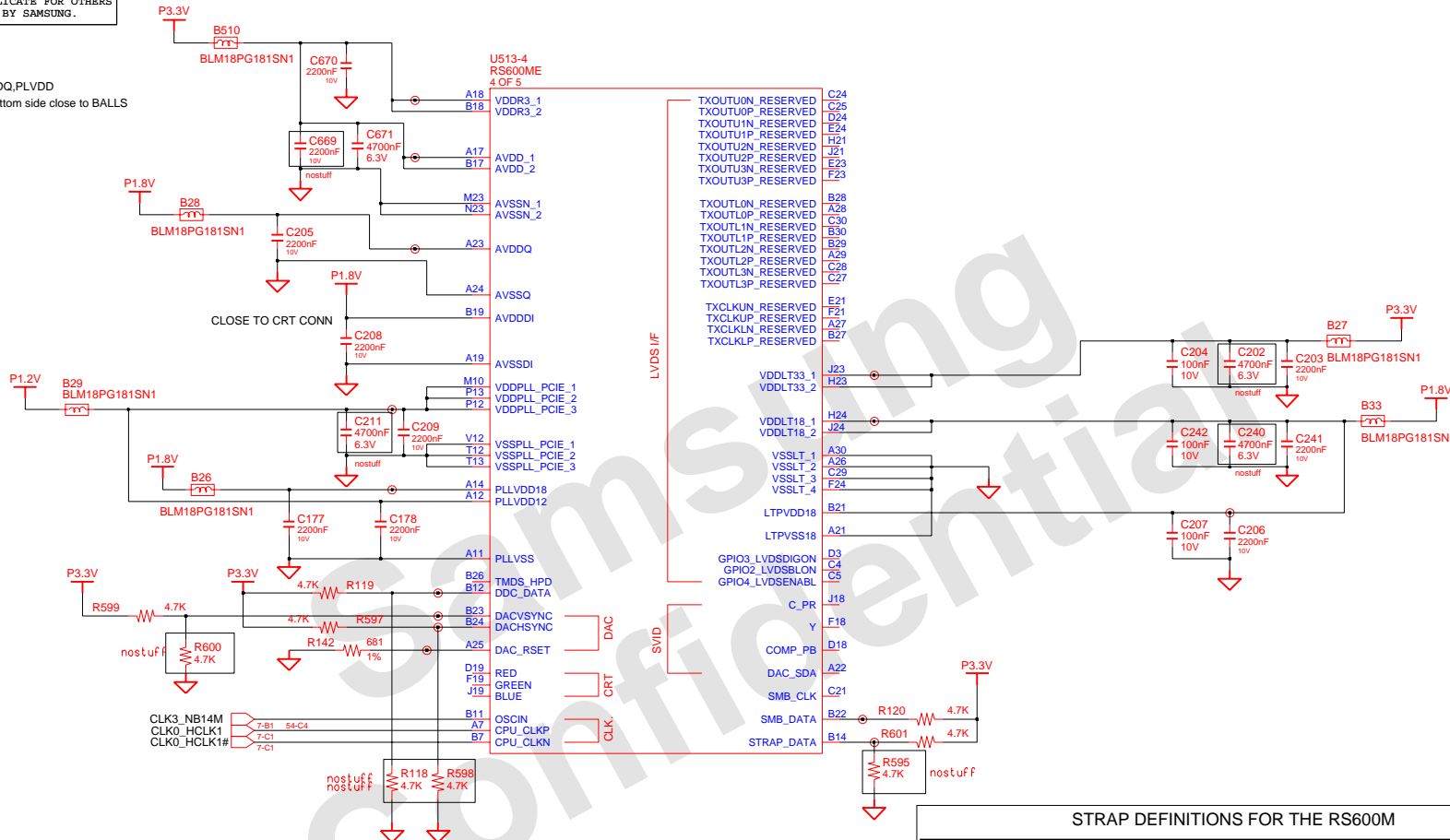
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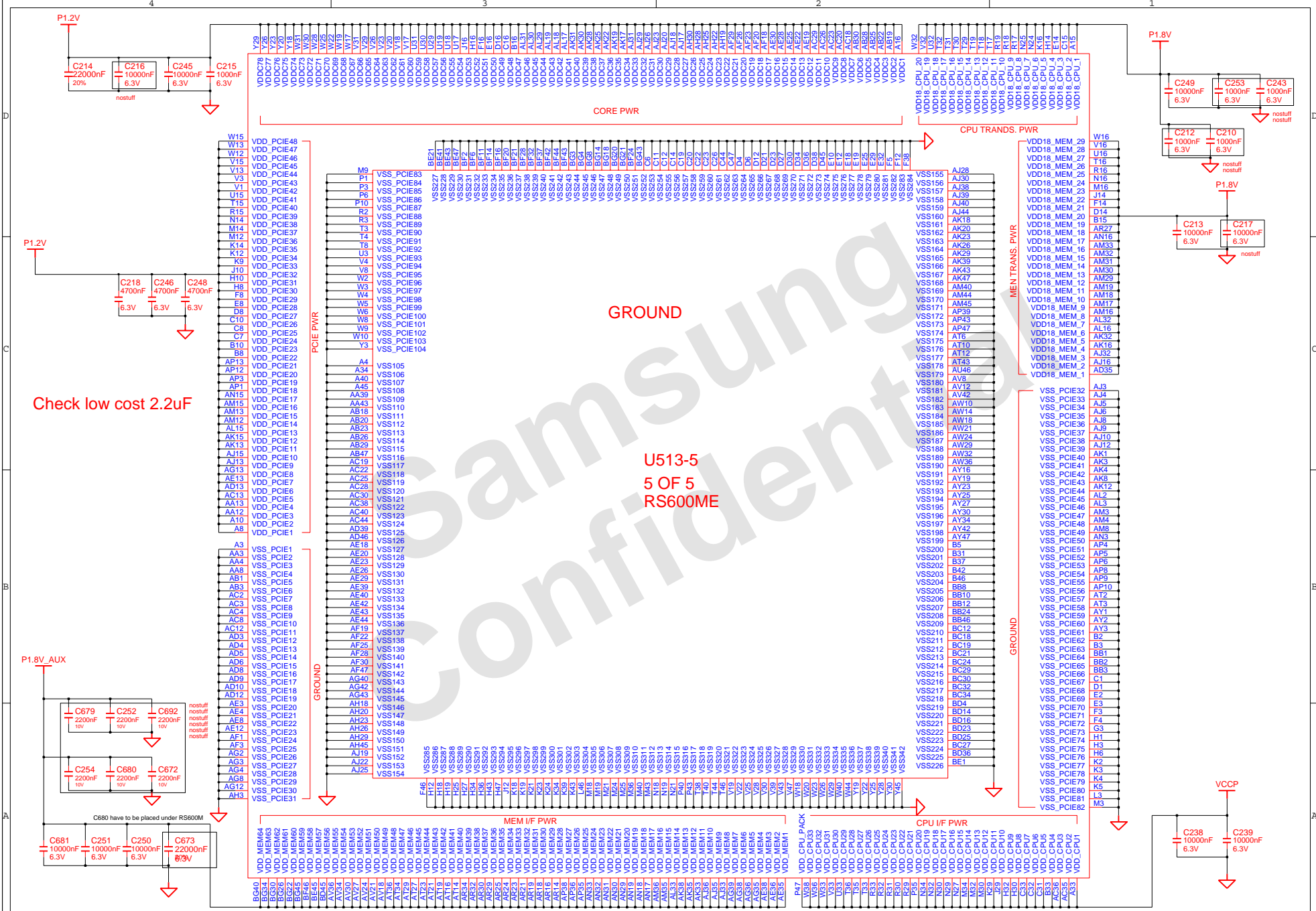
Put the AVDD, AVDDI, AVDDQ, PLVDD decoupling CAPS on the bottom side close to BALLS

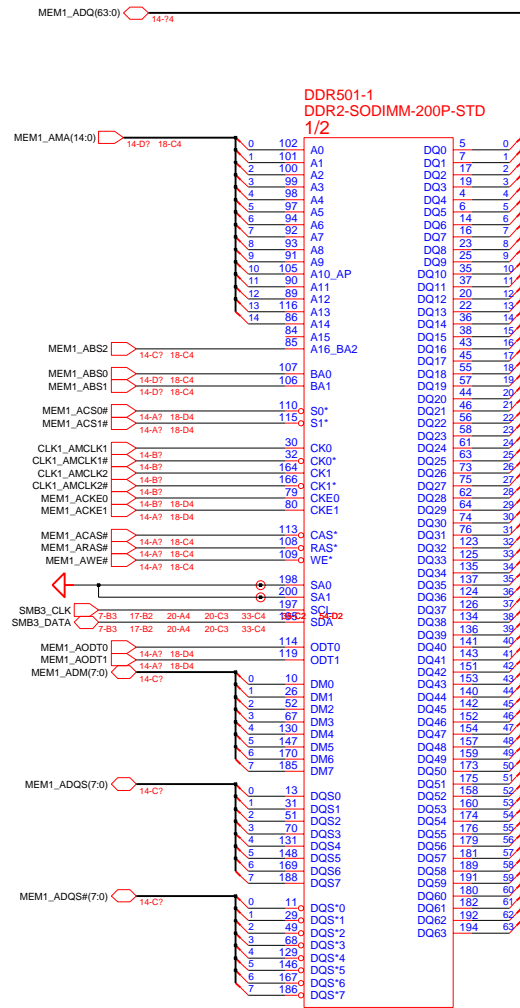


STRAP DEFINITIONS FOR THE RS600M

STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS600M
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

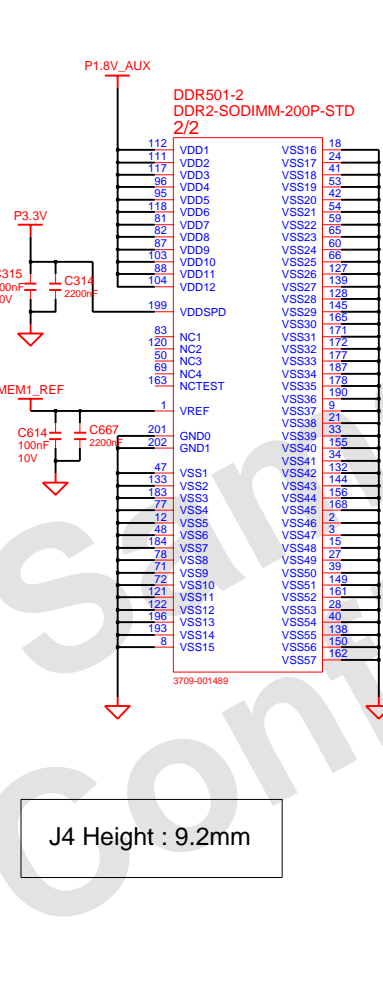
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CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		RS600ME<4/5>	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	15	OF 54





DDR501-1
DDR2-SODIMM-200P-STD
1/2

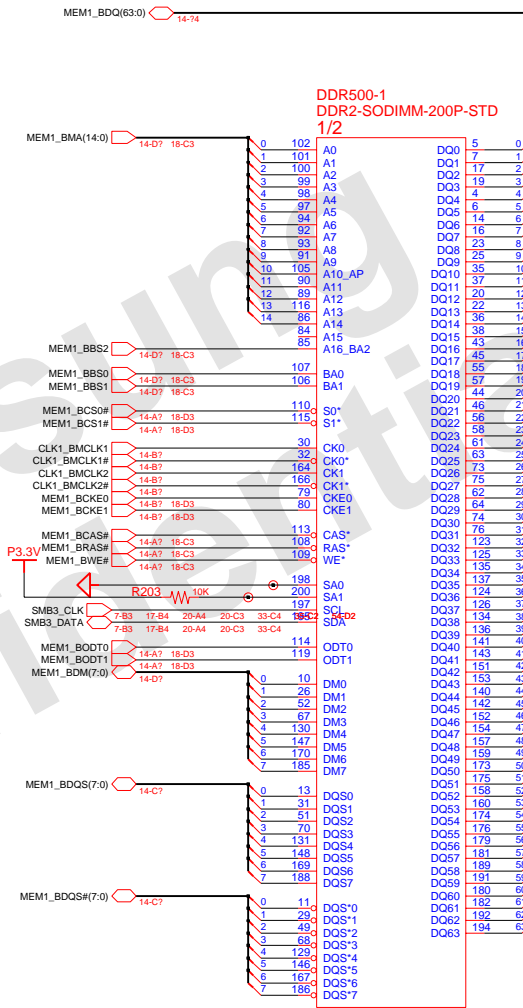
3709-001489



DDR501-2
DDR2-SODIMM-200P-STD
2/2

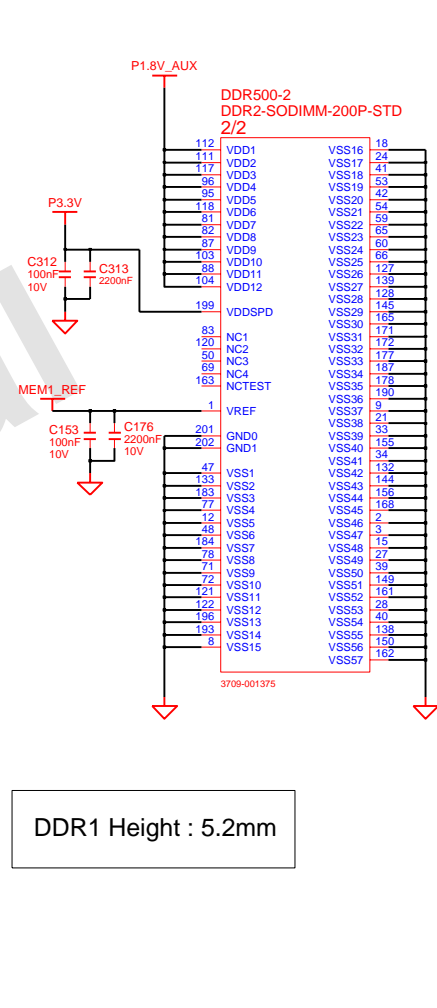
J4 Height : 9.2mm

3709-001489



DDR500-1
DDR2-SODIMM-200P-STD
1/2

3709-001375

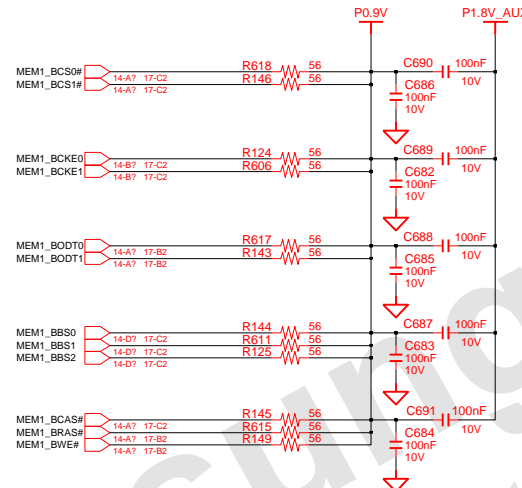
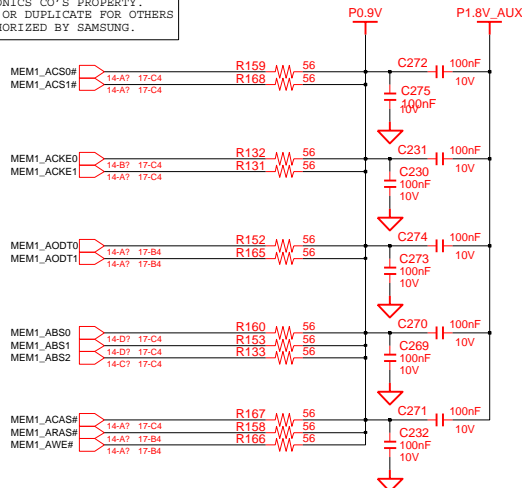


DDR500-2
DDR2-SODIMM-200P-STD
2/2

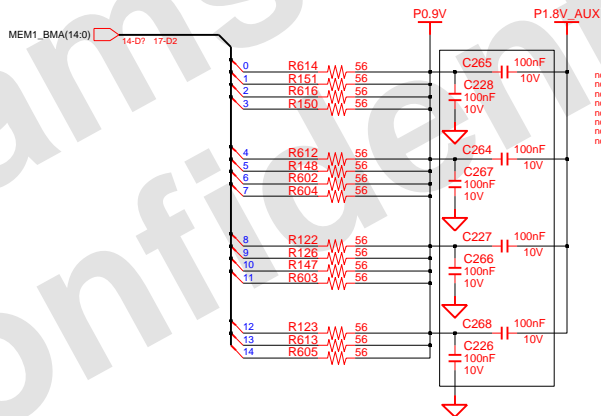
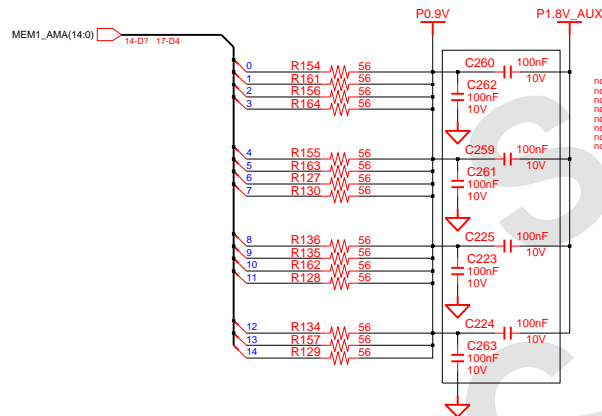
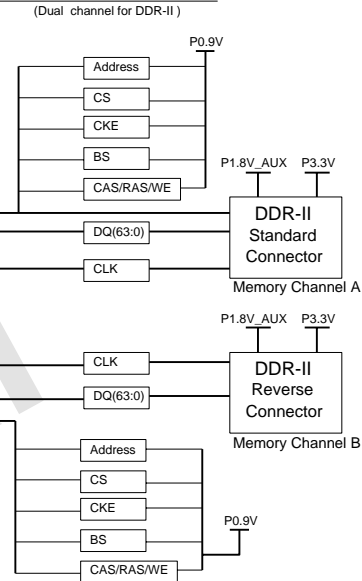
DDR1 Height : 5.2mm

3709-001375

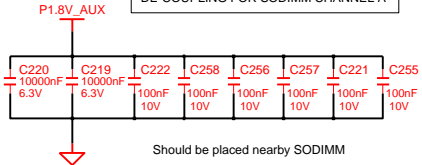
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CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	DDR2 - SODIMM		PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	17	OF 54



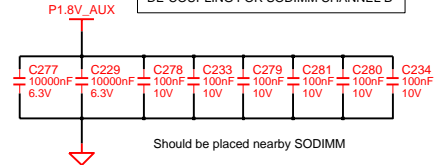
Memory Topology



DE-COUPLING FOR SODIMM CHANNEL A

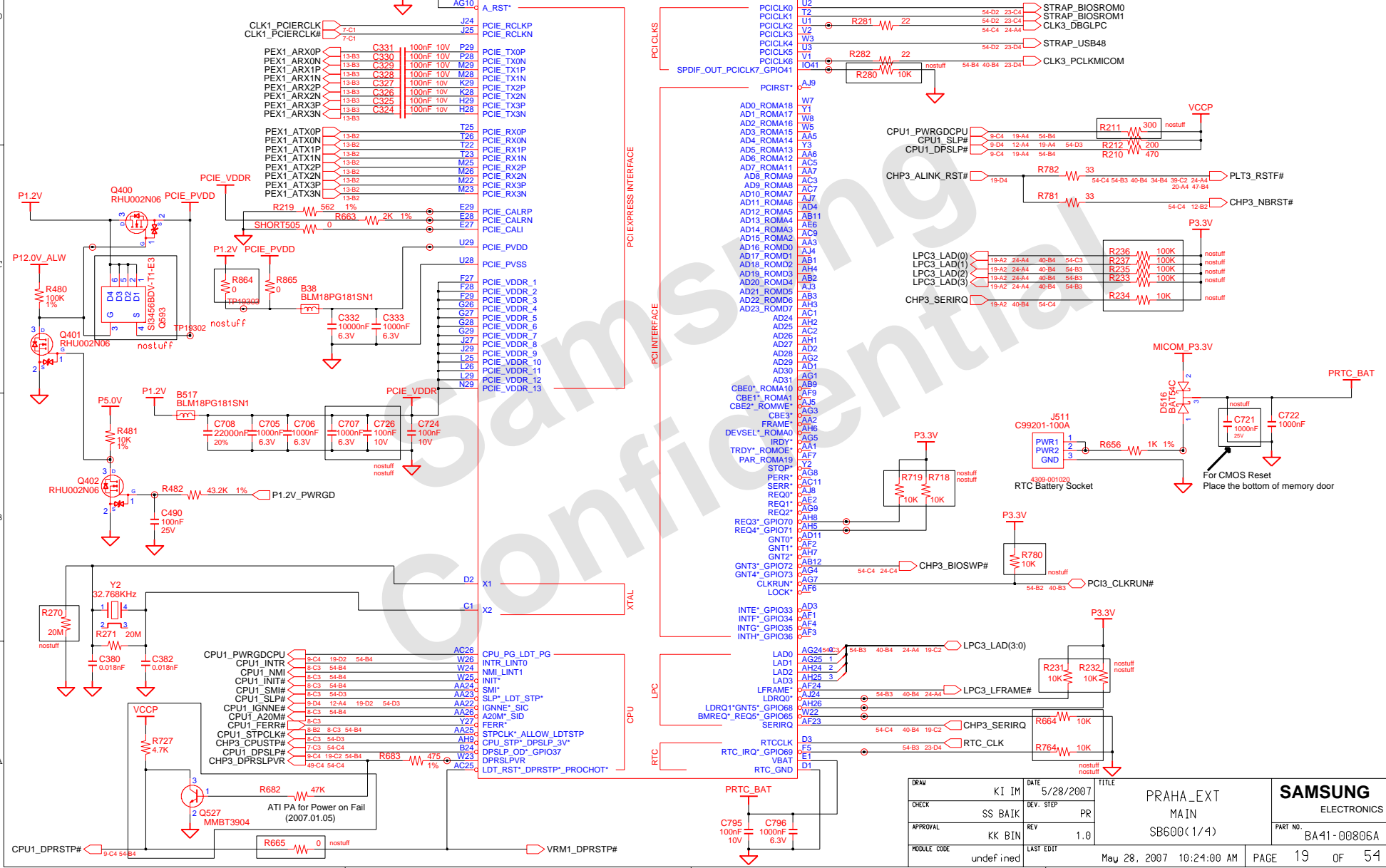


DE-COUPLING FOR SODIMM CHANNEL B



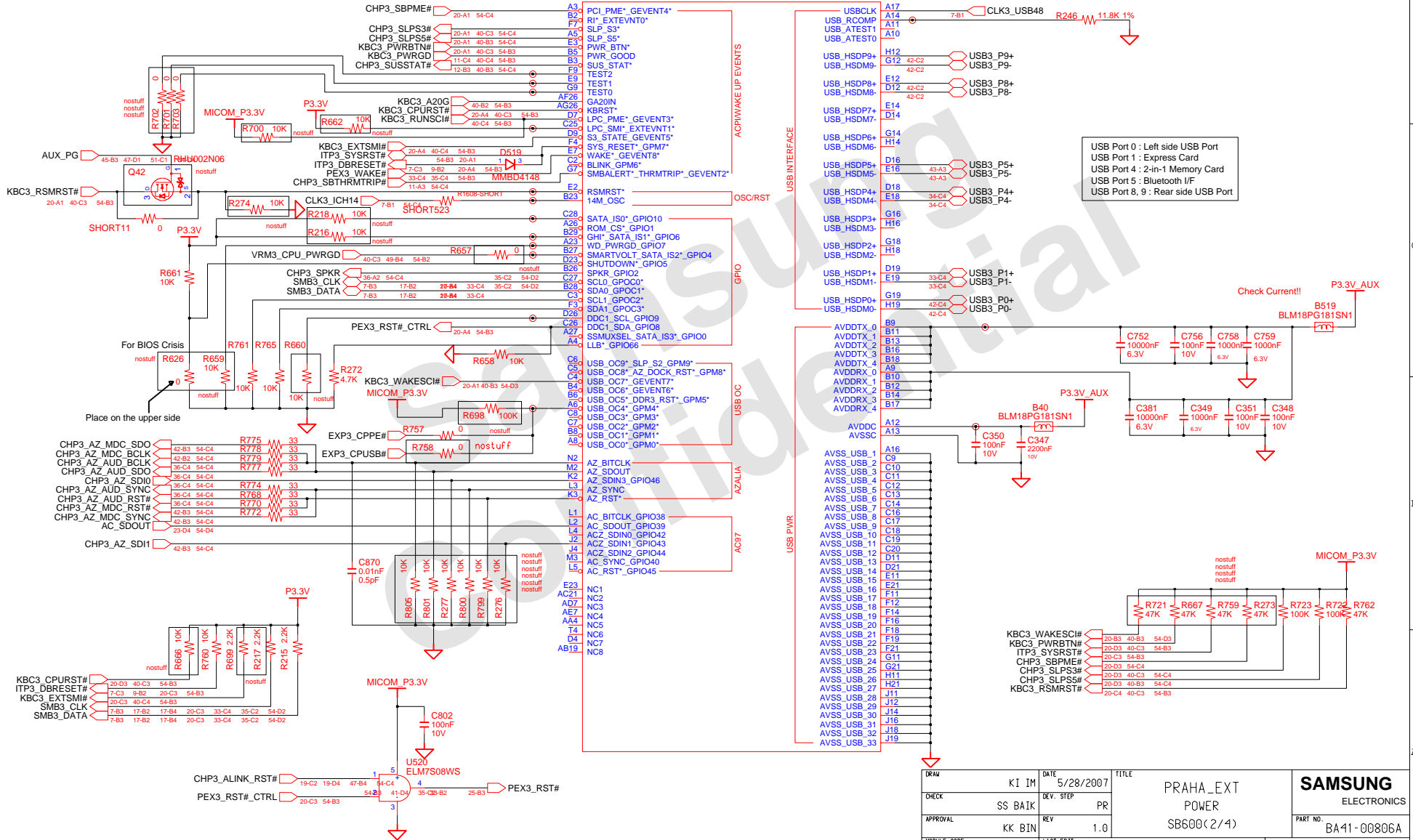
DRAW	KI IM	DATE	5/28/2007	FILE	PRAHA_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	DDR2 - TERMINATION		
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	18 OF 54	

CHP3_ALINK_RST# 19-C2 20-A4 47-B4 54-C4 R717 8.2K AG10 U11-1 218S6ECLA21FG 1/4



DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN	SB600(1/4)	
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	19 OF 54	

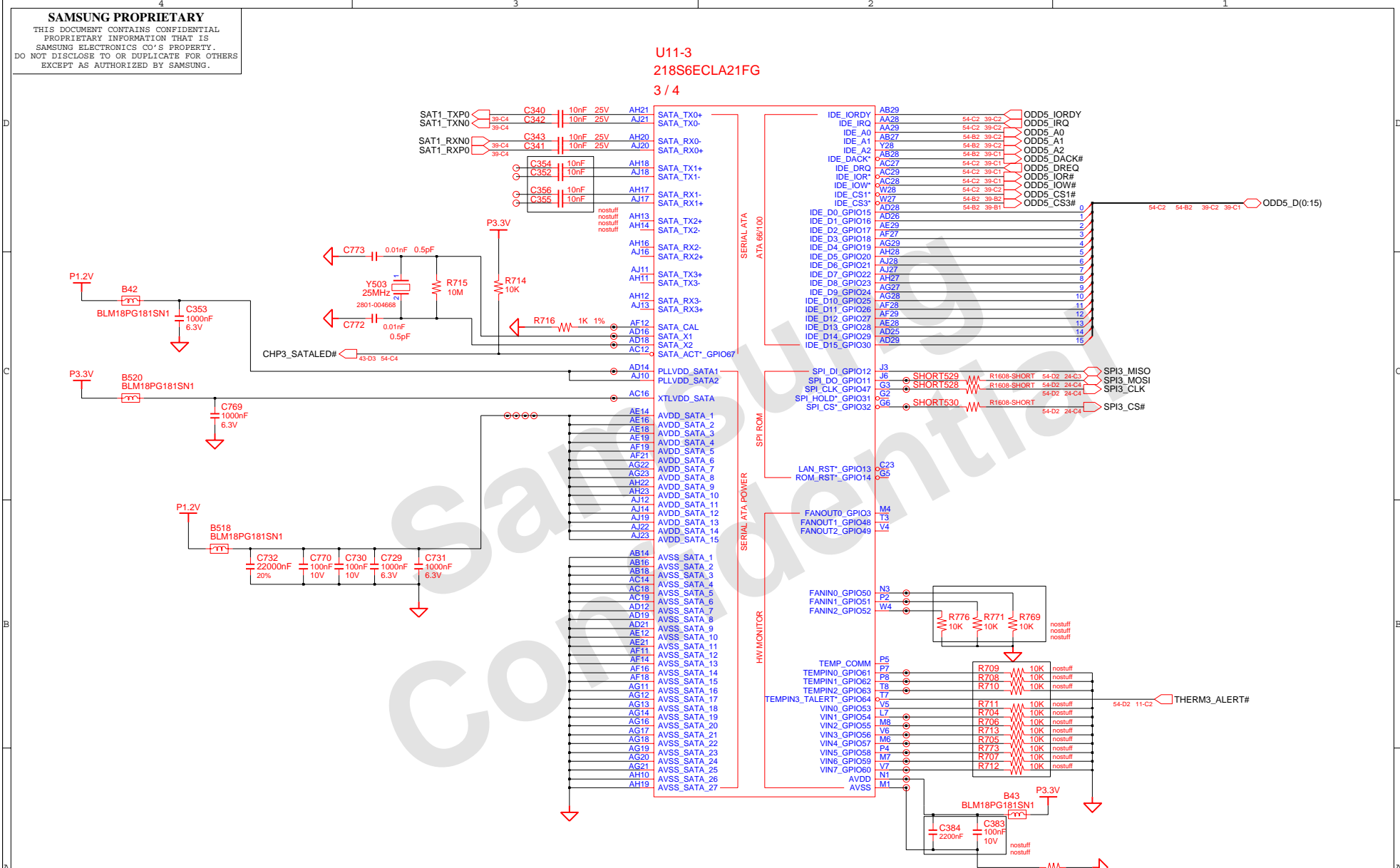
U11-2
218S6ECLA21FG
2 / 4



USB Port 0 : Left side USB Port
USB Port 1 : Express Card
USB Port 4 : 2-in-1 Memory Card
USB Port 5 : Bluetooth HIF
USB Port 8, 9 : Rear side USB Port

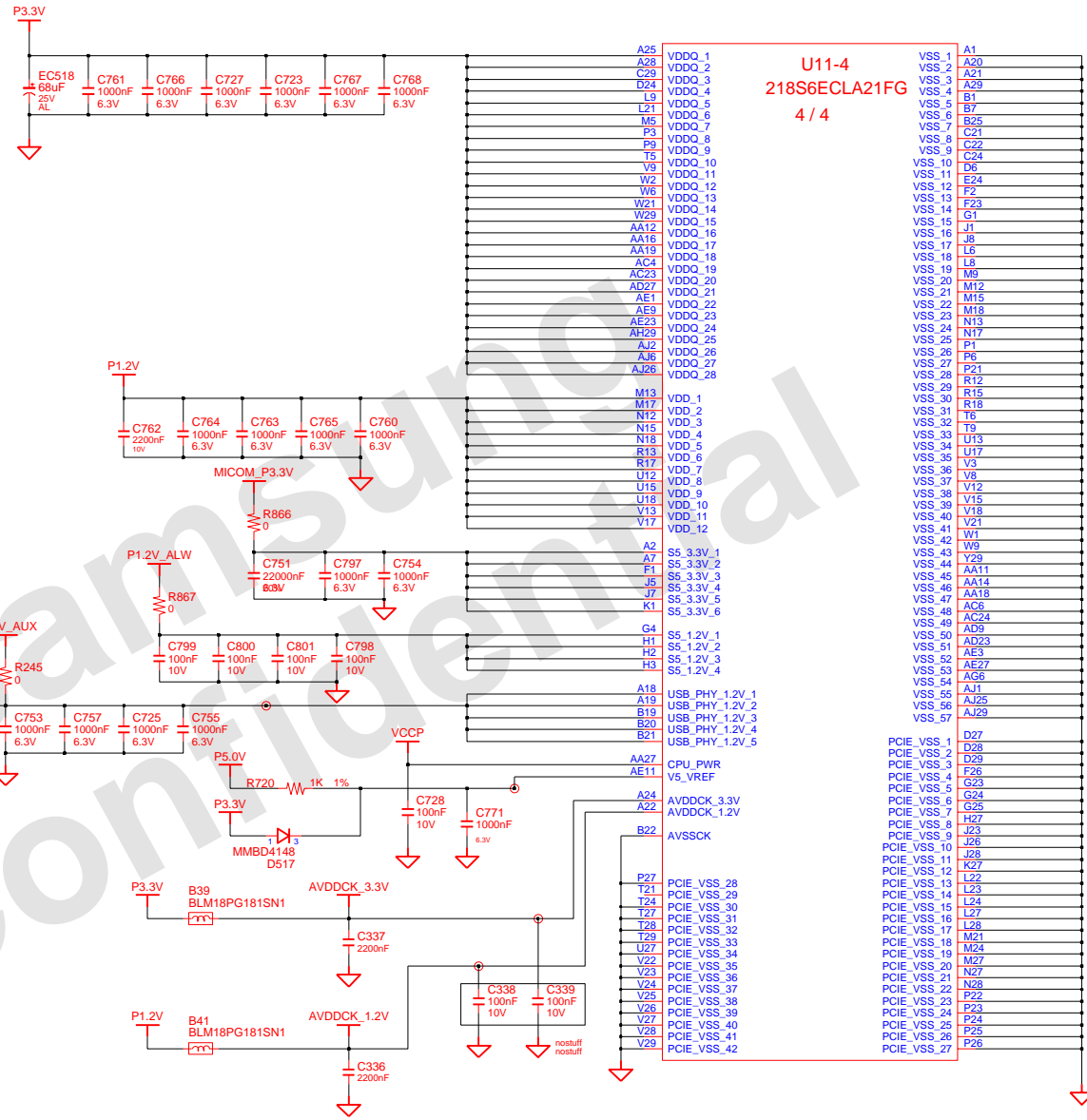
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CHECK	SS BAIK	DEV. STEP	PR		SB600(2/4)	
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT		May 28, 2007 10:24:00 AM	PAGE 20 OF 54	

U11-3
218S6ECLA21FG
3 / 4



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	SB600(3/4)		PART NO.
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	21	OF 54

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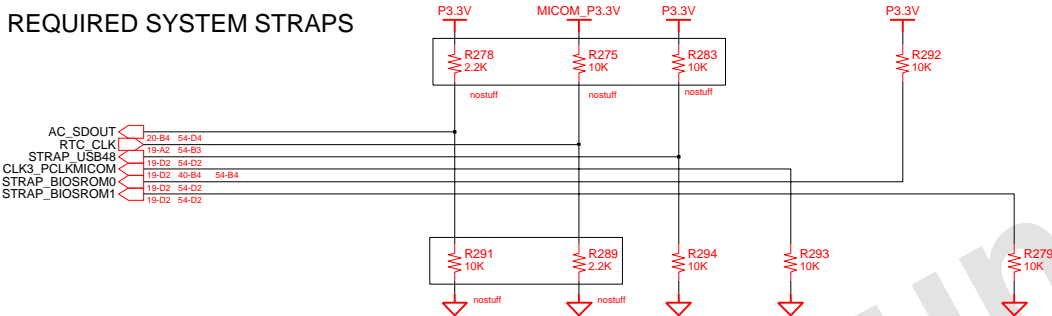


U11-4
 218S6ECLA21FG
 4 / 4

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CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		SB600(4/4)	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	22	OF 54

SB600 HAS AN INTERNAL PD FOR AC_SDOUT
 SB600 HAS AN INTERNAL PU FOR RTC_CLK

REQUIRED SYSTEM STRAPS



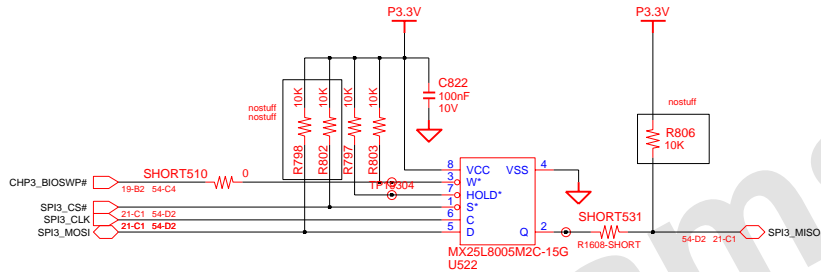
	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0	PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM	
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS

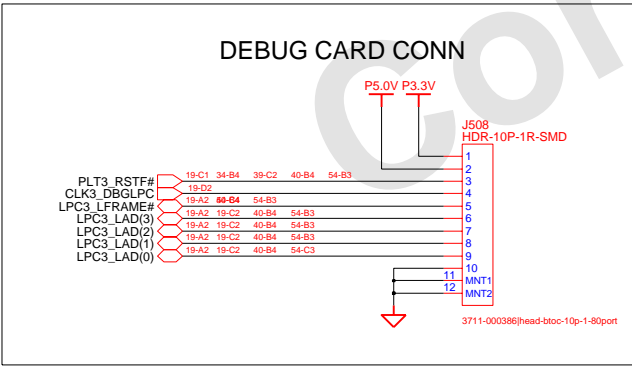
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

DRAW	KI IM	DATE	5/28/2007	FILE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0		STRAPS	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM		PAGE	23 OF 54

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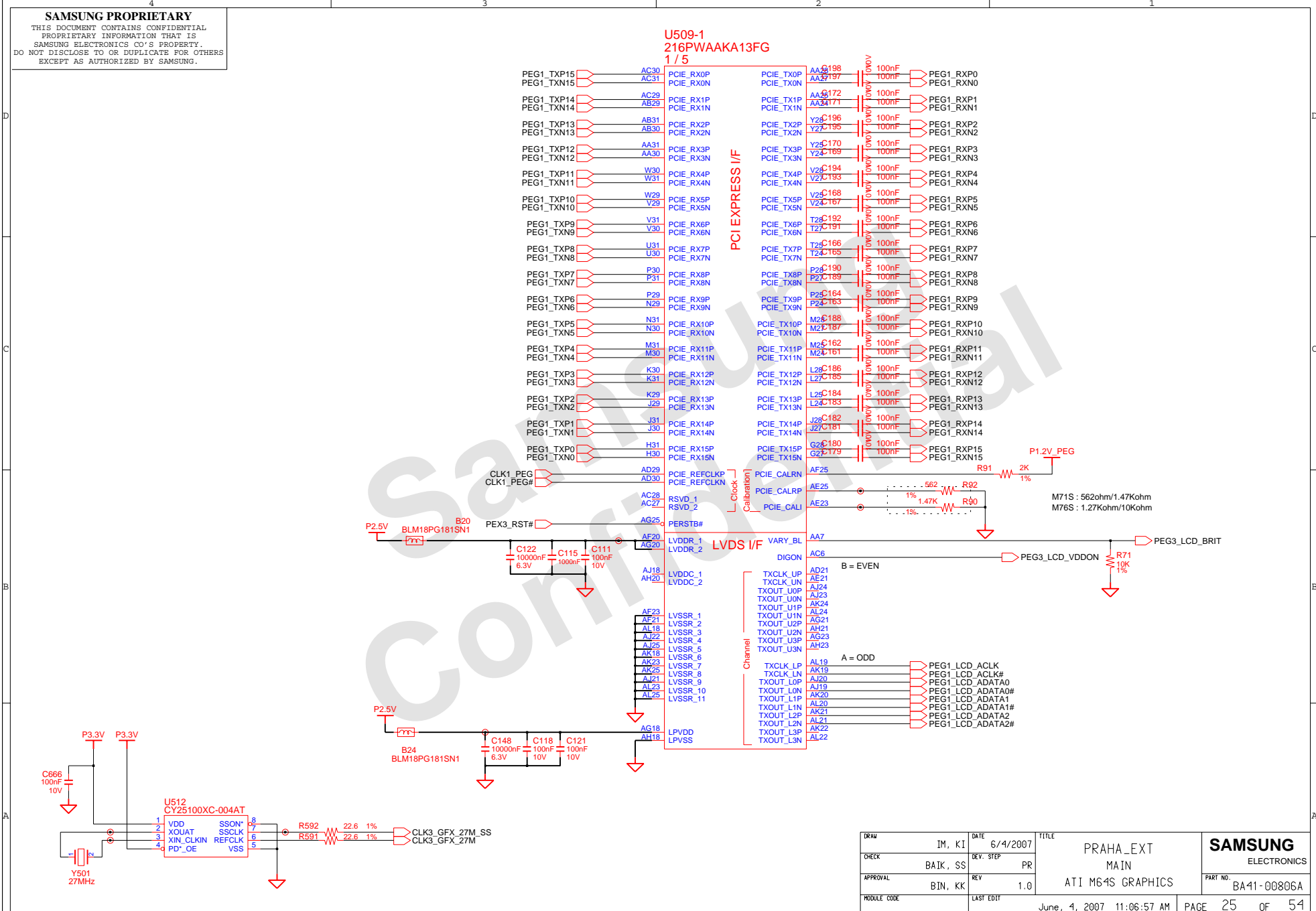
SPI3_CS#
 SB600 prior to A21 : Pulled up to P3.3V_ALW with 1Kohm resistor.
 SB600 A21 and newer : No external pull-up resistor required.



- | | |
|---------------------------------------|------------------------------------|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU.REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD EERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE | 7E TEST COPROCESSER IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET | 86 RE-INIT. ON-BOARD I/O PORT |
| WITH INITIAL POST VALUE | 88 INIT. BIOS DATA ROM |
| 14 INIT. KEYBOARD CONTROLLER | 8A INIT.EXTENDED BIOS DATA AREA |
| 16 CHECK CHECKSUM | 8C INIT. FDD CONTROLLER |
| 18 8254 TIMER INIT. | 9A SHADOW OPTION ROMS |
| 1A 8237 DMA CONTROLLER INIT. | 9C SETUP POWER MANAGER |
| 1C RESET INTERRUPT CONTROLLER | 9E ENABLE H/W INTERRUPT |
| 20 TEST DRAM REFRESH | A0 SET TIME OF DAY |
| 22 TEST 8742 KEYBOARD CONTROLLER | A4 INIT. TYPEMATIC RATE |
| 24 SET ES SEGMENT REG. TO 4GB | A8 ERASE F2 PROMPT |
| 26 ENABLE A20 | AA SCAN FOR F2 KEY STROKE |
| 28 AUTO SIZING DRAM | AC ENTER SETUP |
| 32 COMPUTE THE CPU SPEED | AE CLEAR IN POST FLAG |
| 34 TESET CMOS RAM | B0 CHECK FOR ERRORS |
| 38 SHADOW SYSTEM BIOS ROM | B2 POST DONE-PREPARE TO BOOT O/S |
| 3A AUTO SIZING CACHE | B4 ONE BEEP |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B6 CHECK PASSWORD (OPTION) |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B7 ACPI INIT |
| 42 INIT. INTERRUPT VECTOR | BA DMI INIT |
| 44 INIT. BIOS INTERRUPT | BE CLEAR SCREEN |
| 46 CHECK ROM COPYRIGHT NOTICE | C0 TRY BOOT WITH INT19 |
| 47 INIT. i20 SUPPORT IF INSTALLED | D0 INTERRUPT HANDLER ERROR |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D2 UNKNOWN INTERRUPT ERROR |
| 49 INIT. PCI BUS AND DEVICE | D4 PENDING INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 4C SHADOW VIDEO BIOS ROM | D8 SHUTDOWN ERROR |
| 50 DISPLAY CPU TYPE AND SPEED | DA EXTENDED BLOCK MOVE |
| 52 TEST KEYBOARD | DC SHUTDOWN 10 |
| 54 SET KEYCLICK IF ENABLED | 89 ENABLE NMI |
| 56 ENABLE KEYBOARD | 90 INIT. HDD CONTROLLER |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5A DISPLAY " PRESS SETUP" | 92 JUMP TO USER PATCH 2 |
| 5C TEST RAM BETWEEN 512K AND 640K | 94 DISABLE A20 ADDRESS LINE |
| 60 TEST EXTENDED MEMORY | 96 CLEAR HUGE ES SEGMENT REG. |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 98 SEARCH FOR OPTION ROMS |
| 64 JUMP TO USER PATCH 1 | |

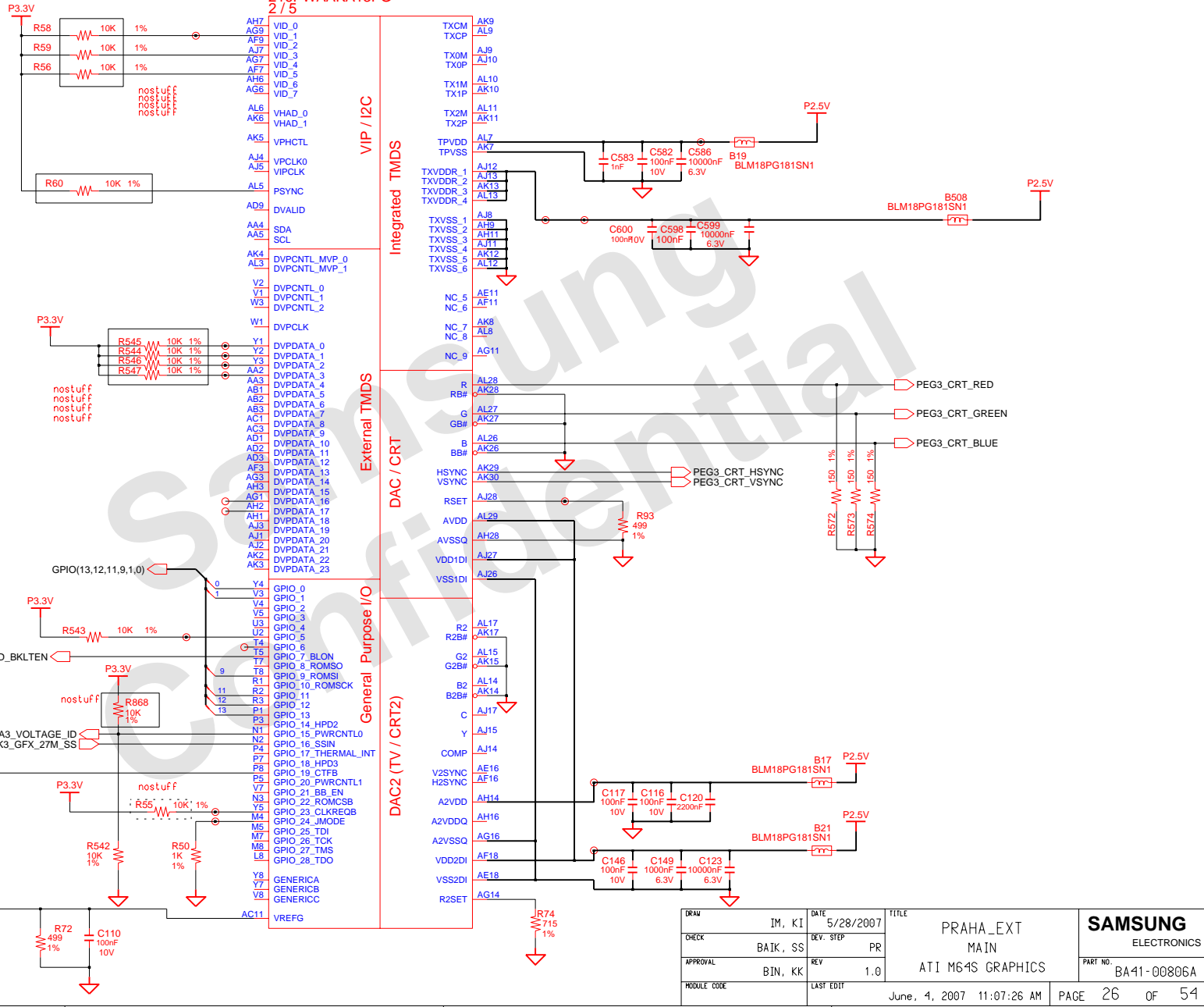
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CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0	SPI ROM & DEBUG PORT		PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	24	OF 54

U509-1
216PWAACA13FG
1 / 5



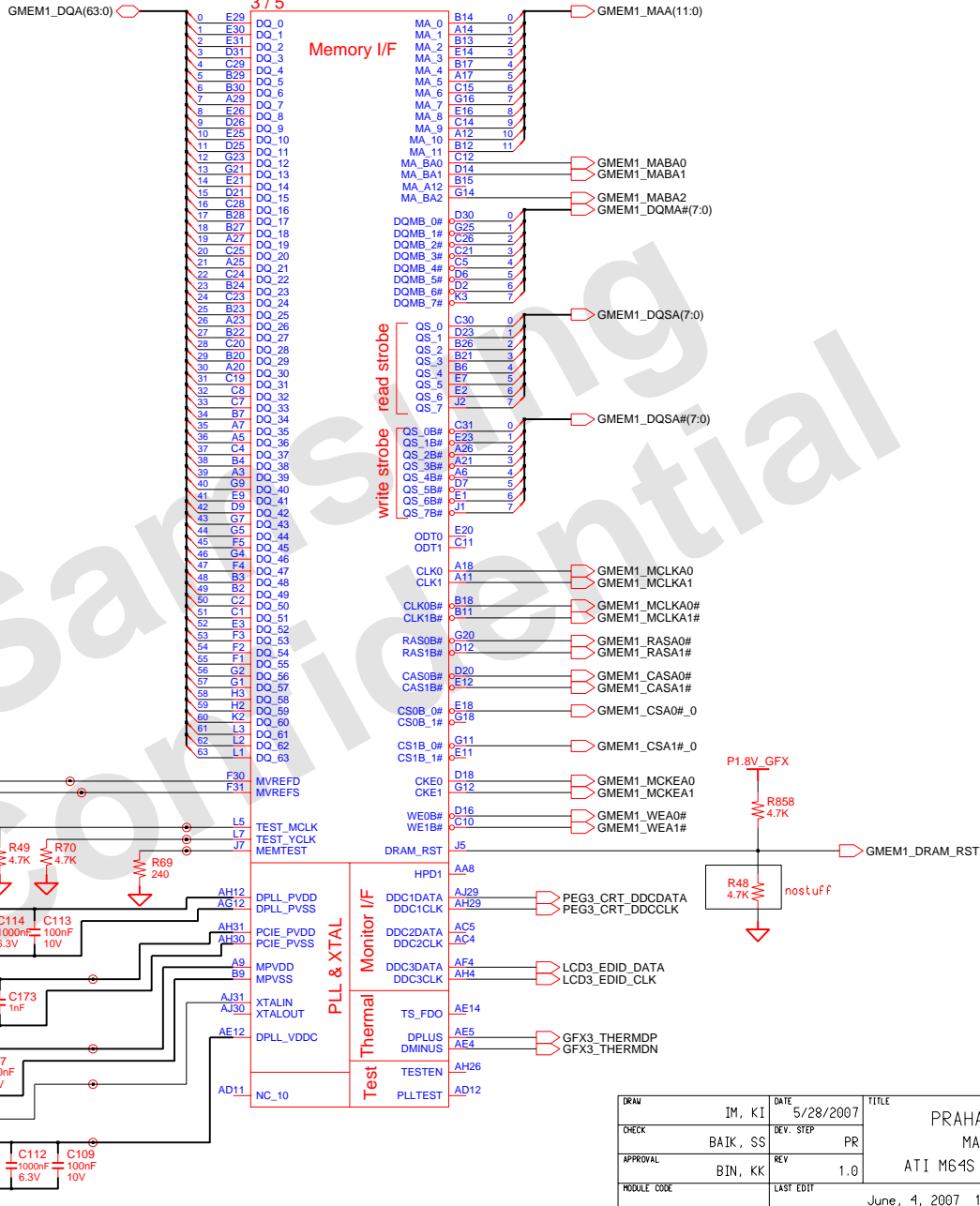
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CHECK	BAIK, SS	DEV. STEP	PR	MAIN		
APPROVAL	BIN, KK	REV	1.0	ATI M64S GRAPHICS		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		June, 4, 2007	11:06:57 AM	PAGE 25 OF 54

**U509-2
 216PWAAKA13FG
 2 / 5**

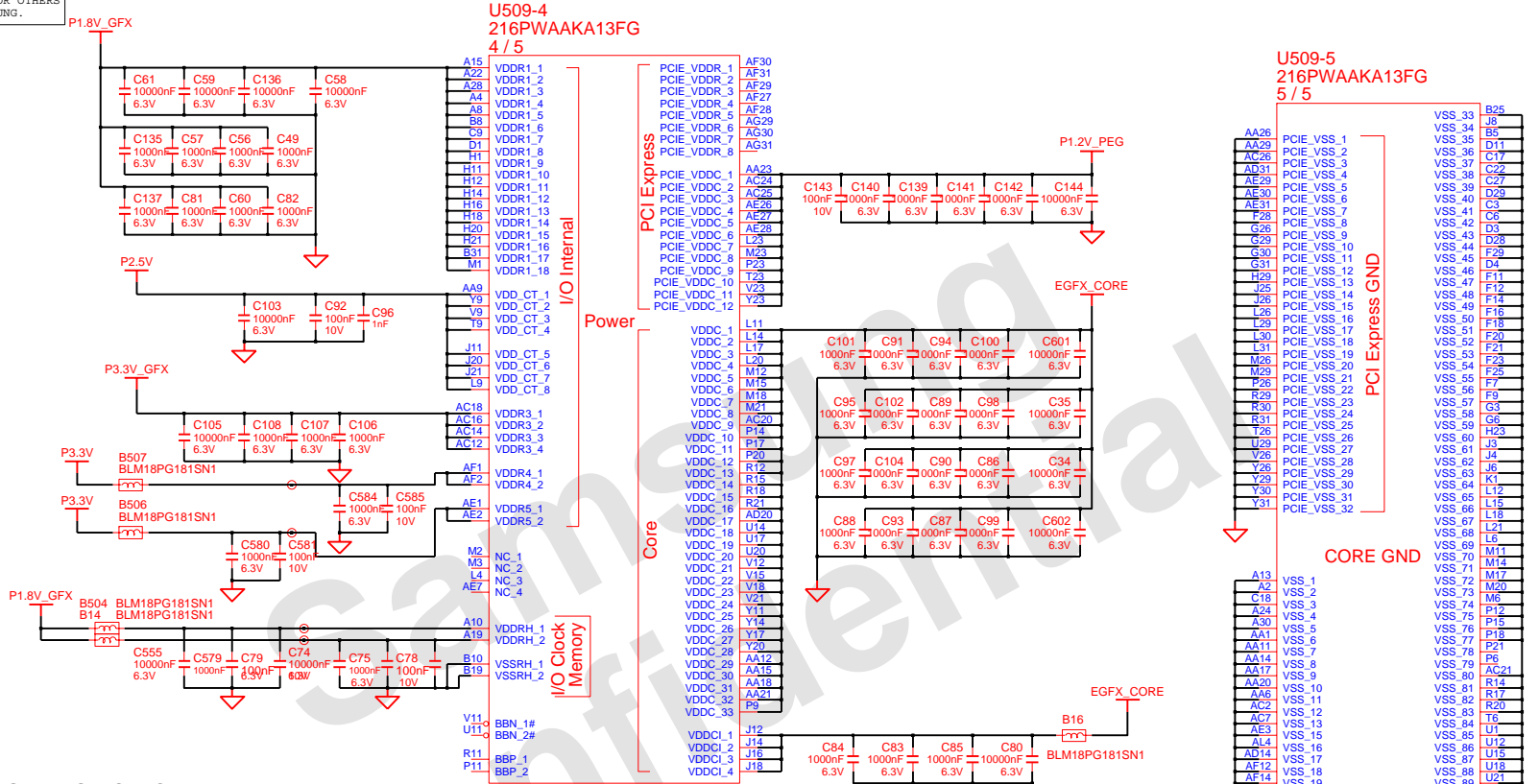


DRAW	IM, KI	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	PR	MAIN		
APPROVAL	BIN, KK	REV	1.0	ATI M64S GRAPHICS		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		June, 4, 2007 11:07:26 AM		PAGE 26 OF 54

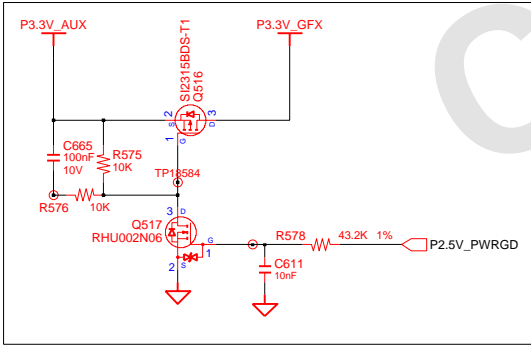
U509-3 216PWAAKA13FG 3 / 5



DRAW	IM, KI	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	BAIK, SS	DEV. STEP	PR		MAIN	
APPROVAL	BIN, KK	REV	1.0		ATI M64S GRAPHICS	
MODULE CODE		LAST EDIT				
				June, 4, 2007 11:08:03 AM	PAGE	27 OF 54

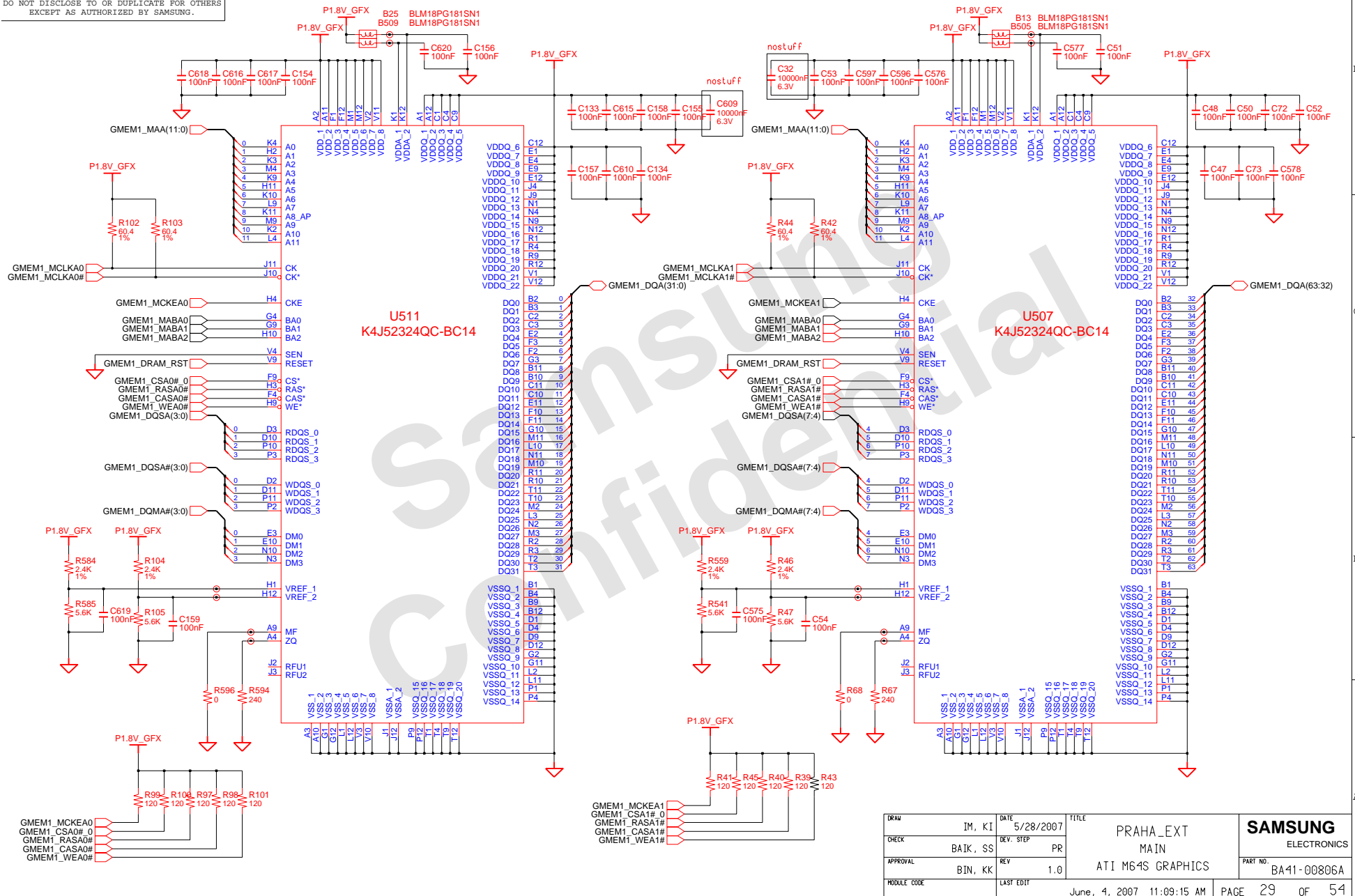


P3.3V_GFX CONTROL CIRCUIT



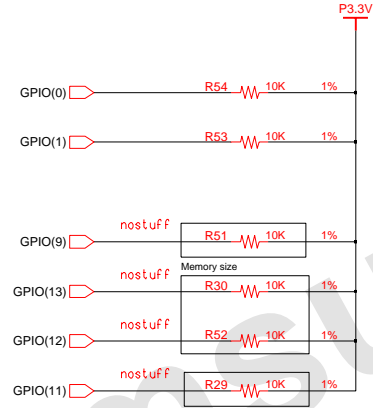
DRAW	IM, KI	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	PR	MAIN		
APPROVAL	BIN, KK	REV	1.0	ATI M64S GRAPHICS		PART NO. BA41-00806A
MODULE CODE		LAST EDIT		June, 4, 2007 11:08:39 AM	PAGE	28 OF 54

A-channel



DRAW	IM, KI	DATE	5/28/2007	TITLE	PRaha_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00806A	
CHECK	BAIK, SS	DEV. STEP	PR	MAIN			
APPROVAL	BIN, KK	REV	1.0	ATI M64S GRAPHICS			
MODULE CODE		LAST EDIT		June, 4, 2007 11:09:15 AM			
						PAGE	29 OF 54

Need to option



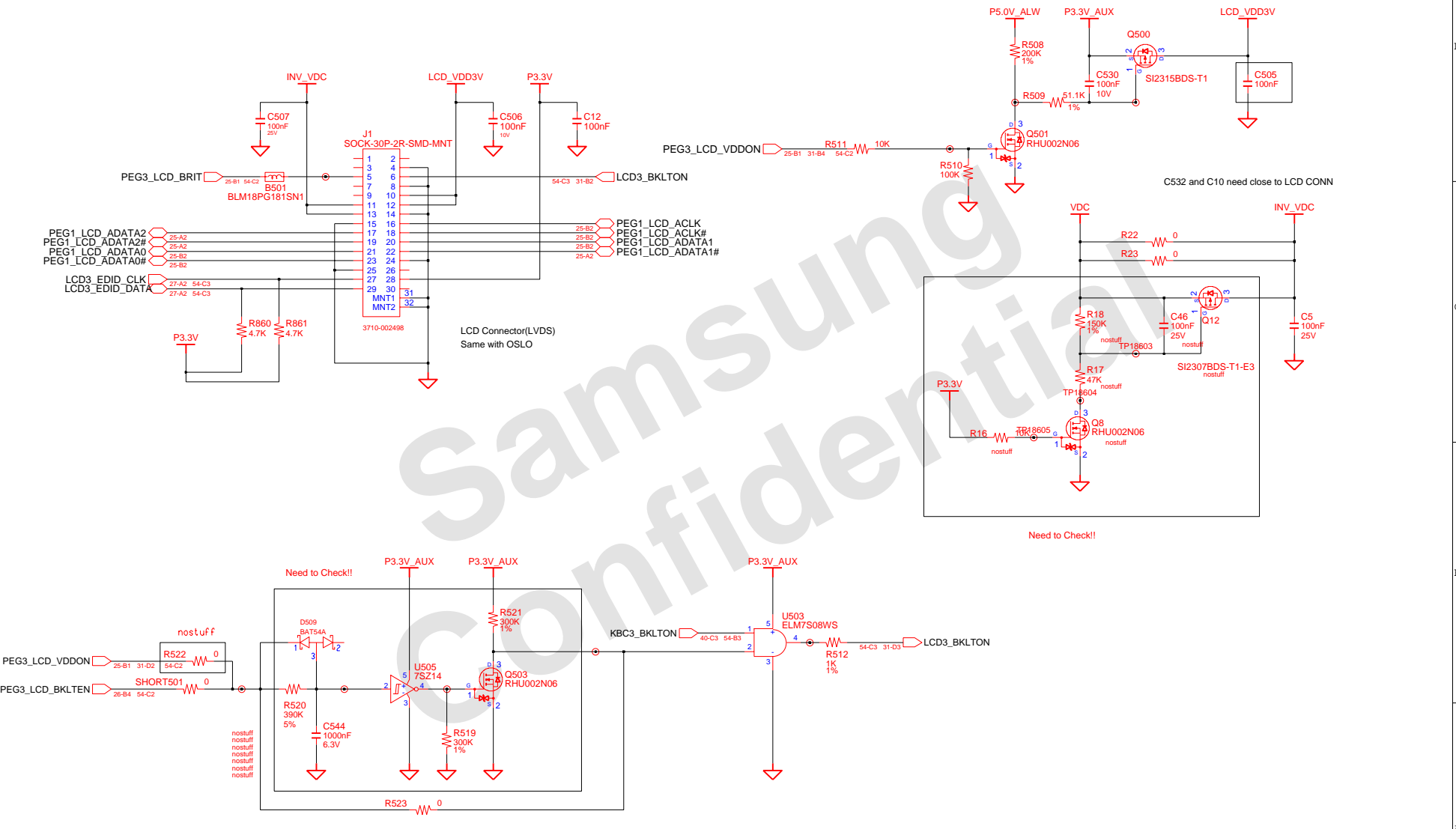
(DEFAULT : pull-down)

STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.
ROMIDCFQ[3:0]	GPIO[9,13:11]	When no ROM is attached, GPIO[9] is set to 0. GPIO[13:12] is used to select the frame buffer aperture size. GPIO[13:12] = 00: 128M frame buffer GPIO[13:12] = 01: 256M frame buffer GPIO[13:12] = 10: 64M frame buffer GPIO[13:12] = 11: reserved

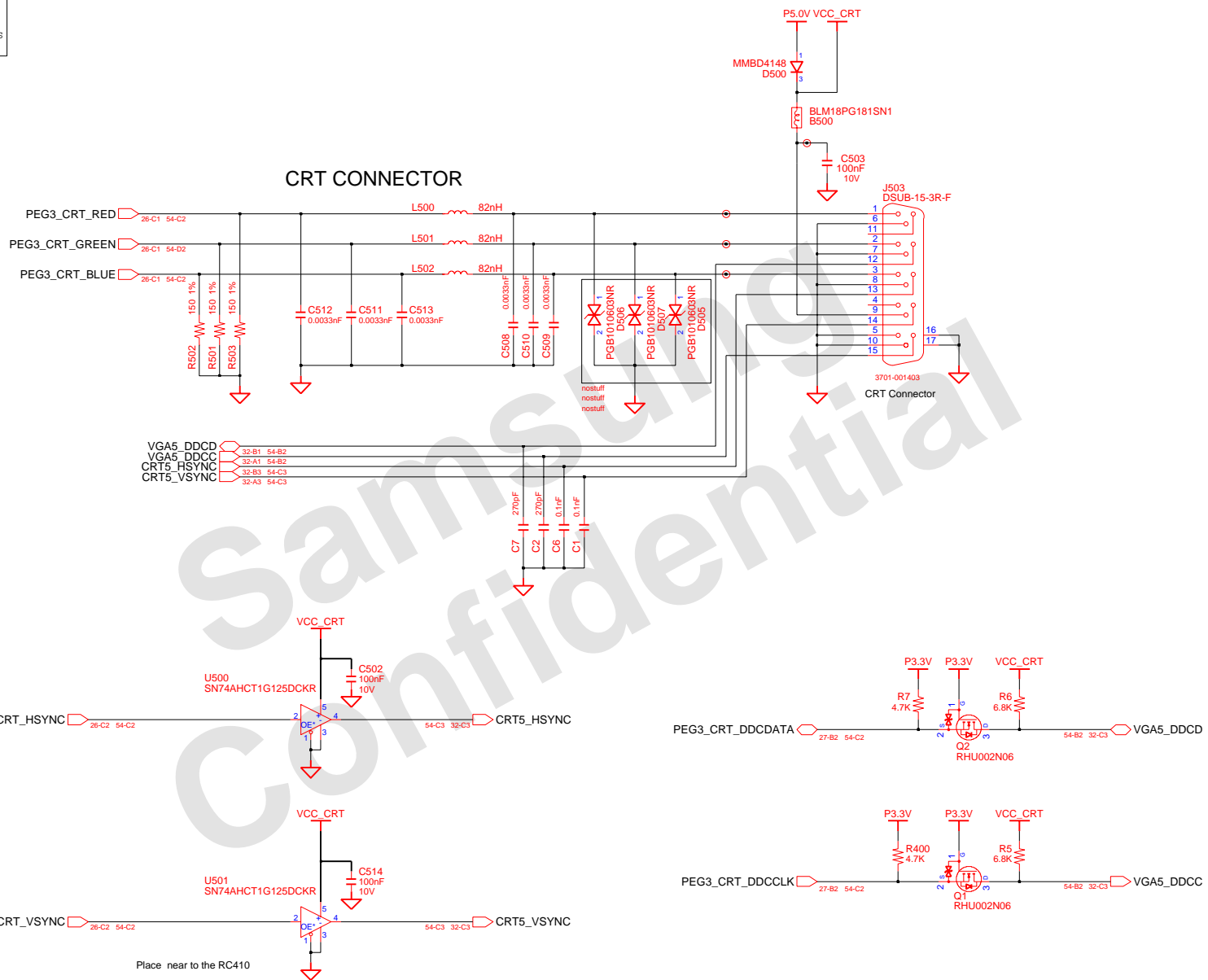
DRAW	IM, KI	DATE	5/28/2007	FILE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	PR		MAIN	
APPROVAL	BIN, KK	REV	1.0		ATI M64S GRAPHICS	PART NO. BA41-00806A
MODULE CODE		LAST EDIT	June, 4, 2007 11:09:49 AM	PAGE	30	OF 54

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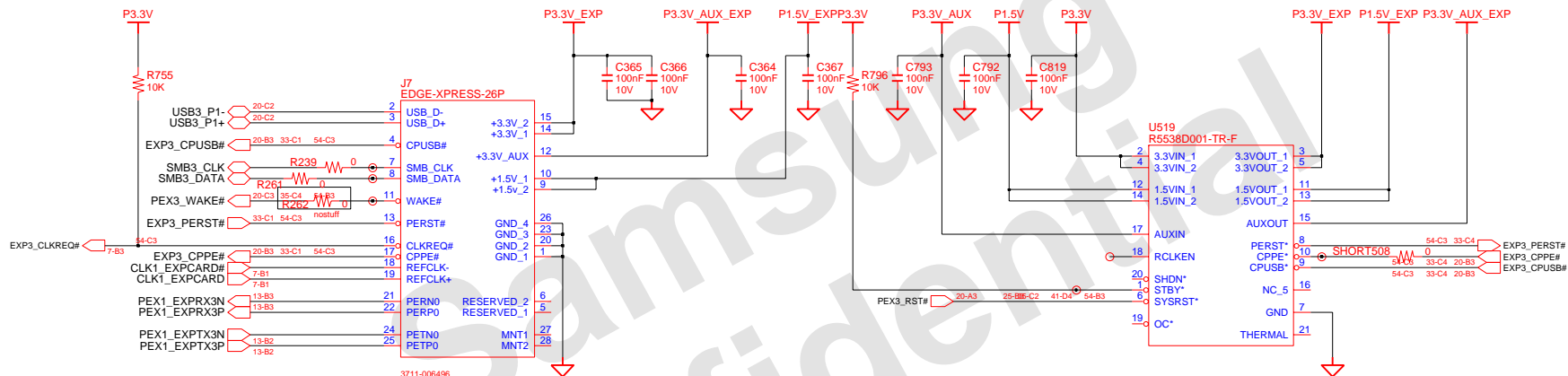
DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	LCD Connector & SPREAD SPECTRUM		
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	31	OF 54



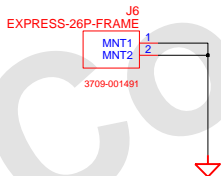
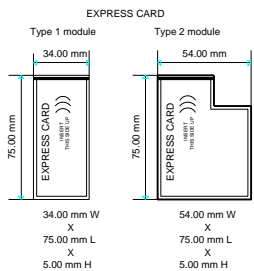
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0		CRT	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	32	OF 54

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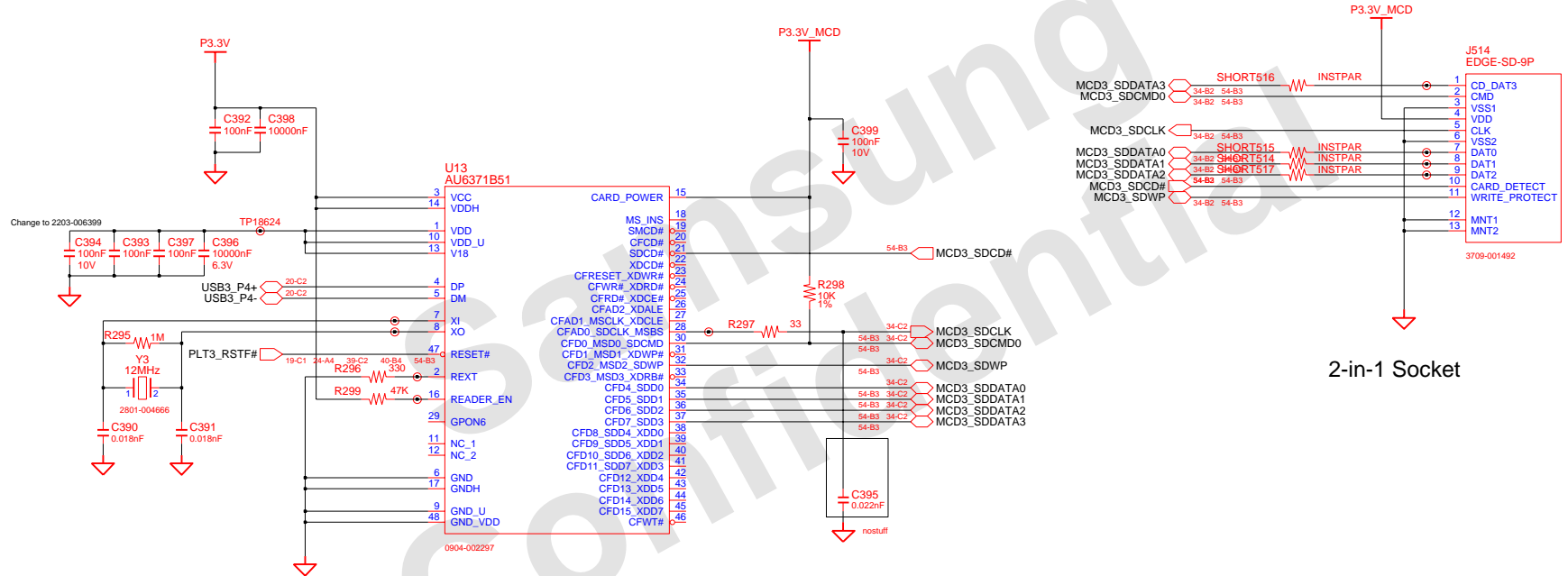


3711-006496



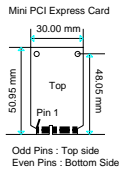
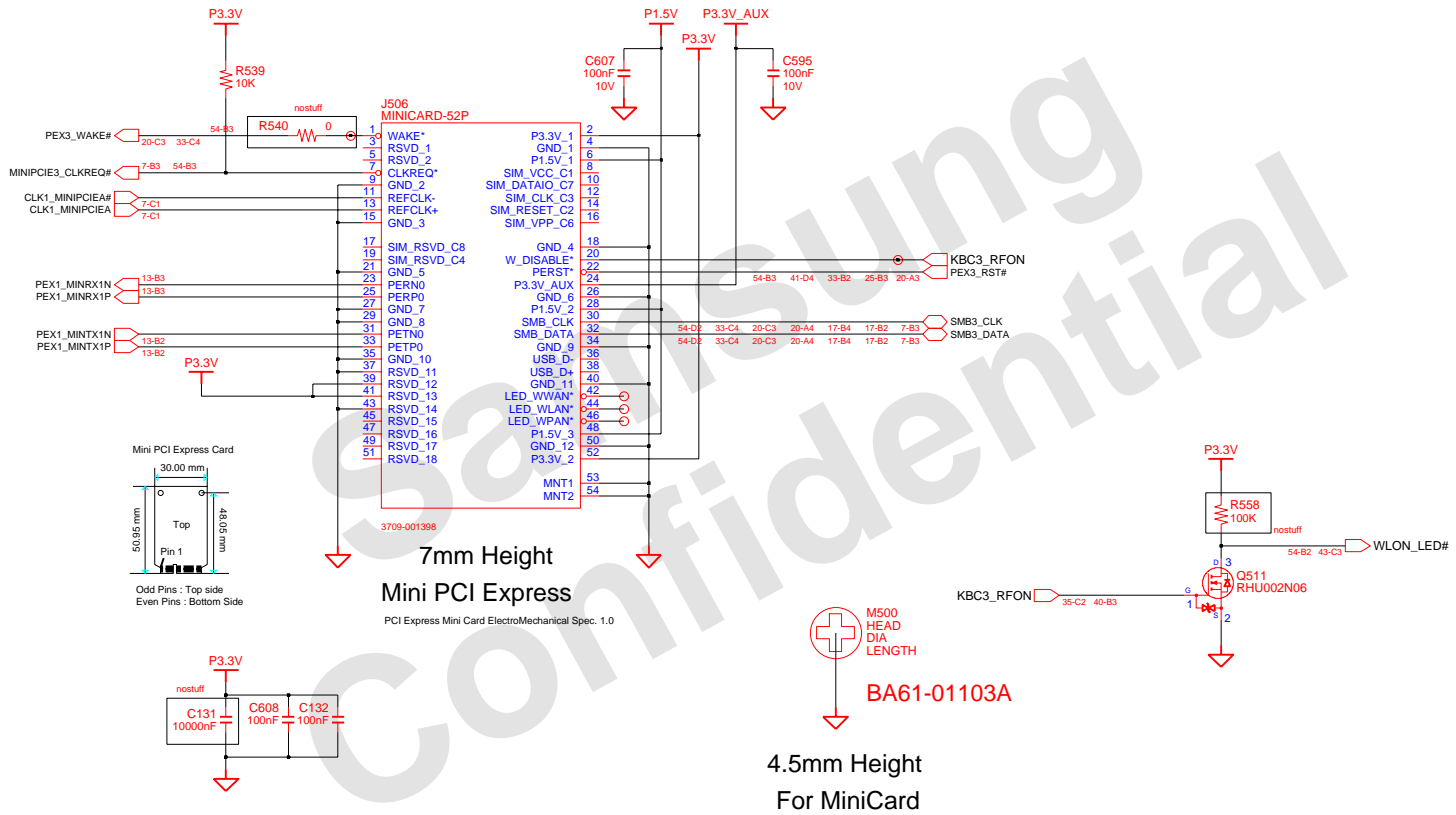
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CHECK	SS BAIK	DEV. STEP	PR	EXPRESS CARD	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-00806A	
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	33	OF 54

2 IN 1 CARD



2-in-1 Socket

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	2 in 1 Socket		
APPROVAL	KK BIN	REV	1.0			PART NO. BA41-00806A
MODULE CODE	LAST EDIT		May 28, 2007 10:24:00 AM	PAGE	34	OF 54



7mm Height
 Mini PCI Express
 PCI Express Mini Card ElectroMechanical Spec. 1.0



4.5mm Height
 For MiniCard

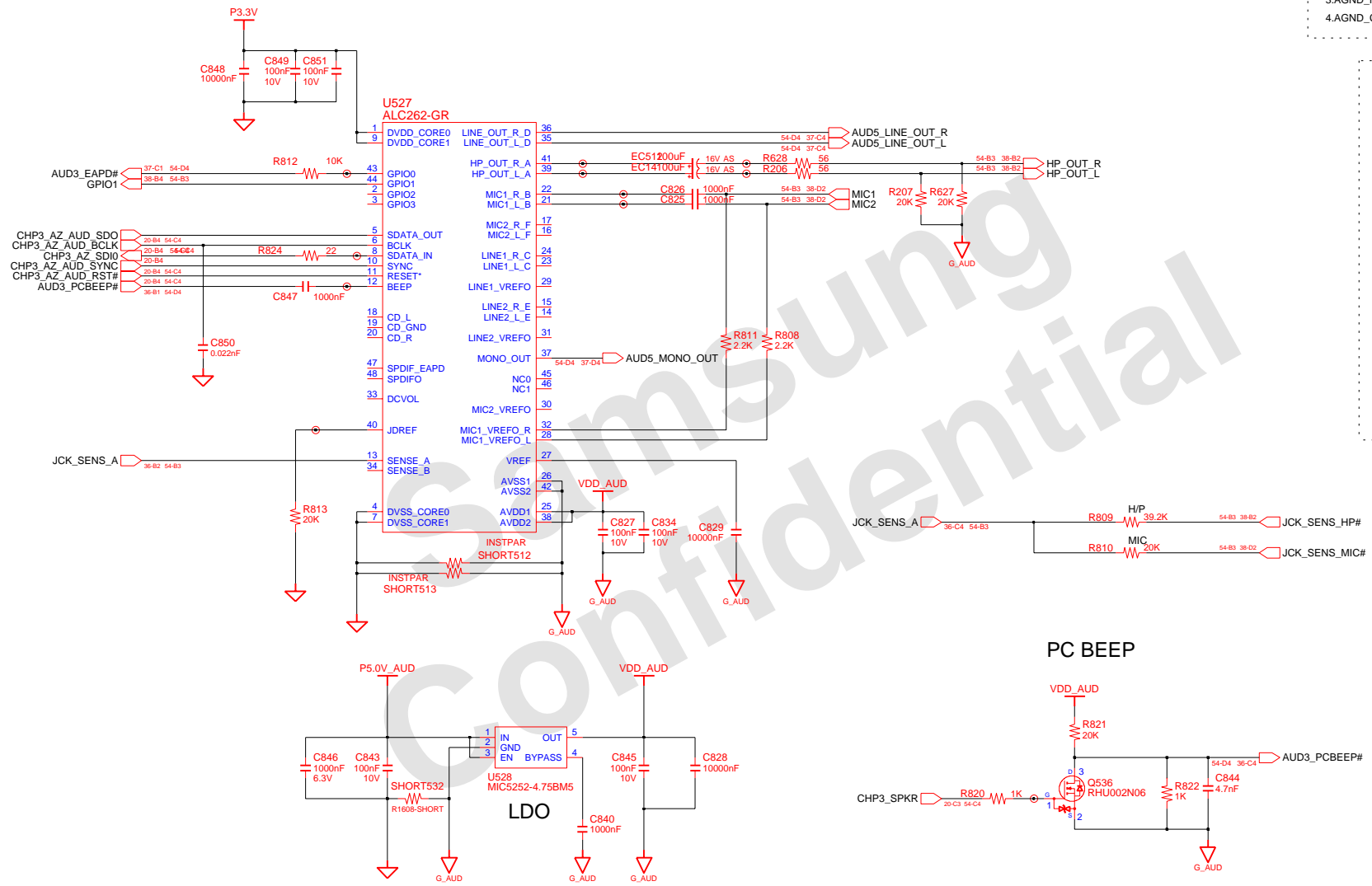
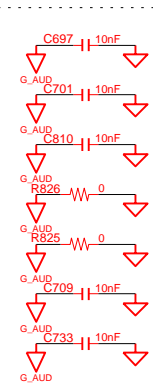
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	MINI CARD	PART NO.	BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	35	OF 54

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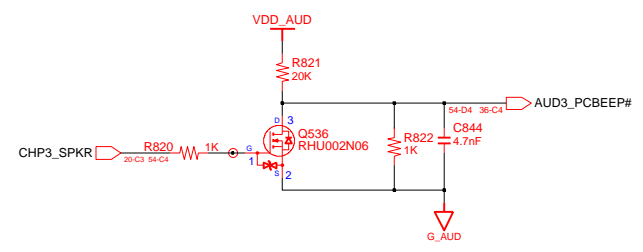
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- 1.AGND_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASSIS GROUND

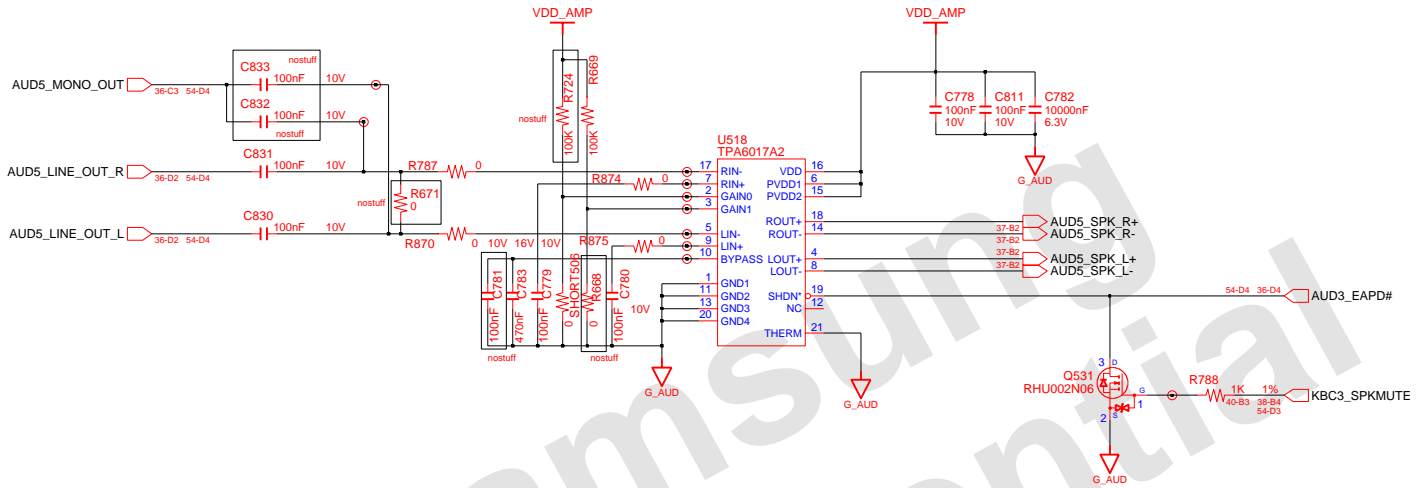
ALL TYPE IS 1608



PC BEEP



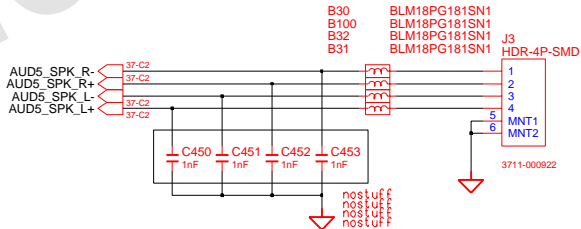
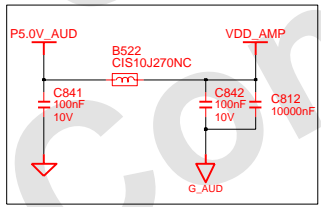
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CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		AUDIO CODEC	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	36	OF 54



INTERNAL STEREO SPEAKERS

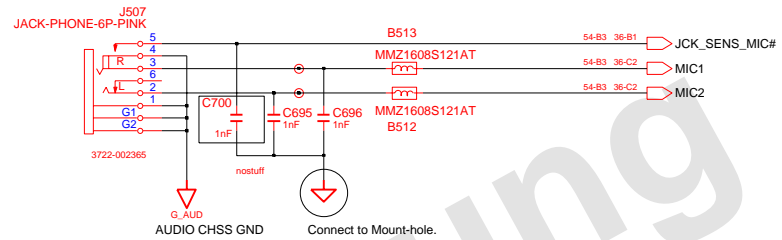
The trace bigger than 30mil

AMP_VDD

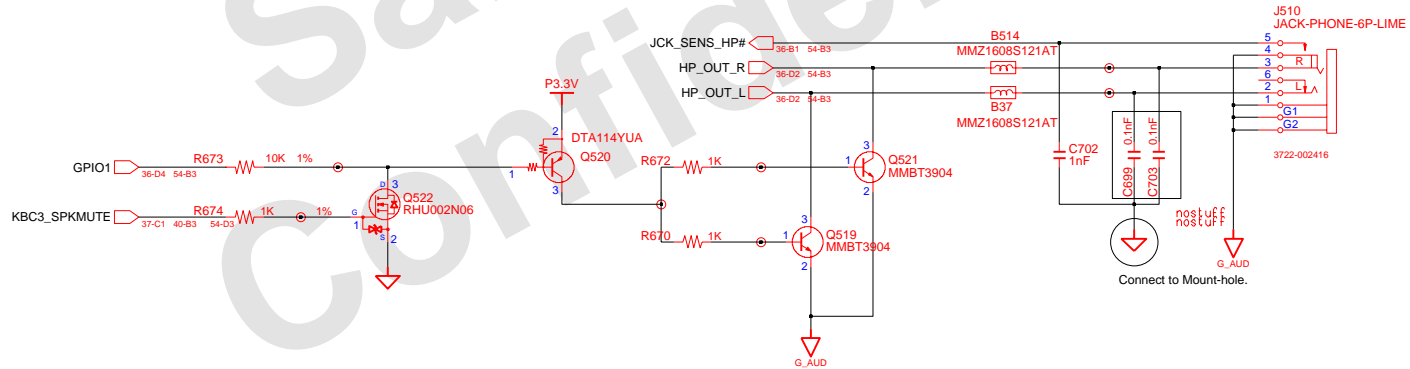


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		LIMITER & AMP	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	37	OF 54

MIC JACK



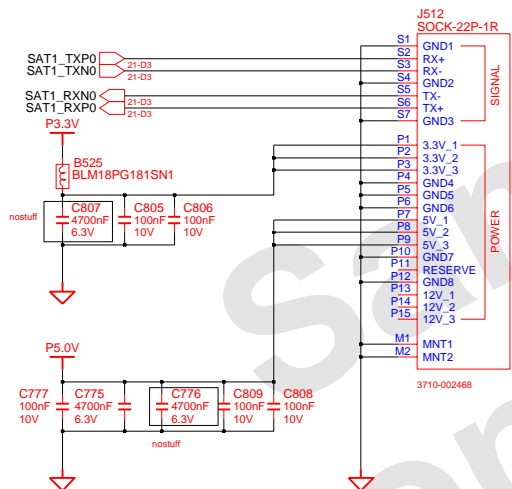
HEADPHONE



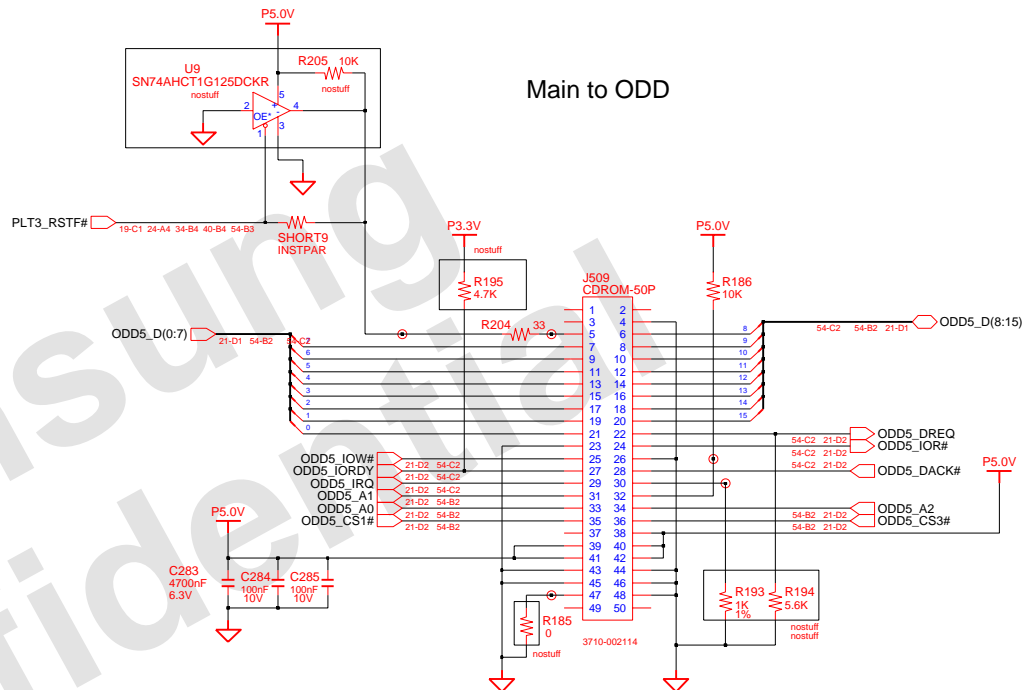
The traces led to Audio Jacks have the width over 10mil

DRAW	KI IM	DATE	5/28/2007	FILE	PRAHA_EXT	SAMSUNG
CHECK	SS BAIK	DEV. STEP	PR		MAIN	
APPROVAL	KK BIN	REV	1.0		MIC & HEADPHONE	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	38	OF 54

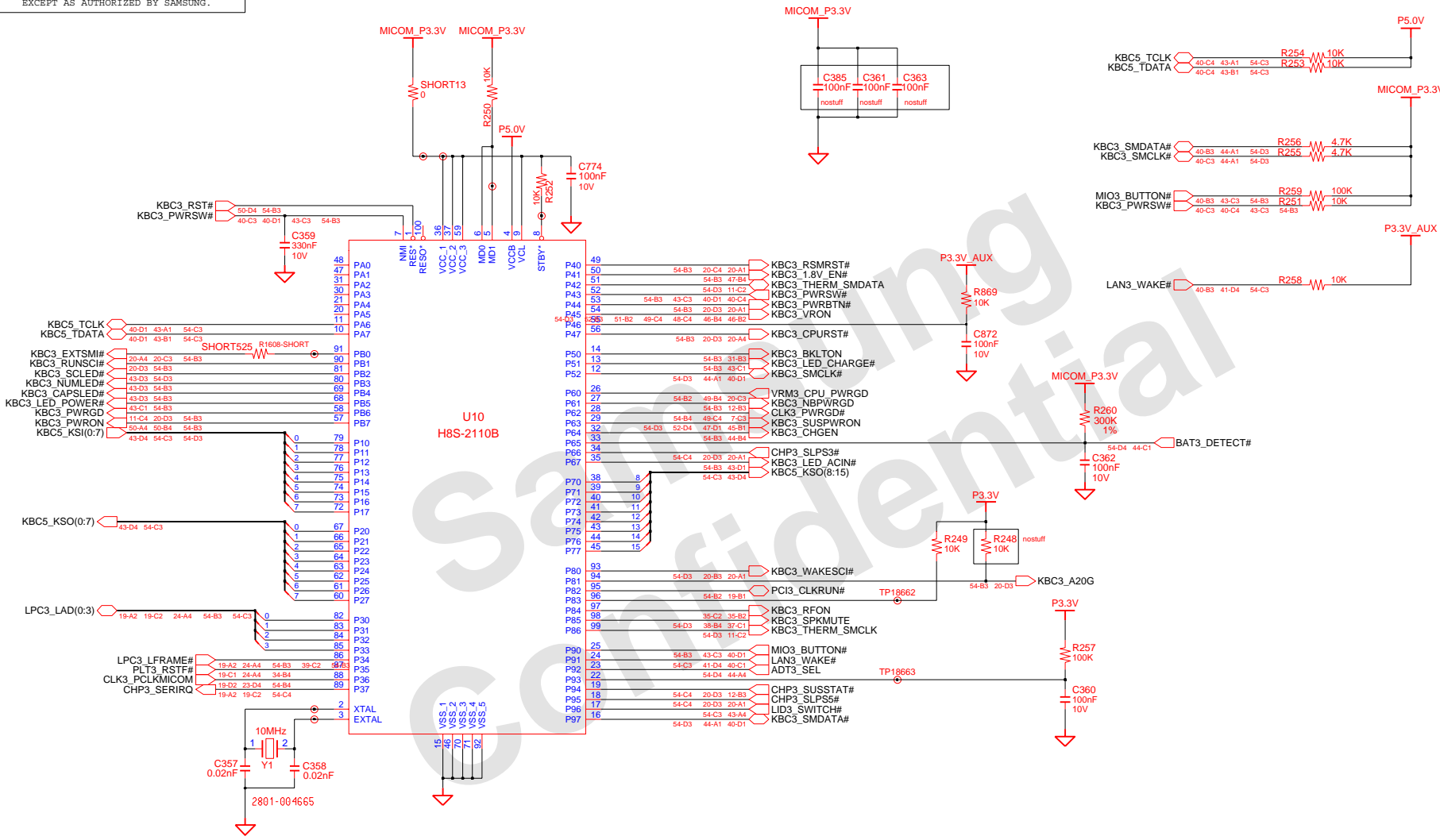
Main to HDD



Main to ODD



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	REV	1.0	
APPROVAL	KK BIN	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	39	OF 54
MODULE CODE	undefined					PART NO. BA41-00806A



MICOM Crisis Update
 Condition: P90=P91=P92=High(MICOM_P3V)
 MD0=MD1=Low(0V)
 Serial Port: P84 & P85

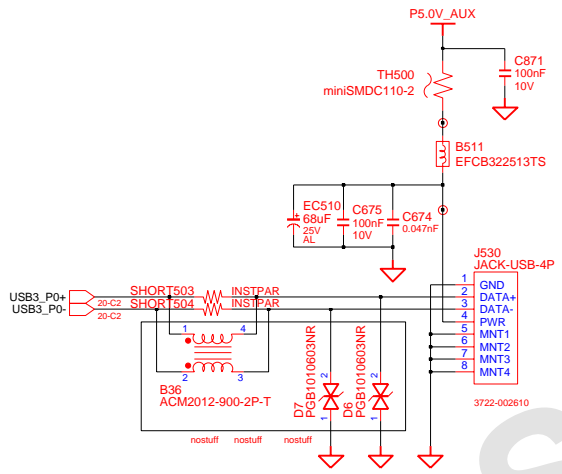
The removed signal compared from 144pin

- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR		POWER	
APPROVAL	KK BIN	REV	1.0		MICOM	PART NO. BA41-00806A
MODULE CODE	undef ined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	40	OF 54

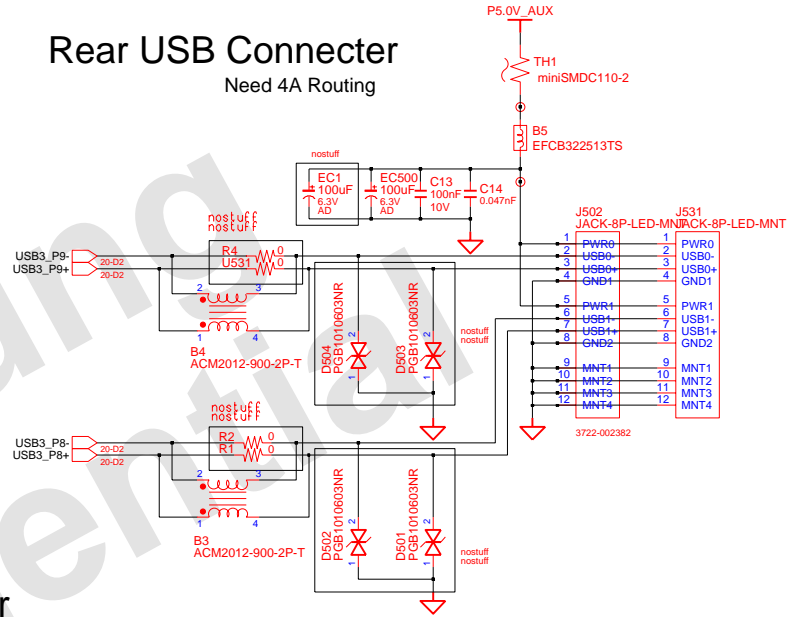
Check if need USB Power S/W(TPS2062)

Side USB Connector



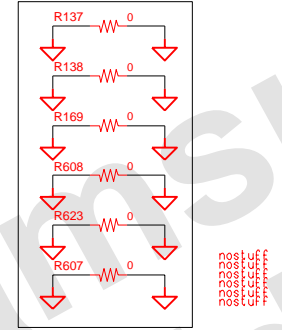
Rear USB Connector

Need 4A Routing

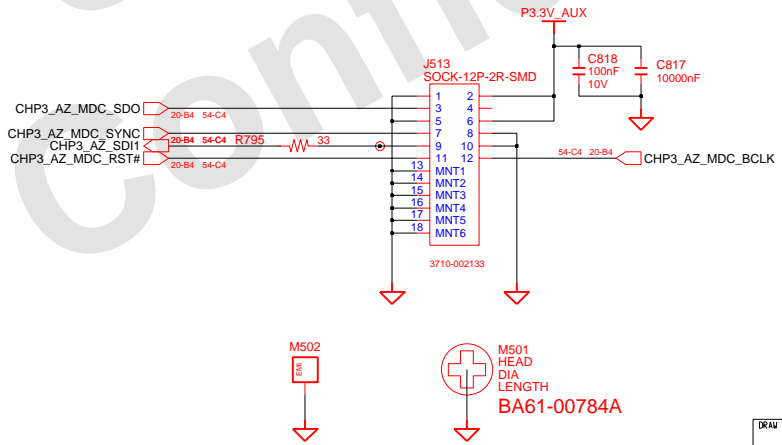


Connect left side USB GND with CPU GND

Top : 3EA Bottom : 3EA



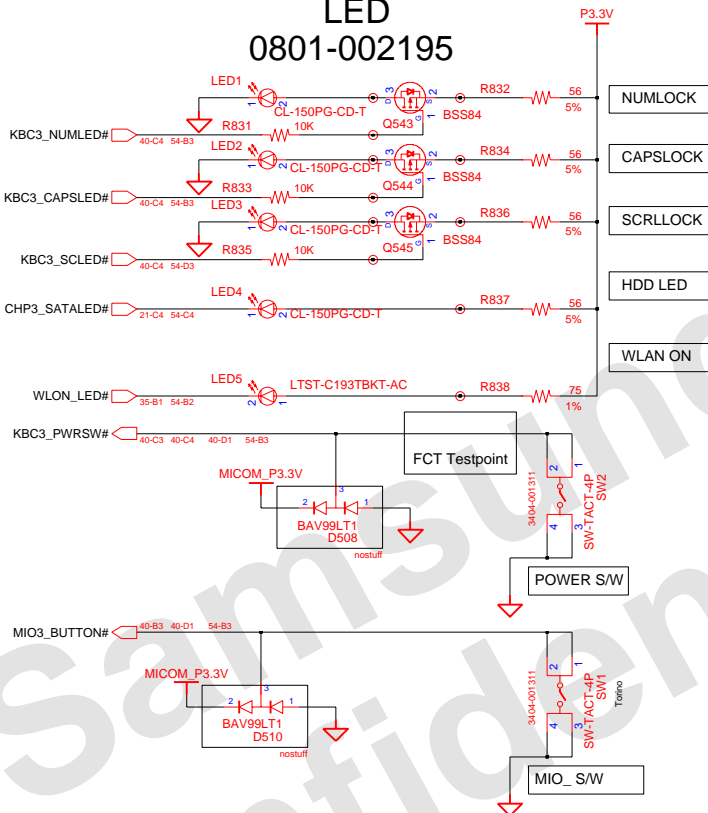
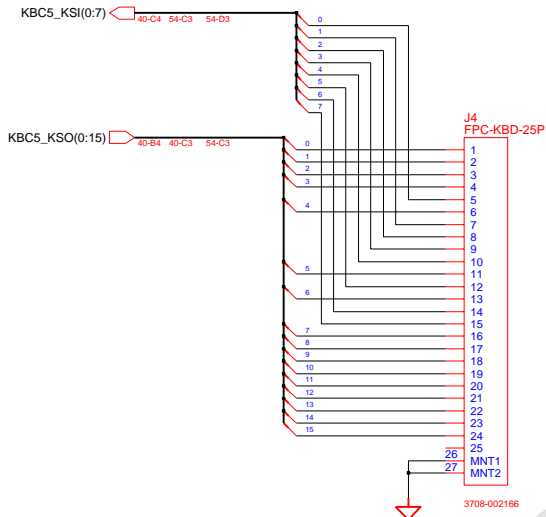
MDC Connector



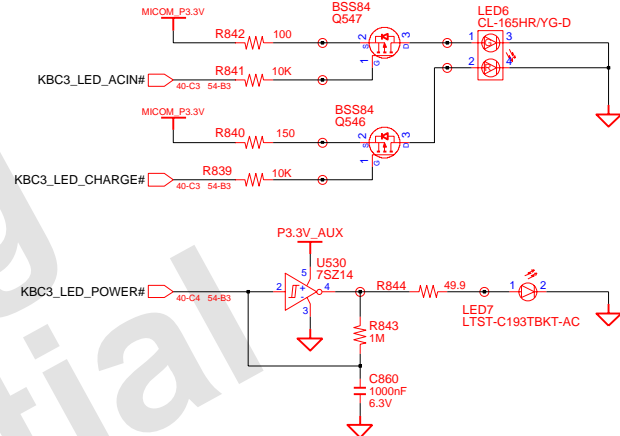
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	USB PORT & MDC Conn.		PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	42	OF 54

LED
0801-002195

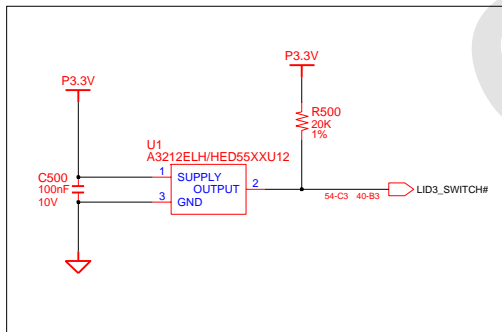
KEYBOARD



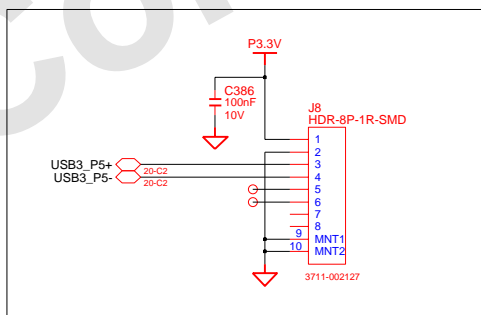
ADAPTERIN/CHARGING LED



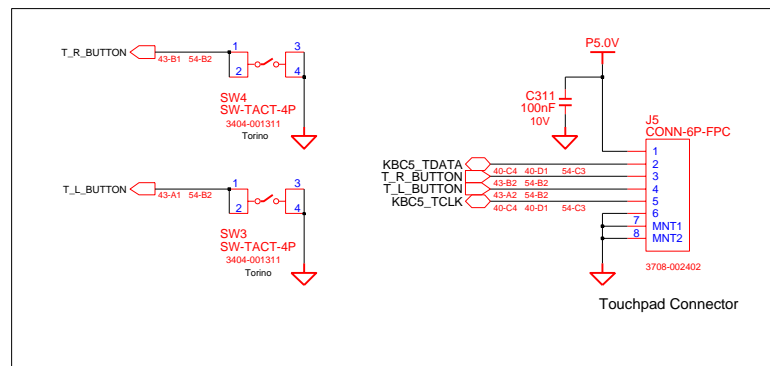
LID SWITCH



Bluetooth Interface
Factory Option



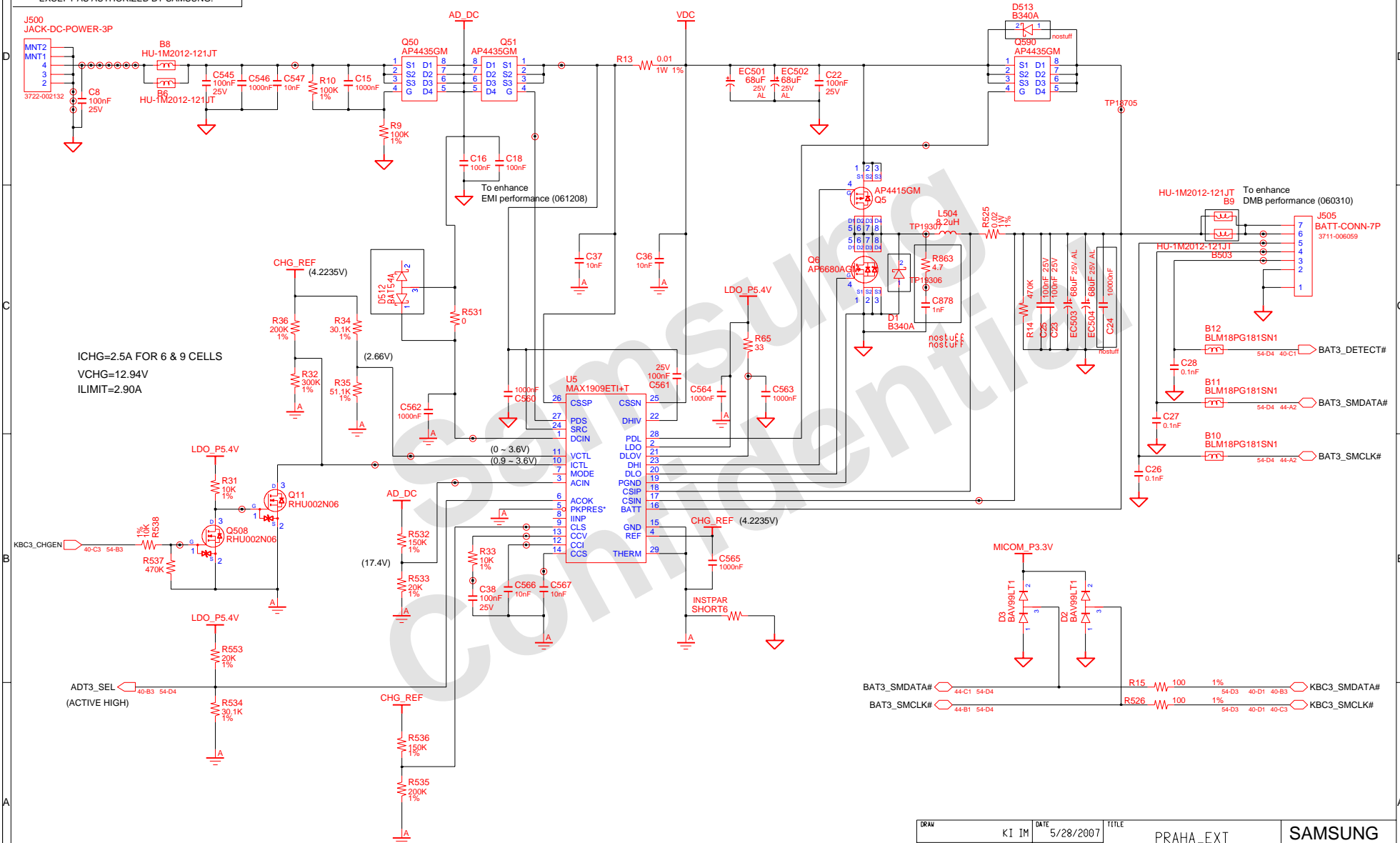
TOUCHPAD



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	LED & BLUETOOTH		
APPROVAL	KK BIN	REV	1.0	TOUCHPAD & KBD & LID S/W		PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	43	OF 54

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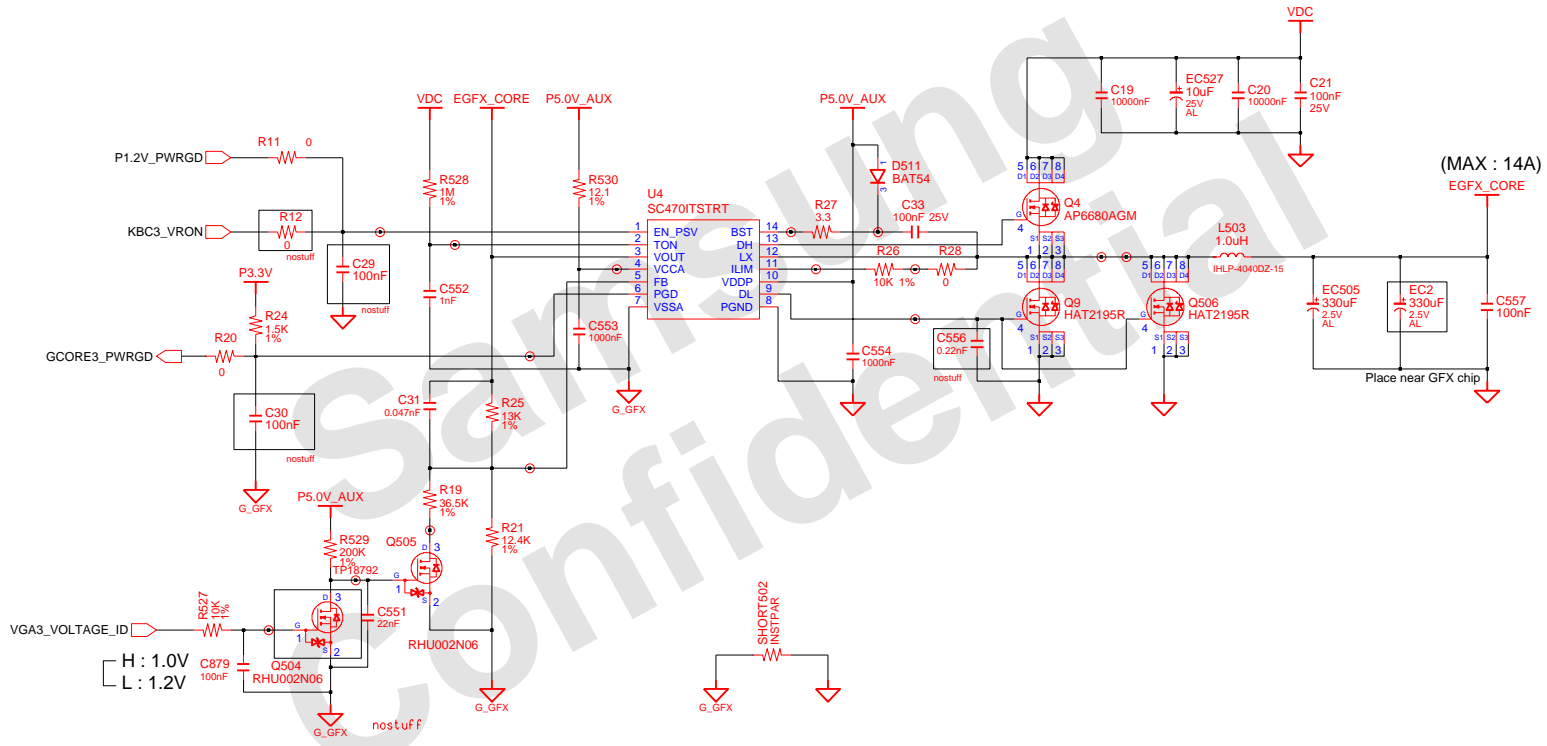
CHARGER & POWER MANAGEMENT



DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MAIN		
APPROVAL	KK BIN	REV	1.0	CHARGER		PART NO. BA41-00806A
MODULE CODE	undef ined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	44	OF 54

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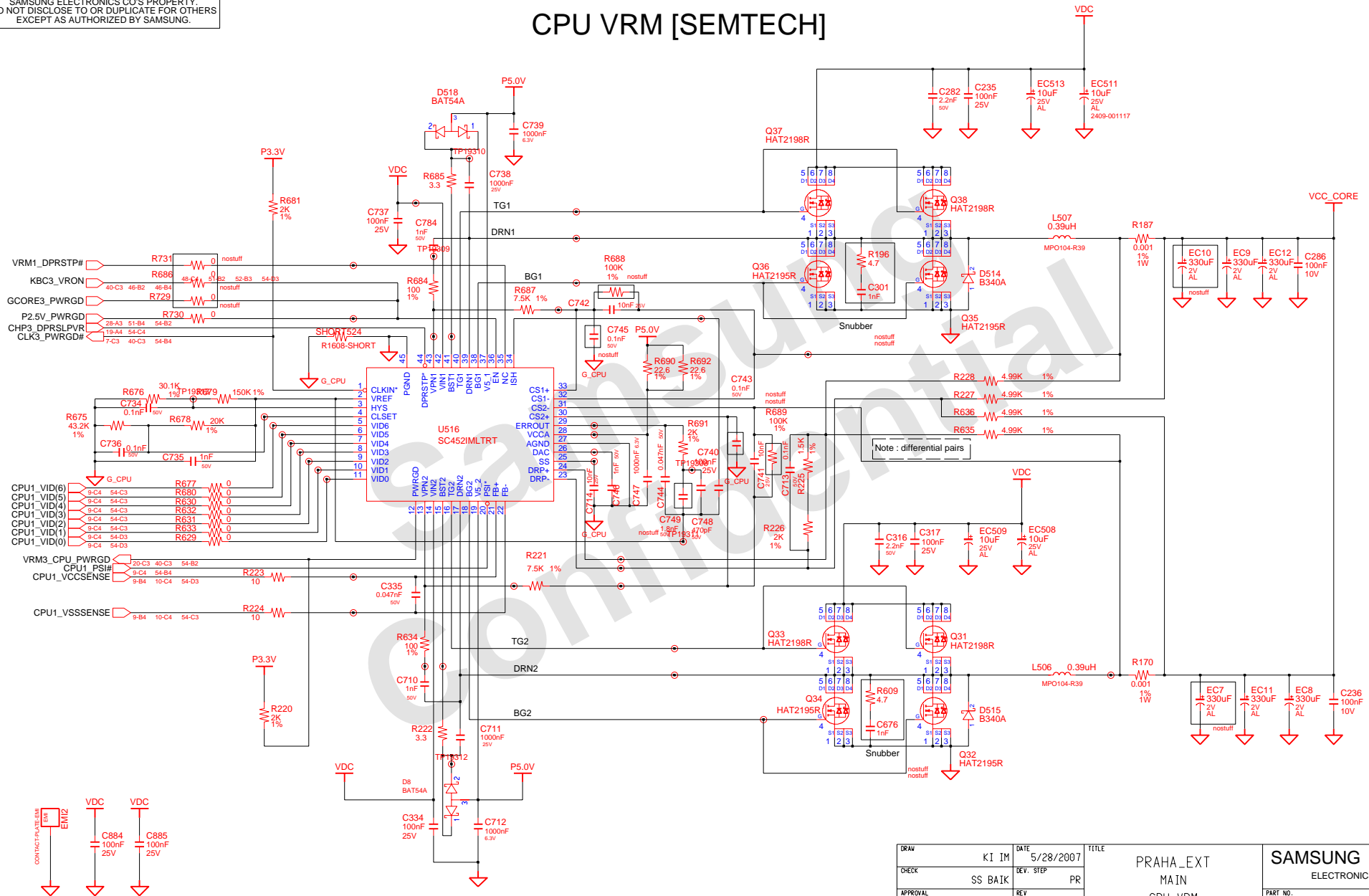
GFX CORE [SEMTECH]



DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	UNDEFINED	UNDEFINED	
APPROVAL	KK BIN	REV	1.0	UNDEFINED	UNDEFINED	PART NO. BA41-00806A
MODULE CODE		LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	48	OF 54

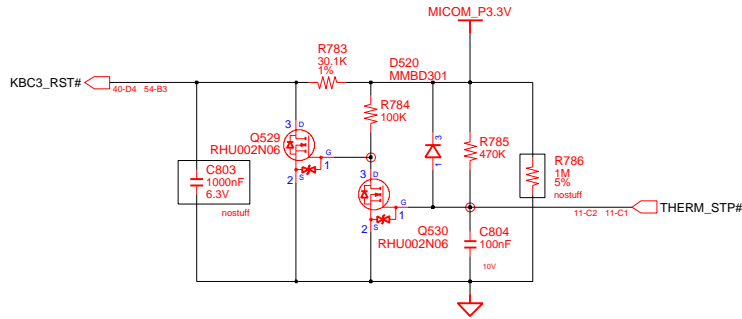
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CPU VRM [SEMTECH]

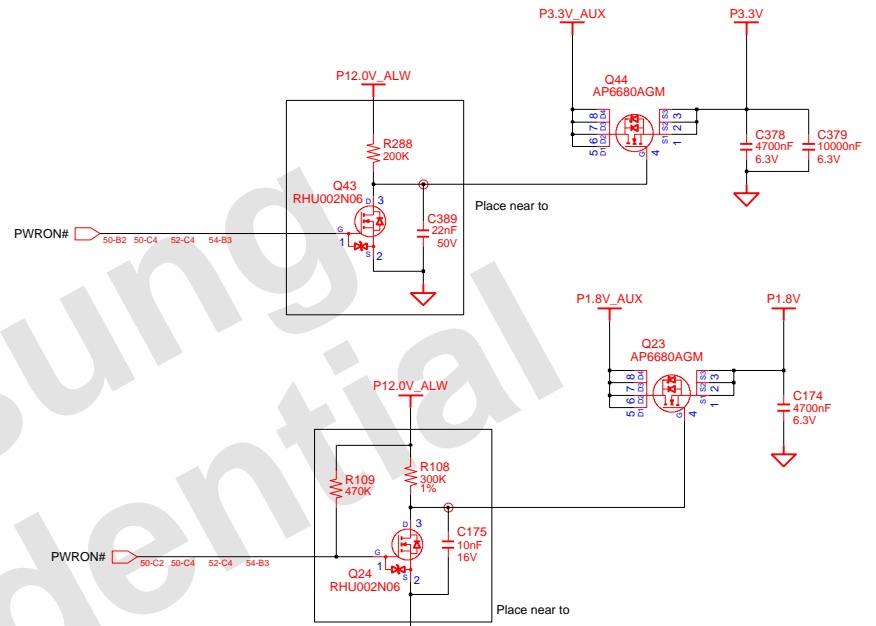


DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT MAIN CPU VRM	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	49 OF 54	

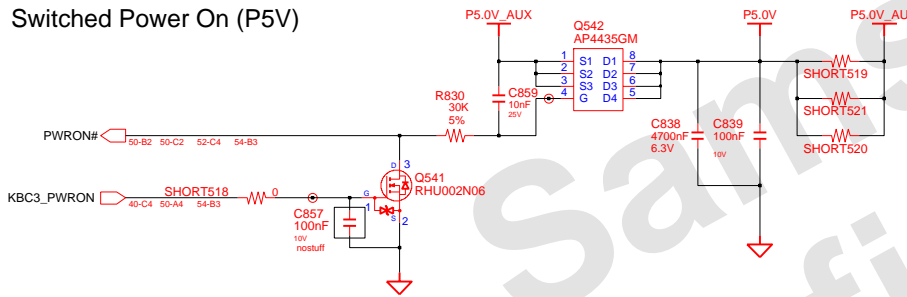
MICOM RESET



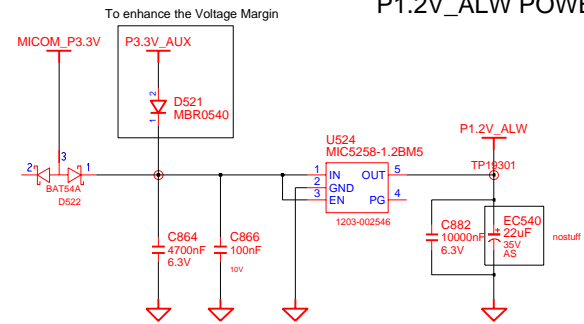
Switched Power On (P3.3V & 1.8V)



Switched Power On (P5V)

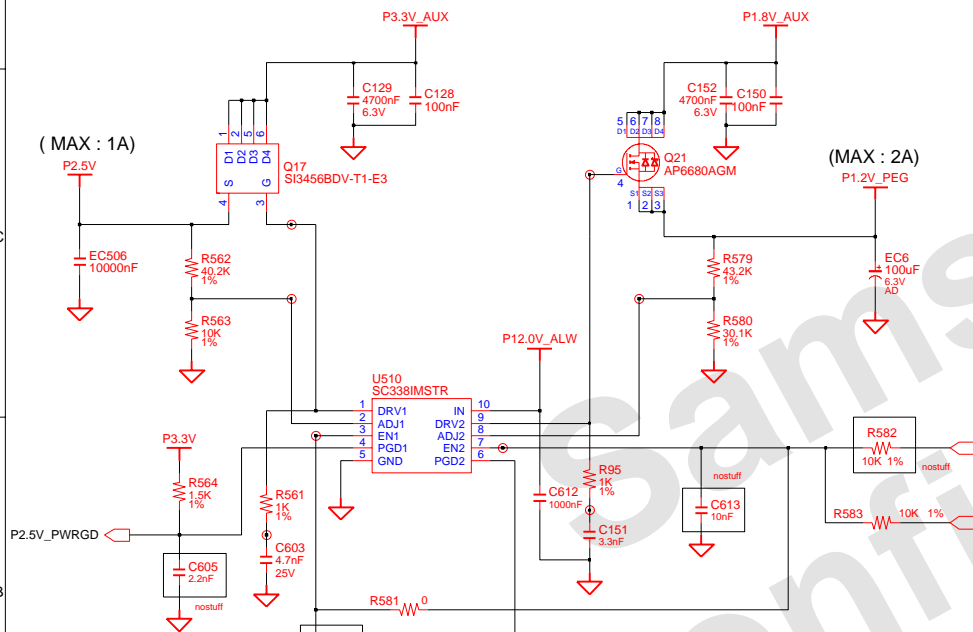


P1.2V_ALW POWER

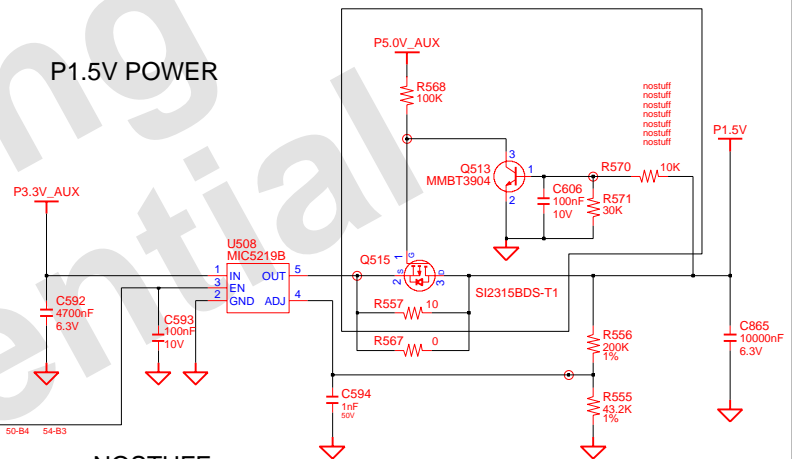


DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAIN	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	MICOM & SWITCHED POWER		
APPROVAL	KK BIN	REV	1.0	PART NO. BA41-00806A		PAGE 50 OF 54
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM			

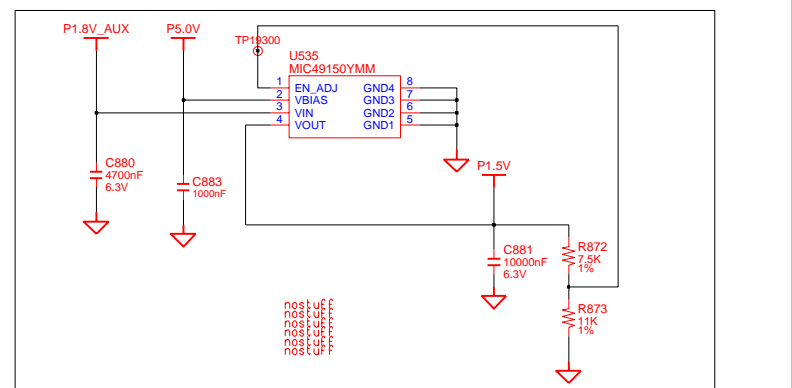
P1.2V_NB / P2.5V POWER



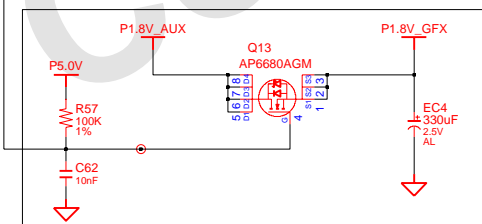
P1.5V POWER



NOSTUFF



P1.8V_GFX POWER

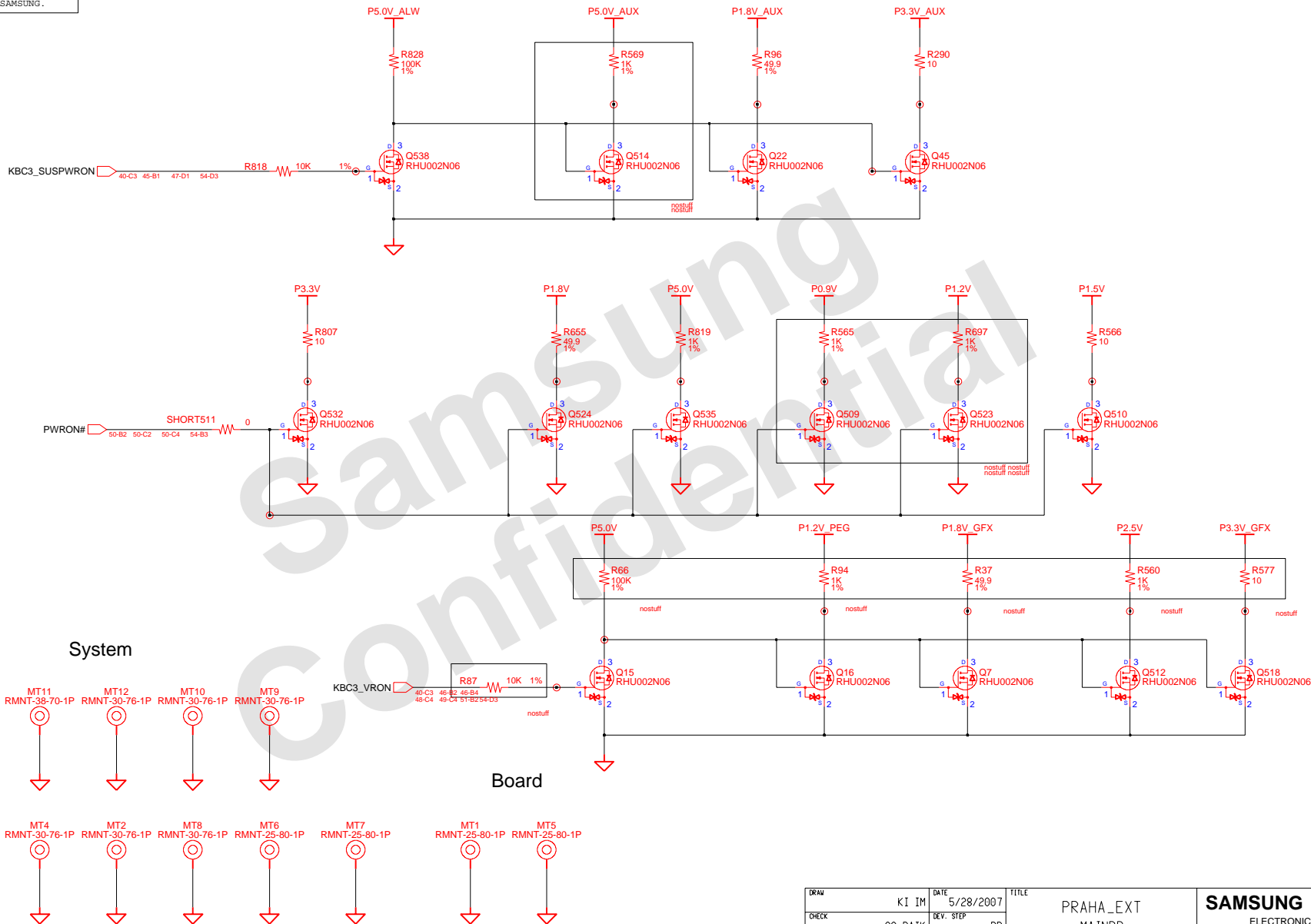


Place near GFX chip.

DRAW	KI IM	DATE	5/28/2007	TITLE	PRaha_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR	ICT PORT	PART NO.	
APPROVAL	KK BIN	REV	1.0		BA41-00806A	
MODULE CODE	undef ined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	51	OF 54

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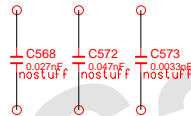
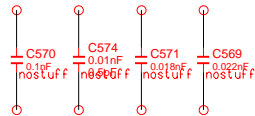
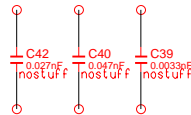
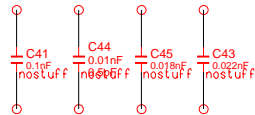


System

Board

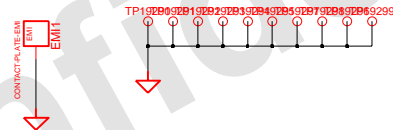
DRAW	KI IM	DATE	5/28/2007	TITLE	PRAHA_EXT MAINBND	SAMSUNG ELECTRONICS PART NO. BA41-00806A
CHECK	SS BAIK	DEV. STEP	PR	POWER DRAW & MNT HOLE		
APPROVAL	KK BIN	REV	1.0	May 28, 2007 10:24:00 AM		PAGE 52 OF 54
MODULE CODE	undefined	LAST EDIT				

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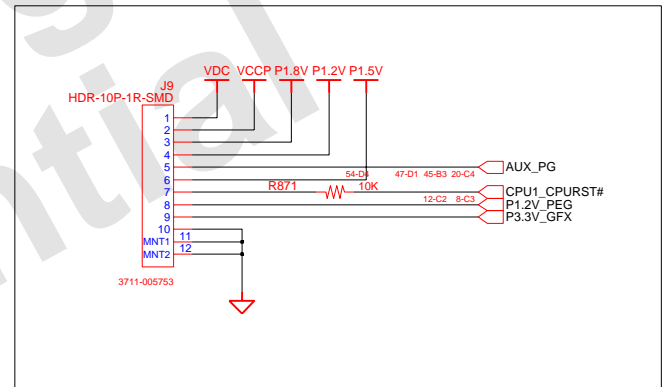


REV1
 1 ○
 2 ○ ○3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



ICT PORT



DRAW	KI IM	DATE	5/28/2007	FILE	PRAHA_EXT	SAMSUNG ELECTRONICS
CHECK	SS BAIK	DEV. STEP	PR			
APPROVAL	KK BIN	REV	1.0		TP	PART NO. BA41-00806A
MODULE CODE	undefined	LAST EDIT	May 28, 2007 10:24:00 AM	PAGE	53	OF 54

TP18982OAC_SDOUIT
 TP18983CAD3_SEL
 TP18984CAUD3_EPAP#
 TP18985CAUD3_PCBEEP#
 TP18986CAUD5_L_INE_OUT_L
 TP18987CAUD5_L_INE_OUT_R
 TP18988CAUD5_MONO_OUT

TP18993CAUX_PG
 TP18994CBAT3_DETECT#
 TP18995CBAT3_SMCLK#
 TP18996CBAT3_SMDATA#
 TP18997CCHP3_ALINK_RST#
 TP18998CCHP3_AZ_AUD_BCLK
 TP18999CCHP3_AZ_AUD_RST#
 TP19000CCHP3_AZ_AUD_SDO
 TP19001CCHP3_AZ_AUD_SYNC
 TP19002CCHP3_AZ_MDC_BCLK
 TP19003CCHP3_AZ_MDC_RST#
 TP19004CCHP3_AZ_MDC_SDO
 TP19005CCHP3_AZ_MDC_SYNC
 TP19006CCHP3_AZ_SDIO
 TP19007CCHP3_AZ_SD11
 TP19008CCHP3_BIOSUP#
 TP19009CCHP3_CPUSIP#
 TP19010CCHP3_DBRSLPVR
 TP19011CCHP3_NBRST#
 TP19012CCHP3_SATALED#
 TP19013CCHP3_SBPME#
 TP18976CCHP3_SBTMRTRIP#
 TP18977CCHP3_SERIRO
 TP18978CCHP3_SLP53#
 TP18979CCHP3_SLP55#
 TP18980CCHP3_SPKR
 TP18981CCHP3_SUSSTAT#
 TP18989CCLK3_DBGCLK
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TP18962CCPU1_DBSY#
 TP18963CCPU1_DEFR#
 TP18964CCPU1_DPRSTP#
 TP18965CCPU1_DPSLP#
 TP18966CCPU1_DPRW#
 TP18967CCPU1_DRDY#
 TP18939CCPU1_FERR#
 TP18940CCPU1_HIT#
 TP18941CCPU1_HITM#
 TP18942CCPU1_IGNNE#
 TP18943CCPU1_INIT#
 TP18944CCPU1_INT#
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 TP18948CCPU1_PWRGDOPU

TP18949CCPU1_RSQ#
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 TP18952CCPU1_SLF#
 TP18953CCPU1_SM#
 TP18954CCPU1_STPCLK#
 TP18955CCPU1_TCK
 TP18956CCPU1_TDI
 TP18957CCPU1_THRMTRIP#
 TP18958CCPU1_TMS
 TP18959CCPU1_TRDY#
 TP18960CCPU1_TRST#
 TP18961CCPU1_VCGSENSE
 TP18914CCPU1_VID(0)
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 TP18921CCPU1_VSSSENSE
 TP18922CCPU2_THERMID#
 TP18923CCPU2_THERMDC
 TP18924CCPU2_THRMTRIP#
 TP18925CCRT5_VSYNC
 TP18926CCRT5_VSYNC

TP18927CCTRL_R8_25
 TP18928CCTRL_12
 TP18929CEXP3_CLKREQ#
 TP18930CEXP3_CPE#
 TP18931CEXP3_CPBUS#
 TP18932CEXP3_PERST#
 TP18933CFAN3_FDBACK#
 TP18934CFANS_VDD
 TP18935CCORE3_PWRCD
 TP18938CGFX3_THRMTRIP#

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 TP18901CGPI0(13)

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 TP18905CHP_OUT_R
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 TP18907CITPS_SYSRST#
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 TP18909CJCK_SENS_HP#
 TP18910CJCK_SENS_MIC#
 TP18911CKBC3_1_8V_EN#
 TP18912CKBC3_A20G
 TP18913CKBC3_BKLTON
 TP18865CKBC3_CAPSLED#
 TP18866CKBC3_CHGEN
 TP18867CKBC3_CPRST#
 TP18868CKBC3_EXTSMI#
 TP18869CKBC3_LED_ACIN#
 TP18870CKBC3_LED_CHARGE#
 TP18871CKBC3_LED_POWER#
 TP18872CKBC3_NBPWRGD
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 TP18874CKBC3_PWRBTN#
 TP18875CKBC3_PWRGD
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 TP18878CKBC3_RSMRST#
 TP18879CKBC3_RST#
 TP18880CKBC3_RUNSCI#

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 TP18861COLAN3_EDID_DATA
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 TP18863COLPC3_LAD(0)
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TP19025OSC486_EN_PSV
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TP19028OSMB3_CLK
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 TP19036OSTRAP_USB4#
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 TP19039OPEG3_CRT_HS_YNC
 TP19040OPEG3_CRT_RED
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 TP19044OPEG3_LCD_BR11
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 TP19099OV5FLT

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 TP19111OVCC_CR1
 TP19115OVCC
 TP19119OVDD_AMP
 TP19123OVDD_AUB
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 TP19128OP3_3V_GFX
 TP19135OP3_3V_MCD
 TP19136OP5_0V
 TP19140OP5_0V_ALW
 TP19144OP5_0V_AUD
 TP19148OP5_0V_AUX
 TP19152OPCIE_VDDR

TP19159OP1_8V_AUX
 TP19160OP1_8V_GFX
 TP19167OP12_0V_ALW
 TP19168OP2_5V