Intel® Server Board SE7501HG2

Technical Product Specification

Revision 1.0

January 2003

Enterprise Platforms and Services Division

Revision History

Date	Revision Number	Modifications
October 25, 2002	0.5 (Draft)	Initial release.
November 7, 2002	0.6 (Draft)	Fab-2 edits
November 15, 2002	0.7	Additional Fab-2 notations, processor support, signal changes
January 18, 2003	1.0	Final Release

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1. Introduction

The Intel® Server Board SE7501HG2 Technical Product Specification (TPS) provides technical details for the server board's functional architecture and feature set. It also provides a high-level detail of some of the board's functional sub-systems.

This document is sub-divided into the following main chapters:

Chapter 2: SE7501HG2 Server Board Overview

Chapter 3: Functional Architecture

Chapter 4: Configuration and Initialization

Chapter 5: Clock Generation and Distribution

Chapter 6: PCI I/O Subsystem

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1.1 Audience

This document is intended for technical personnel who desire a technical overview of the SE7501HG2 server board. Familiarity with personal computers, device interfaces, Intel® server architecture and the Peripheral Component Interconnect (PCI and PCI-X) local bus architecture is assumed.

2. SE7501HG2 Server Board Overview

The server board SE7501HG2 is a monolithic printed circuit board with features that were designed to support the general-purpose volume server market. The architecture is based on the Intel® E7501 chipset and is capable of supporting one or two Intel® Xeon™ processors and up to twelve gigabytes of memory.

2.1 SE7501HG2 Feature Set

The SE7501HG2 sever board supports the following feature set:

- Dual Intel® Xeon™ processors in FC-PGA2P package using Socket 604
- 533 MHz Front Side Bus
- Intel® E7501 chipset
    - E7501 Memory Controller Hub
    - P64H2 PCI/PCI-X 64-bit PCI/PCI-X Controller Hub2
    - ICH3-S I/O Controller Hub
- Support for six DDR266 compliant registered ECC DDR DIMMs providing up to 12 GB of memory.
- Three separate and independent PCI buses:
    - Segment A: 32-bit, 33 MHz, 5 V, Full-length PCI (P32-A) with one embedded devices:
        - Three slots: 32-bit/33MHz PCI Slot (PCI Slot 4, Slot 5 and Slot 6)
        - 2D/3D graphics controller: ATI RAGE* XL Video Controller with 8 MB of SDRAM
    - Segment B: 64-bit, 100 MHz, 3.3 V, Full-length PCI (P64-B) supporting the following configuration:
        - Two slots: 64-bit/100MHz PCI-X[1] Slots (PCI-X Slot 2 and Slot 3)
        - Dual-channel Adaptec* AIC-7902 wide Ultra-320 SCSI Controller
        - Dual-channel Adaptec* HostRAID support
        - Zero Channel RAID (ZCR) support. Also known as modular M-ROMB (Slot2)
    - Segment C: 64-bit, 133 MHz, 3.3 V, Full-length PCI (P64-C) supporting the following configuration:
        - One slot: 64-bit/133MHz PCI-X[1] Slots (PCI-X Slot 1)
        - Dual –channel Intel® 82546EB Gigabit Ethernet Controller
- LPC (Low Pin Count) bus segment with two embedded devices:
    - Baseboard Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on server board

[1] The BIOS is responsible for setting the mode (PCI or PCI-X) and bus speed for the two segments provided by the P64H2. The actual bus mode/speed will be determined by the least capable card installed on that bus.

- Super I/O controller chip providing all PC-compatible I/O (floppy, serial, parallel, keyboard, mouse) X-Bus segment with one embedded device:
    - Flash ROM device for system BIOS: Intel® 32 megabit 28F320C3 Flash ROM
- Three external Universal Serial Bus (USB) ports on the rear of the board with an additional internal header that provides one optional USB port for front panel.
- Two serial ports: One serial port on the rear of the board and one internal header is also available providing an optional Serial B port.
- Two IDE connectors, supporting up to four ATA-100 compatible devices
- Six hot swappable multi-speed system fans and two single-speed CPU fans
- Multiple server management headers providing on-board interconnects to the board's server management features
- SSI-EEB3.0 compliant board form factor, the board size is 12 inch by 13 inch
- SSI-compliant connectors for SSI interface support the 34-pin front panel, floppy, ATA-100 and power connectors

The following figure shows the functional blocks of the server board and the plug-in modules that it supports.

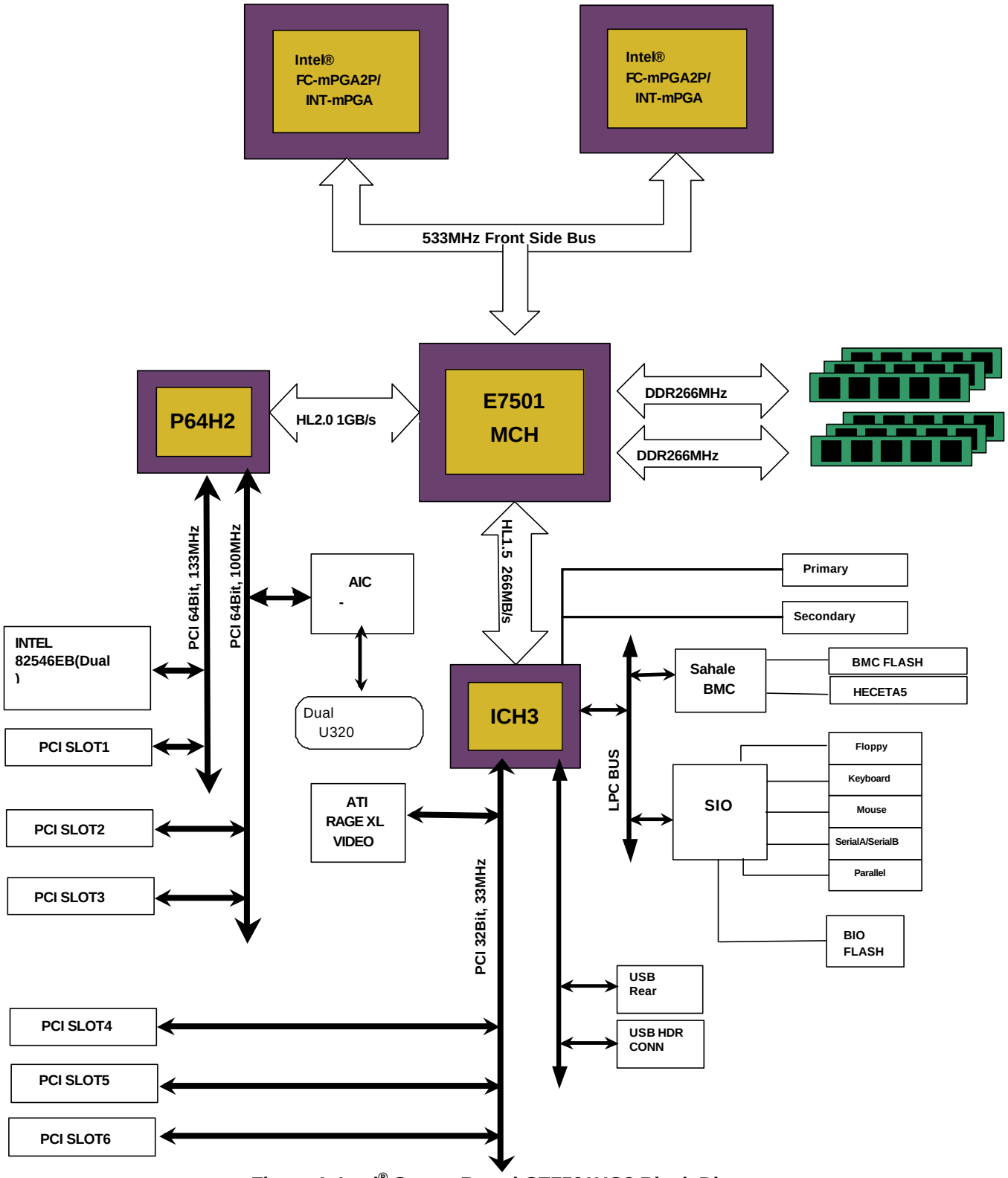


Figure 1. Intel® Server Board SE7501HG2 Block Diagram

3. Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the Intel® Server Board SE7501HG2.

3.1 Processor and Memory Subsystem

The Intel® E7501 chipset provides a 36-bit address, 64-bit data processor host bus interface, operating at 533MHz in the AGTL+ signaling environment. The MCH component of the chipset provides an integrated memory controller, an 8-bit hub interface, and three 16-bit hub interfaces.

The hub interface can provide the interface to two 64-bit, 133-MHz, Rev 1.0 compliant PCI-X buses via the P64H2. The server board SE7501HG2 directly supports up to 12 GB of ECC memory, using six DDR266-compliant registered DIMMs. The ECC implementation in the MCH can detect and correct single-bit errors, can detect multiple-bit errors, and supports the Intel® SDDC feature with x4 DIMMs.

3.1.1 Processor Support

The server board SE7501HG2 supports one or two Intel® Xeon™ processors in the Socket 604 FCPGA2P package. The server board will support the Intel® Xeon processors with 512KB L2 cache. When two processors are installed, both processors must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it should be in the socket labeled CPU-1 (nearest to the edge of the board) and the other socket must be empty. The support circuitry on the server board consists of the following:

- Dual Socket Support for either FC-mPGA2P (533Mhz 604 pin) or INT3-mPGA (400Mhz 603 pin) processor packages (in dual processor configurations both processors must be identical)

Table 1. SE7501HG2 Intel® Xeon™ Processor Support Matrix

Processor Family	Package Type	FSB Frequency	Frequency	Cache Size	Support
Intel® Xeon™	INT3-mPGA	400 MHz	1.8 GHz	512KB	Yes
Intel® Xeon	INT3-mPGA	400 MHz	2.0 GHz	512KB	Yes
Intel® Xeon	INT3-mPGA	400 MHz	2.2 GHz	512KB	Yes
Intel® Xeon	INT3-mPGA	400 MHz	2.4 GHz	512KB	Yes
Intel® Xeon	INT3-mPGA	400 MHz	2.6 GHz	512KB	Yes
Intel® Xeon	INT3-mPGA	400 MHz	2.8 GHz	512KB	Yes
Intel® Xeon	INT3-mPGA	400 MHz	3.0 GHz	512KB	Yes
Intel® Xeon	FC-mPGA2P	533 MHz	1.8 GHz	512KB	Yes
Intel® Xeon	FC-mPGA2P	533 MHz	2.0 GHz	512KB	Yes
Intel® Xeon	FC-mPGA2P	533 MHz	2.2 GHz	512KB	Yes
Intel® Xeon	FC-mPGA2P	533 MHz	2.4 GHz	512KB	Yes
Intel® Xeon	FC-mPGA2P	533 MHz	2.6 GHz	512KB	Yes
Intel® Xeon	FC-mPGA2P	533 MHz	2.8 GHz	512KB	Yes

Processor Family	Package Type	FSB Frequency	Frequency	Cache Size	Support
Intel® Xeon	FC-mPGA2P	533 MHz	3.06 GHz	512KB	Yes

Notes:

- The SE7501HG2 incorporates an auto-termination feature on the second processor socket (labeled CPU #2), which is designed to automatically terminate signal lines that would not be in use in a single processor configuration. If a single processor is to be used, the processor must be located in the primary socket which is closest to the edge of the system board (labeled CPU #1). For socket locations, refer to Figure 17 of this document.

- The server board SE7501HG2 is designed to provide up to 75 Amps per processor. Processors with higher current requirements are not supported.

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor module presence detection logic
- Server management registers and sensors
- Reset configuration logic
- APIC Bus

3.1.1.1 Processor VRM

The SE7501HG2 baseboard has a single VR (voltage regulator) to support two processors. It is compliant with the VRM 9.1 specification and provides a maximum of 150 Amps, which is capable of supporting current supported processors as well as future processors that do not exceed the 150 Amp limit.

The board hardware and BMC will read the processor VID (voltage identification) bits for each processor before turning on the VRM. If the VIDs of the two processors are not identical, then the BMC will not turn on the VRM and a beep code is generated.

3.1.1.2 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc., through the CPUID instruction. The requirements are that all processors in the system must operate at the same frequency and have the same cache sizes. No mixing of product families is supported.

The processor information is read at every system power-on and the speed is set to the fixed processor speed.

Note: No manual processor speed setting options exist either in the form of a BIOS setup option or jumpers when using production level processors.

3.1.1.3 Processor Module Presence Detection

Logic on the baseboard detects the presence and identity of installed processors. The PMC checks the logic and will not turn on the system DC power unless the VIDs of both the processors match in a DP configuration.

3.1.1.4 Interrupts and APIC

Interrupt generation and notification to the processors are done by the APICs in the ICH3-S and the P64H2 using messages on the front side bus.

3.1.1.5 Server Management Registers and Sensors

The baseboard management controller manages registers and sensors associated with the processor / memory subsystem.

3.1.2 Memory Subsystem

The server board SE7501HG2 supports up to six DIMM slots for a maximum memory capacity of 12 GB. The DIMM organization is x72, which includes eight ECC check bits. The memory interface runs at 266MHz. The memory controller supports memory scrubbing, single-bit error correction and multiple-bit error detection and Intel® Single Device Data Correction (SDDC) support with x4 DIMMs. Memory can be implemented with either single-sided (one row) or double-sided (two row) DIMMs.

Note: Intel does not test, recommend, or support mixing of memory types within the same server system. Functionality issues may occur if mixed memory types are installed in the same server system. Intel recommends that memory modules of identical size, type, banking and stacking technology, and vendor are installed in each server system. Intel will not provide support for issues encountered when mixed memory configurations are in use.

The following figure provides a block diagram of the memory sub-system implemented on the server board SE7501HG2.

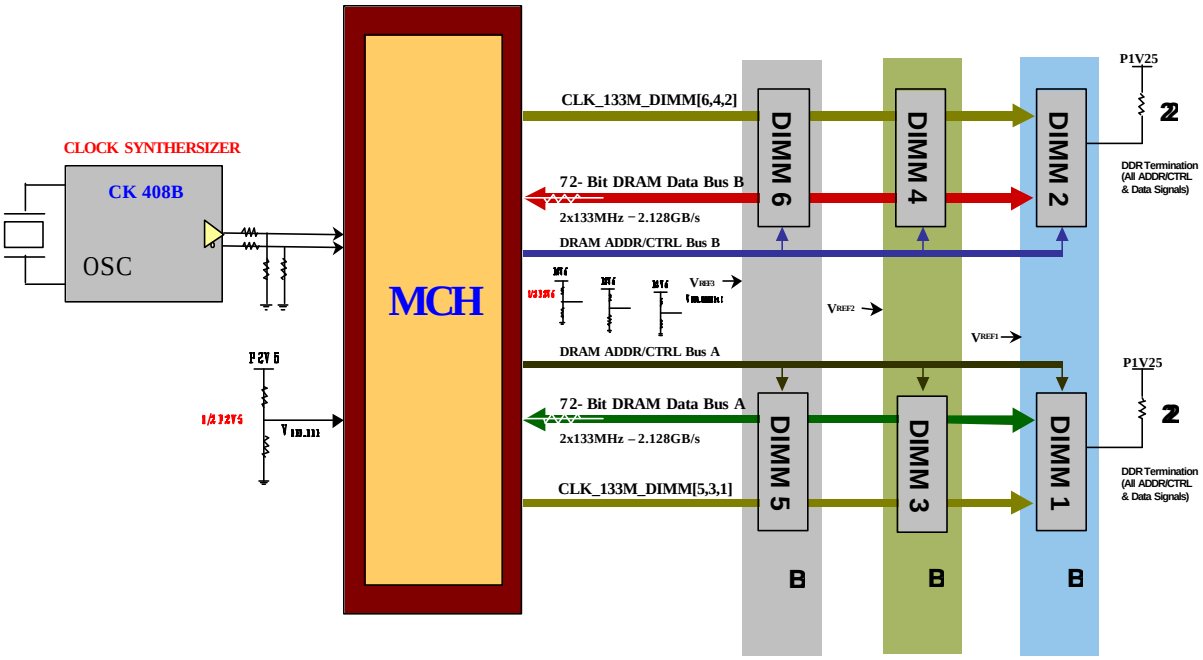


Figure 2. Memory Sub-system Block Diagram

3.1.2.1 Memory DIMM Support

The server board SE7501HG2 supports DDR266 compliant registered ECC DIMMs and DDR 266-compliant ECC DIMMs operating at 266 MHz DDR. Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported on the server board SE7501HG2. A list of qualified DIMMs will be made available. Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported.The minimum supported DIMM size is 128 MB. Therefore, the minimum main memory configuration is 2 x 128 MB or 256 MB. The largest size DIMM supported is a 2 GB stacked registered DDR266 ECC DIMM based on 512 megabit technology.

- Only registered DDR266 compliant, ECC, DDR memory DIMMs will be supported
- ECC single-bit errors will be corrected and multiple-bit errors will be detected.
- SE7501HG2 supports the Intel® Single Device Data Correction (SDDC) feature with x4 DIMMs.
- The maximum memory capacity is 12 GB
- The minimum memory capacity is 256 MB

3.1.2.2 Memory Configuration

Memory interface between the MCH and DIMMs is 144 bits wide. This requires that two DIMMs be populated per bank in order for the system to operate. At least one bank must be populated before the system will boot. If additional banks have less than two DIMMs, the memory for that bank(s) will not be available to the system.

There are three banks of DIMMs, labeled 1, 2, and 3. Bank 1 contains DIMM locations 1A and 1B; Bank 2 contains 2A and 2B; Bank 3 contains 3A and 3B. DIMM socket identifiers are marked with a silk screen next to each DIMM socket on the baseboard. Note that the sockets associated with any given bank are located next to each other.

The baseboard's signal integrity and cooling are optimized when memory banks are populated in order. Therefore, Bank 1 must be installed in pair before Banks 2 and 3.

DIMM and memory configurations must adhere to the following:

- DDR266 DDR registered DIMM modules
- DIMM organization: x72 ECC
- Pin count: 184
- DIMM capacity: 128 MB, 256 MB, 512 MB, 1 GB, 2GB DIMMs
- Serial PD: JEDEC Rev 2.0
- Voltage options: 2.5 V (VDD/VDDQ)
- Two DIMMs must be populated in a bank for a x144 wide memory data path

Table 2. Memory Bank Labels

Memory DIMM	Bank	Row
J9D1 (DIMM 1A), J8D3 (DIMM 1B)	1	0, 1
J8D2 (DIMM 2A), J8D1 (DIMM 2B)	2	2, 3
J7D2 (DIMM 3A), J7D1 (DIMM 3B)	3	4, 5

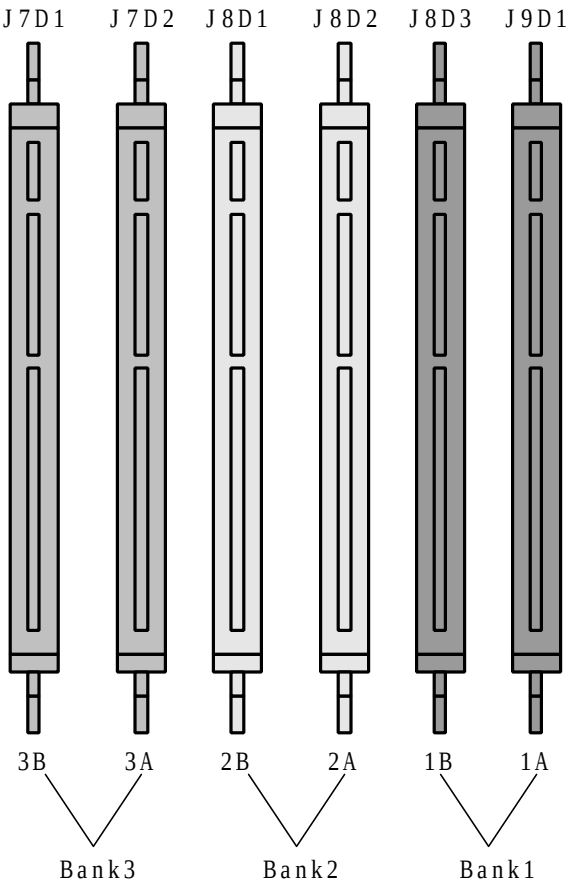


Figure 3. Memory Bank Label Definition

3.1.2.3 I²C* Bus

An I²C bus connects the BMC ICH3-S, MCH, P64H2 and the six DIMM slots. This bus is used by the system BIOS to retrieve DIMM information needed to program the MCH memory registers which are required to boot the system. The following table provides the I²C addresses for each DIMM slots.

Table 3. I²C* Addresses for Memory Module SMB

Device	Address
DIMM 1A	0xA4
DIMM 1B	0xAC
DIMM 2A	0xA2
DIMM 2B	0xAA
DIMM 3A	0xA0
DIMM 3B	0xA8

3.2 Intel® E7501 Chipset

The server board SE7501HG2 is designed around the Intel® E7501 chipset. The chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI-X). This is targeted for multiprocessor systems and standard high-volume servers. The Intel® E7501 chipset consists of three components:

- **MCH: Memory Controller Hub North Bridge.** The MCH North Bridge accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The MCH monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue for subsequent forwarding to the memory subsystem, or to an outbound request queue for subsequent forwarding to one of the PCI buses. The MCH also accepts inbound requests from the P64H2 and the ICH3-S. The MCH is responsible for generating the appropriate controls to control data transfer to and from memory.

- **P64H2: PCI-X 64bit Hub 2.0 I/O Bridge.** The P64H2 provides the interface for 64-bit, 133MHz Rev. 1.0 compliant PCI-X buses. The P64H2 is both master and target on both PCI-X buses.

- **ICH3-S: South Bridge.** The ICH3-S controller has several components. It provides the interface for a 32-bit, 33-MHz Rev. 2.2-compliant PCI bus. The ICH3-S can be both a master and a target on that PCI bus. The ICH3-S also includes a USB controller and an IDE controller. The ICH3-S is also responsible for much of the power management functions, with ACPI control registers built in. The ICH3-S also provides a number of GPIO pins and has the LPC bus to support low speed legacy I/O.

The MCH, P64H2, and ICH3-S chips provide the pathway between processor and I/O systems. The MCH is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the MCH communicates with the P64H2 through a private interface called the HI (Hub Interface) 2.0 bus. If the cycle is directed to the ICH3-S, the cycle is output on the MCH's 8-bit HI 1.5 bus. The P64H2 translates the HI 2.0 bus operation to a 64-bit PCI Rev. 2.2-compliant signaling environment operating at from 133MHz to 33 MHz.

The HI 2.0 bus is 16-bit wide and operates at 66 MHz running 8x data transfers, providing over 1 GB per second of bandwidth.

All I/O for the SE7501HG2, including PCI and PC-compatible, is directed through the MCH and then through either the P64H2 or the ICH3-S provided PCI buses.

- The ICH3-S provides a 32-bit/33-MHz PCI bus hereafter called P32-A
- The P64H2 provides two independent 64-bit buses hereafter called P64-B, and P64-C. P64-C is the PCI-X bus with dual channel gigabit Ethernet controller and P64-B is the PCI-X bus with SCSI controller integrated.

This independent bus structure allows all three PCI buses to operate concurrently.

3.2.1 MCH Memory Architecture Overview

The MCH supports a 144-bit wide memory sub-system that can support a maximum of 12 GB on SE7501HG2 (using 2 GB DIMMs). In this configuration, the MCH supports six DDR266 compliant registered stacked DIMMs for maximum of 12 GB.

The memory interface runs at 266MHz. It uses fifteen address lines (BA [1:0] and MA [12:0]) and supports 64 MB, 128 MB, 256 MB, and 512 MB DRAM densities. The DDR DIMM interface supports memory scrubbing, single-bit error correction, multiple bit error detection, and Intel® Single Device Data Correction (SDDC) with x4 DIMMs.

3.2.1.1 DDR Configurations

The DDR interface supports up to 12 GB of main memory and supports single- and double-density DIMMs. The DDR can be any industry-standard DDR. The following table shows the DDR DIMMs supported.

Table 4. Supported DDRs

DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	# SDRAM Devices / Rows / Banks	# Address bits Rows / Banks / Column
128MB	16M x 72	64Mbit	16M x 4	18/1/4	12/2/10
128MB	16M x 72	64Mbit	8M x 8	18/2/4	12/2/9
128MB	16M x 72	128Mbit	16M x 8	9/1/4	12/2/10
256MB	32M x 72	64Mbit	16M x 4	36/2/4	12/2/10
256MB	32M x 72	128Mbit	32M x 4	18/1/4	12/2/11
256MB	32M x 72	128Mbit	16M x 8	18/2/4	12/2/10
256MB	32M x 72	256Mbit	32M x 8	9/1/4	13/2/10
512MB	64M x 72	128Mbit	32M x 4	36/2/4	12/2/11
512MB	64M x 72	256Mbit	64M x 4	18/1/4	13/2/11
512MB	64M x 72	256Mbit	32M x 8	18/2/4	13/2/10
512MB	64M x 72	512Mbit	64M x 8	9/1/4	13/2/11
1GB	128M x 72	256Mbit	64M x 4	36/2/4	13/2/11
1GB	128M x 72	512Mbit	64M x 8	18/2/4	13/2/11
1GB	128M x 72	512Mbit	128M x 4	18/1/4	13/2/12
2GB	256M x 72	512Mbit	128M x 4	36/2/4	13/2/12

3.2.2 MCH Memory Controller Hub

The E7501 MCH North Bridge (MCH) is a 1005 ball FC-BGA device and uses the proven components of previous generations. In addition, the MCH incorporates a Hub Interface (HI) 2.0. The HI 2.0 interface enables the MCH to directly interface with the P64H2. The MCH also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The MCH integrates three main functions:

- An integrated high performance main memory subsystem

- An HI 2.0 bus interface that provides a high-performance data flow path between the host bus and the I/O subsystem
- A HI 1.5 bus which provides an interface to the ICH3-S (South Bridge).

Other features provided by the MCH include the following:

- Full support of ECC on the memory bus
- Full support of Intel® Single Device Data Correction (SDDC) on the memory interface with x4 DIMMs
- Twelve deep in-order queue
- Full support of registered DDR266 ECC DIMMs
- Support for 12 GB of DDR memory
- Memory scrubbing

3.2.3 P64H2 I/O Bridge

The P64H2 is a 567-ball FCBGA device and provides an integrated I/O bridge that provides a high-performance data flow path between the HI 2.0 and the 64-bit I/O subsystem. This subsystem supports two peer 64-bit PCI-X segments. Because it has two PCI interfaces, the P64H2 can provide large and efficient I/O configurations. The P64H2 functions as the bridge between the HI 2.0 and the two 64-bit PCI-X I/O segments. The HI 2.0 interface can support 1 GB/s of data bandwidth.

Note: BIOS is responsible for setting the mode (PCI or PCI-X) and bus speed for the two segments provided by the P64H2 PCI-X I/O Bridge. The actual bus mode/speed will be determined by the least capable card installed on that bus.

3.2.3.1 PCI Bus P64H2 (PCI-X I/O Bridge) Segment-B I/O Subsystem

P64H2 Segment-B supports the following embedded devices and connectors:

- Two 64-bit/100MHz, 3.3V keyed PCI-X slots (PCI-X slots 2 and 3)
- One Adaptec* 7902 dual-channel Ultra-320 SCSI controller
- PCI slot 2 supports Zero Channel RAID (ZCR) or M-ROMB that allows the on-board SCSI controller to be “hidden” from the system and used by the RAID processor on the add-in card.
- Full length PCI card support

3.2.3.2 PCI Bus P64H2 (PCI-X I/O Bridge) Segment-C I/O Subsystem

P64H2 Segment-C supports the following connectors:

- One 64-bit/133MHz 3.3V keyed PCI-X slot (PCI-X slot 1)
- One Intel® 82546EB dual-channel gigabit Ethernet controller
- Full length PCI card support

3.2.4 ICH3-S I/O Controller Hub (South Bridge)

The ICH3-S South Bridge is a multi-function PCI device, housed in a 421-pin BGA device, providing a PCI-to-LPC bridge, a PCI IDE interface, a PCI USB controller, and a power management controller. Each function within the ICH3-S has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the server board SE7501HG2, the primary role of the ICH3-S is to provide the gateway to all PC-compatible I/O devices and features. The SE7501HG2 uses the following ICH3-S features:

- PCI bus interface
- LPC bus interface
- IDE interface, with Ultra DMA 100 capability
- Universal Serial Bus (USB) interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- General purpose I/O
- System RTC

The following are the descriptions of how each supported feature is used on the server board SE7501HG2.

3.2.4.1 PCI Bus P32-A I/O Subsystem

The ICH3-S provides a legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface.

P32-A supports the following embedded devices:

- An ATI* RAGE XL video controller with 3D/2D graphics accelerator
- Three 32-bit/33 MHz, 5V keyed PCI slots (PCI Slot 4, 5 and 6)

3.2.4.2 PCI Bus Master IDE Interface

The ICH3-S acts as a PCI-based Ultra DMA/100 IDE controller that supports programmed I/O transfers and bus master IDE transfers. The ICH3-S supports two IDE channels, supporting two drives each (drives 0 and 1) through two 40-pin (2x20) IDE connectors. The SE7501HG2 IDE interface supports Ultra DMA/100 Synchronous DMA Mode transfers on each channel.

3.2.4.3 USB Interface

The ICH3-S contains three USB1.1 controllers for up to six USB ports. The USB controller moves data between main memory and USB connectors. All six ports function identically and with the same bandwidth.

The SE7501HG2 provides three external USB ports on the ATX I/O panel area of the server board. The fourth and fifth USB ports are optional and can be accessed by special cabling (not bundled with product) from the internal 9-pin connector located on the baseboard to external USB ports located either in the front or the rear of a given chassis.

3.2.4.4 Compatibility Interrupt Control

The ICH3-S provides the functionality of two 82C59 PIC devices for ISA-compatible legacy AT interrupt handling.

3.2.4.5 APIC

The ICH3-S integrates an IO APIC that is used to distribute 24 PCI interrupts.

3.2.4.6 General Purpose Input and Output Pins (GPIO)

The ICH3-S provides a number of general purpose input and output pins. Many of these pins have alternate functions, and thus all are not available. The following table lists the GPI and GPO pins used on the SE7501HG2 baseboard and gives a brief description of their function.

Table 5. ICH-3 GPIO Usage Table

Pin #	Signal Name	Description
D4	P64H_RASERR_L	Reliability, Availability, Serviceability Error
B6	ICH3_RST_VIDEO_L	Disable Video Controller
B3	ICH3_RST_SCSI_L	Disable SCSI Controller
Y3	ICH3_RST_NIC1_L	Disable Network Interface Controller #1
Y2	SIO_PME_L	PME# from SIO
V2	IDE_CBL_DET_P	Primary IDE Bus 80 Conductor Cabel Detect
V4	BMC_IRQ_SMI_L	
F21	ZZ_MFG_MODE	detect Manufacturing Mode for test
G19	ZZ_PASSWORD_CLR_L	Password Clear
E22	ZZ_BIOS_RCVR_L	Enable Recovery Boot
E21	ZZ_BB_ID0	Baseboard ID 0 - Used to identify revision of board
H21	ZZ_BB_ID1	Baseboard ID 1 - Used to identify revision of board
G23	ZZ_BB_ID2	Baseboard ID 2 - Used to identify revision of board
G21	ZZ_ICH3_FRB3_TIMER_HALT_L	ICH3 FRB3 Timer Halt Output
D23	ZZ_CMOS_CLR_L	CMOS clear
E23	IDE_CBL_DET_S	Secondary IDE Bus 80 Conductor Cabel Detect

3.2.4.7 Power Management

One of the embedded functions of the ICH3-S is a power management controller. The server board SE7501HG2 uses this to implement ACPI-compliant power management features. The SE7501HG2 supports sleep states S0, S1, S4, and S5.

3.2.4.8 Real-time Clock

The SE7501HG2 server board uses the RTC function provided by ICH3-S.

3.3 Super I/O

The National Semiconductor* PC87417 Super I/O device contains the system RTC, all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The server board SE7501HG2 supports the following features:

- GPIOs
- Two serial ports
- Parallel Port
- Floppy
- Keyboard and mouse through PS/2 connectors
- Wake event control

3.3.1 GPIOs

The National Semiconductor* PC87417 Super I/O provides a number of general-purpose input/output pins that the server board SE7501HG2 utilizes. The following table identifies the pin, the signal name used in the schematic and a brief description of each pin's usage.

Table 6. Super I/O GPIO Usage Table

Pin #	Signal Name	Description
49	ROMB_PRESENT_L	ROMB Present in add-in connector
35	BMC_SLP_BTN_L	Sleep Button from BMC
38	SIO_PME_L	PME# to ICH3
124	SIO_EMP_INUSE	Enable EMP port
20	PA_PCIXCAP	PCI-X Capability
21	PB_PCIXCAP	PCI-X Capability
50	PA_PME_L	PME# from P64H2-channel A
51	FP_PWR_LED_L	Front Panel Power Indicator
52	PB_PME_L	PME# from P64H2-channel B
53	BMC_SCI_L	SCI signal

3.3.2 Serial Ports

The server board SE7501HG2 provides two serial ports, one DB9 connector (J8A1) is located on the rear I/O to provide Serial Port A and an internal 9-pin header (J1B1) provides Serial Port B. See Section 9.6.7 for the connector pin-outs.

3.3.3 Parallel Port

The server board SE7501HG2 provides one parallel port via a DB-25 connector (J7A2) located on the rear ATX I/O. See Section 9.6.8 for the connector pin-outs.

3.3.4 Floppy Disk Controller

The floppy disk controller (FDC) in the SIO (Super I/O) is functionally compatible with floppy disk controllers in the DP8473 and N844077. All FDC functions are integrated into the SIO, including an analog data separator and 16-byte FIFO. The SE7501HG2 provides a SSI compliant 36-pin connector (J4J3).

3.3.5 Keyboard and Mouse

Two PS/2 ports are provided for keyboard and mouse and share a common housing (J9A1). The top one is labeled “mouse” and the bottom one is labeled “keyboard,” although the board set supports swapping these connections.

3.3.6 Wake-up Control

The Super I/O contains functionality that allows various events to control the power-on and power-off the system.

3.3.7 BIOS Flash

The server board SE7501HG2 incorporates an Intel® 3-Volt Advanced+ Boot Block 28F320C3 Flash memory component. The 28F320C3 is a high-performance 32-megabit memory component that provides 2048K x 16 of BIOS and non-volatile storage space. The flash device is connected through the X-bus from the SIO.

4. Configuration and Initialization

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration.

4.1 Memory Space

At the highest level, the Intel® Xeon™ processor address space is divided into three regions, as shown in the following figure. Each region contains sub-regions as described in following sections. Attributes can be independently assigned to regions and sub-regions using the SE7501HG2 registers.

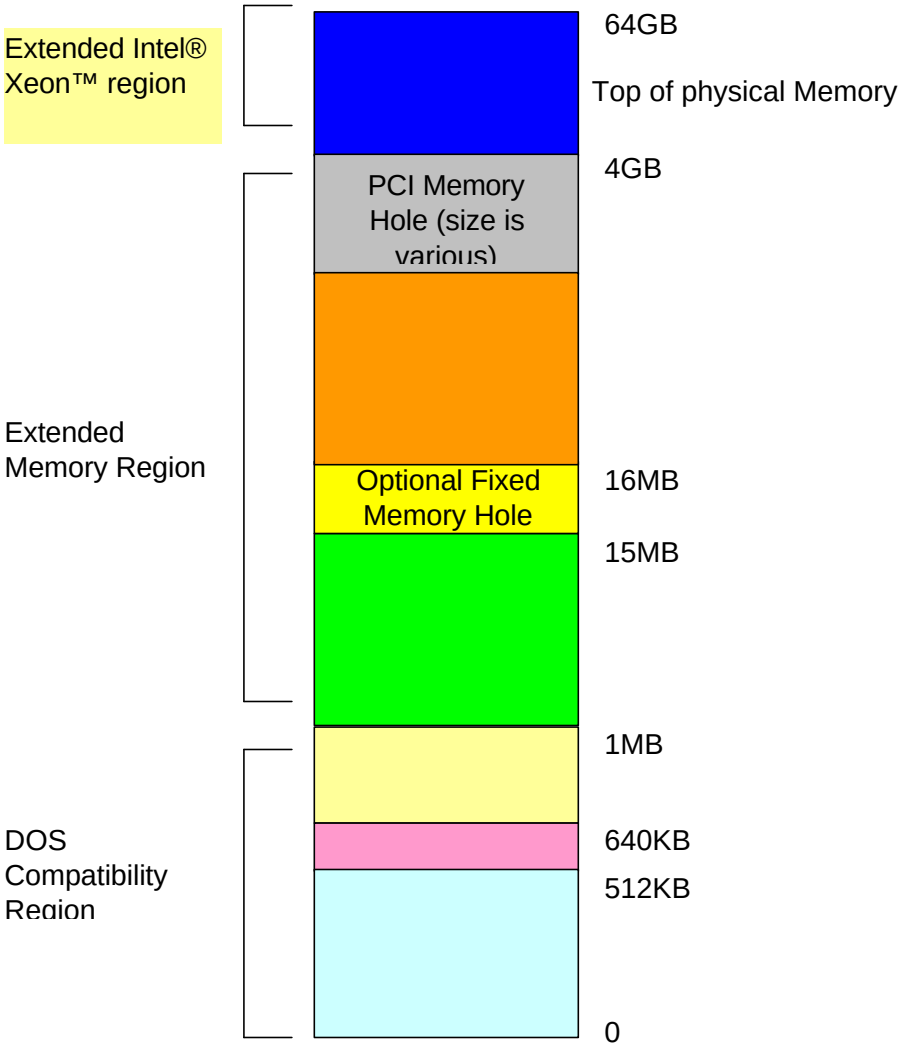


Figure 4. Intel® Xeon™ Processor Memory Address Space

4.1.1 DOS Compatibility Region

The first region of memory below 1 MB was defined for early PCs, and must be maintained for compatibility reasons. The region is divided into sub-regions as shown in the following figure.

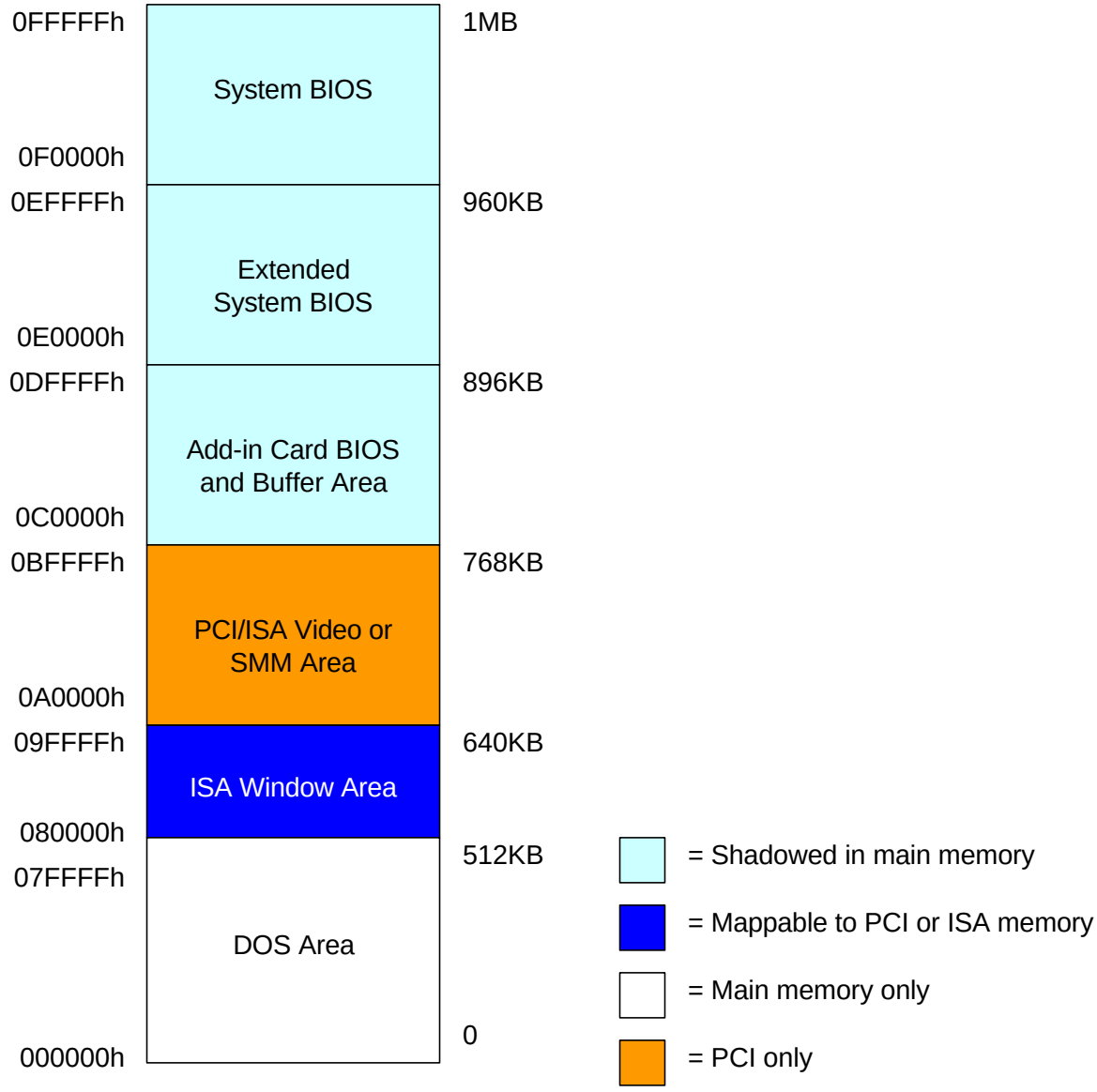


Figure 5. DOS Compatibility Region

4.1.1.1 DOS Area

The DOS region is 512 KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

4.1.1.2 ISA Window Memory

The ISA Window Memory is 128 KB between the addresses of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

4.1.1.3 Video or SMM Memory

The 128 KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space.

4.1.1.4 Add-in Card BIOS and Buffer Area

The 128 KB region between addresses 0C0000h to 0DFFFFh is divided into eight segments of 16 KB segments mapped to ISA memory space, each with programmable attributes, for expansion cards buffers. Historically, the 32 KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on the video card.

4.1.1.5 Extended System BIOS

This 64 KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16 KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically this area is used for RAM or ROM. This region can also be used for extended SMM space.

4.1.1.6 System BIOS

The 64 KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally read/write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory. This region can also be used for extended SMM space.

4.1.2 Extended Memory

Extended memory on SE7501HG2 is defined as all address space greater than 1MB. The extended memory region covers 4GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

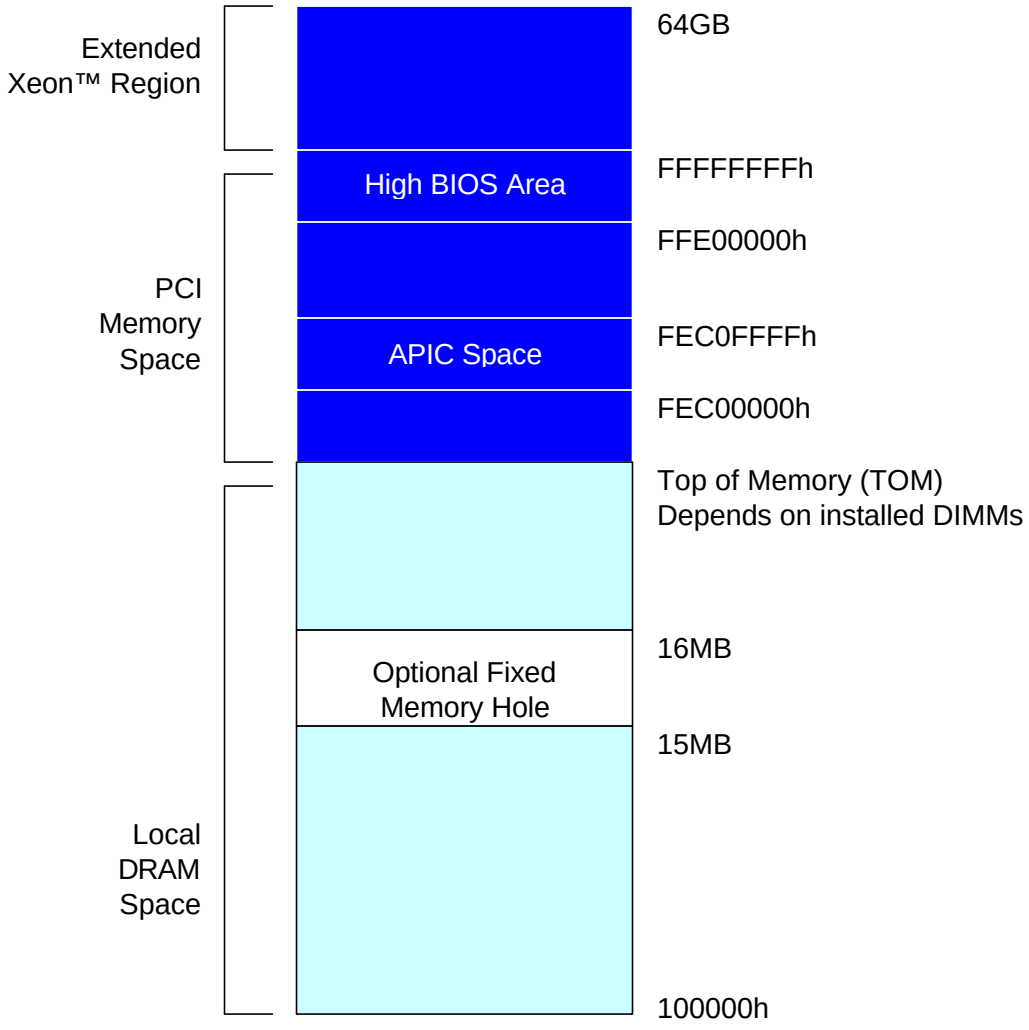


Figure 6. Extended Memory Map

4.1.2.1 Main Memory

All installed memory greater than 1 MB is mapped to local main memory, up to top of physical memory, which is located at 12 GB. Memory between 1 MB to 15 MB is considered to be standard ISA extended memory. 1 MB of memory starting at 15 MB can be optionally mapped to the PCI bus memory space.

The remainder of this space, up to 12 GB, is always mapped to main memory, unless Extended SMRAM is used, which limits the top of memory to 256 MB.

4.1.2.2 PCI Memory Space

Memory addresses below the 4 GB range are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory. The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers.

4.1.2.3 High BIOS

The top 2 MB of Extended Memory is reserved for the system BIOS, extended BIOS for PCI devices, and A20 aliasing by the system BIOS. The Intel® Xeon™ processor begins executing from the high BIOS region after reset.

4.1.2.4 I/O APIC Configuration Space

A 64 KB block located 20 MB below 4 GB (0FEC00000 to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0h from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FEC0c000h where x is the I/O APIC unit (0 through F).

4.1.2.5 Extended Intel® Xeon™ Processor Region (above 4GB)

An Intel® Xeon™ processor-based system can have up to 64 GB of addressable memory. The BIOS uses the Extended Addressing mechanism to use the address ranges.

4.1.3 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into main memory. Typically this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originated from the PCI bus or ISA masters and targeted at shadowed memory block will not appear on the processor’s bus.

4.1.4 System Management Mode Handling

The Intel® E7501 MCH supports System Management Mode (SMM) operation in standard (compatible) mode. System Management RAM (SMRAM) provides code and data storage space for the SMI_L handler code, and is made visible to the processor only on entry to SMM, or other conditions, which can be configured using Intel® E7501 PCI registers. Compatible SMRAM is located in main memory below the 1 MB boundary at addresses 000A0000h through 000B0000h. The region is non-cacheable.

4.2 I/O Map

The SE7501HG2 allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including the ICH3-S, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On the server board SE7501HG2, the ICH3-S provides the bridge to ISA functions through the LPC bus.

4.3 Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the PCI Local Bus Specification.

If dual processors are used, only the processor designated as the BSP should perform PCI configuration space accesses. Precautions should be taken to guarantee that only one processor performs system configuration.

Two DWORD I/O registers in the Intel chipset are used for the configuration space register access:

- CONFIG_ADDRESS (I/O address 0CF8h)
- CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written to with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full DWORD reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the Intel chipset. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

4.3.1 CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bits [6::2] select a specific register in the configuration space of the selected device or function on the bus.

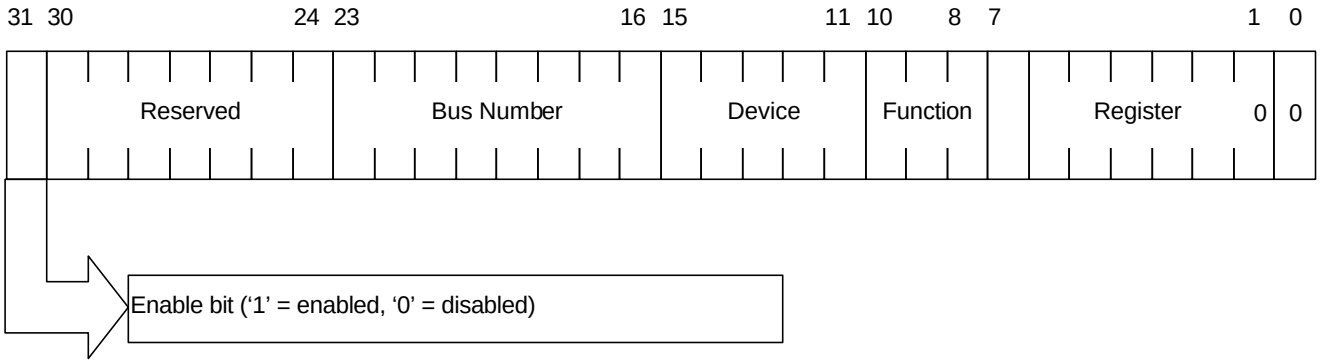


Figure 7. CONFIG_ADDRESS Register

4.3.1.1 Bus Number

PCI configuration space protocol requires that all PCI buses in a system be assigned a Bus Number. Bus Numbers must be assigned in ascending order within hierarchical buses. Each PCI Bridge has registers containing its PCI Bus Number and subordinate PCI Bus Number, which must be loaded by Postcode. The Subordinate PCI Bus Number is the bus number of the last hierarchical PCI bus under the current bridge. The PCI Bus Number and the Subordinate PCI Bus Number are the same in the last hierarchical bridge.

4.3.1.2 Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD [31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 7. PCI Device IDs

Device Description	Bus # (segment)	Device Number (Hex)
North Bridge (MCH)	0	00
ICH3 P2P Bridge	0	1E
ICH3 USB	0	1D
ICH3 IDE	0	1F
Video	1	0C
P64H2 P2P Bridge A	2	1F
P64H2 P2P Bridge B	2	1D
Dual Gigabit NIC	4 (P64-C)	05
Slot 1 (PCI-X 64/133)	4 (P64-C)	02
Slot 2 (PCI-X 64/100)	3 (P64-B)	01
Slot 3 (PCI-X 64/100)	3 (P64-B)	02
Slot 4 (PCI 32/33)	1 (P64-A)	0A
Slot 5 (PCI 32/33)	1 (P32-A)	09
Slot 6 (PCI 32/33)	1 (P32-A)	08
SCSI	3 (P64-B)	04

4.4 Hardware Initialization

An Intel® Xeon™ processor system based on the Intel® E7501 MCH is initialized in the following manner.

1. When power is applied, after receiving RST_PWRGD_PS from the power supply, the BMC provides resets using the RST_P6_PWRGOOD signal. The ICH3-S asserts RST_PCIRST_L to MCH, P64H2, and other PCI devices. MCH then asserts RST_CPURST_L to reset the processor(s).
2. The MCH is initialized, with its internal registers set to default values. Before RST_CPURST_L is de-asserted, the MCH asserts BREQ0_L. Processor(s) in the system determine which host bus agents they are, Agent 0 or Agent 1, based on whether BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.
3. After the processor(s) in the system determines which processor will be the BSP, the non-BSP processor becomes an application processor and idles, waiting for a Startup Inter Processor Interrupt (SIPI).
4. The BSP begins by fetching the first instruction from the reset vector.
5. The Intel® E7501 chipset registers are updated to reflect memory configuration. DIMM is sized and initialized.
6. All PCI and ISA I/O subsystems are initialized and prepared for booting.

5. Clock Generation and Distribution

All buses on the SE7501HG2 baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 133 MHz at 3.3 V logic levels. For processors, MCH, and ITP port
- 66 MHz at 3.3 V logic levels: For MCH, ICH3-S and P64H2 clock
- 33 MHz at 3.3 V logic levels: For ICH3-S, BMC, Video, SIO, and PCI32/33 Slots
- 48 MHz at 3.3 V logic levels: ICH3-S and SIO
- 14 MHz at 3.3V logic levels: ICH3-S, SIO, and Video controller

The synchronous clock sources on the SE7501HG2 baseboard are:

- 133/100-MHz clock for PCI-X Slot, SCSI, and Intel® 82546EB Dual Gigabit NIC
- 133-MHz host clock for processors, MCH, memory DIMMs, and the ITP
- 66-MHz clock for MCH, ICH, and P64H2
- 48-MHz clock for ICH and SIO
- 33-MHz clock for ICH, BMC, video, SIO, and PCI32/33 slots
- 14-MHz clock for ICH and video

For information on processor clock generation, see the *CK408B Synthesizer/Driver Specification*.

The SE7501HG2 baseboard also provides asynchronous clock generators:

- 80-MHz clock for the embedded SCSI controller
- 25-MHz clocks for the embedded network interface controllers
- 32.768-KHz clock for the ICH RTC
- 40-MHz clock for the BMC

The following figure illustrates clock generation and distribution on the server board SE7501HG2.

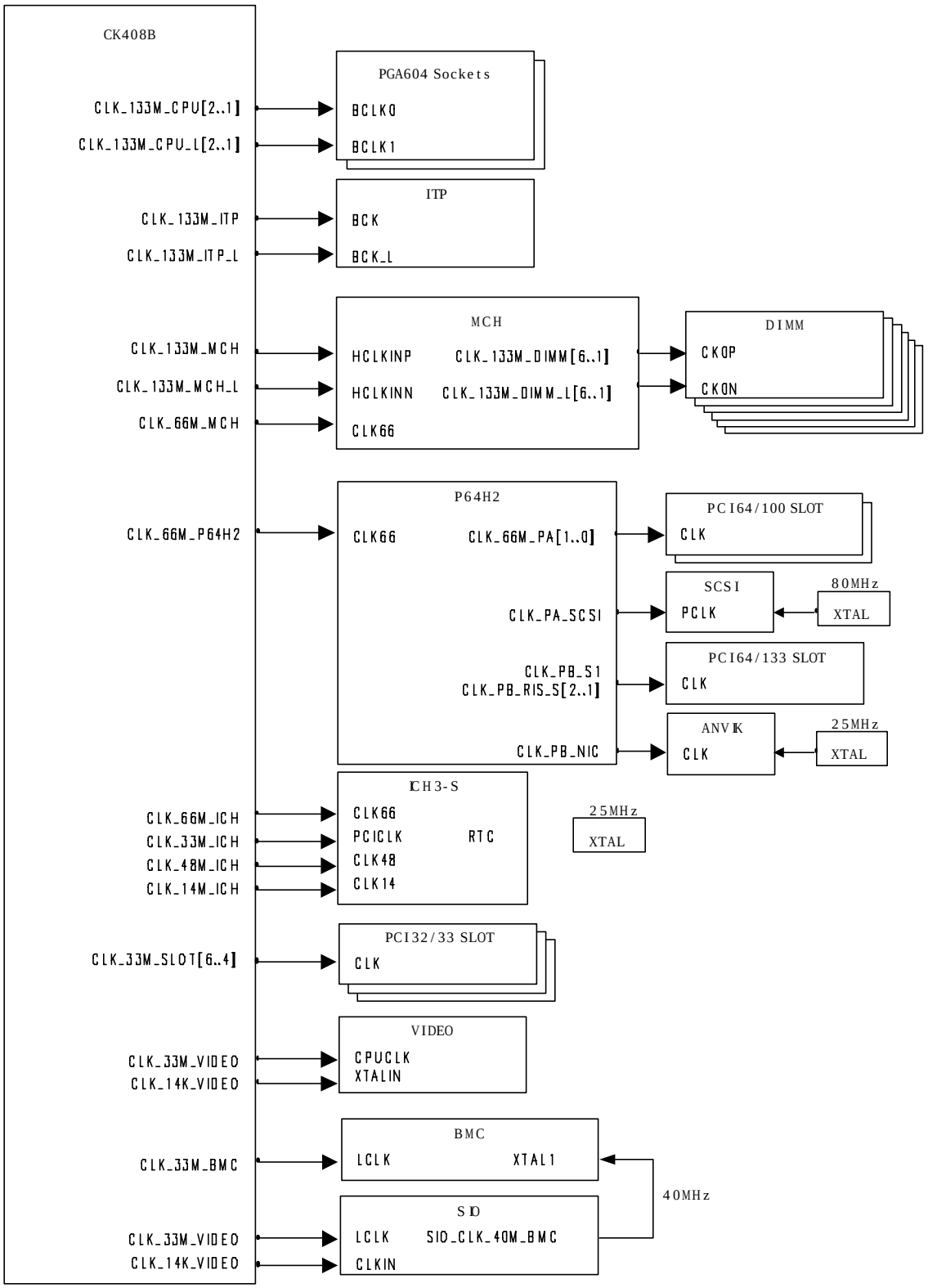


Figure 8. Intel® Server Board SE7501HG2 Clock Distribution

6. PCI I/O Subsystem

6.1 PCI Subsystem

The primary I/O bus for the server board SE7501HG2 is PCI, with three independent PCI bus segments. The PCI buses comply with the *PCI Local Bus Specification*, Rev 2.2 and with the *PCI-X Specification*, Rev 1.0. The P32-A bus segment is directed through the ICH while the two 64-bit segments, P64-B and P64-C, are directed through the P64H2. The following table lists the characteristics of the three PCI bus segments.

Table 8. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Riser Slots
P32-A	5 V	32 bits	33 MHz	Peer Bus	Supports Full-length cards, 5V bus
P64-B	3.3 V	64 bits	100/66 MHz	Peer Bus	Supports Full-length cards, 3.3V bus
P64-C	3.3 V	64 bits	133/100/66 MHz	Peer Bus	Supports Full-length cards, 3.3V bus

6.1.1 P32-A: 32-bit, 33-MHz PCI Subsystem

All 32-bit, 33-MHz PCI I/O for the server board SE7501HG2 is directed through the ICH3-S. The 32-bit, 33-MHz PCI segment created by the ICH is known as the P32-A segment. The P32-A segment supports the following embedded devices and connectors:

- 2D/3D Graphics Accelerator: ATI* RAGE XL Video Controller
- Three 32-bit/33MHz PCI Slots (PCI Slot 4, Slot 5 and Slot 6)

Each of the embedded devices listed above will be allocated a GPIO to disable the device. The PCI segment will support full-length, full-height PCI cards as well as half-length PCI cards.

6.1.1.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD [31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-A devices, and the corresponding device description.

Table 9. P32-A Configuration IDs

IDSEL Value	Device
24	PCI32/33 Slot4
25	PCI32/33 Slot5
26	PCI32/33 Slot6
28	ATI RAGE* XL video controller

6.1.1.2 P32-A Arbitration

P32-A supports five PCI masters (ATI RAGE XL, the ICH3-S, three PCI 32-bit slots). All PCI masters must arbitrate for PCI access, using resources supplied by the ICH3-S. The host bridge PCI interface (ICH3-S) arbitration lines REQx* and GNTx* are special cases in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 10. P32-A Arbitration Connections

Baseboard Signals	Device
PCI_REQ_L3/PCI_GNT_L3	PCI32/33 Slot4
PCI_REQ_L2/PCI_GNT_L2	PCI32/33 Slot5
PCI_REQ_L1/PCI_GNT_L1	PCI32/33 Slot5
PCI_REQ_L0/PCI_GNT_L0	ATI RAGE XL video controller

6.1.2 P64-B: 64-bit, 100/66-MHz PCI-X Subsystem

The 64-bit, 100/66-MHz PCI-X bus segment is directed through the P64H2. This PCI segment, P64-B, provides the following embedded devices and connectors:

- Adaptec* AIC7902 Dual Channel U320 SCSI controller
- Two 64-bit/100MHz PCI-X Slots (PCI-X Slot 2 and Slot 3).

Note: Slot 2 supports ZCR (Zero Channel RAID).

The PCI segment supports full-length, full-height PCI cards as well as half-length PCI cards.

6.1.2.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD [31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P64-B devices, and the corresponding device description.

Table 11. P64-B Configuration IDs

IDSEL Value	Device
20	On-board SCSI controller
17	PCI-X Slot2
18	PCI-X Slot3

6.1.2.2 P64-B Arbitration

P64-B supports four PCI masters (AIC7902, P64H2, and two PCI 64-bit slots). All PCI masters must arbitrate for PCI access using resources supplied by the P64H2. The host bridge PCI interface (P64H2) arbitration lines REQx* and GNTx* are special cases in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 12. P64-B Arbitration Connections

Baseboard Signals	Device
PA_REQ_L0/PA_GNT_L0	On-board SCSI controller
PA_REQ_L2/PA_GNT_L2	PCI-X Slot2
PA_REQ_L1/PA_GNT_L1	PCI-X Slot3

6.1.2.3 Zero Channel RAID (ZCR) Capable Slot 2

The server board SE7501HG2 is capable of supporting either of two zero channel RAID controllers, the Intel® SRCZCR RAID adapter and the Adaptec* ASR-2010S RAID adapter. These ZCR cards are supported only in slot 2 on the P64-B segment.

The ZCR add-in cards leverage the on-board SCSI controller along with their own built-in intelligence to provide a complete RAID controller subsystem on-board. The baseboard uses an implementation commonly referred to as RAID I/O Steering (RAIDIOS) specification version 1.0 to support this feature.

If either of these supported RAID cards are installed, then the SCSI interrupts are routed to the RAID adapter instead of to the PCI interrupt controller. In addition, the IDSEL of the SCSI controller is not driven to the controller and thus will not respond as an on-board device. The host-based I/O device is effectively hidden from the system.

Note: ZCR cards and RAID I/O Steering (RAIDIOS) are only supported in PCI slot 2.

6.1.3 P64-C: 64-bit, 133/100/66-MHz PCI-X Subsystem

The 64-bit, 133/100/66-MHz PCI-X bus segment is directed through the P64H2. This PCI segment, P64-C, provides the following embedded devices and connectors:

- One 64-bit/133MHz PCI-X Slot (PCI-X Slot 1)
- Dual Channel Gigabit Ethernet Controller (Intel® 82546EB)

6.1.3.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD [31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P64H2 segment-C devices, and the corresponding device description.

Table 13. P64-C Configuration IDs

IDSEL Value	Device
21	Intel® 82546EB Dual Gigabit NIC
18	PCI-X Slot1

6.1.3.2 P64-C Arbitration

P64-C supports three PCI masters (P64H, 82546EB Dual Gigabit NIC, and PCI-X slot). All PCI masters must arbitrate for PCI access, using resources supplied by the P64H2. The host bridge PCI interface arbitration lines REQx* and GNTx* are special cases in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 14. P64-C Arbitration Connections

Baseboard Signals	Device
PA_REQ_L4/P64_S_GNT4	82546EB Dual Gigabit NIC
PA_REQ_L1/P64_S_GNT1	PCI-X Slot1

6.2 Ultra 320 SCSI

The server board SE7501HG2 provides an embedded dual-channel SCSI bus through the use of the Adaptec* AIC-7902 SCSI controller, which supports up to Ultra 320 SCSI transfers. The AIC-7902 controller contains single SCSI controller that has a single 64-bit, 133-MHz PCI-X bus master interface as a multi-function device, packaged in a 388-pin BGA.

Internally, the controller is capable of operations using LVD SCSI providing 80 MB/sec (Ultra 2), 160 MB/sec (Ultra 160), or 320 MB/sec (Ultra 320). The controller has its own set of PCI configuration registers and PCI I/O registers. The server board SE7501HG2 supports disabling of the on-board SCSI controller through the BIOS setup menu.

The server board SE7501HG2 provides active terminators, termination voltage, a reset-able fuse, and a protection diode for SCSI channel. By design, the on-board termination will be disabled by BIOS when the SCSI cable is detected. The SCSI channel has two 68-pin connector interfaces.

6.3 Onboard RAID support

The SE7501HG2 incorporates the Adaptec* HostRAID and RAI*DSelect* utility to provide convenient and reliable entry-level RAID support for SCSI devices utilizing the onboard 7902 SCSI subsystem.

The Adaptec RAI*DSelect* Utility is a BIOS-based array configuration utility (included with HostRAID) used for HostRAID array management. The utility is entered by pressing <CTRL-A> during POST. The Adaptec RAI*DSelect* Utility is required to create, delete or view the status of HostRAID arrays on the SE7501HG2 system. This section is intended to introduce the user to the capabilities of the onboard HostRAID subsystem. For a comprehensive explanation of HostRAID features and utility usage, please refer to the Adaptec HostRAID Users Guide.

HostRAID offers the following advanced features:

- Bootable array support
- Support for separate RAID arrays per channel
- Support of Hot Swap drives
- Support for Auto Rebuild (if a spare is dedicated to the volume)
- Support for Auto Verify
- Support for all major SCSI peripherals
- Support for Ultra320 products
- Complete RAID configuration and management utility in the BIOS
- Provides graphical RAID management software

The following HostRAID configurations and related restrictions are available:

- **RAID-0**: (Stripe) One RAID 0 with 3 or 4 drives or Two RAID 0s with two drives each. Minimum 2 drives, maximum 4 drives. Two RAID-0 volumes can be configured per channel, 4 drives total per channel.
- **RAID-1**: (Mirror) Two RAID 1s with one spare each. Minimum 2 drives, maximum 4 drives with 1 spare per mirrored volume. RAID-1 volumes can only consist of 2 drives with the option of adding 1 spare; two volumes can be configured per channel
- **RAID-10**: Is not available with the current version of the utility. (This option, although it may be displayed, will remain grayed out.)
- **SPARE**: Maximum one Spare per RAID-1 volume. Two spares maximum per channel.
- **SPANNING**: The Spanning of RAID volumes or spares across channels is not supported.

Note: SCSI Channel ‘B’ is the Master, HostRAID support must be enabled on this channel for HostRAID to be recognized on re-boot. Channel A can also be RAID enabled but will not be recognized on re-boot if channel ‘B’ is not enabled. You must have at least two hard drives to create an array. If the hard drive you select is already part of a RAID volume, it will not be available for selection.

6.4 Video Controller

The server board SE7501HG2 provides an ATI RAGE XL PCI graphics accelerator, with 8 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI* RAGE XL chip contains an SVGA video controller, a clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2Mx32 SDRAM chip provides 8 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors with up to 100 Hz vertical refresh rate.

The server board SE7501HG2 provides a standard 15-pin VGA connector and supports disabling the on-board video through the BIOS setup menu or when a video card is installed in any of the PCI slots.

6.4.1 Video Modes

The ATI RAGE XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD. The table specifies the minimum memory requirement for various display resolution, refresh rates and color depths.

Table 15. Video Modes

2D Mode	Refresh Rate (Hz)	Intel® Server Board SE7501HG2 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	**Refresh Rate (Hz)**	**SE7501HG2 3D Video Mode Support with Z Buffer Enabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	**Refresh Rate (Hz)**	**SE7501HG2 3D Video Mode Support with Z Buffer Disabled**			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

6.4.2 Video Memory Interface

The memory controller subsystem of the RAGE XL arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The SE7501HG2 supports an 8 MB (512Kx32bitx4 banks) SDRAM device for video memory. The following table shows the video memory interface signals:

Table 16. Video Memory Interface

Signal Name	I/O Type	Description
CAS#	O	Column Address Select
CKE	O	Clock Enable for Memory
CS#[1..0]	O	Chip Select for Memory
DQM[7..0]	O	Memory Data Byte Mask
DSF	O	Memory Special Function Enable
HCLK	O	Memory Clock
[11..0]	O	Memory Address Bus
MD[31..0]	I/O	Memory Data Bus
RAS#	O	Row Address Select
WE#	O	Write Enable

6.4.3 Host Bus Interface

The ATI RAGE XL supports a PCI 33 MHz bus. The following diagram shows the signals for the PCI interface:

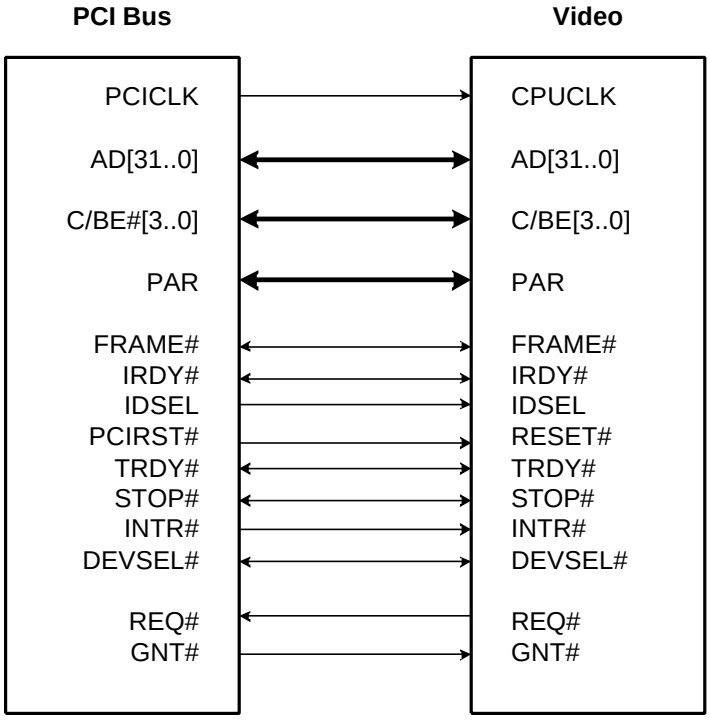


Figure 9. Video Controller PCI Bus Interface

6.5 Network Interface Controller (NIC)

The server board SE7501HG2 supports a dual 10Base-T / 100Base-TX /1000Base-TX network interface controller that is based on the Intel® 82546EB NIC. The 82546EB is highly integrated PCI-X Gigabit Ethernet controller in the 364 PBGA package. The 82546EB architecture is a derivative of the 82543, 82543, and 82544 designs. The 82546EB takes the MAC functionality and integrated copper PHY from its processors, and adds SMBus-based manageability and integrated ASF controller functionality to the MAC. The 82546EB features this architecture in an integrated dual-port solution comprised of two distinct MAC/PHY instances. The server board SE7501HG2 supports disabling the NIC controller using the BIOS setup menu.

The 82546EB supports the following features:

- Glue less 32-bit PCI, Card Bus master interface (Direct Drive of Bus), compatible with *PCI local Bus Specification, Revision 2.2 and PCI-X 1.0a compliant Host interface.*
- Integrated IEEE 802.3ab10Base-T, 100Base-TX, 1000Base-TX compatible copper PHY
- IEEE 820.3ab auto-negotiation support
- Full duplex support at 10 Mbps, 100 Mbps, and 1000 Mbps operation
- Integrated UNDI ROM support
- MDI/MDI-X and HWI support
- Low power +3.3 V device

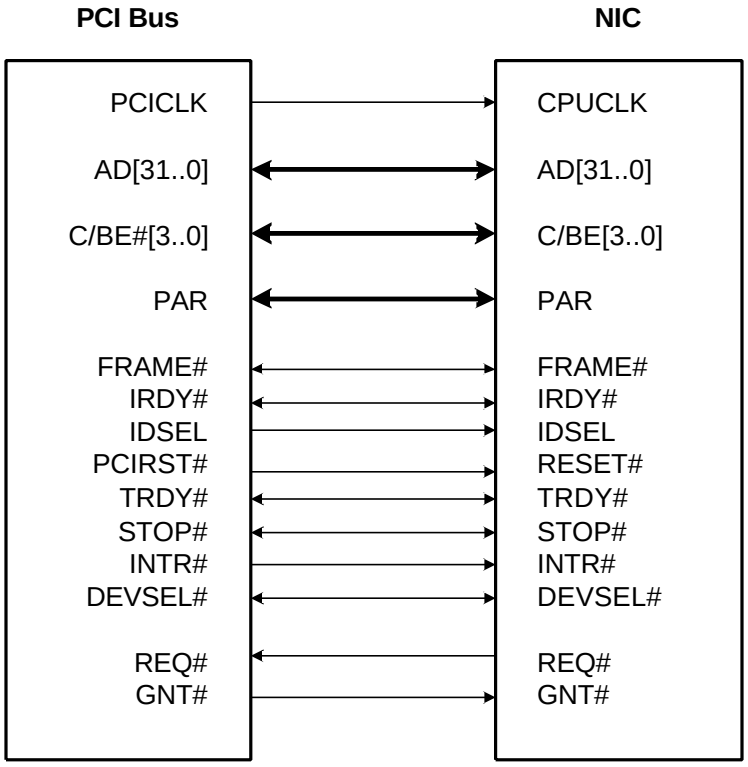


Figure 10. NIC Controller PCI Bus Interface

6.5.1 NIC Connector and Status LEDs

The 82546EB drives two LEDs on each channel located on the network interface connector (connector in the left side when looking from the back of the ATX I/O rear panel). The link/activity LED to the right of the connector indicates network connection when on, and Transmit/Receive activity when blinking. The speed LED (to the left of the connector) indicates 1000-Mbps operations when yellow, 100-Mbps operations when green, and 10-Mbps when off.

Table 17. NIC Status LED

LED Color	LED State	NIC 2 State
Green/Orange (left)	Off	10-Mbps
	Green	100-Mbps
	Yellow	1000-Mbps
Green (right)	On	On
	Blinking	Transmit / Receive activity

6.6 Interrupt Routing

The SE7501HG2 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the ICH3-S and the P64H2.

6.6.1 Legacy Interrupt Routing

For PC-compatible mode, the ICH3-S provides two 82C59 AT legacy compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing.

6.6.1.1 Legacy Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the server board SE7501HG2. The actual interrupt map is defined using configuration registers in the ICH3-S.

Table 18. Interrupt Mapping

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.
IRQ1	Keyboard interrupt.
IRQ3	Serial port A or B interrupt from SIO device, user-configurable.
IRQ4	Serial port A or B interrupt from SIO device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	Parallel Port
IRQ8_L	Active low RTC interrupt.

ISA Interrupt	Description
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	
SMI*	System Management Interrupt. General purpose indicator sourced by the ICH3-S and BMC to the processors.
SCI*	System Control Interrupt. Used by system to change sleep states and other system level type functions.

6.6.1.2 Serialized IRQ Support

The server board SE7501HG2 supports a serialized interrupt delivery mechanism. Serialized IRQs (SERIRQs) consist of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

The following figure shows how the interrupts from the embedded devices and the PCI slots are connected.

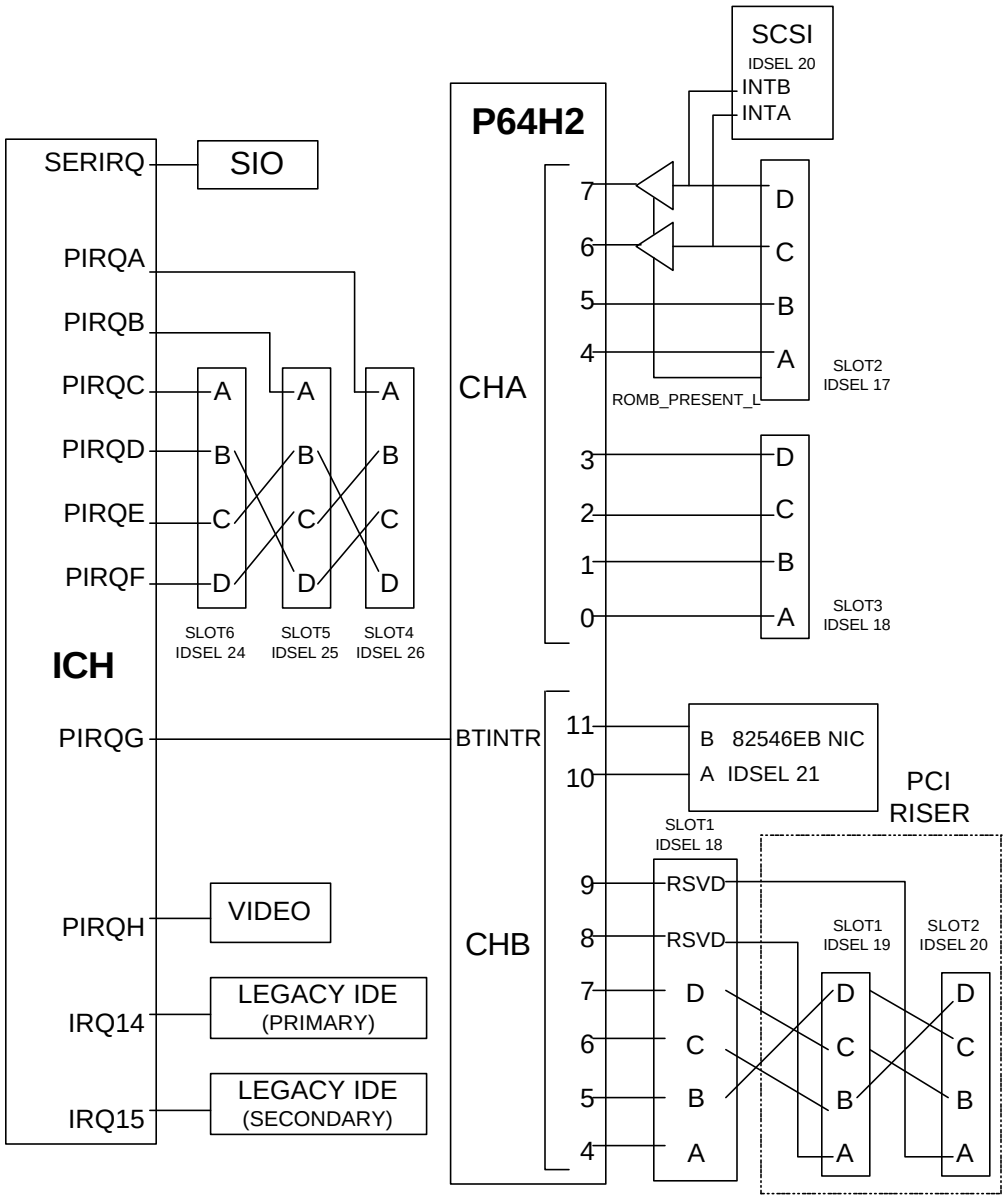


Figure 11. Intel® Server Board SE7501HG2 Interrupt Routing Diagram

7. Server Management

The SE7501HG2 server management features are implemented using the Sahalee server board management controller chip. The Sahalee BMC is an ASIC packaged in a 156-pin BGA that contains a 32-bit RISC processor core and associated peripherals. The following diagram illustrates the SE7501HG2 server management architecture.

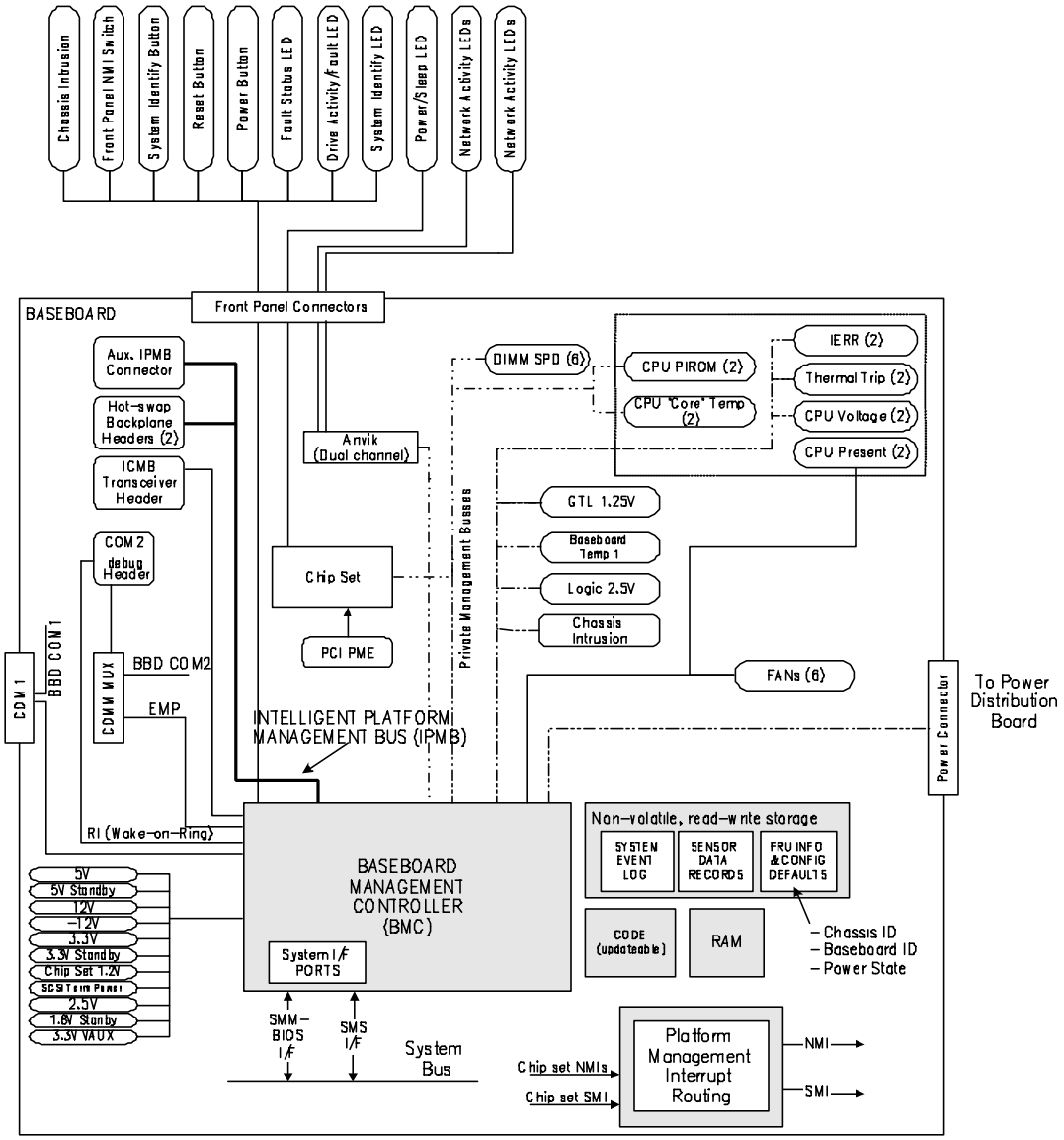


Figure 12. Intel® Server Board SE7501HG2 Sahalee BMC Block Diagram

7.1 Intel® Server Management v5.5 (ISM) Overview

A brief introduction to Intel® Server Management (ISM) is provided in this chapter. For convenience the Intel® Server System SE7501HG2 Platform Sensors are also listed in Appendix A of this document. Please refer to the Intel® Server Management v5.5 Technical Product Specification for a comprehensive explanation of the features and capabilities of ISM.

Intel bundles ISM with the SE7501HG2 server board to provide a differentiated management solution. Intel® Server Management software provides a suite of components that inform users of the server's health and operational condition. ISM also provides for remote access regardless of the operating system or its condition. Remote access is also independent of server power state (On or Off). The access path to the server can be LAN, modem, or direct connect. The design of ISM is motivated by the following goals:

- One integrated solution for remote management of servers over LAN, modem, and serial communications
- A single look and feel for all Intel® Server Management software
- Single installation framework
- The components within ISM will be modular in nature for easy integration into existing OEM management stacks, with well documented interface points for OEM integration and extensibility
- Each component within ISM plugs into a common ISM framework that allows them to snap into the selected Enterprise System Management Console (HP Openview*, CA Unicenter TNG*).

Each component within ISM supports standalone execution. ISM consists of the following user-visible components:

- Platform Instrumentation Control (PIC)
- Direct Platform Control (DPC)
- System Setup Utility (SSU)
- Client System Setup Utility (CSSU)
- LAN Alert Viewer
- Command Line Interface (CLI) / Serial Over LAN (SOL) (system dependent)

All components rely on a foundation of hardware and firmware support supplied by the Platform Management Technology. An additional overview of this technology is provided in Section 3 of the Intel® Server Management v5.5 Technical Product Specification; please refer to this document for more information.

Intel® Server Management applications use the following access paths to provide management data to the remote console:

- Platform Instrumentation Control (PIC) communicates through a LAN connection to the Platform Instrumentation (PI) resident on the server. Standard DMI/RPC protocols are used for the communication.
- Direct Platform Control (DPC) communicates directly to the server's firmware using IPMI messaging. The BMC accepts this connection through the LAN using the NIC TCO port,

the direct serial interface, or a modem. The NIC TCO port is a special side-band interface from the NIC to the BMC. See Section 6 for information on Direct Platform Control.

- The Client System Setup Utility (CSSU) communicates directly to the server firmware using IPMI messaging. The BMC accepts this connection through the LAN using the NIC TCO port, direct serial interface, or a modem. Once the connection is established, the CSSU will reboot the server to a local service partition. When connected to the service partition, CSSU uses additional networking (PPP or TCP/IP) to provide additional functions.

Note: The service partition must be installed during system setup.
Refer to Section 7 and Section 10 of the Intel® Server Management v5.5 Technical Product Specification for more information about the CSSU and service partition.

- The LAN Alert Viewer is a Java* application that can receive and display IPMI PET traps that are generated by the BMC firmware. These traps are sent over the LAN to the management console.
- Serial over LAN (SOL) is the capability of some servers to redirect serial port B over the LAN. SOL uses the CLI proxy to decode this serial data.
- Platform Instrumentation (PI) components are server operating system resident agents that monitor the server health and provide information and control functions to the ISM management consoles. Platform Instrumentation can be used to manage servers running Windows*, Red Hat* Linux, Novell* NetWare and OpenUnix* operating systems.

PIC, DPC, CSSU, and the LAN Alert Viewer can be used on a Microsoft* Windows* operating system. CLI can be used on either a Windows operating system or on a Red Hat Linux operating system. The operating systems supported may vary by server and by software release; see the Readme.txt file for the SE501HG2 server.

All ISM components support integration under multiple management consoles and under the ISM Standalone framework. OEMs can select one or more individual components to integrate directly into their proprietary management consoles or into an Enterprise System Management Console. The ISM Standalone framework provides a solution for customers who do not wish to integrate into a management console infrastructure.

The integration with management consoles is supported on the Windows versions of the management consoles.

7.2 Platform Management Technology

All Intel® Server Management v5.5 components rely on a foundation of hardware and firmware support supplied by the Platform Management Technology. The core parts of this technology consist of the following:

Intelligent Platform Management Interface (IPMI) IPMI is a set of specifications that defines a standardized, message-based interface to platform management controllers. This includes specifications of command (message) sets, interface protocols, and descriptive records

for the platform management subsystem. IPMI messaging is used by the platform management controllers to communicate to each other and to the platform instrumentation software. The ISM 5.x release supports version 1.5 of the IPMI specification.

Intelligent Platform Management Bus (IPMB) This is a set of specifications that define a management bus inside the system chassis. The management bus allows platform management controllers on various system boards to communicate using IPMI messages. The bus provides a standardized way for chassis board management hardware and value-added management devices, such as remote management cards, to connect to the platform management subsystem on the baseboard.

Intelligent Chassis Management Bus (ICMB) The ICMB is an external management bus that interconnects platform management subsystems in multiple chassis. The ICMB specification defines the characteristics of the bus, how a management controller communicates on the bus, and how to provide a 'bridge' function that allows messages to be sent between the IPMB and ICMB.

Platform BIOS The system BIOS on the platform provides functionality to configure and control the system management aspects of the system during the pre-OS boot state.

Emergency Management Port (EMP) This hardware support allows for direct serial (RS-232) access, or remote access (using an external modem) to the platform management subsystem during various stages of system operation, including the times when the system is powered off. This interface and the protocol is part of the IPMI 1.5 specification.

Platform Event Alerting The Platform Event Alerting features allow the platform management subsystem to proactively alert the administrator of critical system failures. These features are implemented in hardware and firmware and work even when the host operating system is down.

Platform Event Paging With Platform Event Paging (PEP), alerts are sent to a numeric pager. BMC LAN Alert Alerts are sent through the LAN.

7.3 Sahalee Baseboard Management Controller

The Sahalee BMC contains a 32-bit RISC processor core and associated peripherals used to monitor the system for critical events. The Sahalee BMC is packaged in a 156-pin BGA and monitors all power supplies, including those generated by the external power supplies and those regulated locally on the server board. It also monitors SCSI termination voltage, fan tachometers for detecting a fan failure, and system temperature. Temperature is measured on each of the processors and at locations on the server board away from the fans. When any monitored

parameter is outside of the defined thresholds, the Sahalee BMC logs an event in the System Event Log.

Management controllers and sensors communicate on the I^2C-based Intelligent Platform Management Bus (IPMB). Attached to one of its private I^2C* bus is Heceta5, an ADM1026, which is a versatile systems monitor ASIC. Some of its features include:

- Analog measurement channels
- Fan speed measurement channels
- General-Purpose Logic I/O pins
- Remote temperature measurement
- On-chip temperature sensor
- Chassis intrusion detect

The following table details the inputs/outputs of the Sahalee BMC as used on the server board SE7501HG2.

Table 19. Sahalee BMC Pin-out

Pin #	Signal Name	Ball	Type	Net Name	Description
1	TDI	B2	Bidir	BMC_TDI	Test Data In
2	TDO	B1	Bidir	BMC_TDO	Test Data Out
3	TRST#	C2	Bidir	BMC_TRST_L	Test Reset
4	TMS	C1	Bidir	BMC_TMS	Test Mode select
5	TCK	D2	Bidir	BMC_TCK	Test clock
6	TEST_MODE_L	D3	Input	PU_BMC_1	Dedicated test mode pin that places Sahalee into production test mode, pulled-up to 3.3Vstandby
7	RST#	D1	Input	BMC_RST_DLY_L	Resets the Sahalee
8	LPCRST#	D4	Input	RST_LPC_BMC_L	LPC bus reset
9	LPCPD#	E2	Input	ICH3_SLP_S1_L	Power down indication
10	LAD<3>	E1	Bidir	LPC_ADR<3>	Address Data Bus
11	LAD<2>	E3	Bidir	LPC_ADR<2>	Address Data Bus
12	IOVCC<0>	E4		P3V3_STBY	I/O Power, 3.3V
13	LAD<1>	F2	Bidir	LPC_ADR<1>	Address Data Bus
14	LAD<0>	F1	Bidir	LPC_ADR<0>	Address Data Bus
15	LFRAME#	F3	Bidir	LPC_FRAME_L	Cycle framing
16	LDRQ#	F4	Bidir	LPC_DRQ_L0	DMA_Request
17	SYSIRQ	G2	Bidir	BMC_SYSIRQ	Interrupt
18	LCLK	G1	Input	CLK_33M_BMC	Bus Clock
19	COREGND<0>	G4		Ground	Ground
20	COREVCC<0>	H3		P3V3_STBY	Core VCC
21	CS1#	G3	Bidir	BMC_SRAM_CE_L	Select line indicating that region 1(external memory-mapping) is active for the current cycle
22	CS0#	H1	Bidir	BMC_CS0_L	Select line indicating that region 0(external memory-mapping) is active for the current cycle

Pin #	Signal Name	Ball	Type	Net Name	Description
23	ADDR<21>	H2	Bidir	BMC_A<21>	Address bit 21, used to clock data into external latch
24	ADDR<20>	H4	Bidir	BMC_A<20>	Address bit 20
25	ADDR<19>	J1	Bidir	BMC_A<19>	Address bit 19
26	ADDR<18>	J3	Bidir	BMC_A<18>	Address bit 18
27	ADDR<17>	J2	Bidir	BMC_A<17>	Address bit 17
28	IOGND<0>	J4		Ground	Ground
29	ADDR<16>	K1	Bidir	BMC_A<16>	Address bit 16
30	ADDR<15>	K3	Bidir	BMC_A<15>	Address bit 15
31	ADDR<14>	K2	Bidir	BMC_A<14>	Address bit 14
32	ADDR<13>	K4	Bidir	BMC_A<13>	Address bit 13
33	ADDR<12>	L1	Bidir	BMC_A<12>	Address bit 12
34	ADDR<11>	L3	Bidir	BMC_A<11>	Address bit 11
35	ADDR<10>	L2	Bidir	BMC_A<10>	Address bit 10
36	VDD5V<0>	M1	SB5V	P5V_STBY	Standby Power
37	ADDR<9>	M3	Bidir	BMC_A<9>	Address bit 9
38	ADDR<8>	M2	Bidir	BMC_A<8>	Address bit 8
39	ADDR<7>	N1	Bidir	BMC_A<7>	Address bit 7
40	ADDR<6>	N2	Bidir	BMC_A<6>	Address bit 6
41	ADDR<5>	P2	Bidir	BMC_A<5>	Address bit 5
42	IOVCC<1>	N3		P3V3_STBY	Core VCC
43	ADDR<4>	P3	Bidir	BMC_A<4>	Address bit 4
44	ADDR<3>	N4	Bidir	BMC_A<3>	Address bit 3
45	ADDR<2>	M4	Bidir	BMC_A<2>	Address bit 2
46	ADDR<1>	P4	Bidir	BMC_A<1>	Address bit 1
47	ADDR<0>	L4	Bidir	BMC_A<0>	Address bit 0
48	DATA<15>	N5	Bidir	BMC_D<15>	Data bit 15
49	DATA<14>	P5	Bidir	BMC_D<14>	Data bit 14
50	DATA<13>	M5	Bidir	BMC_D<13>	Data bit 13
51	DATA<12>	L5	Bidir	BMC_D<12>	Data bit 12
52	DATA<11>	N6	Bidir	BMC_D<11>	Data bit 11
53	DATA<10>	P6	Bidir	BMC_D<10>	Data bit 10
54	DATA<9>	M6	Bidir	BMC_D<9>	Data bit 9
55	IOGND<1>	L6		GND	Ground
56	DATA<8>	N7	Bidir	BMC_D<8>	Data bit 8
57	DATA<7>	P7	Bidir	BMC_D<7>	Data bit 7
58	COREGND<1>	L7		GND	Ground
59	COREVCC<1>	M8		P3V3_STBY	Core VCC
60	XTAL2	M7	Output	Not Connected	
61	XTAL1	P8	Input	SIO_CLK_40M_BMC	40MHz Clock Input
62	DATA<6>	N8	Bidir	BMC_D<6>	Data bit 6
63	DATA<5>	L8	Bidir	BMC_D<5>	Data bit 5
64	DATA<4>	P9	Bidir	BMC_D<4>	Data bit 4

Pin #	Signal Name	Ball	Type	Net Name	Description
65	DATA<3>	M9	Bidir	BMC_D<3>	Data bit 3
66	DATA<2>	N9	Bidir	BMC_D<2>	Data bit 2
67	DATA<1>	L9	Bidir	BMC_D<1>	Data bit 1
68	DATA<0>	P10	Bidir	BMC_D<0>	Data bit 0
69	WE#	M10	Bidir	BMC_WE_L	Write enable signal
70	OE#	N10	Bidir	BMC_OE_L	Output enable
71	IOVCC<2>	L10		P3V3_STBY	Core VCC
72	REG#	P11	Input	BMC_CPU2_SKTOCC_L	Indicates that CPU2 socket is occupied.
73	CE2#	M11	Output	RST_VRM_DIS_L	Disables VCCP VRM
74	CE1#	N11	Input	BMC_CPU1_SKTOCC_L	Indicates that CPU1 socket is occupied.
75	SBHE#	P12	Bidir	BMC_SBHE_L	Byte High Enable
76	IOR#	M12	Output	BMC_SECURE_MODE_KB_L	Disable keyboard in Secure Mode
77	IOW#	N12	Input	FP_PWR_BTN_L	Front panel power button control
78	MEMR#	P13	Input	FP_ID_BTN_L	Front panel unit ID button control
79	MEMW#	N13	Input	FP_SLP_BTN_L	Front panel sleep button control
80	BALE	N14	Input	FP_NMI_BTN_L	Assert NMI signal from front panel (diagnostic control)
81	IOCHRDY	M13	Input	FP_RST_BTN_L	Front panel reset button control
82	BW8#	M14	Output	BMC_SLP_BTN_L	Enable sleep function
83	XINT<7>	L13	Input	ICH3_SMI_BUFF_R_L	SMI asserted from chipset
84	XINT<6>	L12	Input	BMC_CPU12_PROCHOT_L	High temperature warning indicated from CPU1 and/or CPU2
85	XINT<5>	L14	Output	SERIAL_TO_LAN_L	Serial to LAN enable
86	IOGND<2>	L11		GND	Ground
87	XINT<4>	K13	Input	NIC_SMBALERT_L	Interrupt Source
88	XINT<3>	K14	Input	ZZ_FRB3_TIMER_HALT_L	FRB3 timer disable from Jumper
89	XINT<2>	K12	Input	ICH3_CPU_SLP_L	Sleep initiated from chipset
90	XINT<1>	K11	Input	ICH3_SLP_S5_L	Sleep state S5 initiated from chipset
91	XINT<0>	J13	Input	RST_PWRGD_PS	System reset
92	BAUD	J14	Output	BMC_IRQ_SMI_L	BMC initiated SMI
93	RI#	J12	Input	SPB_RI_L	Ring Indicate Input
94	DTR1#	J11	Output	BMC_LATCH_OE_L	External latch enable
95	DCD1#	H13	Input	BMC_ICMB_RX	Tied to ICMB_RX
96	CTS1#	H14	Input	ZZ_BMC_FRC_UPDATE_L	BMC Forced Update
97	COREGND<2>	H11		GND	Ground
98	COREVCC<2>	G12		P3V3_STBY	Core VCC
99	RTS1#	H12	Output	BMC_ICMB_TX_ENB_L	Transmit Enable of ICMB
100	RX1	G14	Input	BMC_ICMB_RX	Received data of ICMB
101	TX1	G13	Output	BMC_ICMB_TX	Transmit data of ICMB
102	IOVCC<3>	G11		P3V3_STBY	Core VCC
103	DTR0#	F14	Output	BMC_DTR_L	Serial B/EMP port DTR
104	DCD0#	F12	Input	BMC_DCD_L	Serial B/EMP port DCD

Pin #	Signal Name	Ball	Type	Net Name	Description
105	CTS0#	F13	Input	BMC_CTS_L	Serial B/EMP port CTS
106	RTS0#	F11	Output	BMC_RTS_L	Serial B/EMP port RTS
107	VDD5V<1>	E14		SB5V	Standby 5V
108	RX0	E12	Input	BMC_SIN	Serial B/EMP port Rx Data
109	TX0	E13	Output	BMC_SOUT	Serial B/EMP port Tx Data
110	TIC4_IN	E11	Input	CLK_32K_RTC	32KHz Clock input from SIO
111	TIC3_OUT	D14	Bidir	BMC_NMI_L	Assert/monitor NMI signal
112	TIC2_IN<7>	D12	Schmitt input	FAN8_TACH	Fan tach signal
113	TIC2_IN<6>	D13	Schmitt input	FAN7_TACH	Fan tach signal
114	TIC2_IN<5>	C14	Schmitt input	FAN6_TACH	Fan Tach signal
115	IOGND<3>	C12		GND	Ground
116	TIC2_IN<4>	C13	Schmitt input	FAN5_TACH	Fan Tach Signal
117	TIC2_IN<3>	B14	Schmitt input	FAN4_TACH	Fan Tach Signal
118	TIC2_IN<2>	B13	Schmitt input	FAN3_TACH	Fan Tach Signal
119	TIC2_IN<1>	A13	Schmitt input	FAN2_TACH	Fan Tach Signal
120	TIC2_IN<0>	B12	Schmitt input	FAN1_TACH	Fan Tach Signal
121	TIC1_OUT	A12	Output	BMC_SPKR_L	Speaker output
122	LSMI#	B11	Output	BMC_SCI_L	BMC generate System Control Interrupt
123	LED<5>	C11	Output	RST_P6_PWRGOOD	Power Good signal to CPUs
124	LED<4>	A11	Output	RST_BMC_PS_PWR_ON_L	Power Supply on/off control
125	LED<3>	D11	Output	BMC_PWR_BTN_L	Power Button output
126	LED<2>	B10	Output	BMC_SPB_OE_L	Serial port B enable
127	LED<1>	A10	Output	ZZ_BMC_ROLLING_BIOS_L	BIOS flash memory highest adress for rolling BIOS
128	LED<0>	C10	Input	CPU12_BSEL0	
129	IOVCC<4>	D10		P3V3_STBY	I/O Vcc
130	SDA5	B9	Schmitt bidir	PB4_I2C_3VSB_SDA	SMB Data/Address for NICs
131	SCL5	A9	Schmitt bidir	PB4_I2C_3VSB_SCL	SMB Clock for NICs
132	SDA4	C9	Schmitt bidir	PB3_I2C_3V_SDA	Private I2C Bus #3 Data/Address to Chipset and Processors
133	SCL4	D9	Schmitt bidir	PB3_I2C_3V_SCL	Private I2C Bus #3 Clockto Chipset and Processors
134	SDA3	B8	Output	SCWA_STPW_EN_L	Onboard SCSI channel A termination enable
135	SCL3	A8	Output	SCWB_STPW_EN_L	Onboard SCSI channel B termination enable
136	COREGND<3>	D8		GND	Ground

Pin #	Signal Name	Ball	Type	Net Name	Description
137	COREVCC<3>	C7		P3V3_STBY	Core VCC
138	SDA2	C8	Schmitt bidir	PB1_I2C_5VSB_SDA	Private I2C Bus #1Data /Address to Front panel, SIO, Heceta and Power supply
139	SCL2	A7	Schmitt bidir	PB1_I2C_5VSB_SCL	Private I2C Bus #1 Clock to Front panel, SIO, Heceta and Power supply
140	SDA1	B7	Schmitt bidir	SMB_I2C_3VSB_SDA	SMB Address
141	SCL1	D7	Schmitt bidir	SMB_I2C_3VSB_SCL	SMB Data
142	SDA0	A6	Schmitt bidir	IPMB_I2C_5VSB_SDA	IPMB Address
143	IOGND<4>	C6		GND	Ground
144	SCL0	B6	Schmitt bidir	IPMB_I2C_5VSB_SCL	IPMB Data
145	AVDD	D6	Analog power	P3V3_STBY	Analog 3.3 supply
146	A2D<7>	A5	Analog input	SCWA_TRMPWR_MON	SCSI channel A Terminator Power Monitor
147	A2D<6>	C5	Analog input	SCWB_TRMPWR_MON	SCSI channel B Terminator Power Monitor
148	A2D<5>	B5	Analog input	Not Connected	
149	A2D<4>	D5	Analog input	Not Connected	
150	A2D<3>	A4	Analog input	Not Connected	
151	A2D<2>	C4	Analog input	Not Connected	
152	A2D<1>	B4	Analog input	Not Connected	
153	A2D<0>	A3	Analog input	Not Connected	
154	VREF	C3	Analog input	BMC_VREF_A_2P5V	Use accurate stable and low noise 2.5 source
155	AVS	B3	round	GND	analog negative power supply, not connected to substrate
156	AVSUB	A2	Analog ground	GND	Analog negative power supply, connected to substrate

An ADM1026 has been attached to the private I^2C bus for monitoring the system temperature, additional analog voltages, and the voltage identifications bits for both processors. The following table describes these added signals. The ADM1026 device also provides a PWM (Pulse Width Modulation) for fan speed control.

Table 20. ADM1026 Input Definition

Pin	Signal Name	Type	Description
3	FAN0/GPIO0	Digital Input	CPU2 VID [0]
4	FAN1/GPIO1	Digital Input	CPU2 VID [1]
5	FAN2/GPIO2	Digital Input	CPU2 VID [2]
6	FAN3/GPIO3	Digital Input	CPU2 VID [3]
9	FAN4/GPIO4	Digital Input	CPU2 VID [4]
10	FAN5/GPIO5	Digital Input	CPU2 IERR
11	FAN6/GPIO6	Digital Input	CPU2 Thermal Trip
12	FAN7/GPIO7	Digital Output	CPU2 disable
2	GPIO<8>	Digital Input	CPU1 VID [0]
1	GPIO<9>	Digital Input	CPU1 VID [1]
48	GPIO<10>	Digital Input	CPU1 VID [2]
47	GPIO<11>	Digital Input	CPU1 VID [3]
46	GPIO<12>	Digital Input	CPU1 VID [4]
45	GPIO<13>	Digital Input	CPU1 IERR
44	GPIO<14>	Digital Input	CPU1 Thermal Trip
43	GPIO<15>	Digital Output	CPU1 disable
16	CHS_INT	Digital Input	An active high input which captures a chassis intrusion event in Bit 7 of Status Register 4. This bit will remain set until cleared,
29	VBAT	Digital Input	So long as battery voltage is applied to the VBAT input, even when the ADM1026 is powered off
13	SCL	Digital Input	BMC Private I2C Bus 1 Clock
14	SDA	Digital I/O	BMC Private I2C Bus 1 Data
15	ADDR/NTESTOUT	Digital Input	I2C Device address select, 0 ohm pull-down to GND
18	PWM	Digital Output	Pulse-width modulated output for control of fan speed. Open drain.
19	RESET_STBY#	Digital Output	Power-on Reset. 5 mA driver (open drain), active low output with a 200 ms minimum pulse width. This is asserted whenever 3.3VSTBY is below the reset threshold. It remains asserted for approx. 200ms after 3.3VSTBY rises above the reset threshold.
30	+5V	Analog Input	Monitors +5 V supply
31	-12V	Analog Input	Monitors -12 V supply
32	+12V	Analog Input	Monitors +12 V supply
33	VCCP	Analog Input	Monitors processor core voltage (0 to 3.0 V)
34	AIN7	Analog Input	Monitors +1.2V supply
35	AIN6	Analog Input	Monitors VTT supply
36	AIN5	Analog Input	Monitors +12V VRM supply
37	AIN4	Analog Input	Monitors +1.8V supply
38	AIN3	Analog Input	Monitors +2.5V supply
39	AIN2	Analog Input	Monitors +5V Standby supply
40	AIN1	Analog Input	Monitors +1.8V Standby supply

Pin	Signal Name	Type	Description
41	AIN0	Analog Input	Monitors +3.3V Standby supply
24	VREF	Analog Input	+2.5V analog reference voltage
25	D1-/NTESTIN	Analog Input	CPU1 Thermal Diode
26	D1+	Analog Input	CPU1 Thermal Diode
27	D2-/AIN9	Analog Input	CPU2 Thermal Diode
28	D2+/AIN8	Analog Input	CPU2 Thermal Diode
7	VDD	Power	3.3V Power
22	STBY_VDD	Power	3.3v Stand-by Power
42	GPIO16/THERM#	Digital Output	Not Connected
23	DAC	Analog Output	Not Connected
21	AGND	Groud	Ground
8	DGND	Groud	Ground
20	RESET#	Digital I/O	Not Connected
17	INT#	Digital Output	Not Connected

7.3.1 Fault Resilient Booting

The Sahalee BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If the default bootstrap processor (BSP) fails to complete the boot process, the FRB attempts to boot using an alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a watchdog timeout during POST. The watchdog timer for FRB level 2 detection is implemented in the Sahalee BMC.
- FRB level 3 is for recovery from a watchdog timeout on hard reset or power-up. The Sahalee BMC provides hardware functionality for this level of FRB.

7.3.1.1 FRB-1

In a multiprocessor system, the BIOS registers the application processors in the MP table and the ACPI APIC tables. When started by the BSP, if an AP fails to complete initialization within a certain time, it is assumed to be non-functional. If the BIOS detects that an application processor has failed BIST or is nonfunctional, it requests that the BMC disable that processor. The BMC then generates a system reset while disabling the processor; the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification, Rev. 1.4*), nor in the ACPI APIC tables, and is invisible to the operating system.

If the BIOS detects that the BSP has failed BIST, it sends a request to BMC to disable the present processor. If there is no alternate processor available, the BMC beeps the speaker and halts the system. If BMC can find another processor, BSP ownership is transferred to that processor via a system reset.

7.3.1.2 FRB-2

The second watchdog timer (FRB-2) in the BMC is set for approximately 6 minutes by BIOS and is designed to guarantee that the system completes BIOS POST. The FRB-2 timer is enabled before the FRB-3 timer is disabled to prevent any “unprotected” window of time. Near the end of POST, before the option ROMs are initialized, the BIOS disables the FRB-2 timer in the BMC.

If the system contains more than 1 GB of memory and the user chooses to test every DWORD of memory, the watchdog timer is disabled before the extended memory test starts. This is because the memory test can take more than 6 minutes under this configuration. If the system hangs during POST, the BIOS does not disable the timer in the BMC, which generates an asynchronous system reset (ASR).

7.3.1.3 FRB-3

The first timer (FRB-3) starts counting down whenever the system comes out of hard reset, which is usually about 5 seconds. If the BSP successfully resets and starts executing, the BIOS disable the FRB-3 timer in the BMC by de-asserting the FRB3_TIMER_HLT* signal (GPIO) and the system continues with the POST.

If the timer expires because of BSP failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system continues to change the bootstrap processor until the BIOS POST gets past disabling the FRB-3 timer in the BMC. The BMC sounds beep codes on the speaker, if it fails to find a good processor. The process of cycling through all the processors is repeated upon system reset or power cycle.

7.4 System Reset Control

Reset circuitry on the server board SE7501HG2 looks at resets from the front panel, ICH3-S, ITP, and the processor subsystem to determine proper reset sequencing for all types of resets. The reset logic accommodates several methods to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

The following subsections describe each type of reset.

7.4.1 Power-up Reset

When the system is disconnected from AC power, all logic on the server board is powered off. When a valid input (AC) voltage level is provided to the power supply, 5-volt standby power will be applied to the server board. The baseboard has a 5-volt to 3.3-volt regulator to produce 3.3-volt standby voltage. A power monitor circuit on 3.3-volt standby will assert BMC_RST_L, causing the BMC to reset. The BMC is powered by 3.3 volt standby and monitors and controls key events in the system related to reset and power control.

After the system is turned on, the power supply will assert the RST_PWRGD_PS signal after all voltage levels in the system have reached valid levels. The BMC receives RST_PWRGD_PS and

after 500 ms asserts RST_P6_PWRGOOD, which indicates to the processors and ICH3-S that the power is stable. Upon RST_P6_PWRGOOD assertion, the ICH3-S will toggle PCI reset.

7.4.2 Hard Reset

A hard reset can be initiated by resetting the system through the front panel switch. During the reset, the Sahalee BMC de-asserts RST_P6_PWRGOOD. After 500 ms, it is reasserted, and the power-up reset sequence is completed.

Note: The Sahalee BMC is not reset by a hard reset. It is only reset when AC power is applied to the system.

7.4.3 Soft Reset

A soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO, by the ICH3-S, or by the operating system.

7.5 Intelligent Platform Management Buses (IPMB)

Management controllers (and sensors) communicate on the I^2C-based Intelligent Platform Management Bus. A bit protocol, defined by the *I^2C Bus Specification*, and a byte-level protocol, defined by the *Intelligent Platform Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on this I^2C bus.

The IPMB extends throughout the server board and system chassis. An added layer in the protocol supports transactions between multiple servers on Inter-Chassis Management Bus (ICMB) I^2C segments.

The server board SE7501HG2 provides two 4-pin IPMB connectors to support a dual HSBP configuration. In addition to the “public” IPMB, the Sahalee BMC also has three private I^2C busses. The Sahalee BMC is the only master on the private busses. The following table lists all server board connections to the Sahalee BMC I^2C buses.

Table 21. Intel® Server Board SE7501HG2 I^2C Bus Address Map

I2C Bus	I^2C Addr	Device
Private Bus 1	0x58	Heceta5
	0x60	SIO
	0xAC	Power Distribution Board
	0xA0	Power Supply1
	0xA2	Power Supply2
	0xA4	Power Supply3
Private Bus 3	0x30	CPU1 therm sensor
	0x32	CPU2 therm sensor
	0x44	ICH3-S
	0x60	MCH

I2C Bus	I^2C Addr	Device
	0xA2	DIMM1
	0xA0	DIMM3
	0xA6	CPU1 SEEPROM
	0xAA	DIMM2
	0xA8	DIMM4
	0xAE	CPU2 SEEPROM
	0xC4	P64H2
	0xD2	CK408B
Private Bus 4	0x84	NIC1
	0x86	NIC2

7.6 Inter Chassis Management Bus (ICMB)

The BMC on the SE7501HG2 has built-in support for the ICMB interface. However an optional ICMB card is required to use this feature since the ICMB transceivers are not provided on the board. A five pin ICMB connector on the SE7501HG2 board provides the interface to the ICMB module.

7.7 Error Reporting

This section documents the types of system bus error conditions monitored by the SE7501HG2 board set.

7.7.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System error reporting on the SE7501HG2 can be disabled and enabled individually. These can be categorized as follows:

- PCI bus errors
- Processor bus errors
- Memory single- and multi-bit errors
- General Server Management sensors

On the SE7501HG2 platform, the Sahalee BMC manages general server management sensors.

7.7.2 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

7.7.3 Intel® Xeon™ Processor Bus Errors

The MCH supports the data integrity features supported by the Intel® Xeon™ processor system bus, including address, request, and response parity. In addition, the MCH can generate BERR# on unrecoverable errors detected on the processor bus. Unrecoverable errors are routed to an NMI if enabled by the BIOS.

7.7.4 Memory Bus Errors

The MCH is programmed to generate an SMI on single-bit or multi-bit data errors in the memory array if ECC memory is installed. The MCH performs the scrubbing. The SMI handler records the error and the DIMM location to the system event log.

7.7.5 ID LED

The blue “ID LED”, located at the back edge of the baseboard near the speaker, is used to help locate a given server platform when the server is installed in a multi-system rack. The LED is lit when the front panel ID button is pressed and is turned off when the button is pressed again. A user-defined interface can be developed to activate the ID LED remotely.

7.7.6 System Status LED

The System Status LED is located on the Front Panel Controller board and can be viewed from the front bezel behind the front cover of the SC5200 server chassis. Each status is described in the following table.

Table 22. Boot Block POST Progress Codes

LED Color	LED State	Description
Green	ON	Running. BIOS Initialization complete, boot started / normal operation.
	Blink	Degraded condition
Amber	ON	Critical or Non-Recoverable Condition
	Blink	Non-Critical Condition (e.g., Fan fault)
Off	Off	POST / System Stop.

7.7.6.1 System Status Indications

- **Critical Condition.** Any critical or non-recoverable threshold crossing associated with the following events:
    - Temperature, voltage, or fan critical threshold crossing.
    - Power Subsystem Failure. The BMC asserts this failure whenever it detects a power control fault (e.g., the BMC detects that the system power is remaining ON even though the BMC has de-asserted the signal to turn off power to the system). A hot-swap backplane would use the Set Fault Indication command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane.

- The system is unable to power up due to incorrectly installed processor(s), or processor incompatibility.
- The satellite controller sends a critical or non-recoverable state, via the Set Fault Indication command to the BMC.
- “Critical Event Logging” errors exist.

- **Non-Critical Condition**
    - o Temperature, voltage, or fan non-critical threshold crossing.
    - o Chassis Intrusion.
    - o The satellite controller sends a non-critical state, via the Set Fault Indication command, to the BMC.
    - o Set Fault Indication Command.
- **Degraded Condition**
    - o Non-redundant power supply operation. This only applies when the BMC is configured for a redundant power subsystem. The power unit configuration is configured via OEM SDR records.
    - o A processor is disabled by the FRB or BIOS.
    - o BIOS has disabled or mapped out some of the system memory.

7.7.7 POST Progress Codes

The system will perform a Power On Self Test (POST) during each system initialization. If a system should hang during the initialization process, a POST-code should be generated to aid in determining the last process that was executed prior to the hang.

Table 23. Boot Block POST Progress Codes

POST Code	Description
06h	Uncompressing the POST code.
10h	The NMI is disabled. Strart Power-on delay. Initialization code checksum verified.
11h	Initialize the DMA controller, perform the keyboard controller BAT test, start memory refresh, and enter 4 GB flat mode.
12h	Get start of initialization code and check BIOS header.
13h	Memory sizing.
14h	Test base 512K of memory. Return to real mode. Execute any OEM patches and set up the stack.
15h	Pass control to the uncompressed code in shadow RAM. The initialization code is copied to segment 0 and control will be transferred to segment 0.
16h	Control is in segment 0. Verify the system BIOS checksum. If the system BIOS checksum is bad, go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
17h	Pass control to the interface module.
18h	Decompress of the main system BIOS failed.
19h	Build the BIOS stack. Disable USB controller. Disable cache.
1Ah	Uncompress the POST code module. Pass control to the POST code module.
1Bh	Decompress the main system BIOS runtime code.
1Ch	Pass control to the main system BIOS in shadow RAM.
D2h	Starting chipset register initialization and memory sizing.
D3h	Doing memory sizing and chipset register initialization. First set BIOS size to 128K and do memory sizing.
D5h	The initialization code is copied to segment 0 and control will be transferred to segment 0.

POST Code	Description
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
A0h	Detect memory device type using SPD
A8h	To program ECC Mode
E0h	Start of recovery BIOS. Initialize interrupt vectors, system timer, DMA controller, and interrupt controller.
E8h	Initialize extra module if present.
E9h	Initialize floppy controller.
EAh	Try to boot floppy diskette.
EBh	If floppy boot fails, intialize ATAPI hardware.
ECh	Try booting from ATAPI CD-ROM drive.
EEh	Jump to boot sector.
EFh	Disable ATAPI hardware.

Table 24. POST Progress Code Table

POST Code	Description
0Eh	The keyboard controller BAT command result has been verified. It is auto-sensing of external keyboard and mouse mostly used in laptop.
15h	8254 timer.read/ write test on channel 2.
20h	Uncompress various BIOS Modules
22h	Verify password Checksum
24h	Verify CMOS Checksum.
26h	Read Microcode updates from BIOS ROM.
28h	Initializing the processors. Set up processor registers. Select least featured processor as the BSP.
2Ah	Go to Big Real Mode
2Ch	Decompress INT13 module
2Eh	Keyboard Controller Test: The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller
30h	Keyboard/Mouse port swap, if needed
32h	Write Command Byte 8042: The initialization after the keyboard controller BAT command test is done. The keyboard command byte will be written next.
34h	Keyboard Init: The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands
36h	Disable and initialize 8259
38h	Detect Configuration Mode, such as CMOS clear.
3Ah	Chipset Initialization before CMOS initialization
3Ch	Init System Timer: The 8254 timer test is over. Starting the legacy memory refresh test next.
3Eh	Check Refresh Toggle: The memory refresh line is toggling. Checking the 15 second on/off time next
40h	Calculate CPU speed
42h	Init interrupt Vectors: Interrupt vector initialization is done.
44h	Enable USB controller in chipset
46h	Initialize SMM handler. Initialize USB emulation.
48h	Validate NVRAM areas. Restore from backup if corrupted.

POST Code	Description
4Ah	Load defaults in CMOS RAM if bad checksum or CMOS clear jumper is detected.
4Ch	Validate date and time in RTC.
4Eh	Determine number of micro code patches present
50h	Load Micro Code To All CPUs
52h	Scan SMBIOS GPNV areas
54h	Early extended memory tests
56h	Disable DMA
58h	Disable video controller
5Ah	8254 Timer Test on Channel 2
5Ch	Enable 8042. Enable timer and keyboard IRQs. Set Video Mode: Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
5Eh	Init PCI devices and motherboard devices. Pass control to video BIOS. Start serial console redirection.
60h	Initialize memory test parameters
62h	Initialize AMI display manager Module. Initialize support code for headless system if no video controller is detected.
64h	Start USB controllers in chipset
66h	Set up video parameters in BIOS data area.
68h	Activate ADM: The display mode is set. Displaying the power-on message next.
6Ah	Initialize language module. Display splash logo.
6Ch	Display Sign on message, BIOS ID and processor information.
6Eh	Detect USB devices
70h	Reset IDE Controllers
72h	Displaying bus initialization error messages.
74h	Display Setup Message: The new cursor position has been read and saved. Displaying the Hit Setup message next.
76h	Ensure Timer Keyboard Interrupts are on.
78h	Extended background memory test start
7Ah	Disable parity and nmi reporting.
7Ch	Test 8237 DMA Controller: The DMA page register test passed. Performing the DMA Controller 1 base register test next
7Eh	Init 8237 DMA Controller: The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
80h	Enable Mouse and Keyboard: The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next
82h	Keyboard Interface Test: A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
83h	Disable parity and NMI.
84h	Check Stuck Key Enable Keyboard: The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
86h	Disable parity NMI: The command byte was written and global data initialization has completed. Checking for a locked key next
88h	Display USB devices
8Ah	Verify RAM Size: Checking for a memory size mismatch with CMOS RAM data next
8Ch	Lock out PS/2 keyboard/mouse if unattended start is enabled.
8Eh	Init Boot Devices: The adapter ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
90h	Display IDE mass storage devices.

POST Code	Description
92h	Display USB mass storage devices.
94h	Report the first set of POST Errors To Error Manager.
96h	Boot Password Check: The password was checked. Performing any required programming before Setup next.
98h	Float Processor Initialize: Performing any required initialization before the coprocessor test next.
9Ah	Enable Interrupts 0,1,2: Checking the extended keyboard, keyboard ID, and NUM Lock key next. Issuing the keyboard ID command next
9Ch	Init FDD Devices. Report second set of POST errors To Error messager
9Eh	Extended background memory test end
A0h	Prepare And Run Setup: Error manager displays and logs POST errors. Waits for user input for certain errors. Execute setup.
A2h	Set Base Expansion Memory Size
A4h	Program chipset setup options, build ACPI tables, build INT15h E820h table
A6h	Set Display Mode
A8h	Build SMBIOS table and MP tables.
AAh	Clear video screen.
ACh	Prepare USB controllers for OS
AEh	One Beep to indicate end of POST. No beep if silent boot is enabled.
F2h	Enable USB function/Clock. Initialize GPC for USB. GPC initialization consist of USB initialization and APM initialization.
F5h	Validate the NVRAM area. Called at check point 27h.
000h	POST completed. Passing control to INT 19h boot loader next.

7.7.8 POST Error Codes and Messages

The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some of the error messages are preceded by the string “Error” to highlight the fact that the system might be malfunctioning. All POST errors and warnings are logged in the system event log, unless the SEL is full.

Table 25. Standard POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
100	Timer Channel 2 Error	Yes
101	Master Interrupt Controller	Yes
102	Slave Interrupt Controller	Yes
103	CMOS Battery Failure	Yes
104	CMOS Options not Set	Yes
105	CMOS Checksum Failure	Yes
106	CMOS Display Error	Yes
107	Insert Key Pressed	Yes
108	Keyboard Locked Message	Yes
109	Keyboard Stuck Key	Yes
10A	Keyboard Interface Error	Yes
10B	System Memory Size Error	Yes

Error Code	Error Message	Pause on Boot
10E	External Cache Failure	Yes
110	Floppy Controller Error	Yes
111	Floppy A: Error	Yes
112	Floppy B: Error	Yes
113	Hard disk 0 Error	Yes
114	Hard disk 1 Error	Yes
115	Hard disk 2 Error	Yes
116	Hard disk 3 Error	Yes
117	CD-ROM disk 0 Error	Yes
118	CD-ROM disk 1 Error	Yes
119	CD-ROM disk 2 Error	Yes
11A	CD-ROM disk 3 error	Yes
11B	Date/Time not set	Yes
11E	Cache memory bad	Yes
120	CMOS clear	Yes
121	Password clear	Yes
122	CMOS cleared by BMC	Yes
140	PCI Error	Yes
141	PCI Memory Allocation Error	Yes
142	PCI IO Allocation Error	Yes
143	PCI IRQ Allocation Error	Yes
144	Shadow of PCI ROM Failed	Yes
145	PCI ROM not found	Yes
146	Insufficient Memory to Shadow PCI ROM	Yes

Table 26. Extended POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
8100	Processor 1 failed BIST	No
8101	Processor 2 failed BIST	No
8110	Processor 1 Internal error (IERR)	No
8111	Processor 2 Internal error (IERR)	No
8120	Processor 1 Thermal Trip error	No
8121	Processor 2 Thermal Trip error	No
8130	Processor 1 disabled	No
8131	Processor 2 disabled	No
8140	Processor 1 failed FRB-3 timer	No
8141	Processor 2 failed FRB-3 timer	No
8150	Processor 1 failed initialization on last boot.	No
8151	Processor 2 failed initialization on last boot.	No
8160	Processor 01: unable to apply BIOS update	Yes
8161	Processor 02: unable to apply BIOS update	Yes
8170	Processor P1 :L2 cache Failed	Yes
8171	Processor P2 :L2 cache Failed	Yes

Error Code	Error Message	Pause on Boot
8180	Bios does not support current stepping for Processor P1	Yes
8181	Bios does not support current stepping for Processor P2	Yes
8190	Watchdog Timer failed on last boot	No
8191	4:1 Core to bus ratio: Processor Cache disabled	Yes
8192	L2 Cache size mismatch	Yes
8193	CPUID, Processor Stepping are different	Yes
8194	CPUID, Processor Family are different	Yes
8195	Front Side Bus Speed mismatch. System Halted	Yes, Halt
8196	Processor Model are different	Yes
8197	Cpu Speed mismatch	Yes
8300	Baseboard Management Controller failed to function	Yes
8301	Front Panel Controller failed to Function	Yes
8305	Hotswap Controller failed to Function	Yes
8306	OS boot watchdog timer failure	No
8307	BIOS/POST watchdog timer failure	Yes
8310	Change in server management configuration	No
8420	Intelligent System Monitoring Chassis Opened	Yes
84F1	Intelligent System Monitoring Forced Shutdown	Yes
84F2	Server Management Interface Failed	Yes
84F3	BMC in Update Mode	Yes
84F4	Sensor Data Record Empty	Yes
84FF	System Event Log Full	Yes
8500	Bad or missing memory in slot 3A	Yes
8501	Bad or missing memory in slot 2A	Yes
8502	Bad or missing memory in slot 1A	Yes
8504	Bad or missing memory in slot 3B	Yes
8505	Bad or missing memory in slot 2B	Yes
8506	Bad or missing memory in slot 1B	Yes
8601	All Memory marked as fail. Forcing minimum back online.	Yes
8602	Single/Double bank mixed DIMM population error	Yes

7.7.9 POST Error Beep Codes

The following three tables list POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users of error conditions. Short beeps will be generated and an error code will be posted on debug port 80h.

7.7.10 BIOS Recovery Beep Codes

In the case of a Bootblock update, where video is not available for text messages to be displayed, speaker beeps are necessary to inform the user of any errors. The following table describes the type of error beep codes that may occur during the Bootblock update.

Table 27. BIOS Recovery Beep Codes

Beeps	Error message	POST Progress Code	Description
1	Recovery started		Start recovery process
2	Recovery boot error	Flashing series of post codes: E9h Eeh Ebh Ech EFh	Unable to boot to floppy, ATAPI, or ATAPI CD-ROM. Recovery process will retry.
Series of long low-pitched single beeps	Recovery failed	EEh	Unable to process valid BIOS recovery images. BIOS already passed control to operating system and flash utility.
2 long high-pitched beeps	Recovery complete	EFh	BIOS recovery succeeded, ready for power-down, reboot.
3	Recovery Failed	F0h	Recovery diskette is not bootable or a recovery diskette is not inserted.

Recovery BIOS will generate two beeps and flash a POST code sequence of E9h, EAh, EBh, ECh, and EFh on the Port 80 diagnostic LEDs.

During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

7.7.11 Bootblock Error Beep Codes

Table 28. Bootblock Error Beep Codes

Beep Code	Error message	Description
1	Refresh timer failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity error	Parity can not be reset
3	Boot Block Failure	Boot Block Failure failure. **See “3-Beep-Boot Block Failure Error Code” table for additional error details.
4	System timer	System timer is not operational
5	Processor failure	Processor failure detected
6	Keyboard controller Gate A20 failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor exception interrupt error	The CPU generated an exception interrupt.
8	Display memory read/write error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.

Beep Code	Error message	Description
9	ROM checksum error	System BIOS ROM checksum error
10	Shutdown register error	Shutdown cmos register read/write error detected
11	Invalid BIOS	General BIOS ROM error

Table 29. 3-Beep Boot Block Failure Error Codes

Beep Code	POST Code	Description
3	00h	No memory was found in the system
3	01h	Memory mixed type detected
3	02h	EDO is not supported
3	03h	First row memory test failure
3	04h	Mismatched DIMMs in a row
3	05h	Base memory test failure
3	06h	Failure on decompressing post module
3	07h-0Dh	Generic memory error
3	0Eh	SMBUS protocol error
3	0Fh	Generic memory error
3	DDh	CPU microcode cannot be found for processor in slot 0.
3	EEh	CPU microcode cannot be found for processor in slot 1.

7.8 Temperature Sensors

The server board SE7501HG2 can measure the system and board temperatures from a variety of sources. The first is located inside the Heceta chip (U5F1) and is used to measure the baseboard temperature. Diodes located inside each processor are used by the SE7501HG2 to monitor the temperature at the processors.

When the SE7501HG2 board set is installed in the Intel® SC5200 server chassis, the server also uses a temperature sensor on the front panel and HSBPs to measure the ambient temperature and will boost the fans depending on the reading it receives from these sensors.

Table 30. Temperature Sensors

Temperature Sensor	Description	Resolution	Accuracy	Location
Server board	Server board temperature sensor, located in the hot-spot selected according to thermal design	8-bit	+/- 3°C or better	U5F1
Primary Processor	Primary processor socket thermal sensor	8-bit	+/- 5°C or better	J8H1
Secondary Processor	Secondary processor socket thermal sensor	8-bit	+/- 5°C or better	J6H1

8. SE7501HG2 ACPI Implementation

8.1 ACPI

An ACPI aware operating system generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by sending the appropriate command to the BMC to enable ACPI mode. The system automatically returns to legacy mode upon hard reset or power-on reset.

The SE7501HG2 platform supports S0, S1, S4, and S5 states. When the system is operating in ACPI mode, the OS retains control of the system and OS policy determines the entry methods and wakeup sources for each sleep state. Sleep entry and wakeup event capabilities are provided by the hardware but are enabled by the operating system.

S0 Sleep State The S0 sleep state is when everything is on. This is the state that no sleep is enabled.

S1 Sleep State The S1 sleep state is a low wake-up latency sleep state. In this state, no system context is lost (processor or chip set). The system context is maintained by the hardware.

S4 Sleep State The S4 Non-Volatile Sleep state (NVS) is a special global system state that allows system context to be saved and restored (relatively slowly) when power is lost to the baseboard. If the system has been commanded to enter the S4 sleep state, the OS will write the system context to a non-volatile storage file and leave appropriate context markers.

S5 Sleep State The S5 sleep state is similar to the S4 sleep state except the operating system does not save any context nor enable any devices to wake the system. The system is in the “soft” off state and requires a complete boot when awakened.

8.1.1 Front Panel Switches

The server board SE7501HG2 supports up to five front panel buttons (via any one of three different front panel interface connectors):

- The power button
- The sleep button
- The reset button
- A system identification button
- An NMI button

The power button input (FP_PWR_BTN*) request is forwarded by the BMC to the power state functions in the National* PC87417 Super I/O chip. The power button state is monitored by the BMC. It does not directly control power on the power supply.

The power button input and the sleep button input (FP_SLP_BTN*) behave differently depending on whether or not the operating system supports ACPI. The sleep button has no effect unless an

operating system with ACPI support is running. If the operating system supports ACPI and the system is running, pressing the sleep switch causes an event. The OS will cause the system to transition to the appropriate system state depending on the user settings. The power button can also be programmed to be a sleep button.

Power/Sleep Button Off to On: The ICH3-S and SIO may be configured to generate wakeup events for several different system events: Wake on LAN*, PCI Power Management Interrupt, and Real Time Clock Alarm are examples of these events. The BMC monitors the power button and wakeup event signals from the ICH3-S. A transition from either source results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The ICH3-S receives power good and reset from the BMC and then transitions to an ON state.

Power/Sleep Button On to Off (Legacy): The BMC monitors power state signals from the ICH-3 and de-asserts the PS_PWR_ON signal to the power supply. As a safety mechanism, the BMC automatically powers off the system in 4-5 seconds.

Power/Sleep Button On to Off (ACPI): If an ACPI operating system is loaded, the power button switch generates a request (via SCI) to the operating system to shutdown the system. The operating system retains control of the system and determines what sleep state (if any) the system transitions to.

Power/Sleep Button On to Sleep (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a request (via SCI) to the operating system to place the system in “sleep” mode. The operating system retains control of the system and determines into which sleep state, if any, the system transitions.

Power/Sleep Button Sleep to On (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a wake event to the ICH3-S and a request (via SCI) to the OS to place the system in the “On” state. The operating system retains control of the system and determines from which sleep state, if any, the system can wake.

Reset Button: The reset button will generate a hard reset to the system.

NMI Button: The NMI button will force an NMI to the BMC, which will generate an NMI to the processor.

System ID Button: The System ID button is used to aid a technician in locating a system for servicing when installed in a rack environment. Pushing the ID button will light the blue ID LED located on the back edge of the baseboard near the speaker and battery. It will also light an LED on a front panel if configured to do so.

8.1.2 Wake up Sources (ACPI and Legacy)

The server board SE7501HG2 is capable of wake up from several sources under a non-ACPI configuration, e.g., when the operating system does not support ACPI. The wake up sources are defined in the following table. Under ACPI, the operating system programs the ICH3-S and SIO to wake up on the desired event, but in legacy mode, the BIOS enables/disables wake up sources based on an option in BIOS Setup. It is required that the operating system or a driver will clear any pending wake up status bits in the associated hardware (such as the Wake on LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device). The legacy wake up feature is disabled by default.

Table 31. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Ring indicate from Serial-A	S1, S4	Yes
Ring indicate from Serial-B	S1, S4 If Serial-B is used for EMP, Serial-B wakeup is disabled.	Yes
PME from PCI cards	S1, S4	Yes
RTC Alarm	S1. Always wakes the system up from S4.	Yes
Mouse	S1	No
Keyboard	S1	No
USB	S1	No

9. SE7501HG2 Connectors

9.1 Main Power Connector

The main power supply connection is obtained using the 24-pin connector. The following table defines the pin-outs of the connector.

Table 32. Power Connector Pin-out (J9C1)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	GND	Black	15	GND	Black
4	+5Vdc	Red	16	PS_ON#	Green
5	GND	Black	17	GND	Black
6	+5Vdc	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR_OK	Gray	20	RSVD_(5V)	White
9	5VSB	Purple	21	+5Vdc	Red
10	+12V Vdc	Yellow	22	+5Vdc	Red
11	+12V Vdc	Yellow	23	+5Vdc	Red
12	+3.3Vdc	Orange	24	GND	Black

Table 33. Power Supply Signal Connector (J9B1)

Pin	Signal	Color
1	5VSB_SCL	Orange
2	5VSB_SDA	Black
3	PS_ALERT_L, Not used	Red
4	3.3V SENSE(-)	Yellow
5	3.3V SENSE(+)	Green

Table 34. 12V Power Connector (J4E1)

Pin	Signal	Color
1	GND	Black
2	GND	Black
3	GND	Black
4	GND	Black
5	+12Vdc	Yellow
6	+12Vdc	Yellow
7	+12Vdc	Yellow
8	+12Vdc	Yellow

9.2 Memory Module Connector

The server board SE7501HG2 has six DDR DIMM connectors and supports registered ECC DDR266 modules. For additional DIMM information, refer to the *DDR-266 Registered DIMM Specification.*

Table 35. DIMM Connectors (J9D1, J8D3, J8D2, J8D1, J7D2, J7D1)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	34	GND	67	DQS5	100	GND	133	DQ31	166	DQ53
2	DQ0	35	DQ25	68	DQ42	101	NC	134	CB4	167	FETEN
3	GND	36	DQS3	69	DQ43	102	NC	135	CB5	168	VDD
4	DQ1	37	A4	70	VDD	103	A13	136	VDDQ	169	DM6
5	DQS0	38	VDD	71	RSVD	104	VDDQ	137	CK0P	170	DQ54
6	DQ2	39	DQ26	72	DQ48	105	DQ12	138	CK0N	171	DQ55
7	VDD	40	DQ27	73	DQ49	106	DQ13	139	GND	172	VDDQ
8	DQ3	41	A2	74	GND	107	DM1	140	DM8	173	NC
9	NC	42	GND	75	RSVD	108	VDD	141	A10	174	DQ60
10	RESET*	43	A1	76	RSVD	109	DQ14	142	CB6	175	DQ61
11	GND	44	CB0	77	VDDQ	110	DQ15	143	VDDQ	176	GND
12	DQ8	45	CB1	78	DQS6	111	CKE1	144	CB7	177	DM7
13	DQ9	46	VDD	79	DQ50	112	VDDQ	145	GND	178	DQ62
14	DQS1	47	DQS8	80	DQ51	113	BA2	146	DQ36	179	DQ63
15	VDDQ	48	A0	81	GND	114	DQ20	147	DQ37	180	VDDQ
16	RSVD	49	CB2	82	VDDID	115	A12	148	VDD	181	SA0
17	RSVD	50	GND	83	DQ56	116	GND	149	DM4	182	SA1
18	GND	51	CB3	84	DQ57	117	DQ21	150	DQ38	183	SA2
19	DQ10	52	BA1	85	VDD	118	A11	151	DQ39	184	VDDSPD
20	DQ11	53	DQ32	86	DQS7	119	DM2	152	GND	185	NC
21	CKE0	54	VDDQ	87	DQ58	120	VDD	153	DQ44	186	NC
22	VDDQ	55	DQ33	88	DQ59	121	DQ22	154	RAS*	187	NC

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
23	DQ16	56	DQS4	89	GND	122	A8	155	DQ45		
24	DQ17	57	DQ34	90	NC	123	DQ23	156	VDDQ		
25	DQS2	58	GND	91	SDA	124	GND	157	CS0*		
26	GND	59	BA0	92	SCL	125	A6	158	CS1*		
27	A9	60	DQ35	93	GND	126	DQ28	159	DM5		
28	DQ18	61	DQ40	94	DQ4	127	DQ29	160	GND		
29	A7	62	VDDQ	95	DQ5	128	VDDQ	161	DQ46		
30	VDDQ	63	WE*	96	VDDQ	129	DM3	162	DQ47		
31	DQ19	64	DQ41	97	DM0	130	A3	163	RSVD		
32	A5	65	CAS*	98	DQ6	131	DQ30	164	VDDQ		
33	DQ24	66	GND	99	DQ7	132	GND	165	DQ52		

9.3 Processor Socket

The SE7501HG2 has two Socket 604 processor sockets. The following table provides the processor socket pin numbers and pin names:

Table 36. Socket 604 Processor Socket Pin-out (J6H1, J8H1)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	Reserved	B6	VCC	C11	A30#	D16	A17#	E21	RS0#
A2	VCC	B7	A31#	C12	A23#	D17	A9#	E22	HIT#
A3	SKTOCC#	B8	A27#	C13	VSS	D18	VCC	E23	VSS
A4	VCCVID	B9	VSS	C14	A16#	D19	ADS#	E24	TCK
A5	VSS	B10	A21#	C15	A15#	D20	BREQ1#	E25	TDO
A6	A32#	B11	A22#	C16	VCC	D21	VSS	E26	VCC
A7	A33#	B12	VCC	C17	A8#	D22	RS1#	E27	FERR#
A8	VCC	B13	A13#	C18	A6#	D23	BPRI#	E28	VCC
A9	A26#	B14	A12#	C19	VSS	D24	VCC	E29	VSS
A10	A20#	B15	VSS	C20	REQ[3]#	D25	Reserved	E30	VCC
A11	VSS	B16	A11#	C21	REQ[2]#	D26	VSSENSE	E31	VSS
A12	A14#	B17	VSS	C22	VCC	D27	VSS	F1	VCC
A13	A10#	B18	A5#	C23	DEFER#	D28	VSS	F2	VSS
A14	VCC	B19	REQ[0]#	C24	TDI	D29	VCC	F3	VID0
A15	FRCEPR#	B20	VCC	C25	VSS	D30	VSS	F4	VCC
A16	Reserved	B21	REQ[1]#	C26	IGNNE#	D31	VCC	F5	BPM3#
A17	LOCK#	B22	REQ[4]#	C27	SMI#	E1	VSS	F6	BPM0#
A18	VCC	B23	VSS	C28	VCC	E2	VCC	F7	VSS
A19	A7#	B24	INTR	C29	VSS	E3	VID1	F8	BPM1#
A20	A4#	B25	PROCHOT#	C30	VCC	E4	BPM5#	F9	GTLREF
A21	VSS	B26	VCC	C31	VSS	E5	IERR#	F10	VCC
A22	A3#	B27	VCCSENSE	D1	VCC	E6	VCC	F11	BINIT#
A23	HITM#	B28	VSS	D2	VSS	E7	BPM2#	F12	BREQ0#

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A24	VCC	B29	VCC	D3	VID2	E8	BPM4#	F13	VSS
A25	TMS	B30	VSS	D4	STPCLK#	E9	VSS	F14	ADSTB1#
A26	Reserved	B31	VCC	D5	VSS	E10	AP0#	F15	A19#
A27	VSS	C1	TESTLOW	D6	INIT#	E11	BR2#[1]	F16	VCC
A28	VCC	C2	VCC	D7	MCERR#	E12	VCC	F17	ADSTB0#
A29	VSS	C3	VID3	D8	VCC	E13	A28#	F18	DBSY#
A30	VCC	C4	VCC	D9	AP1#	E14	A24#	F19	VSS
A31	VSS	C5	VCCVID	D10	BR3#[1]	E15	VSS	F20	BNR#
B1	Reserved	C6	RSP#	D11	VSS	E16	COMP1	F21	RS2#
B2	VSS	C7	VSS	D12	A29#	E17	VSS	F22	VCC
B3	VID4	C8	A35#	D13	A25#	E18	DRDY#	F23	GTLREF
B4	VCC	C9	A34#	D14	VCC	E19	TRDY#	F24	TRST#
B5	OTDEN	C10	VCC	D15	A18#	E20	VCC	F25	VSS
F26	THERMTRIP#	J3	VSS	L24	VCC	P1	VSS	T9	VSS
F27	A20M#	J4	VCC	L25	VSS	P2	VCC	T23	VSS
F28	VSS	J5	VSS	L26	VCC	P3	VSS	T24	VCC
F29	VCC	J6	VCC	L27	VSS	P4	VCC	T25	VSS
F30	VSS	J7	VSS	L28	VCC	P5	VSS	T26	VCC
F31	VCC	J8	VCC	L29	VSS	P6	VCC	T27	VSS
G1	VSS	J9	VSS	L30	VCC	P7	VSS	T28	VCC
G2	VCC	J23	VSS	L31	VSS	P8	VCC	T29	VSS
G3	VSS	J24	VCC	M1	VCC	P9	VSS	T30	VCC
G4	VCC	J25	VSS	M2	VSS	P23	VSS	T31	VSS
G5	VSS	J26	VCC	M3	VCC	P24	VCC	U1	VCC
G6	VCC	J27	VSS	M4	VSS	P25	VSS	U2	VSS
G7	BOOT_SEL	J28	VCC	M5	VCC	P26	VCC	U3	VCC
G8	VCC	J29	VSS	M6	VSS	P27	VSS	U4	VSS
G9	VSS	J30	VCC	M7	VCC	P28	VCC	U5	VCC
G23	NMI	J31	VSS	M8	VSS	P29	VSS	U6	VSS
G24	VCC	K1	VCC	M9	VCC	P30	VCC	U7	VCC
G25	VSS	K2	VSS	M23	VCC	P31	VSS	U8	VSS
G26	VCC	K3	VCC	M24	VSS	R1	VCC	U9	VCC
G27	VSS	K4	VSS	M25	VCC	R2	VSS	U23	VCC
G28	VCC	K5	VCC	M26	VSS	R3	VCC	U24	VSS
G29	VSS	K6	VSS	M27	VCC	R4	VSS	U25	VCC
G30	VCC	K7	VCC	M28	VSS	R5	VCC	U26	VSS
G31	VSS	K8	VSS	M29	VCC	R6	VSS	U27	VCC
H1	VCC	K9	VCC	M30	VSS	R7	VCC	U28	VSS
H2	VSS	K23	VCC	M31	VCC	R8	VSS	U29	VCC
H3	VCC	K24	VSS	N1	VCC	R9	VCC	U30	VSS
H4	VSS	K25	VCC	N2	VSS	R23	VCC	U31	VCC
H5	VCC	K26	VSS	N3	VCC	R24	VSS	V1	VSS
H6	VSS	K27	VCC	N4	VSS	R25	VCC	V2	VCC
H7	VCC	K28	VSS	N5	VCC	R26	VSS	V3	VSS
H8	VSS	K29	VCC	N6	VSS	R27	VCC	V4	VCC

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
H9	VCC	K30	VSS	N7	VCC	R28	VSS	V5	VSS
H23	VCC	K31	VCC	N8	VSS	R29	VCC	V6	VCC
H24	VSS	L1	VSS	N9	VCC	R30	VSS	V7	VSS
H25	VCC	L2	VCC	N23	VCC	R31	VCC	V8	VCC
H26	VSS	L3	VSS	N24	VSS	T1	VSS	V9	VSS
H27	VCC	L4	VCC	N25	VCC	T2	VCC	V23	VSS
H28	VSS	L5	VSS	N26	VSS	T3	VSS	V24	VCC
H29	VCC	L6	VCC	N27	VCC	T4	VCC	V25	VSS
H30	VSS	L7	VSS	N28	VSS	T5	VSS	V26	VCC
H31	VCC	L8	VCC	N29	VCC	T6	VCC	V27	VSS
J1	VSS	L9	VSS	N30	VSS	T7	VSS	V28	VCC
J2	VCC	L23	VSS	N31	VCC	T8	VCC	V29	VSS
V30	VCC	Y22	VCC	AB1	VSS	AC11	D43#	AD21	D29#
V31	VSS	Y23	D5#	AB2	VCC	AC12	D41#	AD22	DBI1#
W1	VCC	Y24	D2#	AB3	BSEL1[2]	AC13	VSS	AD23	VSS
W2	VSS	Y25	VSS	AB4	VCCA	AC14	D50#	AD24	D21#
W3	Reserved	Y26	D0#	AB5	VSS	AC15	DP2#	AD25	D18#
W4	VSS	Y27	THERMDA	AB6	D63#	AC16	VCC	AD26	VCC
W5	BCLK1	Y28	THERMDC	AB7	PWRGOOD	AC17	D34#	AD27	D4#
W6	TESTHI0	Y29	SM_TS1_A1	AB8	VCC	AC18	DP0#	AD28	SM_ALERT#
W7	TESTHI1	Y30	VSS	AB9	DBI3#	AC19	VSS	AD29	SM_WP
W8	TESTHI2	Y31	VSS	AB10	D55#	AC20	D25#	AD30	VCC
W9	GTLREF	AA1	VCC	AB11	VSS	AC21	D26#	AD31	VSS
W23	GTLREF	AA2	VSS	AB12	D51#	AC22	VCC	AE2	VSS
W24	VSS	AA3	BSEL0[2]	AB13	D52#	AC23	D23#	AE3	VCC
W25	VCC	AA4	VCC	AB14	VCC	AC24	D20#	AE4	Reserved
W26	VSS	AA5	VSSA	AB15	D37#	AC25	VSS	AE5	TESTHI6
W27	VCC	AA6	VCC	AB16	D32#	AC26	D17#	AE6	SLP#
W28	VSS	AA7	TESTHI4	AB17	D31#	AC27	DBI0#	AE7	D58#
W29	VCC	AA8	D61#	AB18	VCC	AC28	SM_CLK	AE8	VCC
W30	VSS	AA9	VSS	AB19	D14#	AC29	SM_DAT	AE9	D44#
W31	VCC	AA10	D54#	AB20	D12#	AC30	SLEW_CTRL	AE10	D42#
Y1	VSS	AA11	D53#	AB21	VSS	AC31	VCC	AE11	VSS
Y2	VCC	AA12	VCC	AB22	D13#	AD1	Reserved	AE12	DBI2#
Y3	Reserved	AA13	D48#	AB23	D9#	AD2	VCC	AE13	D35#
Y4	BCLK0	AA14	D49#	AB24	VCC	AD3	VSS	AE14	VCC
Y5	VSS	AA15	VSS	AB25	D8#	AD4	VCCIOPLL	AE15	Reserved
Y6	TESTHI3	AA16	D33#	AB26	D7#	AD5	TESTHI5	AE16	Reserved
Y7	VSS	AA17	VSS	AB27	VSS	AD6	VCC	AE17	DP3#
Y8	RESET#	AA18	D24#	AB28	3.3V_STBY	AD7	D57#	AE18	VCC
Y9	D62#	AA19	D15#	AB29	3.3V_STBY	AD8	D46#	AE19	DP1#
Y10	VCC	AA20	VCC	AB30	VCC	AD9	VSS	AE20	D28#
Y11	DSTBP3#	AA21	D11#	AB31	VSS	AD10	D45#	AE21	VSS
Y12	DSTBN3#	AA22	D10#	AC1	Reserved	AD11	D40#	AE22	D27#
Y13	VSS	AA23	VSS	AC2	VSS	AD12	VCC	AE23	D22#

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
Y14	DSTBP2#	AA24	D6#	AC3	VCC	AD13	D38#	AE24	VCC
Y15	DSTBN2#	AA25	D3#	AC4	VCC	AD14	D39#	AE25	D19#
Y16	VCC	AA26	VCC	AC5	D60#	AD15	VSS	AE26	D16#
Y17	DSTBP1#	AA27	D1#	AC6	D59#	AD16	COMP0	AE27	VSS
Y18	DSTBN1#	AA28	3.3V_STBY	AC7	VSS	AD17	VSS	AE28	3.3V_STBY
Y19	VSS	AA29	3.3V_STBY	AC8	D56#	AD18	D36#	AE29	3.3V_STBY
Y20	DSTBP0#	AA30	VSS	AC9	D47#	AD19	D30#		
Y21	DSTBN0#	AA31	VCC	AC10	VCC	AD20	VCC		

Notes:

a. These are “Reserved” pins on the Intel® Xeon™ processor. In systems utilizing the Intel® Xeon™ processor, the system designer must terminate these signals to the processor Vcc.

b. Base boards treating AA3 and AB3 as Reserved will operate correctly with a bus clock of 100 MHz.

9.4 System Management Headers

9.4.1 ICMB Header

Table 37. ICMB Header Pin-out (J1A1)

Pin	Signal Name	Type	Description
1	5 V standby	Power	+5 V Standby
2	Transmit	Signal	UART signals
3	Transmit Enable	Signal	UART signals
4	Receive	Signal	UART signals
5	Ground	GND	

9.4.2 OEM IPMB Header

Table 38. IPMB Header Pin-out (J4K6)

Pin	Signal Name	Description
1	Local I2C SDA	BMC IMB 5 V Standby Clock Line
2	GND	
3	Local I2C SCL	BMC IMB 5 V Standby Data Line

9.4.3 SCSI IPMB Header

Table 39. IPMB Header Pin-out (J4J2, J4K1)

Pin	Signal Name	Description
1	5VSB SDA	Data Line
2	GND	
3	5VSB SCL	Clock Line
4	Not used	

9.5 PCI Slot Connector

There are three peer PCI buses implemented on the SE7501HG2 board. Segment A supports 5V PCI 32-bit/33MHz, segment B supports 3.3V PCI-X 64-bit/100/66MHz, and segment C supports 3.3V PCI-X 64-bit/133/100/66MHz operation. All segments support full-length PCI add-in cards. The following tables list the characteristics and pin-outs for the PCI slots.

Table 40. PCI Slot Characteristics

Slot No.	Mode	Width	Speed	Voltage	Notes
1	PCI-X	64-bit	133MHz	3.3V	
2	PCI-X	64-bit	100MHz	3.3V	Supports ZCR (Zero Channel RAID)
3	PCI-X	64-bit	100MHz	3.3V	
4	PCI	32-bit	33MHz	5V	
5	PCI	32-bit	33MHz	5V	
6	PCI	32-bit	33MHz	5V	

Table 41. Slot 1 PCI-X 64-bit 3.3V Pin-out (J4D1)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	TCK	+12 V	50	Ground	Ground
3	Ground	TMS	51	Ground	Ground
4	TDO	TDI	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	REQ[3]#	57	Ground	AD[02]
10	GNT[2]#	+3.3 V	58	AD[01]	AD[00]
11	PRSNT2#	GNT[3]#	59	+3.3 V	+3.3 V
12	**Connector Key**	**Connector Key**	60	ACK64#	REQ64#

Pin	Side B	Side A	Pin	Side B	Side A
13	**Connector Key**	**Connector Key**	61	+5 V	+5 V
14	REQ[2]#	3.3 VAUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+3.3 V		**Connector Key**	**Connector Key**
17	Ground	GNT[1]#	63	CLK	Ground
18	REQ[1]#	Ground	64	Ground	C/BE[7]#
19	+3.3 V	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+3.3 V
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+3.3 V	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+3.3 V
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+3.3 V	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	PCIXCAP	STOP#	84	AD[41]	+3.3 V
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+3.3 V	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	IRQB[8]	IRQB[9]
47	AD[12]	AD[11]	93	RISER_PRESENCE_L	GND
48	AD[10]	Ground	94	Ground	CLK

Table 42. Slot 2 PCI-X 64-bit 3.3V ZCR(Zero Channel RAID) Pin-out (J3D2)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	TCK	+12 V	50	Ground	Ground
3	Ground	TMS(PA_TMS)	51	Ground	Ground
4	TDO	ROMB_PRESENT_L	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	RSV	57	Ground	AD[02]
10	RSV	+3.3 V	58	AD[01]	AD[00]
11	PRSNT2#	RSV	59	+3.3 V	+3.3 V
12	**Connector Key**	**Connector Key**	60	ACK64#	REQ64#
13	**Connector Key**	**Connector Key**	61	+5 V	+5 V
14	RSV	3.3 VAUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+3.3 V		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	RSV	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#
19	+3.3 V	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+3.3 V
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+3.3 V	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+3.3 V
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+3.3 V	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+3.3 V
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+3.3 V	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]

Pin	Side B	Side A	Pin	Side B	Side A
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	RSV	RSV
47	AD[12]	AD[11]	93	RSV	GND
48	AD[10]	Ground	94	Ground	RSV

Table 43. Slot 3 PCI-X 64-bit3.3V Pin-out (J3D1)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	TCK	+12 V	50	Ground	Ground
3	Ground	TMS	51	Ground	Ground
4	TDO	TDI	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	RSV	57	Ground	AD[02]
10	RSV	+3.3 V	58	AD[01]	AD[00]
11	PRSNT2#	RSV	59	+3.3 V	+3.3 V
12	**Connector Key**	**Connector Key**	60	ACK64#	REQ64#
13	**Connector Key**	**Connector Key**	61	+5 V	+5 V
14	RSV	3.3 VAUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+3.3 V		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	RSV	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#
19	+3.3 V	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+3.3 V
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+3.3 V	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+3.3 V
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+3.3 V	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground

Pin	Side B	Side A	Pin	Side B	Side A
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+3.3 V
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+3.3 V	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	RSV	RSV
47	AD[12]	AD[11]	93	RSV	GND
48	AD[10]	Ground	94	Ground	RSV

Table 44. Slots 4, 5 and 6 32-bit 5V Pin-out (J2C2, J2C1, J1C4)

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	32	AD[17]	AD[16]
2	TCK	+12 V	33	C/BE[2]#	+3.3 V
3	Ground	TMS	34	Ground	FRAME#
4	TDO	TDI	35	IRDY#	Ground
5	+5 V	+5 V	36	+3.3 V	TRDY#
6	+5 V	INTA#	37	DEVSEL#	Ground
7	INTB#	INTC#	38	Ground	STOP#
8	INTD#	+5 V	39	LOCK#	+3.3 V
9	PRSNT1#	RSV	40	PERR#	SMBUS CLK
10	RSV	+5 V (I/O)	41	+3.3 V	SMBUS DAT
11	PRSNT2#	RSV	42	SERR#	Ground
12	Ground	Ground	43	+3.3 V	PAR
13	Ground	Ground	44	C/BE[1]#	AD[15]
14	RSV	3.3 VSB	45	AD[14]	+3.3 V
15	Ground	RST#	46	Ground	AD[13]
16	CLK	+5 V (I/O)	47	AD[12]	AD[11]
17	Ground	GNT#	48	AD[10]	Ground
18	REQ#	Ground	49	Ground	AD[09]
19	+5 V	PME#	50	**Connector Key**	**Connector Key**
20	AD[31]	AD[30]	51	**Connector Key**	**Connector Key**
21	AD[29]	+3.3 V	52	AD[08]	C/BE[0]#
22	Ground	AD[28]	53	AD[07]	+3.3 V
23	AD[27]	AD[26]	54	+3.3 V	AD[06]
24	AD[25]	Ground	55	AD[05]	AD[04]
25	+3.3 V	AD[24]	56	AD[03]	Ground
26	C/BE[3]#	IDSEL	57	Ground	AD[02]
27	AD[23]	+3.3 V	58	AD[01]	AD[00]

Pin	Side B	Side A	Pin	Side B	Side A
28	Ground	AD[22]	59	+5 V	+5 V (I/O)
29	AD[21]	AD[20]	60	ACK64#	REQ64#
30	AD[19]	Ground	61	+5 V	+5 V
31	+3.3 V	AD[18]	62	+5 V	+5 V

9.6 Front Panel Connectors

34-pin header (J1J2) is provided to support a system front panel. The headers contain reset, NMI, power control buttons, and LED indicators. The following tables detail the pin-outs of the headers.

Table 45. Front Panel 34-Pin Header Pin-out (J1J2)

Pin	Signal Name	Pin	Signal Name
1	Power LED Anode	2	5VSB
3	Key	4	Fan Fail LED Anode
5	Power LED Cathode	6	Fan Fail LED Cathode
7	HDD Activity LED Anode	8	Power Fault LED Anode
9	HDD Activity LED Cathode	10	Power Fault LED Cathode
11	Power Switch	12	NIC#1 Activity LED Anode
13	GND (Power Switch)	14	NIC#1 Activity LED Cathode
15	Reset Switch	16	I2C SDA
17	GND (Reset Switch)	18	I2C SCL
19	ACPI Sleep Switch	20	Chassis Intrusion
21	GND (ACPI Sleep Switch)	22	NIC#2 Activity LED Anode
23	NMI to CPU Switch	24	NIC#2 Activity LED Cathode
25	KEY	26	Key
27	ID LED Anode	28	System Ready Anode
29	ID LED Cathode	30	System Ready Cathode
31	ID Switch	32	HDD Fault Anode
33	GND (ID Switch)	34	HDD Fault Cathode

9.6.1 VGA Connector

The following table details the pin-out of the VGA connector.

Table 46. VGA Connector Pin-out (J7A1)

Pin	Signal Name
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	No connection
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

9.6.2 SCSI Connectors

The server board SE7501HG2 provides two internal wide SCSI connectors. The following table details the pin-out of the SCSI connector.

Table 47. 68-Pin SCSI Connector Pin-out (J1D1, J1F1)

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
1	+DB(12)	-DB(12)	35
2	+DB(13)	-DB(13)	36
3	+DB(14)	-DB(14)	37
4	+DB(15)	-DB(15)	38
5	+DB(P1)	-DB(P1)	39
6	+DB(0)	-DB(0)	40
7	+DB(1)	-DB(1)	41
8	+DB(2)	-DB(2)	42
9	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
14	+DB(P)	-DB(P)	48
15	GROUND	GROUND	49
16	DIFFSENSE	GROUND	50
17	TERMPWR	TERMPWR	51
18	TERMPWR	TERMPWR	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57
24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

9.6.3 NIC Connectors

The server board SE7501HG2 supports a dual stacked RJ45 connector. It supports dual gigabit Ethernet channels and includes magnetics. The following table details the pin-out of the connector.

Table 48. Dual NIC Stacked RJ45 Connector Pin-out (J5A2)

Pin	Signal Name	Pin	Signal Name
1	CHGND	2	NICB_MDI3M
3	NICB_MDI2P	4	P2V5_NICB
5	NICB_MDI1M	6	NICB_MDI0P
7	P2V5_NICB	8	NICB_MDI3P
9	P2V5_NICB	10	NICB_MDI2M
11	NICB_MDI1P	12	P2V5_NICB
13	NICB_MDI0M	14	P2V5_NICA
15	NICA_MDI0P	16	NICA_MDI1M
17	P2V5_NICA	18	NICA_MDI2P
19	NICA_MDI3M	20	CHGND
21	NICA_MDI0M	22	P2V5_NICA
23	NICA_MDI1P	24	NICA_MDI2M
25	P2V5_NICA	26	NICA_MDI3P

Pin	Signal Name	Pin	Signal Name
27	NICA_LINK_LED_L	28	NICA_ACT_LED_L
29	NICA_LINK100_LED_L	30	NICA_LINK1000_LED_L
31	NICB_LINK_LED_L	32	NICB_ACT_LED_L
33	NICB_LINK100_LED_L	34	NICB_LINK1000_LED_L

9.6.4 ATA Connectors

The ATA-100 SE7501HG2 board provides two 40-pin low-density ATA-100 connectors. The pin-outs for both connectors are identical and are listed in the following table.

Table 49. ATA-100 40-Pin Connectors Pin-out (J1J4, J2J2)

Pin	Signal Name	Pin	Signal Name
1	RESET_L	2	GND
3	DD7	4	IDE_DD8
5	DD6	6	IDE_DD9
7	DD5	8	IDE_DD10
9	DD4	10	IDE_DD11
11	DD3	12	IDE_DD12
13	DD2	14	IDE_DD13
15	DD1	16	IDE_DD14
17	DD0	18	IDE_DD15
19	GND	20	KEY
21	IDE_DMAREQ	22	GND
23	IDE_IOW_L	24	GND
25	IDE_IOR_L	26	GND
27	IDE_IORDY	28	GND
29	IDE_DMAACK_L	30	GND
31	IRQ_IDE	32	Test Point
33	IDE_A1	34	DIAG
35	IDE_A0	36	IDE_A2
37	IDE_DCS0_L	38	IDE_DCS1_L
39	IDE_HD_ACT_L	40	GND

9.6.5 USB Connector

The server board SE7501HG2 supports one stacked triple USB connector. The following table details the pin-out of the connector.

Table 50. USB Connectors Pin-out (J9A2)

Pin	Signal Name
1	USB_PWR<0> (Fused 5 V)
2	USB_BCK0_L
3	USB_BCK0
4	GND
5	USB_PWR<1> (Fused 5 V)
6	USB_BCK1_L
7	USB_BCK1
8	GND
9	USB_PWR<2> (Fused 5 V)
10	USB_BCK2_L
11	USB_BCK2
12	GND

A header on the server board provides an option to support an additional USB connector. The pin-out of the header is detailed in the following table.

Table 51. Optional USB Connection Header Pin-out (J4J1)

Pin	Signal Name	Description
1	USB_PWR<5>	USB Port 5 Power
2	USB_PWR<4>	USB Port 4 Power
3	USB_BCK5_L	USB Port 5 Negative Signal
4	USB_BCK4_L	USB Port 4 Negative Signal
5	USB_BCK5	USB Port 5 Positive Signal
6	USB_BCK4	USB Port 4 Positive Signal
7	Ground	
8	Ground	
9	No Connect	KEY
10	TP_USB_OVRCUR3_L	Front Panel USB Overcurrent signal. This signal is not used

9.6.6 Floppy Connector

The server board SE7501HG2 provides a standard 34-pin interface to the floppy drive controller. The following table details the pin-out of the 34-pin legacy floppy connector.

Table 52. Legacy 34-Pin Floppy Connector Pin-out (J4J3)

Pin	Signal Name	Pin	Signal Name
1	GND	2	FD_DENSEL0
3	GND	4	Test Point
5	KEY	6	FD_DENSEL1
7	GND	8	FD_INDEX_L
9	GND	10	FD_MTR0_L
11	GND	12	FD_DS1_L
13	GND	14	FD_DS0_L
15	GND	16	FD_MTR1_L
17	Test Point	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	Test Point	28	VCC
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

9.6.7 Serial Port Connector

The SE7501HG2 supports two serial ports:

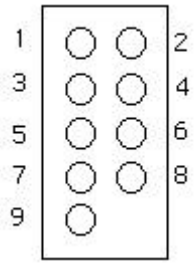
- A DB-9 connector is located on the rear side of the baseboard to supply Serial A.
- A Serial B port is provided through a 9-pin header on the server board.

The following tables detail the pin-outs of these two ports.

Table 53. Rear DB-9 Serial A Port Pin-out (J8A1)

Pin	Signal Name	Description
7	RTS	Request To Send
4	DTR	Data Terminal Ready
3	TD	Transmit Data
5	SGND	Signal Ground
9	RI	Ring Indicate
2	RD	Receive Data
1	DCD	Carrier Detect
8	CTS	Clear to send
6	DSR	Data Set Ready

Table 54. 9-Pin Header Serial B Port Pin-out (J1B1)

Pin	Signal Name	Description	COM2 Pin-out
1	DCD	Carrier Detect	
2	DSR	Data Set Ready	
3	RD	Receive Data	
4	RTS	Request To Send	
5	TD	Transmit Data	
6	CTS	Clear To Send	
7	DTR	Data Terminal Ready	
8	RI	Ring Indicator	
9	SGND	Signal Ground	

9.6.8 Parallel Port

The SE7501HG2 supports one DB-25 parallel port connector provided on the rear I/O. The following table details the pin-out of the connector.

Table 55. DB-25 Parallel Port Pin-out (J7A2)

Pin	Signal Name	Pin	Signal Name
1	STROBE_L	2	DATA0
3	DATA1	4	DATA2
5	DATA3	6	DATA4
7	DATA5	8	DATA6
9	DATA7	10	ACK_L
11	BUSY	12	PAPER_END
13	SELECT	14	AUTOFD_L
15	ERROR_L	16	INIT_L
17	SLCT_INPUT_L	18	GND
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	GND		

9.6.9 Keyboard and Mouse Connector

Two PS/2 ports are provided for keyboard and mouse and share a common housing. The top one is labeled “mouse” and the bottom one is labeled “keyboard,” although the board set supports swapping these connections. The following table details the pin-out of the PS/2 connectors.

Table 56. Keyboard and Mouse PS2 Connector Pin-out (J9A1)

Keyboard		Mouse	
Pin	**Signal Name**	**Pin**	**Signal Name**
1	KBDATA	1	MSDATA
2	N/C	2	N/C
3	GND	3	GND
4	Fused 5V	4	Fused 5V
5	KBCLK	5	MSCLK
6	N/C	6	N/C

9.7 Miscellaneous Headers

9.7.1 Fan Headers

The server board SE7501HG2 provides seven 3-pin fan headers. The fans are labeled Sys Fan1 through Sys Fan 5, CPU1 Fan, and CPU2 Fan. The CPU1 Fan and CPU2 Fan are not variable speed fan headers; both CPU fans use direct 12 volts for full speed operation.

Note: The CPU fan headers will only support fan types that do not require controlled speed, such as those used on CPU fan heat sinks.

Headers for system fans are labeled: Sys Fan1, Sys Fan2, Sys Fan3, Sys Fan4, and Sys Fan5. These headers provide variable speed fan control and will support variable speed fans. Each of the six system fans has a two-pin header for support of the Hot-swap Fan feature (which are “Fan Presence” and “LED”).

Table 57. 3-Pin Fan Headers Pin-out (J5A1, J4A1, J4K4, J4K2, J2K4, J2K1, J7F1, J5F1)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Variable Speed Fan Power (except CPU fans, straight 12V)
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Table 58. 2-Pin Hot-Swap Fan Optional Headers Pin-out (J5B1, J4B1, J4K5, J4K3, J2K5, J2K2)

Pin	Signal Name	Type	Description
1	PRESENCE	In	Fan Presence detect pin
2	LEDPWR	Power	Hot-Swap Fan LED power

10. Configuration Jumpers

This section describes configuration jumper options on the server board.

10.1 System Recovery and Update Jumpers

The SE7501HG2 server board provides two jumper blocks. One 11-pin single in-line header (J1H1), located on the edge of the baseboard next to the Front Panel connector, provides a total of three 3-pin jumper blocks that are used to configure several system recovery and update options. The second 3-pin header (J1J1) provides one 3-pin jumper block that is used to configure BMC recovery options. The following figure shows the factory default locations for each jumper option.

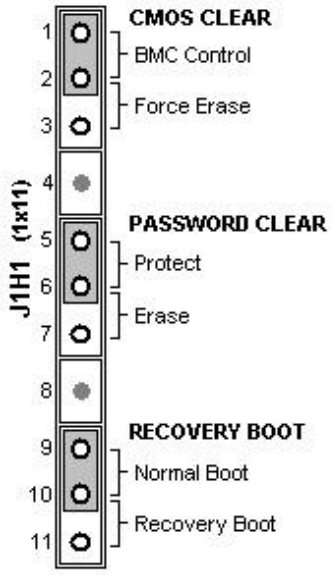


Figure 13. Intel® Server Board SE7501HG2 Configuration Jumpers (J1H1)

The following table describes each jumper option.

Table 59. Configuration Jumper Options

Option	Description
CMOS Clear	If pins 1 and 2 are jumpered (default), preservation of configuration CMOS through system reset is controlled by the BMC. If pins 2 and 3 are jumpered, CMOS contents are set to manufacturing default during system reset.
Password Clear	If pins 5 and 6 are jumpered (default), the current BIOS Setup Utility passwords are maintained during system reset. If pins 6 and 7 are jumpered, the Administrator and user passwords are cleared on reset.
Recovery Boot	If pins 9 and 10 are jumpered (default) the system will attempt to boot using the BIOS programmed in the Flash memory. If pins 10 and 11 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted.

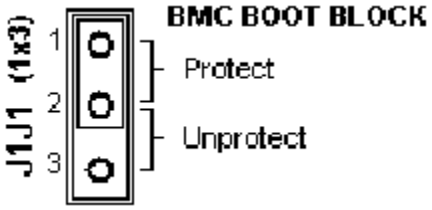


Figure 14. Intel® Server Board SE7501HG2 BMC Configuration Jumpers (J1J1)

The following table describes each jumper option.

Table 60. BMC Configuration Jumper Options

Option	Description
BMC Boot Block	If pins 1 and 2 are jumpered (default) the BMC will write-protect the BMC Flash. If pins 2 and 3 are jumpered, the BMC will unlock the boot block for update.

11. Power Information

11.1 Absolute Maximun Ratings

Operating the server board SE7501HG2 at conditions beyond those shown in the following table may cause permanent damage to the system. This table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 61. Absolute Maximum Ratings

Operating Temperature	5 degrees C to 50 degrees C [1]
Storage Temperature	-55 degrees C to +150 degrees C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V [2]
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:

1. Chassis design must provide proper airflow to avoid exceeding Intel® Xeon™ case temperature.
2. VDD means supply voltage for the device

11.2 SE7501HG2 Power Budget

The following table shows the power consumed on each supply line for a server board SE7501HG2 that is configured with two processors (each 30W max), >1GHz FMB @ 75% usage. This configuration includes four DIMMs stacked burst, 70% max. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at higher than average stress levels.

Table 62. Intel® Server Board SE7501HG2 Power Budget

SE7501HG2	3.3V	5.V	12.V	5.VSB	
Processors			15.47		
Memory/Keyboard/Mouse		0.50A	7.02A		
Server Board	2.97A	1.99A	2.20A	1.81A	
Fans			4.16A		
Hard Drives		8.00A	12.50A		
PCI Slots	9.09A	6.00A			
Peripherals		0.90A	1.10A		
Total Current	12.06A	17.39A	42.45A	1.81A	**Total Power**
Total Power	39.80W	86.95W	509.40W	9.05W	645.34W

11.3 Power Supply Specifications

This section provides power supply design guidelines for the SE7501HG2-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 63. Intel® Server Board SE7501HG2 Static Power Supply Voltage Specification

Parameter	Min	Nom	Max	Units	Tolerance
+3.3 V	+3.25	+3.30	+3.35	V_{rms}	+1.5/-1.5%
+5 V	+4.90	+5.00	+5.10	V_{rms}	+2/-2%
+12 V	+11.76	+12.00	+12.24	V_{rms}	+2/-2%
-12 V	-11.40	-12.20	-13.08	V_{rms}	+9/-5%
+5 VSB	+4.85	+5.00	+5.20	V_{rms}	+4/-3%

Table 64. Intel® Server Board SE7501HG2 Dynamic Power Supply Voltage Specification

Output	Min	Max	Tolerance
+3.3 V	3.20 V	3.46 V	+5 / -3 %
+5 V	4.80 V	5.25 V	+5 / -4 %
+12 V	11.52 V	12.6 V	+5 / -4 %
+5 V SB	4.80 V	5.25 V	+5/ -4%

11.3.1 Power Timing

This section discusses the timing requirements for operation with a single power supply. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 ms to 70 ms. The +3.3 V, +5 V and +12 V output voltages start to rise approximately at the same time. All outputs must rise monotonically. The +5 V output must be greater than the +3.3 V output during any point of the voltage rise, however, never by more than 2.25 V. Each output voltage shall reach regulation within 50 ms (T_{vout_on}) of each other and begin to turn off within 400 ms (T_{vout_off}) of each other. The following figure shows the output voltage timing parameters.

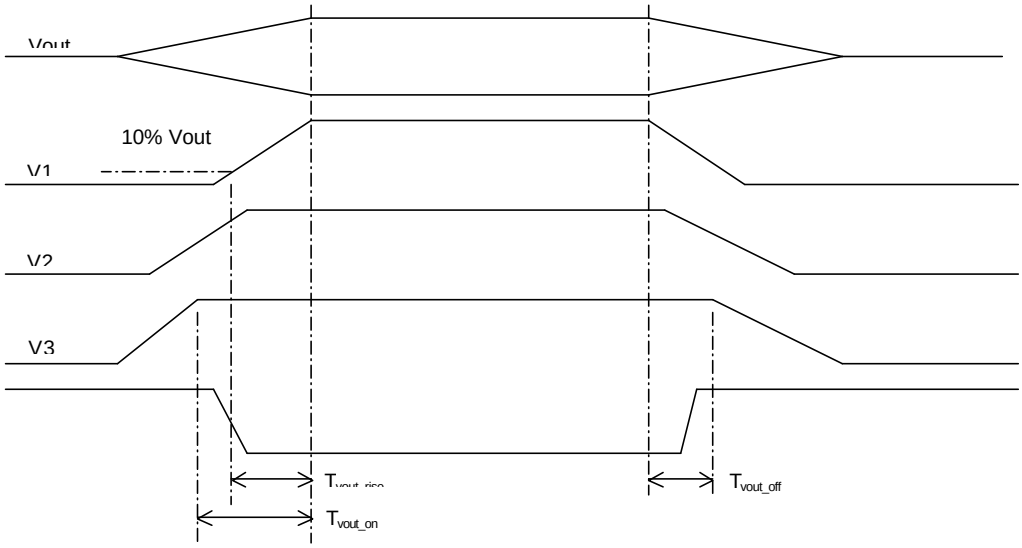


Figure 15. Output Voltage Timing

The following tables show the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The ACOK# signal is not being used to enable the turn on timing of the power supply.

Table 65. Voltage Timing Parameters

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	70	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

Table 66. Turn On/Off Timing

Item	Description	Min	Max	Units
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation.		1500	msec
T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	msec
Tvout_holdup	Time all output voltages stay within regulation after loss of AC.	21		msec
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK	20		msec
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T pson_pwok	Delay from PSON# deactive to PWOK being de-asserted.		50	msec
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T pwok_off	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	2		msec
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
Tsb_vout	Delay from 5 V SB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec

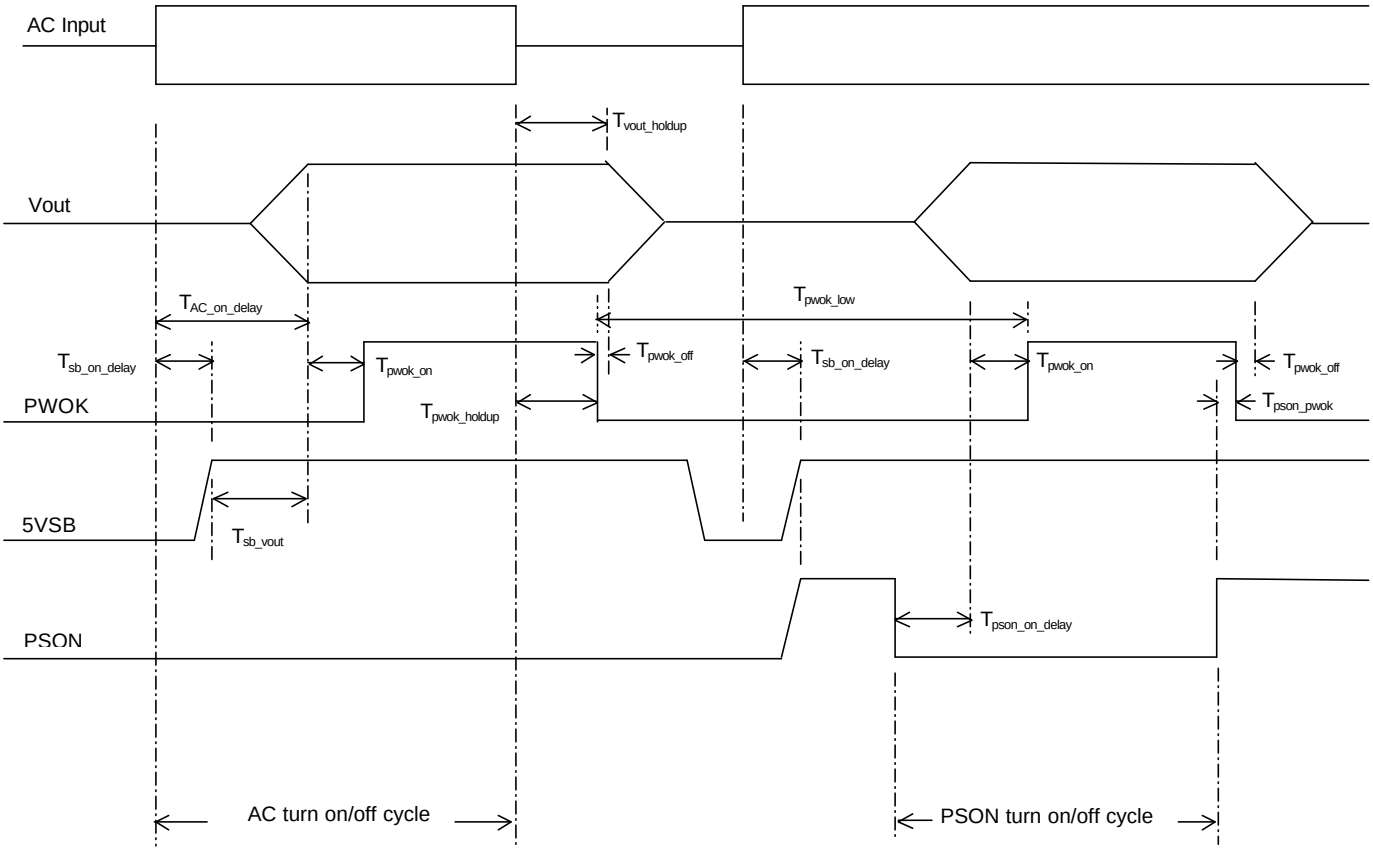


Figure 16. Turn On/Off Timing

11.3.2 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

- Voltage shall remain within +/- 5% of the nominal set voltage on the +5 V, +12 V, 3.3 V, -5 V and -12 V outputs, during instantaneous changes in load shown in the following table.
- Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.
- Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50 Hz to 5 kHz. The load slew rate shall not be greater than 0.2 A/µs.

Table 67. Transient Load Requirements

Output	Step Load Size	Starting Level	Finishing Level	Slew Rate
+3.3 V	4.8 A	30Min. Load	Min. load + 4.8 A and step up to max. load	0.50 A/µs
+5 V	3.0 A	30Min. Load	Min. load + 3.0 A and step up to max. load	0.50 A/µs
+12 V	10.4 A	Min. Load	Min. load + 10.4 A and step up to max. load	0.50 A/µs
+5 VSB	500 mA	Min. Load	Min. load + 500 mA and step up to max. load	0.50 A/µs
-12 V	325 mA	Min. Load	Min load +325 mA and step up to max. load	0.50 A/µs

12. Regulatory and Integration Information

12.1 Product Regulatory Compliance

12.1.1 Product Safety Compliance

The SE7501HG2 complies with the following safety requirements:

- UL 1950 - CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE (74-SEC) 207/94 (Nordics)
- GOST R 50377-92 (Russia)

12.1.2 Product EMC Compliance

The SE7501HG2 system has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel® host system. For information on compatible host system(s), contact your local Intel representative.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22 (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- CE – EMC Directive (89/336/EEC) (European Union)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) Radiated & Conducted Emissions (Korea)
- BSMI (Class A) Radiated & Conducted Emissions (Taiwan)

12.1.3 Product Regulatory Compliance Markings

This product is provided with the following Product Certification Markings:

- cURus Recognition Mark
- CE Mark
- Russian GOST Mark
- Australian C-Tick Mark
- Taiwan BSMI Certification Number 3902I904 and BSMI EMC Warning

12.2 Electromagnetic Compatibility Notices

12.2.1 Europe (CE Declaration of Conformity)

This product has been tested in accordance to, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

12.2.2 Australian Communications Authority (ACA) (C-Tick Declaration of Conformity)

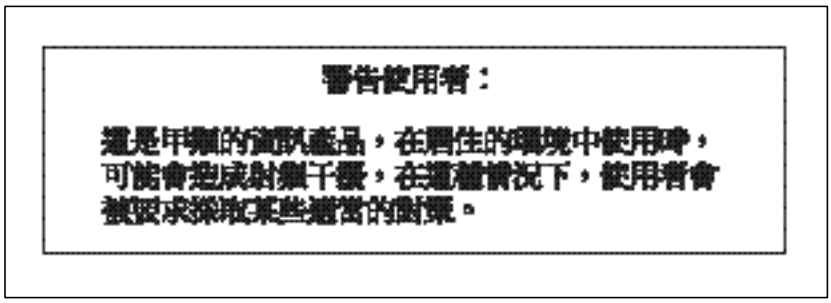
This product has been tested to AS/NZS 3548, and complies with ACA emission requirements. The product has been marked with the C-Tick Mark to illustrate its compliance.

12.2.3 Ministry of Economic Development (New Zealand) Declaration of Conformity

This product has been tested to AS/NZS 3548, and complies with New Zealand's Ministry of Economic Development emission requirements.

12.2.4 BSMI (Taiwan)

The BSMI Certification number 3902I904 is silk screened on the component side of the server board; and the following BSMI EMC warning is located on the solder side of the server board.



12.3 Replacing the Back up Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

13. Mechanical Specifications

The following figure shows the mechanical drawing of the SE7501HG2 server board.

Figure 17. Intel® Server Board SE7501HG2 Server Board Mechanical Drawing

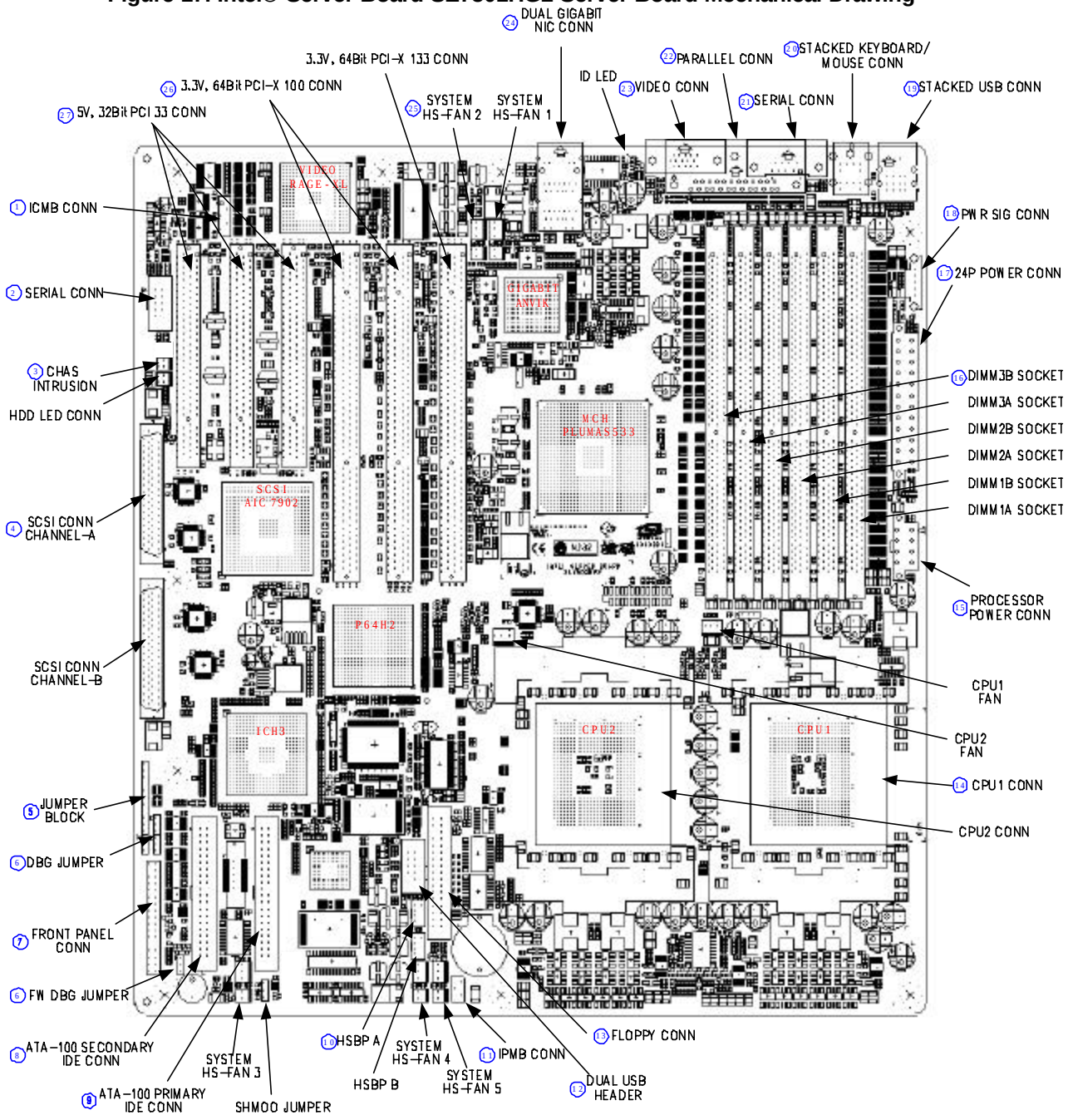


Table 68. Server Board Connector Specifications

Item	Qty.	Manufacturer and Part Number	Description
1	1	Molex* 22-43-6050	5P ICMB Connector
2	1	Wooyoung* BHS-9A(R)-2.54D	9P Header Type Serial Connector
3	3	Foxconn* HF06021-P1	2P Connector, EMP IN USE, Chas. Intrusion, and HDD LED
4	2	AMP* 6-316173-7	68P SCSI Connector
5	1	Wooyoung SPS01-S11A-5A3-R2	9P Connector
6	5	Wooyoung SPS01-S03A-5A1	3P Connector, BMC, DBG, SHMOO
7	1	Wooyoung SPS01-D34A-R3	34P Front Panel Connector
8	1	Wooyoung BHS-33A-2.54D	40P ATA-100 Connector, WHITE
9	1	WorWin* W31-007-4020	40P ATA-100 Connector, BLUE
10	2	Foxconn HF55040-P1	4P External IPMB Connector, HSBP
11	1	Molex 22-44-7031	3P IPMB Connector
12	1	TACT* 100-009-501-J11-T	9P Header Type USB Connector
13	1	Wooyoung BHS-33A-2.54D	33P Floppy Connector
14	2	AMP C-1489688-1	604P PGA604 CPU Socket
15	1	Molex 44206-0003	8P 12V Power Connector
16	6	WinWin* W2DRD-184-A2A-3L2B	184P DIMM Connector
17	1	Molex 44472-2470	24P Power Connector
18	1	Molex 70545-0039	5P AUX Power Connector
19	1	Foxconn UB11123-M1	12P Stacked USB Connector
20	1	Foxconn MH11061-PD2	6P Single PS/2 Connector, Keyb'd, Mouse
21	1	TACT 100-009-501-J11-T	10P Serial Port Connector
22	1	TACT 106-025-601-51A-T	25P Parallel Port Connector
23	1	TACT 147-015-601-C1A-T	15P Video Port Connector
24	1	Foxconn JFM31A1A-0105W	34P Dual Gigabit NIC Connector
25	8	Foxconn HF08030-P1	3P Connector, CPU-Fan, System-Fan
	6	Foxconn HF08020-P1	2P System-Fan Connctor, HS-FAN
26	3	Molex 89177-9260	184P 64bit PCI-X Connector
27	3	Molex 87249-6010	120P 32bit PCI Connector

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Glossary

This appendix contains important terms used in the preceding chapters. For ease of use, numeric entries are listed first (e.g., “82460GX”) with alpha entries following (e.g., “AGP 4x”). Acronyms are then entered in their respective place, with non-acronyms following.

Term	Definition
ACPI	Advanced Configuration and Power Interface
ASIC	application specific integrated circuit
BGA	Ball Grid Array
BIOS	Basic input/output system
BIST	Built-in self test
BMC	Server board Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other.
BSP	Bootstrap processor
Byte	8-bit quantity.
IOB	PCI 64-bit hub
CMOS	This term is used in this document to describe the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
SB	Legacy I/O controller hub
EMP	Emergency management port.
EPS	External Product Specification
FRB	Fault resilient booting
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
Hz	Hertz (1 cycle/second)
I^2C	Inter-integrated circuit bus
IA	Intel® architecture
ICMB	Intelligent Chassis Management Bus
IERR	Internal error
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ITP	In-target probe
KB	1024 bytes.
LAN	Local area network
LCD	Liquid crystal display
LPC	Low pin count
MB	1024 KB
Ms	milliseconds
Mux	multiplexor
NIC	Network Interface Controller
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
Ohm	Unit of electrical resistance

Term	Definition
P32-A	32-bit PCI Segment
P64-B	Full Length 64/100 MHz PCI-X Segment
P64-C	low-profile 64/133 MHz PCI-X Segment
PGA	Pin Grid Array
POST	Power-on Self Test
RAM	Random Access Memory
RISC	Reduced instruction set computing
ROM	Read Only Memory
DDR	Synchronous Dynamic RAM
SEL	System Event Log
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt.
TBD	To Be Determined
UART	Universal asynchronous receiver and transmitter
USB	Universal Serial Bus
Word	16-bit quantity

Appendix A: Intel® Server System SE7501HG2 Platform Sensors

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData	Rearm	Standby
Power Unit Status	01h	Power Unit 09h	Sensor Specific 6Fh	Power Off Power Cycle A/C Lost Soft Power Control Fault Power Unit Failure	As	–	Trig Offset	A	X
Power Unit Redundancy	02h	Power Unit 09h	Generic 0Bh	Redundancy lost	As	–	Trig Offset	A	X
Watchdog	03h	Watchdog2 23h	Sensor Specific 6Fh	Timer Expired Hard Reset Power Down Power Cycle Timer Interrupt	As & De	–	Trig Offset	A	X
Platform Security Violation	04h	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	Secure mode violation attempt Out-of-band access password violation	As	–	Trig Offset	A	X
Physical Security Violation	05h	Physical Security 05h	Sensor Specific 6Fh	General Chassis Intrusion LAN Leash Lost	As & De	General Chassis Intrusion LAN Leash Lost	Trig Offset	A	X
POST Error	06h	POST error 0Fh	Sensor Specific 6Fh	POST error	As	–	POST Code	A	–
Critical Inerrupt Sensor	07h	Critical Interrupt 13h	Sensor Specific 6Fh	Front Panel NMI Bus Error	As & De	–	Trig Offset	A	–
Memory	08h	Memory 0Ch	Sensor Specific 6Fh	Uncorrectable ECC	As	–	Trig Offset	A	–
Event Logging Disabled	09h	Event Logging Disabled 10h	Sensor Specific 6Fh	Correctable Memory Error Logging Disabled Log Area Reset/Cleared	As	–	Trig Offset	A	X
Session Audit	0Ah	Session Audit 2Ah	Sensor Specific 6Fh	00: Session Activation 01: Session Deactivation	As	–	As defined by IPMI	A	X
BB +1.2V	10h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData	Rearm	Standby
BB +1.25V_A	11h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +1.8V	12h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +1.8V Standby	13h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	X
BB +2.5V	14h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +3.3V	15h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +3.3V Auxillary	16h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +5V	17h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +5V Standby	18h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	X
BB +12V	19h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB +12V VRM	1Ah	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB -12V	1Bh	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
BB VBAT	1Ch	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	X
BB Temp	30h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	X
Front Panel Temp	31h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	X
Fan Boost BB Temp	32h	OEM C7h	Threshold 01h	[u][nc]	As & De	Analog	–	A	–
Fan Boost Front Panel Temp	33h	OEM C7h	Threshold 01h	[u][nc]	As & De	Analog	–	A	–
Tach Fan 1	40h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Tach Fan 2	41h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Tach Fan 3	42h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Tach Fan 4	43h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Tach Fan 5	44h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Tach Fan 6	45h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Digital Fan 1	50h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–	Trig Offset	M	–

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData	Rearm	Standby
Digital Fan 2	51h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–	Trig Offset	M	–
Digital Fan 3	52h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–	Trig Offset	M	–
Digital Fan 4	53h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–	Trig Offset	M	–
Digital Fan 5	54h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–	Trig Offset	M	–
Digital Fan 6	55h	Fan 04h	Digital Discrete 06h	Performance Met or Lags	As & De	–	Trig Offset	M	–
LVDS SCSI A channel terminator power	60h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
LVDS SCSI B channel terminator power	61h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
Power Supply Status 1	70h	Power Supply 08h	Sensor Specific 6Fh	Presence Failure Predictive Fail A/C Lost	As & De	–	Trig Offset	A	X
Power Supply Status 2	71h	Power Supply 08h	Sensor Specific 6Fh	Presence Failure Predictive Fail A/C Lost	As & De	–	Trig Offset	A	X
Power Supply Status 3	72h	Power Supply 08h	Sensor Specific 6Fh	Presence Failure Predictive Fail A/C Lost	As & De	–	Trig Offset	A	X
Power Cage Fan 1	73h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
Power Cage Fan 2	74h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
Power Cage Temp	76h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	X
Processor Missing	80h	Module / Board 15h	Digital Discrete 03h	State Asserted State Deasserted	As	–	Trig Offset	A	–
System ACPI Power State	82h	System ACPI Power State 22h	Sensor Specific 6Fh	S0 / G0 S1 S4 S5 / G2 • G3 Mechanical Off	As	–	Trig Offset	A	X

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData	Rearm	Standby
System Event	83h	System Event 12h	Sensor Specific 6Fh	OEM System Boot Event (Hard Reset) • PEF Action	As	–	Trig Offset	A	–
Button	84h	Button 14h	Sensor Specific 6Fh	Power Button Sleep Button Reset Button	As	–	Trig Offset	A	X
SMI Timeout	85h	SMI Timeout F3h	Digital Discrete 03h	State Asserted State Deasserted	As	–	Trig Offset	A	–
Sensor Failure	86h	Sensor Failure F6h	OEM Sensor Specific 73h	I^2C device not found I^2C device error detected I^2C Bus Timeout	As	–	Trig Offset	A	X
NMI Signal State	87h	OEM C0h	Digital Discrete 03h	State Asserted State Deasserted	–	–	–	–	–
SMI Signal State	88h	OEM C0h	Digital Discrete 03h	State Asserted State Deasserted	–	–	–	–	–
Front Side Bus Speed Mismatch	89h	BSEL Mismatch F7h	Digital Discrete 03h	State Asserted	As	–	Trig Offset	A	–
Proc 1 Status	90h	Processor 07h	Sensor Specific 6Fh	Presence Thermal Trip IERR, FRB1. FRB2. FRB3 Disabled Terminator Presence	As & De	–	Trig Offset	M	X
Proc 2 Status	91h	Processor 07h	Sensor Specific 6Fh	Presence Thermal Trip IERR. FRB1, FRB2, FRB3, Disabled • Terminator Presence	As & De	–	Trig Offset	M	X
Proc 1 Core Temp	98h	Temp 01h	Threshold 01h	• [u,l][c,nc]	As & De	Analog	R, T	A	–
Proc 2 Core Temp	99h	Temp 01h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
Fan Boost Proc 1 Core Temp	A0h	OEM C7h	Threshold 01h	[u,l][nc]	As & De	Analog	–	A	–
Fan Boost Proc 2 Core Temp	A1h	OEM C7h	Threshold 01h	[u,l][nc]	As & De	Analog	–	A	–
Processor 1 Fan	A8h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData	Rearm	Standby
Processor 2 Fan	A9h	Fan 04h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	M	–
Proc Vccp	B8h	Voltage 02h	Threshold 01h	[u,l][c,nc]	As & De	Analog	R, T	A	–
Processor HOT	C0h	Temp 01h	Digital Discrete 03h	State Asserted State Deasserted	As & De	–	Trig Offset	M	–
Fan Redundancy	D0h	Fan 04h	Generic 0Bh	Redundancy Regained Redundancy lost Redundancy Degraded	As	-	Trig Offset	A	-
Fan 1 Presence	D8h	Slot/Connector 21h	Sensor Specific 6Fh	Fault Status asserted Identify Status Asserted	As	–	Trig Offset	A	-
Fan 2 Presence	D9h	Slot/Connector 21h	Sensor Specific 6Fh	Fault Status asserted Identify Status Asserted	As	–	Trig Offset	A	-
Fan 3 Presence	DAh	Slot/Connector 21h	Sensor Specific 6Fh	Fault Status asserted Identify Status Asserted	As	–	Trig Offset	A	-
Fan 4 Presence	DBh	Slot/Connector 21h	Sensor Specific 6Fh	Fault Status asserted Identify Status Asserted	As	–	Trig Offset	A	-
Fan 5 Presence	DCh	Slot/Connector 21h	Sensor Specific 6Fh	Fault Status asserted Identify Status Asserted	As	–	Trig Offset	A	-
Fan 6 Presence	DDh	Slot/Connector 21h	Sensor Specific 6Fh	Fault Status asserted Identify Status Asserted	As	–	Trig Offset	A	-
DIMM 1	E0h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–	Trig Offset	A	–
DIMM 2	E1h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–	Trig Offset	A	–
DIMM 3	E2h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–	Trig Offset	A	–

Sensor Name	Sensor #	Sensor Type	Event / Reading Type	Event Offset Triggers	Assert / Deassert	Readable Value / Offsets	EventData	Rearm	Standby
DIMM 4	E3h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–	Trig Offset	A	–
DIMM 5	E4h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–	Trig Offset	A	–
DIMM 6	E5h	Slot Connector 21h	Sensor Specific 6Fh	Fault Status Asserted Device Installed Disabled	As	–	Trig Offset	A	–

Reference Documents

Refer to the following documents for additional information:

- *PCI Local Bus Specification* Revision 2.2
- *PCI-X Specification 1.0a*
- *ATI RAGE XL Graphics Controller Specifications, Technical Reference Manual*, Rev 2.01
- RAID I/O Steering (RAIDIOS) specification version 1.0
- VRM 9.1 DC-DC Converter Design Guide Line
- Intel® Xeon™ Processor Voltage Regulator Down Design Guide Lines
- I2C Bus Specification
- IPMB Communications Protocol Specification
- SE7501HG2 Intel® Server Management TPS v5.5

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