DATA SHEET

SUNPLUS

SPIF223A

ATA to Serial ATA Bi-direction Bridge

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Version 1.2

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A SINGLE-CHIP SOLUTION FOR AN ATA TO SERIAL ATA DEVICE BRIDGE

1. GENERAL DESCRIPTION

The Sunplus SPIF223A is a single-chip solution for bi-direction of ATA to Serial ATA and Serial ATA to ATA device bridge. It could accept ATA commands through both ATA and SATA interface , decode the commands and converts them into ATA commands to the device. Response from the device through the serial ATA or ATA bus are deciphered, processed and converted to ATA protocol and sent to the host. The SPIF223A supports the Serial ATA generation 1 transfer rate of 1.5Gb/s (150MB/s) on the serial side and is compatible with Ultra133 on the ATA side.

2. FEATURES

- **Overall Features**
  - Bi-Direction of ATA to Serial ATA bridge chip.
  - Compliant with ATA specification.
  - Compliant with SATA 1.0a specification.
  - Compatible with Ultra ATA 133.
  - Fabricated in 0.16um CMOS process with 1.8 volt core and 3.3 volt I/Os.
  - Available in a 64-pin TQFP package with e-Pad[1].
  - PHY isolation debug mode
  - Full scan for high production test coverage
  - Build-in 8051 uP to control data flow.
  - Support UART, SPI, I2C bus.
  - Support ATA bus skew-rate programming by UART/SPI interface.[2]
- **Serial ATA Features**
  - Integrated Serial ATA Link and PHY logic.
  - Compliant with Serial ATA 1.0A specifications.
  - Support Serial ATA Generation 1 transfer rate of 1.5Gb/s.
  - Support Spread Spectrum in receiver.
  - Support Serial ATA power saving mode : Partial, and Slumber..
- **ATA Features**
  - Compliant with ATA specifications.
  - Compatible with Ultra ATA 133.
  - Support PIO mode 0,1,2,3,4,5,6 MDMA0,1,2 and Ultra DMA mode 0,1,2,3,4,5,6
  - Support UDMA data transfer rates of up to 133MBps.
  - Support ATA device master/slave/Chip select emulation.
  - Support ATA bus timing control.
  - Support ATA and ATAPI device like HDD and ODD, Tape..
  - Support ATA interface reverse feature.

3. REFERENCES

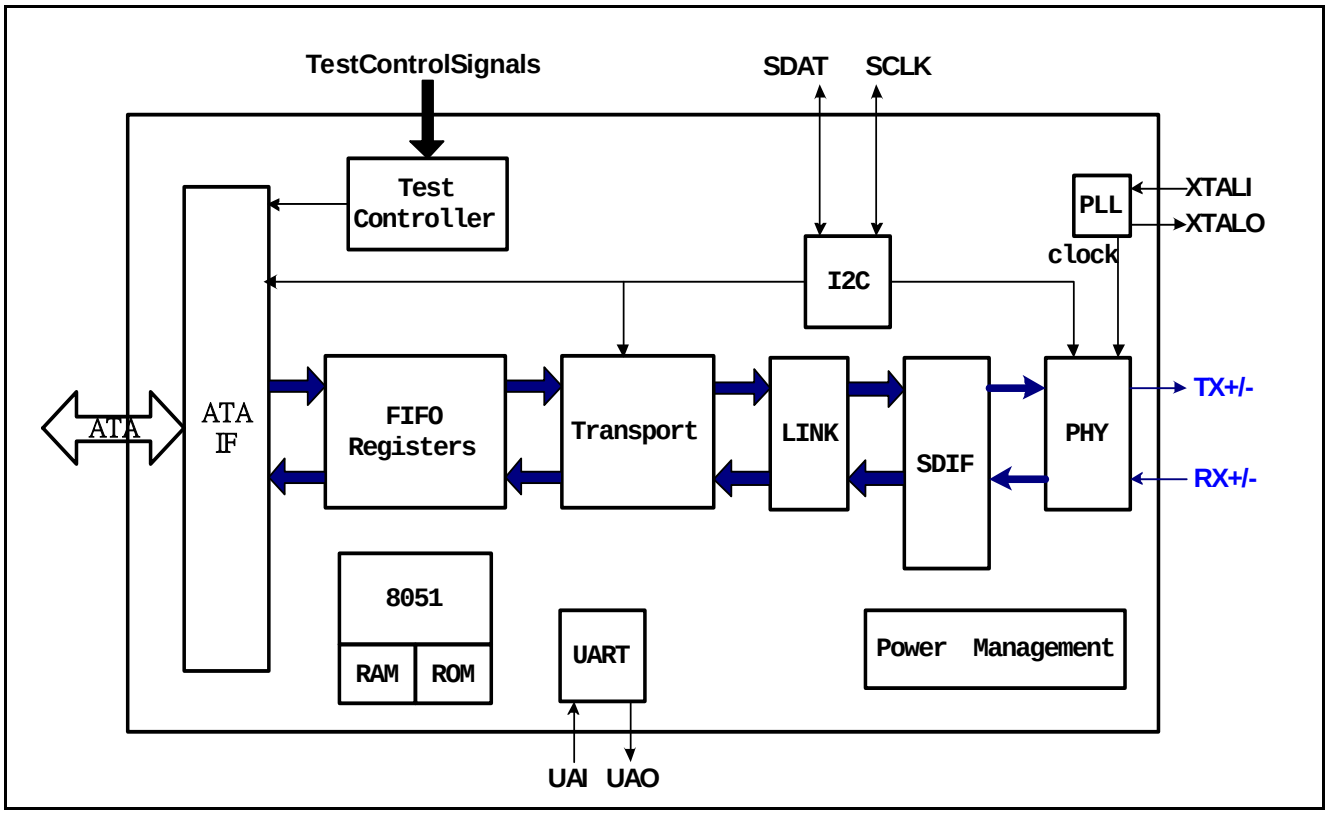
For more details about Serial ATA and ATA technology please refer to the following industry specifications:

- Serial ATA / High Speed Serialized ATA Attachment specification, Revision 1.0A.
- Http://www.T13.org/ ATA/ATAPI specifications.

[1] For e-Pad of SPIF223A, please always connect e-Pad to the ground of application board.

[2] For ATA bus timing control, please check with agent to get more information for UART/SPI interface.

4. FUNCTIONAL BLOCK DIAGRAM



5.SIGNAL DESCRIPTIONS

5.1. Pin Descriptions

Table 5-1: Pin Types

Pin Type	Pin Description
I/O	Bi-directional Pin
I	Input Pin with LVTTL Thresholds
O	Output Pin
I-Sch	Input Pin with Schmitt Trigger
P	Pull-Down resistor is internal
T	Tri-state Output Pin

5.2. Pin List

Table 5-2: SPIF223A Pin Listing

Pin#	Pin Name	Type	Description
1	B_IDE_DD[13]	I/O	ATA Interface Data Bus bit 13
2	B_IDE_DD[2]	I/O	ATA Interface Data Bus bit 2
3	B_IDE_DD[12]	I/O	ATA Interface Data Bus bit 12
4	D3V3_IO	PWR	3.3V Digital I/O Power
5	B_IDE_DD[3]	I/O	ATA Interface Data Bus bit 3
6	B_IDE_DD[11]	I/O	ATA Interface Data Bus bit 11
7	B_IDE_DD[4]	I/O	ATA Interface Data Bus bit 4
8	DVSS	GND	Ground for the Digital Core and I/O
9	D1V8_CO	PWR	1.8V Digital CORE Power
10	B_IDE_DD[10]	I/O	ATA Interface Data Bus bit 10
11	B_IDE_DD[5]	I/O	ATA Interface Data Bus bit 5
12	B_IDE_DD[9]	I/O	ATA Interface Data Bus bit 9
13	B_IDE_DD[6]	I/O	ATA Interface Data Bus bit 6
14	B_IDE_DD[8]	I/O	ATA Interface Data Bus bit 8
15	B_IDE_DD[7]	I/O	ATA Interface Data Bus bit 7
16	I_IDE_RST_B	I/O	ATA Interface Reset.
17	RESET_B	I	ASIC Reset input
18	D3V3_IO	PWR	3.3V Digital I/O Power
19	IDE_ORD_INV	I	ATA Cable Signal Ordering Inverse
20	CFG0	I	Device/Host mode enable
21	UART_SPI_SEL	I	UART/SPI interface enable 0: UART enable, 1: SPI enable
22	XTALI/CLKI	I	Crystal oscillator input or external clock input
23	XTALO	O	Crystal oscillator output
24	VDDA	PWR	1.8V Analog Power
25	GNDA	GND	Analog Ground
26	REXT	I	External reference resistor input
27	RXP	I	Differential receive +ve
28	RXN	I	Differential receive –ve
29	VDDA	PWR	1.8V Analog Power
30	GNDA	GND	Analog Ground
31	TXN	O	Differential transmit –ve

Pin#	Pin Name	Type	Description
32	TXP	O	Differential transmit +ve
33	I_IDE_JUMP0	I	Jumper 0
34	IDE_DASP	I/O	ATA Interface Device Active or Slave(Device 1) Present
35	IDE_JUMP1	I	Jumper 1
36	TEST_CFG	I	Test Configuration bit 0
37	UAO_SPI_OUT	O	UART/SPI data output
38	SPI_En_B	O	SPI Enable
39	SPL_CLK	O	SPI Clock
40	UAI_SPI_IN	I	UART/SPI data in
41	D1V8_CO	PWR	1.8V Digital CORE Power
42	DVSS	GND	Ground for the Digital Core and I/O
43	I2C_SDA	I/O	I2C Serial Data
44	D3V3_IO	PWR	3.3V Digital I/O Power
45	I2C_SCLK	I/O	I2C Serial Clock
46	IDE_PDIAG	I/O	ATA Interface Passed Diagnostics ATA Interface Cable Assembly Type Identifier
47	IDE_CS1_B	I/O	ATA Interface Chip Select 1
48	IDE_CS0_B	I/O	ATA Interface Chip Select 0
49	IDE_DA2	I/O	ATA Interface Device Address bit 2
50	IDE_DA0	I/O	ATA Interface Device Address bit 0
51	IDE_DA1	I/O	ATA Interface Device Address bit 1
52	IDE_CSEL	I/O	ATA Interface Cable Select
53	IDE_INTRQ	I/O	ATA Interface Interrupt Request
54	IDE_DMACK_B	I/O	ATA Interface DMA Acknowledge
55	IDE_IORDY	I/O	ATA Interface I/O Ready ATA Interface DMA Read during Ultra DMA data-out bursts ATA Interface Data Strobe during Ultra DMA data-in bursts
56	D3V3_IO	PWR	3.3V Digital I/O Power
57	DVSS	GND	Ground for the Digital Core and I/O
58	IDE_DIOR_B	I/O	ATA Interface I/O Read ATA Interface DMA Ready during Ultra DMA data-in bursts ATA Interface Data Strobe during Ultra DMA data-out bursts
59	IDE_DIOW_B	I/O	ATA Interface I/O Write ATA Interface Stop during Ultra DMA data bursts
60	IDE_DMARQ	I/O	ATA Interface DMA Request
61	IDE_DD[15]	I/O	ATA Interface Data Bus bit 15
62	IDE_DD[0]	I/O	ATA Interface Data Bus bit 0
63	IDE_DD[14]	I/O	ATA Interface Data Bus bit 14
64	IDE_DD[1]	I/O	ATA Interface Data Bus bit 1

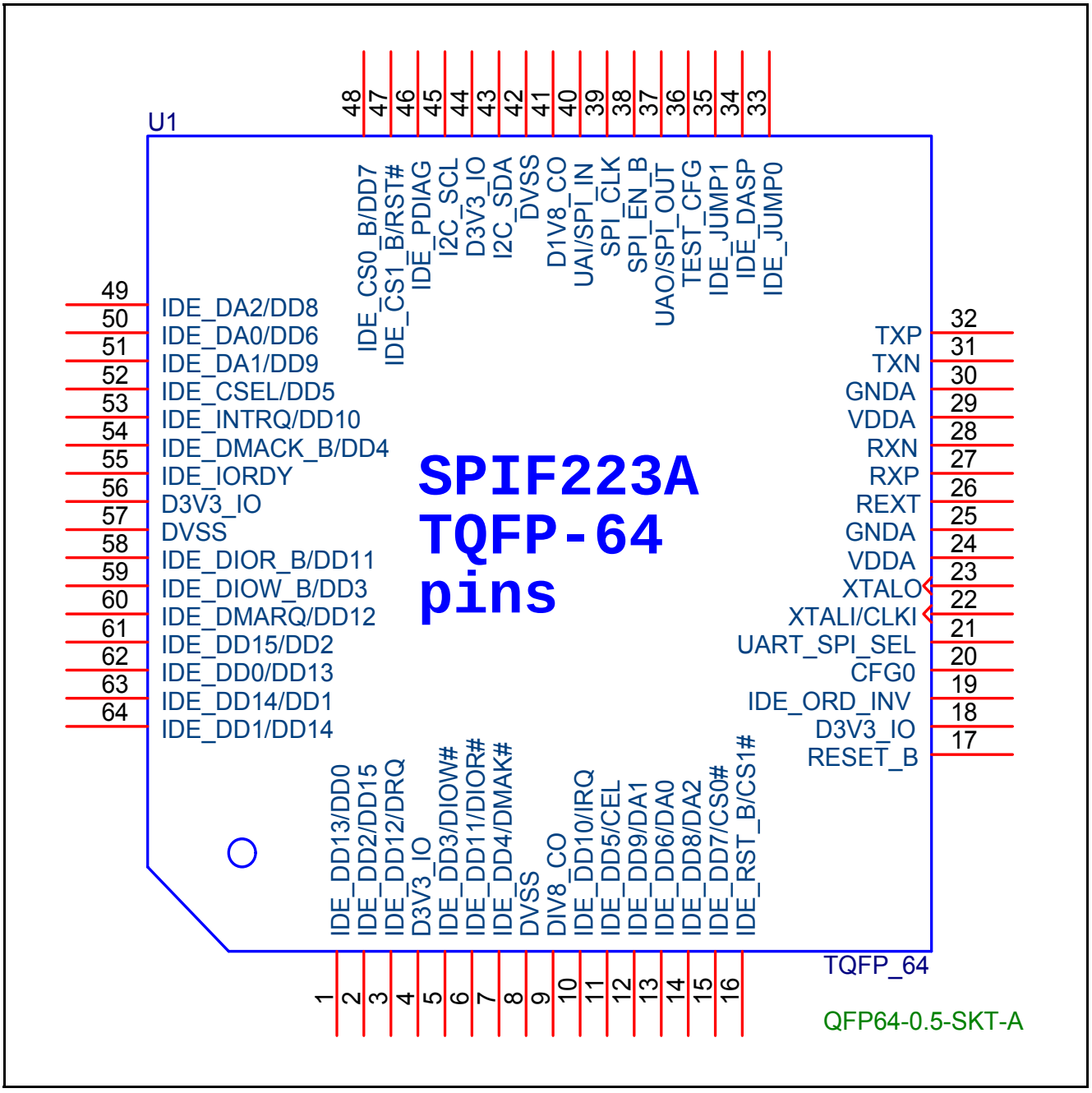
5.3. ATA Interface Reverse

	IDE_ORD_INV = 0	IDE_ORD_INV = 1
Pin#	Pin Name	Pin Name
1	IDE_DD[13]	IDE_DD[0]
2	IDE_DD[2]	IDE_DD[15]
3	IDE_DD[12]	IDE_DMARQ
4	D3V3_IO	
5	IDE_DD[3]	IDE_DIOW_
6	IDE_DD[11]	IDE_DIOR_

	IDE_ORD_INV = 0	IDE_ORD_INV = 1
Pin#	Pin Name	Pin Name
7	B_IDE_DD[4]	IDE_DMACK_
8	DVSS	
9	D1V8_CO	
10	IDE_DD[10]	IDE_INTRQ
11	IDE_DD[5]	IDE_CSEL
12	IDE_DD[9]	IDE_DA1
13	IDE_DD[6]	IDE_DA0
14	IDE_DD[8]	IDE_DA2
15	IDE_DD[7]	IDE_CS0_
16	I_IDE_RST_B	IDE_CS1_
17	RESET_B	
18	D3V3_IO	
19	IDE_ORD_INV	
20	CFG0	
21	UART_SPI_SEL	
22	XTALI/CLKI	
23	XTALO	
24	VDDA	
25	GNDA	
26	REXT	
27	RXP	
28	RXN	
29	VDDA	
30	GNDA	
31	TXN	
32	TXP	
33	I_IDE_JUMP0	
34	IDE_DASP	
35	IDE_JUMP1	
36	TEST_CFG	
37	UAO_SPI_OUT	
38	SPI_En_B	
39	SPL_CLK	
40	UAI_SPI_IN	
41	D1V8_CO	
42	DVSS	
43	I2C_SDA	
44	D3V3_IO	
45	I2C_SCLK	
46	IDE_PDIAG	
47	IDE_CS1_B	IDE_RESET_
48	IDE_CS0_B	IDE_DD[7]
49	IDE_DA2	IDE_DD[8]
50	IDE_DA0	IDE_DD[6]
51	IDE_DA1	IDE_DD[9]

	IDE_ORD_INV = 0	IDE_ORD_INV = 1
Pin#	Pin Name	Pin Name
52	IDE_CSEL	IDE_DD[5]
53	IDE_INTRQ	IDE_DD[10]
54	IDE_DMACK_B	IDE_DD[4]
55	IDE_IORDY	
56	D3V3_IO	
57	DVSS	
58	IDE_DIOR_B	IDE_DD[11]
59	IDE_DIOW_B	IDE_DD[3]
60	IDE_DMARQ	IDE_DD[12]
61	IDE_DD[15]	IDE_DD[2]
62	IDE_DD[0]	IDE_DD[13]
63	IDE_DD[14]	IDE_DD[1]
64	IDE_DD[1]	IDE_DD[14]

5.4. SPIF223A Pin Diagram



6.ELECTRONICAL SPECIFICATION

6.1. Power Requirement

Table 6-1: Total Power Dissipation

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_{IO}	Absolute digital I/O pad power supply	3.3v	0	5.0	-	mA
I_{analog}	Absolute digital power supply and PHY	1.8v	60	90	-	mA

6.2. Absolute Maximum Ratings

Table 6-2: Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating	Limits			Unit
				Min.	Typ.	Max.	
V_{IO}	Absolute digital I/O pad power supply voltage			3.0	3.3	3.6	V
V_{CORE}	Absolute digital power supply			1.62	1.8	1.98	V
V_{ASATA}	Absolute analog power supply voltage for PHY			1.62	1.8	1.98	V
V_I	Absolute input voltage			3.0	3.3	3.6	V
T_{STR}	Absolute storage temperature			-40	25	150	℃

6.3. Recommended/Typical Operating Conditions

Table 6-3: Recommended/Typical Operating Conditions

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CORE}	Operating digital power supply voltage		1.62	1.8	1.98	V
V_{IO}	Operating digital I/O pad supply voltage		3.0	3.3	3.6	V
V_{ASATA}	Operating analog power supply voltage for SATA PHY		1.62	1.8	1.98	V
V_I	Operating Input signal voltage		3.0	3.3	3.6	V
T_{OPE}	Operating temperature		0	25	70	℃

6.4. DC Characteristics

Table 6-4 DC Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{IL}	Input low voltage		-0.3	-	0.8	V
V_{IH}	Input high voltage		2.0	-	V_{DDPST}+0.3	V
V_T	Threshold point		1.45	1.59	1.77	V
V_T^+	Schmitt trig. Low to High threshold point		1.47	1.50	1.50	V
V_T^-	Schmitt trig. high to low threshold point		0.90	0.94	0.96	V
I_I	Input leakage current	V_I=5.5V or 0V	-	-	± 10	μA
I_{OZ}	Tri-state output leakage current	V_O=5.5V or 0V	-	-	± 10	μA
R_{PU}	Pull-up resistor		46	70	114	KΩ
R_{PD}	Pull-down resistor		30	58	129	KΩ
V_{OL}	Output low voltage	I_{OL} (min)	-	-	0.4	V
V_{OH}	Output high voltage	I_{OH} (min)	2.4	-	-	V
I_{OL}	Low level output current	V_{OL}=0.4V 4mA	4.5	6.6	8.3	mA
		V_{OL}=0.4V 8mA	8.9	13.2	16.7	mA
I_{OH}	High level output current	V_{OL}=2.4V 8mA	12.3	24.8	40.5	mA
		V_{OL}=2.4V 12mA	18.5	37.1	60.8	mA

6.5. SPIF223A UART and SPI Interface Select:

SPIF223A have supported 2 IO interface: UART and SPI. Then, it could be configured by pin21 (UART_SPI_Sel)

UART_SPI_Sel : 0 Using UART interface.

UART_SPI_Sel : 1 Using SPI interface.

6.6. SPIF223A Device Mode or Host :

SPIF223A have supported both dirction : SerialATA to ATA host bridge and ATA to SerialAT host bridge. Then, we could use pin20 (H_D_Sel).

H_D_Sel : 0 Serial ATA device to ATA host mode (Connecting to ATA HDD)..

H_D_Sel : 1 ATA device to Serial ATA host mode. (Connecting to Serial ATA HDD).

6.7. SPIF223A ATA Device Mode Select:

When SPIF223A have been choice to H_D_Sel as 1, it will use as ATA device mode. For ATA device, SPIF223A could support master, slave and Cable select. It could be configured by :

Mode	IDE_JUMP0	IDE_JUMP1
Master	0	0
Slave	1	0
Cable Select	1	1

6.8. SPIF223A Serial ATA bus Tri-state Feature:

SPIF223A have supported Serial ATA bus Tri-state feature under UART_SPI_SEL as low. It could help to design a combo interface or multi-interface product.

SPI_CLK : Low Serial ATA bus Hi-Z.

SPI_CLK : High Serial ATA bus normal feature.

6.9. SPIF223A ATA bus Tri-state Feature:

SPIF223A have supported ATA bus tri-state by pin 38 (SPI_EN). If SPI_EN# is low, SPIF223A will enable ATA bus Tri-state. If SPI_EN# is high, SPIF223A will go into normal function to accept ATA bus access. (For this mode, UART_SPI_Sel must be low.)

SPI_EN# : Low ATA bus Tri-State

SPI_EN#: High ATA bus normal feature.

7.COMMAND LIST

The SPIF223A ATA to Serial ATA Controller decodes ATA commands in hardware. The commands supported include ATA/ATAPI-5 and ATA/ATAPI-6 commands, including the 48-bit LBA extended commands. Certain obsolesced commands are also supported. The supported commands are listed below:

7.1. ATA Command List:

Table 7-1 ATA Standard Commands

Command Name	Command Code	Sub Cmd Code	Protocol	Comment
CFA ERASE SECTORS	C0h	—	ND	
CFA REQUEST EXTENDED ERROR	03h	—	ND	
CFA TRANSLATE SECTOR	87h	—	PI	
CFA WRITE MULTIPLE WITHOUT ERASE	CDh	—	PO	
CFA WRITE SECTORS WITHOUT ERASE	38h	—	PO	
CHECK MEDIA CARD TYPE	D1h	—	ND	
CHECK POWER MODE	E5h or 98h	—	ND	
CONFIGURE STREAM	51h		ND	
DEVICE CONFIGURATION RESTORE	B1h	C0h	ND	
DEVICE CONFIGURATION FREEZE LOCK	B1h	C1h	ND	
DEVICE CONFIGURATION IDENTIFY	B1h	C2h	PI	
DEVICE CONFIGURATION SET	B1h	C3h	PO	
DEVICE RESET	08h	—	DR	
EXECUTE DEVICE DIAGNOSTIC	90h	—	DD	
FLUSH CACHE	E7h	—	ND	
FLUSH CACHE EXT	EAh	—	ND	
GET MEDIA STATUS	DAh	—	ND	
IDENTIFY DEVICE	ECh	—	PI	
IDENTIFY PACKET DEVICE	A1h	—	PI	
IDLE	E3h or 97h	—	ND	
IDLE IMMEDIATE	E1h or 95h	—	ND	
INITIALIZE DEVICE PARAMETERS	91h	—	ND	Obsolete
MEDIA EJECT	EDh	—	ND	
MEDIA LOCK	DEh	—	ND	
MEDIA UNLOCK	DFh	—	ND	
NOP	00h	—	ND	
PACKET	A0h	—	P	
READ BUFFER	E4h	—	PI	
READ DMA	C8h	—	DM	
READ DMA WITHOUT RETRY	C9h	—	DM	Obsolete
READ DMA EXT	25h	—	DM	
READ LOG EXT	2Fh	—	PI	
READ MULTIPLE	C4h	—	PI	
READ MULTIPLE EXT	29h	—	PI	
READ NATIVE MAX ADDRESS	F8h	—	ND	
READ NATIVE MAX ADDRESS EXT	27h	—	ND	
READ LONG	22h	—	PI	Obsolete
READ LONG WITHOUT RETRY	23h	—	PI	Obsolete

READ SECTOR(S)	20h	—	PI	
READ SECTOR(S) EXT	24h	—	PI	
READ SECTOR(S) WITHOUT RETRY	21h	—	PI	Obsolete
READ STREAM DMA EXT	2Ah	—	DM	
READ STREAM EXT	2Bh	—	PI	
READ VERIFY SECTOR(S)	40h	—	ND	
READ VERIFY SECTOR(S) WITHOUT RETRY	41h	—	ND	Obsolete
READ VERIFY SECTOR(S) EXT	42h	—	ND	
RECALIBARATE	1Xh	—	ND	Obsolete
SECURITY DISABLE PASSWORD	F6h	—	PO	
SECURITY ERASE PREPARE	F3h	—	ND	
SECURITY ERASE UNIT	F4h	—	PO	
SECURITY FREEZE LOCK	F5h	—	ND	
SECURITY SET PASSWORD	F1h	—	PO	
SECURITY UNLOCK	F2h	—	PO	
SEEK	7Xh	—	ND	Obsolete
SET FEATURES	EFh	—	ND	
SET MAX ADDRESS	F9h	—	ND	
SET MAX SET PASSWORD	F9h	01h	PO	
SET MAX LOCK	F9h	02h	ND	
SET MAX UNLOCK	F9h	03h	PO	
SET MAX FREEZE LOCK	F9h	04h	ND	
SET MAX ADDRESS EXT	37h	—	ND	
SET MULTIPLE MODE	C6h	—	ND	
SLEEP	E6h or 99h	—	ND	
SMART READ DATA	B0h	D0h	PI	
SMART READ THRESHOLDS	B0h	D1h	PI	Obsolete
SMART ENABLE/DISABLE AUTOSAVE	B0h	D2h	ND	
SMART SAVE VALUES	B0h	D3h	ND	Obsolete
SMART EXECUTE OFF-LINE IMMEDIATE	B0h	D4h	ND	
SMART READ LOG	B0h	D5h	PI	
SMART WRITE LOG	B0h	D6h	PO	
SMART WRITE ATTRIBUTE THRESHOLDS	B0h	D7h	PO	Obsolete
SMART ENABLE	B0h	D8h	ND	
SMART DISABLE	B0h	D9h	ND	
SMART RETURN STATUS	B0h	DAh	ND	
SMART ENABLE/DISABLE AUTO OFF-LINE	B0h	DBh	ND	Obsolete
SMART PENDING SECTOR REPAIR SELF TEST	B0h	FAh	ND	Vendor Specific
STANDBY	E2h or 96h	—	ND	
STANDBY IMMEDIATE	E0h or 94h	—	ND	
WRITE BUFFER	E8h	—	PO	
WRITE DMA	CAh	—	DM	
WRITE DMA WITHOUT RETRY	CBh	—	DM	
WRITE DMA EXT	35h	—	DM	

WRITE DMA FUA EXT	3Dh	—	DM	
WRITE LOG EXT	3Fh	—	PO	
WRITE MULTIPLE	C5h	—	PO	
WRITE MULTIPLE EXT	39h	—	PO	
WRITE MULTIPLE FUA EXT	CEh	—	PO	
WRITE SECTOR(S)	30h	—	PO	
WRITE SECTOR(S) WITHOUT RETRY	31h	—	PO	Obsolete
WRITE SECTOR(S) EXT	34h	—	PO	
WRITE LONG	32h	—	PO	Obsolete
WRITE LONG WITHOUT RETRY	33h	—	PO	Obsolete
WRITE STREAM DMA EXT	3Ah	—	DM	
WRITE STREAM EXT	3Bh	—	PO	
WRITE VERIFY	3Ch	—	PO	

Key:
ND = Non-data command
PI = PIO data-in command
PO = PIO data-out command
DM = DMA command
DR = DEVICE RESET command
DD = EXECUTE DEVICE DIAGNOSTIC command

7.2. ATAPI Command List:

Command Name	Op Code	Protocol	Type	Comment
BLANK	A1h	No Data	MMC	
CLOSE TRACK/SESSION	5Bh	No Data	MMC	
ERASE(6)	19h	No Data	SSC	
ERASE(10)	2Ch	No Data	MMC	
FORMAT UNIT	04h	Data Out	MMC	
GET CONFIGURATION	46h	Data In	MMC	
GET EVENT STATUS NOTIFICATION	4Ah	Data In	MMC	
GET PERFORMANCE	ACh	Data In	MMC	
INQUIRY	12h	Data In	SPC	
LOAD/UNLOAD MEDIUM	A6h	No Data	MMC	
LOG SENSE	4Dh	Data In	SPC	
LOG SELECT	4Ch	Data Out	SPC	
MECHANISM STATUS	BDh	Data In	MMC	
MODE SELECT(6)	15h	Data Out	SPC	
MODE SELECT(10)	55h	Data Out	SPC	
MODE SENSE(6)	1Ah	Data In	SPC	
MODE SENSE(10)	5Ah	Data In	SPC	
PAUSE/RESUME	4Bh	No Data	MMC	
PLAY AUDIO(10)	45h	No Data	MMC	
PLAY AUDIO(12)	A5h	No Data	MMC	
PLAY AUDIO MSF	47h	No Data	MMC	
PLAY CD	BCh	No Data	INF-8090	Obsolete
PREVENT ALLOW MEDIUM REMOVAL	1Eh	No Data	MMC	
READ(6)	08h	Data In	SSC	
READ(10)	28h	Data In	MMC	
READ(12)	A8h	Data In	MMC	
READ BUFFER CAPACITY	5Ch	Data In	MMC	
READ CAPACITY	25h	Data In	MMC	
READ BLOCK LIMITS	05h	Data In	SSC	
READ BUFFER	3Ch	Data In	SPC	
READ HEADER	44h	Data In	INF-8090	Obsolete
READ CD	BEh	Data In	MMC	
READ CD MSF	B9h	Data In	MMC	
READ DISK INFORMATION	51h	Data In	MMC	
READ DISC STRUCTURE	ADh	Data In	MMC	
READ FORMAT CAPACITIES	23h	Data In	MMC	
READ SUBCHANNEL	42h	Data In	MMC	
READ TOC	43h	Data In	MMC	
READ TRACK RZONE INFORMATION	52h	Data In	MMC	

REPORT KEY	A4h	Data In	MMC	
REQUEST SENSE	03h	Data In	SPC	
RESERVE TRACK	53h	No Data	MMC	
REZERO UNIT	01h	No Data	SCSI-2	
SCAN	BAh	No Data	MMC	
SEEK(6)	0Bh	No Data	SCSI-2	
SEEK(10)	2Bh	No Data	MMC	
SEND CUE SHEET	5Dh	Data Out	MMC	
SEND EVENT	A2h	Data Out	INF-8090	
SEND OPC INFORMATION	54h	Data Out	MMC	
SET CD SPEED	BBh	No Data	MMC	
SET LIMITS	33h	No Data	SCSI-2	
SET STREAMING	B6h	Data Out	MMC	
SPACE	11h	No Data	SSC	
START STOP UNIT	1Bh	No Data	MMC	
STOP PLAY/SCAN	4Eh	No Data	MMC	
SYNCHRONIZE CHACHE	35h	No Data	MMC	
TEST UNIT READY	00h	No Data	SPC	
VERIFY(10)	2Fh	No Data	MMC	
WRITE(6)	0Ah	Data Out	SSC	
WRITE(10)	2Ah	Data Out	MMC	
WRITE(12)	AAh	Data Out	MMC	
WRITE BUFFER	3Bh	Data Out	SPC	
WRITE FILEMARKS	10h	Data Out	SSC	
WRITE AND VERIFY(10)	2Eh	Data Out	MMC	

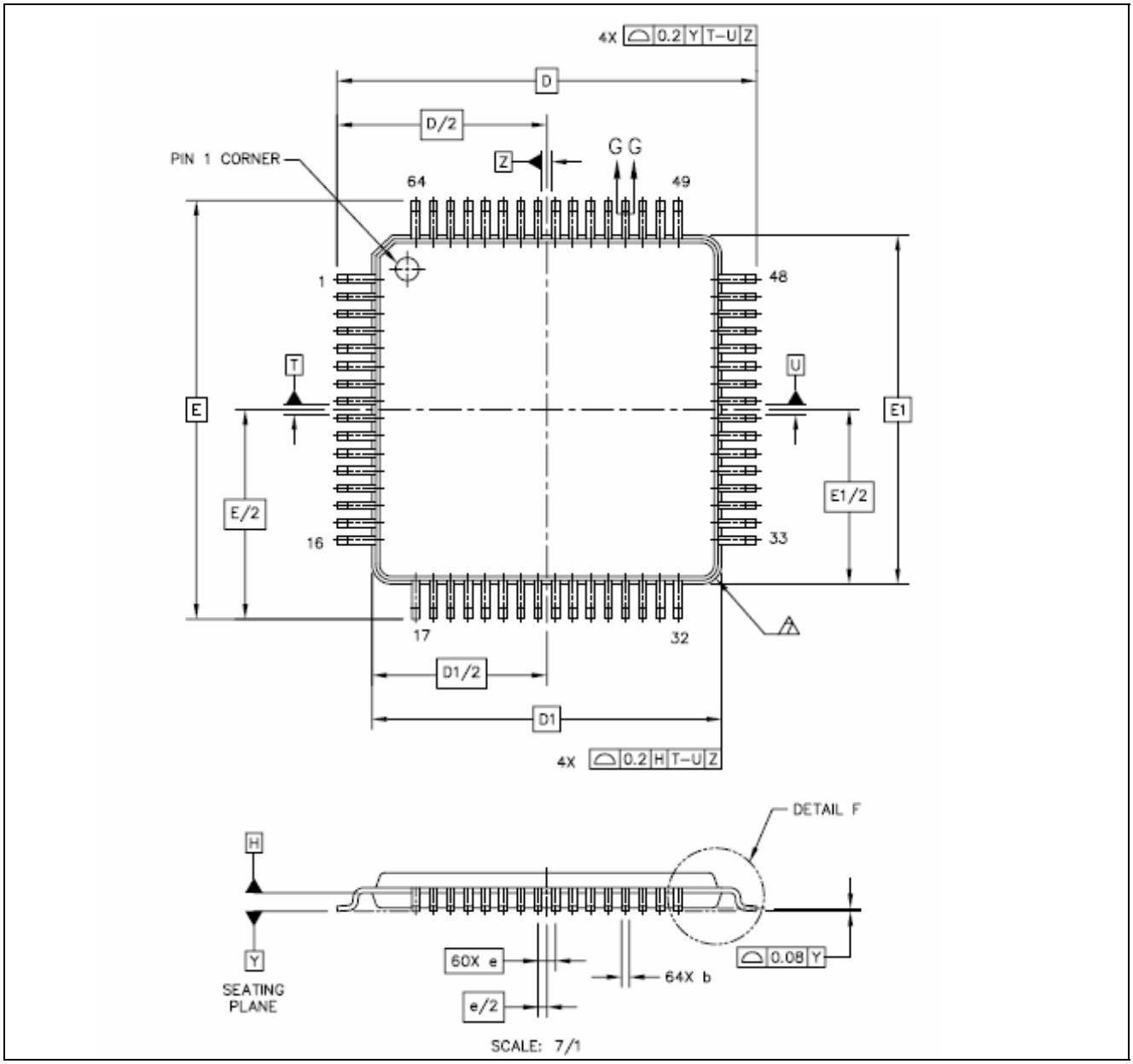
[3]

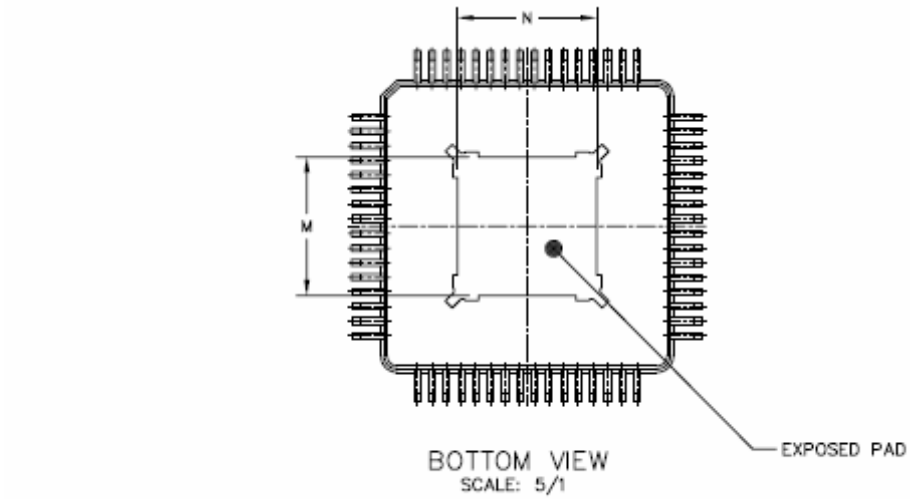
[3] About ATAPI command, SPIF223A will not support 16-byte SCSI command if ATAPI device don't indicate 16-byte packet support on Identify packet device information.

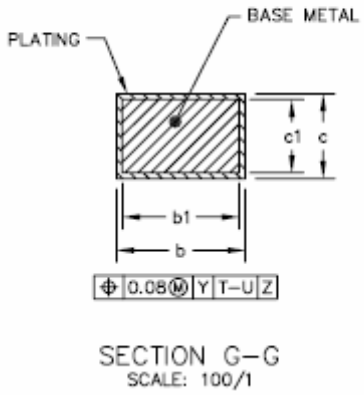
8.PACKAGE/PAD LOCATIONS

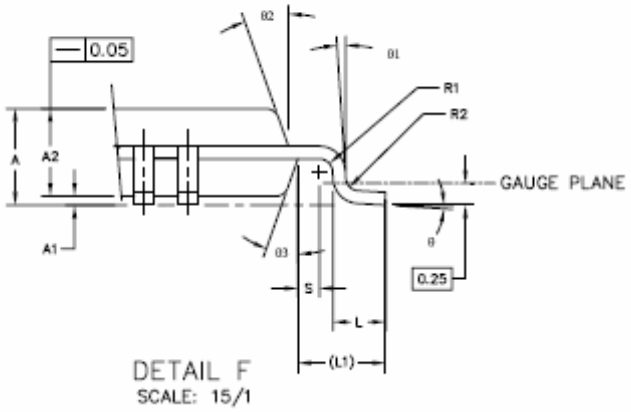
8.1. Package Information

8.1.1. 64 pin TQFP









DIM	MIN		MAX
A	---		1.2
A1	0.05		0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		12 BSC	
D1		10 BSC	
e		0.5 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.6	0.75

DIM	MIN		MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°
M	4.58		4.78
N	4.58		4.78

Fig 8-1: SPIF223A in TQFP-64 package

◎E-Pad dimension could be changed without notice.

8.2. Ordering Information

Product Number	Package Type
SPIF223A - HF021	Green Package form – TQFP 64*

8.3. Storage Condition and Period for Package

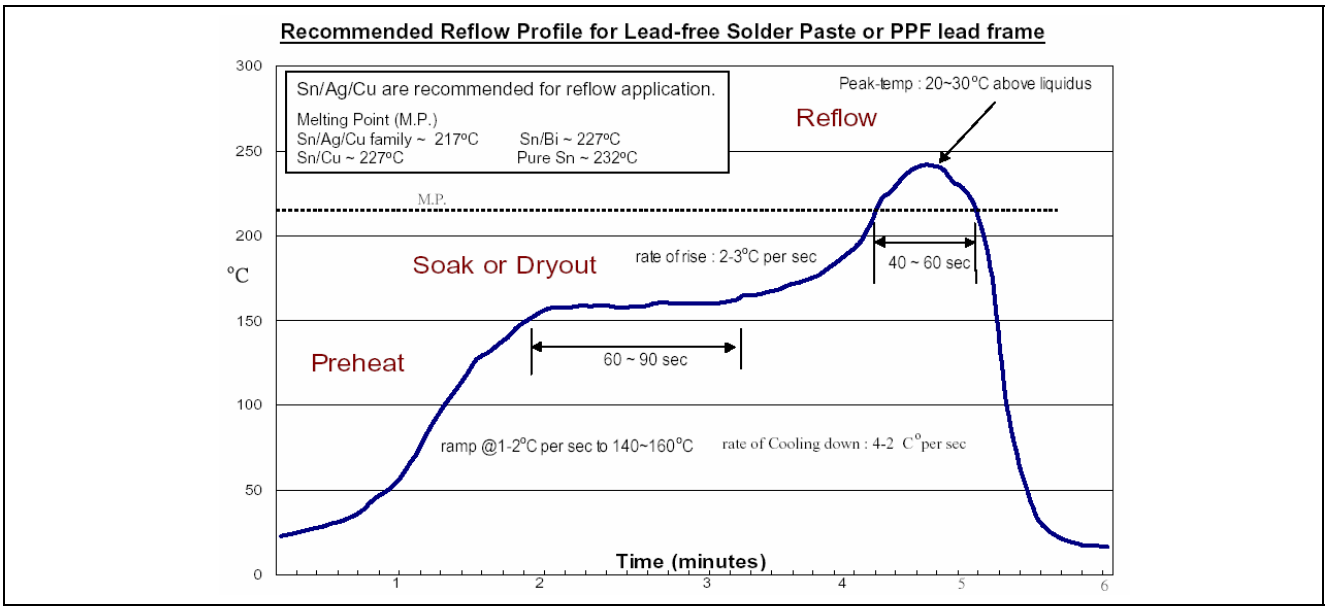
Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
TQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JFSD22-A112

Note2: or refer to the "CAUTION Note" on dry pack bag.

8.4. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of SUNPLUS leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF(Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



9.DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
MAY 29, 2006	1.2	1.Update application into datasheet . (UART/SPI, ATA_bus Tri-State, SerialATA Hi_Z) 2.Update AC timing 3.Add command list for ATA command and Packet command.	3-6 10-11 12-16
APR. 25, 2006	1.1	1.Update application into datasheet . (UART/SPI, ATA_bus Tri-State, SerialATA Hi_Z) 2.Update AC timing 3.Add command list for ATA command and Packet command. 4.Update pin assignment, 5.Add ATA interface reverse 5.3 section.	3-6 10-11 12-16 18 6-8
SEP. 08, 2005	1.0	Original	16