Model Name :Q5WV1/Q5WS1
Compal Project Name :
File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document

Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH

Nvidia N13P GS/GL

2012-02-03b

REV:0.3

MB PCB

Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B

ZZZ2 1G@ X76344BOL01

ZZZ3 2G@ X76344BOL02

Security Classification	Compal Secret Data		
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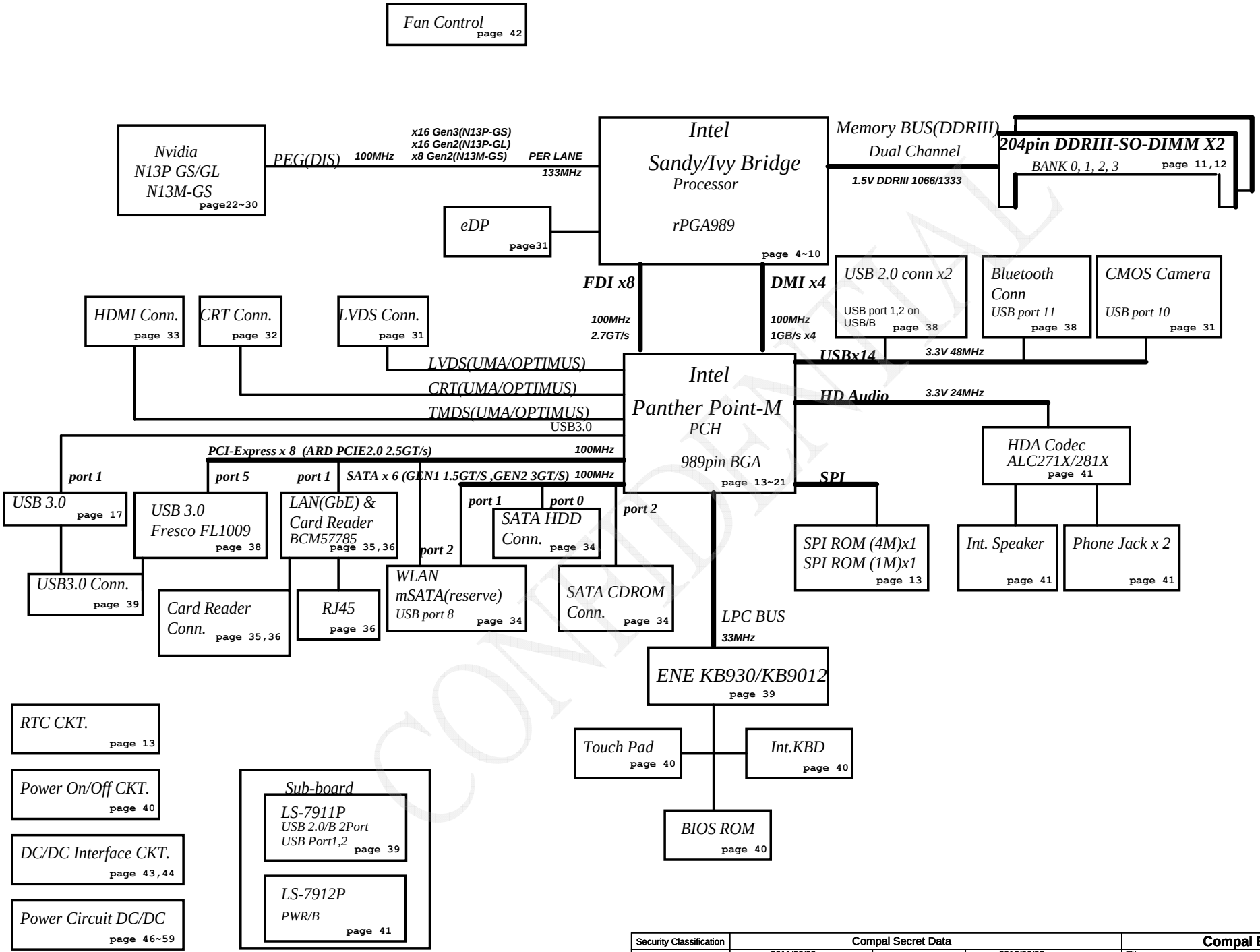

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

4319IDBOL01SMT MB A7912 Q5WV1 HM77 QC UMA 3
4319IDBOL02SMT MB A7912 Q5WV1 HM77 QC 13PGL1G 3
4319IDBOL03SMT MB A7912 Q5WV1 HM77 QC 13PGL2G 3
4319IDBOL04SMT MB A7912 Q5WV1 HM77 QC 13PGS1G 3
4319IDBOL05SMT MB A7912 Q5WV1 HM77 QC 13PGS2G 3
4319IDBOL06SMT MB A7912 Q5WV1 HM77 DC UMA 2
4319IDBOL07SMT MB A7912 Q5WV1 HM77 DC UMA 3
4319IDBOL08SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 2
4319IDBOL09SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 3
4319IDBOL10SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 2
4319IDBOL11SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 3
4319IDBOL12SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 2
4319IDBOL13SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 3
4319IDBOL14SMT MB A7912 Q5WV1 HM77 DC 13PGS2G 3

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB3@
Internal USB 2.0	PUSB@
USB 2.0 flag	PUSB2@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@
N13P-GS & GL	GSGL@
N13M-GS	GM@
support AC function	AC@
no AC function	NOAC@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	
	UHCI5	10	Camera
		11	BlueTooth
	UHCI6	12	
		13	

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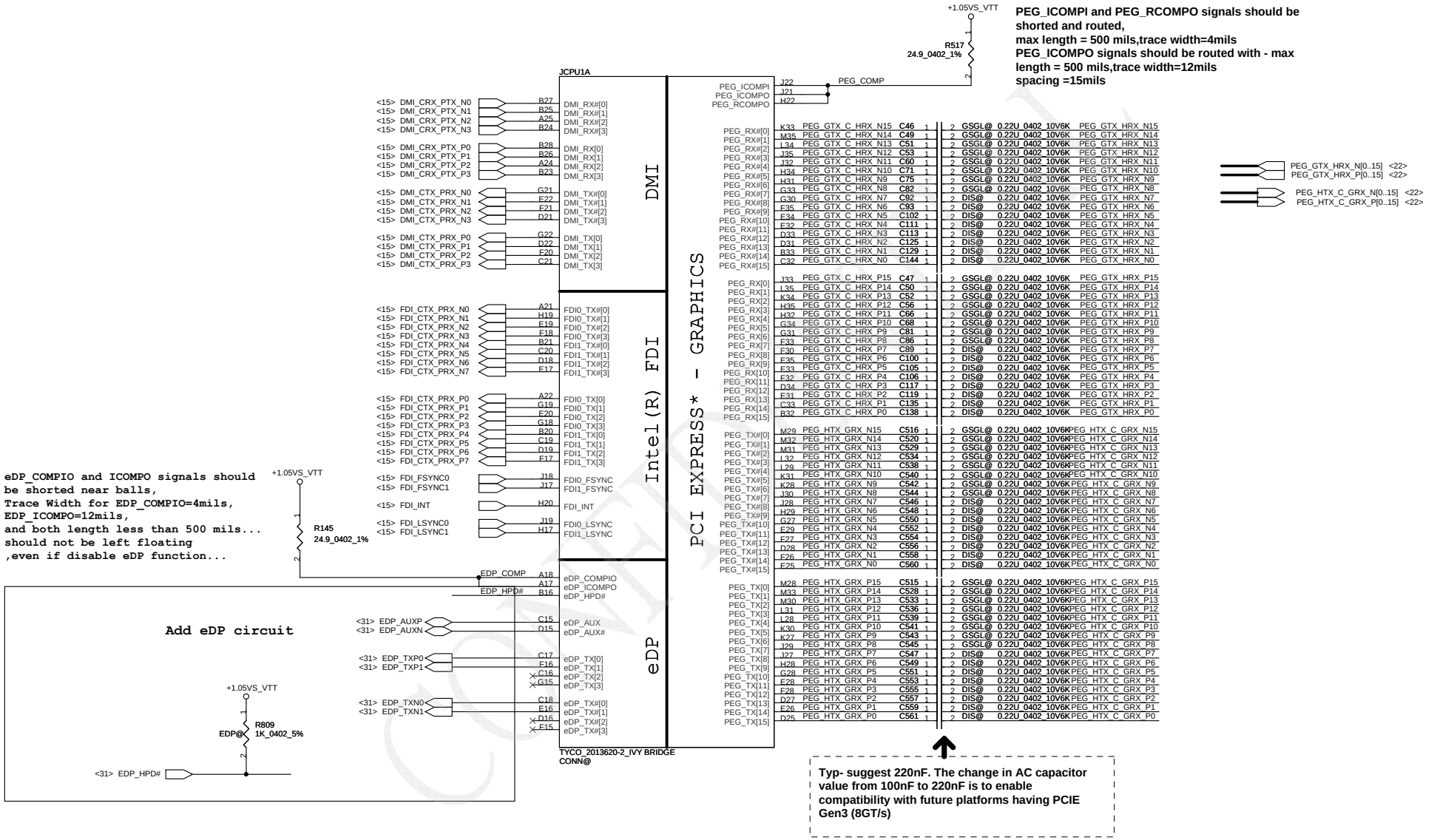

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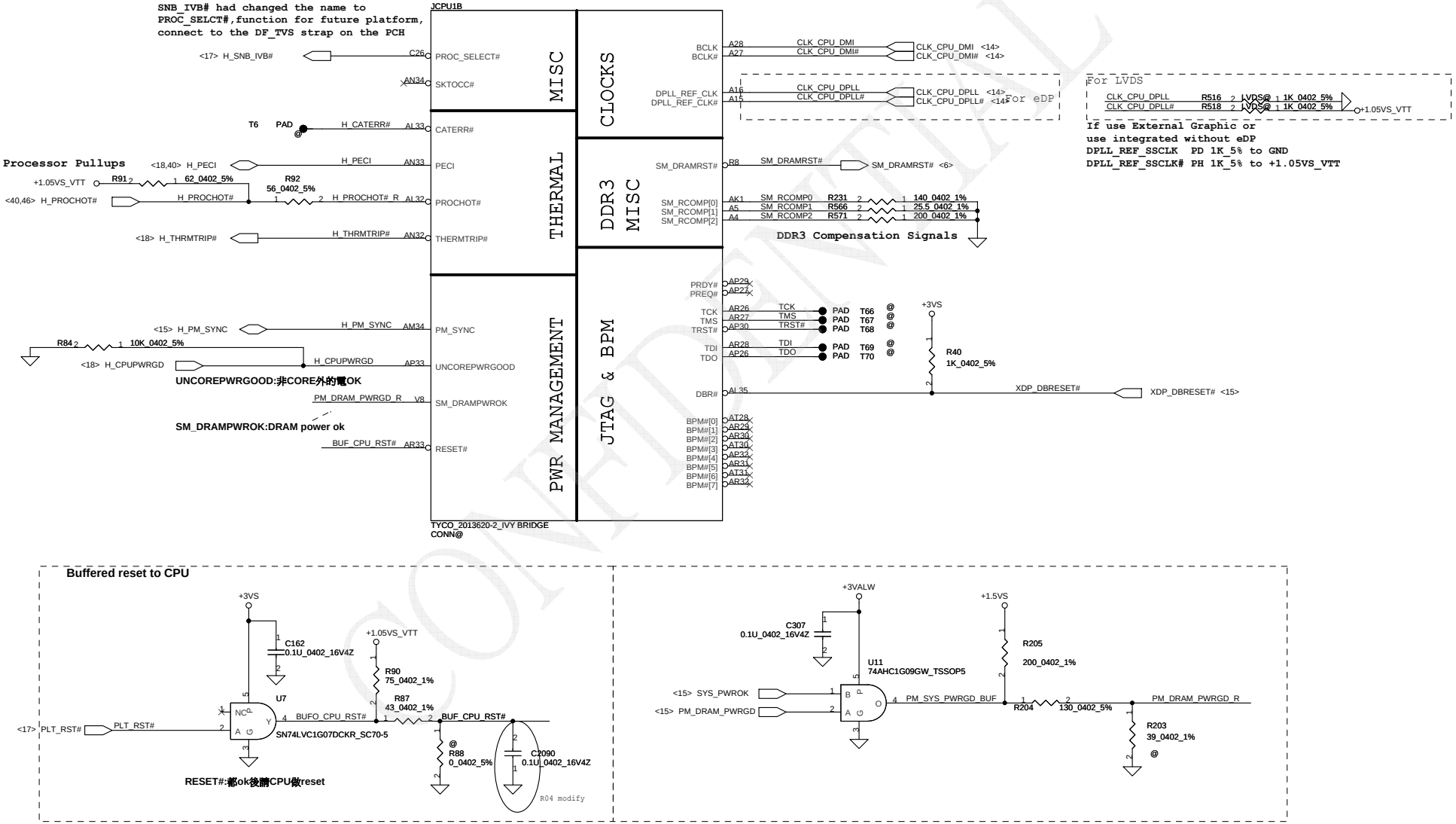

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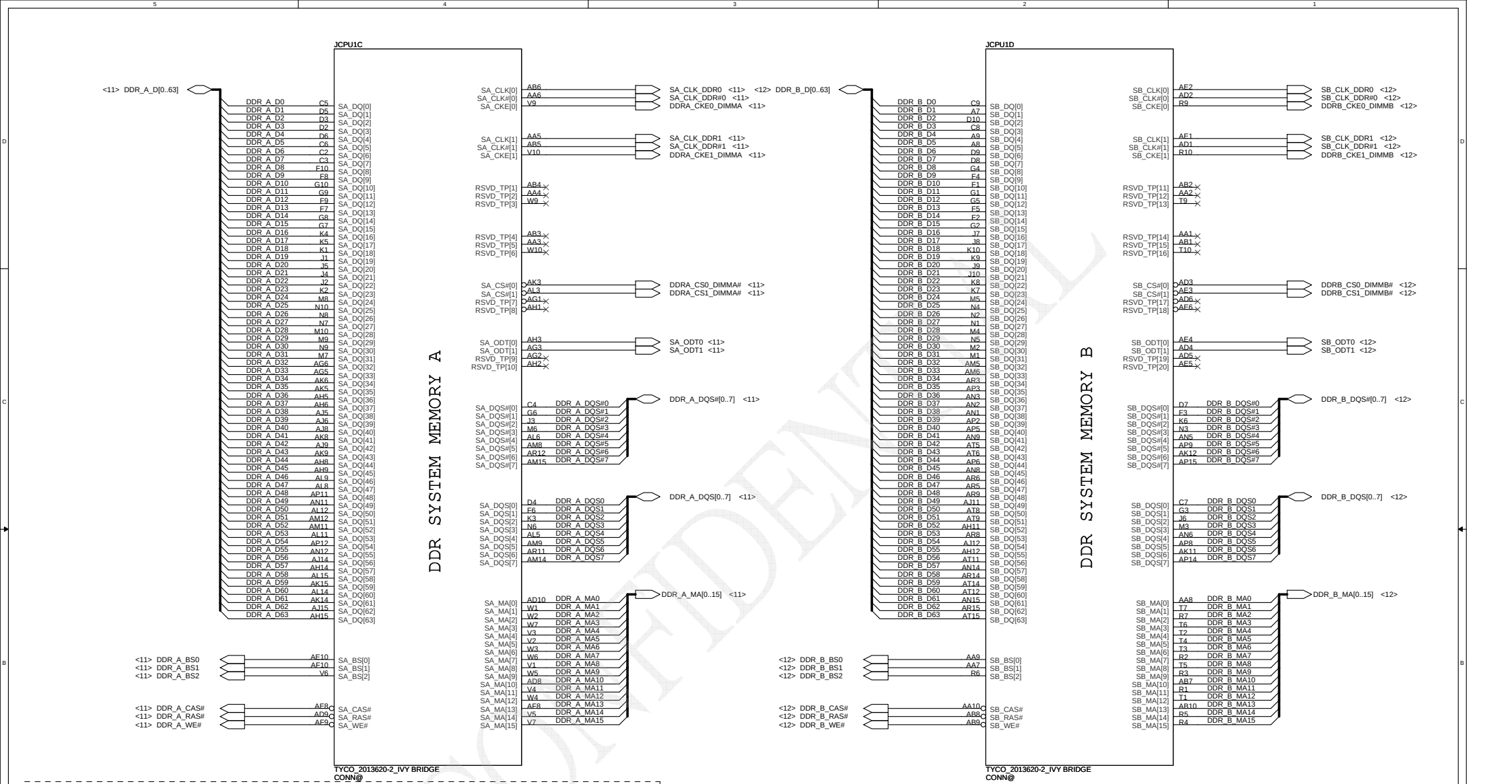

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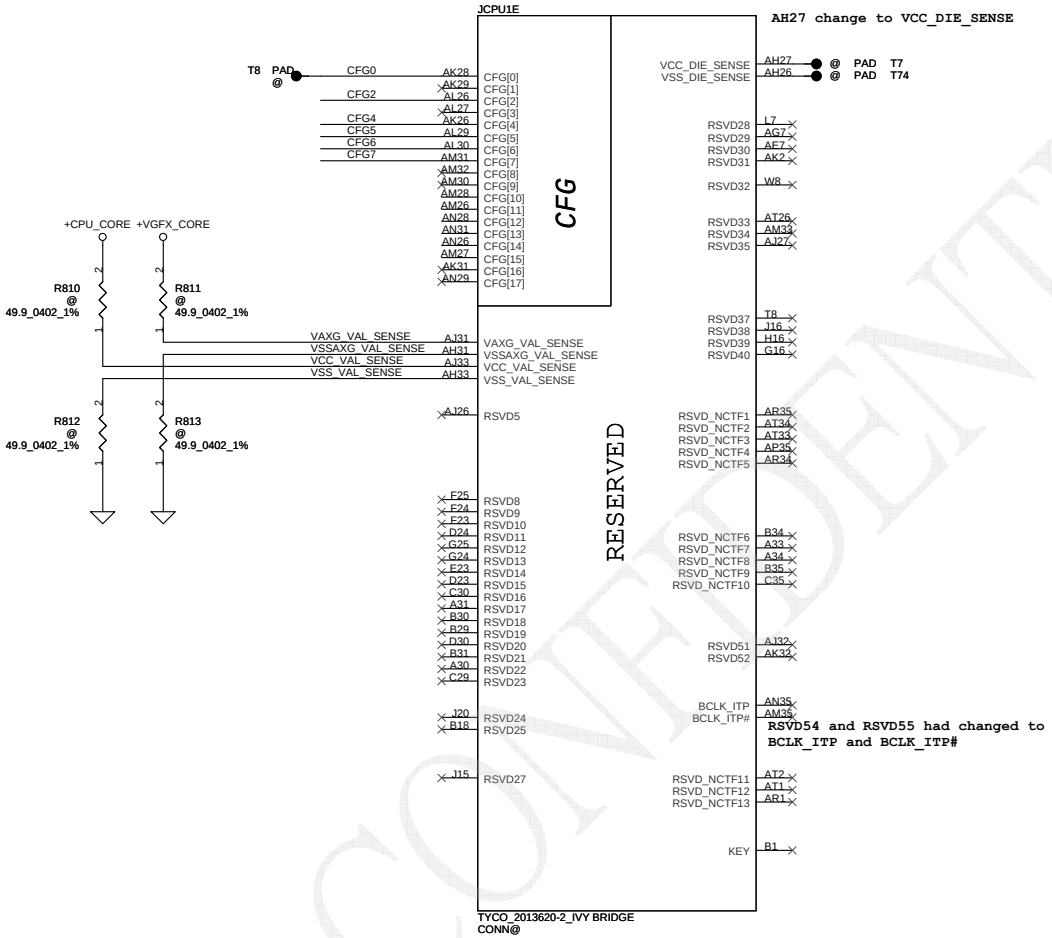
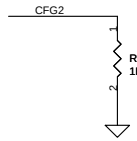
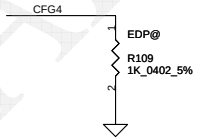
CFG Straps for Processor

AH26	Sandy	Ivy
	GND	VSS_DIE_SENSE

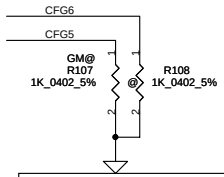




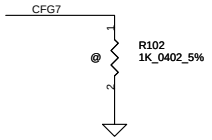
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

SV type CPU

QC 53A
DC 53A

JCPU1F

+CPU_CORE

CORE SUPPLY

AG35	VCC1	AE35	VCC71
AG34	VCC2	AE34	VCC72
AG33	VCC3	AE33	VCC73
AG32	VCC4	AE32	VCC74
AG31	VCC5	AE31	VCC75
AG30	VCC6	AE30	VCC76
AG29	VCC7	AE29	VCC77
AG28	VCC8	AE28	VCC78
AG27	VCC9	AE27	VCC79
AG26	VCC10	AE26	VCC80
AF35	VCC11	AD35	VCC81
AF34	VCC12	AD34	VCC82
AF33	VCC13	AD33	VCC83
AF32	VCC14	AD32	VCC84
AF31	VCC15	AD31	VCC85
AF30	VCC16	AD30	VCC86
AF29	VCC17	AD29	VCC87
AF28	VCC18	AD28	VCC88
AF27	VCC19	AD27	VCC89
AF26	VCC20	AD26	VCC90
AD35	VCC21	AC35	VCC91
AD34	VCC22	AC34	VCC92
AD33	VCC23	AC33	VCC93
AD32	VCC24	AC32	VCC94
AD31	VCC25	AC31	VCC95
AD30	VCC26	AC30	VCC96
AD29	VCC27	AC29	VCC97
AD28	VCC28	AC28	VCC98
AD27	VCC29	AC27	VCC99
AD26	VCC30	AC26	VCC100
AC35	VCC31	AA35	VCC41
AC34	VCC32	AA34	VCC42
AC33	VCC33	AA33	VCC43
AC32	VCC34	AA32	VCC44
AC31	VCC35	AA31	VCC45
AC30	VCC36	AA30	VCC46
AC29	VCC37	AA29	VCC47
AC28	VCC38	AA28	VCC48
AC27	VCC39	AA27	VCC49
AC26	VCC40	AA26	VCC50
AA35	VCC41	Y35	VCC51
AA34	VCC42	Y34	VCC52
AA33	VCC43	Y33	VCC53
AA32	VCC44	Y32	VCC54
AA31	VCC45	Y31	VCC55
AA30	VCC46	Y30	VCC56
AA29	VCC47	Y29	VCC57
AA28	VCC48	Y28	VCC58
AA27	VCC49	Y27	VCC59
AA26	VCC50	Y26	VCC60
Y35	VCC51	V35	VCC61
Y34	VCC52	V34	VCC62
Y33	VCC53	V33	VCC63
Y32	VCC54	V32	VCC64
Y31	VCC55	V31	VCC65
Y30	VCC56	V30	VCC66
Y29	VCC57	V29	VCC67
Y28	VCC58	V28	VCC68
Y27	VCC59	V27	VCC69
Y26	VCC60	V26	VCC70
V35	VCC61	U35	VCC71
V34	VCC62	U34	VCC72
V33	VCC63	U33	VCC73
V32	VCC64	U32	VCC74
V31	VCC65	U31	VCC75
V30	VCC66	U30	VCC76
V29	VCC67	U29	VCC77
V28	VCC68	U28	VCC78
V27	VCC69	U27	VCC79
V26	VCC70	U26	VCC80
U35	VCC71	R35	VCC81
U34	VCC72	R34	VCC82
U33	VCC73	R33	VCC83
U32	VCC74	R32	VCC84
U31	VCC75	R31	VCC85
U30	VCC76	R30	VCC86
U29	VCC77	R29	VCC87
U28	VCC78	R28	VCC88
U27	VCC79	R27	VCC89
U26	VCC80	R26	VCC90
R35	VCC81	P35	VCC91
R34	VCC82	P34	VCC92
R33	VCC83	P33	VCC93
R32	VCC84	P32	VCC94
R31	VCC85	P31	VCC95
R30	VCC86	P30	VCC96
R29	VCC87	P29	VCC97
R28	VCC88	P28	VCC98
R27	VCC89	P27	VCC99
R26	VCC90	P26	VCC100

PEG AND DDR

8.5A

+1.05VS_VTT

VCCIO1	AH13	VCCIO21	F12
VCCIO2	AH10	VCCIO22	F11
VCCIO3	AG10	VCCIO23	E14
VCCIO4	AC10	VCCIO24	E12
VCCIO5	Y10	VCCIO25	E11
VCCIO6	U10	VCCIO26	D14
VCCIO7	P10	VCCIO27	D13
VCCIO8	L10	VCCIO28	D12
VCCIO9	J14	VCCIO29	D11
VCCIO10	J13	VCCIO30	C14
VCCIO11	J12	VCCIO31	C13
VCCIO12	J11	VCCIO32	C12
VCCIO13	H14	VCCIO33	C11
VCCIO14	H12	VCCIO34	B14
VCCIO15	H11	VCCIO35	B12
VCCIO16	G14	VCCIO36	A14
VCCIO17	G13	VCCIO37	A13
VCCIO18	G12	VCCIO38	A12
VCCIO19	F14	VCCIO39	A11
VCCIO20	F13	VCCIO40	J23

SVID

+1.05VS_VTT

R450 130_0402_1%

+1.05VS_VTT

R447 75_0402_5%

R448 43_0402_1%

VIDALERT#	AJ29	H_CPU_SVIDALRT#			VR_SVID_ALRT# <52>
VIDSCLK	AJ30	H_CPU_SVIDCLK	R446	0_0402_5%	VR_SVID_CLK <52>
VIDSOUT	AJ28	H_CPU_SVIDDAT	R449	0_0402_5%	VR_SVID_DAT <52>

SENSE LINES

Place the PU resistors close to CPU

+CPU_CORE

R445 100_0402_1%

VCC_SENSE	AJ35	VCCSENSE_R	R444	0_0402_5%	VCCSENSE <52>
VSS_SENSE	AJ34	VSSSENSE_R	R443	0_0402_5%	VSSSENSE <52>

R442 100_0402_1%

R910 10_0402_5% +1.05VS_VTT

VCCIO_SENSE	B10	VCCIO_SENSE	VCCIO_SENSE <50>
VSS_SENSE_VCCIO	A10	VSSIO_SENSE	VSSIO_SENSE <50>

VSSIO_SENSE change to VSS_SENSE_VCCIO

R163 10_0402_5%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

TYCO_2013620-2_IVY BRIDGE CONN@

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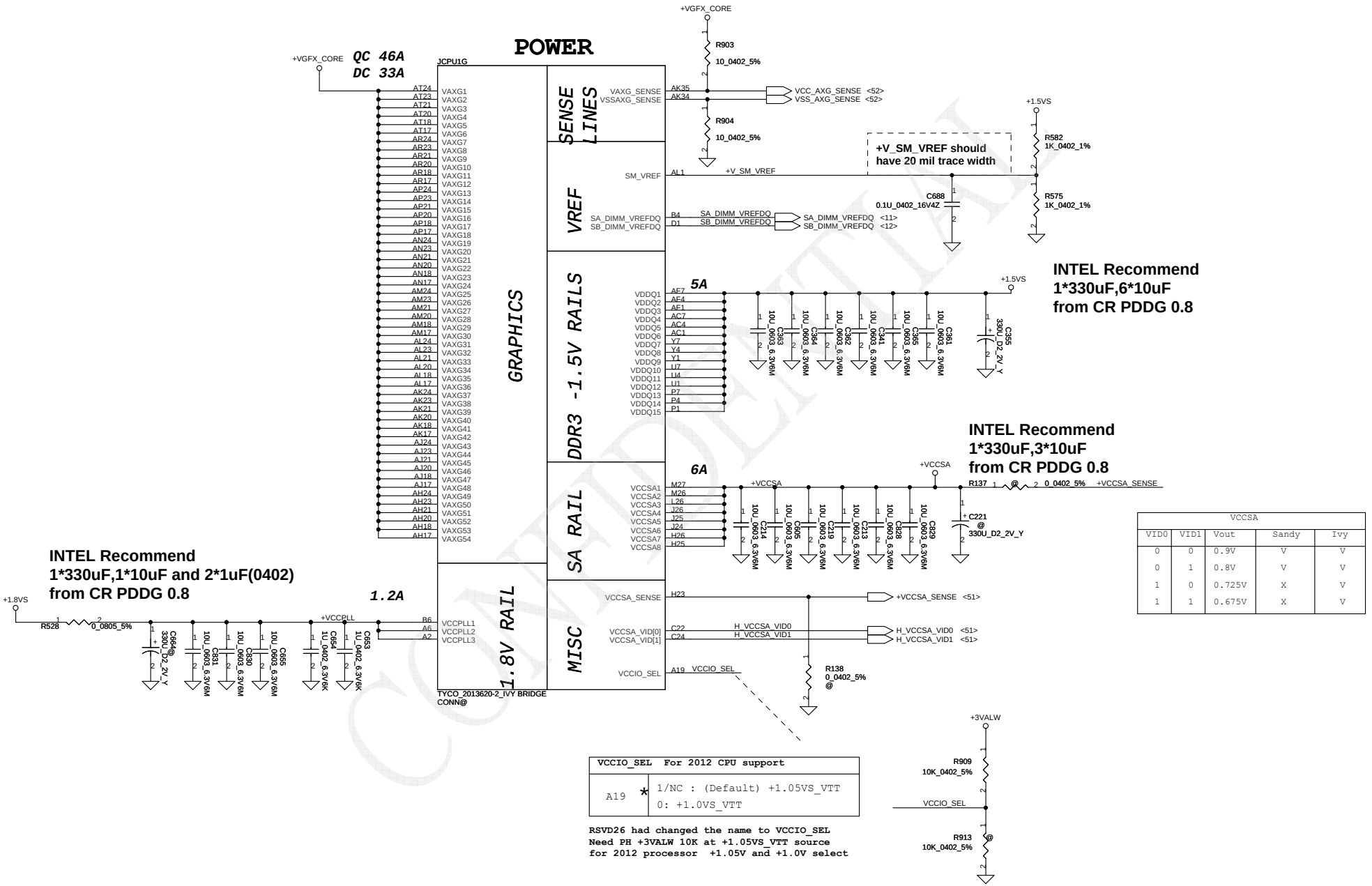

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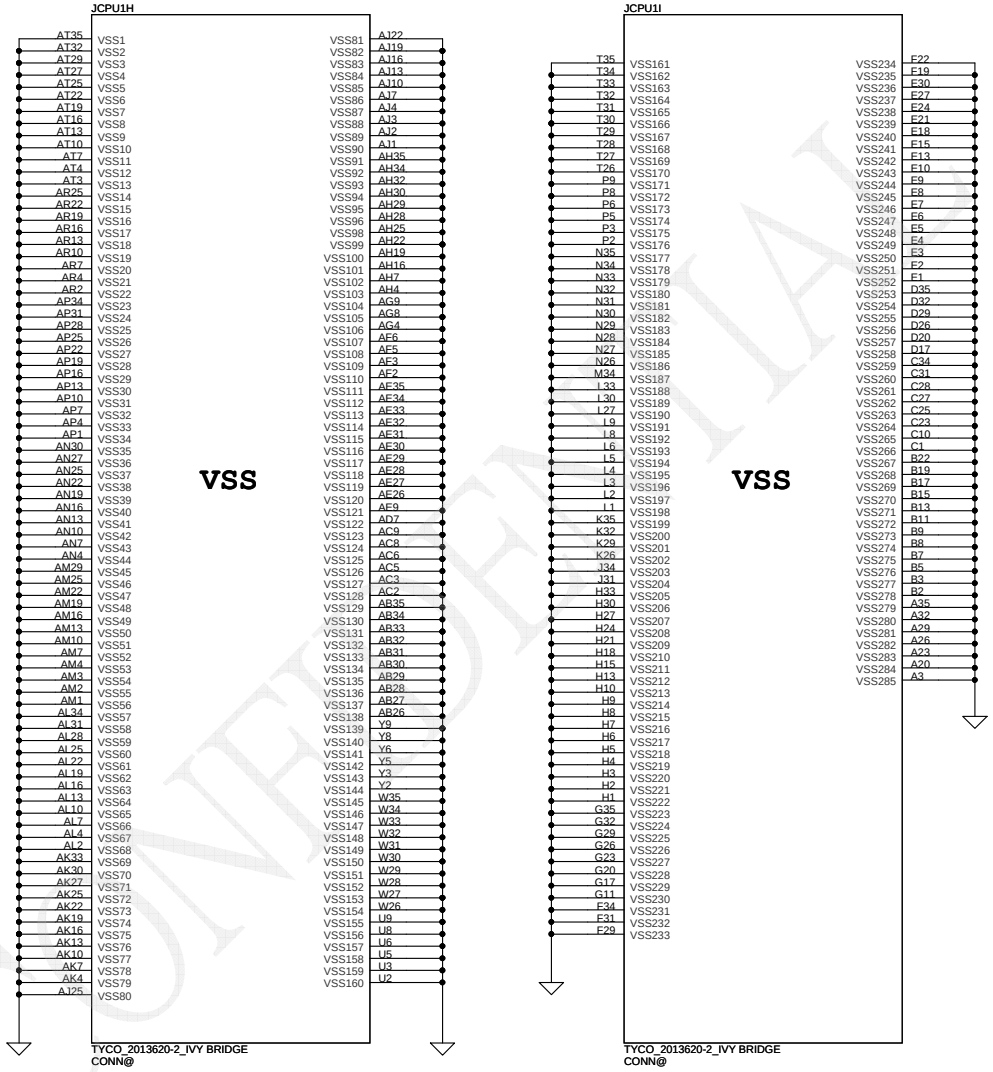

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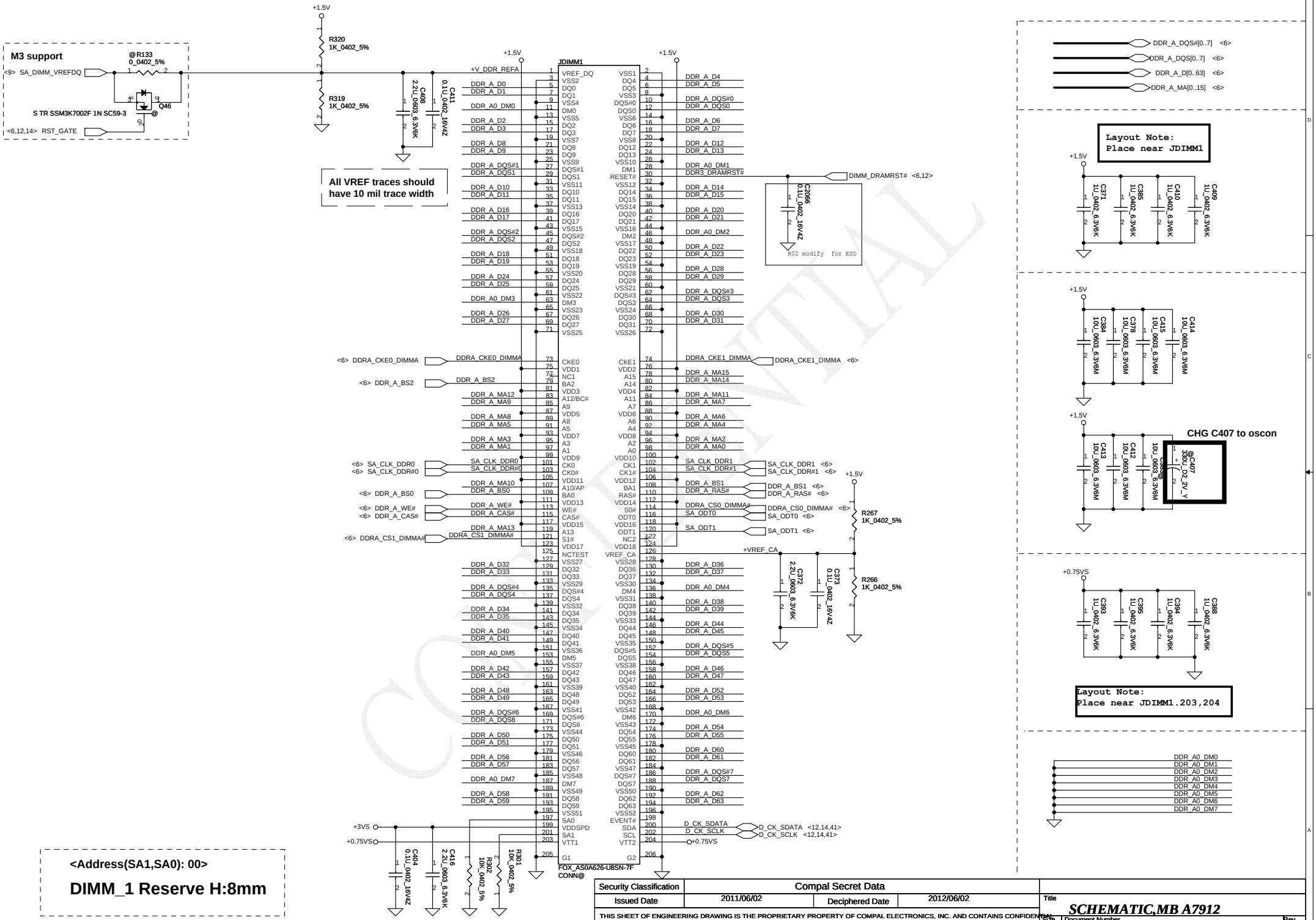

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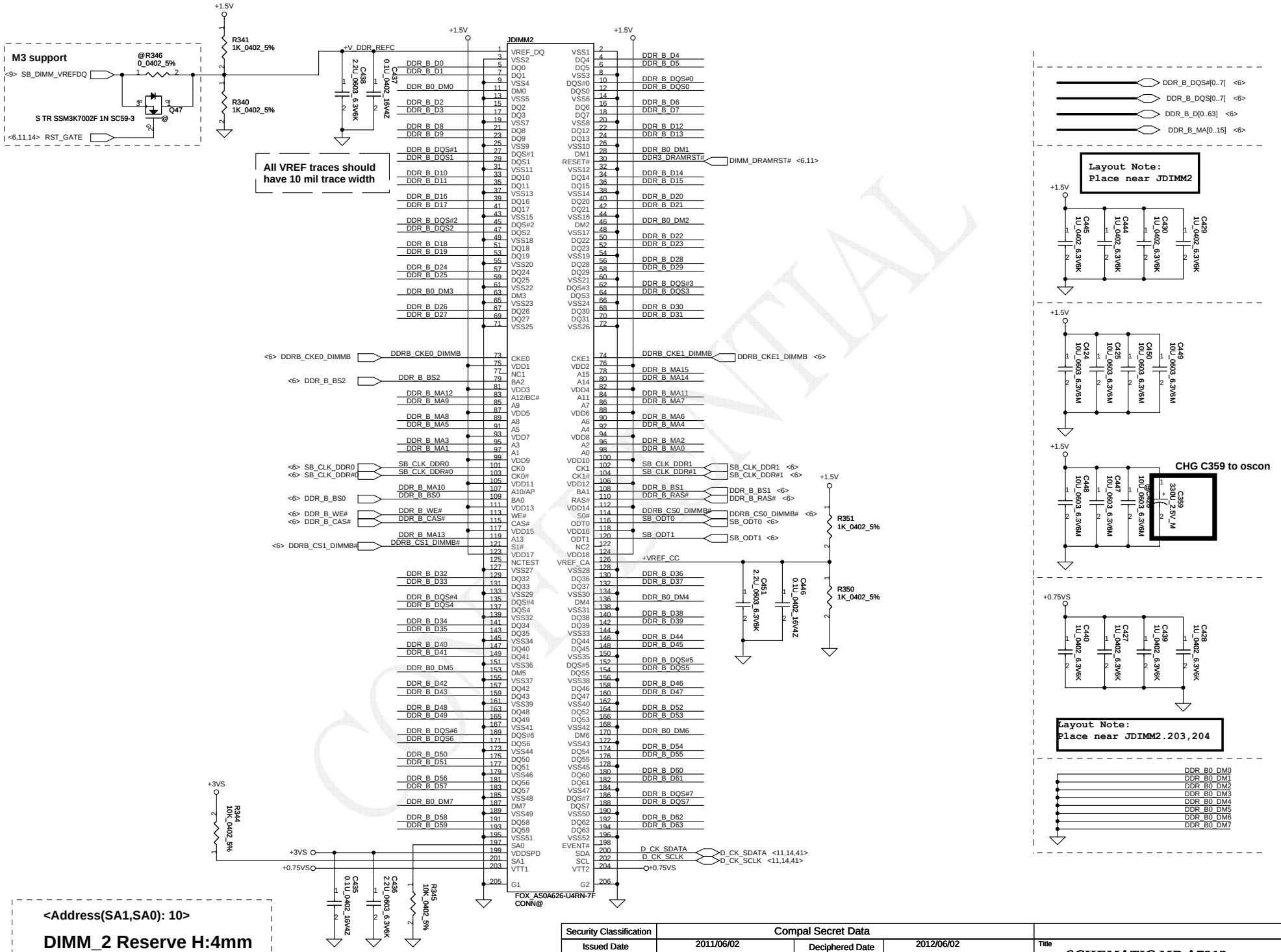

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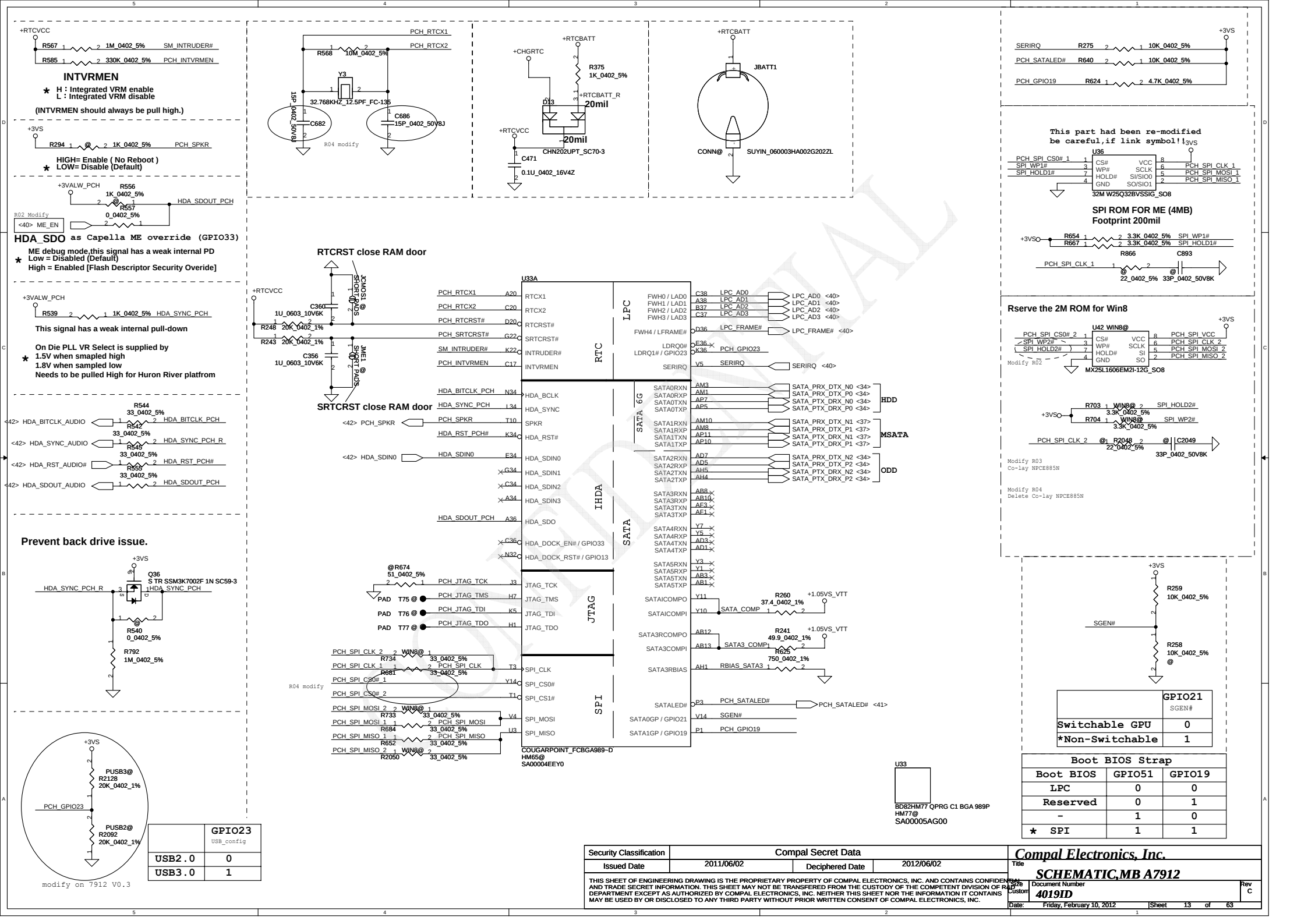

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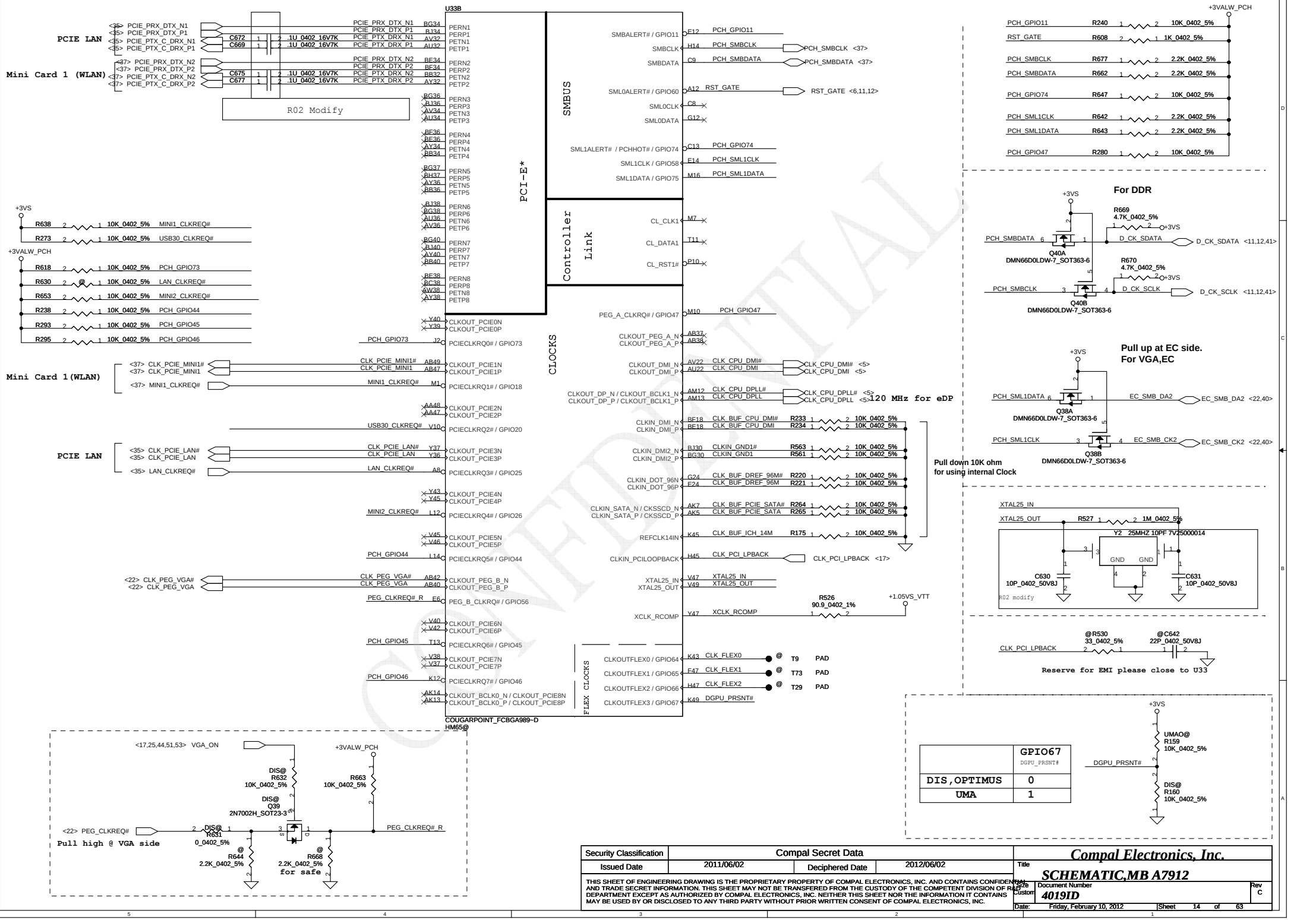

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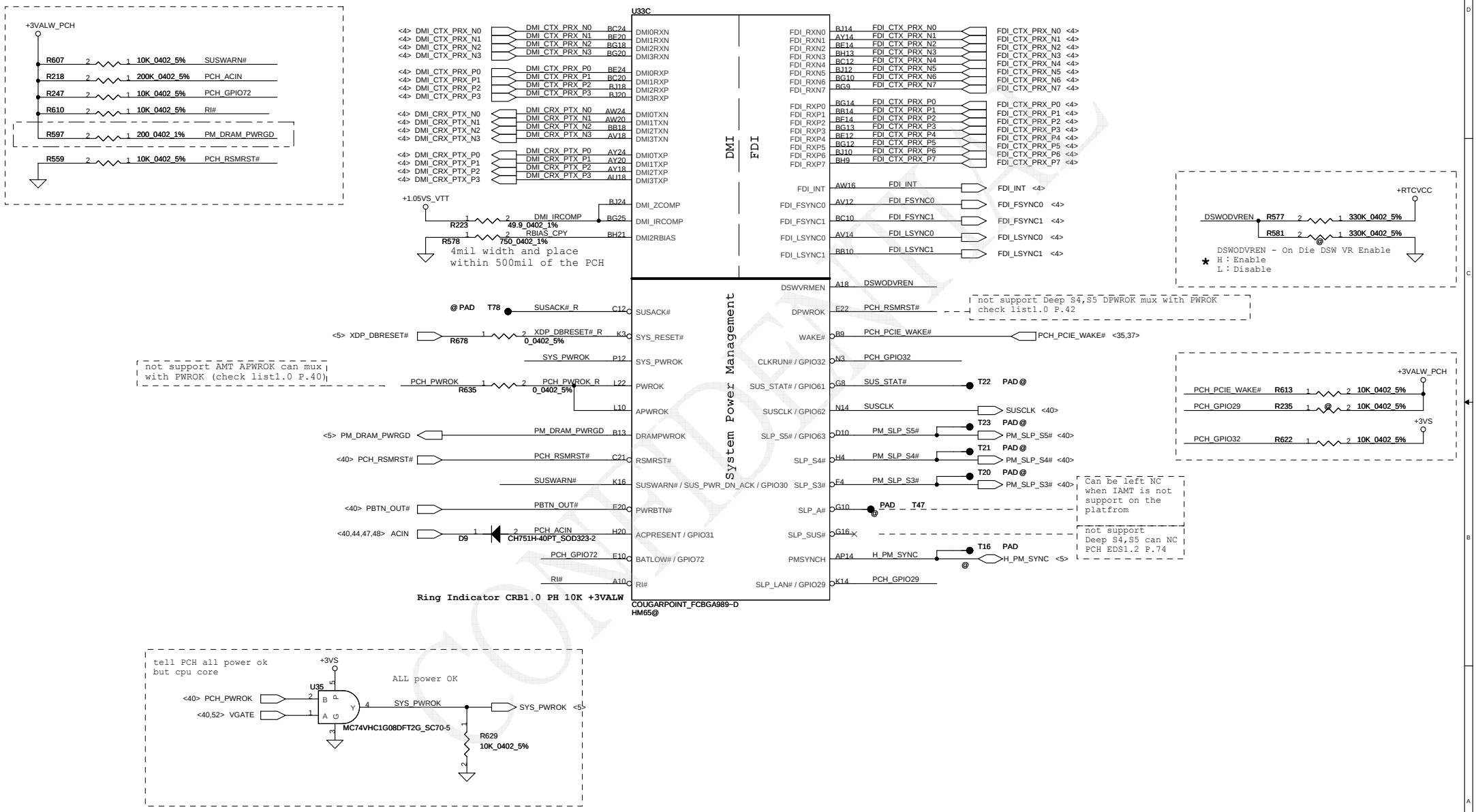

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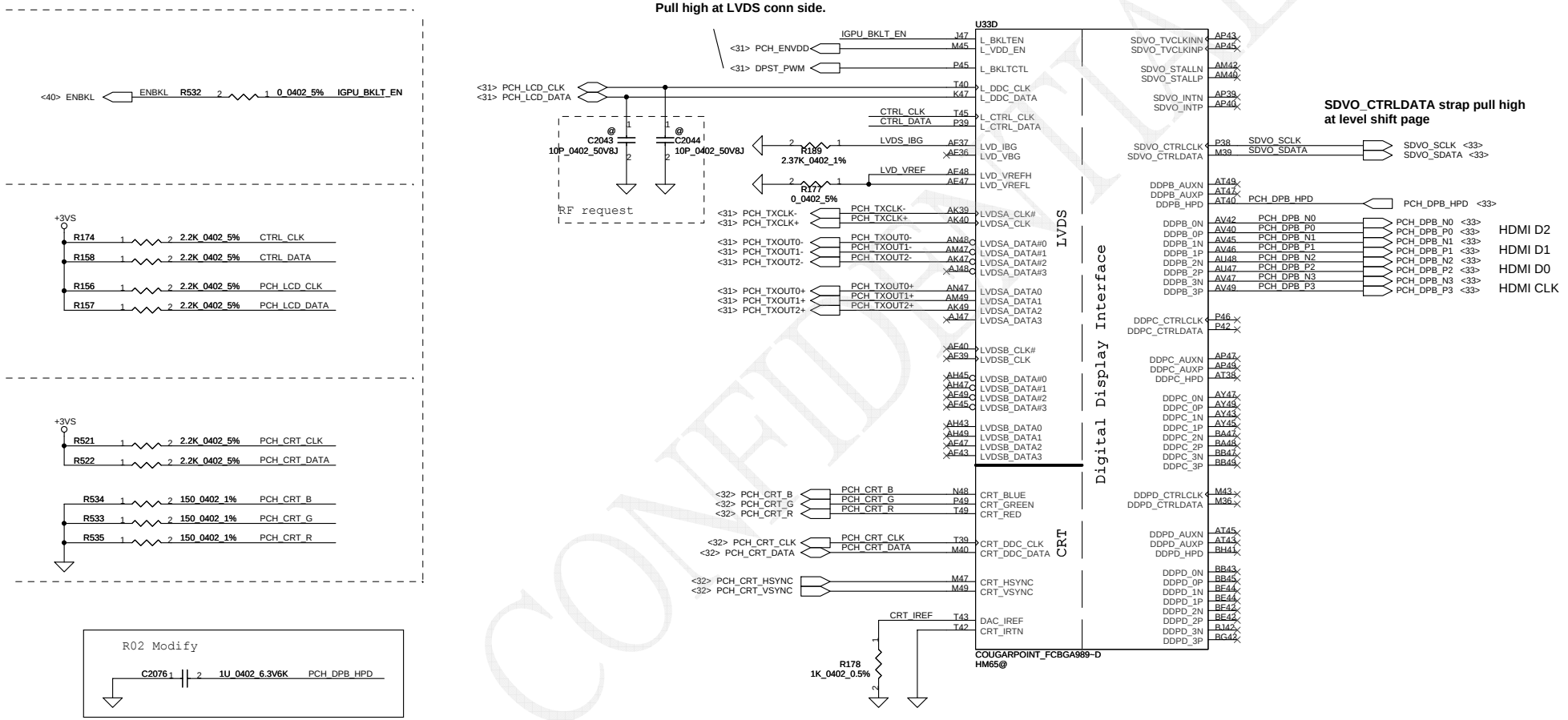

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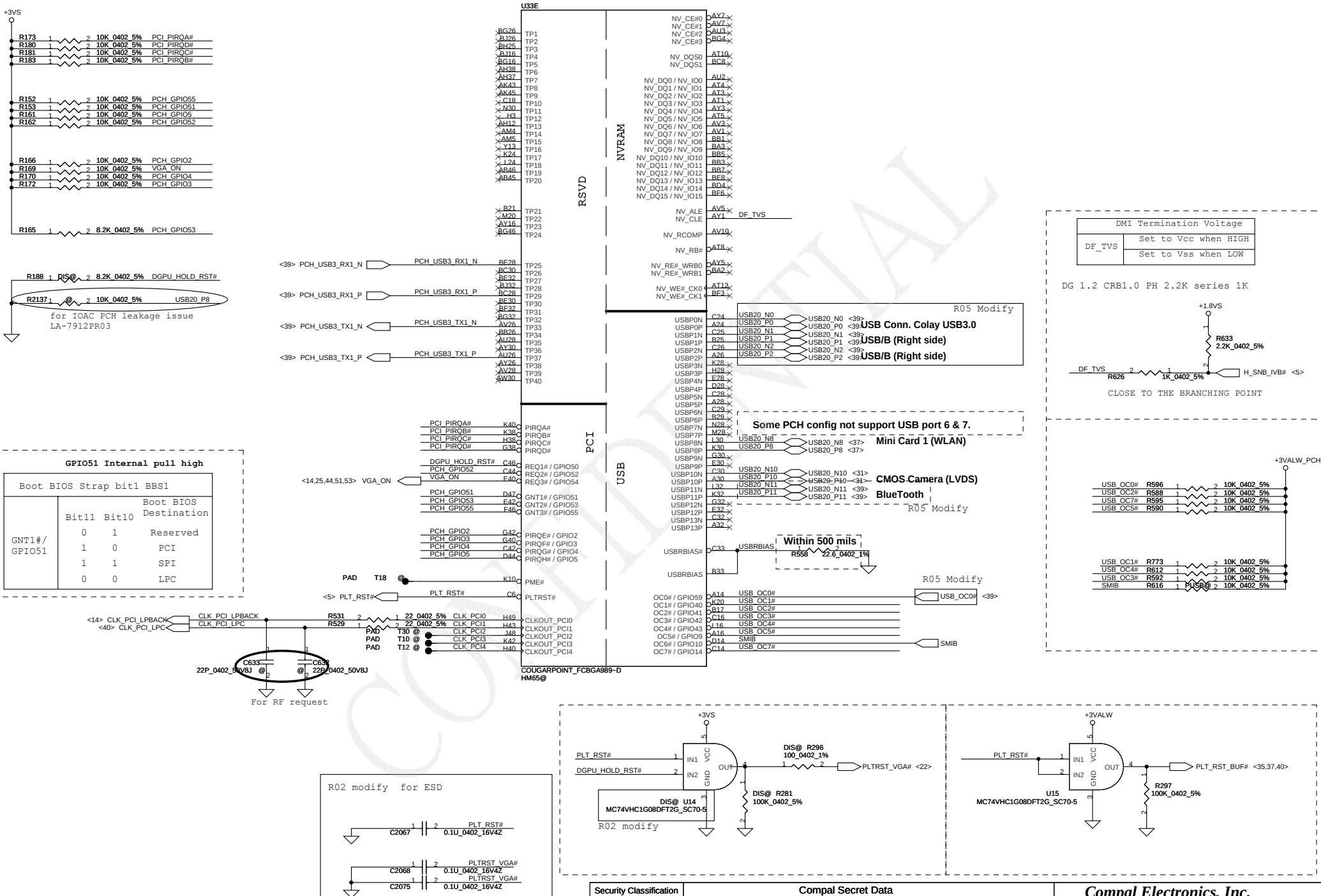

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HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

+3VALW_PCH
R768 4.7K_0402_5%
R272 @ 1K_0402_5%
PCH_GPIO28

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 10K_0402_5% PCH_GPIO27

+3VS
R623 @ 10K_0402_5% OPTIMUS_EN#
R639 DIS@ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1

+3VS
R277 @ 200K_0402_5% WWAN_OFF#
R276 10K_0402_5% PCH_GPIO0
R546 10K_0402_5% WL_EN#
R191 10K_0402_5% PCH_GPIO6
R641 10K_0402_5% MSATA_DET#
R290 10K_0402_5% PCH_GPIO22
R649 10K_0402_5% PCH_GPIO39
R291 @ 200K_0402_5% PCH_GPIO36
R619 NOAC@ 10K_0402_5% BT_ON#
R292 10K_0402_5% PCH_GPIO48
R274 NOAC@ 10K_0402_5% WL_OFF#

+3VALW_PCH
R262 10K_0402_5% PCH_GPIO24
R620 10K_0402_5% PCH_GPIO12
R672 1K_0402_5% EC_LID_OUT#
R263 10K_0402_5% PCH_GPIO57

R911 10K_0402_5% PCH_GPIO36
R912 10K_0402_5% WWAN_OFF#

+3VS
R2053 10K_0402_5%
DGPU_PWROK
+3VSDGPU
DIS@ R2055 10K_0402_5%
DIS@ R2054 10K_0402_5%
Q2001A DIS@ DMN66D0LDW-7_SOT363-6
DIS@ Q2001B DMN66D0LDW-7_SOT363-6
DIS@ C2050 0.1U_0402_16V4Z
DIS@ C2051 1U_0402_6.3V6K

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

U33F

	PCH_GPIO0	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40	PCH_GPIO68
<39> WL_EN#	WL_EN#	A42	TACH1 / GPIO1	TACH5 / GPIO69	B41	PCH_GPIO69
	PCH_GPIO6	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41	PCH_GPIO70
<40> EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40	PCH_GPIO71
<40> EC_SMI#	EC_SMI#	C10	GPIO8			
	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12			
<40> EC_LID_OUT#	EC_LID_OUT#	G2	GPIO15	A20GATE	P4	GATEA20 <40>
<37> MSATA_DET#	MSATA_DET#	U2	SATA4GP / GPIO16	PECI	AU16	H_PECI <5,40>
	DGPU_PWROK	D40	TACH0 / GPIO17	RCIN#	P5	EC_KBRST# <40>
	PCH_GPIO22	T5	SCLOCK / GPIO22	PROCPWRGD	AY11	H_CPUPWRGD <5>
	PCH_GPIO24	E8	GPIO24 / MEM_LED	THRMTRIP#	AY10	H_THRMTRIP# <5>
	PCH_GPIO27	E16	GPIO27	INIT3_3V#	T14	
	PCH_GPIO28	P8	GPIO28			
<37,39,40> BT_ON#	BT_ON#	K1	STP_PCI# / GPIO34			
		K4	GPIO35	NC_1	AH8	
	PCH_GPIO36	V8	SATA2GP / GPIO36	NC_2	AK11	
WWAN_OFF#	WWAN_OFF#	M5	SATA3GP / GPIO37	NC_3	AH10	
	OPTIMUS_EN#	N2	SLOAD / GPIO38	NC_4	AK10	
	PCH_GPIO39	M3	SDATAOUT0 / GPIO39	NC_5	P37	
	PCH_GPIO48	V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2	
<37,40> WL_OFF#	WL_OFF#	V3	SATA5GP / GPIO49	VSS_NCTF_16	BG48	
	PCH_GPIO57	D6	GPIO57	VSS_NCTF_17	BH3	
				VSS_NCTF_18	BH47	
		A4	VSS_NCTF_1	VSS_NCTF_19	BJ4	
		A44	VSS_NCTF_2	VSS_NCTF_20	BJ44	
		A45	VSS_NCTF_3	VSS_NCTF_21	BJ45	
		A46	VSS_NCTF_4	VSS_NCTF_22	BJ46	
		A5	VSS_NCTF_5	VSS_NCTF_23	BJ5	
		A6	VSS_NCTF_6	VSS_NCTF_24	BJ6	
		B3	VSS_NCTF_7	VSS_NCTF_25	C2	
		B47	VSS_NCTF_8	VSS_NCTF_26	C48	
		BD1	VSS_NCTF_9	VSS_NCTF_27	D1	
		BD49	VSS_NCTF_10	VSS_NCTF_28	D49	
		BE1	VSS_NCTF_11	VSS_NCTF_29	E1	
		BE49	VSS_NCTF_12	VSS_NCTF_30	E49	
		BF1	VSS_NCTF_13	VSS_NCTF_31	F1	
		BF49	VSS_NCTF_14	VSS_NCTF_32	F49	

GPIO
CPU/MISC
NCTF

COUGARPOINT_FCBGA989~D
HM65@

+3VS
R278 10K_0402_5%
PCH_PECI CPU-EC
R627 390_0402_5%
CTRL+ALT+DEL
non CPU power ok
I30 degree shut sown

iNIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4 PD to GND

+3VS
PCH_GPIO68 R771 10K_0402_5%
EC_KBRST# R279 10K_0402_5%

+3VS
R554 10K_0402_5%
R548 10K_0402_5%
PCH_GPIO69
PCH_GPIO70
R553 10K_0402_5%
R549 10K_0402_5%

Project ID	GPIO69	GPIO70
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

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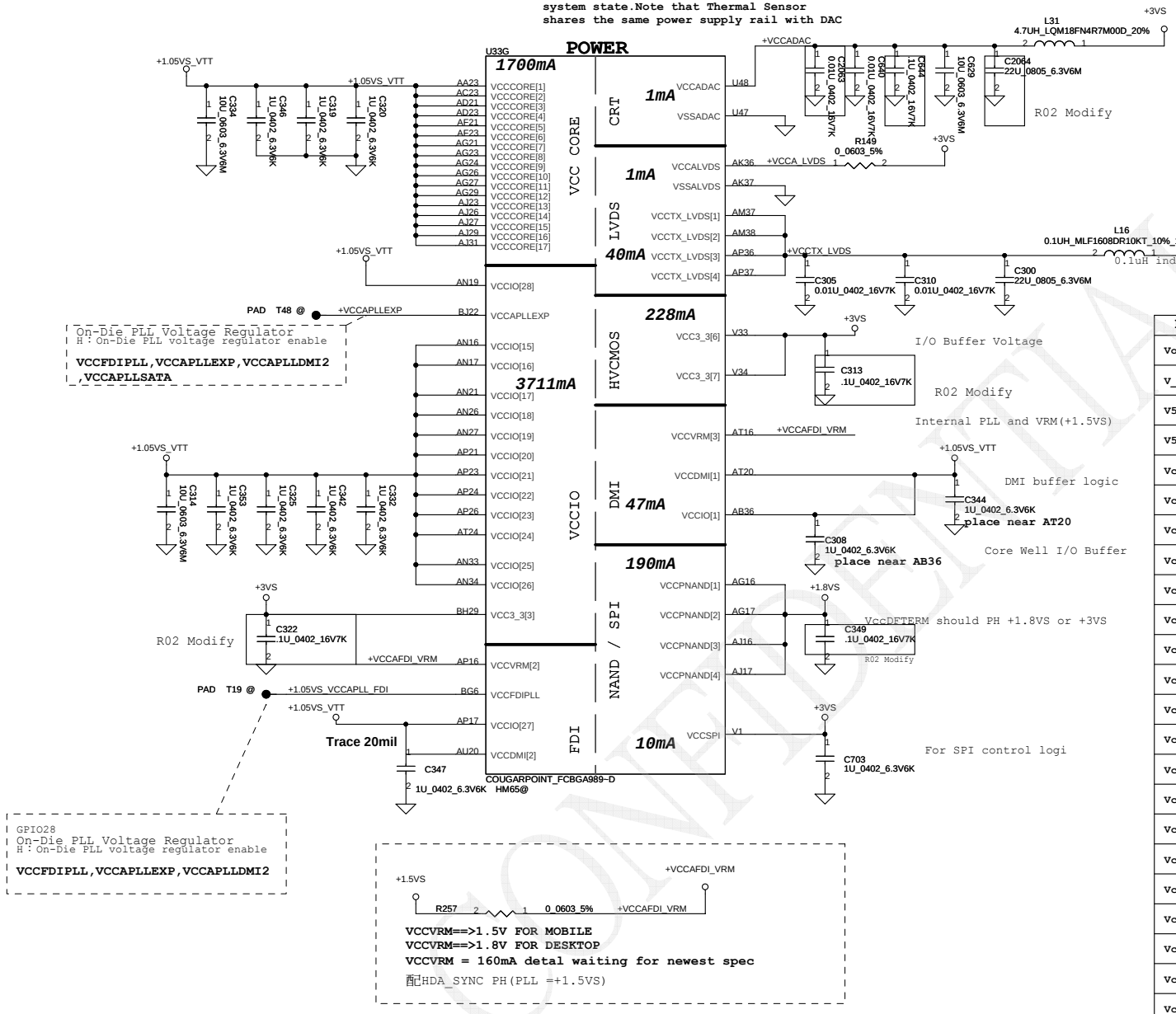

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

+5VALW TO +5VALW_PCH(PCH AUX Power)

POWER

Have internal VRM

U33J

Not support Deep S4,S5 connect to +3VALW

supplied by internal 1.05V VR must NC

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

SGA00001700
220U 2.5V M B2
ESR 35mohm@100Khz

R03 Modify

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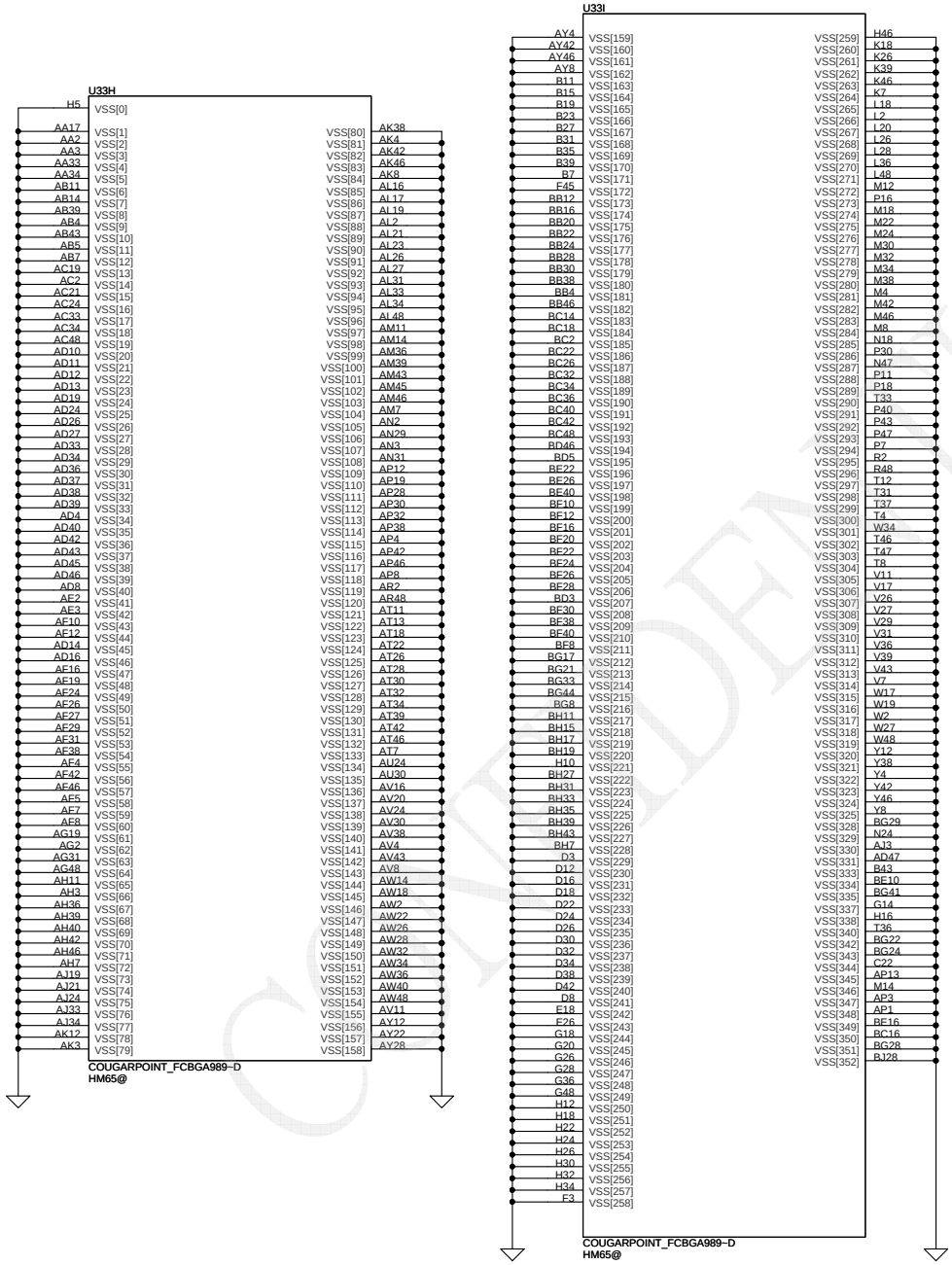

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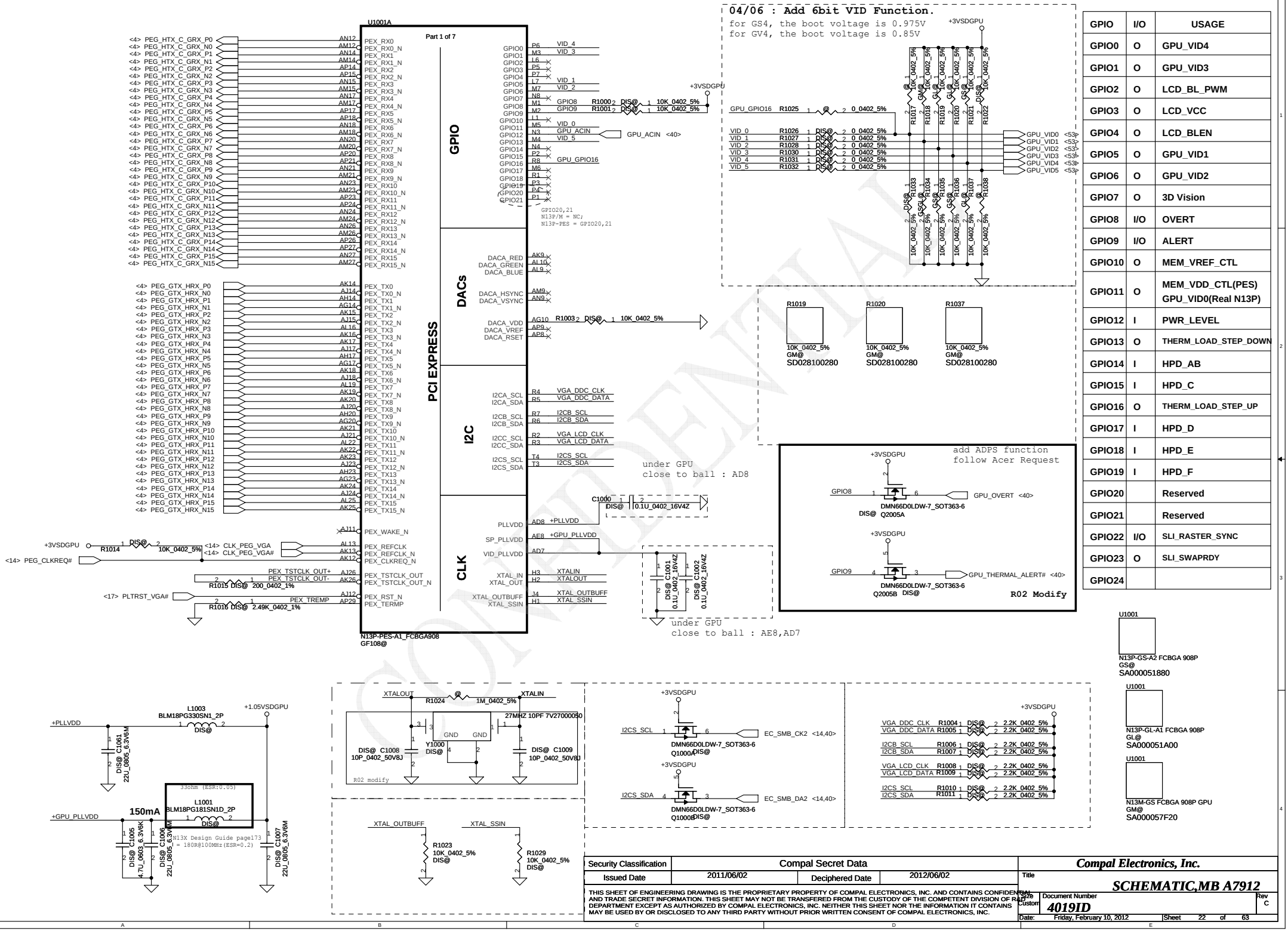

GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

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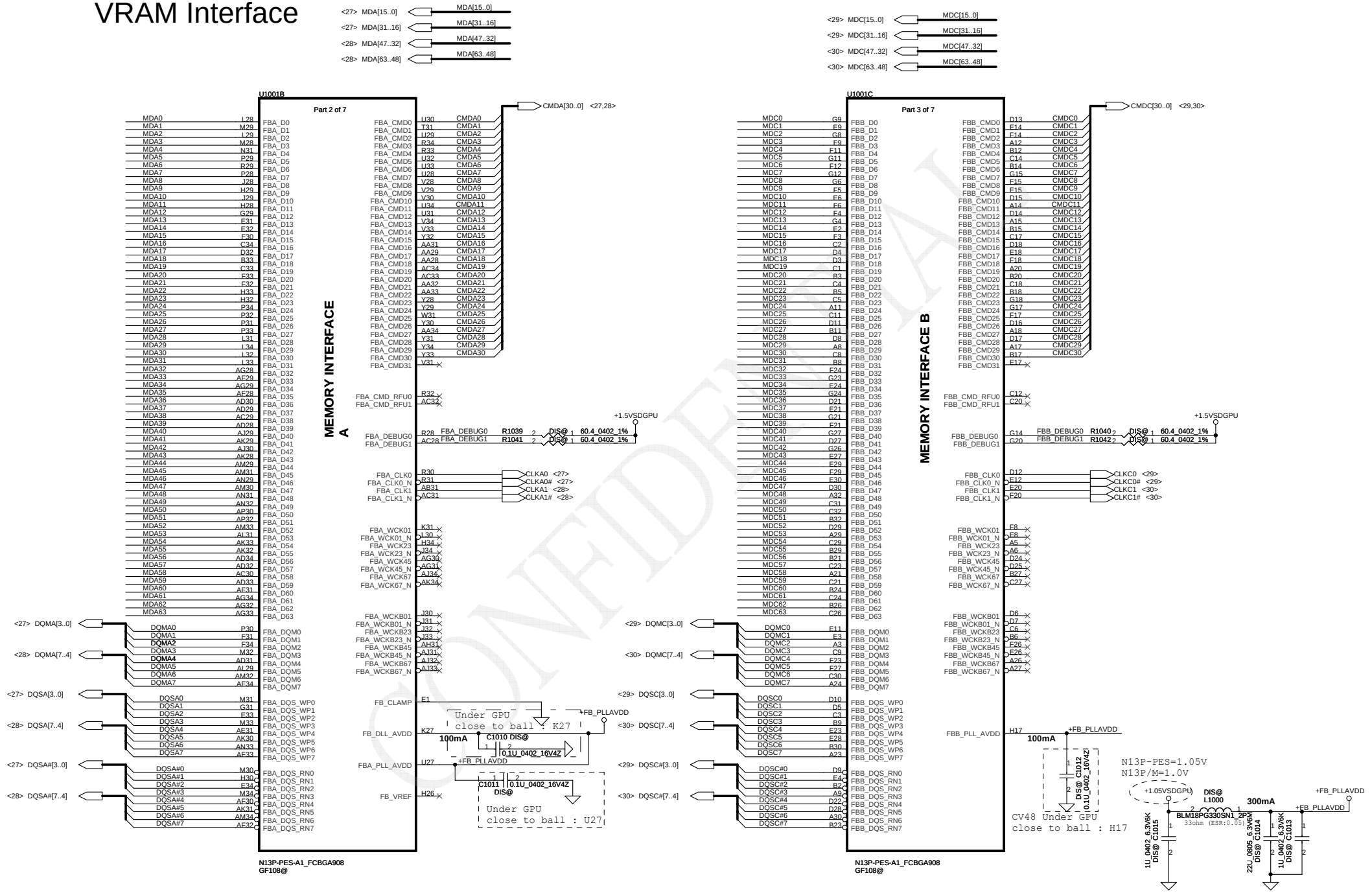
VRAM Interface



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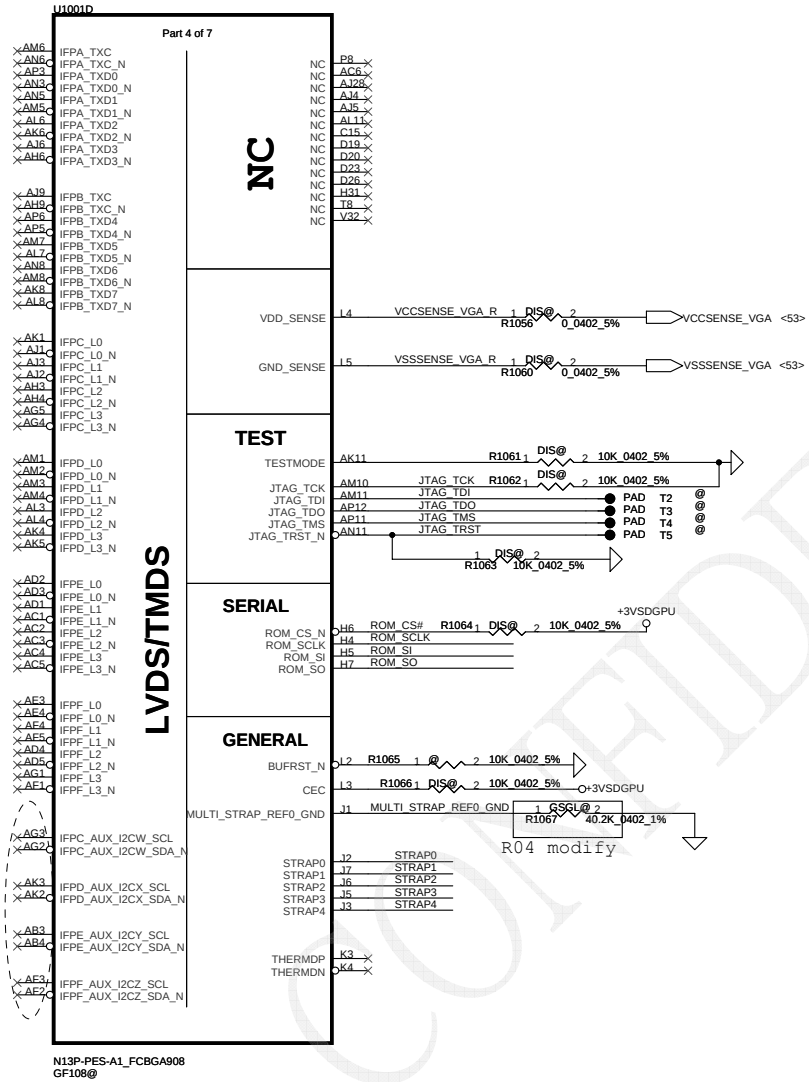

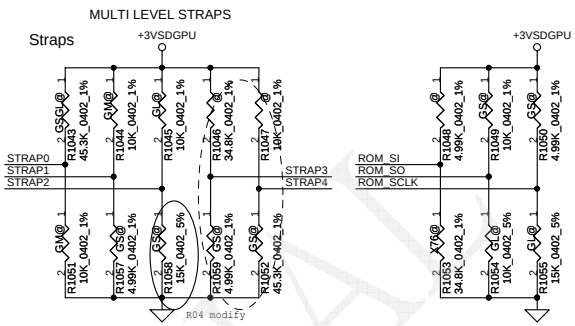

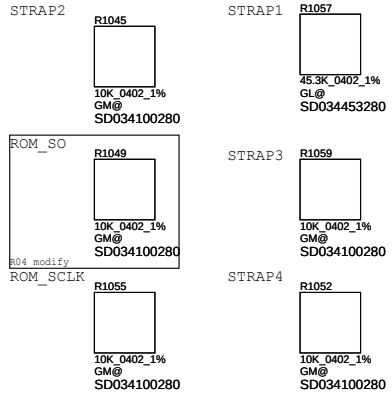

For N13P-GS(QS) strap table (PN:SA000051880)

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 15K	R PU 10K	R PU 5K

For N13P-GL(QS) strap table (PN:SA000051A00)

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

For N13M-GS(QS) strap table (PN:SA000051A00)

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PU 10K	R PD 10K

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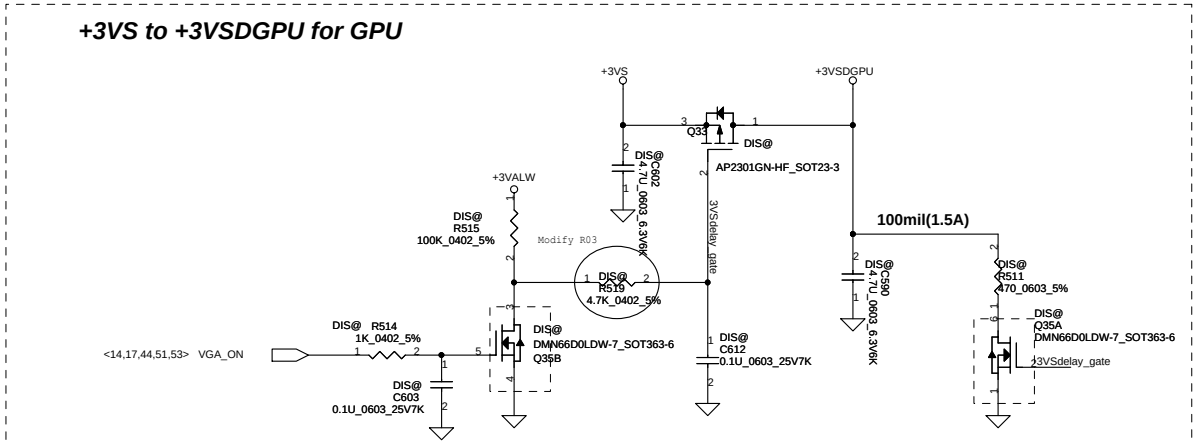
+3VS to +3VSDGPU for GPU



Design guide no define

U1001E

Part 5 of 7

POWER

7200mA

2700 mA
total 2700mA
Design guide page.68

150mA

370mA

150mA

120mA

Design guide no define

Reference Sch = 300R@100MHz
Design Guide page69 沒定義

L1002 BLM18PG121SN1D_0603 GL@ N13P

L1002 0_0603_5% GM@ SD013000080

L1002 0_0603_5% GS@ SD013000080

N13P-PES-A1_FCBGA908
GF108@

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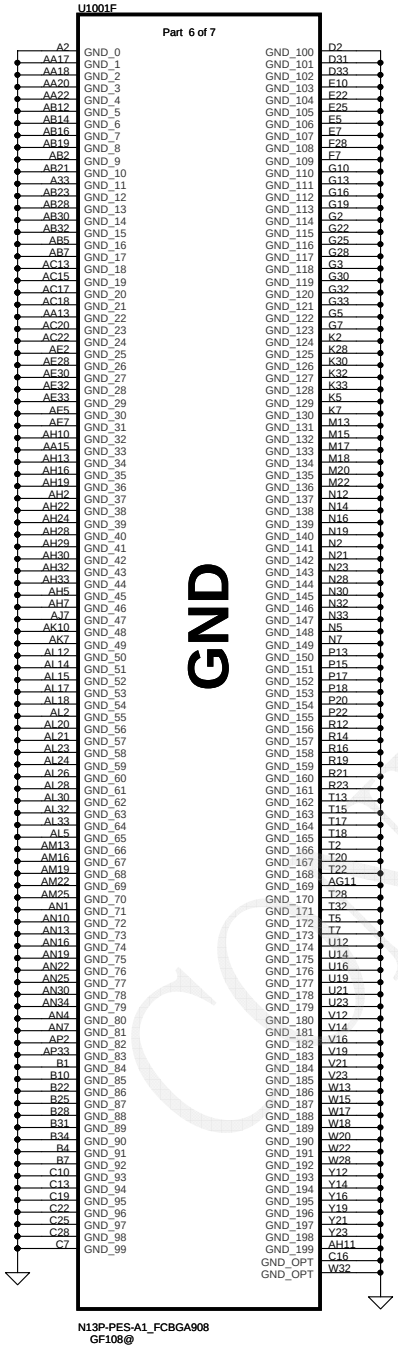

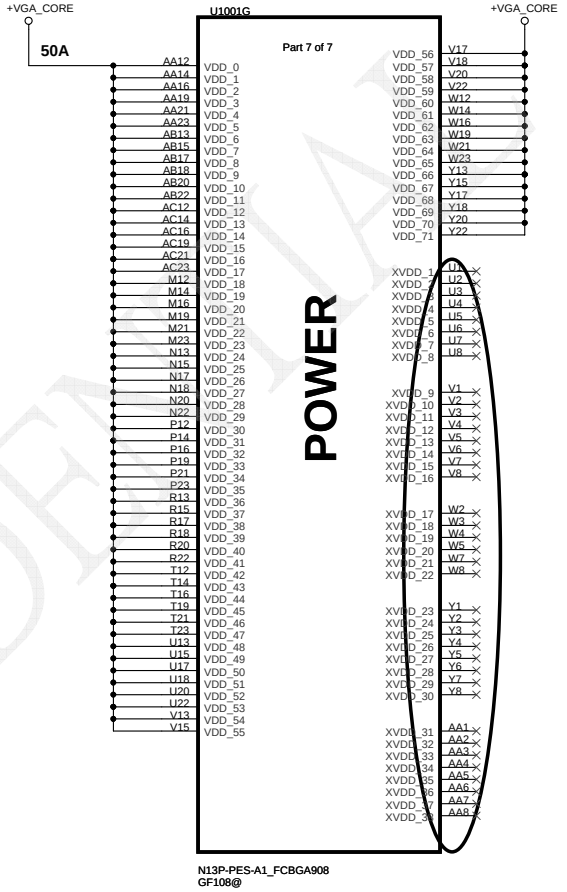

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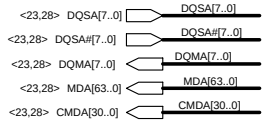
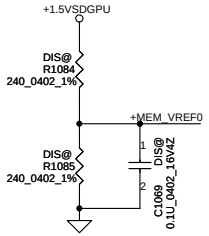
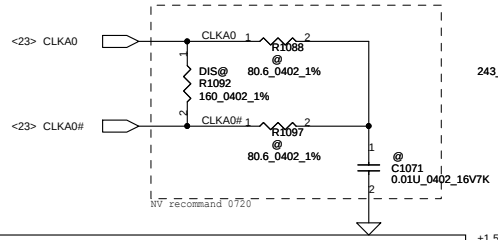
VRAM DDR3 chips (1GB)

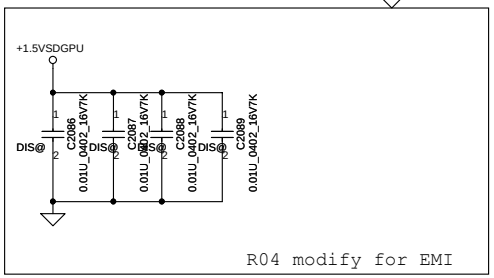
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

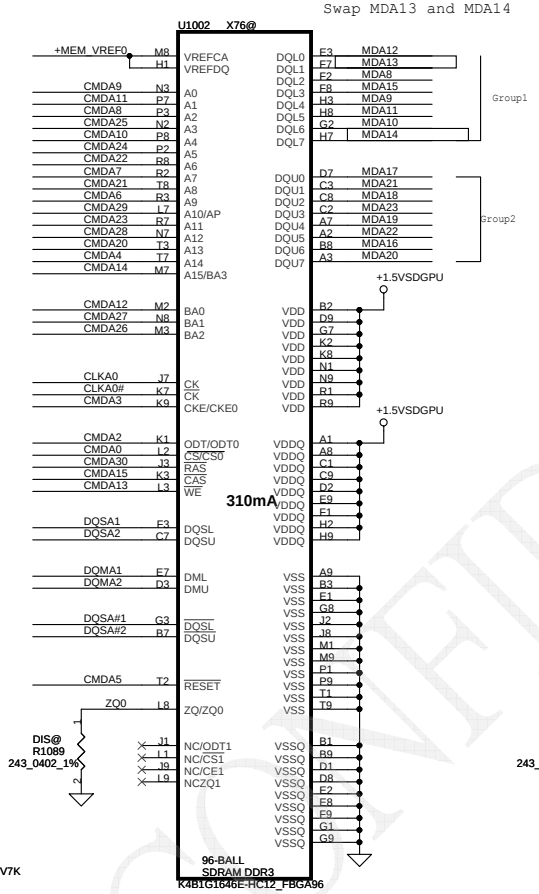
R02 modify
Swap MDA13 and MDA14

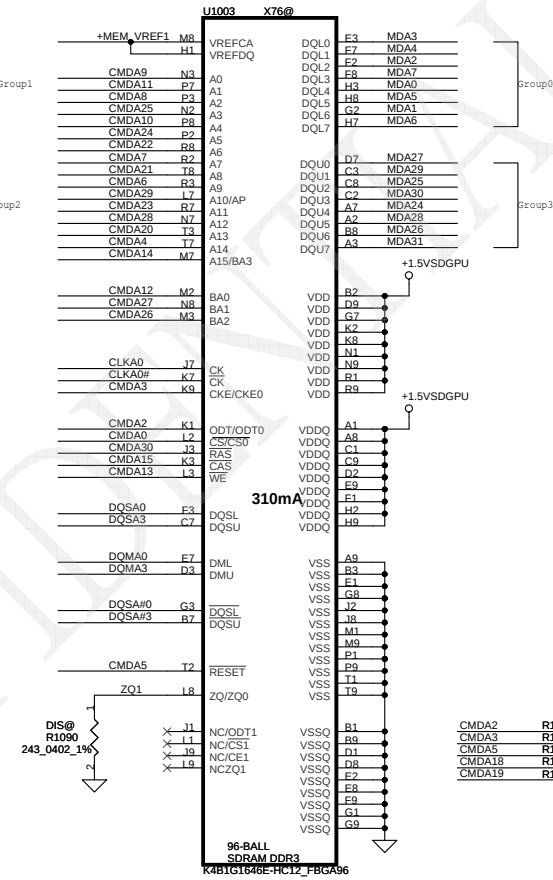


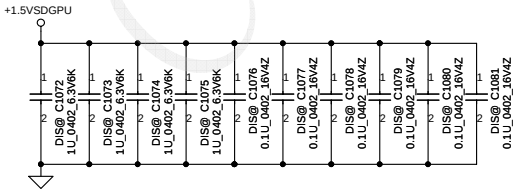


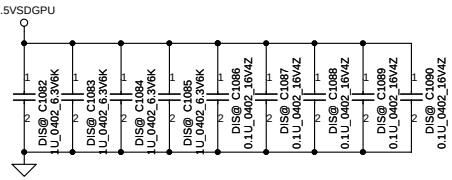


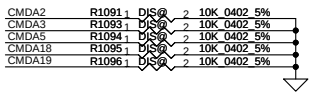












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Hynix : SA00003YO20 (S IC D3 128M16 H5TQ2G63BFR-11C FBGA)
Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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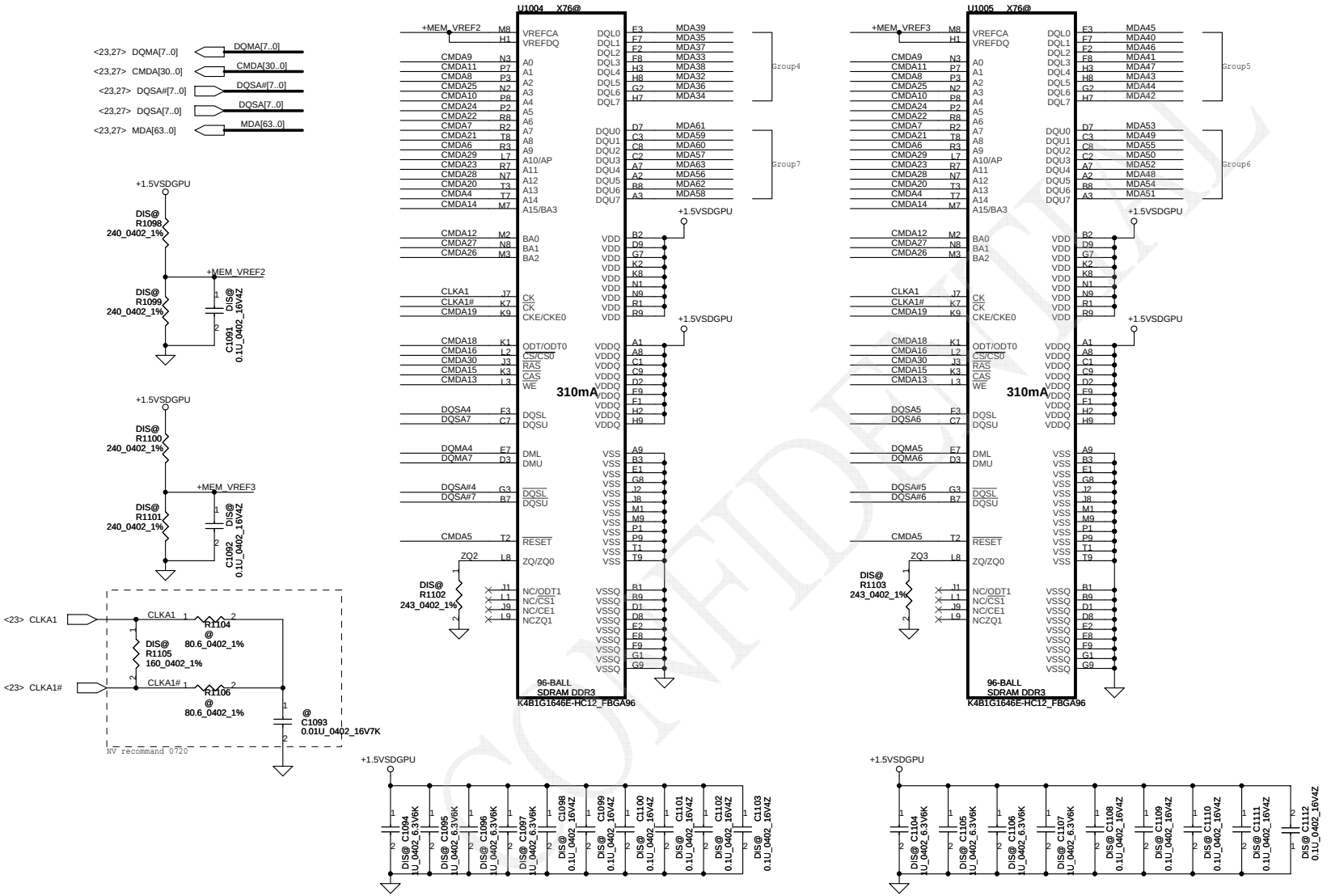
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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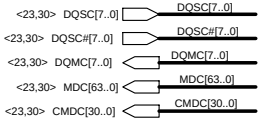
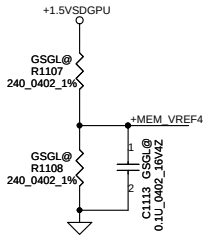
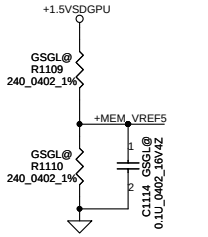
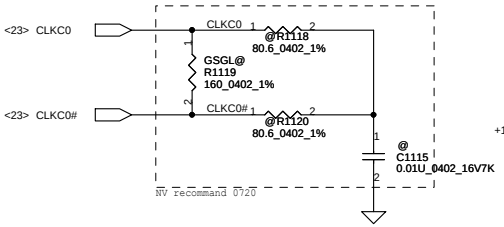
VRAM DDR3 chips (1GB)

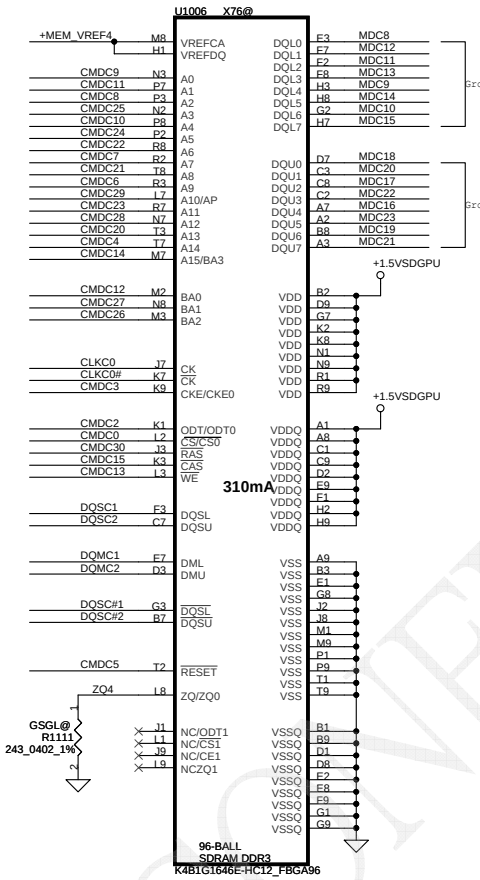
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

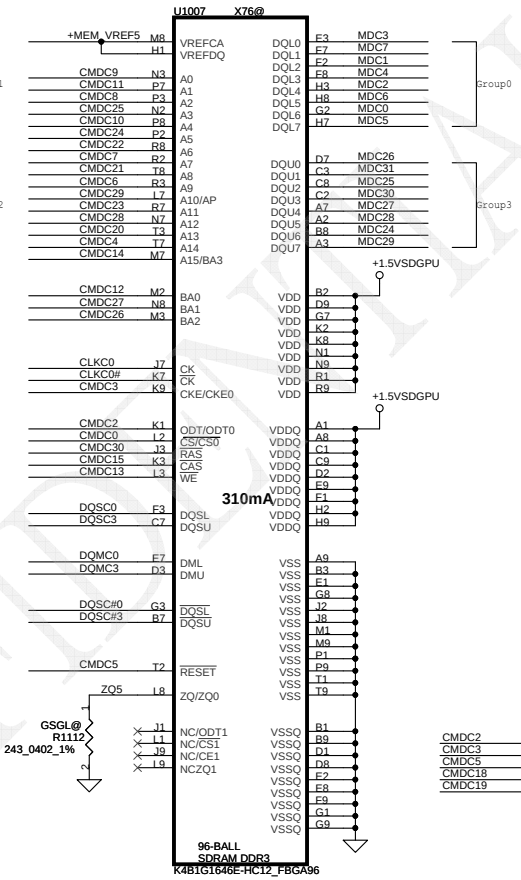


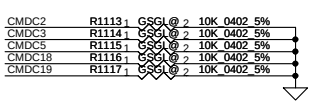




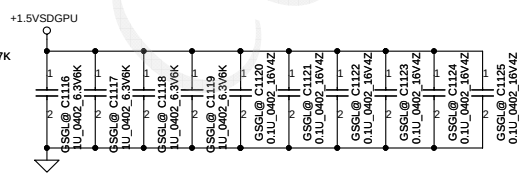


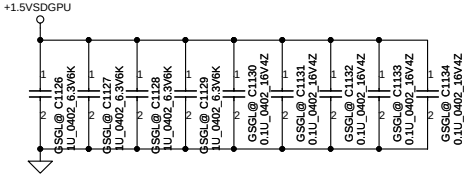






	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
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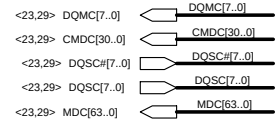
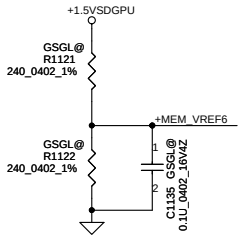
VRAM DDR3 chips (1GB)

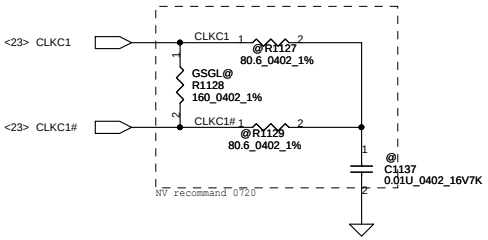
64Mx16 DDR3 *8==>1GB

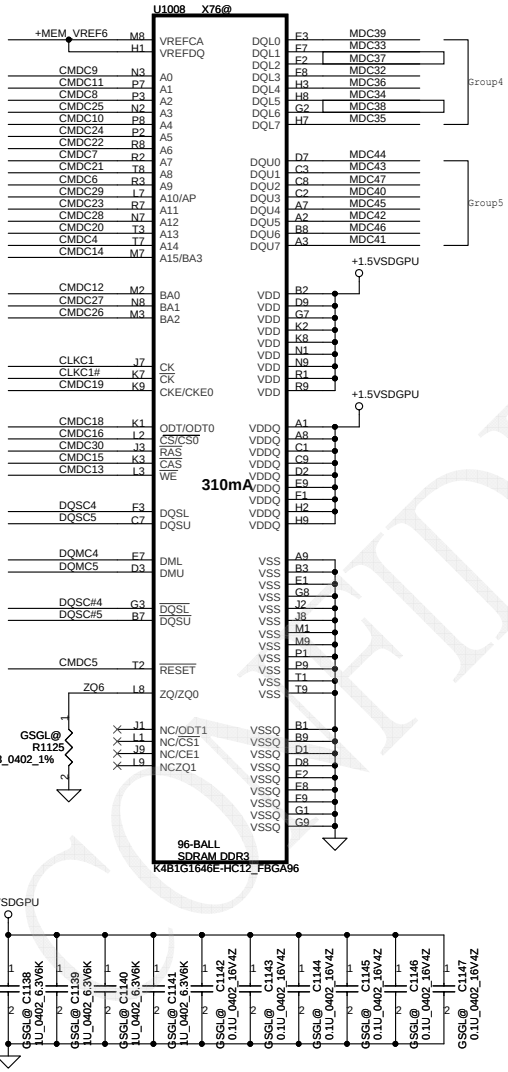
128Mx16 DDR3 *8==>2GB

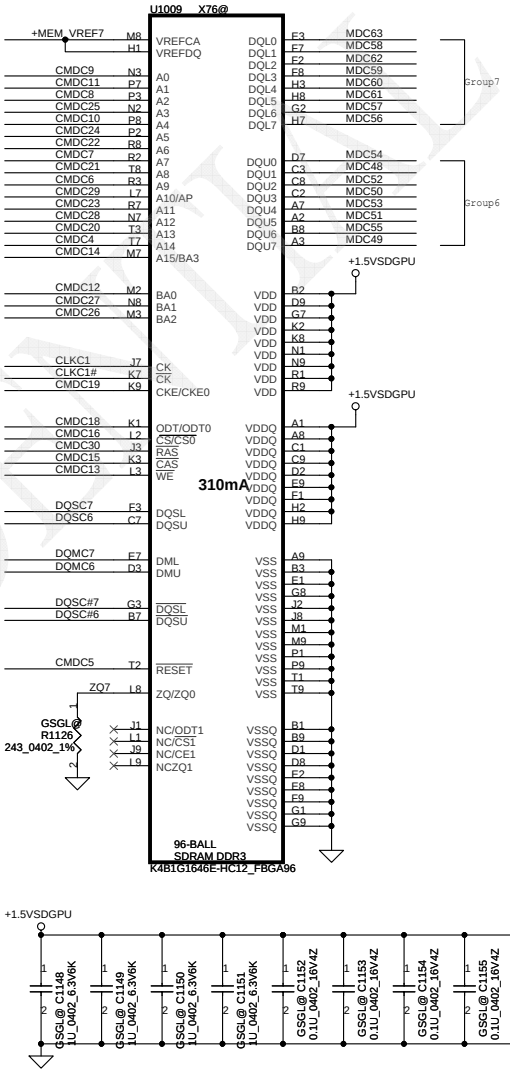
R02 modify
Swap MDC37 and MDC38











Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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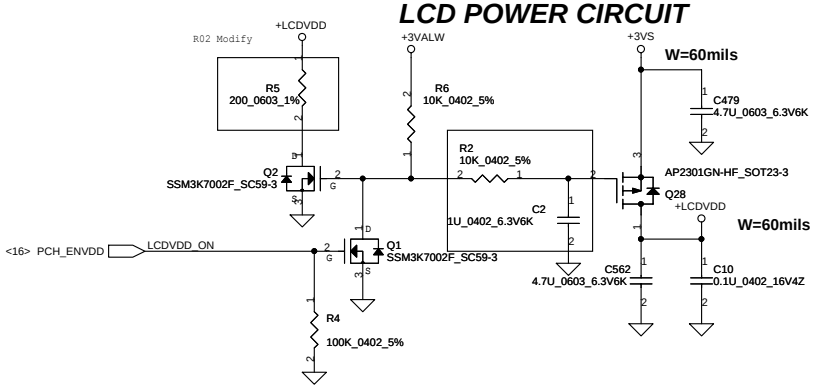
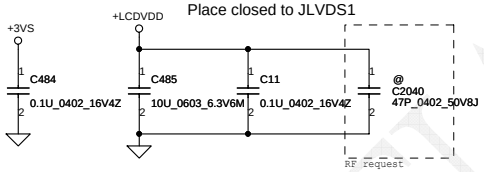
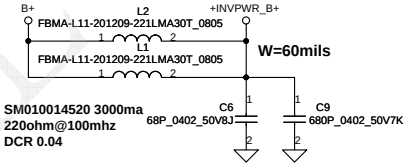
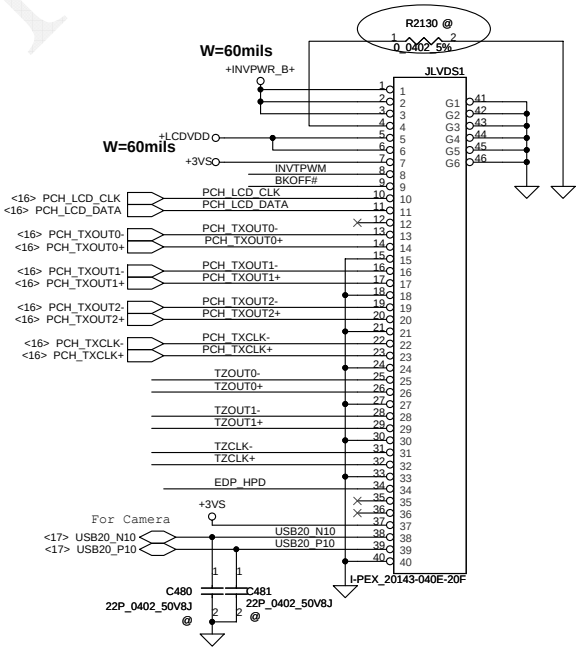
LCD POWER CIRCUIT



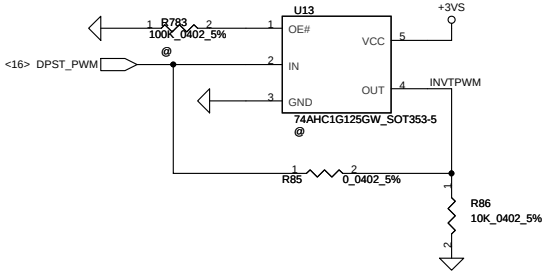


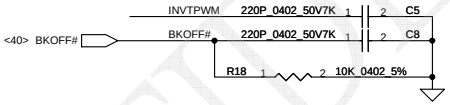


LCD/LED PANEL Conn.

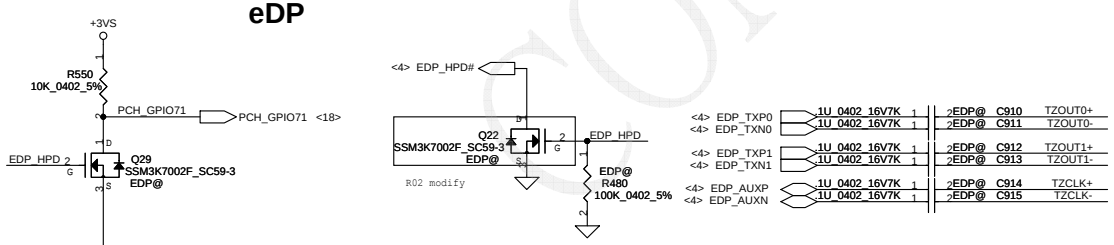


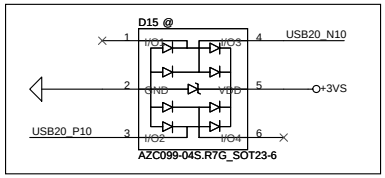
add on 7912_0.3





eDP





Modify R02

	GPIO71 PCH_GPIO71
eDP	0
LVDS	1

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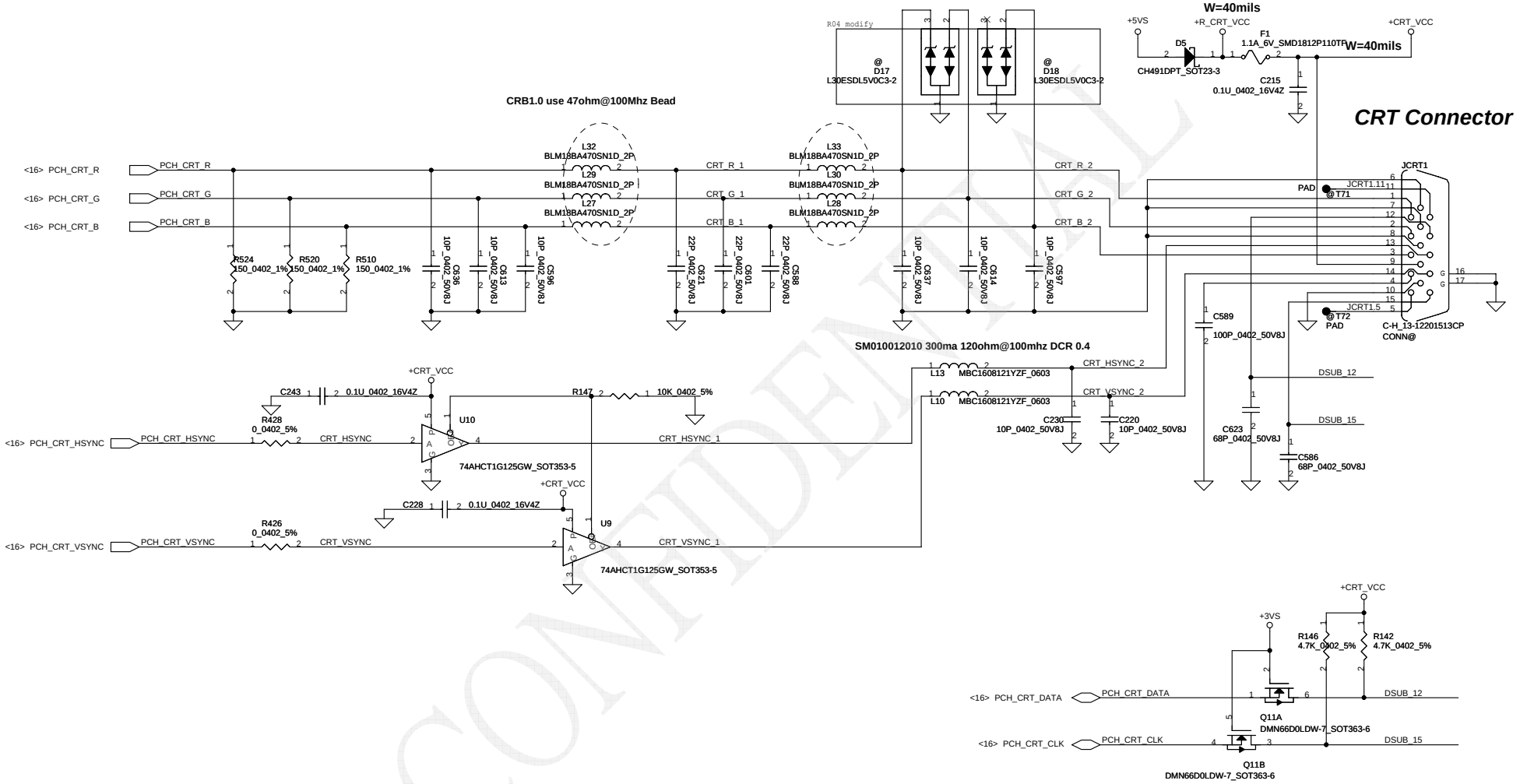

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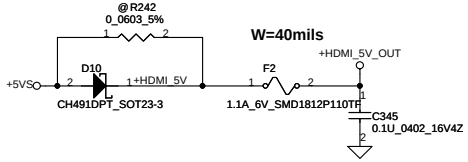
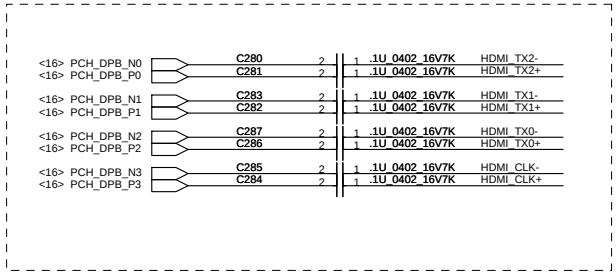
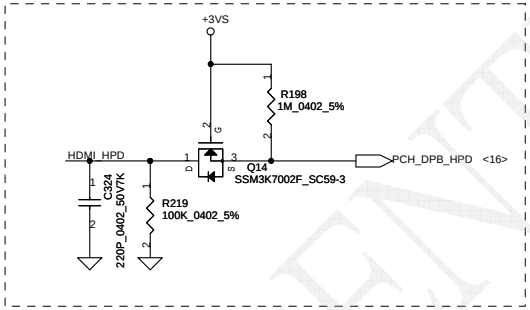
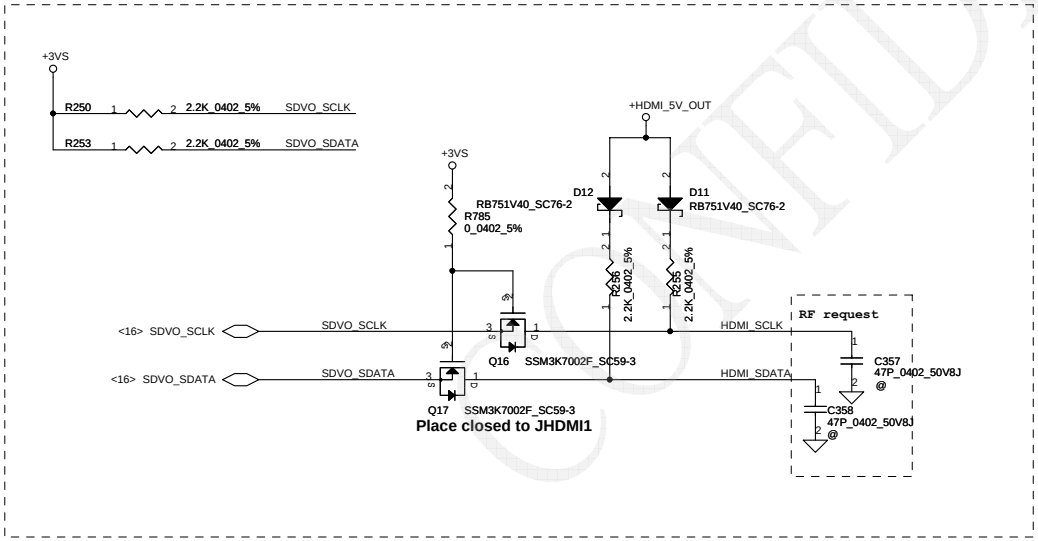
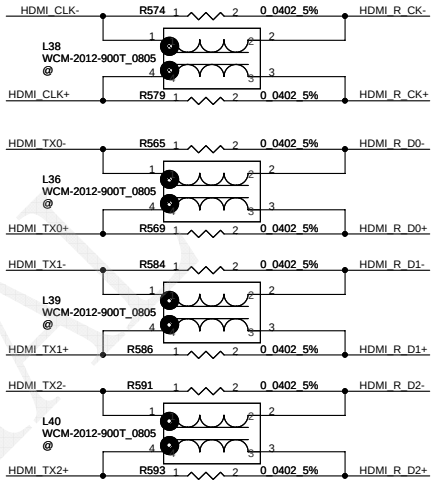


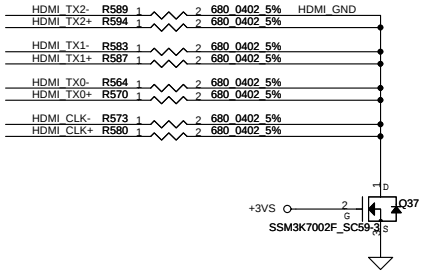


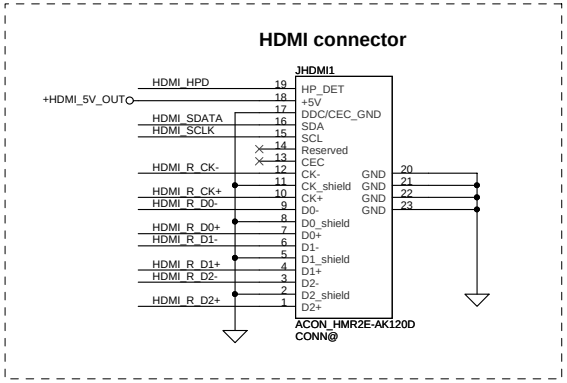




SM070001310 400ma 90ohm@100mhz DCR 0.3







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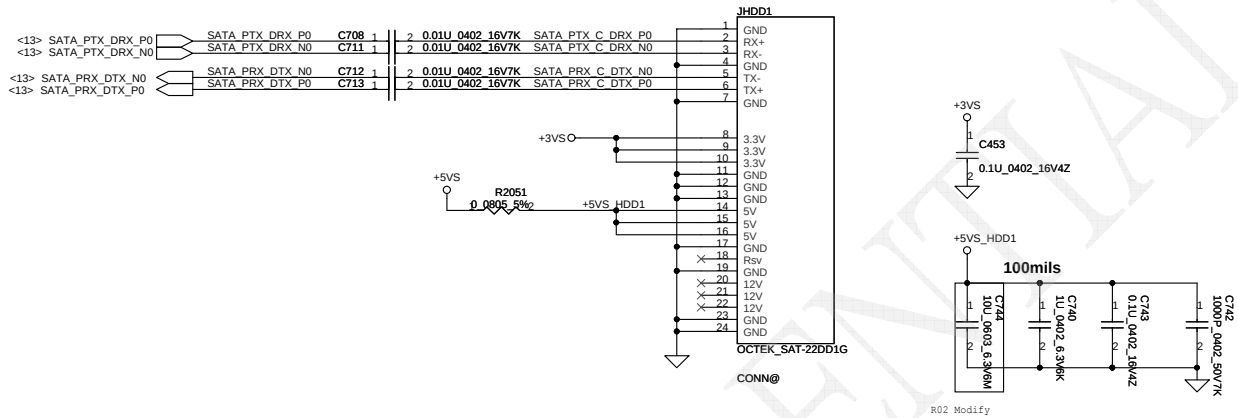
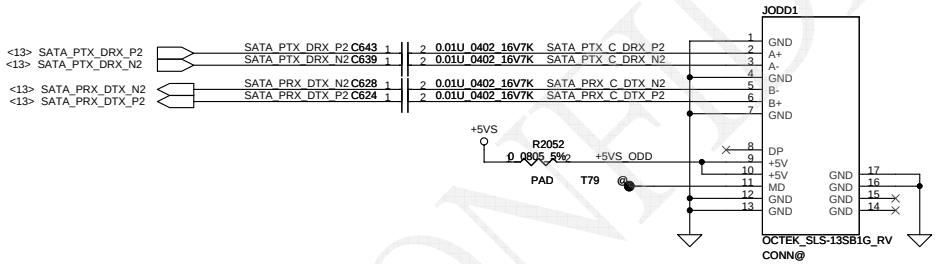
SATA HDD1 Conn.

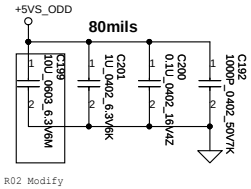
CL 4.0 mm



R02 Modify

SATA ODD Conn.





R02 Modify

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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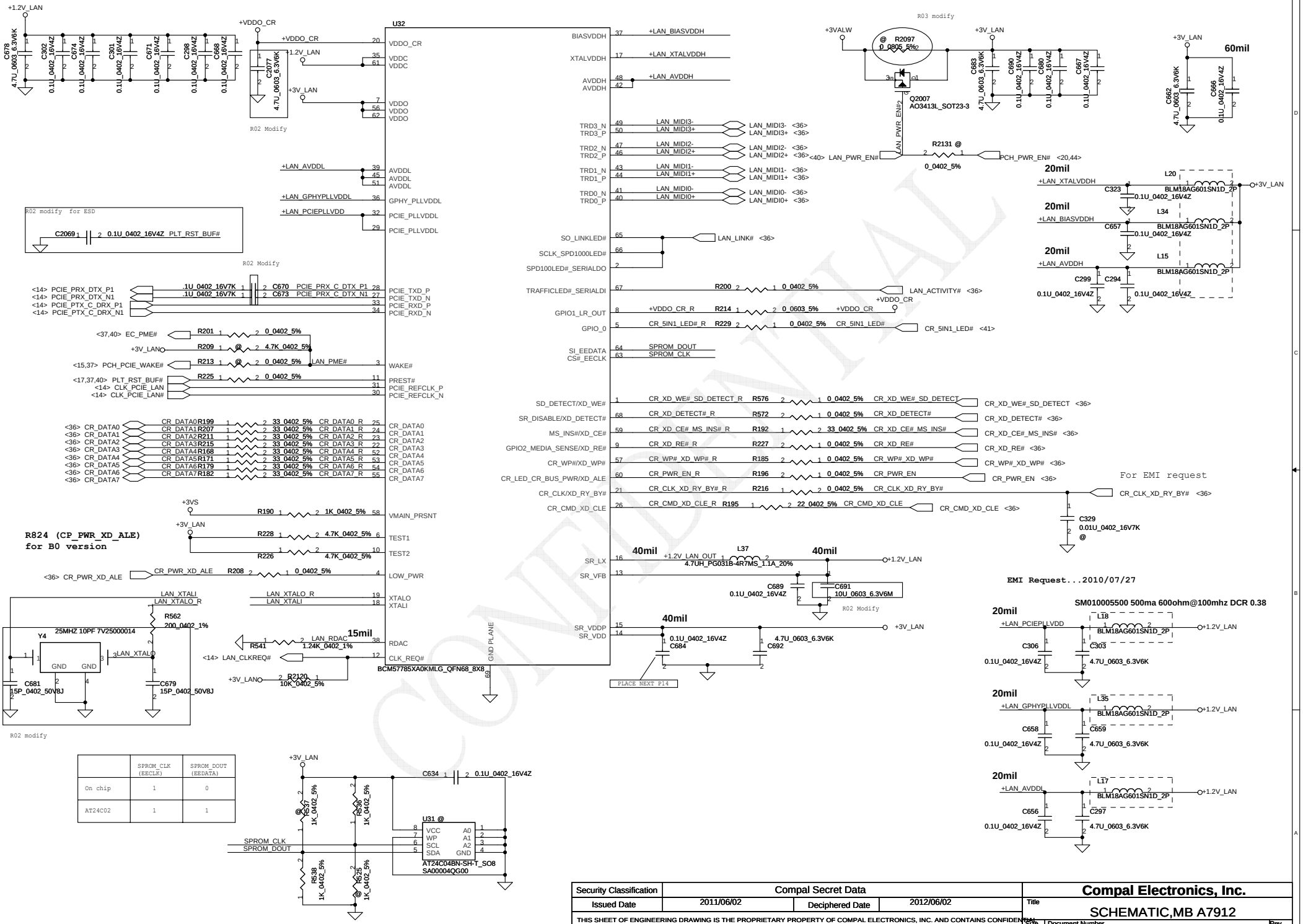

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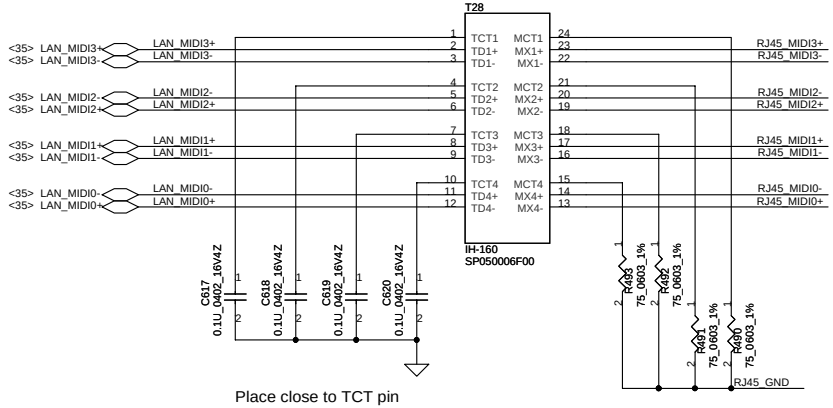
LAN Connector



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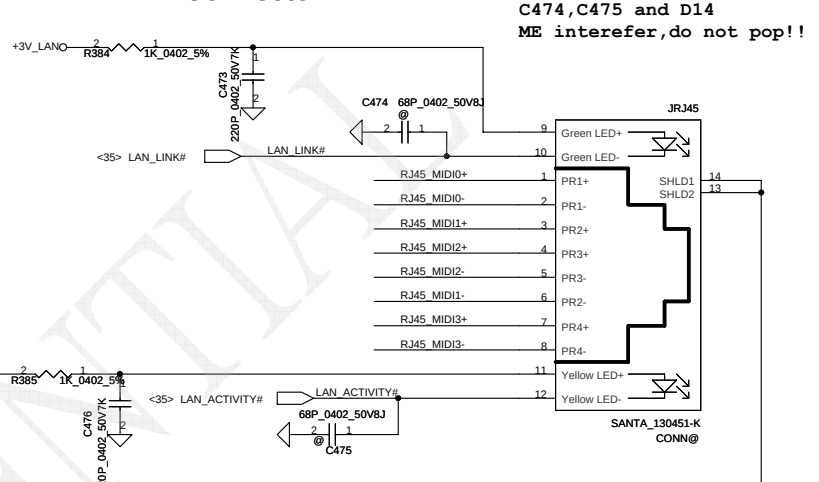
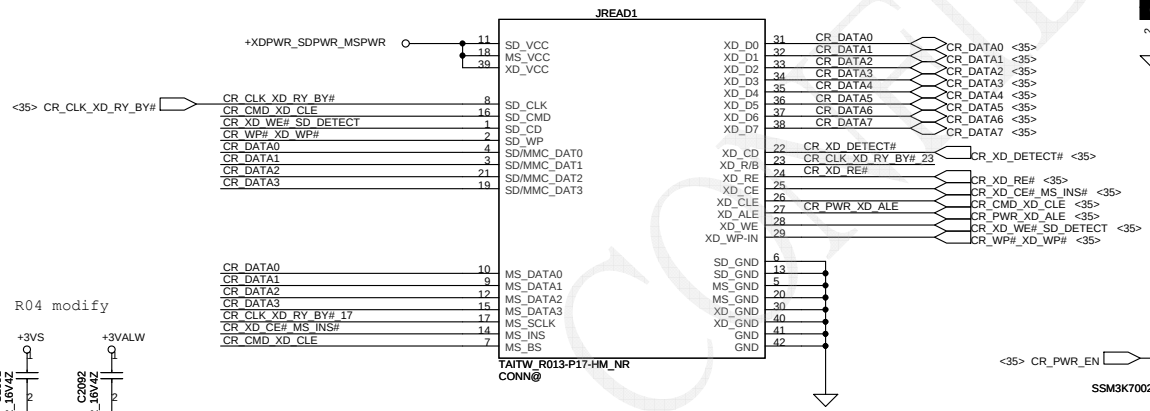
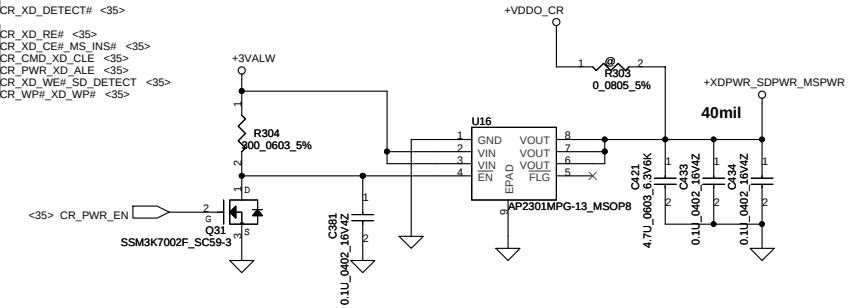
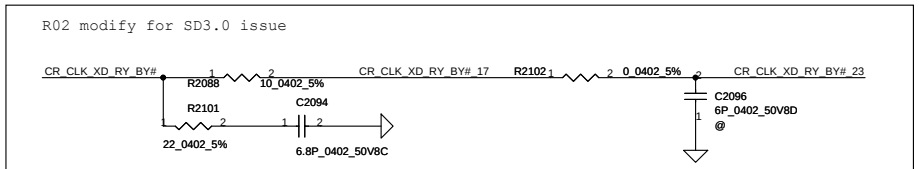
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



Card Reader Connector







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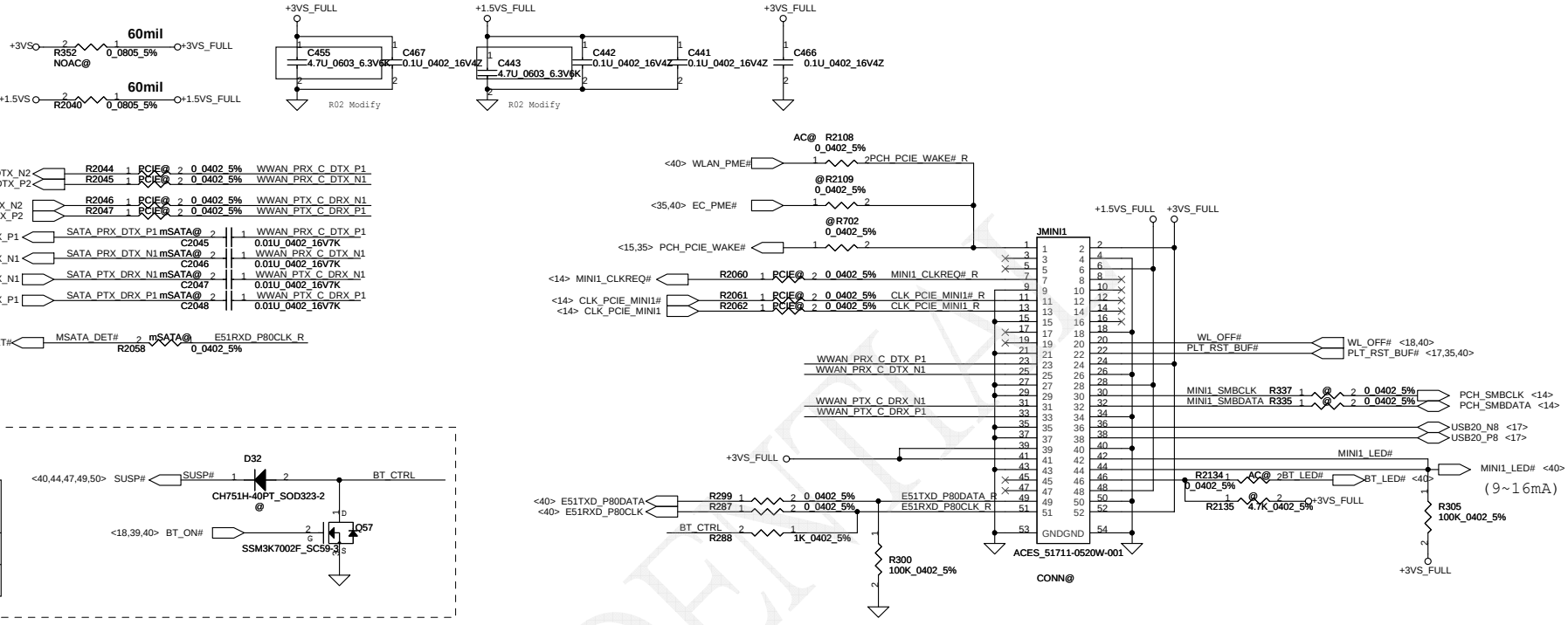
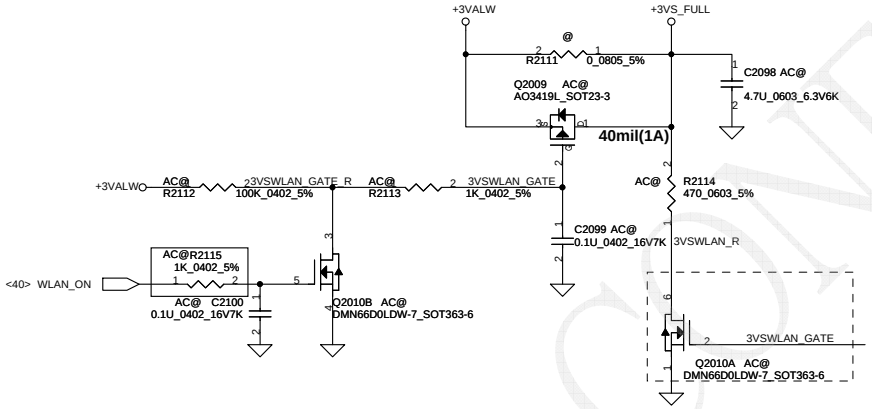
For Wireless LAN or MSATA



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



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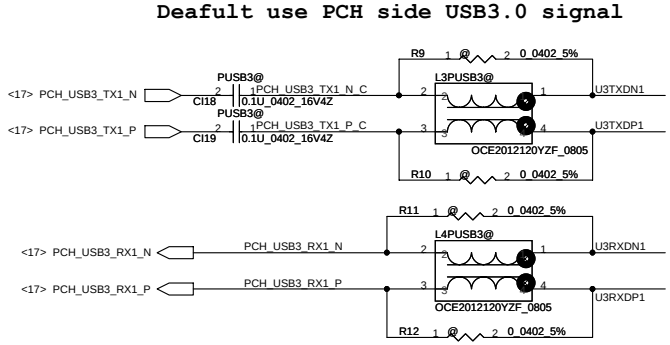
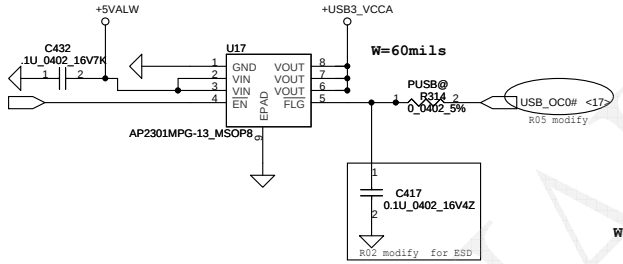
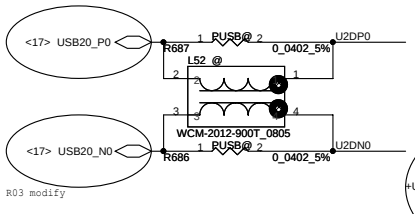
Deafult use PCH side USB3.0 signal

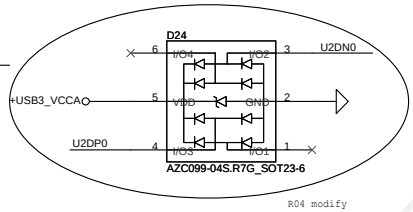
For USB2.0 ESD request



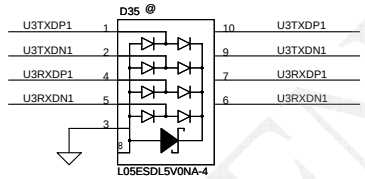


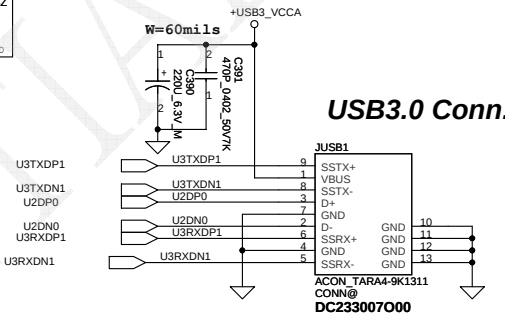


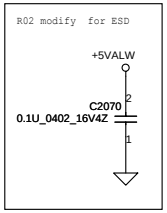
For USB2.0 ESD request

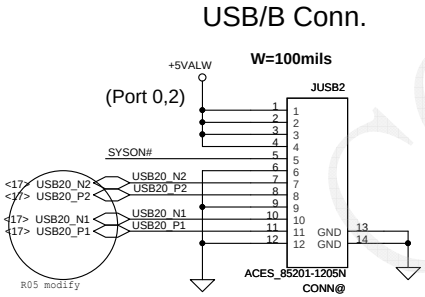


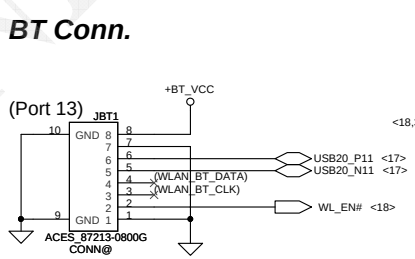
For ESD request

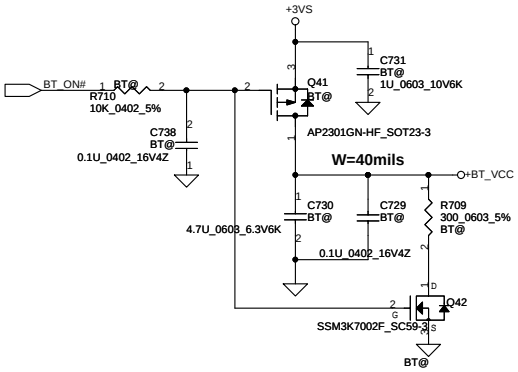












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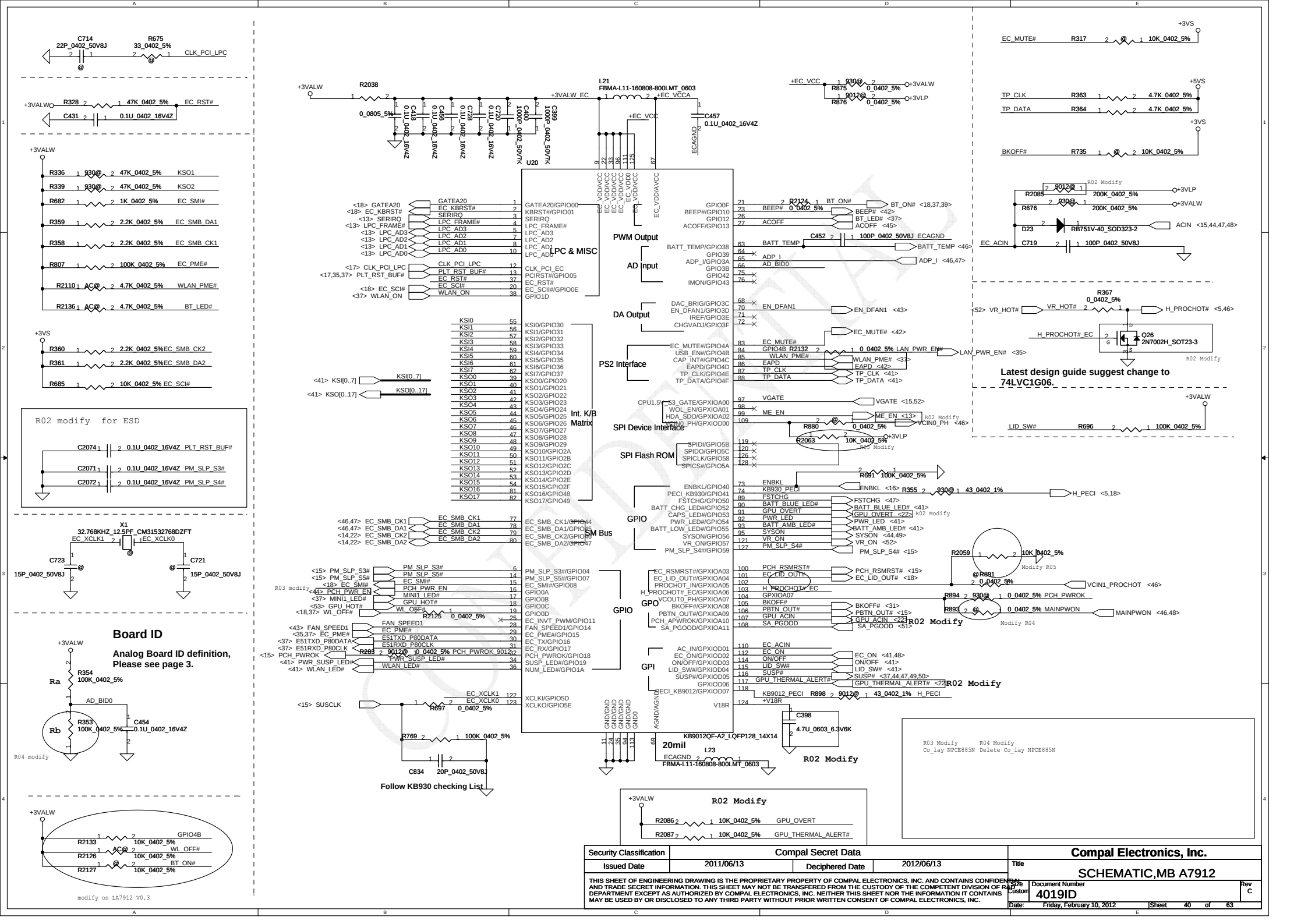

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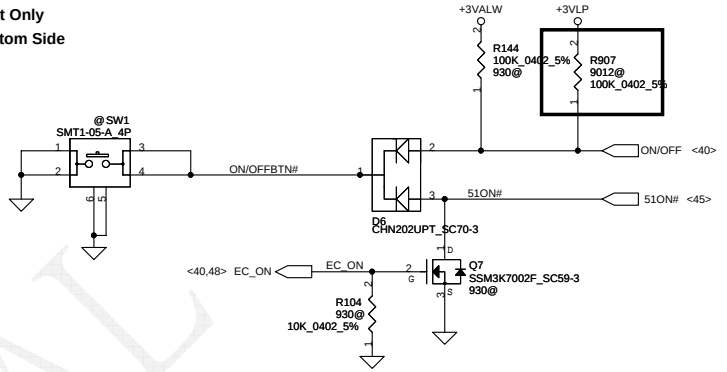
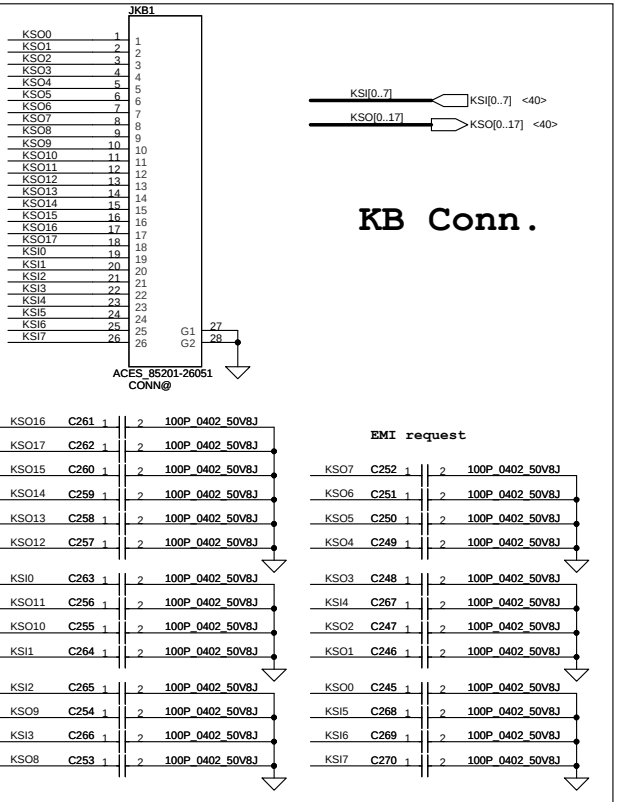
ON/OFF BTN

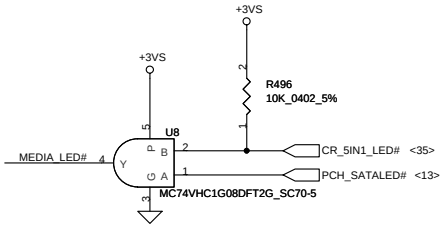
Test Only

Bottom Side

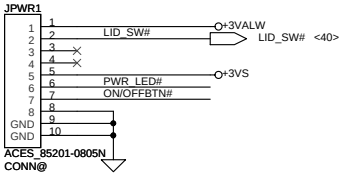


KB Conn.

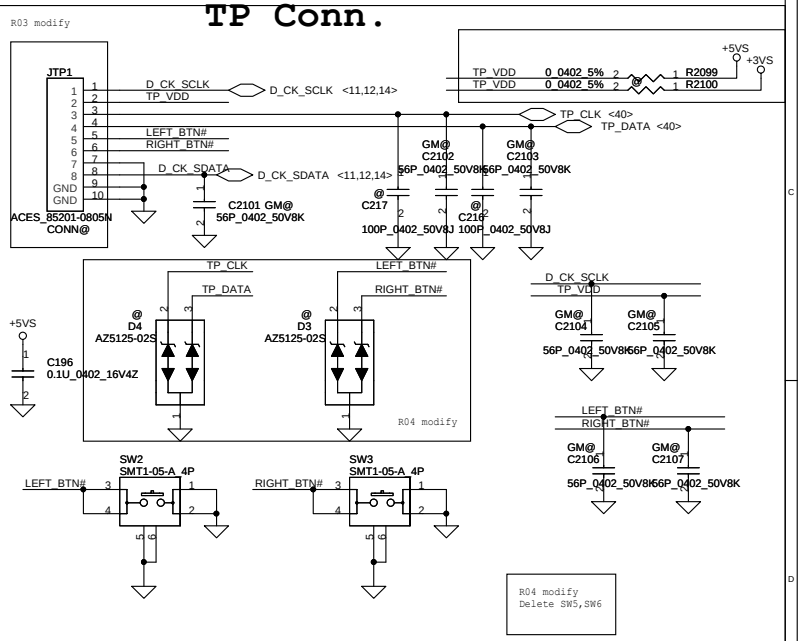




PWR/B



TP Conn.



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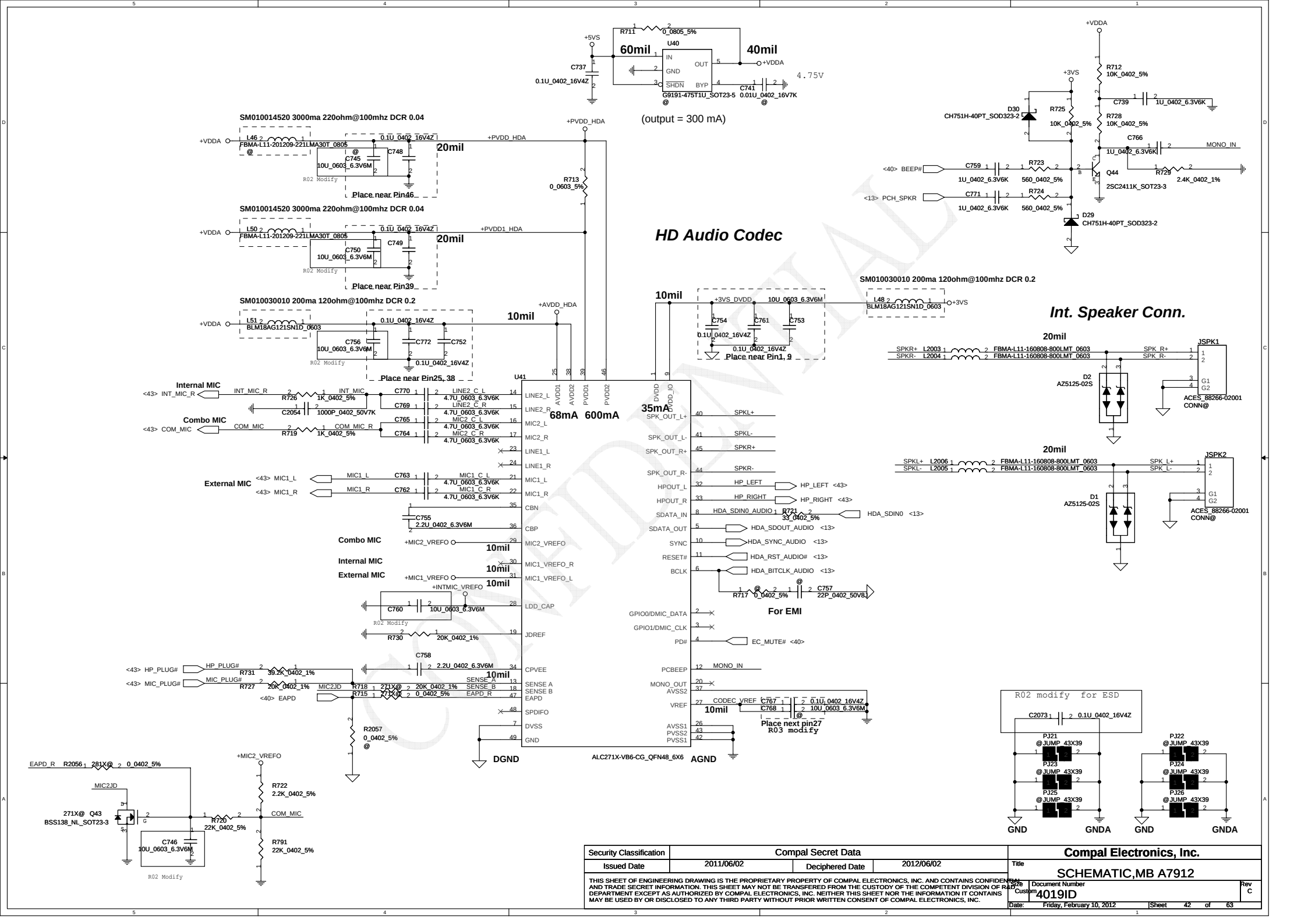

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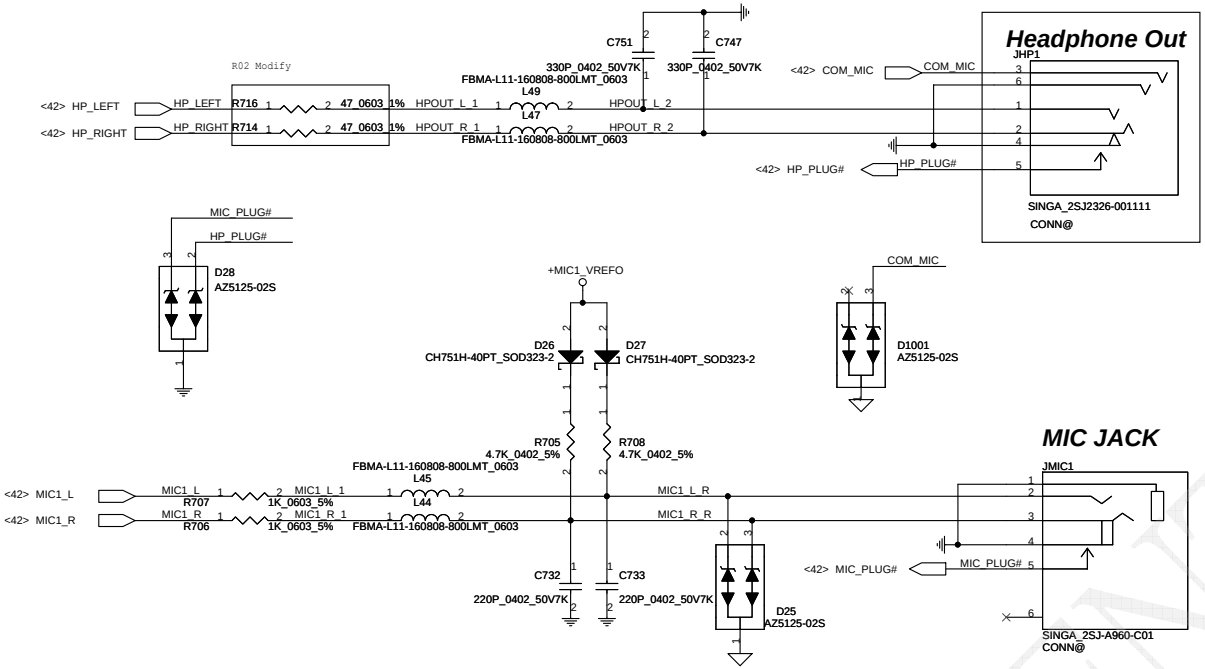

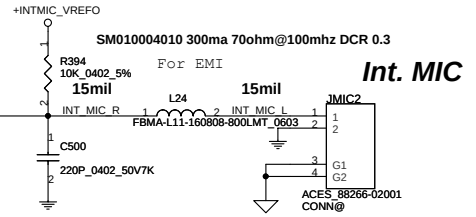

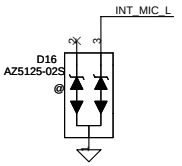

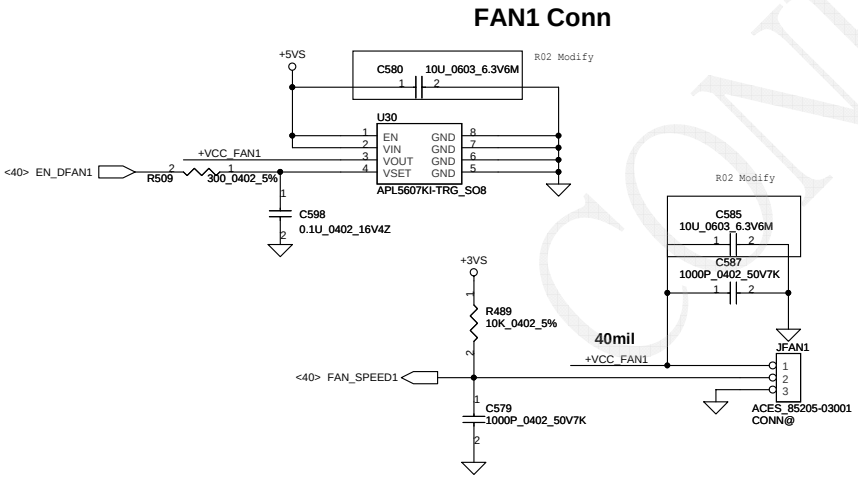

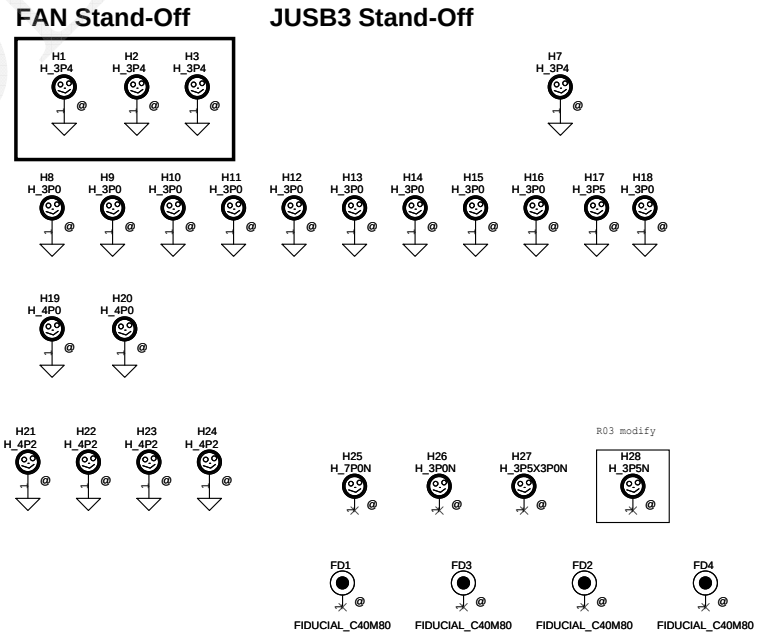

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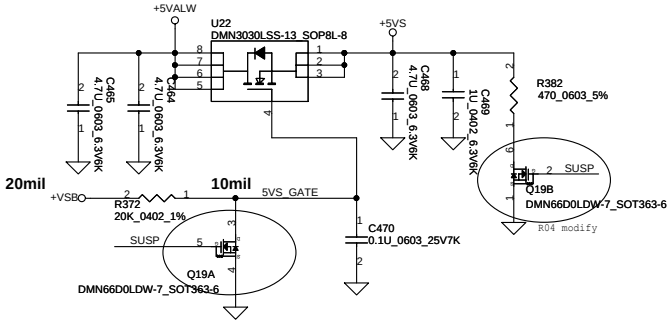
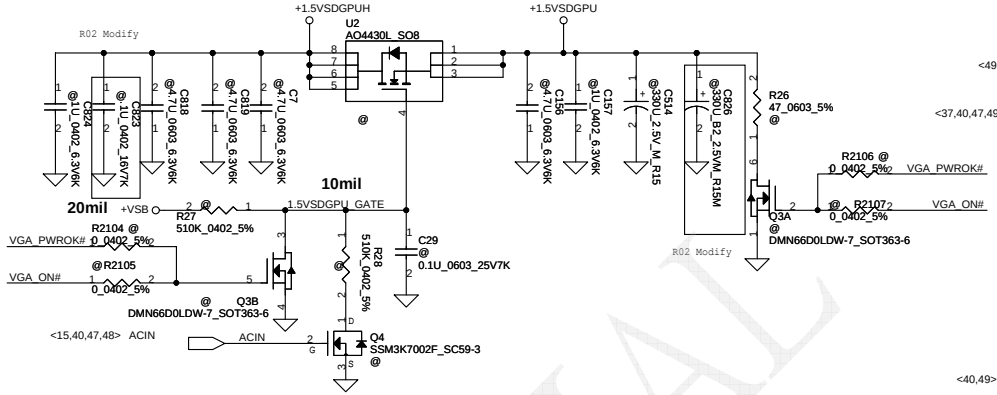
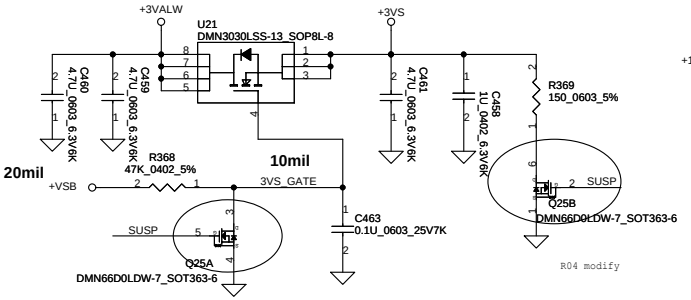
+5VALW TO +5VS

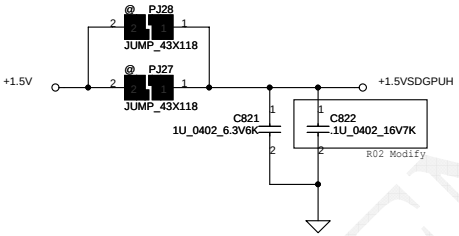


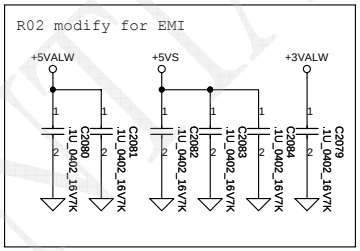
+1.5VSDGPUH to +1.5VSDGPU for GPU

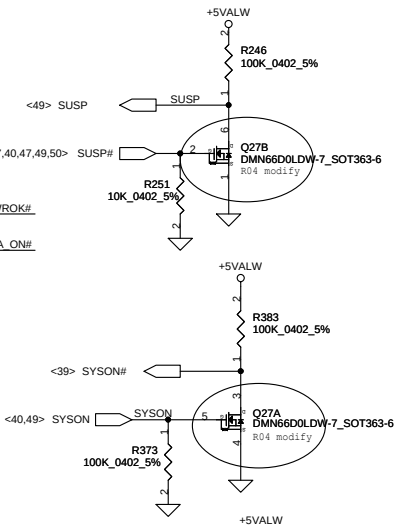


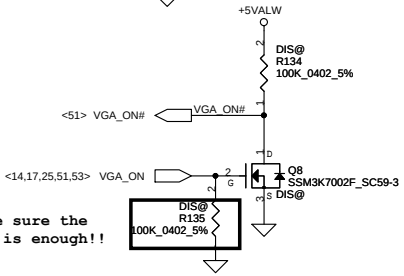
+3VALW TO +3VS





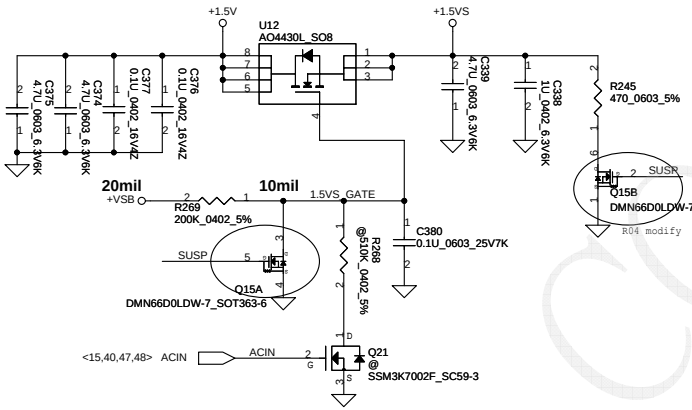




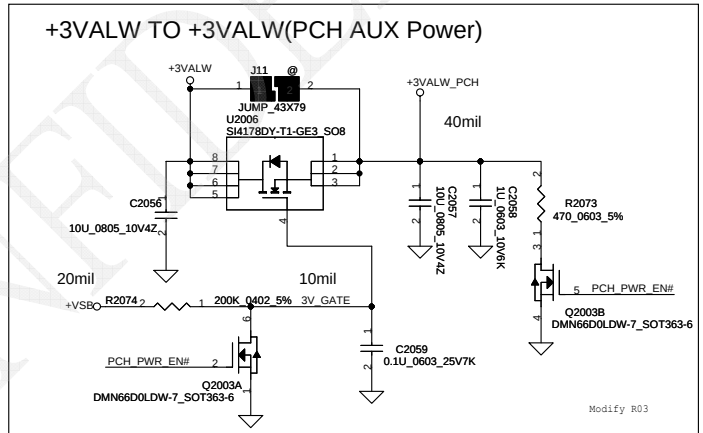


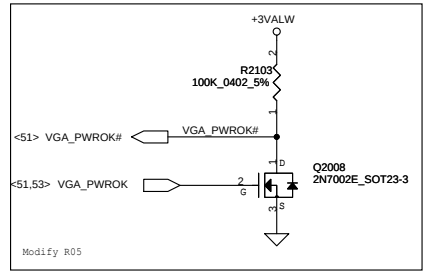
Use 100k to make sure the divided voltage is enough!!

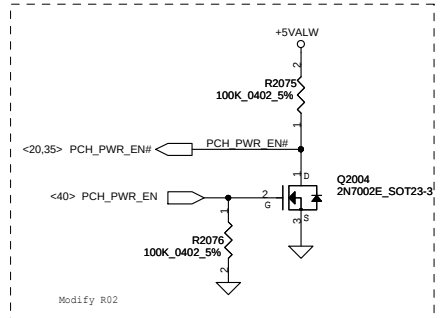
+1.5V to +1.5VS

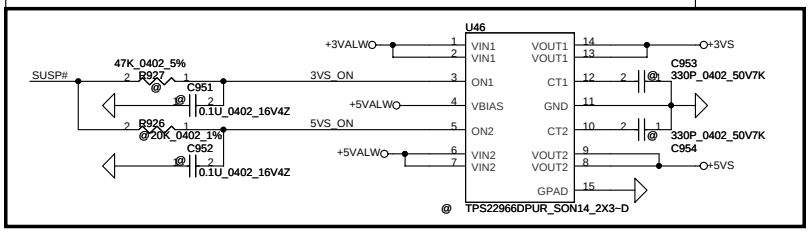


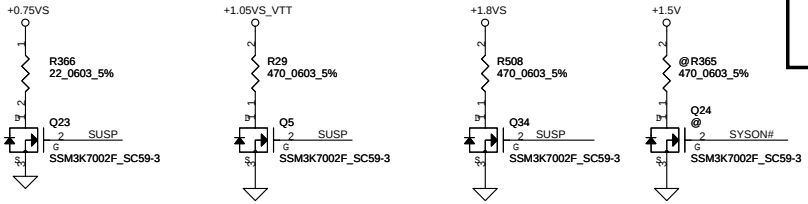
+3VALW TO +3VALW(PCH AUX Power)











Reserved

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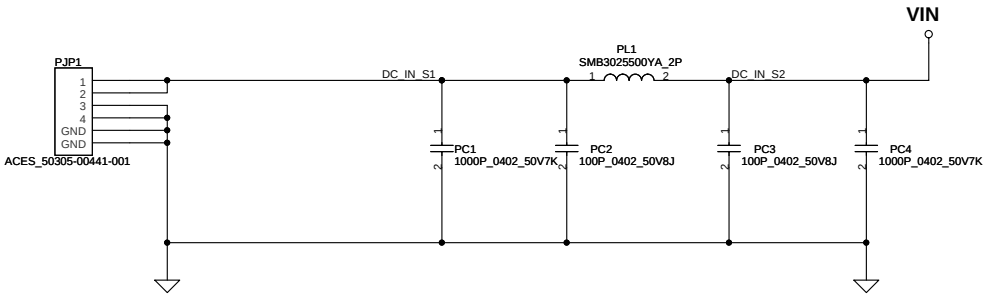

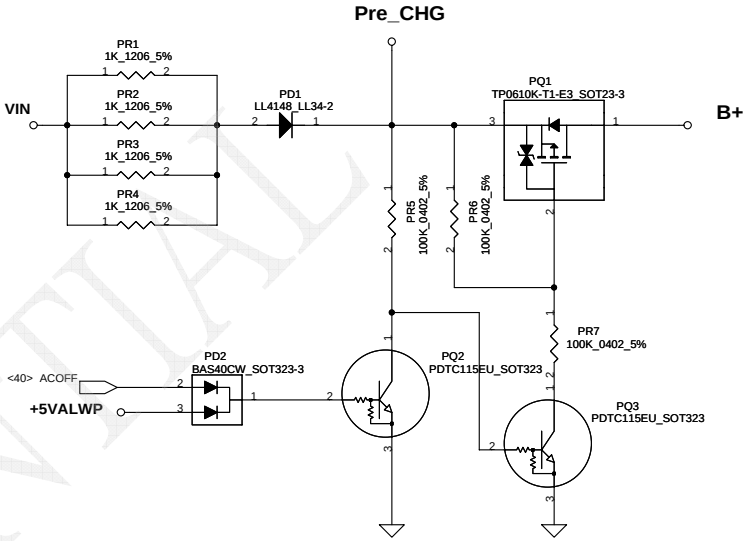

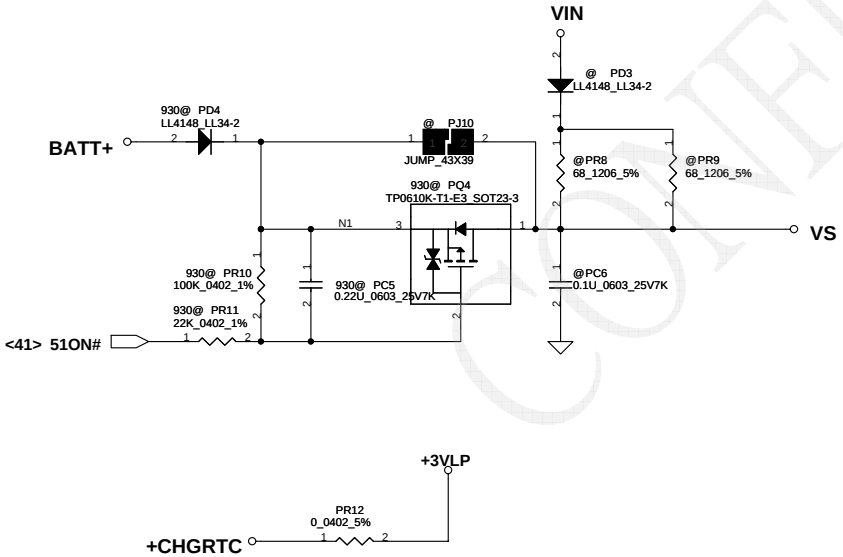

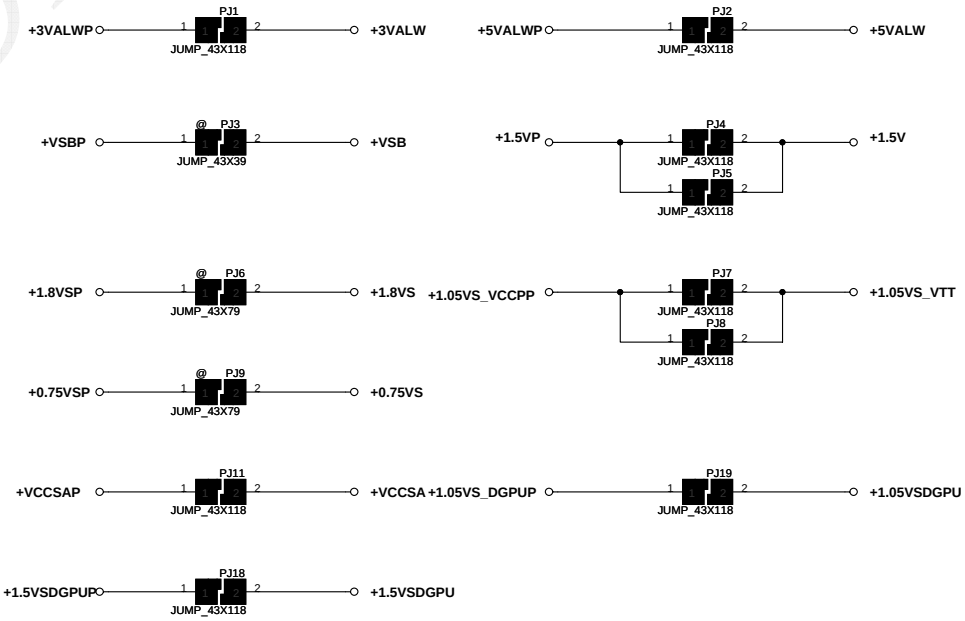

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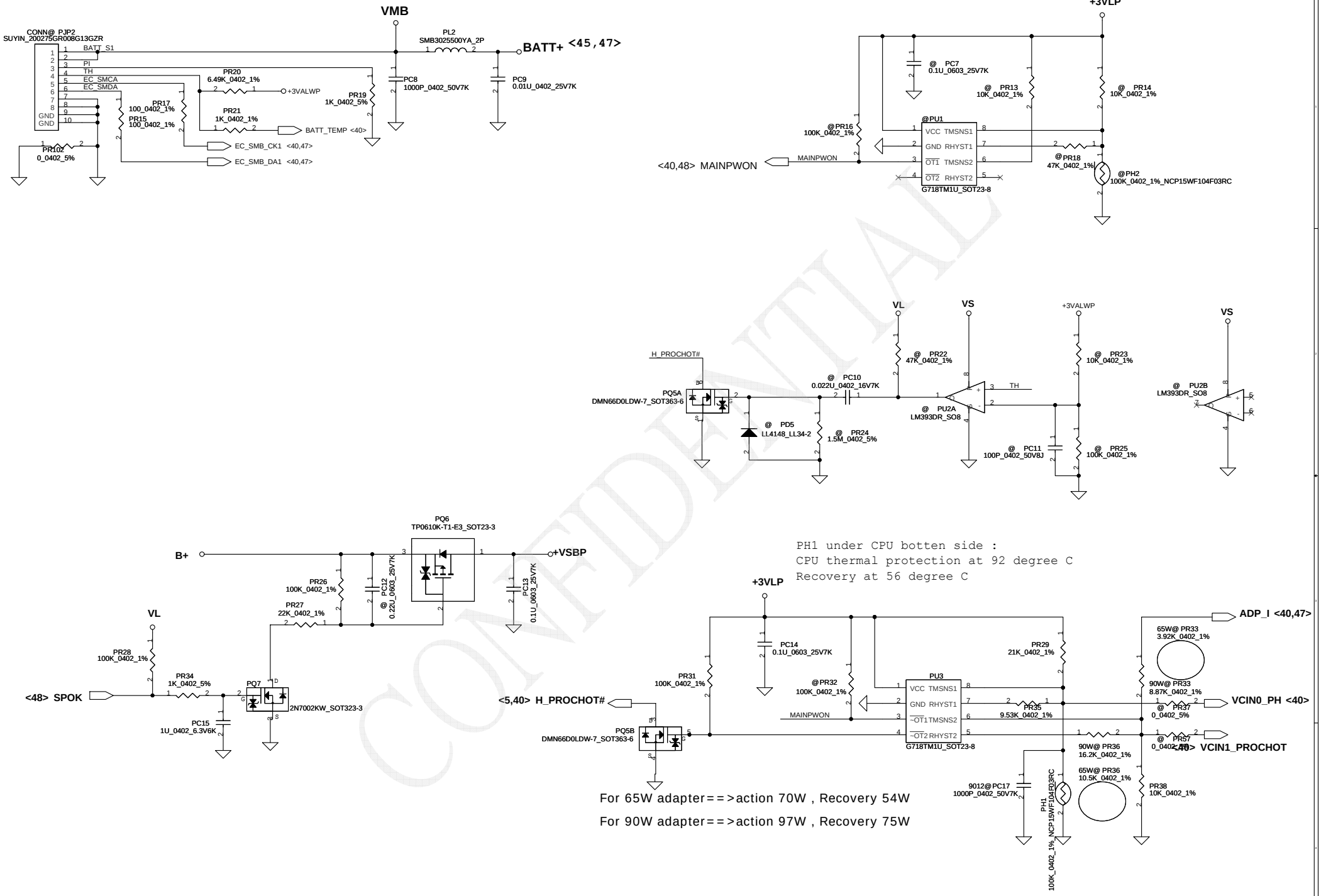

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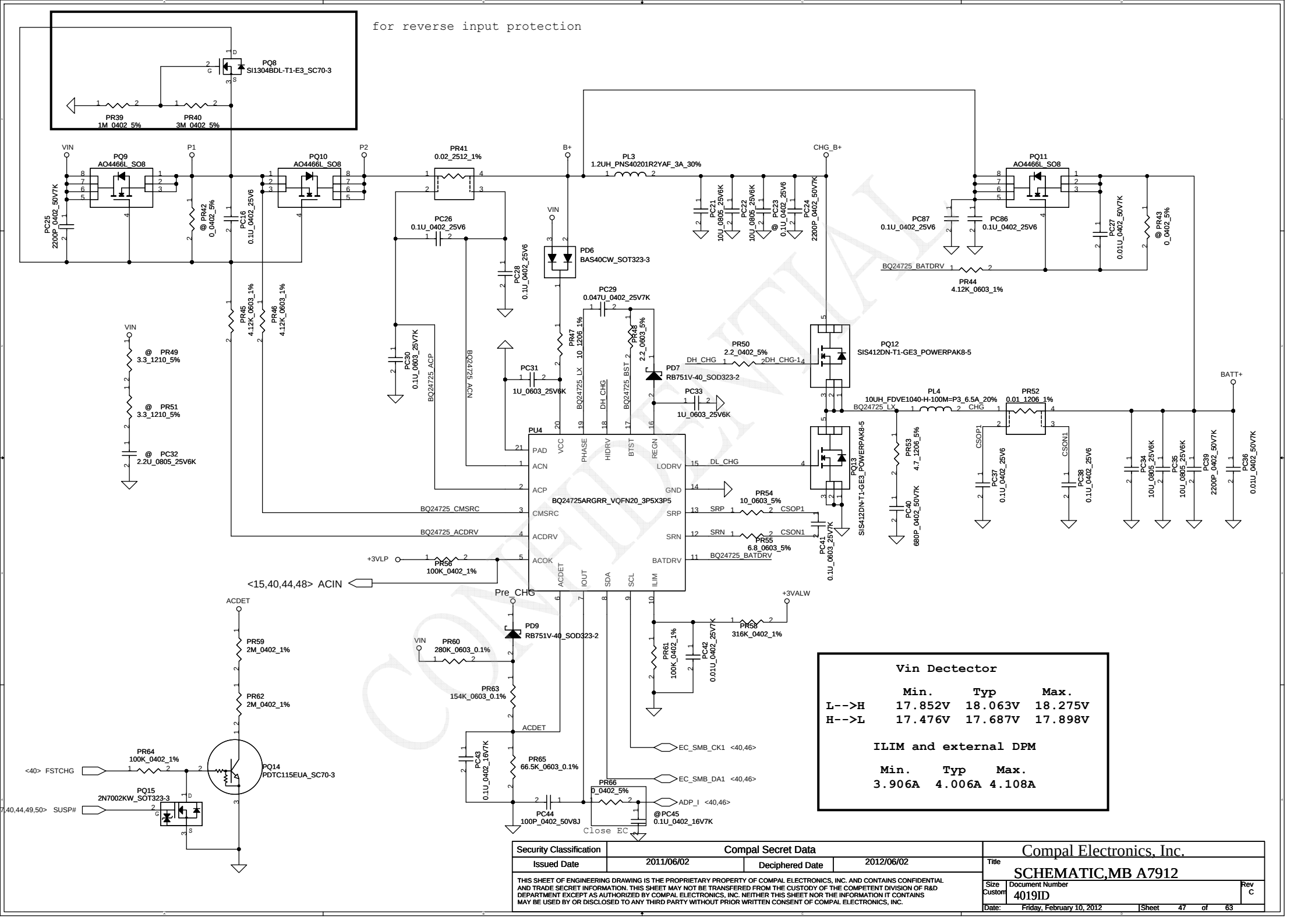

Vin Dectector

	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

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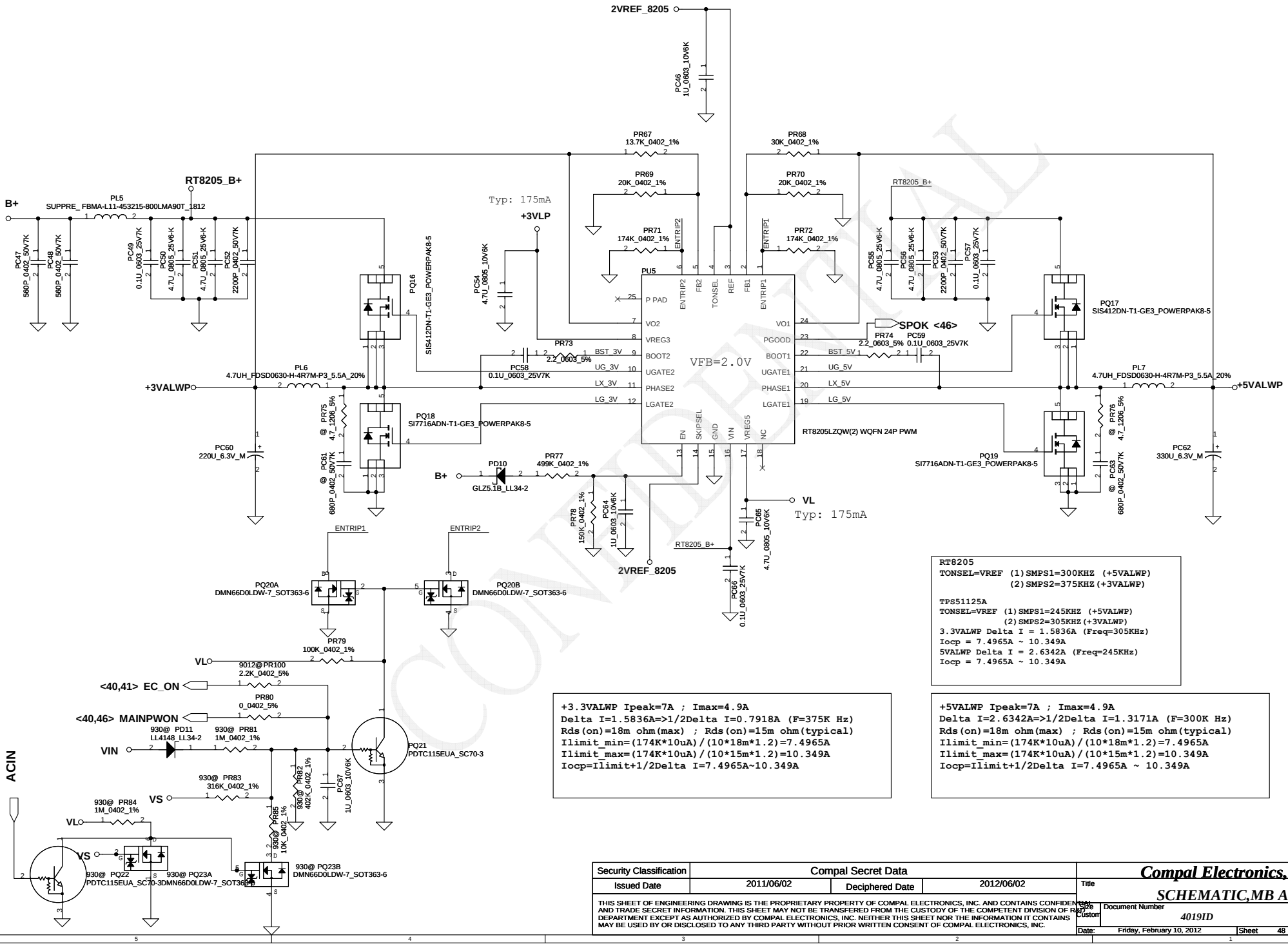
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.5836A (Freq=305KHz)
Iocp = 7.4965A ~ 10.349A
5VALWP Delta I = 2.6342A (Freq=245KHz)
Iocp = 7.4965A ~ 10.349A

+3.3VALWP Ipeak=7A ; Imax=4.9A
Delta I=1.5836A=>1/2Delta I=0.7918A (F=375K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(174K*10uA)/(10*18m*1.2)=7.4965A
Ilimit_max=(174K*10uA)/(10*15m*1.2)=10.349A
Iocp=Ilimit+1/2Delta I=7.4965A~10.349A

+5VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.6342A=>1/2Delta I=1.3171A (F=300K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(174K*10uA)/(10*18m*1.2)=7.4965A
Ilimit_max=(174K*10uA)/(10*15m*1.2)=10.349A
Iocp=Ilimit+1/2Delta I=7.4965A ~ 10.349A

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Compal Electronics, Inc.

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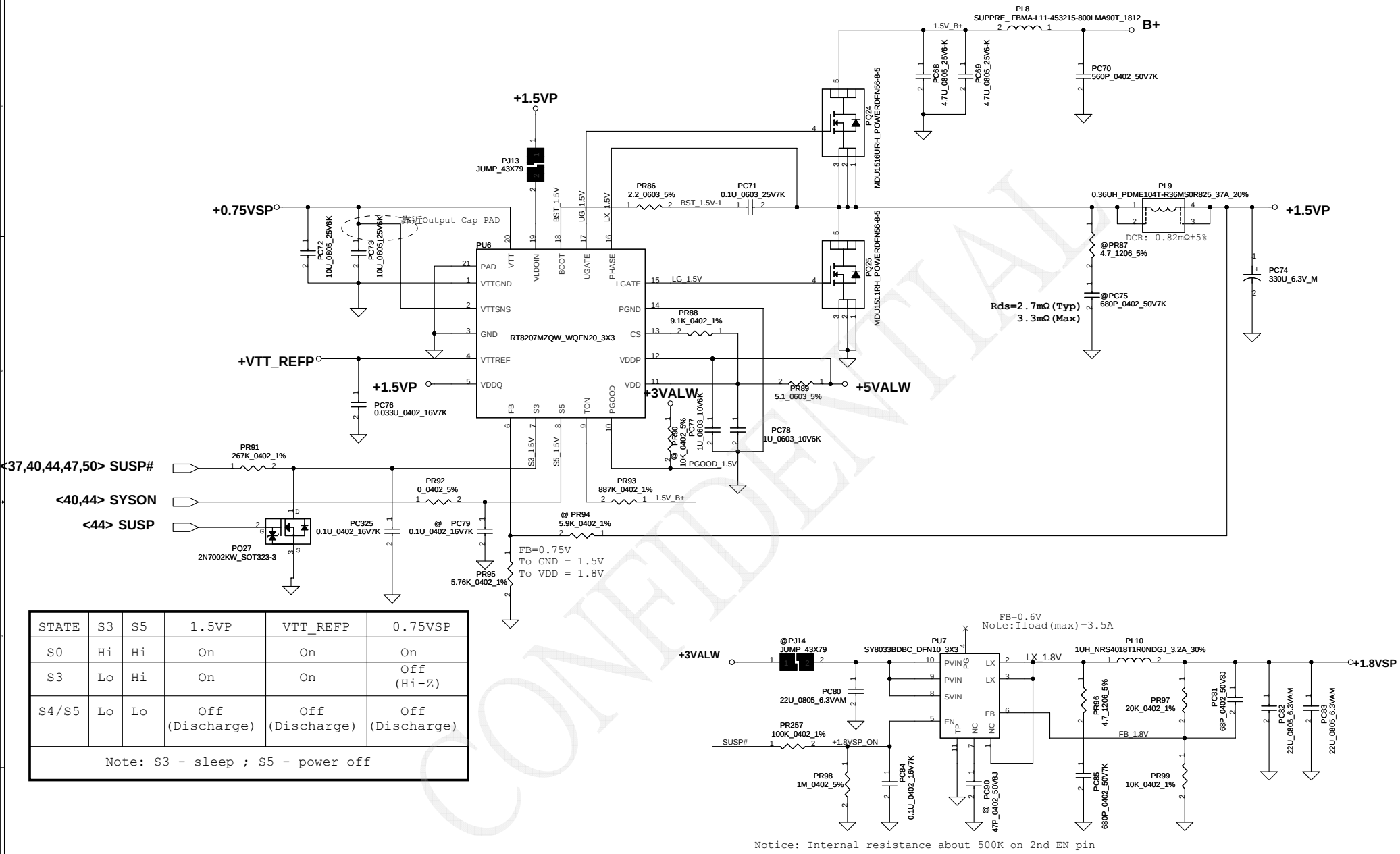

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

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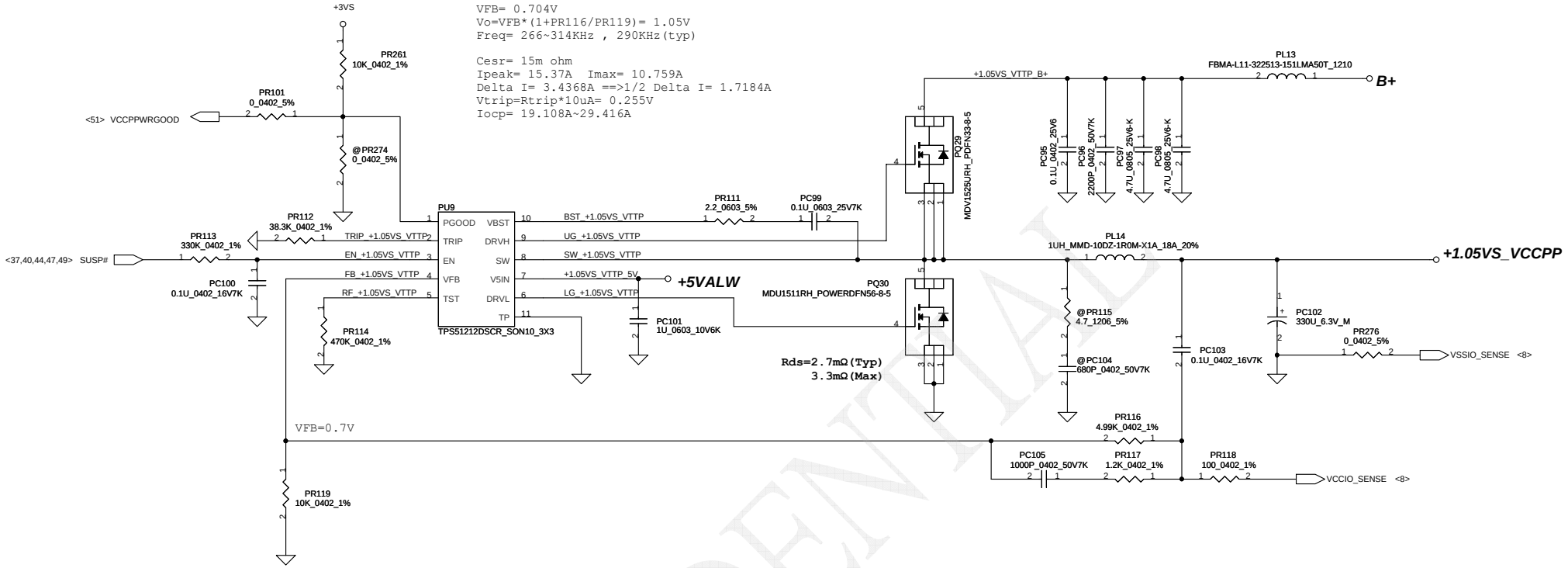

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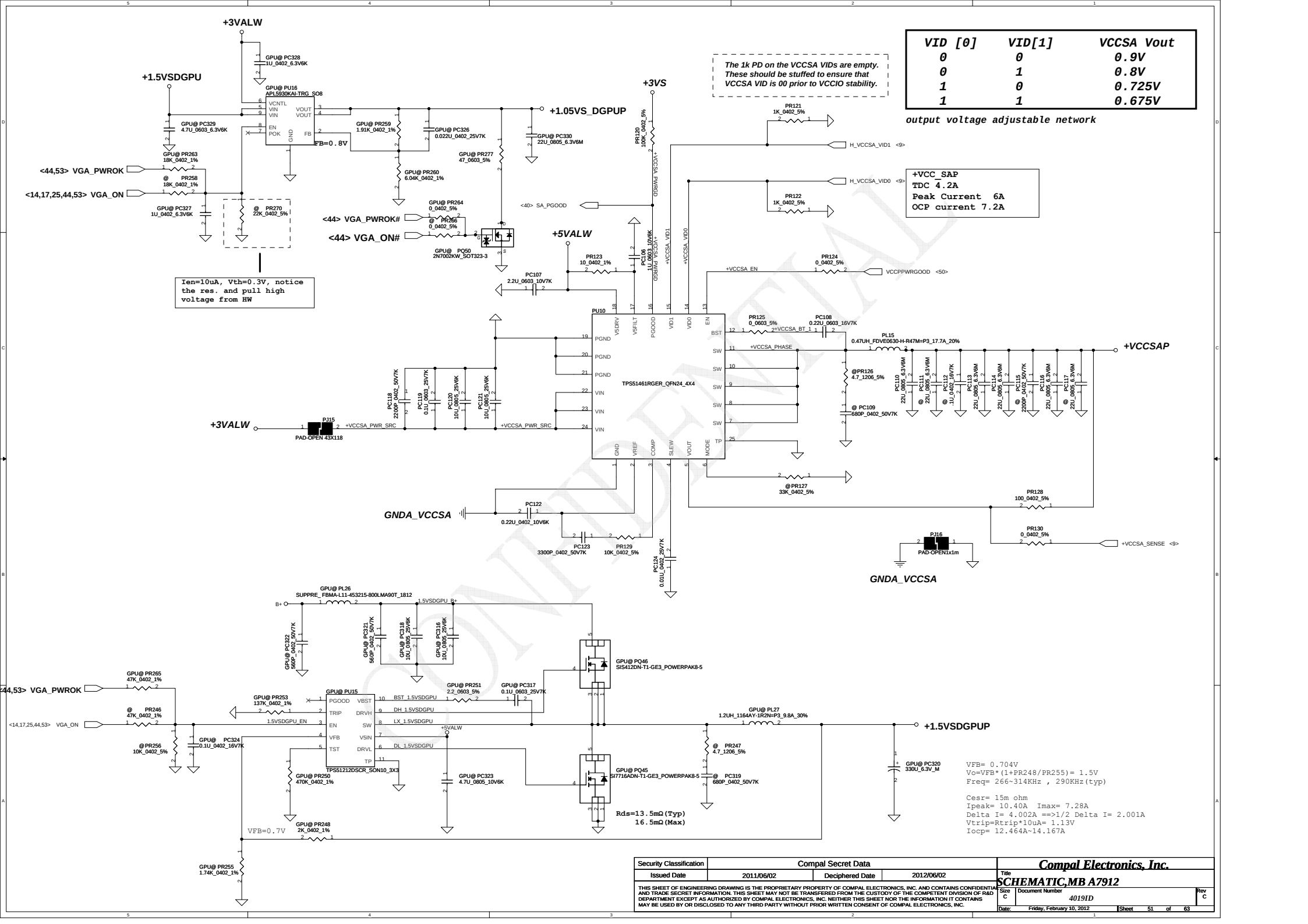

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

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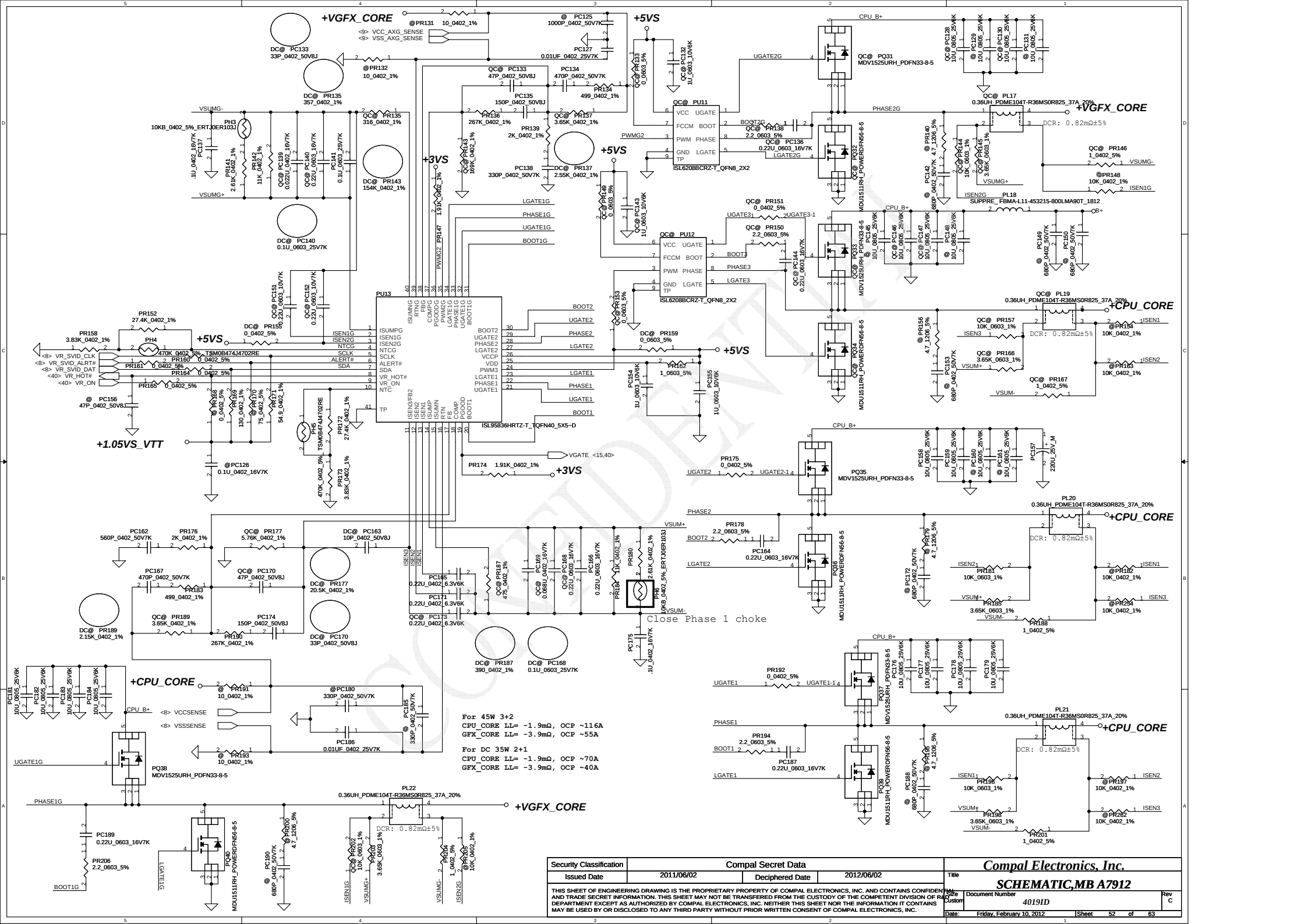

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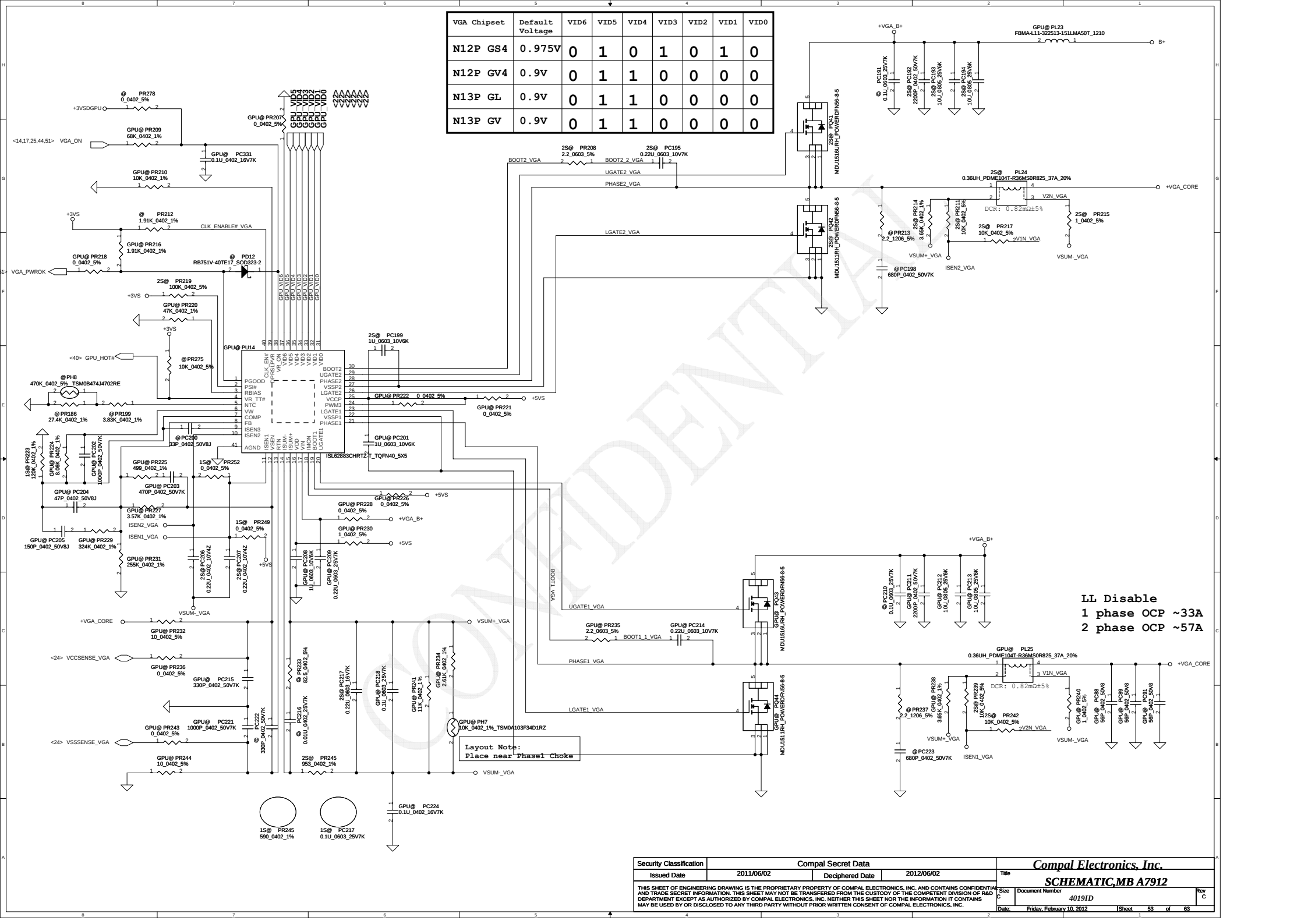
VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0



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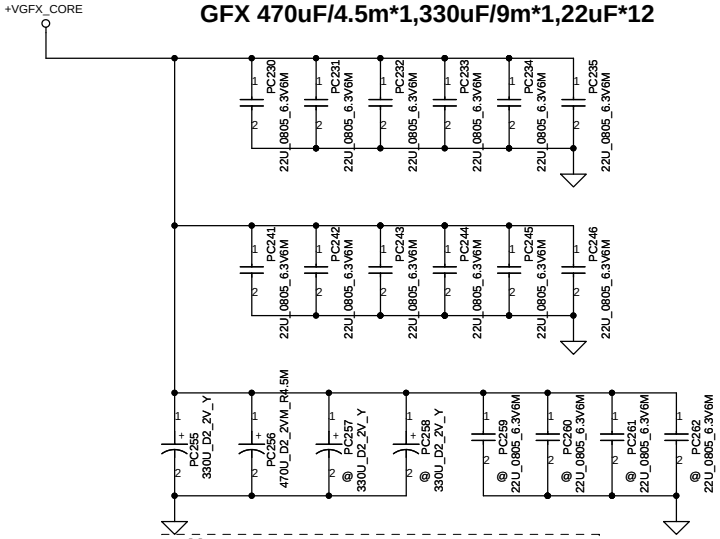
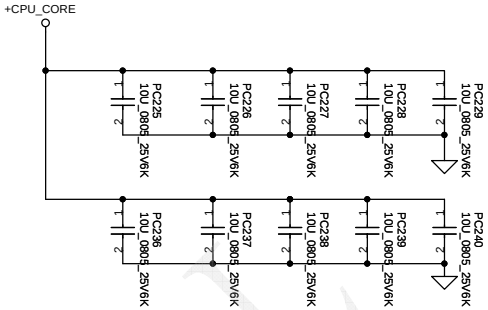
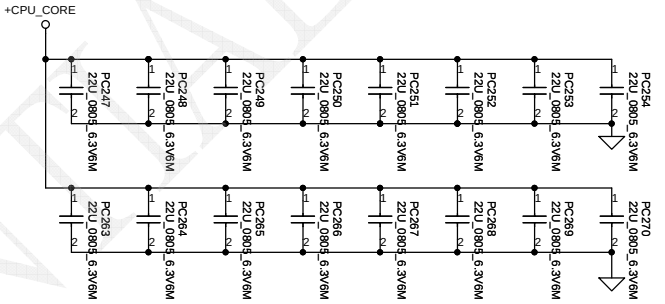
PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12

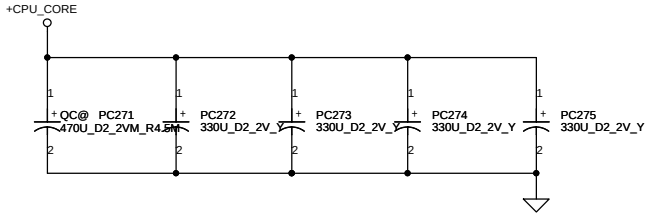


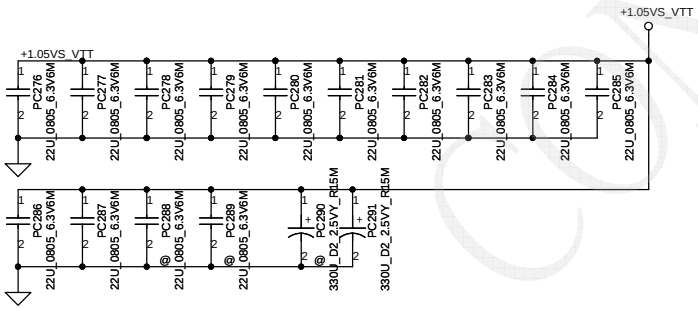
Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**









INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0

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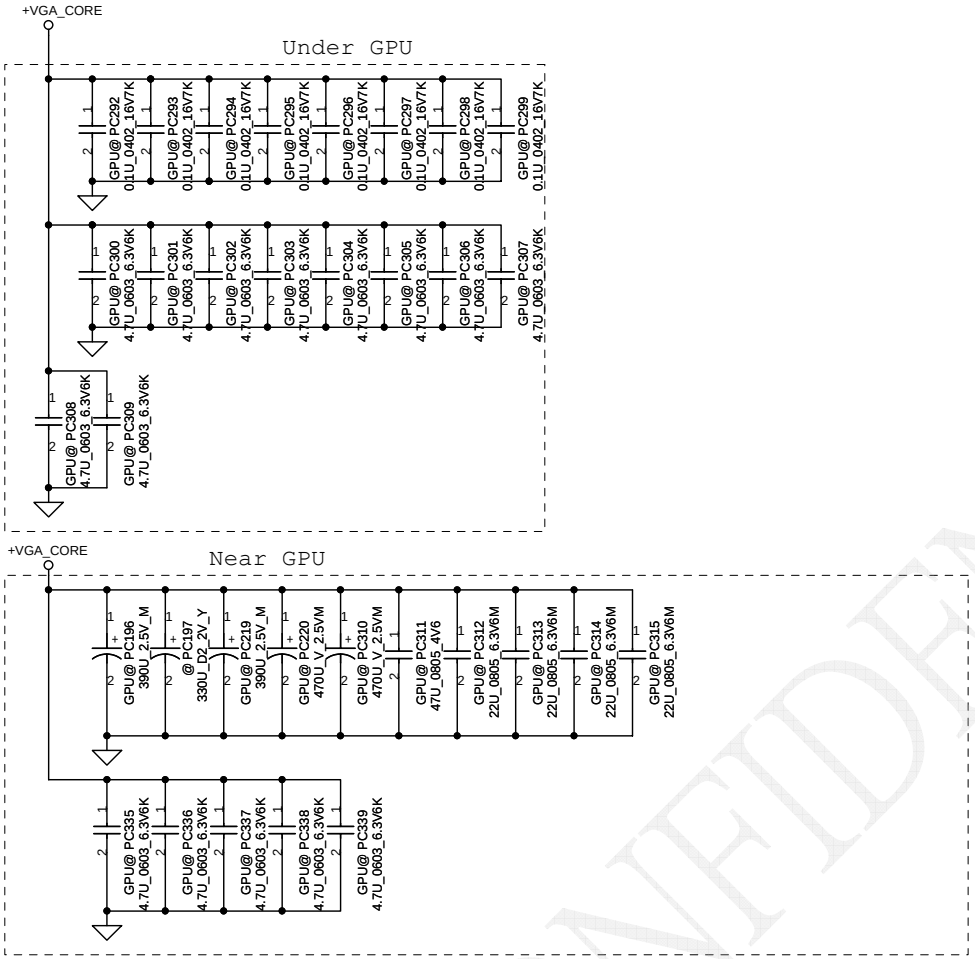

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2	2011 1208	DVT
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	PVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	PVT
8		Consider part rating		51	Change PR277 from 0402 to 0603	2011 1222	PVT
9		Tune transient character		52	Add PC139, PC169 Swap PC271 & PC275	2011 1222	PVT
10		PH1 OTP and ADP_I throttling by H/W control		46	Delete PR37, PR57	2011 1222	PVT
11		Follow Power design		55	Add PC313, PC314, PC315	2011 1222	PVT
12	VGA sequence meet nVidia SPEC			51	Swap PR258 & PR263, PR266 & PR264, PR246 & PR265	2011 1223	PVT
13	Cut-in EMI solution			47	Add PR53, PC40	2012 0104	PVT2
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add fl1009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	~~Add USB chargaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)~~		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	~~Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)~~		0.2
7	P.44		9/7	HW	~~Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)~~		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2082)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU_ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	P.44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P.36		9/20	HW	For SD3.0 issue (Add R2088.R2089)		0.2
27	P.20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P.44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P.40		10/17	HW	Board ID error. Add R353.		0.3
30	P.40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P.17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P.18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P.13.40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43	P.41		11/16	ME		Delete SW5,SW6, Pop SW2,SW3	0.4
44	P.05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P.35		11/17	HW	LAN SPROM on Chip	De-pop U31,R537 Pop R538	0.4
46	P.36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P.13		11/17	HW	RTC issue	Change C682,C686 to 15P	0.4
48	P.31,32,41		11/17	ESD		De-pop D3,D4,D17,D18,D15 Pop D24,D36	0.4
49	P.40		11/17	HW		De-pop R891,R893	0.4
50	P.24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P.13		11/21	HW		Chip Select Change R651,R2049 to 0ohm	0.4
52	P.13,40		11/21	HW		Delete NPCE885N (R2091.R2092.R2094.R2095.R2096,R698, R699,R692,C2085)	0.4
53	P.45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P.35,36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525,R536,R537,R538 to 1k	0.4
56	P.13		11/23	HW		Delete R2093,R2049,R651(0ohm)	0.4
57	P.13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P.35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P.36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
58	P.24.25		12/02			Change R1057 from 35kohm to 45kohm Change R1077 from 40.2ohm to 42.2ohm Change R1080 from 60.4ohm to 51.1ohm	0.4
59	P.22		12/02			for N13P_GS, the boot voltage is 0.9V pop R1022,R1021,R1036,R1035,R1034,R1033 for N13P_GL, the boot voltage is 0.95V pop R1022,R1037,R1020,R1019,R1034,R1033 for N13M_GS, the boot voltage is 0.925V pop R1022,R1037,R1020,R1019,R1018,R1033	0.4
60	P.44		12/02			Change R369 from 470ohm to 150ohm Change R26 from 470ohm to 47ohm Pop Q3	0.4
61	P.13		12/02			BIOS ROM(4M) Change U36 to SA00003K800	0.4
62	P.35		12/06			EMI suggestion for Card Reader Change R195 from 33ohm to 22ohm Change R216 from 22ohm to 0ohm Change C2094 from 6pF to 6.8pF Change R2101 from 0ohm to 22ohm Change R2088 from 47ohm to 75ohm Change R2102 from 47ohm to 0ohm De-pop C2096	0.4
63	P.36		12/07			EMI request for 家電下鄉 Add C2097	0.5
64	P.39		12/07			For PCH HM70 Change USB port0 to co-lay USB3.0 Change USB port2 to USB2.0 Change USB port 11 to BT	0.5
65	P.44		12/07			Change 1.5VSDGPU EN from VGA_ON# to VGA_PWROK# Add R2103,Q2008	0.5
66	P.18		12/09			For eDP Change Q2007 from SB501380020 to SB501110010	0.5

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67	P.31		12/16	EE		change Q2007 to 2N7002 for eDP_HPD circuit	LA-7912 0.2
68	P.40		12/16	EE		add WLAN_PME# on pin85. add wlan_on signal on EC pin38 add AC circuit	LA-7912 0.2
69	P.35		12/16	EE		reserve Q2007 for open +3V_LAN by PCH_PWREN#	LA-7912 0.2
70	P.40		12/16	EE		add R2063 for pull high VCIN0_PH to +3VL 10k add R2059 for pull low VCIN1 10k	LA-7912 0.2
71	P.41		12/20	EE		resever R2116 ~ R2119 for change LED power to 3V resever C2101~C2107 56pF on T/P for EMI	LA-7912 0.2
72	P.36, 14		12/22	EE		change R384 & R385 power to +3V_LAN unpop R630 & reserve R2120 to pull high +3V_LAN	LA-7912 0.2
73	P.42, 35		12/22	EE		change Q43 from 2n7002 to BSS138 unpop R209	LA-7912 0.2
74	P.40		12/23	PWR		change R353 to 56k for board ID 0.2 power request pop R2063, R2059 un-pop R880, R891, R893	LA-7912 0.2
75	P.39		12/23	EMI		change USB3 signal pass by chock (SM070001600)	LA-7912 0.2
76	P.41		12/23	ME		Change LED(Blue) SC591NB5A30 to SC591TBKA10 Change LED(AMBEL) SC500007700 to SC500005930 change (R2116=130ohm),(R377,2118,378=390ohm) (R2117,2119 = 51 ohm)	LA-7912 0.2
78	P.36		12/23	EMI		R2088 change to 10ohm	LA-7912 0.2
79	P.25		12/23	EMI		L1002 use SM010028800 (for N13P_GL) use 0ohm on N13P_GS,N13M_GS	LA-7912 0.2
80	P.44		12/24	EE		POP R2104, R2106 unpop R2105, R2107 for VGA sequence	LA-7912 0.2
81	P.41,24		12/24	EMI,EE		De-pop C217,C216 EMI request. add R1019, R1020, R1037 for GM@ (VGA_CORE)	LA-7912 0.2
82	P.40,27		12/27	EE		change R2059&R2063 to 10k ohm for EC request C2086~C2089 change bom sturte to DIS@	LA-7912 0.2
83	P.40		12/27	EE		add R2125, R2123 for option WL_OFF# to EC or PCH add R2122, R2124 for option BT_ON# to EC or PCH reserve R2126 to pull high 3VALW reserve R2127 to pull high 3VALW	LA-7912 0.3

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
83	P.41		01/02	EE		reserve R2121 for WLAN_LED connect +3VALW change C2101~2107 bomstucture to GM@	LA-7912 0.3
84	P.13		01/09	EE		add GPIO23 for define USB config. (R2128 & R2092)	LA-7912 0.3
85	P.45~56		01/09	PWR		update power circuit	LA-7912 0.3
86	P.37		01/09	EE		change R2110 to pull high +3VS_FULL	LA-7912 0.3
87	P.31		01/10	EE		add R2130 reserve for lvds short issue	LA-7912 0.3
88	P.40		01/10	EE		change board ID to 0.3 (R353 100k)	LA-7912 0.3
89	P.37		01/11	EE		change R2110 to pull high +3VALW	LA-7912 0.3
90	P.37		01/11	EE		pop +3VS_FULL 開電線路	LA-7912 0.3
91	P.13		01/11	EE		add new bom structer usb2@ for usb flag	LA-7912 0.3
92	P.44		01/11	EE		UNPOP +1.5VSDGPUH to +1.5VSDGPU circuit	LA-7912 0.3
93	P.35, 40		01/12	EE		add R2131,R2132 for option turn off 3VLAN power by PCH_PWR_EN# or LAN_PWR_EN# (from EC)	LA-7912 0.3
94	P.37, 40		01/18	EE		add R2134~R2136 reserve for AOIC for ACER request	LA-7912 0.3
95	P.17		01/18	EE		reserve R2137 pull low USB_P8 for PCH leakage	LA-7912 0.3
96	P.32		02/02	EE		change R428 & R426 to 0 ohm for CRT issue	LA-7912 0.3

Security Classification	Compal Secret Data		
Issued Date	2011/08/31	Deciphered Date	2012/08/31

Compal Electronics, Inc.

Title: SCHEMATIC,MB A7912

Size: Custom | Document Number: 4019ID | Rev: C

Date: Friday, February 10, 2012 | Sheet 63 of 63