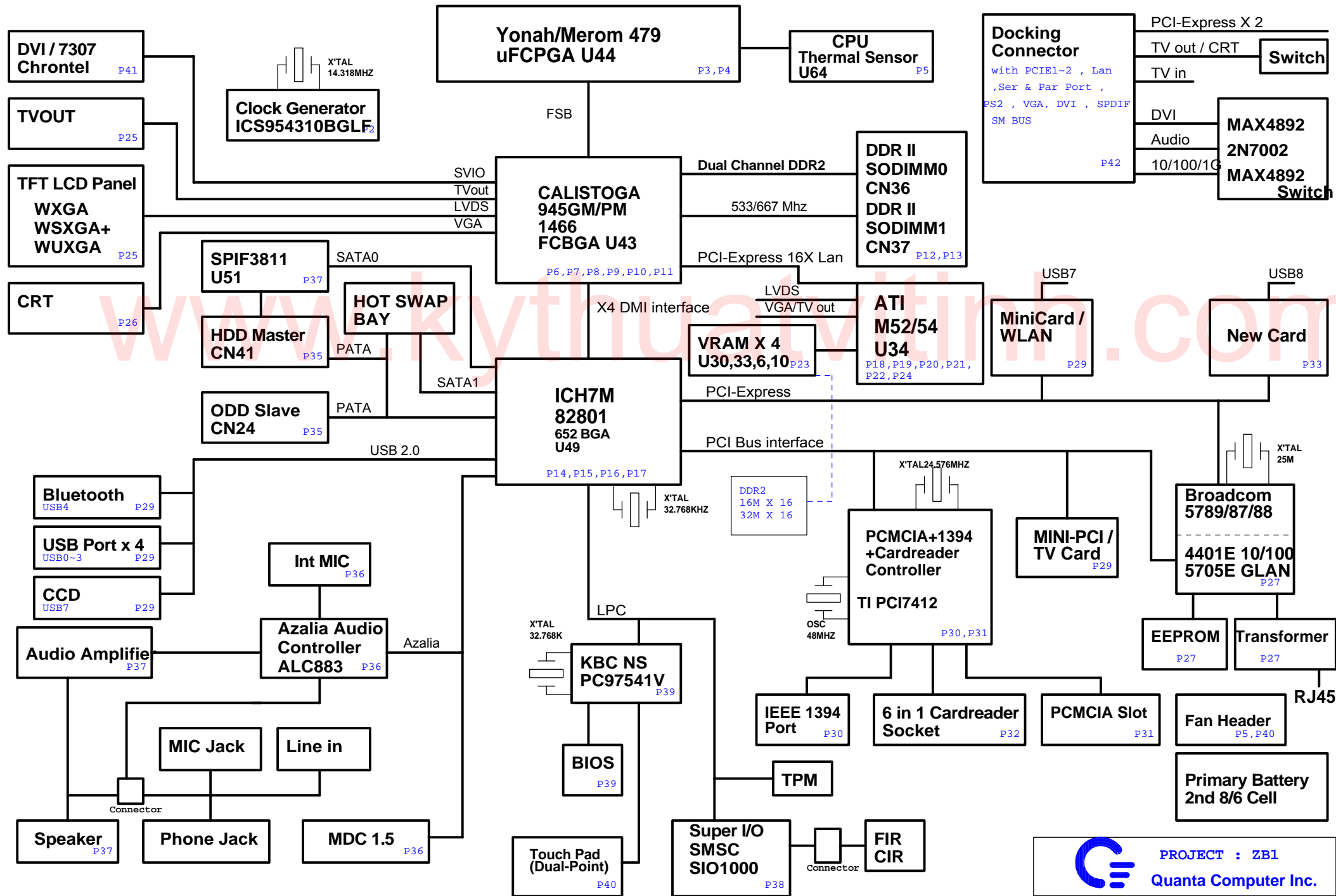
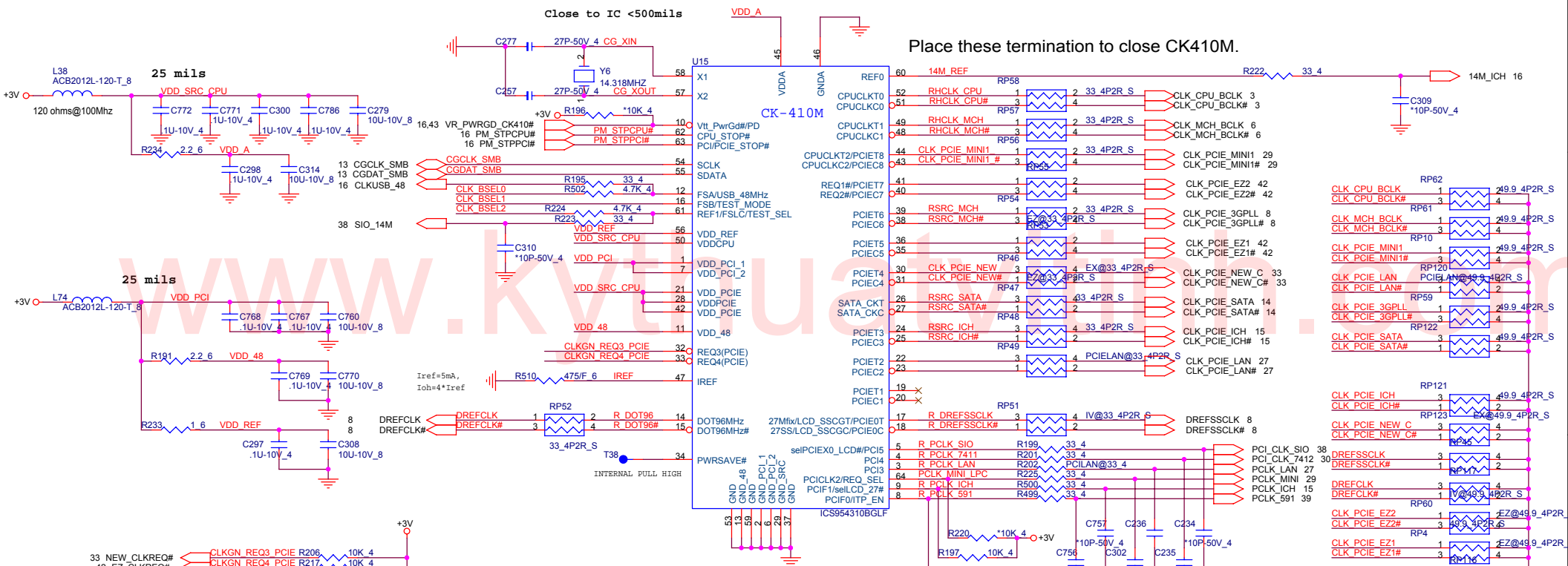


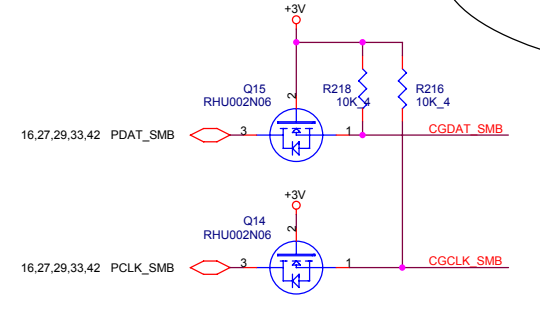
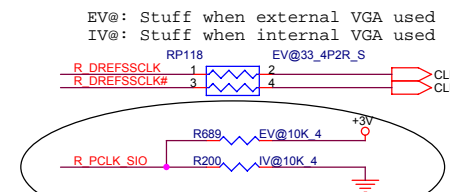
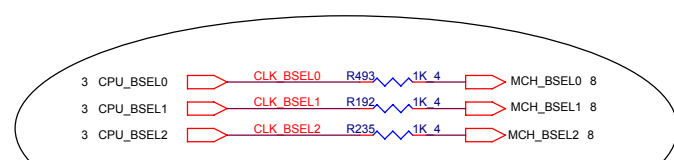
ZB1 SYSTEM BLOCK DIAGRAM



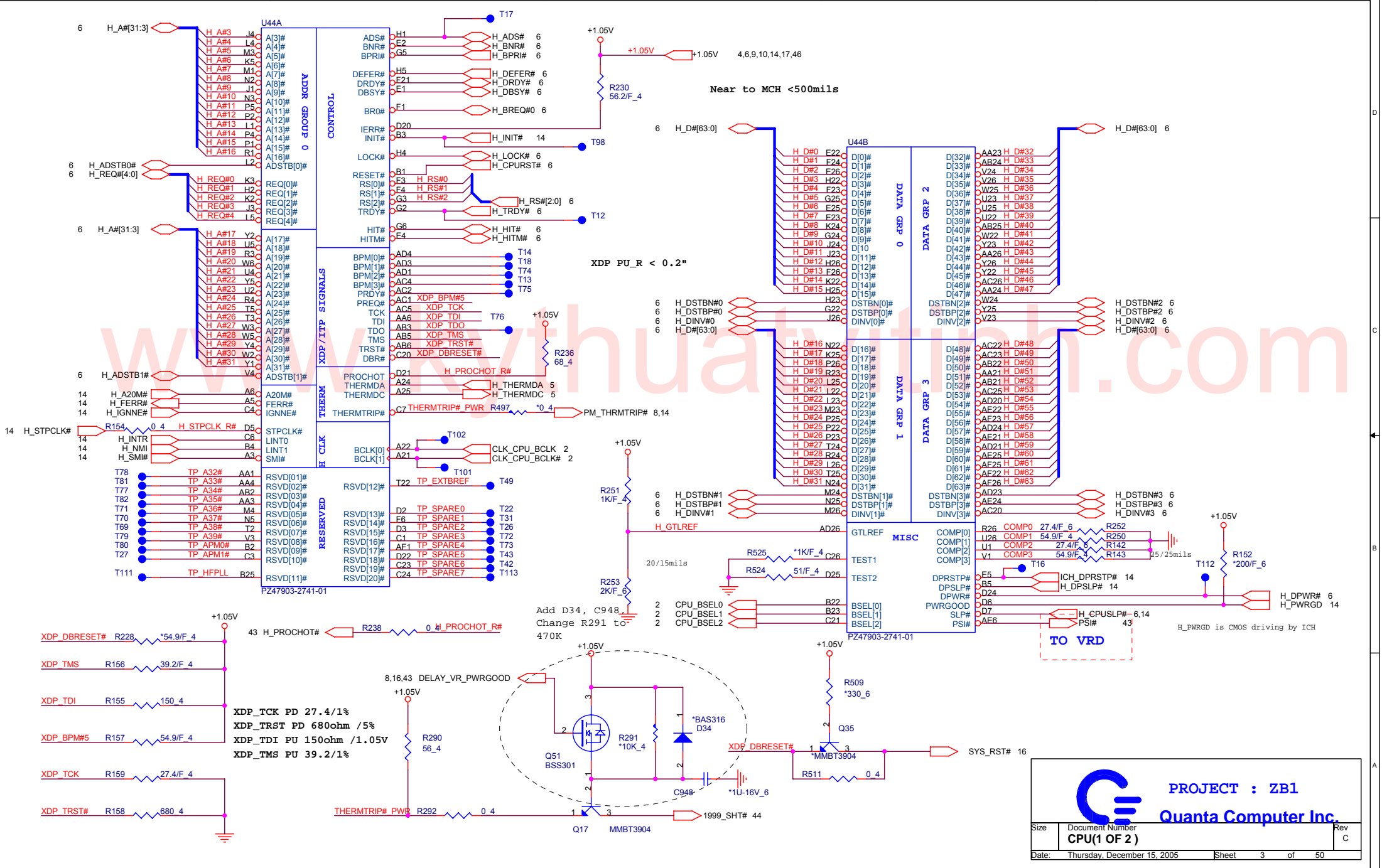



Place these termination to close CK410M.

BSEL strappings need to be set for 533MHz Moby Dick (Intel?915GM - Calistoga Interposer)
(if Calistoga is designed for 667MHz board).



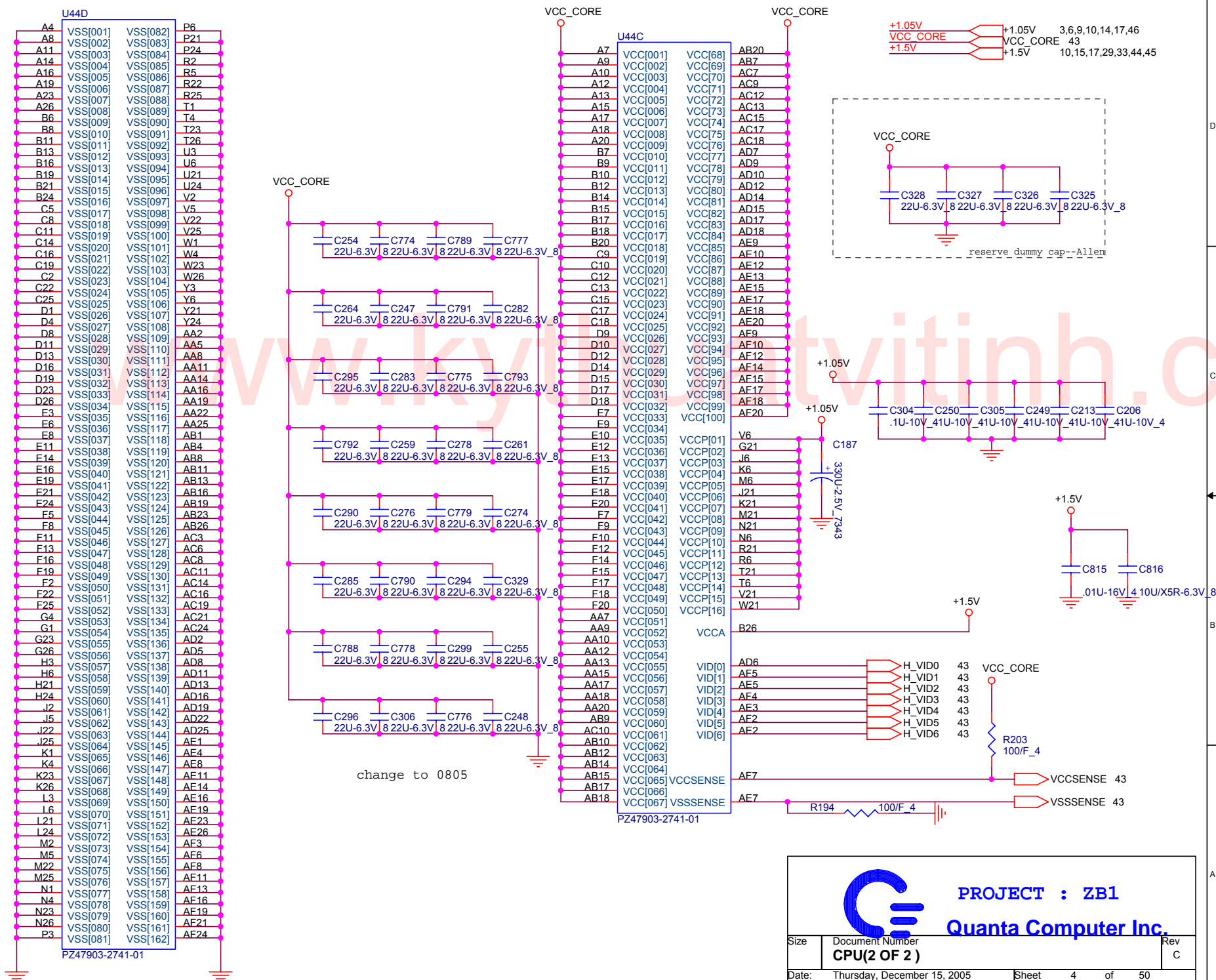
	FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100		33
0	0	1	133	100		33
0	1	1	166	100		33
0	1	0	200	100		33
0	0	0	266	100		33
1	0	0	333	100		33
1	1	0	400	100		33
1	1	1	200	100		33





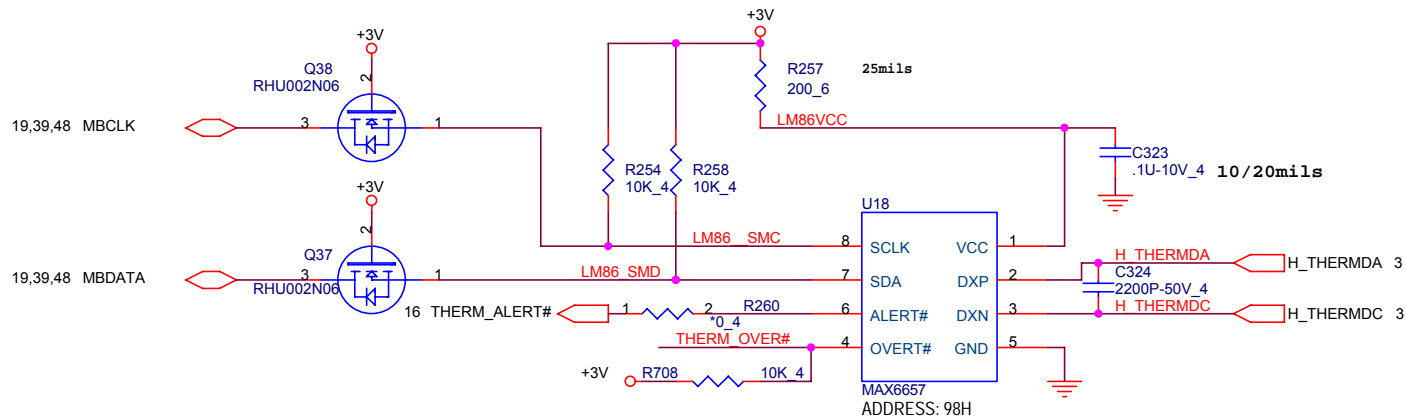
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	CPU(1 OF 2)	Rev
			C
Date:	Thursday, December 15, 2005	Sheet	3 of 50



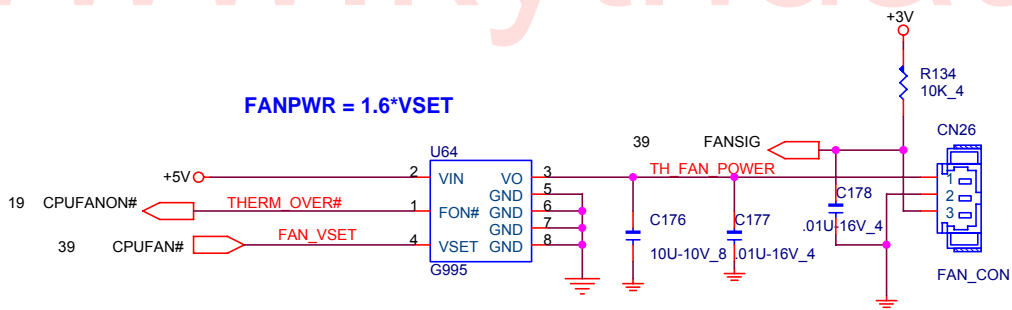
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev	
	CPU(2 OF 2)	C	
Date:	Thursday, December 15, 2005	Sheet	4 of 50




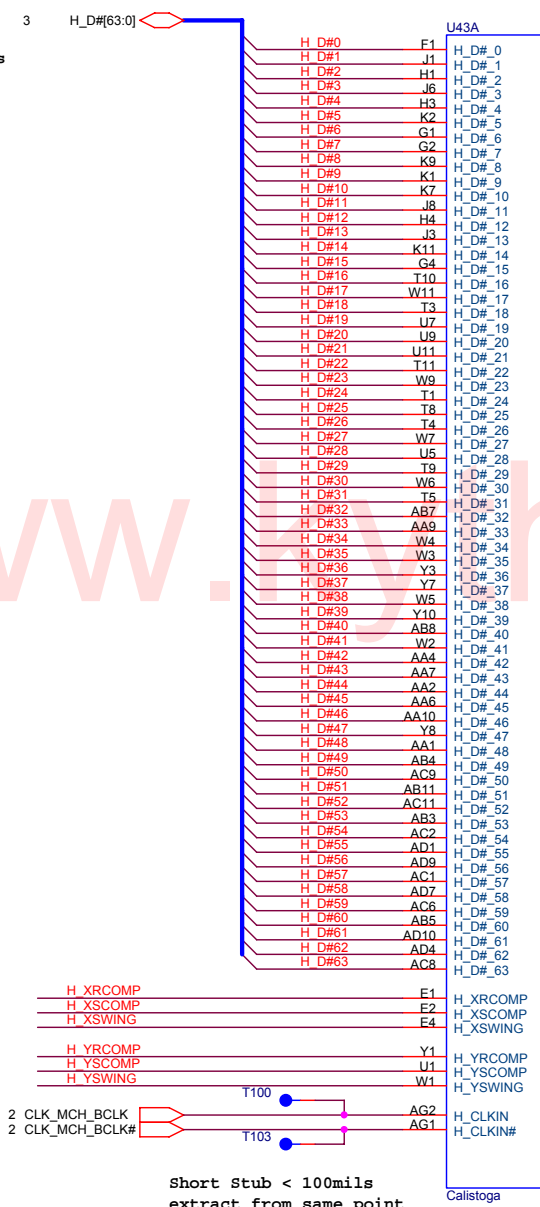
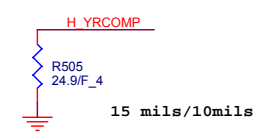
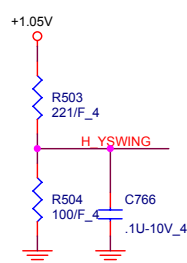
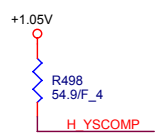
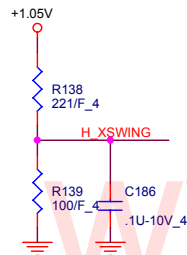
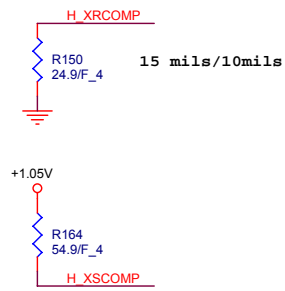
www.kythuatvithinh.com

CPU FAN



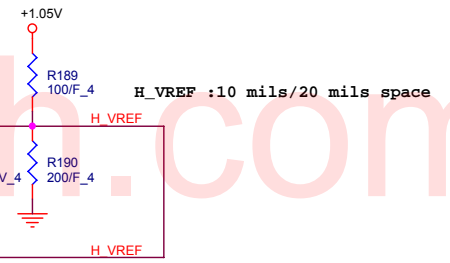
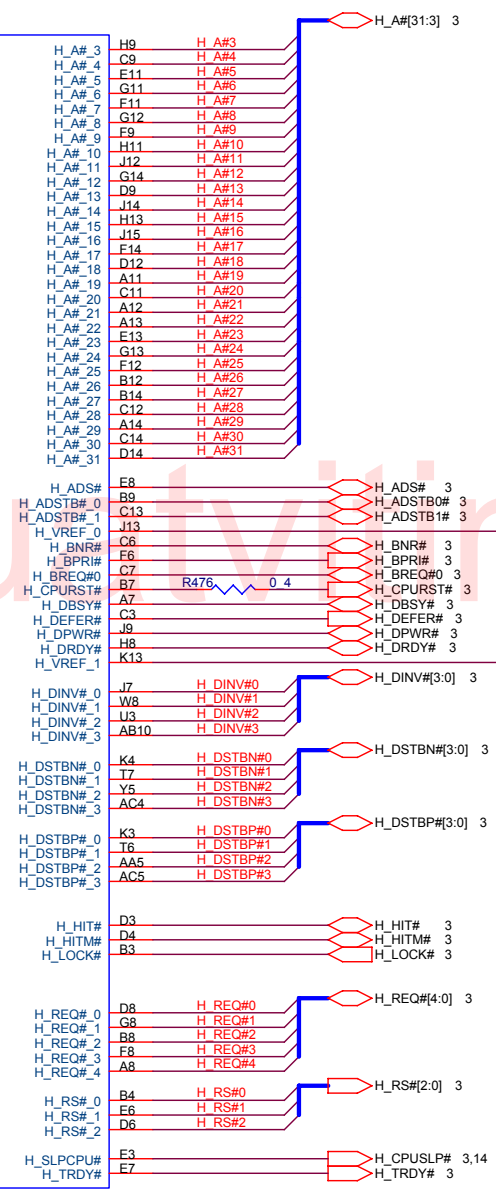
FANPWR = 1.6*VSET

		PROJECT : ZB1	
		Quanta Computer Inc. Thermal Sensor LM86	
Size	Docu	Number	Rev
Date:	Thursday, December 15, 2005	Sheet	5 of 50



Short Stub < 100mils
extract from same point

HOST



COMPONENTS	P/N
945GM	AJ009450T04
945PM	AJ009450T12

PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number GMCH HOST(1 OF 6)	Rev C
Date:	Thursday, December 15, 2005	Sheet 6 of 50

13 M_A_DQ[63:0]

M A DQ0	AJ35	SA_DQ0
M A DQ1	AJ34	SA_DQ1
M A DQ2	AM31	SA_DQ2
M A DQ3	AM33	SA_DQ3
M A DQ4	AJ36	SA_DQ4
M A DQ5	AK35	SA_DQ5
M A DQ6	AJ32	SA_DQ6
M A DQ7	AH31	SA_DQ7
M A DQ8	AN35	SA_DQ8
M A DQ9	AP33	SA_DQ9
M A DQ10	AR31	SA_DQ10
M A DQ11	AP31	SA_DQ11
M A DQ12	AN38	SA_DQ12
M A DQ13	AM36	SA_DQ13
M A DQ14	AM34	SA_DQ14
M A DQ15	AN33	SA_DQ15
M A DQ16	AK26	SA_DQ16
M A DQ17	AL27	SA_DQ17
M A DQ18	AM26	SA_DQ18
M A DQ19	AN24	SA_DQ19
M A DQ20	AK28	SA_DQ20
M A DQ21	AL28	SA_DQ21
M A DQ22	AM24	SA_DQ22
M A DQ23	AP26	SA_DQ23
M A DQ24	AP23	SA_DQ24
M A DQ25	AL22	SA_DQ25
M A DQ26	AP21	SA_DQ26
M A DQ27	AN20	SA_DQ27
M A DQ28	AL23	SA_DQ28
M A DQ29	AP24	SA_DQ29
M A DQ30	AP20	SA_DQ30
M A DQ31	AT21	SA_DQ31
M A DQ32	AR12	SA_DQ32
M A DQ33	AR14	SA_DQ33
M A DQ34	AP13	SA_DQ34
M A DQ35	AP12	SA_DQ35
M A DQ36	AT13	SA_DQ36
M A DQ37	AT12	SA_DQ37
M A DQ38	AL14	SA_DQ38
M A DQ39	AL12	SA_DQ39
M A DQ40	AK9	SA_DQ40
M A DQ41	AN7	SA_DQ41
M A DQ42	AK8	SA_DQ42
M A DQ43	AK7	SA_DQ43
M A DQ44	AP9	SA_DQ44
M A DQ45	AN9	SA_DQ45
M A DQ46	AT5	SA_DQ46
M A DQ47	AL5	SA_DQ47
M A DQ48	AY2	SA_DQ48
M A DQ49	AW2	SA_DQ49
M A DQ50	AP1	SA_DQ50
M A DQ51	AN2	SA_DQ51
M A DQ52	AV2	SA_DQ52
M A DQ53	AT3	SA_DQ53
M A DQ54	AN1	SA_DQ54
M A DQ55	AL2	SA_DQ55
M A DQ56	AG7	SA_DQ56
M A DQ57	AE9	SA_DQ57
M A DQ58	AG4	SA_DQ58
M A DQ59	AE6	SA_DQ59
M A DQ60	AG9	SA_DQ60
M A DQ61	AH6	SA_DQ61
M A DQ62	AF4	SA_DQ62
M A DQ63	AF8	SA_DQ63

U43D

DDR SYSTEM MEMORY A

Calistoga

SA_BS_0	AU12	M A BS#0
SA_BS_1	AV14	M A BS#1
SA_BS_2	BA20	M A BS#2
SA_CAS#	AY13	M A CAS#
SA_DM_0	AJ33	M A DM0
SA_DM_1	AM35	M A DM1
SA_DM_2	AL26	M A DM2
SA_DM_3	AN22	M A DM3
SA_DM_4	AM14	M A DM4
SA_DM_5	AL9	M A DM5
SA_DM_6	AR3	M A DM6
SA_DM_7	AH4	M A DM7
SA_DQS_0	AK33	M A DQS0
SA_DQS_1	AT33	M A DQS1
SA_DQS_2	AN28	M A DQS2
SA_DQS_3	AM22	M A DQS3
SA_DQS_4	AN12	M A DQS4
SA_DQS_5	AN8	M A DQS5
SA_DQS_6	AP3	M A DQS6
SA_DQS_7	AG5	M A DQS7
SA_DQS#_0	AK32	M A DQS#0
SA_DQS#_1	AU33	M A DQS#1
SA_DQS#_2	AN27	M A DQS#2
SA_DQS#_3	AM21	M A DQS#3
SA_DQS#_4	AM12	M A DQS#4
SA_DQS#_5	AL8	M A DQS#5
SA_DQS#_6	AN3	M A DQS#6
SA_DQS#_7	AH5	M A DQS#7
SA_MA_0	AY16	M A A0
SA_MA_1	AU14	M A A1
SA_MA_2	AW16	M A A2
SA_MA_3	BA16	M A A3
SA_MA_4	BA17	M A A4
SA_MA_5	AU16	M A A5
SA_MA_6	AV17	M A A6
SA_MA_7	AU17	M A A7
SA_MA_8	AW17	M A A8
SA_MA_9	AT16	M A A9
SA_MA_10	AU13	M A A10
SA_MA_11	AT17	M A A11
SA_MA_12	AV20	M A A12
SA_MA_13	AV12	M A A13

SA_RAS#	AW14	M_A_RAS# 12,13
SA_RCVENIN#	AK23	TP MA RCVENIN# T37
SA_RCVENOUT#	AK24	TP MA RCVENOUT# T36
SA_WE#	AY14	M_A_WE# 12,13

13 M_B_DQ[63:0]

M B DQ0	AK39	SB_DQ0
M B DQ1	AJ37	SB_DQ1
M B DQ2	AP39	SB_DQ2
M B DQ3	AR41	SB_DQ3
M B DQ4	AJ38	SB_DQ4
M B DQ5	AK38	SB_DQ5
M B DQ6	AN41	SB_DQ6
M B DQ7	AP41	SB_DQ7
M B DQ8	AT40	SB_DQ8
M B DQ9	AV41	SB_DQ9
M B DQ10	AU38	SB_DQ10
M B DQ11	AV38	SB_DQ11
M B DQ12	AP38	SB_DQ12
M B DQ13	AR40	SB_DQ13
M B DQ14	AW38	SB_DQ14
M B DQ15	AY38	SB_DQ15
M B DQ16	BA38	SB_DQ16
M B DQ17	AV36	SB_DQ17
M B DQ18	AR36	SB_DQ18
M B DQ19	AP36	SB_DQ19
M B DQ20	BA36	SB_DQ20
M B DQ21	AU36	SB_DQ21
M B DQ22	AP35	SB_DQ22
M B DQ23	AP34	SB_DQ23
M B DQ24	AY33	SB_DQ24
M B DQ25	BA33	SB_DQ25
M B DQ26	AT31	SB_DQ26
M B DQ27	AU29	SB_DQ27
M B DQ28	AU31	SB_DQ28
M B DQ29	AW31	SB_DQ29
M B DQ30	AV29	SB_DQ30
M B DQ31	AW29	SB_DQ31
M B DQ32	AL19	SB_DQ32
M B DQ33	AP14	SB_DQ33
M B DQ34	AN14	SB_DQ34
M B DQ35	AN14	SB_DQ35
M B DQ36	AN17	SB_DQ36
M B DQ37	AM16	SB_DQ37
M B DQ38	AP15	SB_DQ38
M B DQ39	AL15	SB_DQ39
M B DQ40	AJ11	SB_DQ40
M B DQ41	AH10	SB_DQ41
M B DQ42	AJ9	SB_DQ42
M B DQ43	AN10	SB_DQ43
M B DQ44	AK13	SB_DQ44
M B DQ45	AH11	SB_DQ45
M B DQ46	AK10	SB_DQ46
M B DQ47	AJ8	SB_DQ47
M B DQ48	BA10	SB_DQ48
M B DQ49	AW10	SB_DQ49
M B DQ50	BA4	SB_DQ50
M B DQ51	AW4	SB_DQ51
M B DQ52	AY10	SB_DQ52
M B DQ53	AY9	SB_DQ53
M B DQ54	AW5	SB_DQ54
M B DQ55	AY5	SB_DQ55
M B DQ56	AV4	SB_DQ56
M B DQ57	AR5	SB_DQ57
M B DQ58	AK4	SB_DQ58
M B DQ59	AK3	SB_DQ59
M B DQ60	AT4	SB_DQ60
M B DQ61	AK5	SB_DQ61
M B DQ62	AJ5	SB_DQ62
M B DQ63	AJ3	SB_DQ63

U43E

DDR SYSTEM MEMORY B

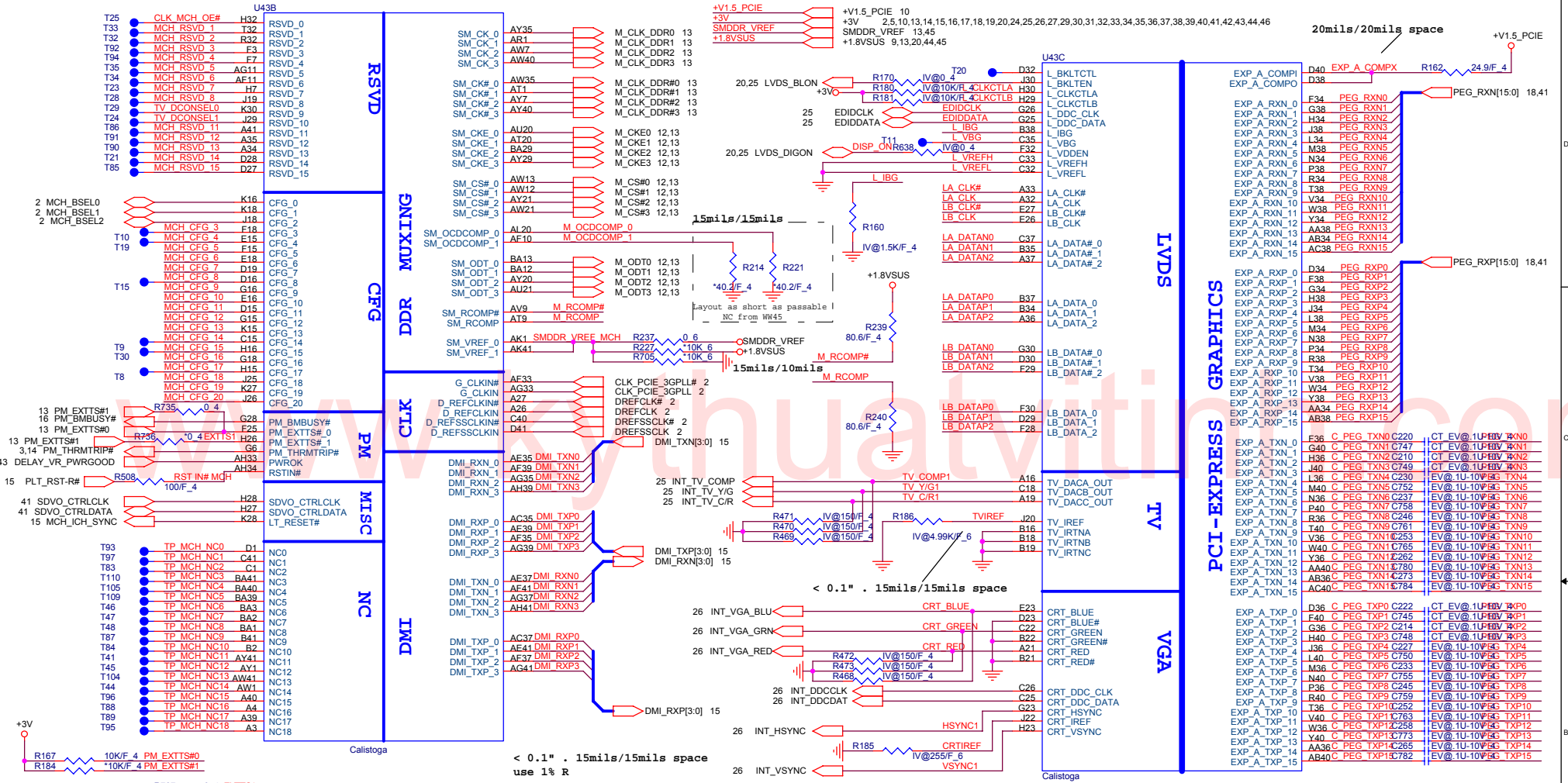
Calistoga

SB_BS_0	AT24	M_B_BS#0 12,13
SB_BS_1	AV23	M_B_BS#1 12,13
SB_BS_2	AY28	M_B_BS#2 12,13
SB_CAS#	AR24	M_B_CAS# 12,13
SB_DM_0	AK36	M_B DM0
SB_DM_1	AR38	M_B DM1
SB_DM_2	AT36	M_B DM2
SB_DM_3	BA31	M_B DM3
SB_DM_4	AL17	M_B DM4
SB_DM_5	AH8	M_B DM5
SB_DM_6	BA5	M_B DM6
SB_DM_7	AN4	M_B DM7
SB_DQS_0	AM39	M_B DQS0
SB_DQS_1	AT39	M_B DQS1
SB_DQS_2	AU35	M_B DQS2
SB_DQS_3	AR29	M_B DQS3
SB_DQS_4	AR16	M_B DQS4
SB_DQS_5	AR10	M_B DQS5
SB_DQS_6	AR7	M_B DQS6
SB_DQS_7	AN5	M_B DQS7
SB_DQS#_0	AM40	M_B DQS#0
SB_DQS#_1	AU39	M_B DQS#1
SB_DQS#_2	AT35	M_B DQS#2
SB_DQS#_3	AP29	M_B DQS#3
SB_DQS#_4	AP16	M_B DQS#4
SB_DQS#_5	AT10	M_B DQS#5
SB_DQS#_6	AT7	M_B DQS#6
SB_DQS#_7	AP5	M_B DQS#7
SB_MA_0	AY23	M_B A0
SB_MA_1	AW24	M_B A1
SB_MA_2	AY24	M_B A2
SB_MA_3	AR28	M_B A3
SB_MA_4	AT27	M_B A4
SB_MA_5	AT28	M_B A5
SB_MA_6	AU27	M_B A6
SB_MA_7	AV28	M_B A7
SB_MA_8	AV27	M_B A8
SB_MA_9	AW27	M_B A9
SB_MA_10	AV24	M_B A10
SB_MA_11	BA27	M_B A11
SB_MA_12	AY27	M_B A12
SB_MA_13	AR23	M_B A13
SB_RAS#	AU23	M_B_RAS# 12,13
SB_RCVENIN#	AK16	TP MB RCVENIN# T39
SB_RCVENOUT#	AK18	TP MB RCVENOUT# T40
SB_WE#	AR27	M_B_WE# 12,13



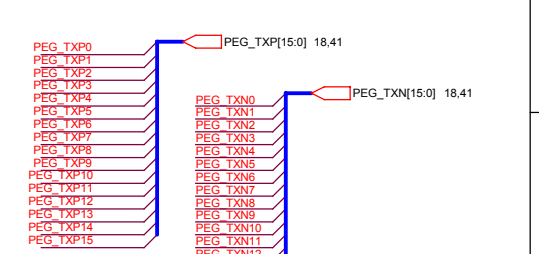
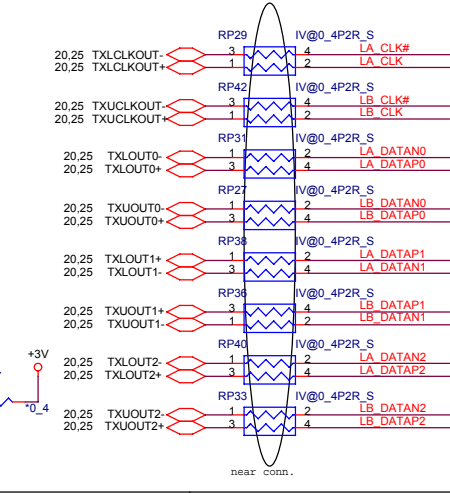
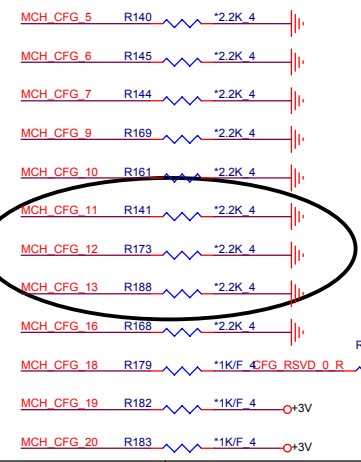
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(2 OF 6)	C
Date:	Thursday, December 15, 2005	Sheet 7 of 50



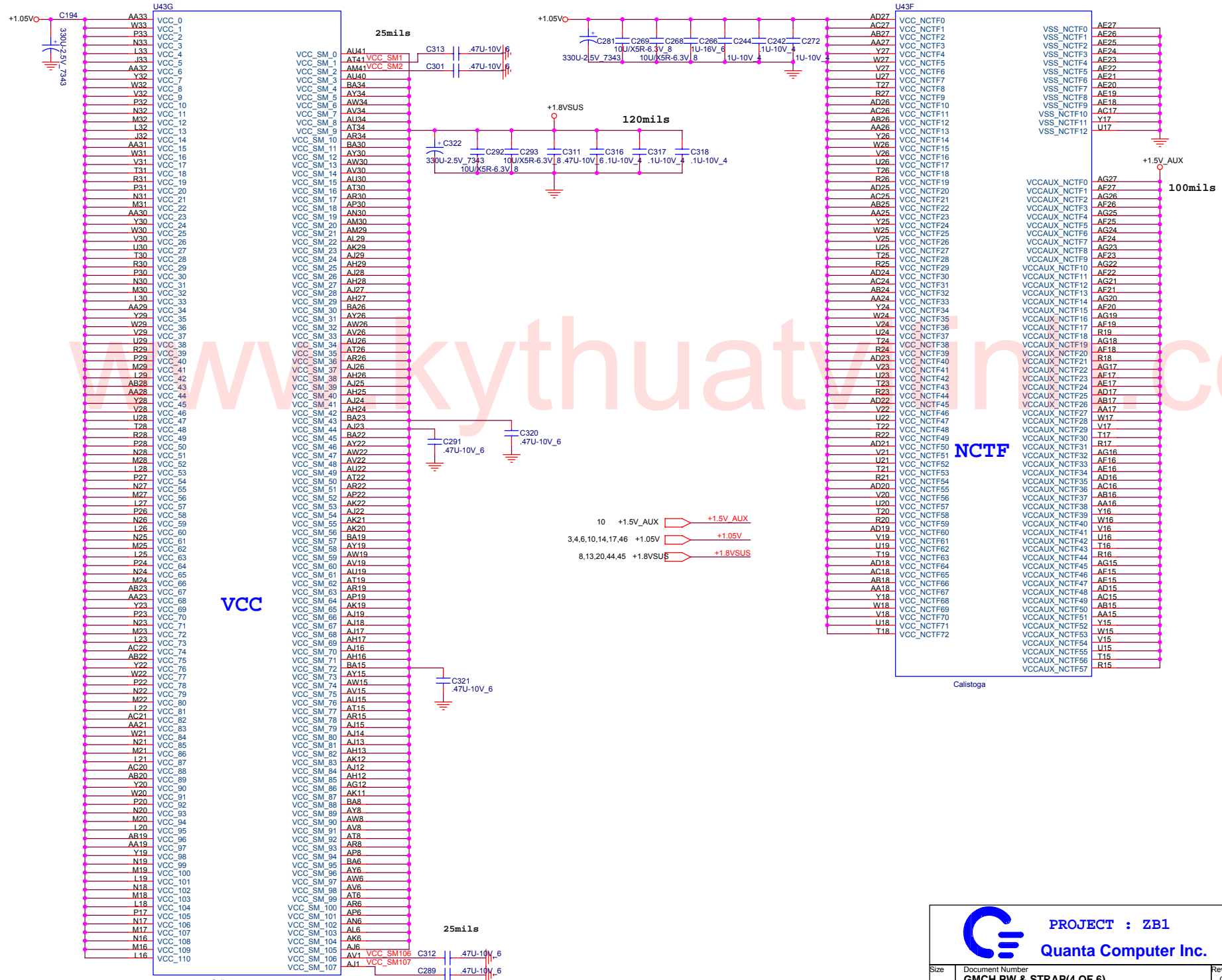
- 16.43 PM_DPRSLPVR \square R737 \square 0.4 EXITS!
- MCH_CFG_5 Low = DMI X2, High=DMIX4
 - MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
 - MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
 - MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
 - MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
 - MCH_CFG_11: Low=Calistoga, High=Reserved
 - MCH_CFG_16 FSB Dynamic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
 - MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
 - MCH_CFG_19 DMI LANE Reversal: Low=Normal,High=LANES Reversed.
 - MCH_CFG_20 PCIE Backward interoperability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

GMCH Strap pin



PROJECT : ZB1
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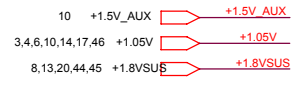
Size	Document Number	Rev
	GMCH DMI/VEDIO(3 OF 6)	C
Date:	Thursday, December 15, 2005	Sheet 8 of 50



VCC

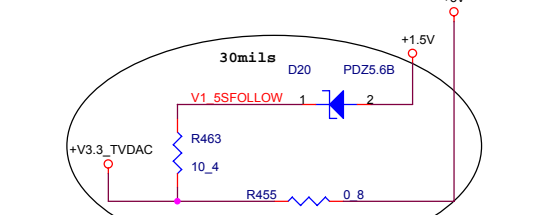
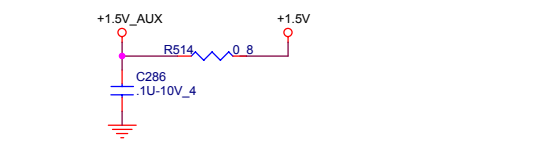
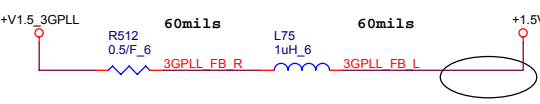
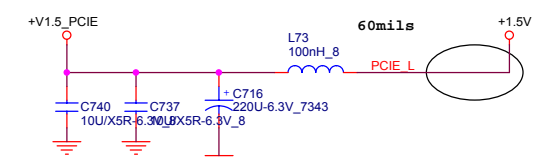
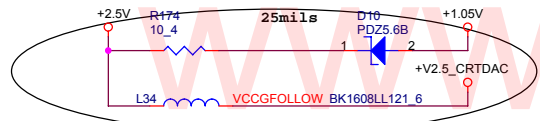
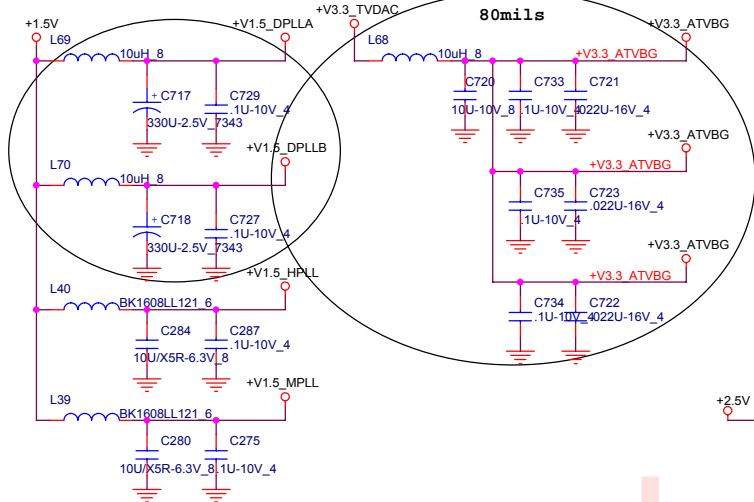
NCTF

Calistoga

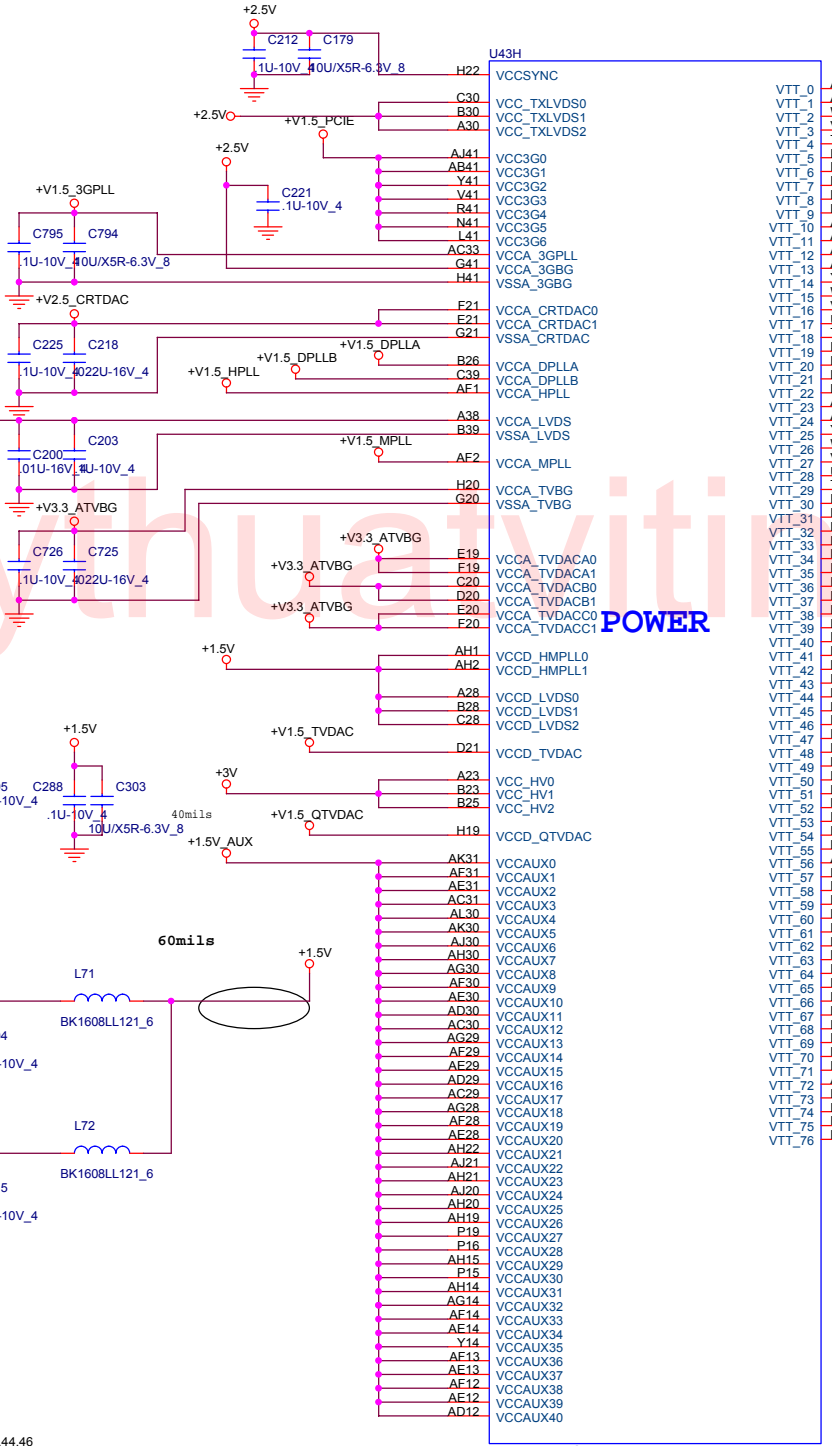


PROJECT : ZB1
Quanta Computer Inc.

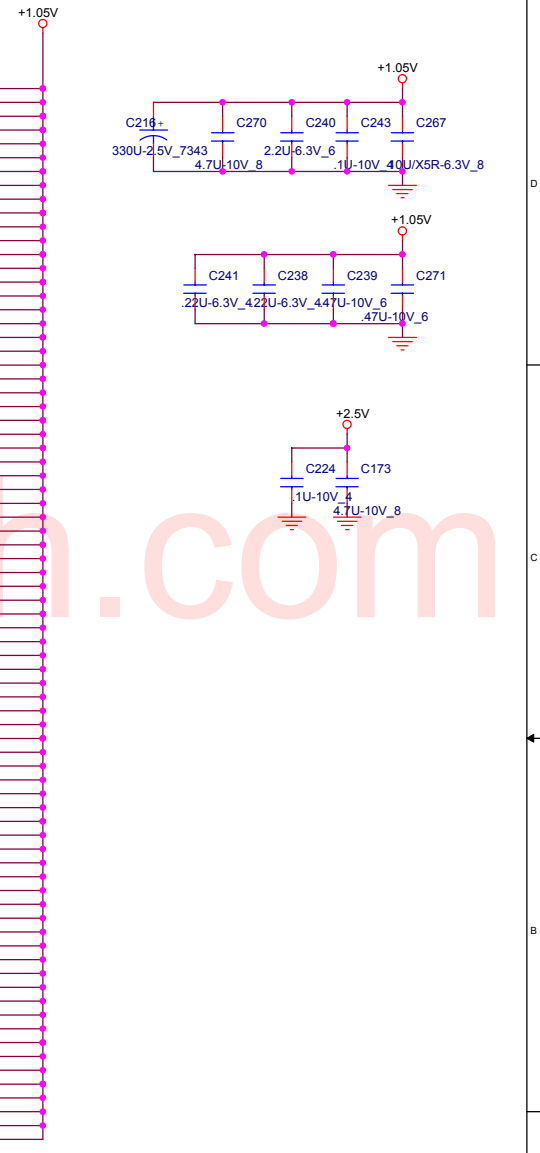
Size	Document Number	Rev
	GMCH PW & STRAP(4 OF 6)	C
Date:	Thursday, December 15, 2005	Sheet 9 of 50



+1.05V	+1.05V	3,4,6,9,14,17,46
+1.5V	+1.5V	4,15,17,29,33,44,45
+V1.5_PCIE	+V1.5_PCIE	8
+2.5V	+2.5V	19,20,25,41,44,45
+3V	+3V	2,5,8,13,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,46



POWER



PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH POWER (5 OF 6)	C
Date:	Thursday, December 15, 2005	Sheet 10 of 50

Calistoga


U43I		
AC41	VSS_0	VSS_97
AA41	VSS_1	VSS_98
V41	VSS_2	VSS_99
T41	VSS_3	VSS_100
P41	VSS_4	VSS_101
M41	VSS_5	VSS_102
J41	VSS_6	VSS_103
F41	VSS_7	VSS_104
AV40	VSS_8	VSS_105
AF40	VSS_9	VSS_106
AN40	VSS_10	VSS_107
AK40	VSS_11	VSS_108
AL40	VSS_12	VSS_109
AH40	VSS_13	VSS_110
AG40	VSS_14	VSS_111
AF40	VSS_15	VSS_112
AE40	VSS_16	VSS_113
E40	VSS_17	VSS_114
AY39	VSS_18	VSS_115
AW39	VSS_19	VSS_116
AV39	VSS_20	VSS_117
AR39	VSS_21	VSS_118
AN39	VSS_22	VSS_119
AJ39	VSS_23	VSS_120
AC39	VSS_24	VSS_121
AB39	VSS_25	VSS_122
AA39	VSS_26	VSS_123
Y39	VSS_27	VSS_124
W39	VSS_28	VSS_125
V39	VSS_29	VSS_126
T39	VSS_30	VSS_127
R39	VSS_31	VSS_128
P39	VSS_32	VSS_129
N39	VSS_33	VSS_130
M39	VSS_34	VSS_131
L39	VSS_35	VSS_132
J39	VSS_36	VSS_133
H39	VSS_37	VSS_134
G39	VSS_38	VSS_135
F39	VSS_39	VSS_136
D39	VSS_40	VSS_137
AT38	VSS_41	VSS_138
AM38	VSS_42	VSS_139
AH38	VSS_43	VSS_140
AG38	VSS_44	VSS_141
AF38	VSS_45	VSS_142
AE38	VSS_46	VSS_143
C38	VSS_47	VSS_144
AK37	VSS_48	VSS_145
AH37	VSS_49	VSS_146
AB37	VSS_50	VSS_147
AA37	VSS_51	VSS_148
Y37	VSS_52	VSS_149
W37	VSS_53	VSS_150
V37	VSS_54	VSS_151
T37	VSS_55	VSS_152
R37	VSS_56	VSS_153
P37	VSS_57	VSS_154
N37	VSS_58	VSS_155
M37	VSS_59	VSS_156
L37	VSS_60	VSS_157
J37	VSS_61	VSS_158
H37	VSS_62	VSS_159
G37	VSS_63	VSS_160
F37	VSS_64	VSS_161
D37	VSS_65	VSS_162
AY36	VSS_66	VSS_163
AW36	VSS_67	VSS_164
AV36	VSS_68	VSS_165
AH36	VSS_69	VSS_166
AG36	VSS_70	VSS_167
AF36	VSS_71	VSS_168
AE36	VSS_72	VSS_169
AC36	VSS_73	VSS_170
C36	VSS_74	VSS_171
B36	VSS_75	VSS_172
BA35	VSS_76	VSS_173
AV35	VSS_77	VSS_174
AR35	VSS_78	VSS_175
AH35	VSS_79	VSS_176
AB35	VSS_80	VSS_177
AA35	VSS_81	VSS_178
Y35	VSS_82	VSS_179
W35	VSS_83	
V35	VSS_84	
T35	VSS_85	
R35	VSS_86	
P35	VSS_87	
N35	VSS_88	
M35	VSS_89	
L35	VSS_90	
J35	VSS_91	
H35	VSS_92	
G35	VSS_93	
F35	VSS_94	
D35	VSS_95	
AN34	VSS_96	

Callistoga

U43J		
AT23	VSS_180	VSS_273
AN23	VSS_181	VSS_274
AM23	VSS_182	VSS_275
AH23	VSS_183	VSS_276
AC23	VSS_184	VSS_277
W23	VSS_185	VSS_278
K23	VSS_186	VSS_279
AV33	VSS_187	VSS_280
F23	VSS_188	VSS_281
C23	VSS_189	VSS_282
AA22	VSS_190	VSS_283
K22	VSS_191	VSS_284
G22	VSS_192	VSS_285
F22	VSS_193	VSS_286
E22	VSS_194	VSS_287
D22	VSS_195	VSS_288
A22	VSS_196	VSS_289
BA21	VSS_197	VSS_290
AV21	VSS_198	VSS_291
AR21	VSS_199	VSS_292
AN21	VSS_200	VSS_293
AL21	VSS_201	VSS_294
AB21	VSS_202	VSS_295
Y21	VSS_203	VSS_296
P21	VSS_204	VSS_297
K21	VSS_205	VSS_298
AB32	VSS_206	VSS_299
H21	VSS_207	VSS_300
C21	VSS_208	VSS_301
AW20	VSS_209	VSS_302
AR20	VSS_210	VSS_303
AM20	VSS_211	VSS_304
AA20	VSS_212	VSS_305
K20	VSS_213	VSS_306
B20	VSS_214	VSS_307
Y21	VSS_215	VSS_308
AN19	VSS_216	VSS_309
AC19	VSS_217	VSS_310
W19	VSS_218	VSS_311
K19	VSS_219	VSS_312
G19	VSS_220	VSS_313
C19	VSS_221	VSS_314
AH18	VSS_222	VSS_315
K18	VSS_223	VSS_316
H18	VSS_224	VSS_317
D18	VSS_225	VSS_318
A18	VSS_226	VSS_319
AY17	VSS_227	VSS_320
AR17	VSS_228	VSS_321
AP17	VSS_229	VSS_322
AM17	VSS_230	VSS_323
AK17	VSS_231	VSS_324
AV16	VSS_232	VSS_325
AN16	VSS_233	VSS_326
AL16	VSS_234	VSS_327
J16	VSS_235	VSS_328
F16	VSS_236	VSS_329
C16	VSS_237	VSS_330
AN15	VSS_238	VSS_331
AM15	VSS_239	VSS_332
AK15	VSS_240	VSS_333
N15	VSS_241	VSS_334
M15	VSS_242	VSS_335
L15	VSS_243	VSS_336
B15	VSS_244	VSS_337
A15	VSS_245	VSS_338
BA14	VSS_246	VSS_339
AT14	VSS_247	VSS_340
AK14	VSS_248	VSS_341
K14	VSS_249	VSS_342
AD14	VSS_250	VSS_343
A14	VSS_251	VSS_344
U14	VSS_252	VSS_345
K14	VSS_253	VSS_346
H14	VSS_254	VSS_347
AV13	VSS_255	VSS_348
AR13	VSS_256	VSS_349
D25	VSS_257	VSS_350
AM13	VSS_258	VSS_351
AL13	VSS_259	VSS_352
AG13	VSS_260	VSS_353
P13	VSS_261	VSS_354
F13	VSS_262	VSS_355
D13	VSS_263	VSS_356
B13	VSS_264	VSS_357
AY12	VSS_265	VSS_358
AC12	VSS_266	VSS_359
K12	VSS_267	VSS_360
H12	VSS_268	
E12	VSS_269	
AD11	VSS_270	
AA11	VSS_271	
Y11	VSS_272	

VSS

Callistoga

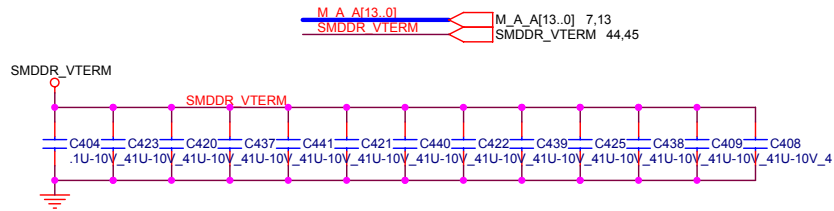


PROJECT : ZB1
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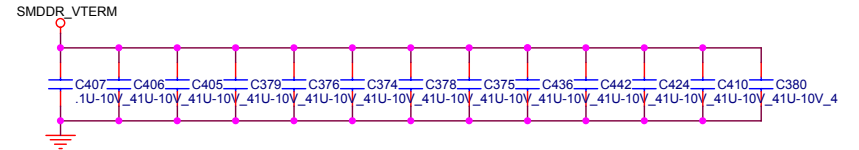
Size	Document Number	Rev
	GMCH GND(6 OF 6)	C
Date:	Thursday, December 15, 2005	Sheet 11 of 50

DDRII DUAL CHANNEL A,B.

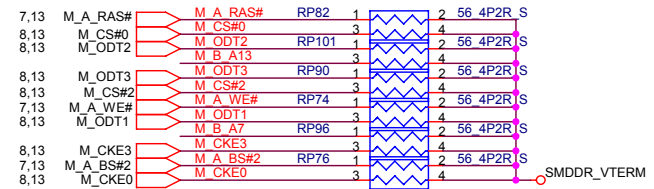
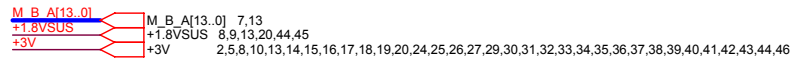
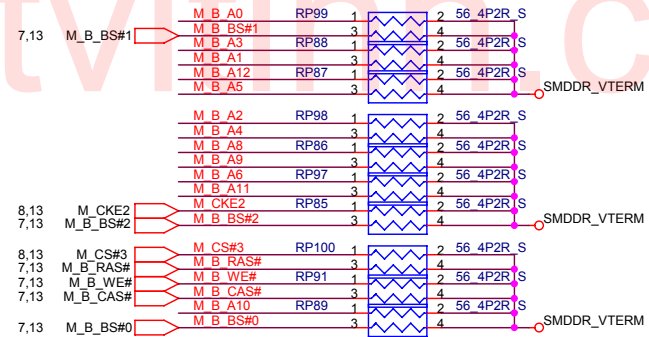
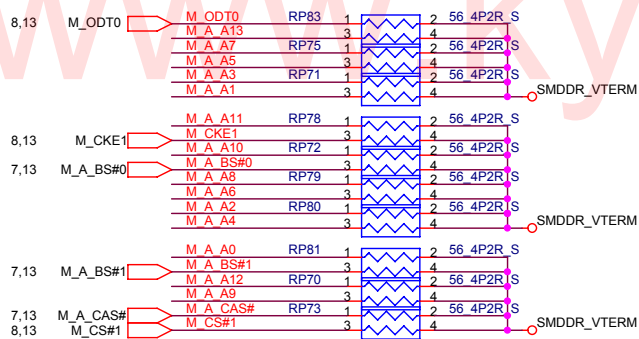
DDRII A CHANNEL



DDRII B CHANNEL

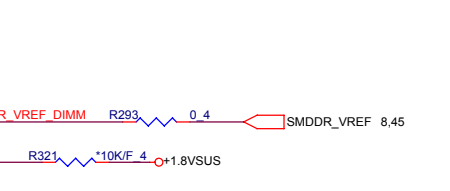
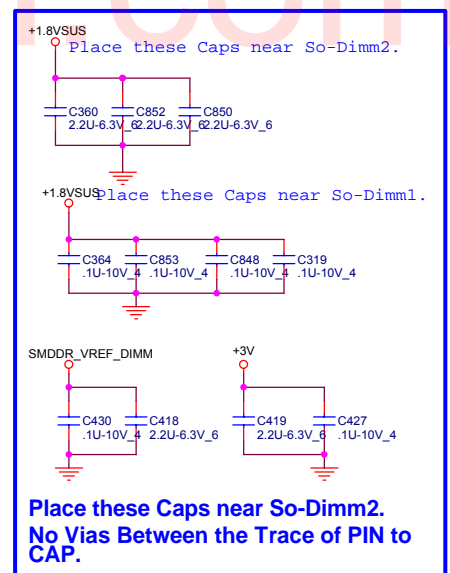
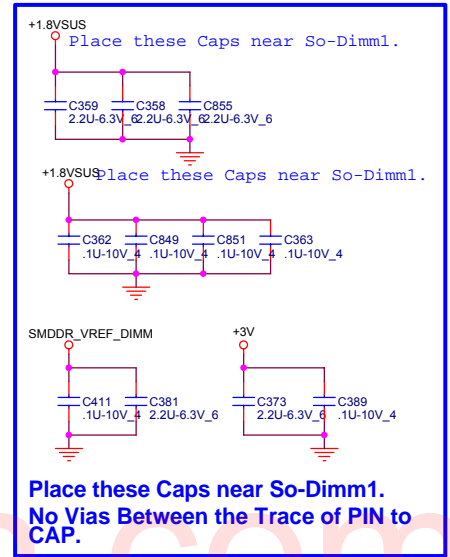
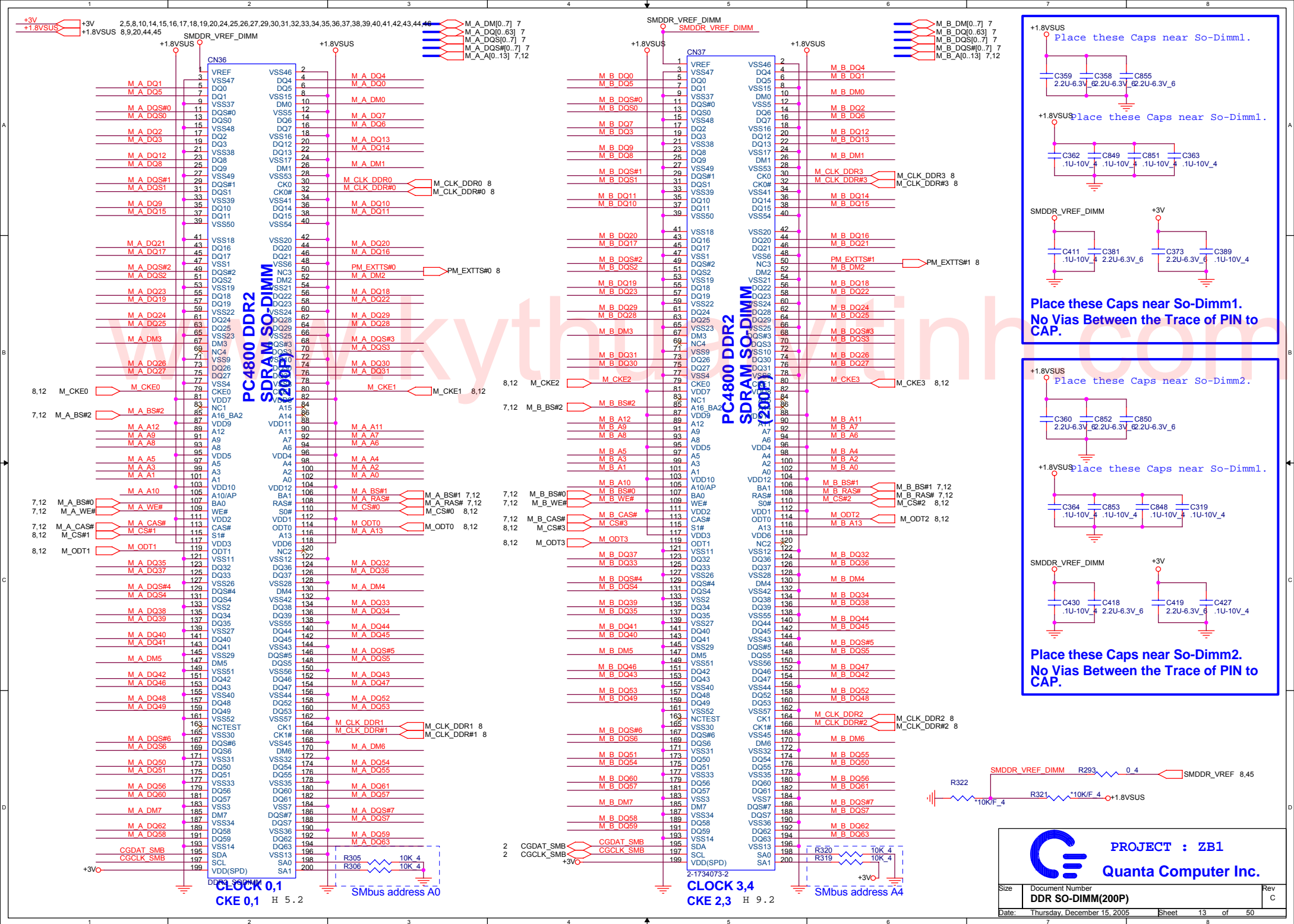


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



PROJECT : ZB1
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Size	Document Number	Rev
	DDR RES. ARRAY	C
Date:	Thursday, December 15, 2005	Sheet 12 of 50



PROJECT : ZB1

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Size	Document Number	Rev
	DDR SO-DIMM(200P)	C
Date:	Thursday, December 15, 2005	Sheet 13 of 50

CLOCK 0,1
CKE 0,1 H 5.2

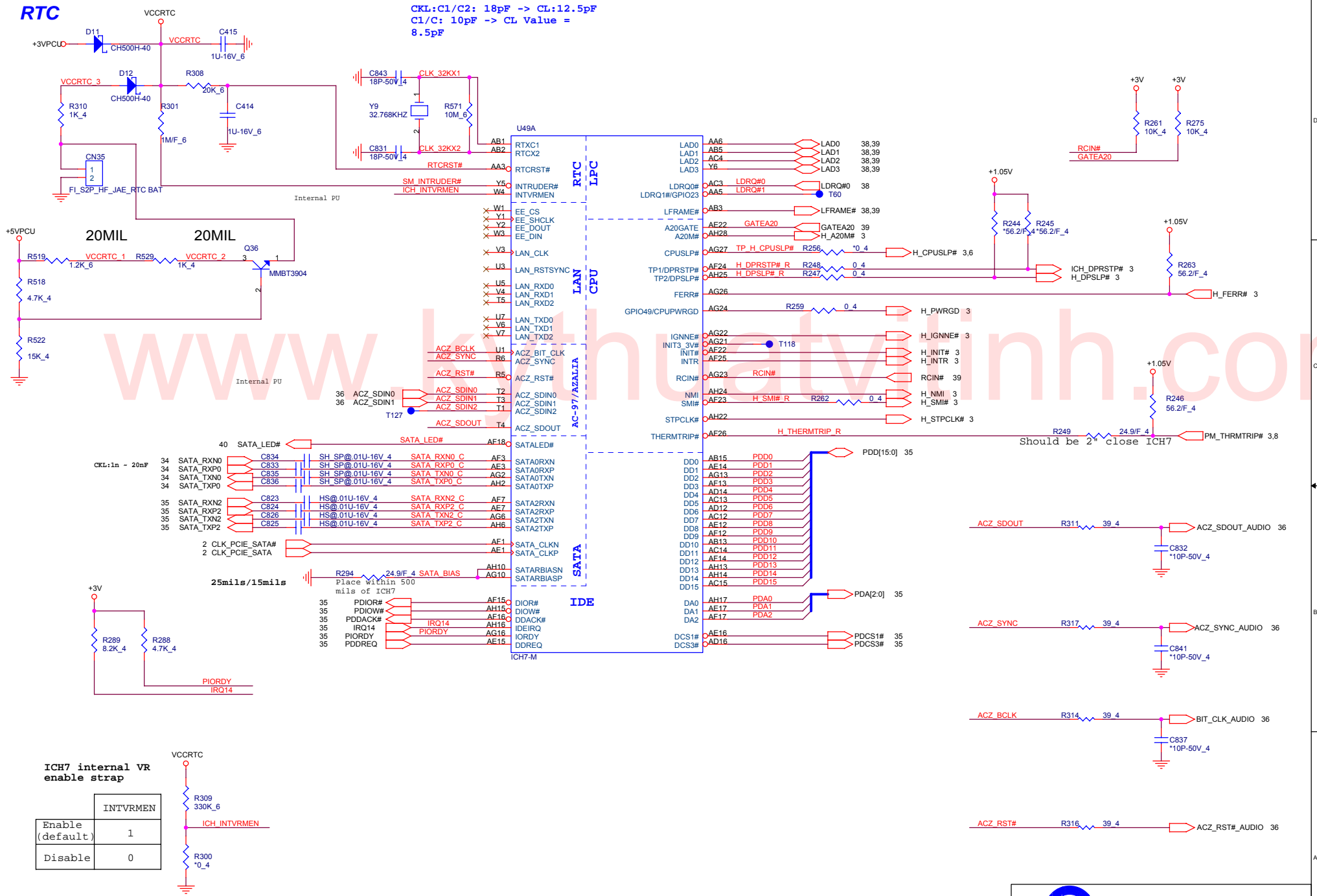
CLOCK 3,4
CKE 2,3 H 9.2

SMBus address A0

SMBus address A4

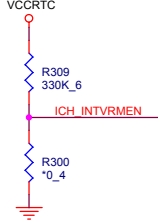
RTC

CLK: C1/C2: 18pF -> CL: 12.5pF
 C1/C: 10pF -> CL Value = 8.5pF



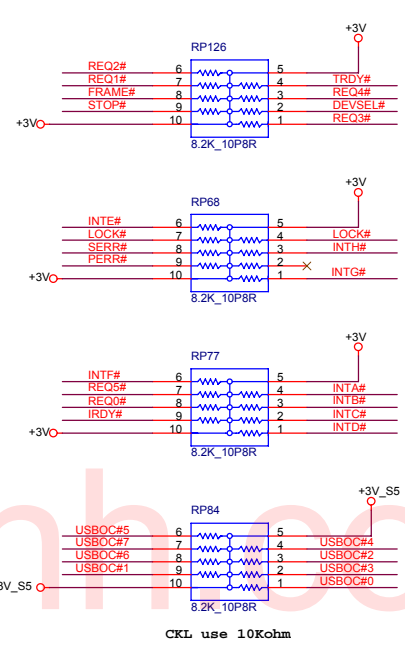
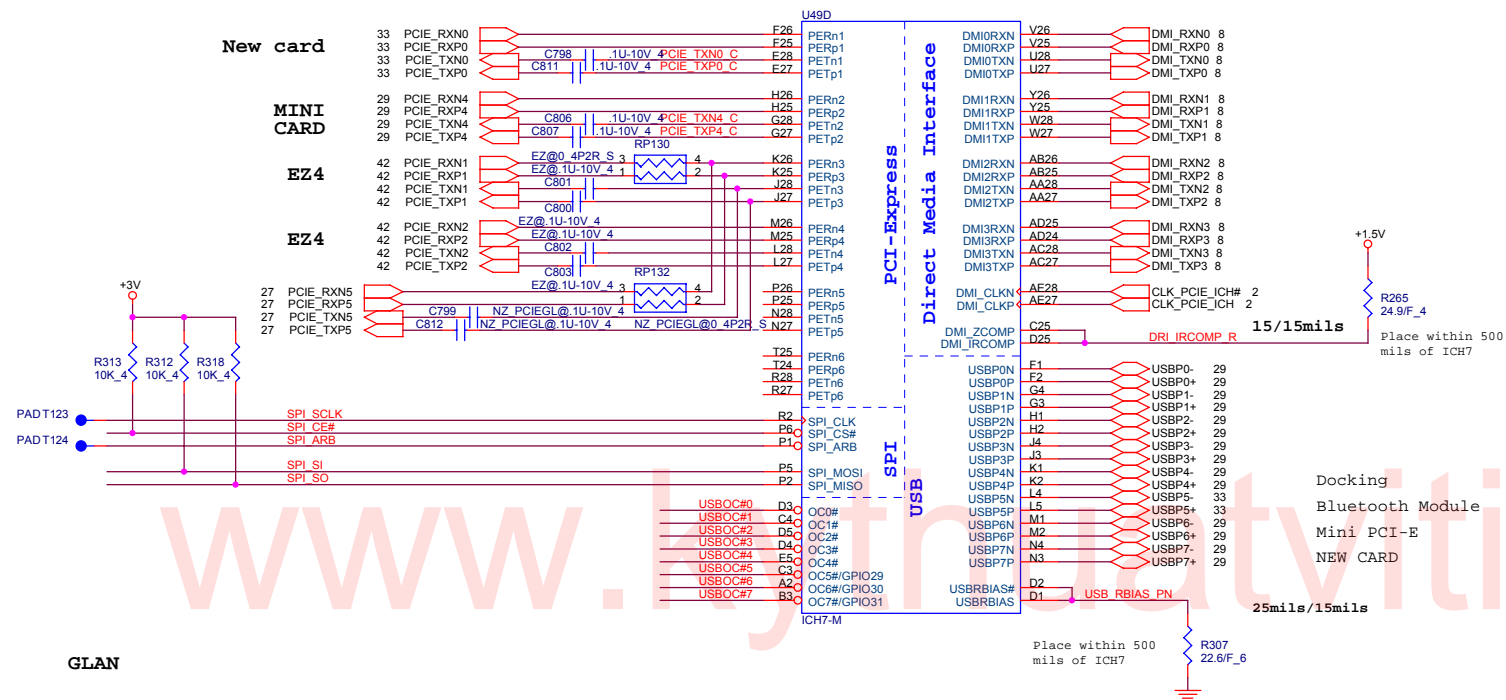
ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0



PROJECT : ZB1
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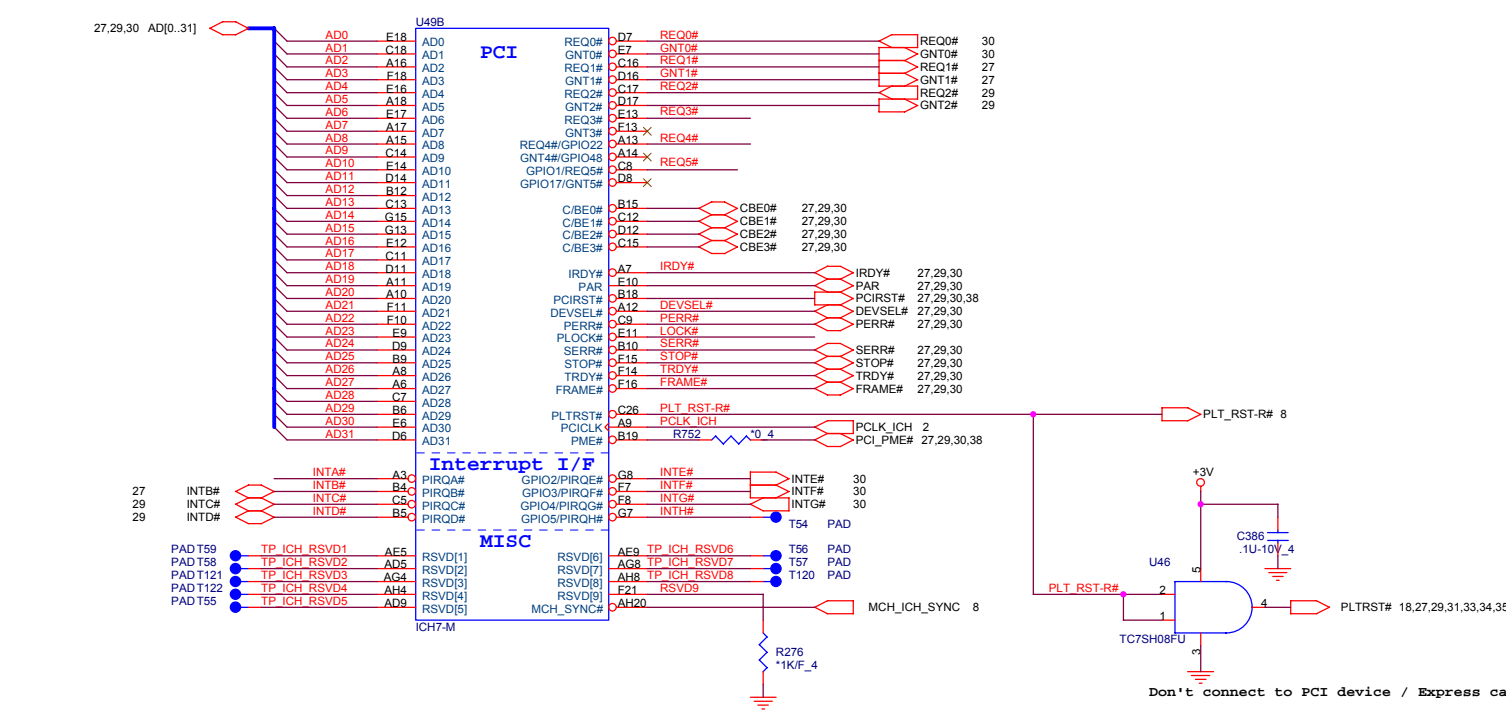
Size	Document Number	Rev
	ICH7-M HOST (1 OF 4)	C
Date:	Thursday, December 15, 2005	Sheet 14 of 50



Docking
Bluetooth Module
Mini PCI-E
NEW CARD

ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

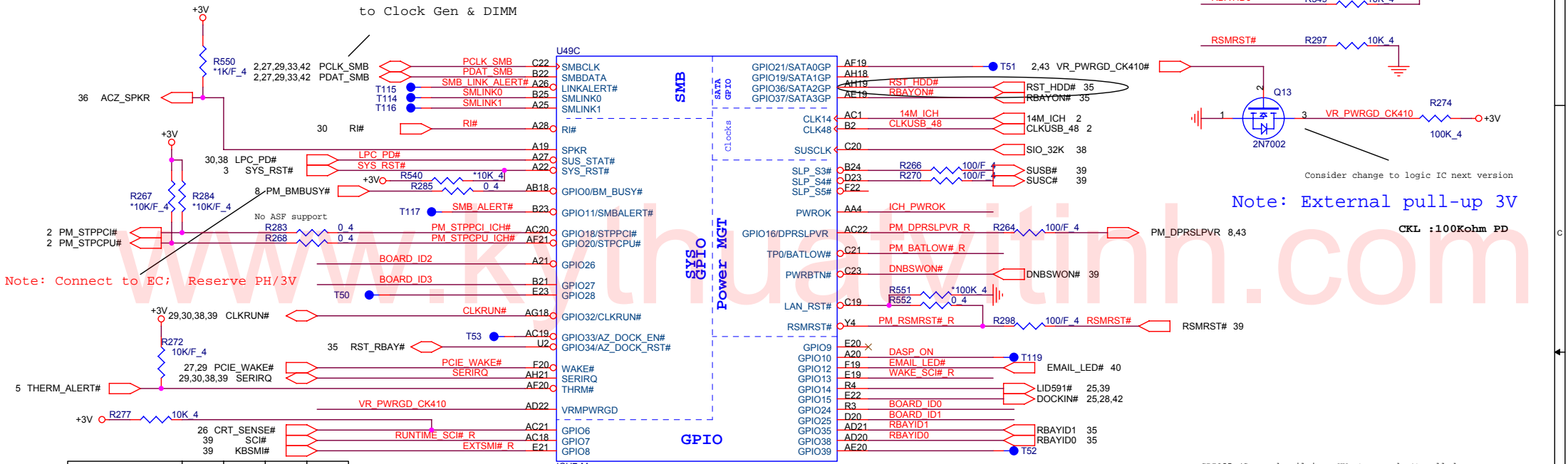
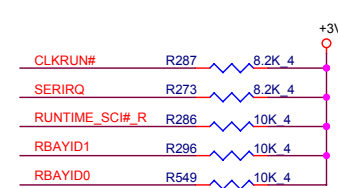
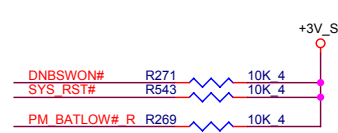
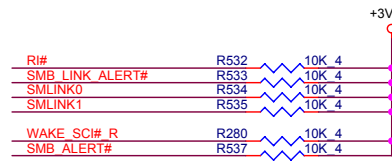
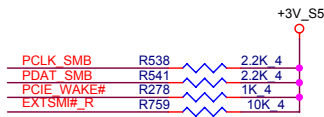


PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	INT E/F/G#
Relleck Lan	AD16	REQ1# / GNT1#	INT B#
MINI PCI	AD19	REQ2# / GNT2#	INT C/D#

PROJECT : ZB1
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Size	Document Number	Rev
	ICH7-M PCI E (2 OF 4)	C
Date:	Thursday, December 15, 2005	Sheet 15 of 50

Don't connect to PCI device / Express card



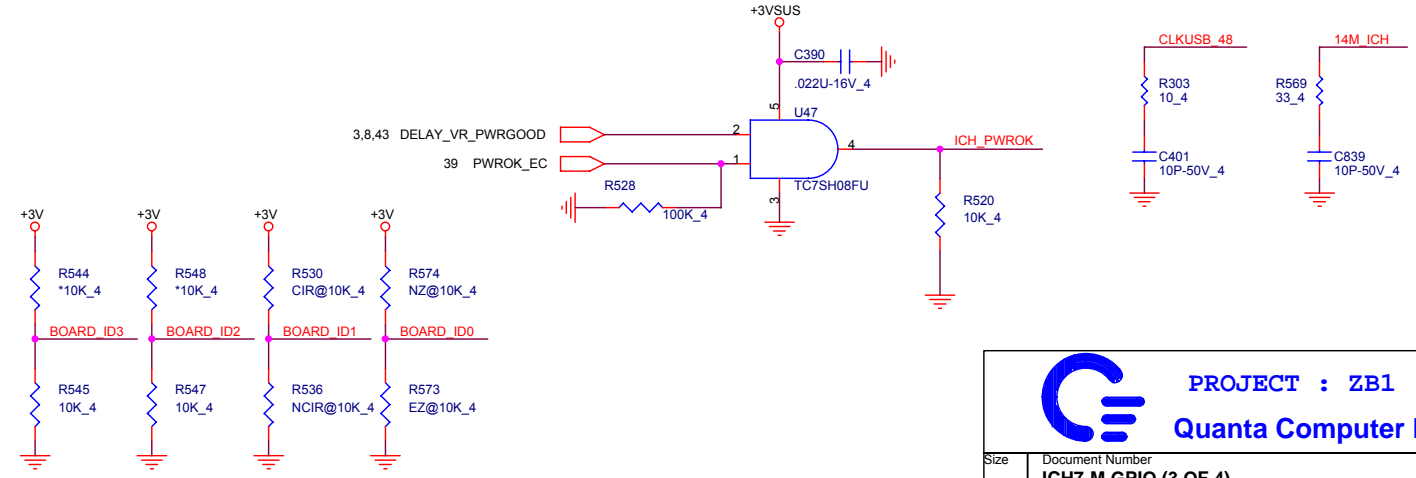
Note: Connect to EC; Reserve PH/3V


Note: External pull-up 3V

Consider change to logic IC next version

GPIO25 /Suspend rail is a HW strap, don't pull down.

Board ID	ID3	ID2	ID1	ID0
With EZ Dock W/O CIR	0	0	0	0
W/O EZ Dock W/O CIR	0	0	0	1
With EZ Dock With CIR	0	0	1	0
W/O EZ Dock With CIR	0	0	1	1
RSV	0	1	0	0

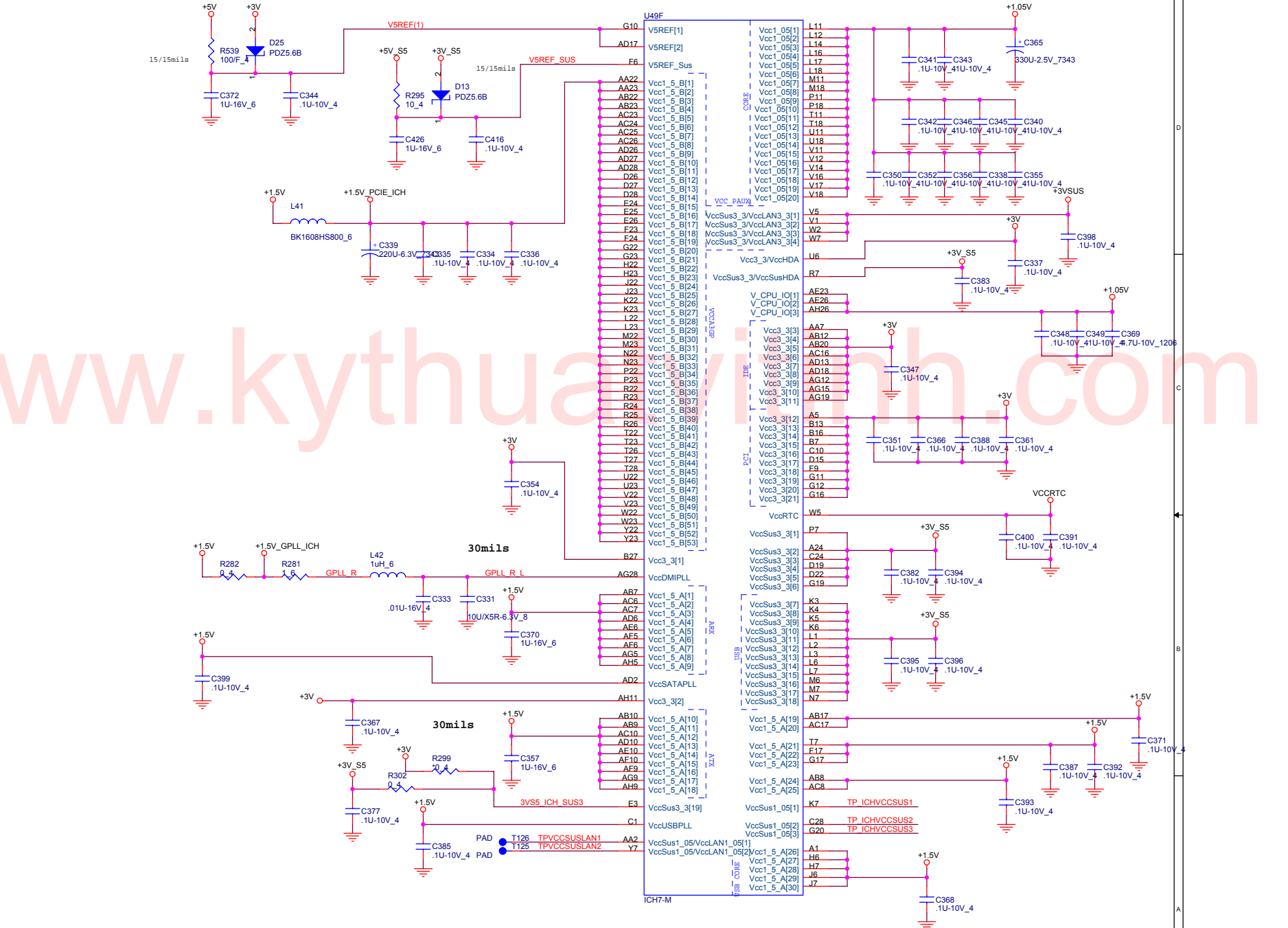




PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO (3 OF 4)	C
Date:	Thursday, December 15, 2005	Sheet
	16	of 50

U49E	VSS1	VSS2	VSS3	VSS4	VSS5	VSS6	VSS7	VSS8	VSS9	VSS10	VSS11	VSS12	VSS13	VSS14	VSS15	VSS16	VSS17	VSS18	VSS19	VSS20	VSS21	VSS22	VSS23	VSS24	VSS25	VSS26	VSS27	VSS28	VSS29	VSS30	VSS31	VSS32	VSS33	VSS34	VSS35	VSS36	VSS37	VSS38	VSS39	VSS40	VSS41	VSS42	VSS43	VSS44	VSS45	VSS46	VSS47	VSS48	VSS49	VSS50	VSS51	VSS52	VSS53	VSS54	VSS55	VSS56	VSS57	VSS58	VSS59	VSS60	VSS61	VSS62	VSS63	VSS64	VSS65	VSS66	VSS67	VSS68	VSS69	VSS70	VSS71	VSS72	VSS73	VSS74	VSS75	VSS76	VSS77	VSS78	VSS79	VSS80	VSS81	VSS82	VSS83	VSS84	VSS85	VSS86	VSS87	VSS88	VSS89	VSS90	VSS91	VSS92	VSS93	VSS94	VSS95	VSS96	VSS97
P28	VSS98	VSS99	VSS100	VSS101	VSS102	VSS103	VSS104	VSS105	VSS106	VSS107	VSS108	VSS109	VSS110	VSS111	VSS112	VSS113	VSS114	VSS115	VSS116	VSS117	VSS118	VSS119	VSS120	VSS121	VSS122	VSS123	VSS124	VSS125	VSS126	VSS127	VSS128	VSS129	VSS130	VSS131	VSS132	VSS133	VSS134	VSS135	VSS136	VSS137	VSS138	VSS139	VSS140	VSS141	VSS142	VSS143	VSS144	VSS145	VSS146	VSS147	VSS148	VSS149	VSS150	VSS151	VSS152	VSS153	VSS154	VSS155	VSS156	VSS157	VSS158	VSS159	VSS160	VSS161	VSS162	VSS163	VSS164	VSS165	VSS166	VSS167	VSS168	VSS169	VSS170	VSS171	VSS172	VSS173	VSS174	VSS175	VSS176	VSS177	VSS178	VSS179	VSS180	VSS181	VSS182	VSS183	VSS184	VSS185	VSS186	VSS187	VSS188	VSS189	VSS190	VSS191	VSS192	VSS193	VSS194

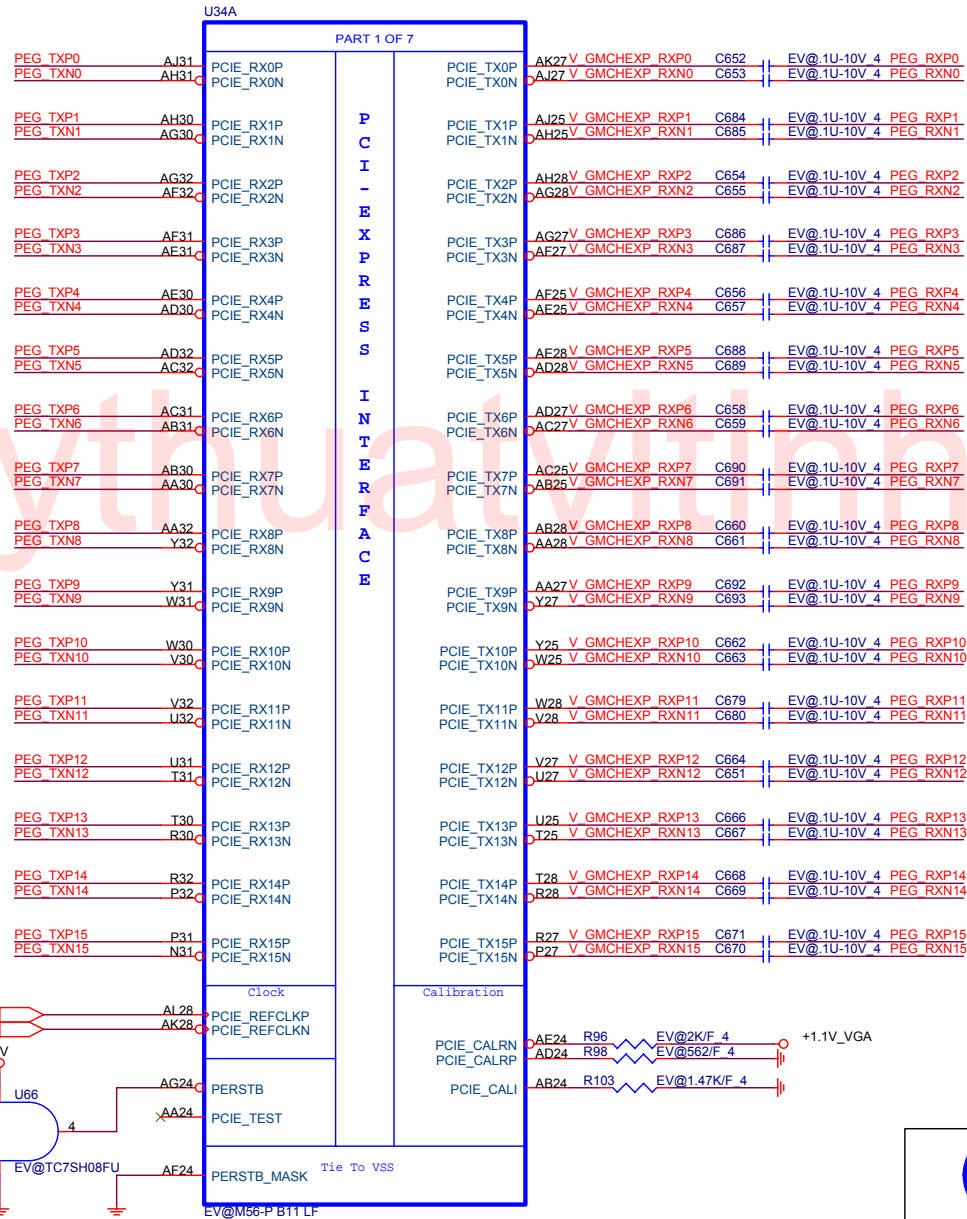
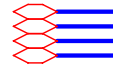


PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M POWER (4 OF 4)	C
Date:	Thursday, December 15, 2005	Sheet 17 of 50

NOTE: some of the PCIe testpoints will be available through via on traces.

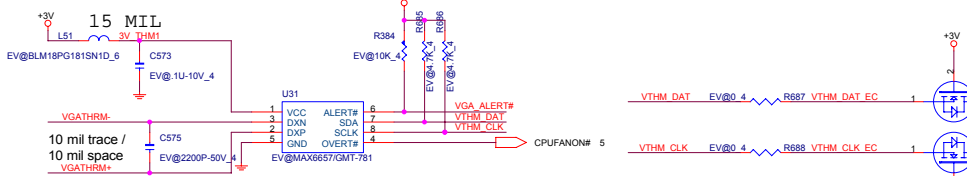
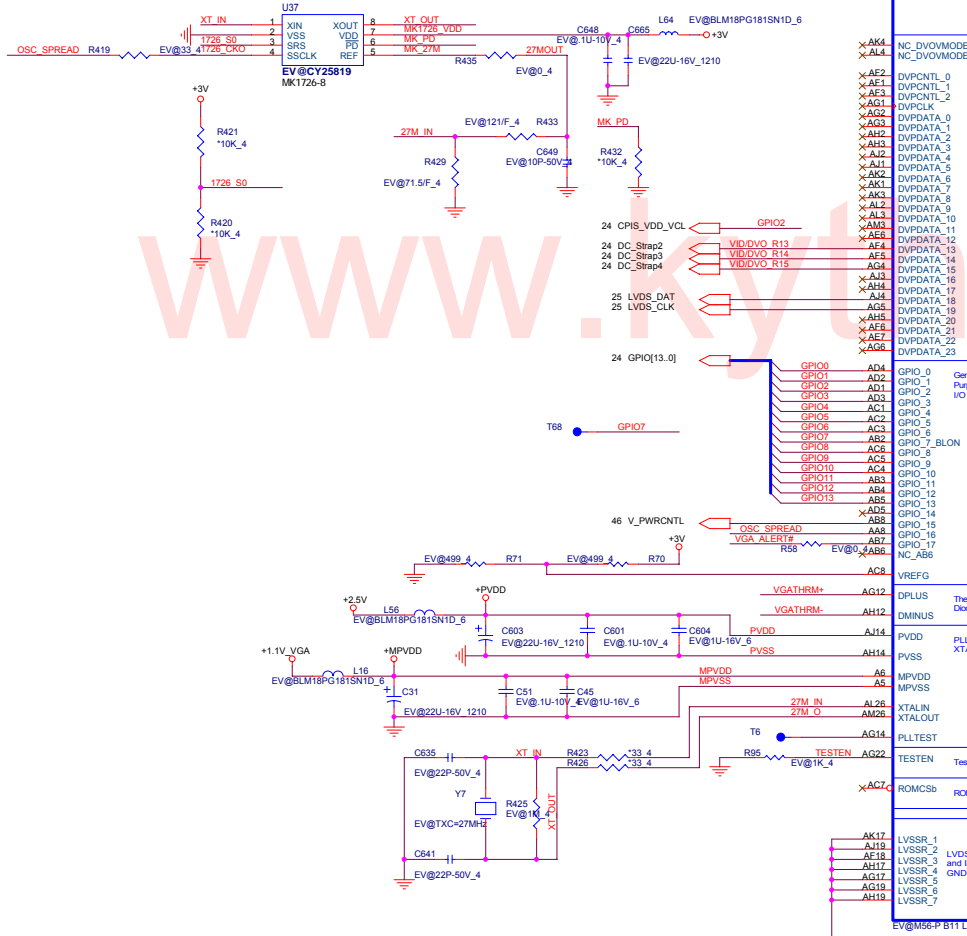
8,41 PEG_RXP[15:0]
 8,41 PEG_RXN[15:0]
 8,41 PEG_TXP[15:0]
 8,41 PEG_TXN[15:0]



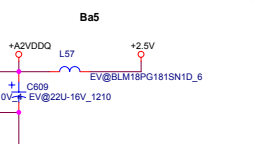
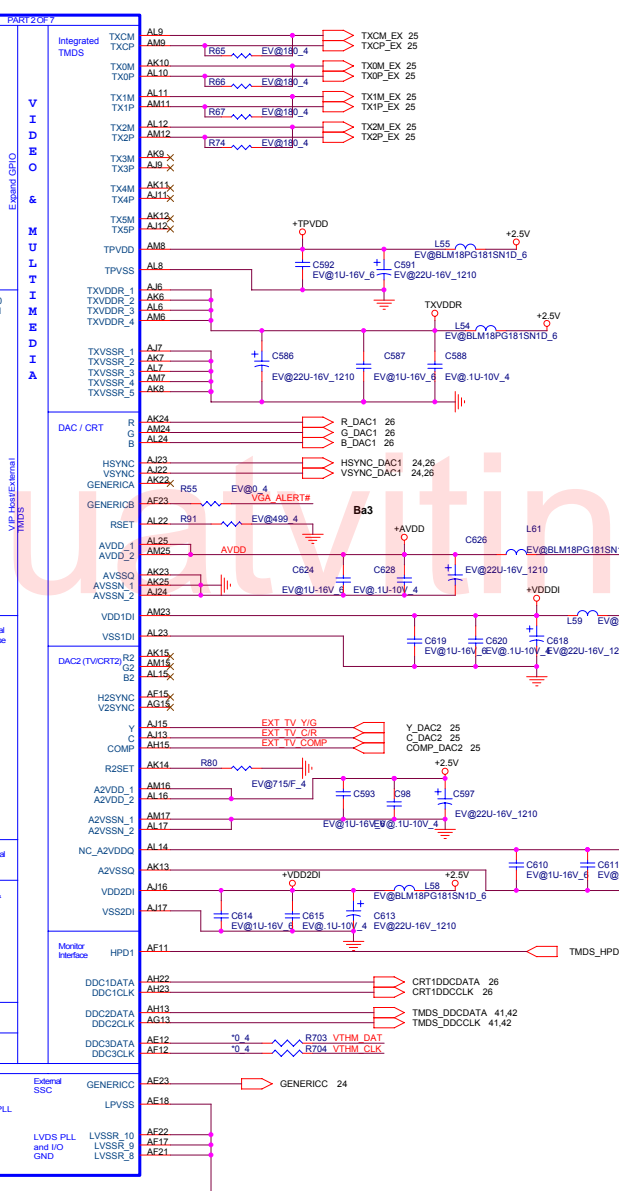
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	M56P 1 OF 7	C
Date:	Thursday, December 15, 2005	Sheet 18 of 50

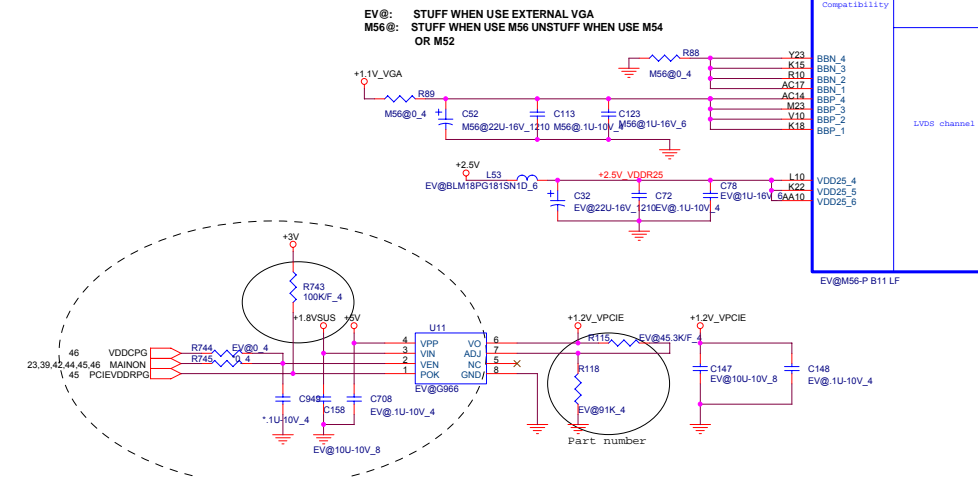
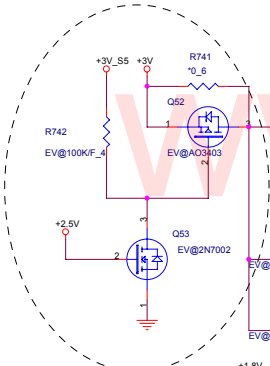
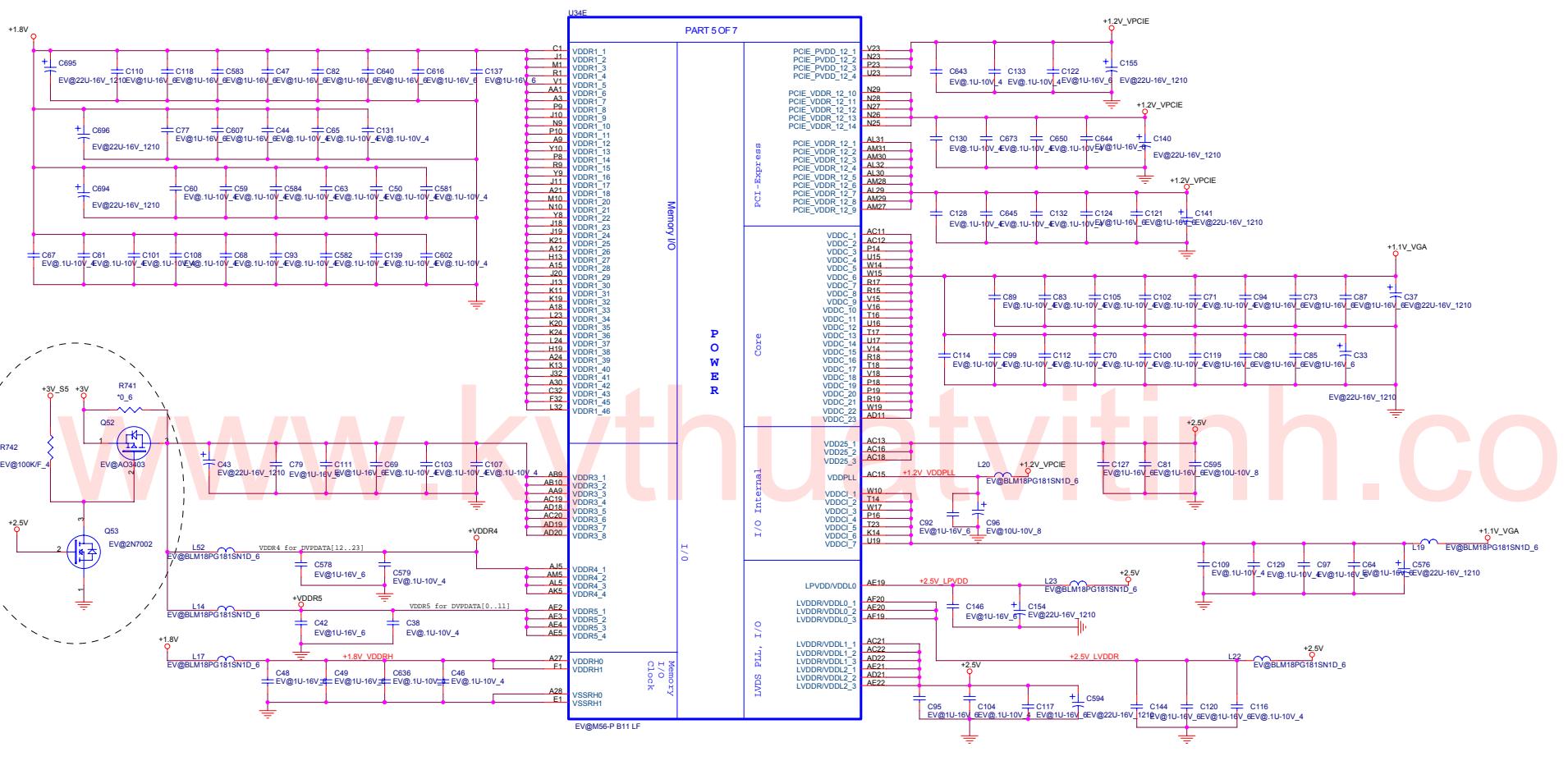
MEMORY CLOCK SPREAD SPECTRUM



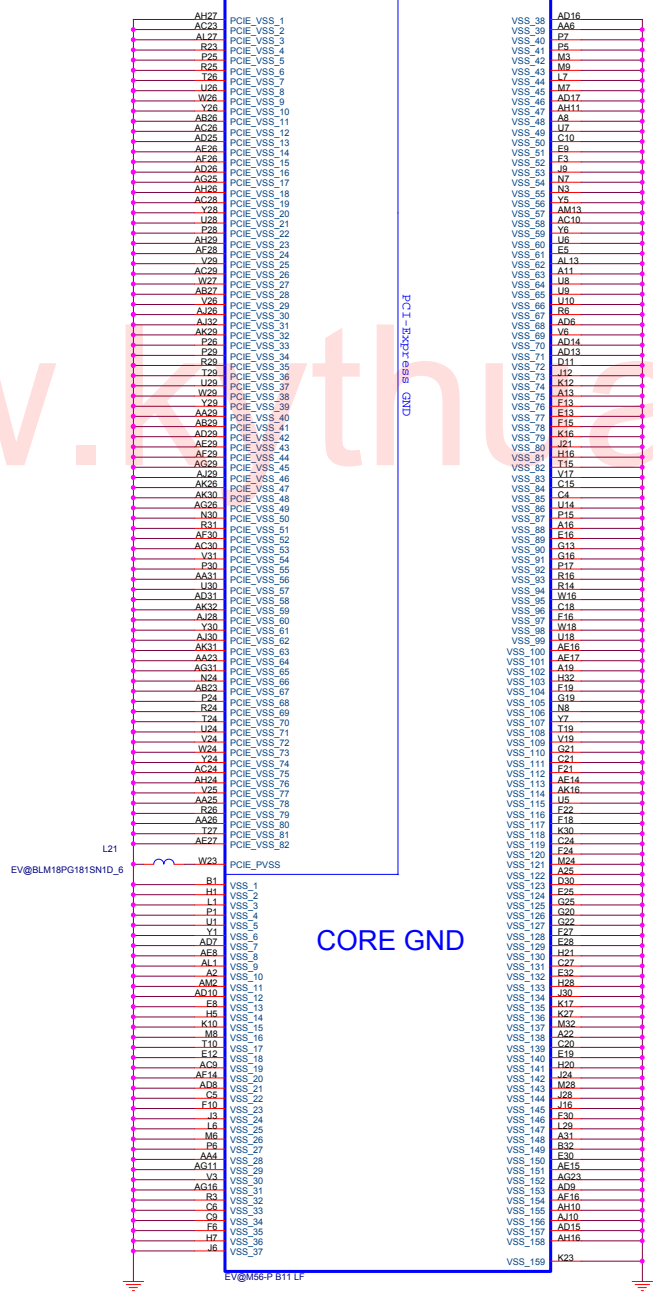
Close to pin ASIC SLAVE ADDRESS: 9A



PROJECT : ZB1
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U34F Part 6 of 7



www.threatvith.com

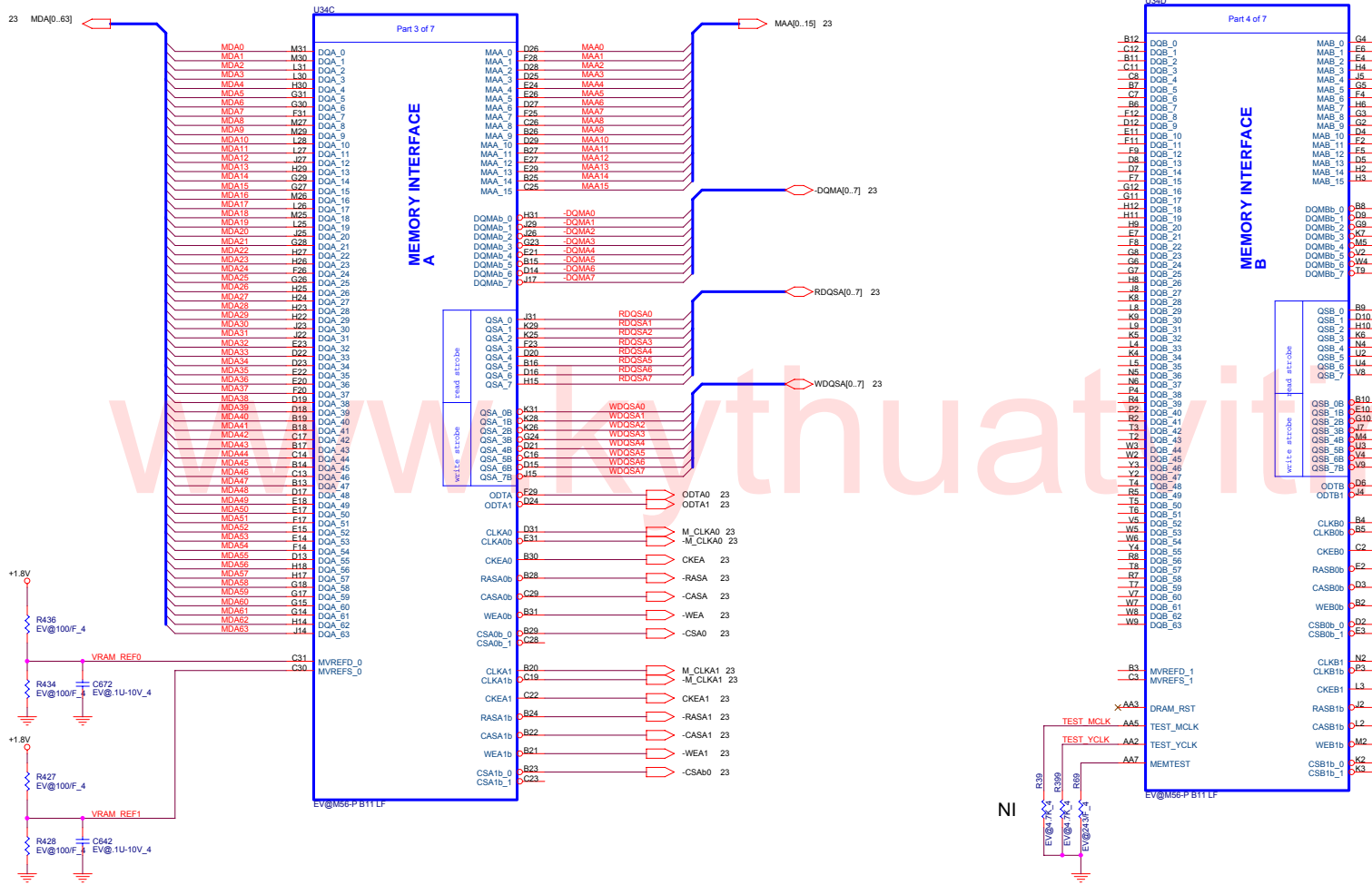
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
M56P 6 OF 7		C
Date	Thursday, December 15, 2005	Sheet 21 of 50

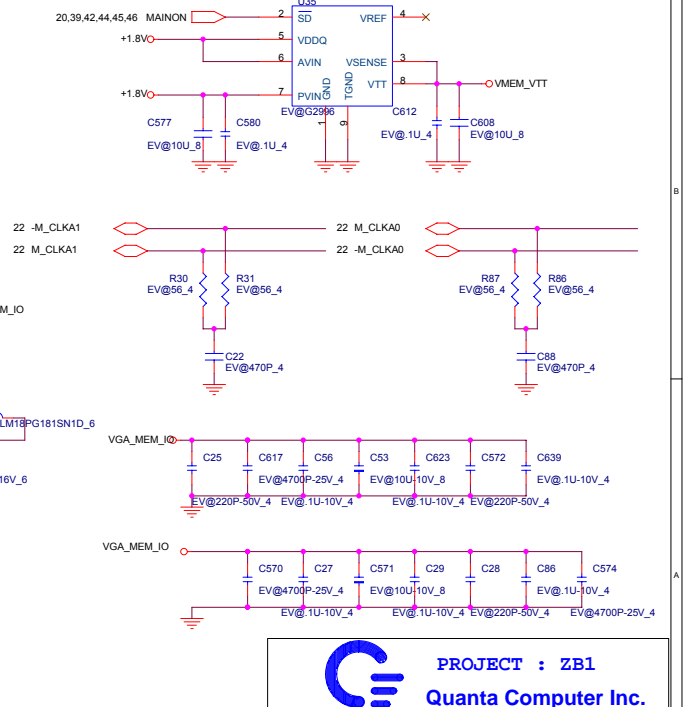
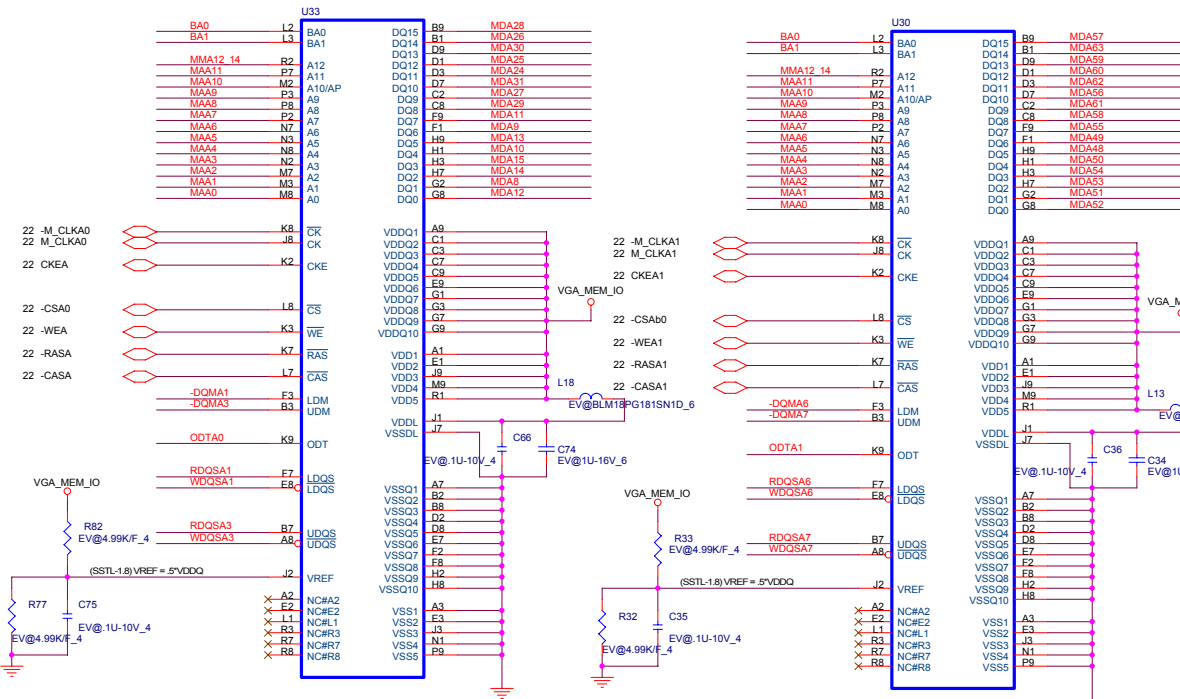
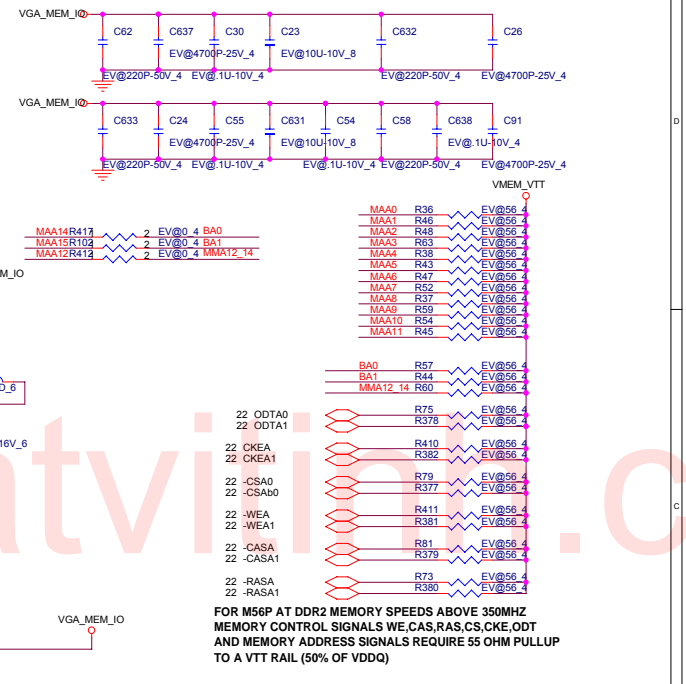
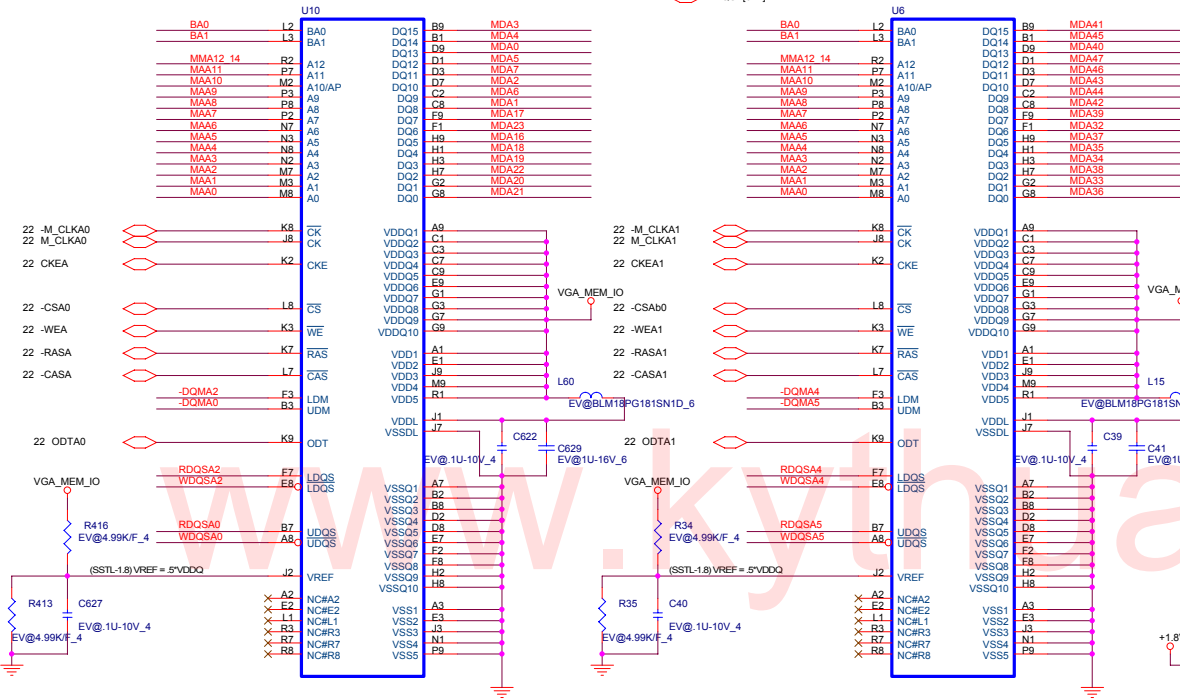
RV410 MEMORY CHANNELS A and B

Channel A

Channel B



CHAN A DDR2 84BGA 16MX16 MEMORY



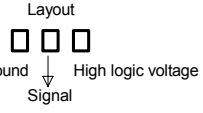
FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE.CAS.RAS.CS.CKE.ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)

PROJECT : ZB1
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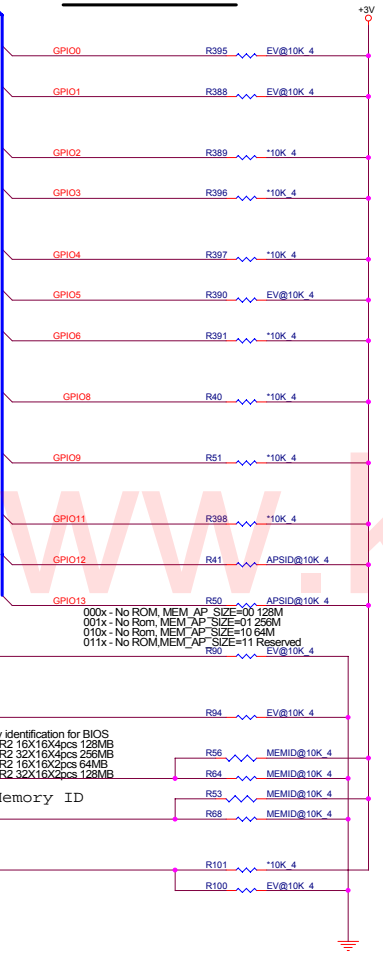
Size	Document Number	Rev
	VRAM DDR2	C
Date:	Thursday, December 15, 2005	Sheet 23 of 50

OPTION STRAPS

Overlap pads to save space and to prevent assembly of both resistors.



Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.



Memory identification for BIOS
 00 - DDR2 16X16X4pcs 128MB
 01 - DDR2 32X16X4pcs 256MB
 10 - DDR2 16X16X2pcs 64MB
 11 - DDR2 32X16X2pcs 128MB

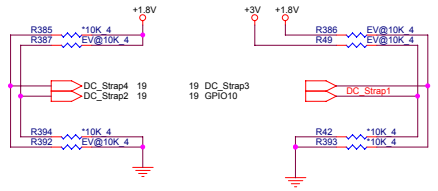
Memory ID

M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWR5_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	1
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDs from ROM 1011 - Serial M25P10 ROM (ST), chip IDs from ROM 1100 - Serial M25P05 ROM (ST), chip IDs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDs from ROM	000
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port devices present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GBNER ICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

Board Straps REV. 0.3

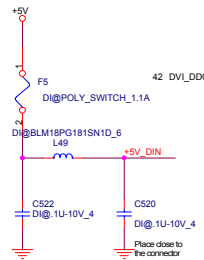
STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PALNTSC	LCDDATA(18)	TV0 Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1



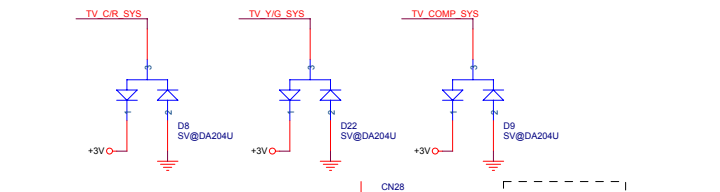
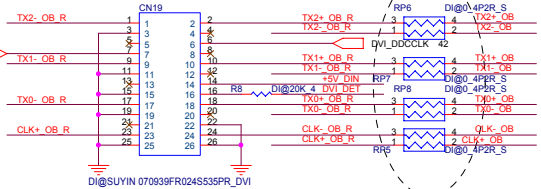
PROJECT : ZB1
Quanta Computer Inc.

Size: Document Number: M56P OPTION STRAPS Rev: C
 Date: Thursday, December 15, 2005 Sheet: 24 of 50

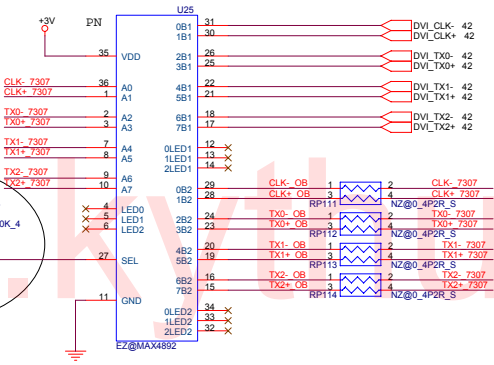
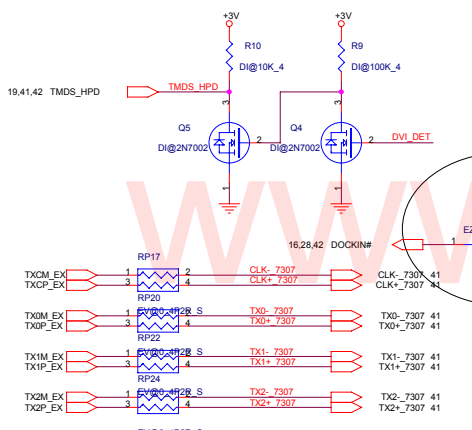
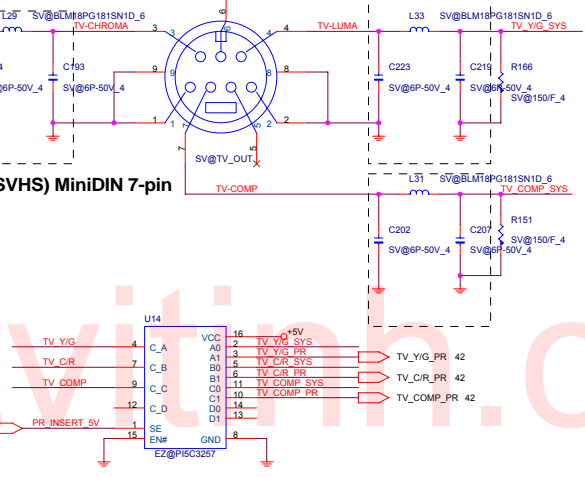
DVI-H CONNECTOR (DVI-D)



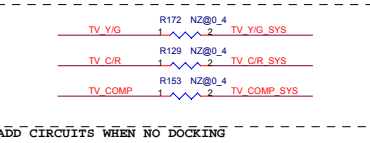
DVI PORT



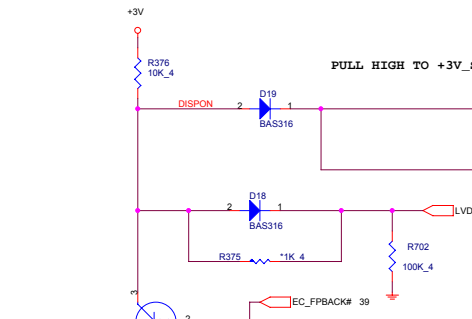
TV Out (SVHS) MiniDIN 7-pin



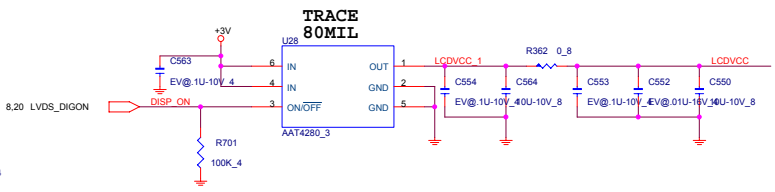
SEL	FUN
H	B2
L	B1



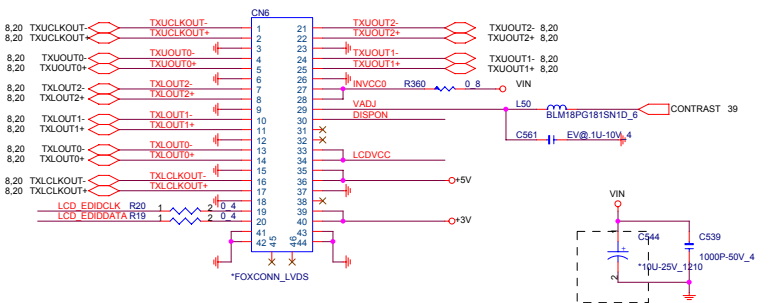
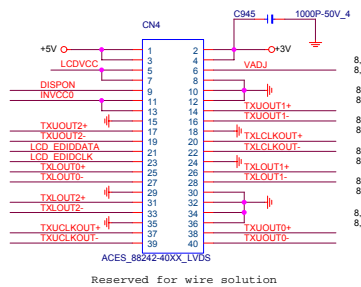
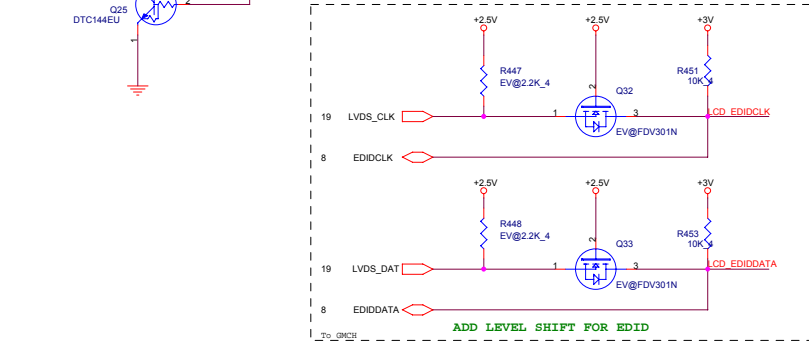
- 8 INT_TV_YIG R165 IV@0.4 TV_YIG
- 8 INT_TV_CIR R132 IV@0.4 TV_CIR
- 8 INT_TV_COMP R147 IV@0.4 TV_COMP
- 19 Y_DAC2 R171 EV@0.4 TV_YIG
- 19 C_DAC2 R128 EV@0.4 TV_CIR
- 19 COMP_DAC2 R148 EV@0.4 TV_COMP



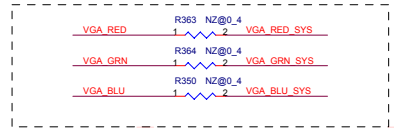
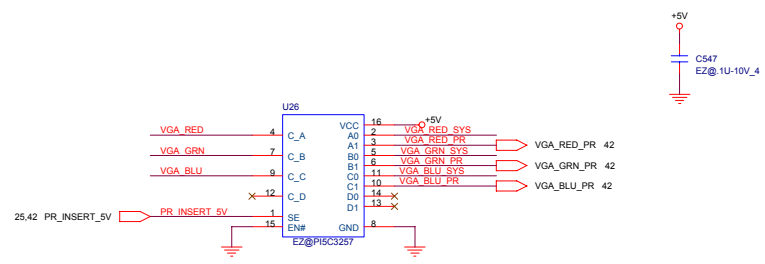
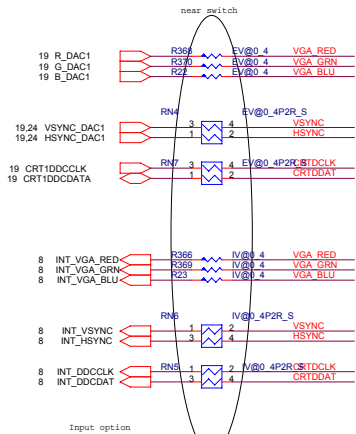
Lid Switch



TRACE 80MIL

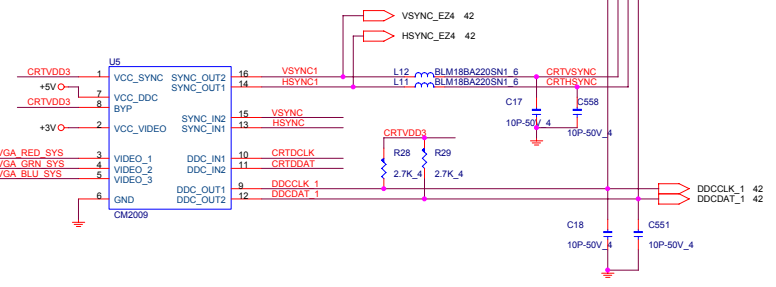
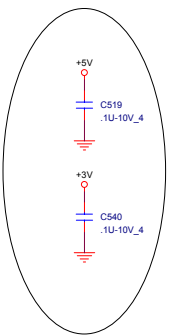
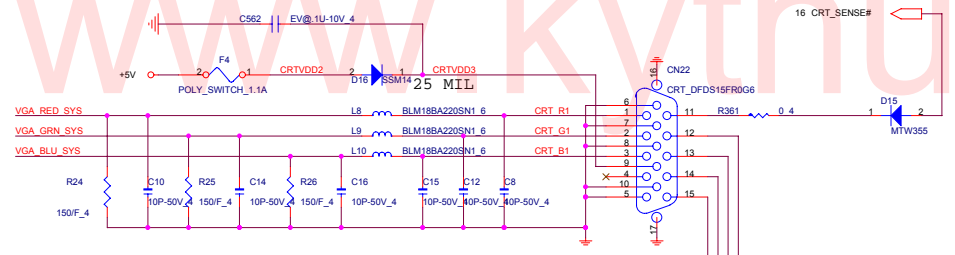


PROJECT : ZB1
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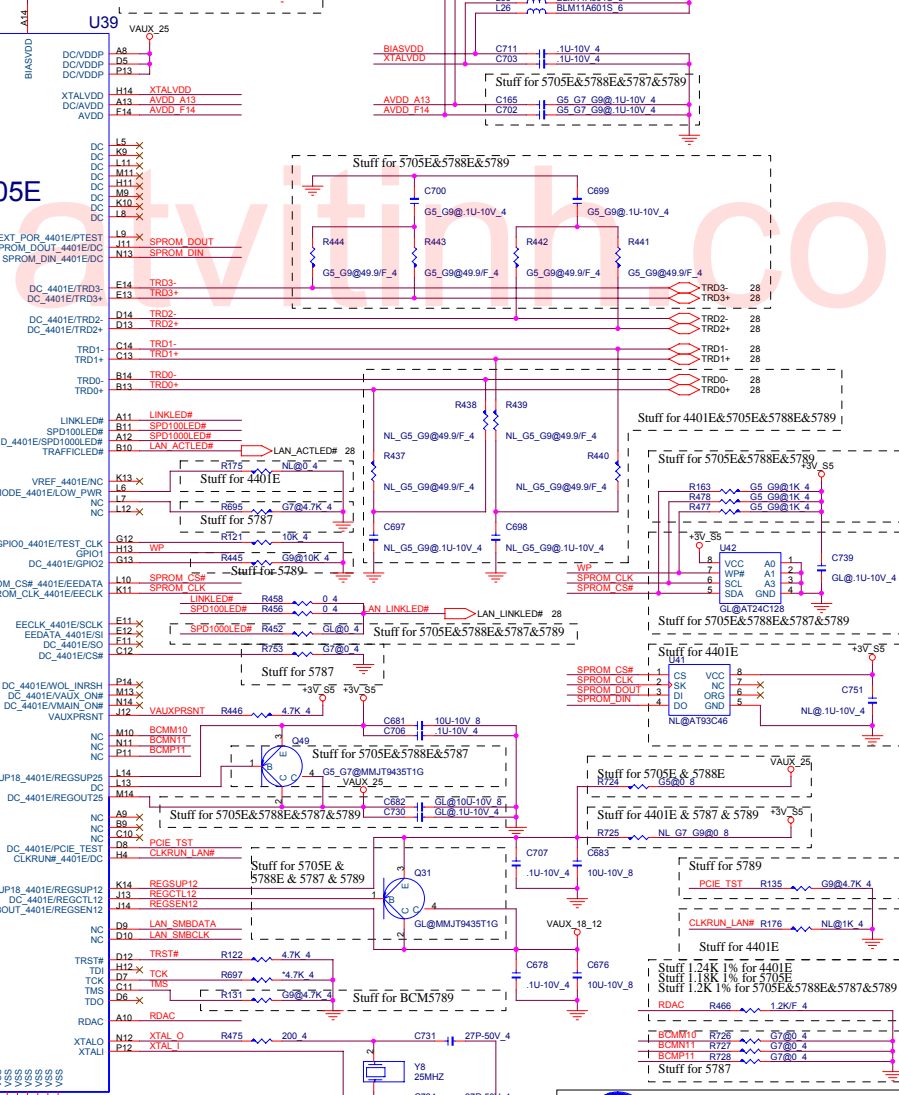
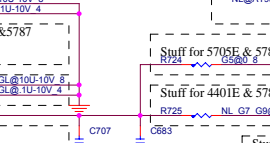
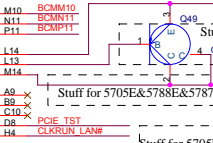
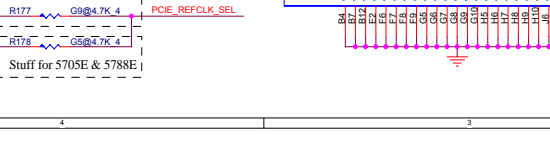
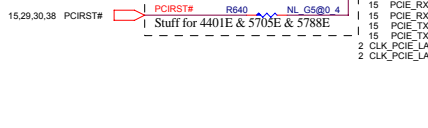
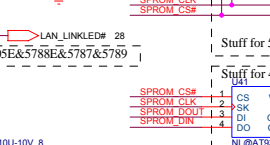
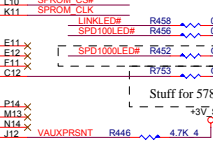
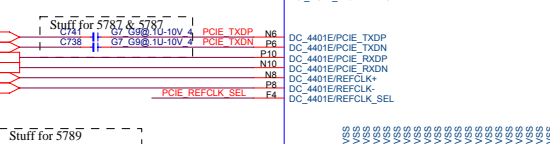
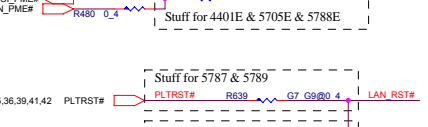
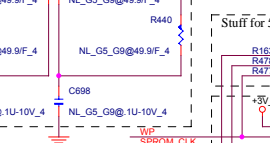
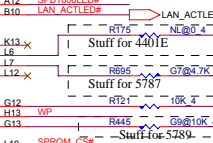
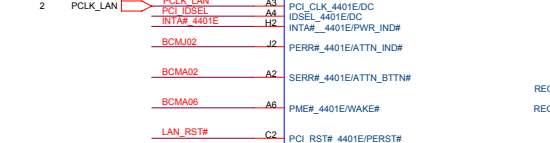
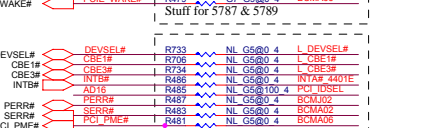
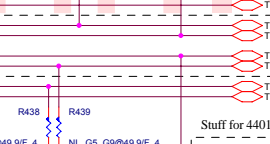
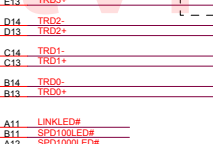
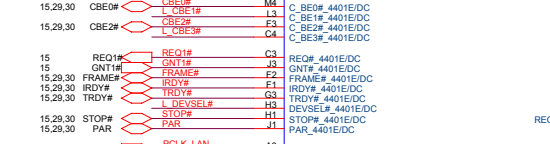
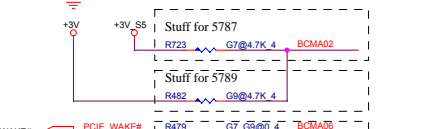
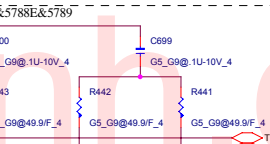
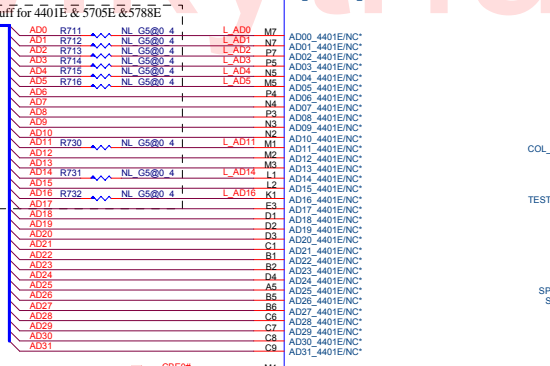
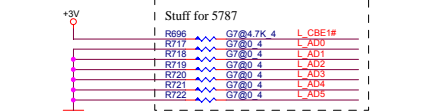
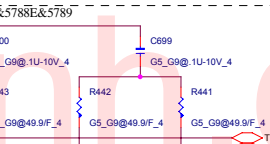
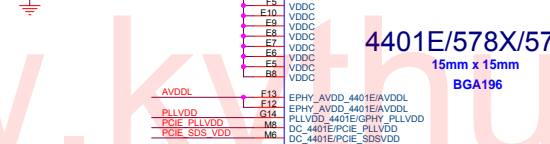
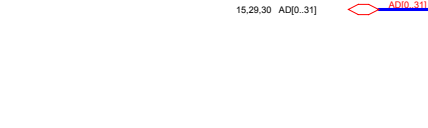
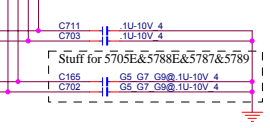
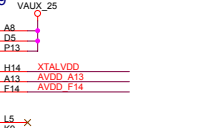
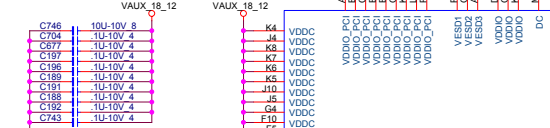
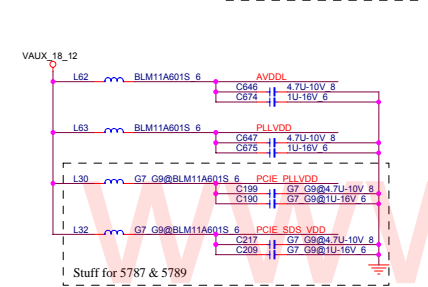
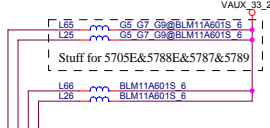
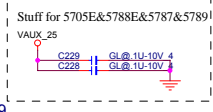
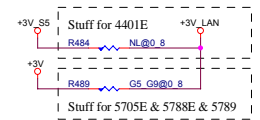
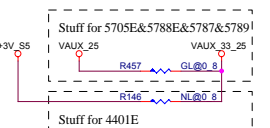
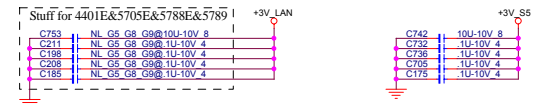
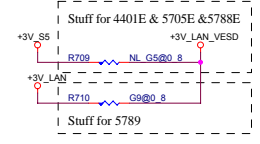


SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

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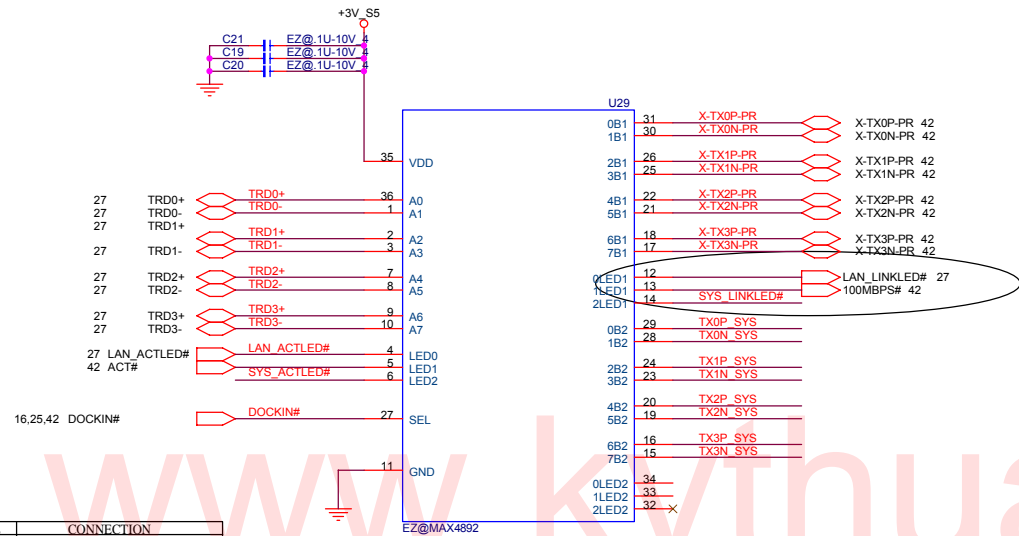


NL@ 4401E
 G5@ 5705E&5788E
 G7@ 5787
 G9@ 5789
 GL@ 5705E&5788E&5787&5789

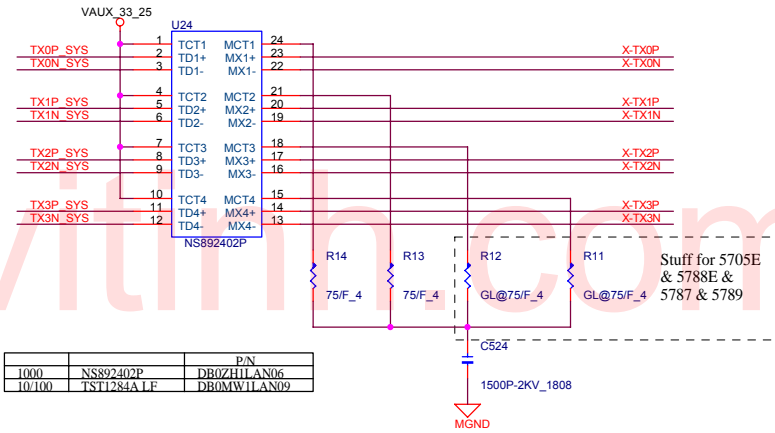
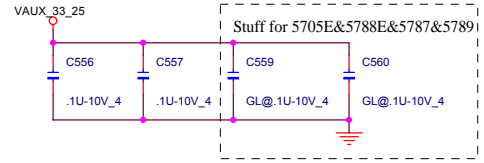


INTERFACE	4401E	5789	5787	5705E
P/N	A0H400T01	A05789T010	A05787T010	A05705T013

PROJECT : ZB1
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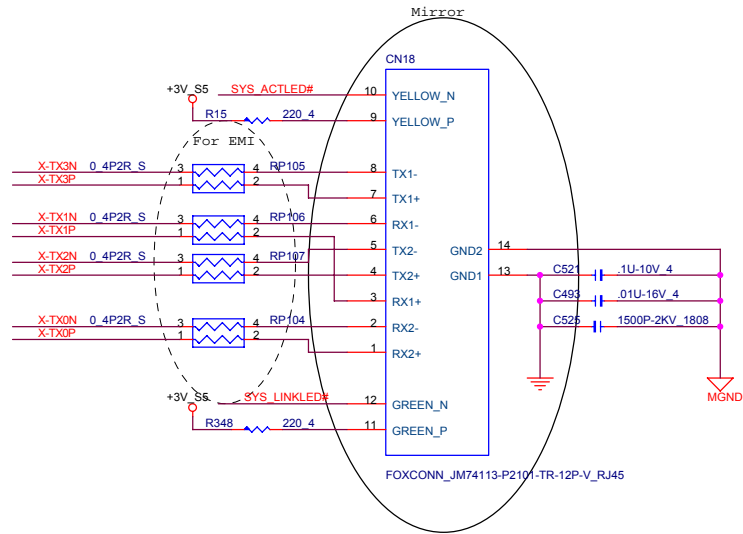
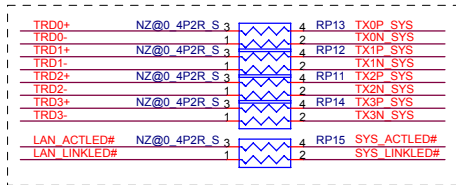


SEL	CONNECTION
0	Ax to xB1 : LEDx to xLED1
1	Ax to xB2 : LEDx to xLED2

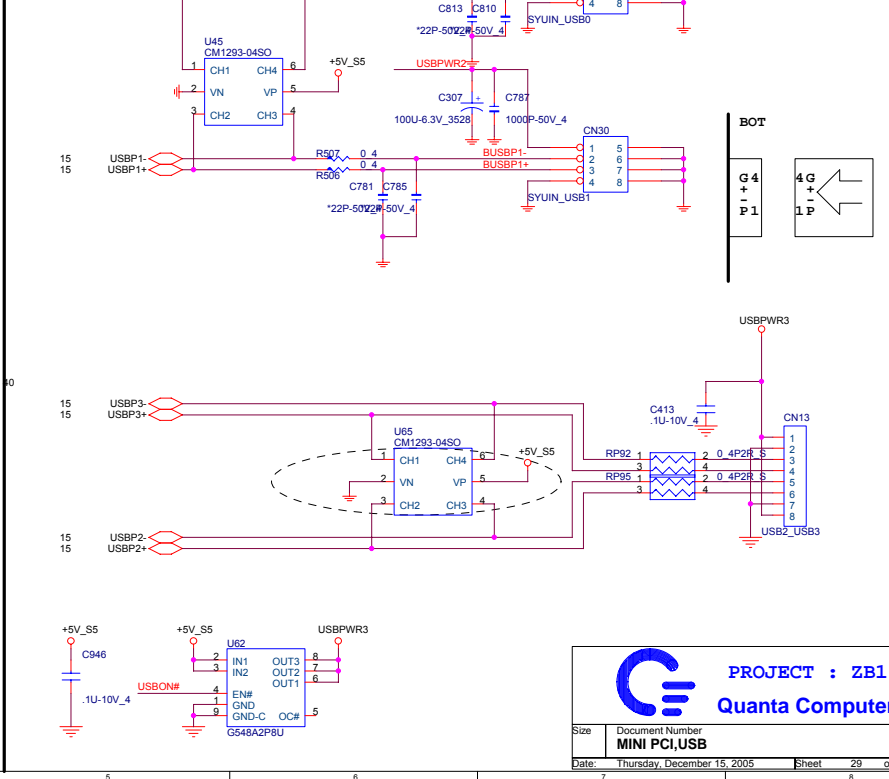
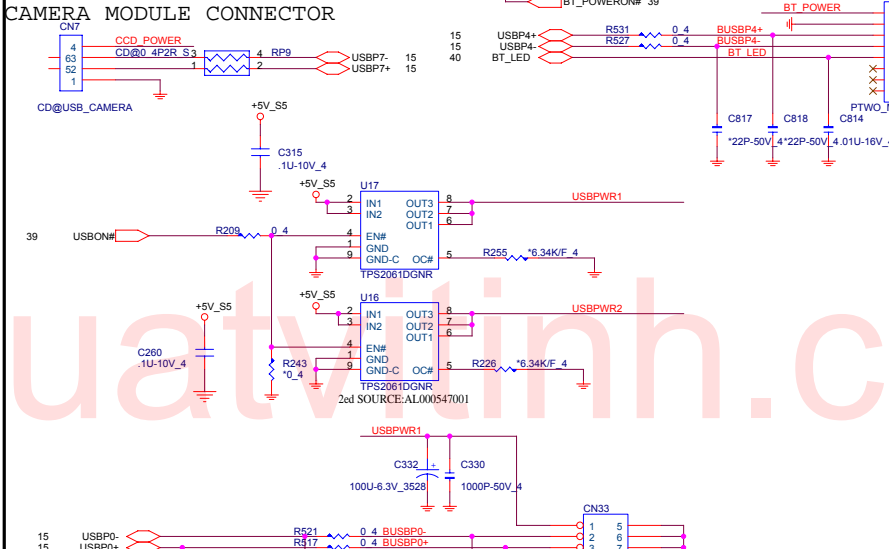
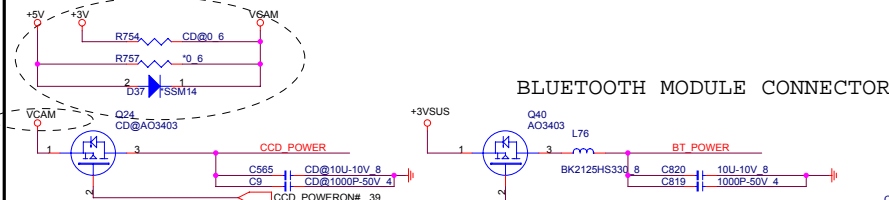
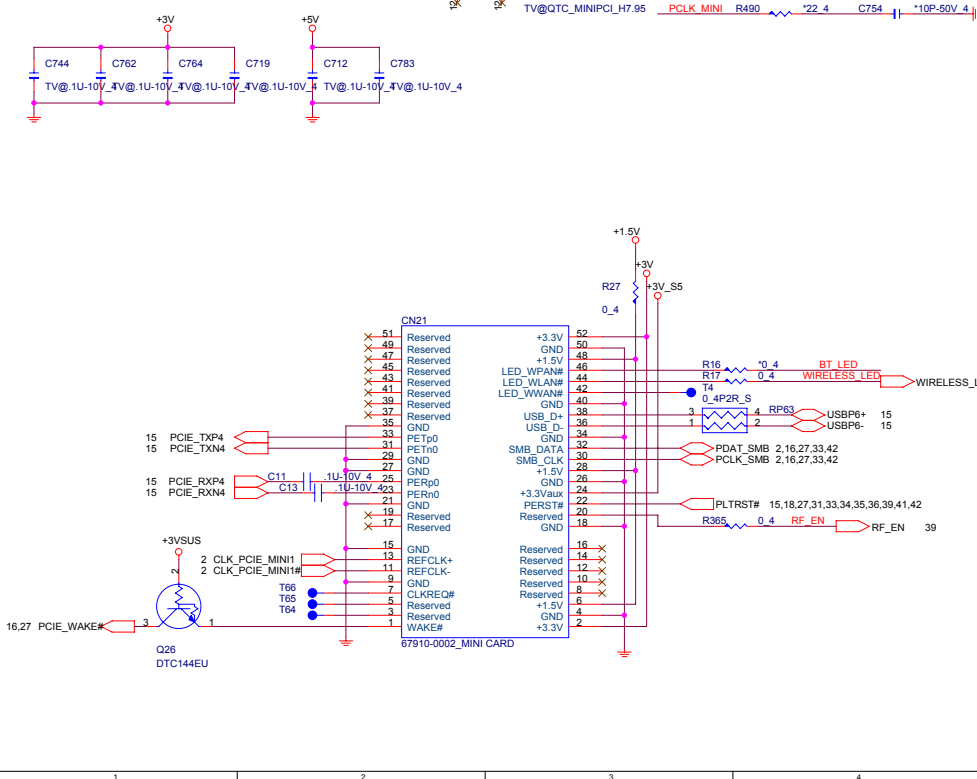
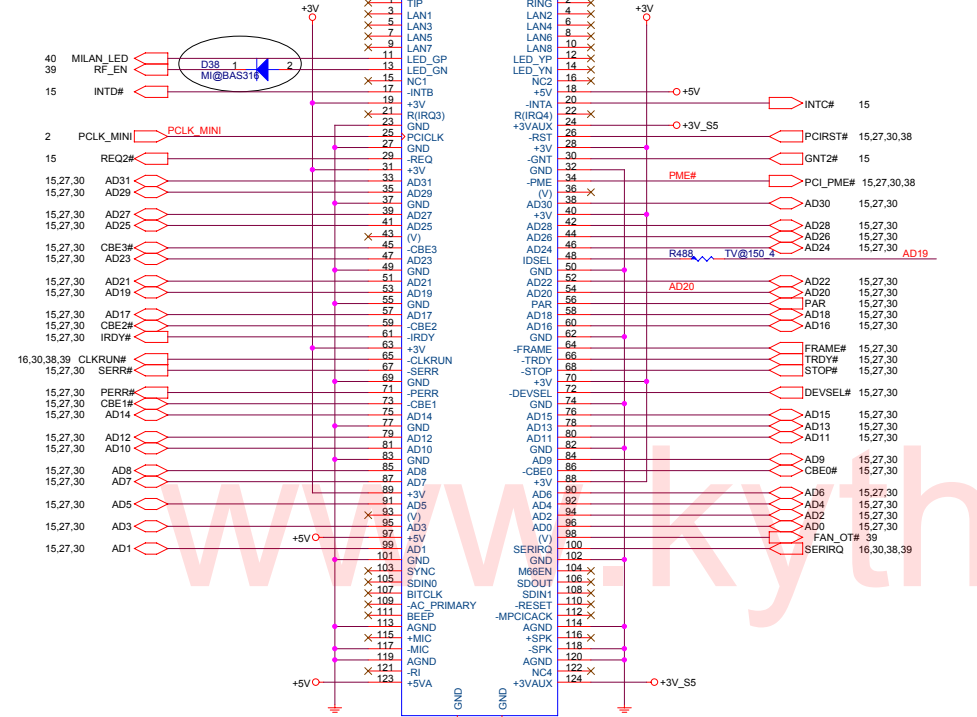


	P/N
1000	NS892402P DB0ZHLAN06
10/100	TST1284A LF DB0MW1LAN09

ADD CIRCUITS WHEN NO DOCKING

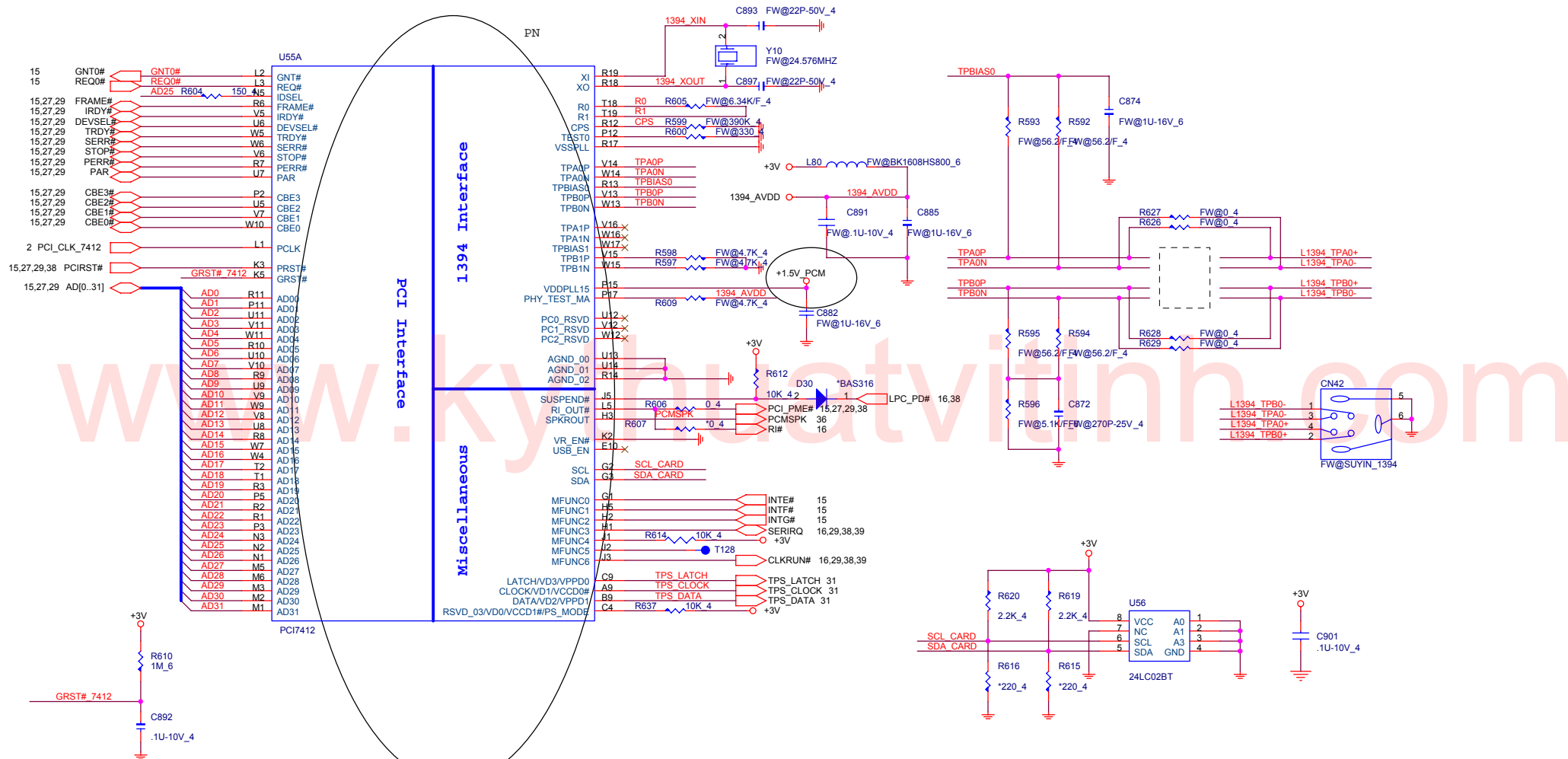


MINI-PCI



PROJECT : ZB1
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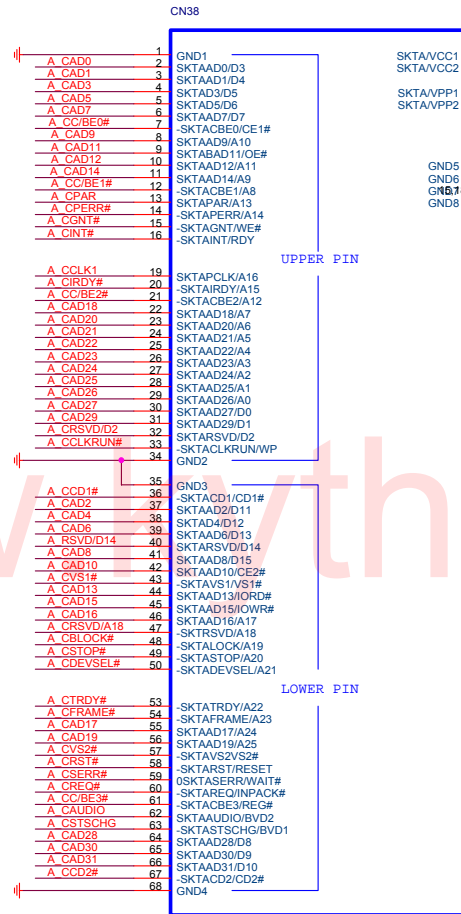
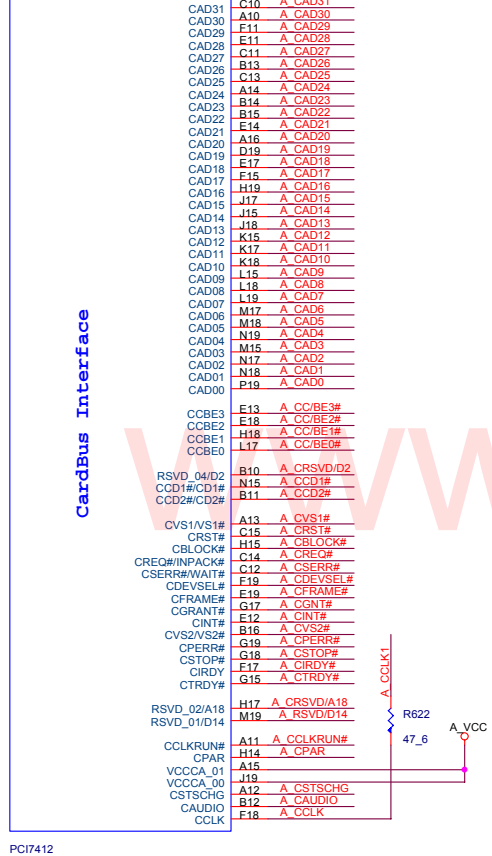
Size	Document Number	Rev
	MINI PCI, USB	C
Date:	Thursday, December 15, 2005	Sheet 29 of 50



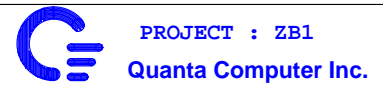
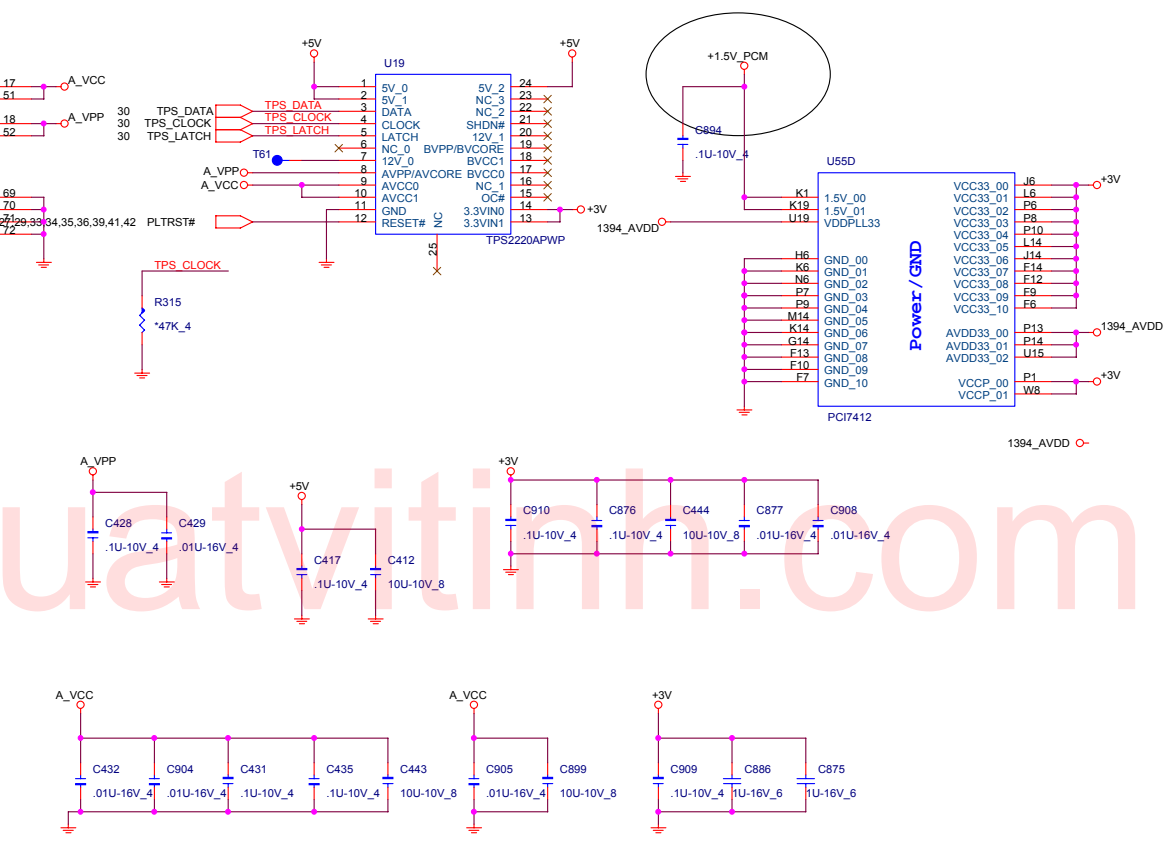
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U55B

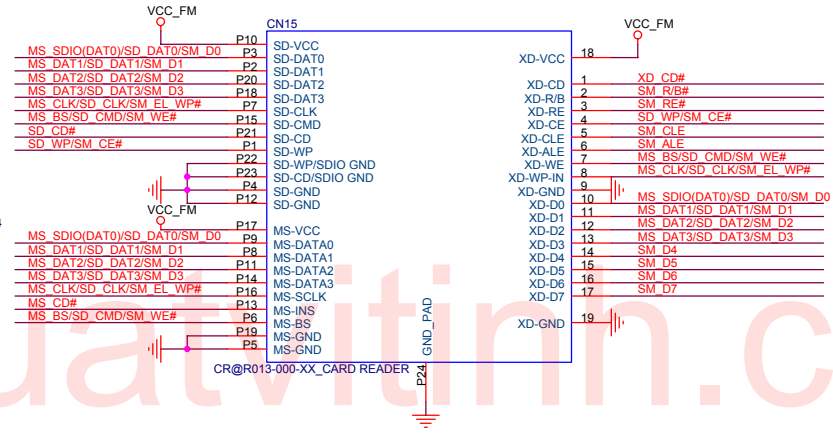
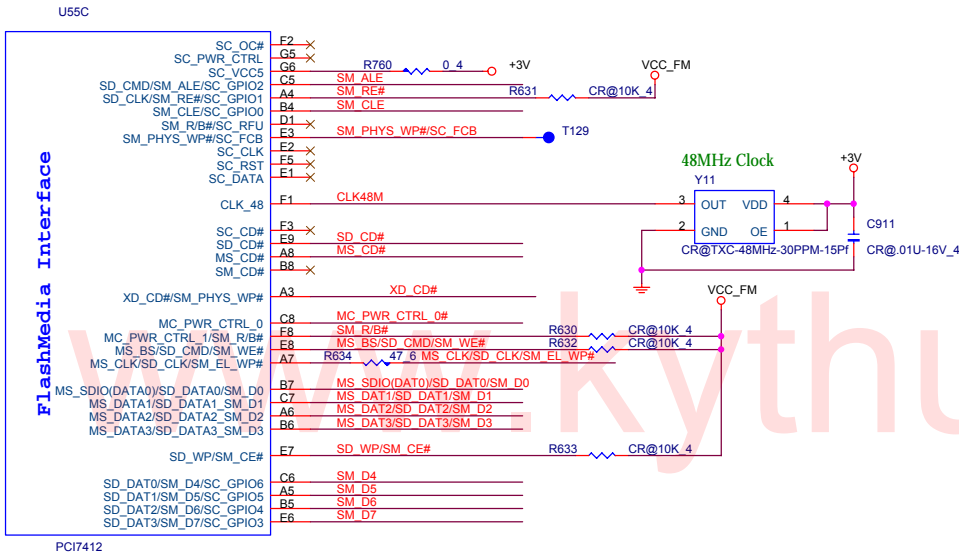
CardBus Interface



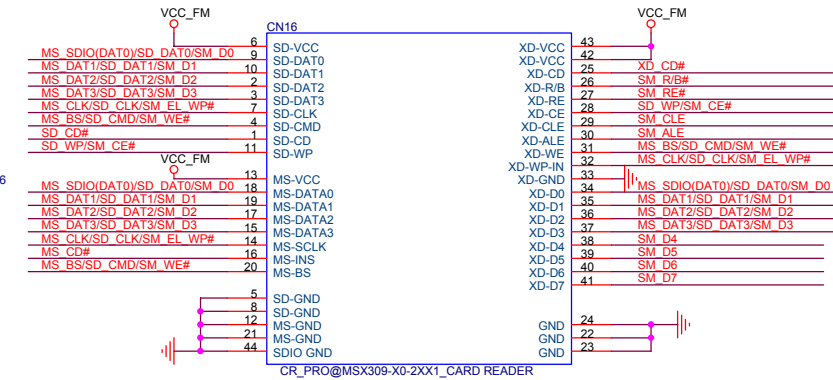
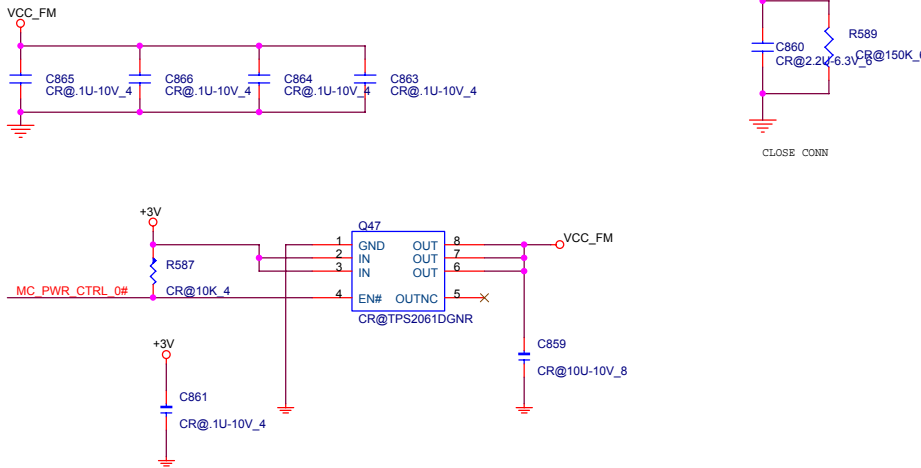
CARDBUS SLOT
FOX_1CA4CSG2-TC_CARD BUS

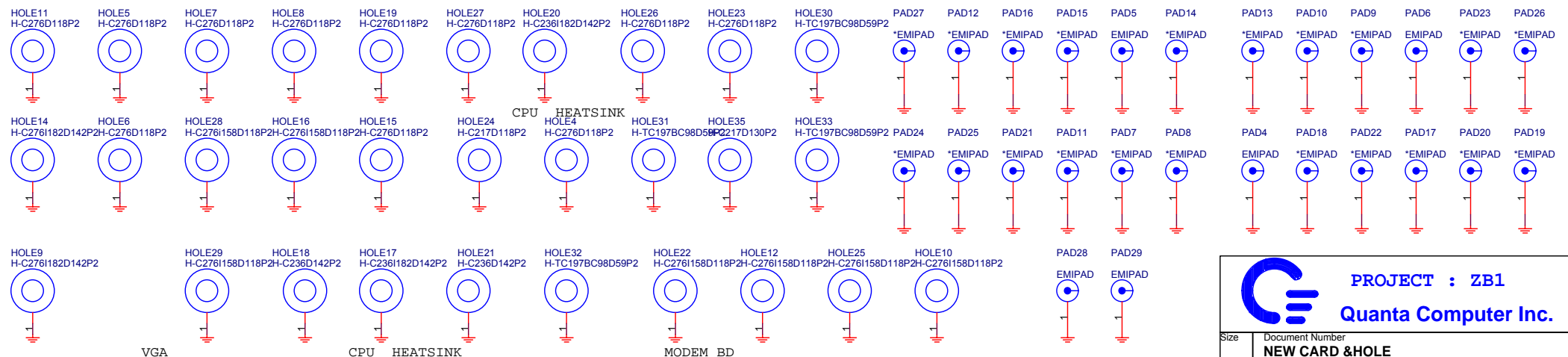
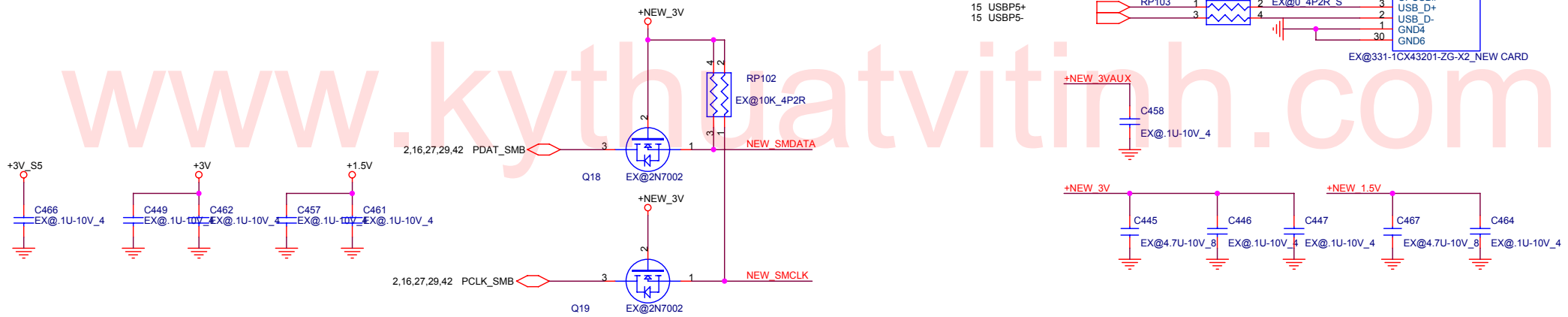
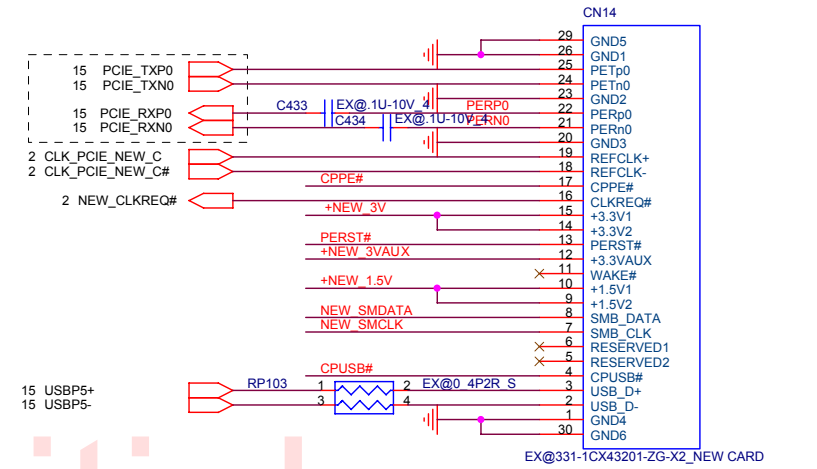
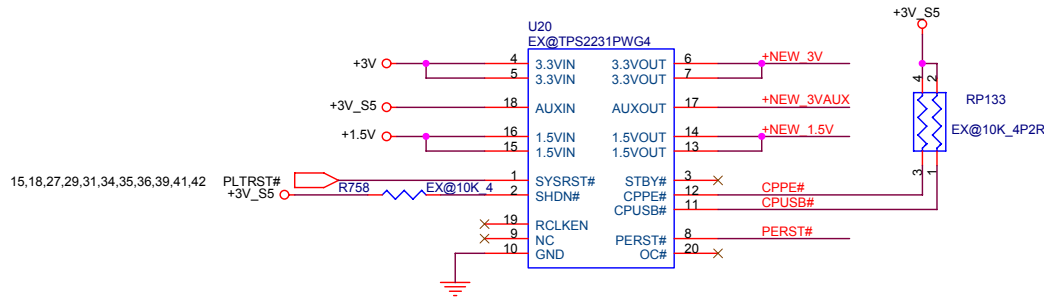


DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.



5 IN1 CARD READER



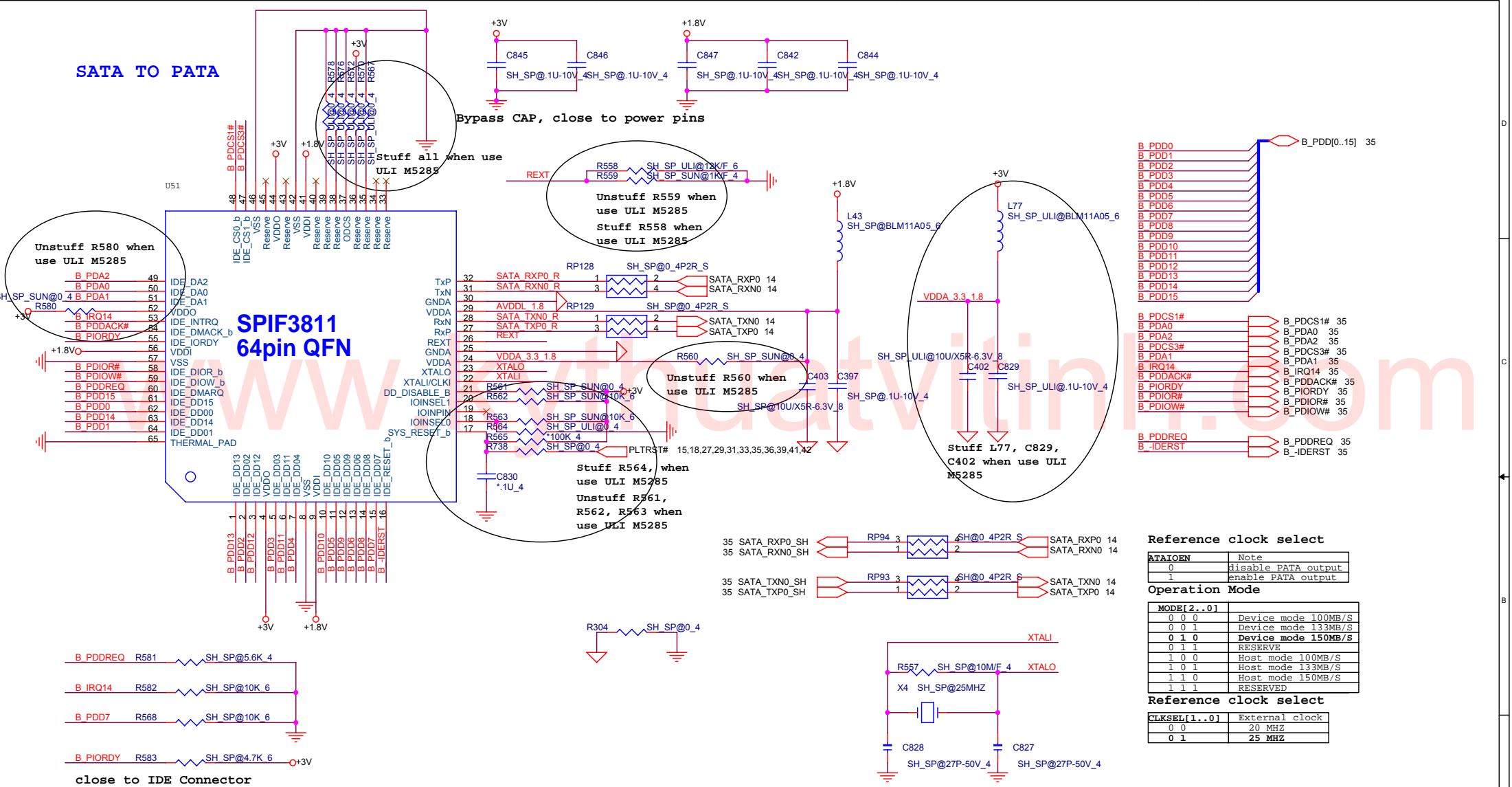


PROJECT : ZB1
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Size Document Number
NEW CARD & HOLE Rev C

Date: Thursday, December 15, 2005 Sheet 33 of 50

SATA TO PATA



Unstuff R580 when use ULI M5285

Bypass CAP, close to power pins

Unstuff R559 when use ULI M5285
Stuff R558 when use ULI M5285

Unstuff R560 when use ULI M5285

Stuff R564, when use ULI M5285
Unstuff R561, R562, R563 when use ULI M5285

Stuff L77, C829, C402 when use ULI M5285

Unstuff R580 when use ULI M5285

- B_PDA2 49
- B_PDA0 50
- B_PDA1 51
- B_IRQ14 52
- B_PDDACK# 53
- B_PIORDY 54
- B_PDIOR# 57
- B_PDIOW# 58
- B_PDDREQ 59
- B_PDD15 60
- B_PDD0 61
- B_PDD14 62
- B_PDD1 63
- B_PDD13 64
- B_PDD2 65

- IDE_DA2
- IDE_DA0
- IDE_DA1
- VDDO
- IDE_INTRQ
- IDE_DMACK_b
- IDE_IORDY
- VDDI
- VSS
- IDE_DIOR_b
- IDE_DIOW_b
- IDE_DMARQ
- IDE_DD15
- IDE_DD00
- IDE_DD14
- IDE_DD01
- THERMAL_PAD

- B_PDD13
- B_PDD2
- B_PDD12
- B_PDD3
- B_PDD11
- B_PDD4
- B_PDD10
- B_PDD5
- B_PDD6
- B_PDD8
- B_PDD9
- B_PDD7
- B_PDD14
- B_PDD1

close to IDE Connector

- B_PDD0
- B_PDD1
- B_PDD2
- B_PDD3
- B_PDD4
- B_PDD5
- B_PDD6
- B_PDD7
- B_PDD8
- B_PDD9
- B_PDD10
- B_PDD11
- B_PDD12
- B_PDD13
- B_PDD14
- B_PDD15

- B_PDCS1#
- B_PDA0
- B_PDA2
- B_PDCS3#
- B_PDA1
- B_IRQ14
- B_PDDACK#
- B_PIORDY
- B_PDIOR#
- B_PDIOW#
- B_PDDREQ
- B_IDERST

Reference clock select


ATAIOEN	Note
0	Disable PATA output
1	enable PATA output

Operation Mode

MODE[2..0]	Device mode
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	Device mode 150MB/S
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

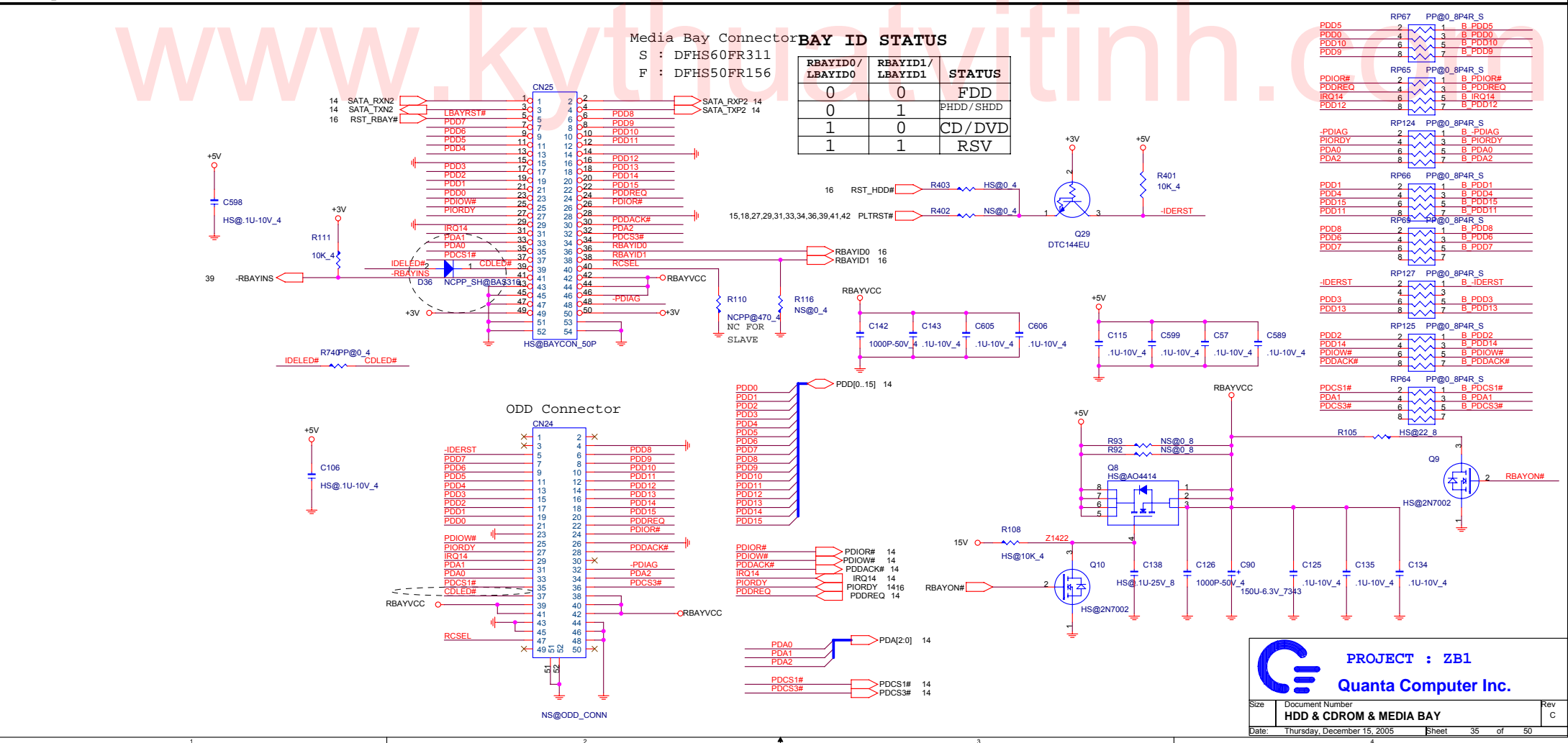
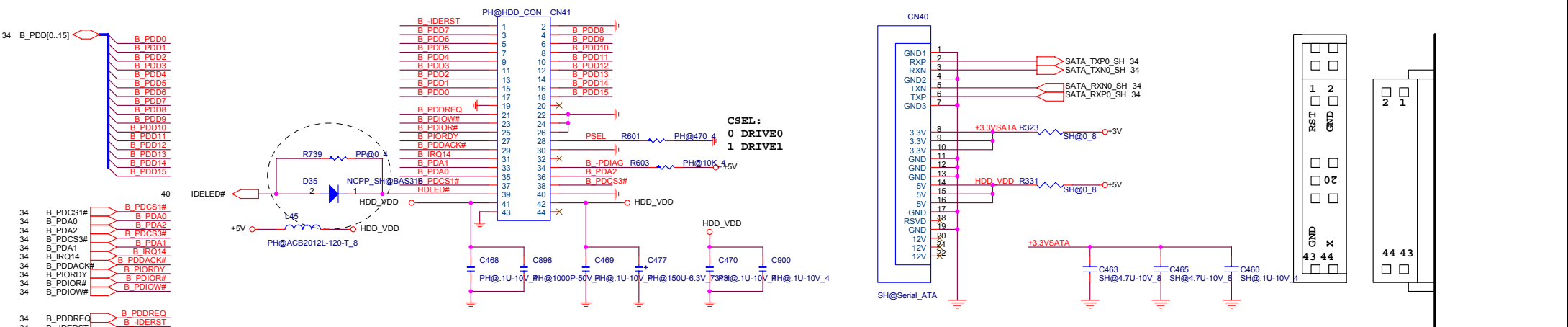
Reference clock select

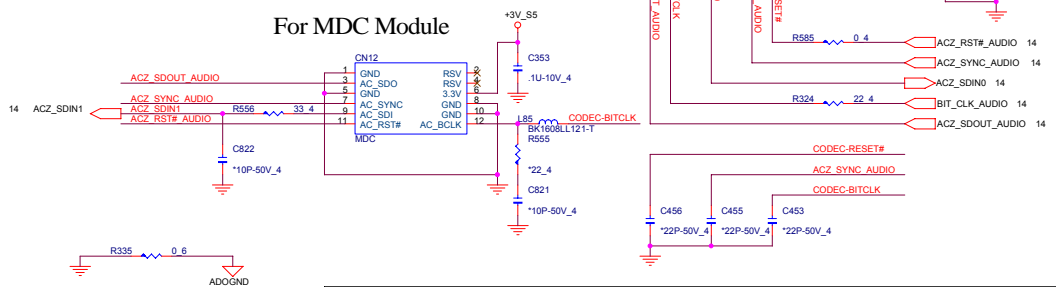
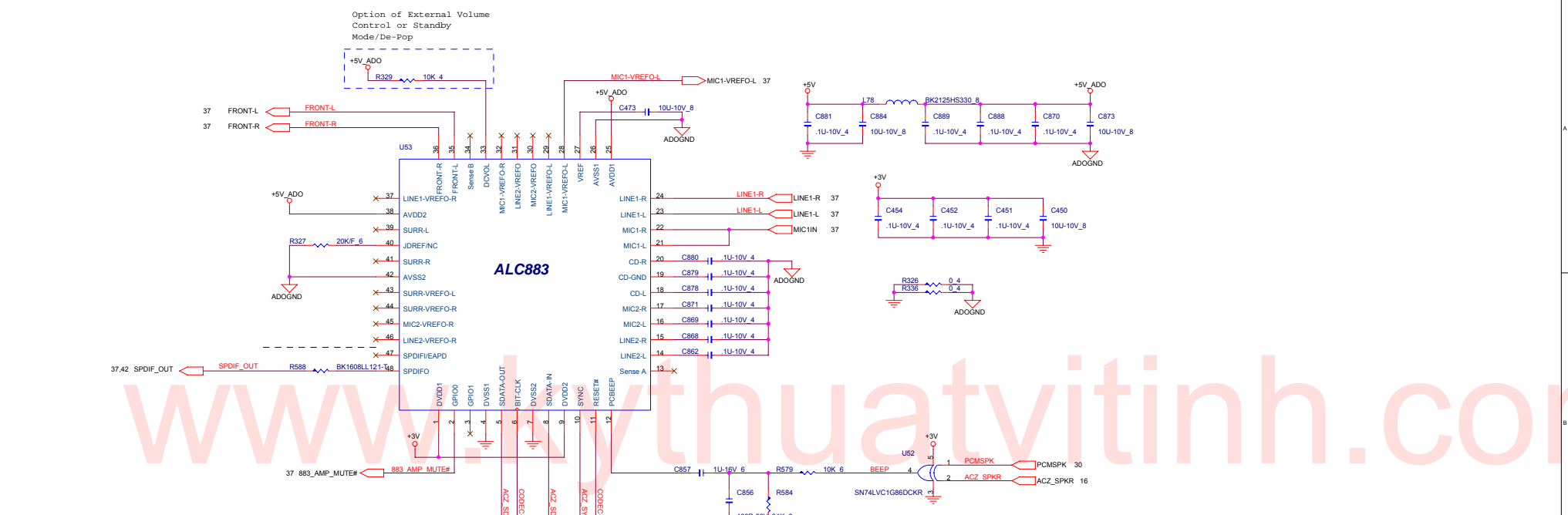
CLKSEL[1..0]	External clock
0 0	20 MHz
0 1	25 MHz



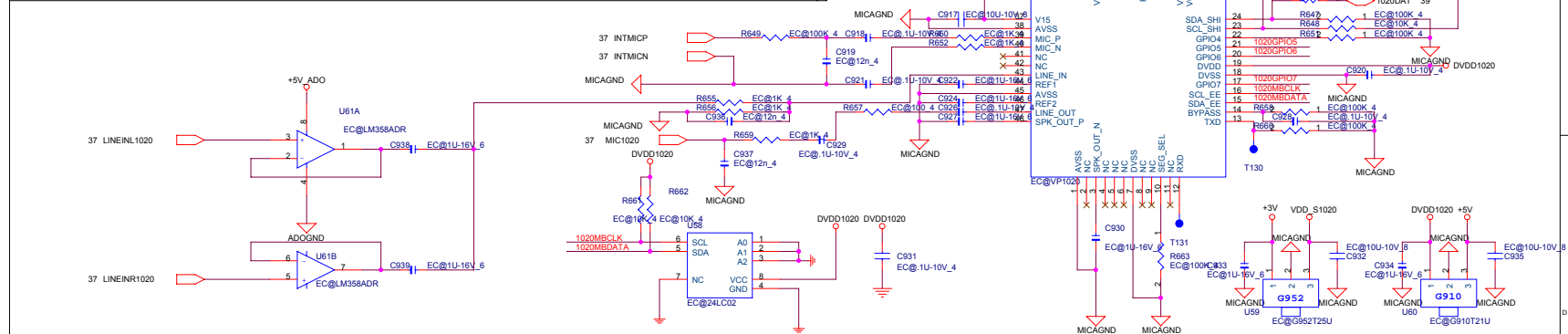
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/PATA	C
Date:	Thursday, December 15, 2005	Sheet 34 of 50



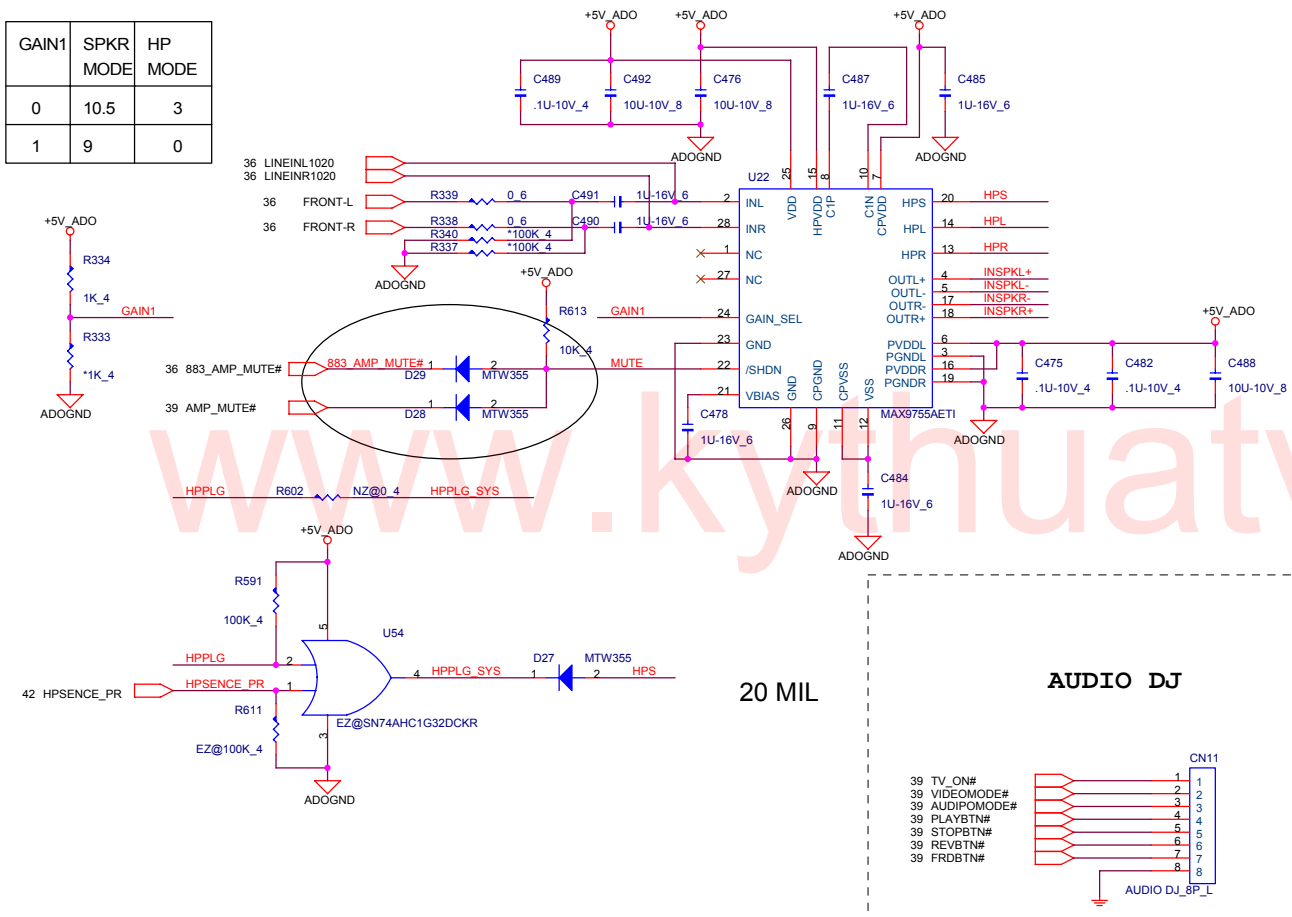


Tied at one point only under the
codec or near the codec



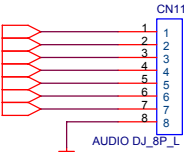
GPIO7	GPIO6	GPIO5	Internal mode
0	0	X	Internal mode
0	1	X	Reserved
1	0	0	Small EEPROM
1	1	0	Large EEPROM
1	0	1	SHI
1	1	1	UART

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

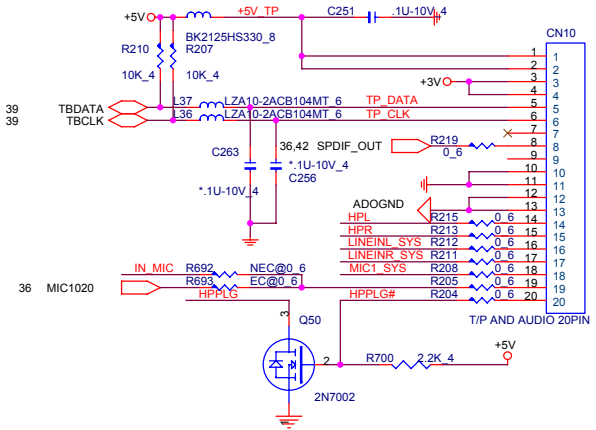


20 MIL

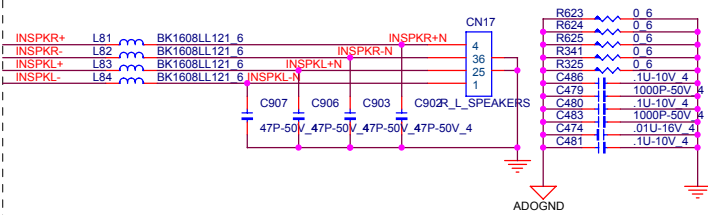
AUDIO DJ



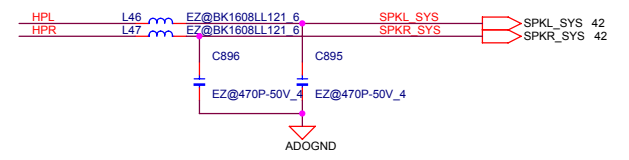
TOUCH PAD/AUDIO JACK FFC connector



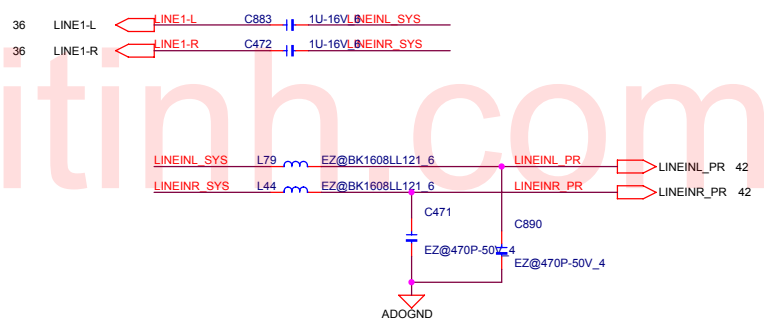
SPEAKER CONNECTOR



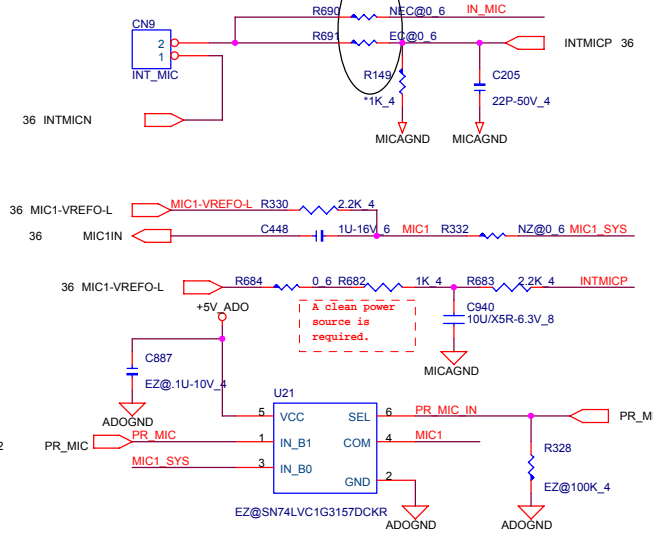
LINE OUT



LINE IN



MIC

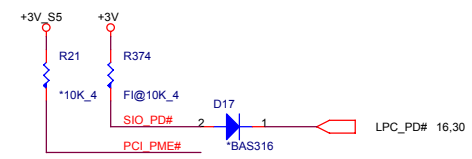
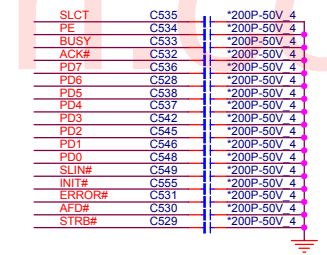
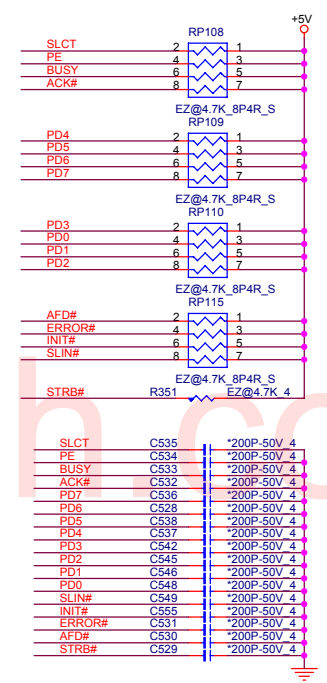
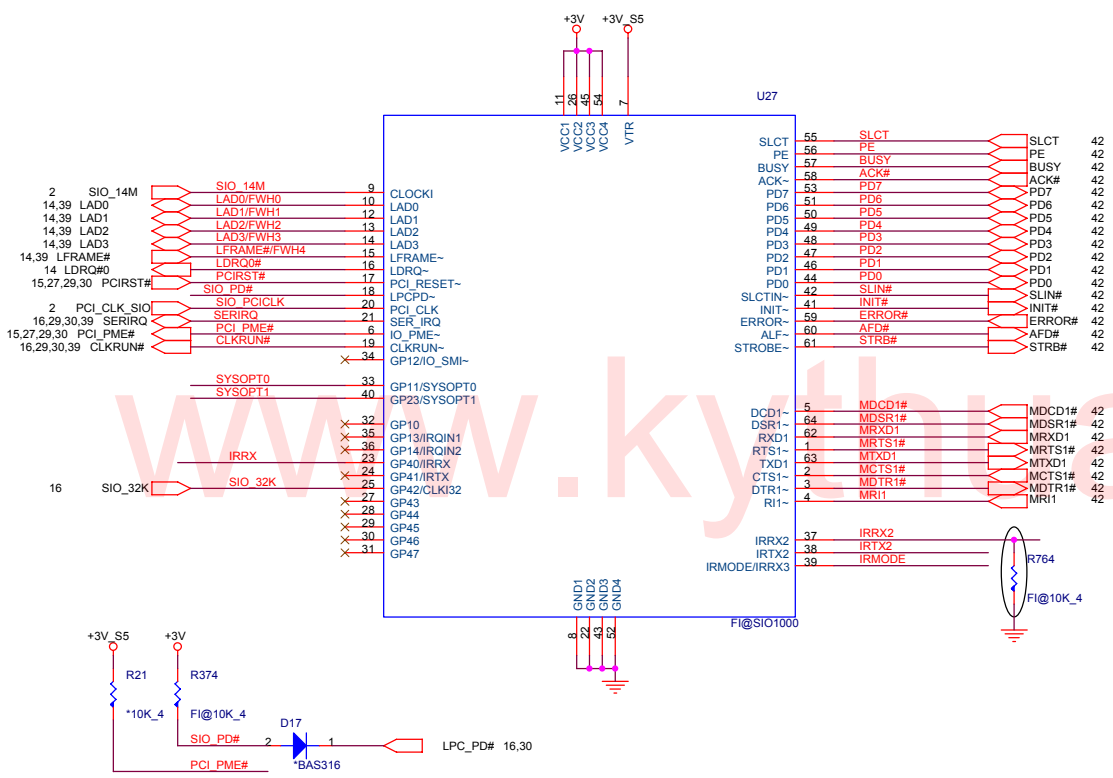


SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

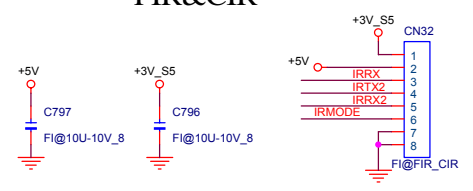
PROJECT : ZL6
Quanta Computer Inc.

Size: Document Number
AUDIO AMP (MAX 9755) Rev C

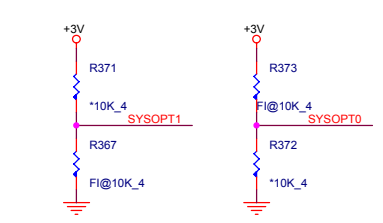
Date: Thursday, December 15, 2005 Sheet 37 of 50



FIR&CIR



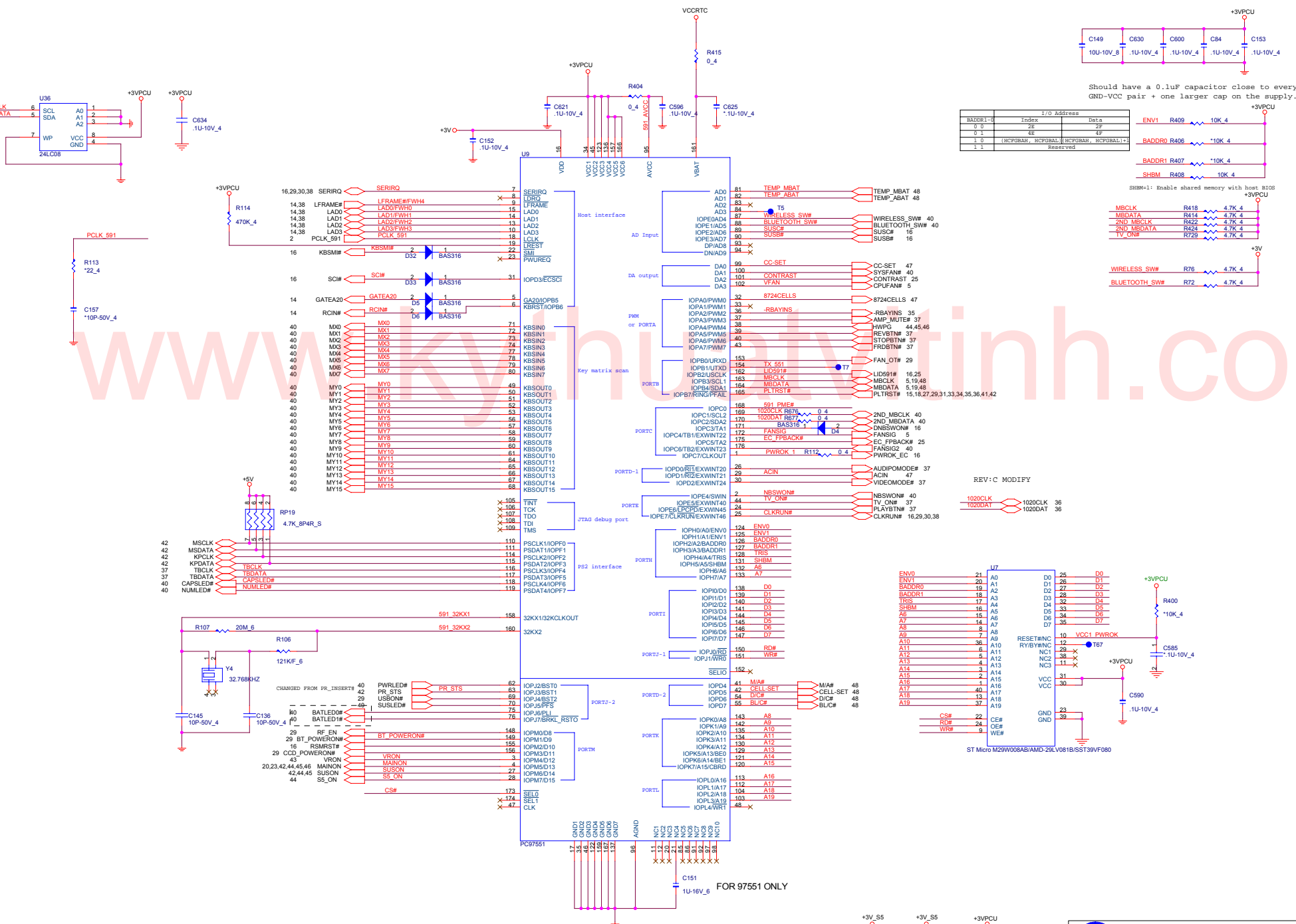
SYSOPT1	SYSOPT0	DEFAULT CONFIGURATION PORT BASE ADDRESS
0	0	0X002E
0	1	0X004E
1	0	0X162E
1	1	0X164E



PROJECT : ZB1
Quanta Computer Inc.

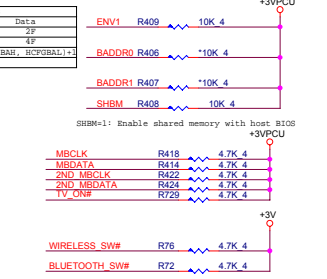
Size	Document Number	Rev
	SIO1000	C
Date:	Thursday, December 15, 2005	Sheet 38 of 50

LDRQ#(pin 8) internal is no use

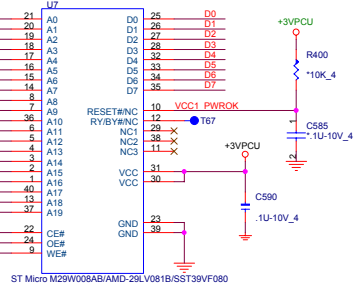
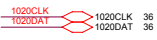


BADDR[1:0]	Index	I/O Address	Data
0 0	2E	2E	2F
0 1	4E	4E	4F
1 0	(HCPBMAN, HCPBVAL) (HCPBMAN, HCPBVAL)		
1 1	Reserved		

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.



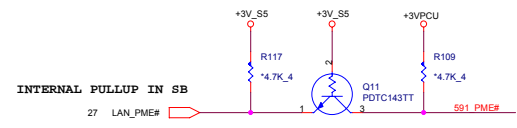
REV: C MODIFY



ST Micro M22W08AB/AMD-25LV0818/SS139VFB80

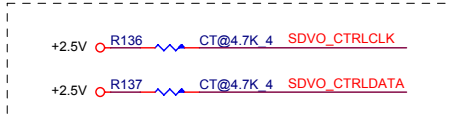
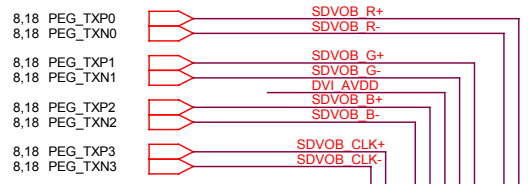
C151 1U-16V_4 FOR 97551 ONLY

INTERNAL PULLUP IN SB



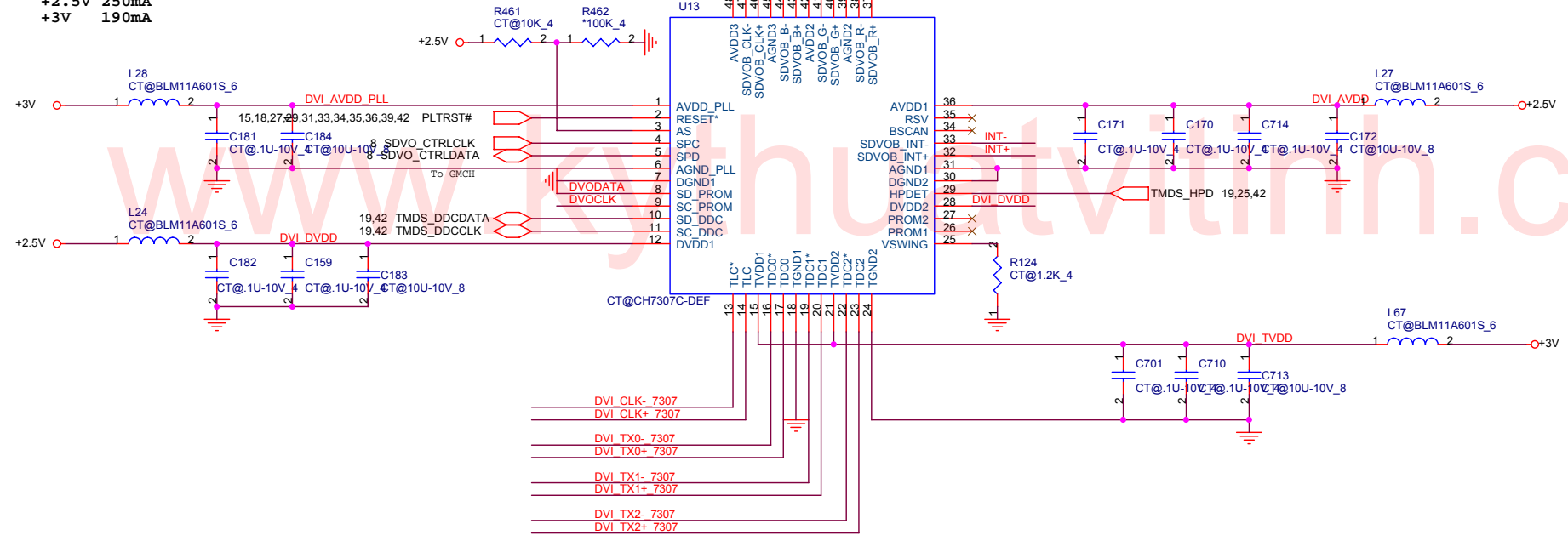
PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
	97551 & FLASH	C
Date	Thursday, December 15, 2005	Sheet 39 of 50

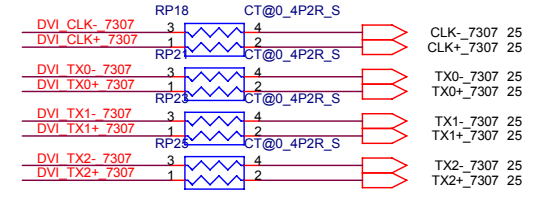
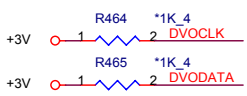
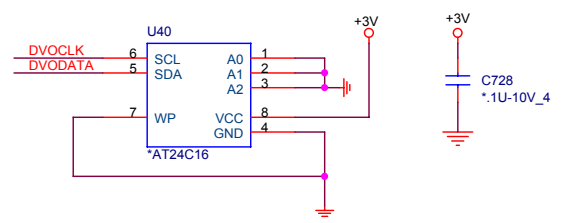


PULL LOW FOR DVO NOT PRESENT (INTERNAL PULLLOW IN 915GM)

+2.5V 250mA
+3V 190mA

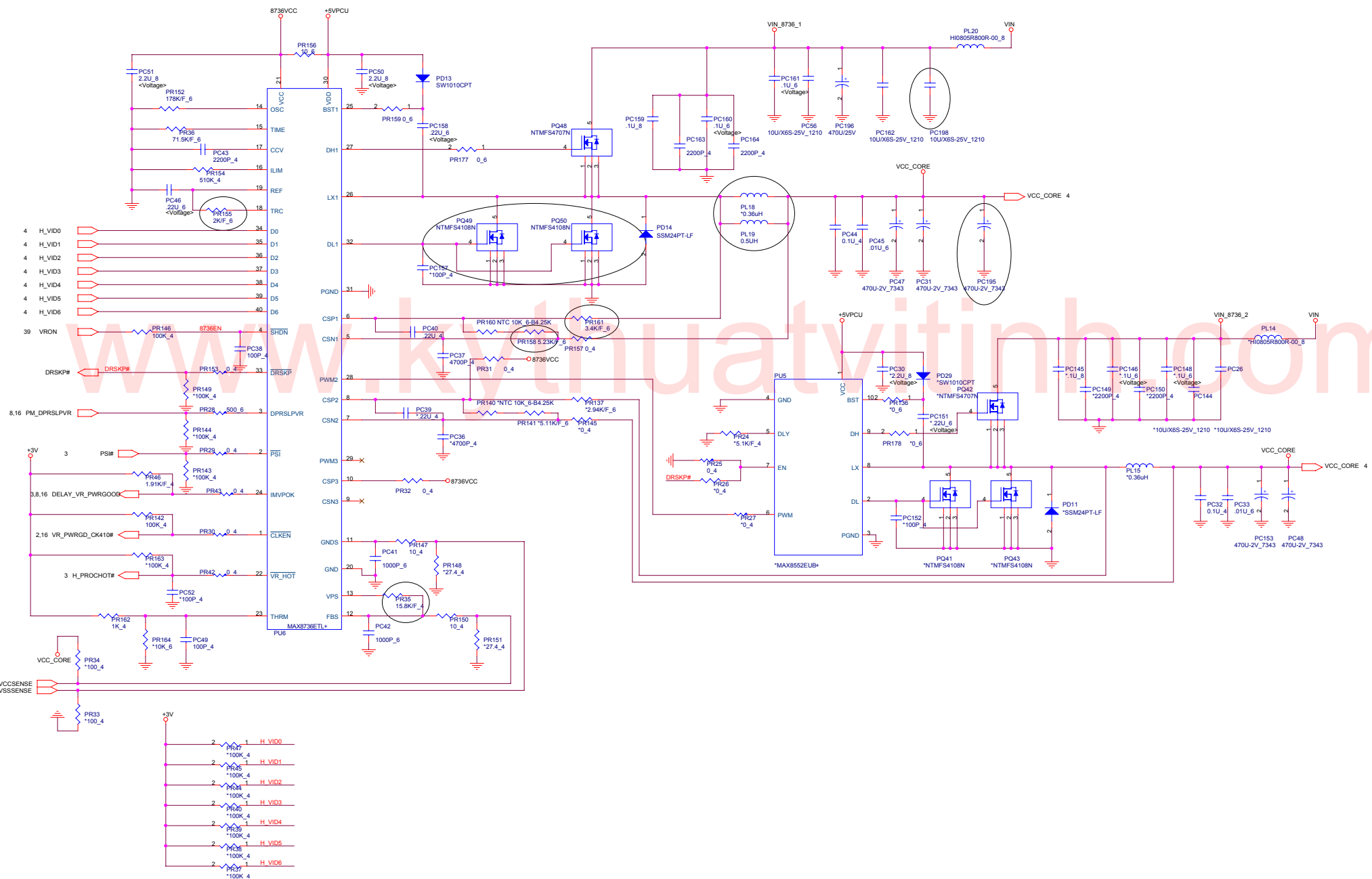


ALWAYS NOT ON, TEST ONLY

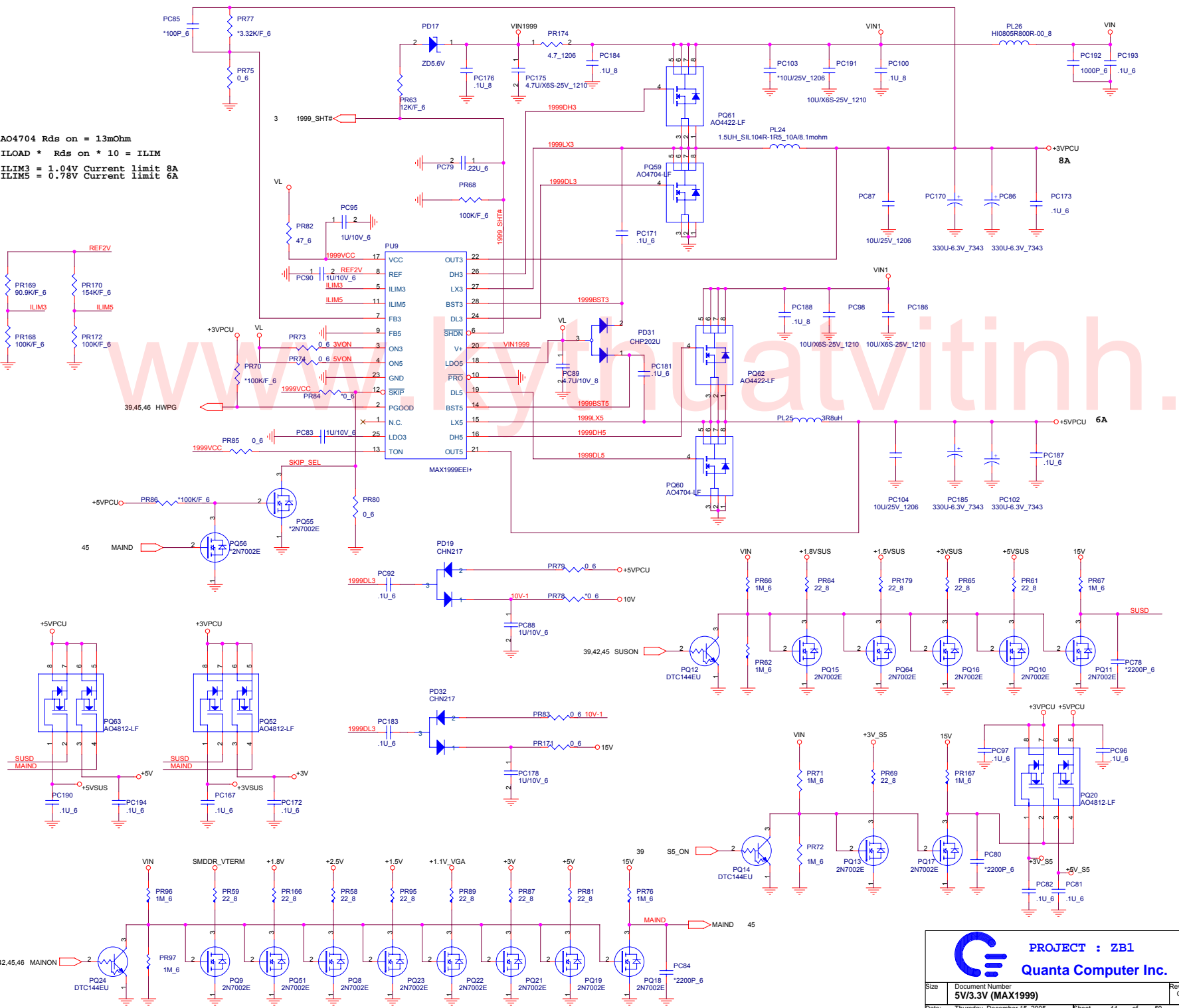


PROJECT : ZB1
Quanta Computer Inc.

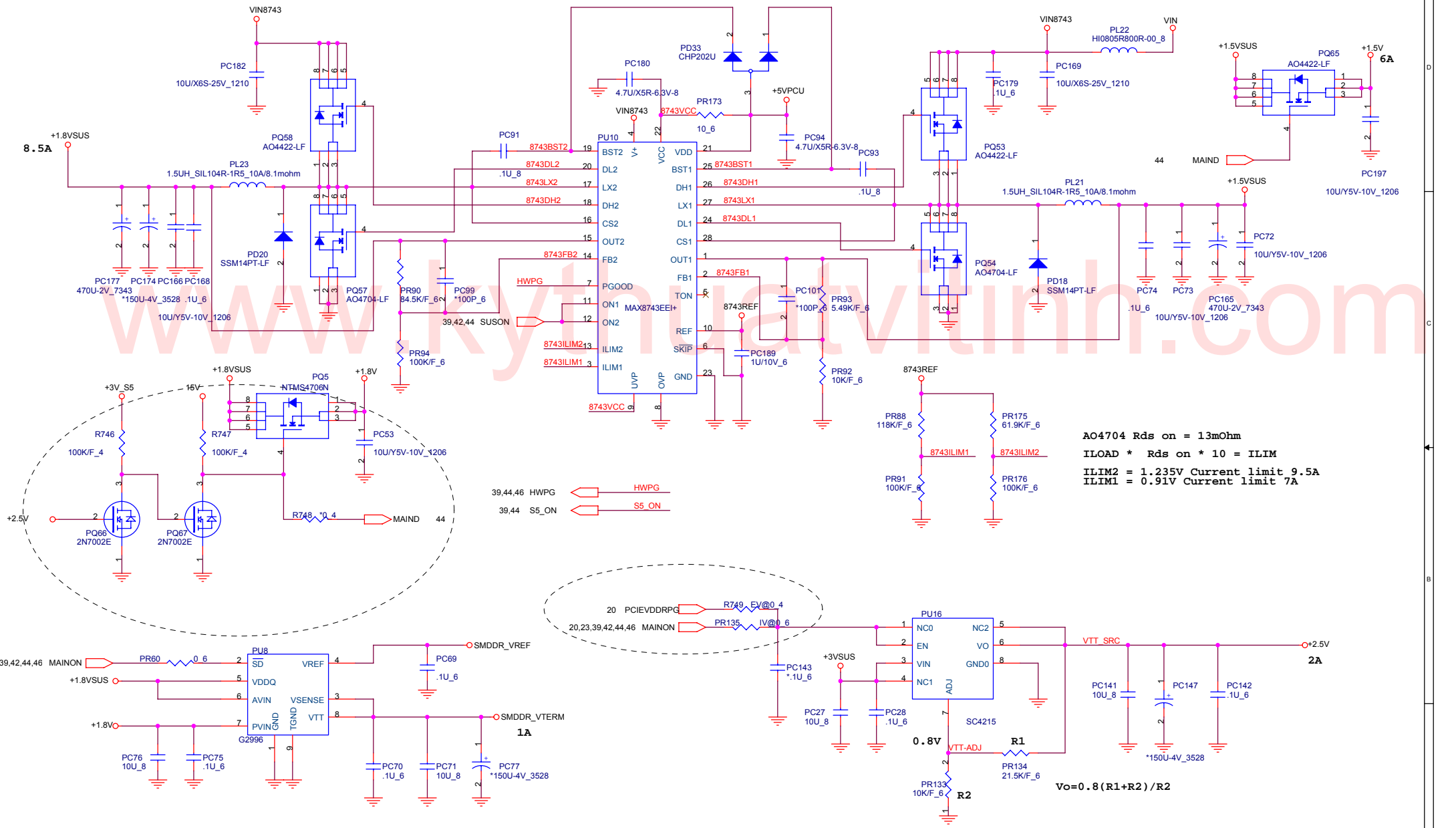
Size	Document Number	Rev
	CH7307	C
Date:	Thursday, December 15, 2005	Sheet 41 of 50



AO4704 Rds on = 13mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM3 = 1.04V Current limit 8A
 ILIM5 = 0.76V Current limit 6A



PROJECT : ZB1
Quanta Computer Inc.



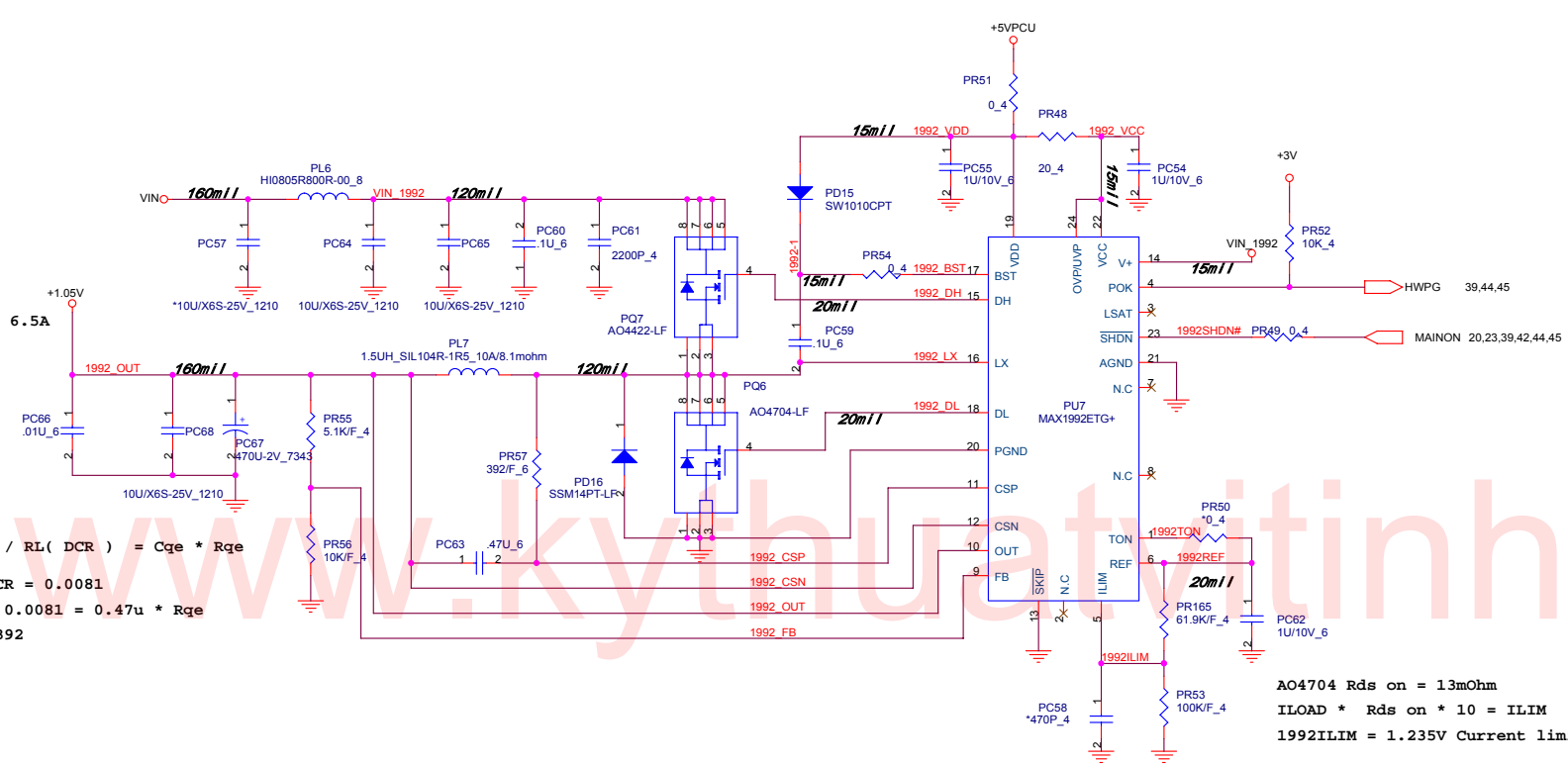
AO4704 Rds on = 13mOhm
 ILOAD * Rds on * 10 = ILIM
 ILIM2 = 1.235V Current limit 9.5A
 ILIM1 = 0.91V Current limit 7A

39.44,46 HWPG ← HWPG
 39.44 S5_ON ← S5_ON

$$V_o = 0.8 \frac{R1 + R2}{R2}$$

PROJECT : ZB1
Quanta Computer Inc.

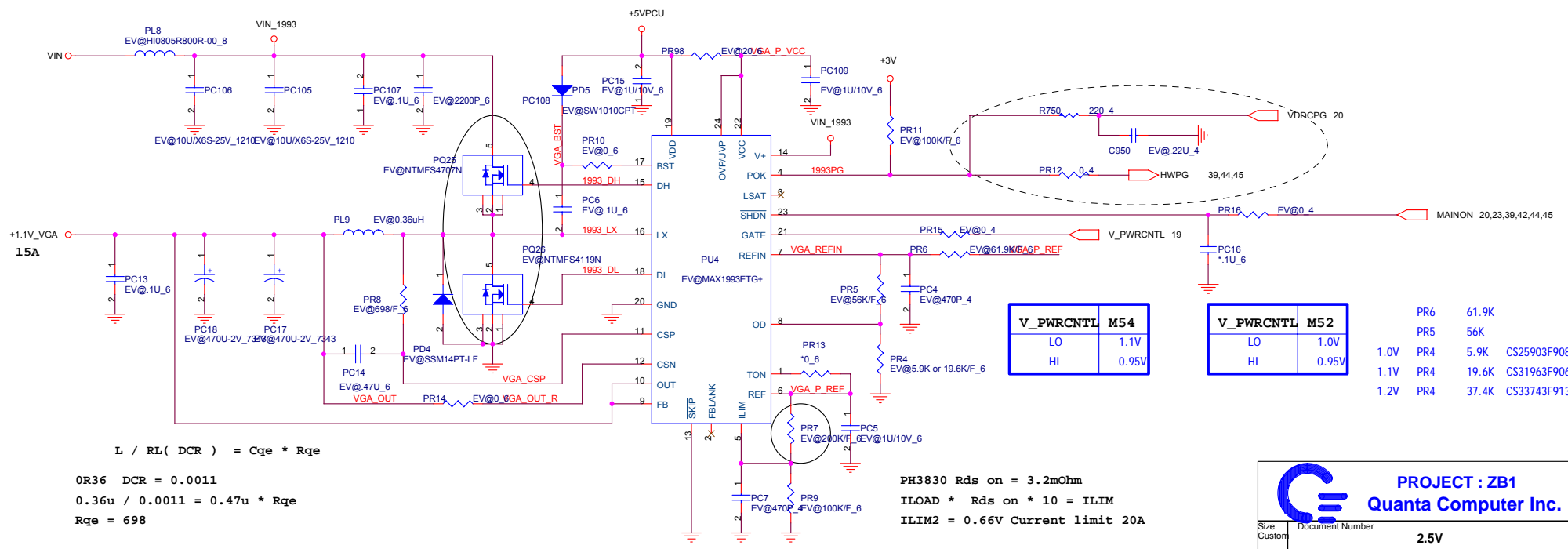
Size	Document Number	Rev
	+1.5 / CPUIO	C
Date:	Thursday, December 15, 2005	Sheet 45 of 50



$L / RL(DCR) = Cqe * Rqe$
 $1R5 DCR = 0.0081$
 $1.5u / 0.0081 = 0.47u * Rqe$
 $Rqe = 392$

AO4704 Rds on = 13mOhm
 $ILOAD * Rds on * 10 = ILIM$
 $1992ILIM = 1.235V$ Current limit 9.5A

M54



$L / RL(DCR) = Cqe * Rqe$
 $0R36 DCR = 0.0011$
 $0.36u / 0.0011 = 0.47u * Rqe$
 $Rqe = 698$

PH3830 Rds on = 3.2mOhm
 $ILOAD * Rds on * 10 = ILIM$
 $ILIM2 = 0.66V$ Current limit 20A

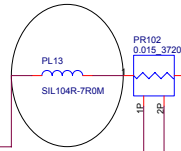
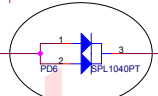
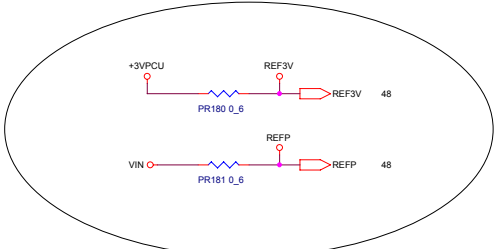
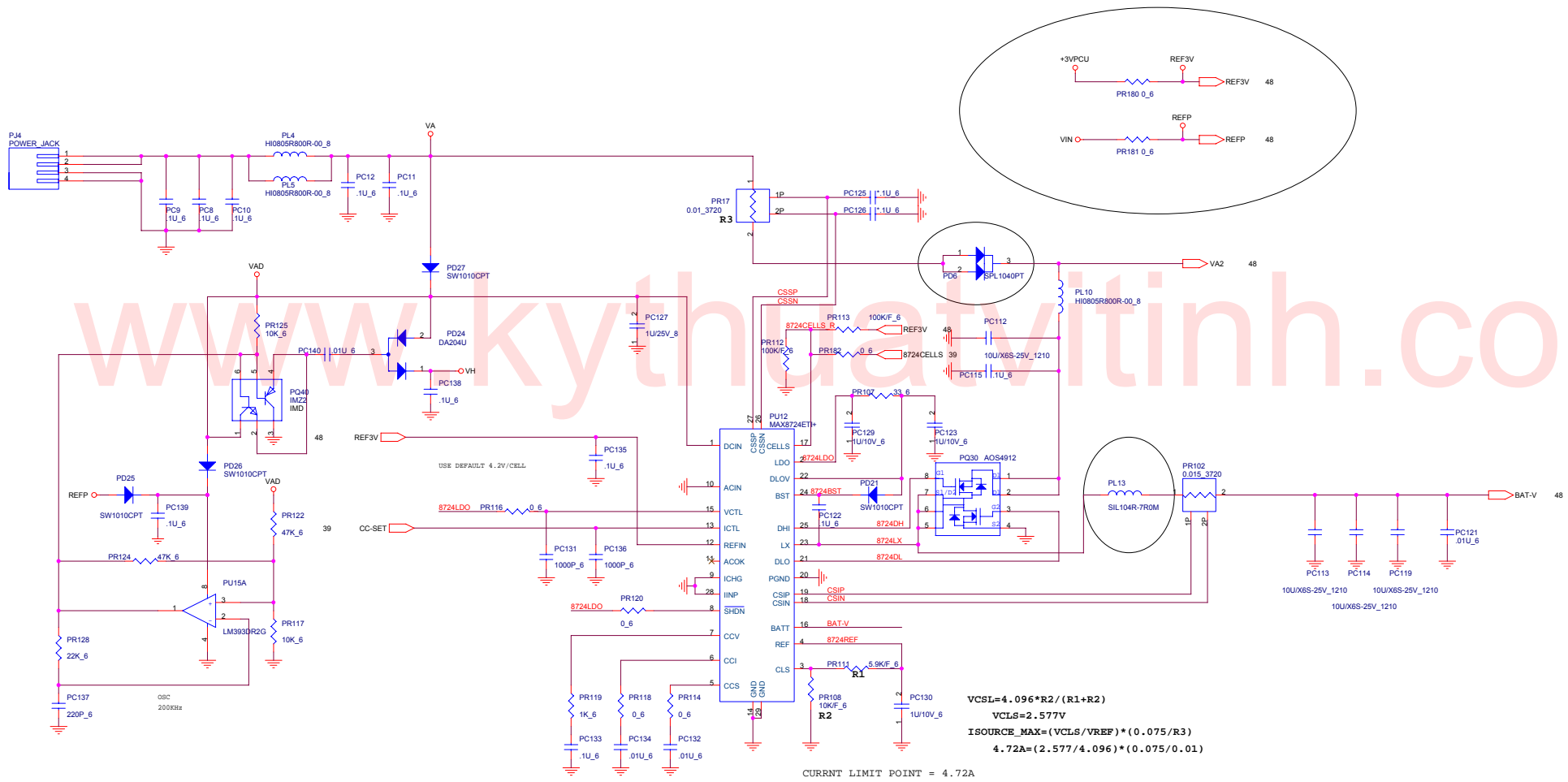
V_PWRCTRL M54	
LO	1.1V
HI	0.95V

V_PWRCTRL M52	
LO	1.0V
HI	0.95V

- PR6 61.9K
- PR5 56K
- 1.0V PR4 5.9K CS25903F908
- 1.1V PR4 19.6K CS31963F906
- 1.2V PR4 37.4K CS33743F913

PROJECT : ZB1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	2.5V	C
Date:	Thursday, December 15, 2005	Sheet 46 of 50



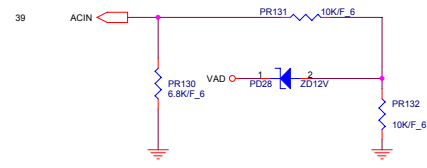
$$VCSL = 4.096 * R2 / (R1 + R2)$$

$$VCLS = 2.577V$$

$$ISOURCE_MAX = (VCLS / VREF) * (0.075 / R3)$$

$$4.72A = (2.577 / 4.096) * (0.075 / 0.01)$$

CURRNT LIMIT POINT = 4.72A



- P1. PR37 , PR38 , PR39 , PR40 , PR44 , PR45 , PR47 Change from 100K to NC.....Page 43
- P2. PR154 Change from 680K_4 to 510K_4Page 43
- P3. PR152 Change from 143K/F_4 to 169K_4Page 43
- P4. PR46 Change from 100K_4 to 1.91K/F_4Page 43
- P5. Add PC196 470u/25VPage 43
- P6. Add PC195 470u/2VPage 43
- P7. Add PR177 , PR178 0_6Page 43
- P8. PQ48 , PQ42 Change from PH7030L to NTMSF4707NPage 43
- P9. PQ41 , PQ43 , PQ49 , PQ50 Change from PH7030L to NTMSF4119NPage 43
- P10. Add PQ64 2N7002EPage 44
- P11. Add PR179 22_8Page 44
- P12. PU10 Pin11 connect Change from MAINON to SUSONPage 45
- P12. Add PQ65 AO4422Page 45
- P13. Add PC197 10u/Y5V-10_1206Page 45
- P14. PR52 pull hi Change from 3VFCU to +3VPage 46
- P15. PU7 Pin4 connect to HWPGPage 46
- P16. PR49 connect Change from VRON to MAINONPage 46
- P17. PR165 Change from 105K/F_4 to 61.9K/F_4Page 46
- P18. PQ25 Change from PH7030L to NTMSF4707NPage 46
- P19. PQ26 Change from PH7030L to NTMSF4119NPage 46
- P20. PR115 Change from 0 Ohm to NCPage 47
- P21. PR116 Change from NC to 0 OhmPage 47
- P22. Delete PQ33 IMD2 , PULL G914D , PC116 10u/10V_8 , PC118 0.1_6 , PC117 1u/10V_6.....Page 47
- P23. Add PR180 0_6.....Page 47
- P24. Add PR181 0_6.....Page 47
- P25. PL13 Change from 10u to 7u.....Page 47
- 1. RP62, RP61 Part number change from 33ohm to 49.9ohm (Part_No_A is correct)
- 2. PCIE n/p mirror (Giga LAN and Mini card LAN)
- 3. RP67, 64, 125, 127, 69, 66, 124, 65 Change to 0ohm
- 4. Unconnected cable select pin between HDD and CDROM.
- 5. Change R292 to 0Ohm for 1999_SHT#
- 6. R141,R173,R188 change to unstuff for GMCH strap
- 7. Add R247,R248, on BOM
- 8. Unstuff R51,R398,R41,R50 when use ATI VGA
- 9. Pull R395 to +3V when use ATI VGA
- 10. Unstuff R431 when use ATI VGA
- 11. Stuff C220,C747,C210,C749,C222,C745,C214,C748
- 12. R560 change to unstuff when use ULI chip
- 13. R136,R137 only stuff when use 7307
- 14. Add R637 (10K ohm)
- 15. Add CN35 on C,D CKU
- 16. U52 change to ON'a part
- 17. U41 Net swap between PIN3 and PIN4 for LAN EEPROM
- 18. Change footprint of SW4, S, 6, 7, 8 and U4
- 19. R628, R629 Change to unstuff for ZB1C
- 20. Change E24 PCIE to Lane5, 6
- 21. Delete C808, C809, CN31, Q16, R241, R242, R492 to unstuff (Acer specification change)
- 22. Change USB6 to CN21
- 23. PJ4 change to 4pin and cancel ADPID function.(Acer specification change)
- 24. VCCP power enable signal change to Mianon.
- 25. Add R638 (0 ohm, stuff when use UNA)
- 26. Add echo cancellation circuit.
- 27. Delete TPM circuit.
- 28. R116 change to stuff when no hot swap.
- 29. Add R685, R686 for VGA SMBus pull hi.
- 30. Add R687, R688 for VGA SMBus EC reserve.
- 31. Add R689 for ATI VGA PCIE clock strap.
- 32. Modify SB power plane.
- 33. Modify S-video pin define.
- 34. Modify USB power source to S5 power.
- 35. Add D31, R694 for S3-S5 wake on LAN.
- 36. Add R690-R693 for echo cancellation select.
- 37. Move R519, R540 to U5 for power decoupling.
- 38. Change R678, R679, R680, R681 to 1M Ohm for audio noise.
- 39. Modify U29 pin define for lan LED issue.
- 40. Exchange location of wireless LED and BT LED.
- 41. L73 change to CVA9115MN10

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5 4 3 2 1
NCPP@ Unstuff when use PATA HDD + PATA ODD.

EV@ Stuff when use external VGA.

IV@ Stuff when use UMA.

M56@ unstuff when use M52/54 ASIC.

EZ@ Stuff when use EZ4.

NZ@ Stuff when no EZ4.

DI@ Stuff when use DVI port.

CT@ Stuff when UMA with DVI port.

CT_EV@ Stuff when UMA with DVI port or external VGA.

SV@ Stuff when use S-video.

GL@ Stuff when use Giga lan.

NL@ Stuff when use 10/100 lan.

CR@ Stuff when use card reader

CR_PRO@ Stuff when card reader connector use PROCONN

FI@ Stuff when use FIR.

FW@ Stuff when use IEEE1394.

PH@ Stuff when use PATA HDD.

PP@ Stuff when use PATA HDD + PATA ODD.

SH@ Stuff when use SATA HDD.

SH_SP@ Stuff when use PATA to SATA bridge.

SH_SP_SUN@ Stuff when PATA to SATA bridge use SUNPLUS chip.

SH_SP_ULI@ Stuff when PATA to SATA bridge use ULI chip.

WIRE@ Stuff when LCD connector use wire type.

TV@ Stuff when use TV in.

CD@ Stuff when use camera.

NCD@ unstuff when use camera.

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Size	Document Number	Rev
	SKU Note	C
Date:	Thursday, December 15, 2005	Sheet 50 of 50