K40AB SCHEMATIC R1.3

SYSTEM PAGE REF.

POWER PAGE REF.

ASUSTeK COMPUTER INC. NB1

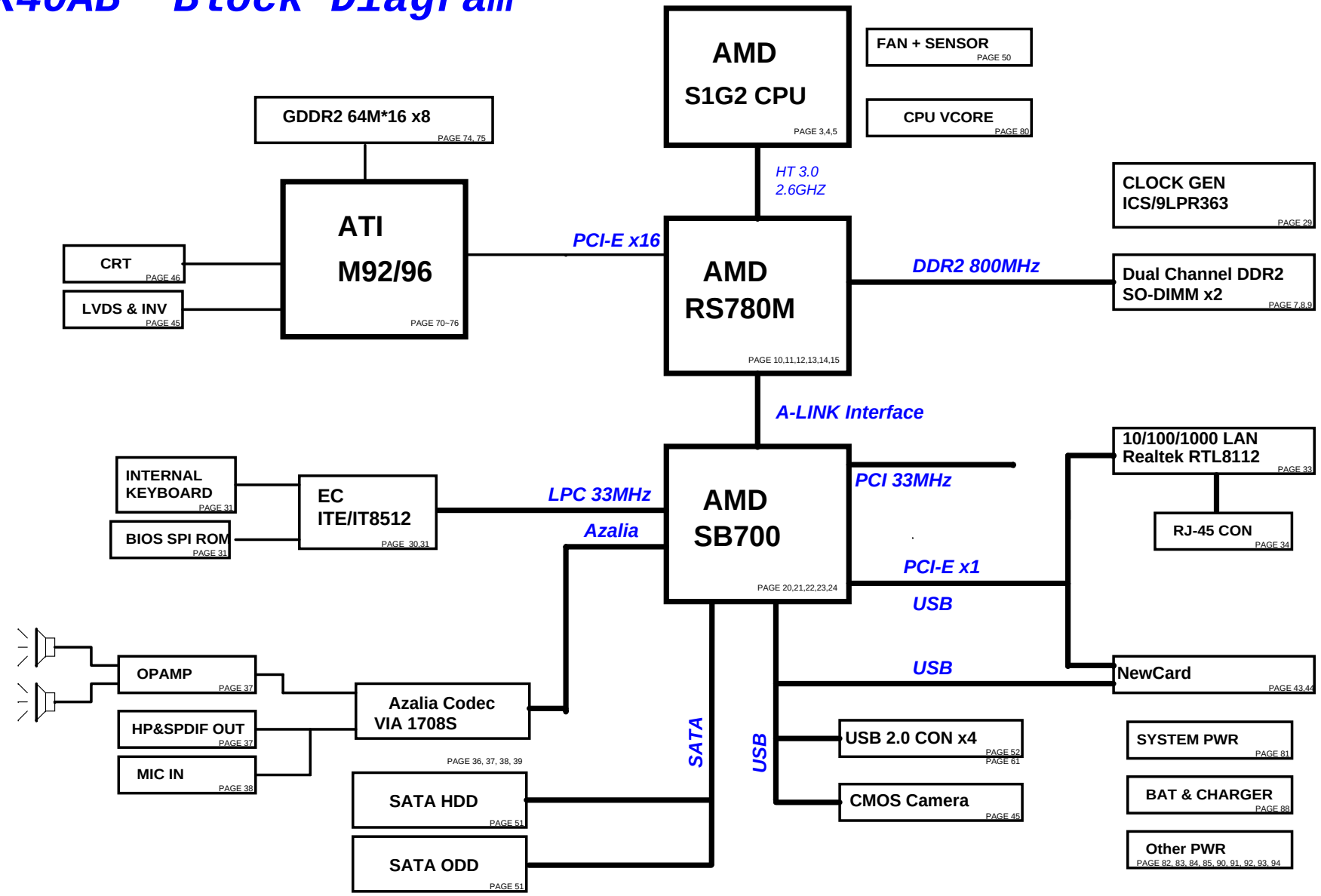
Title : Page Reference

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

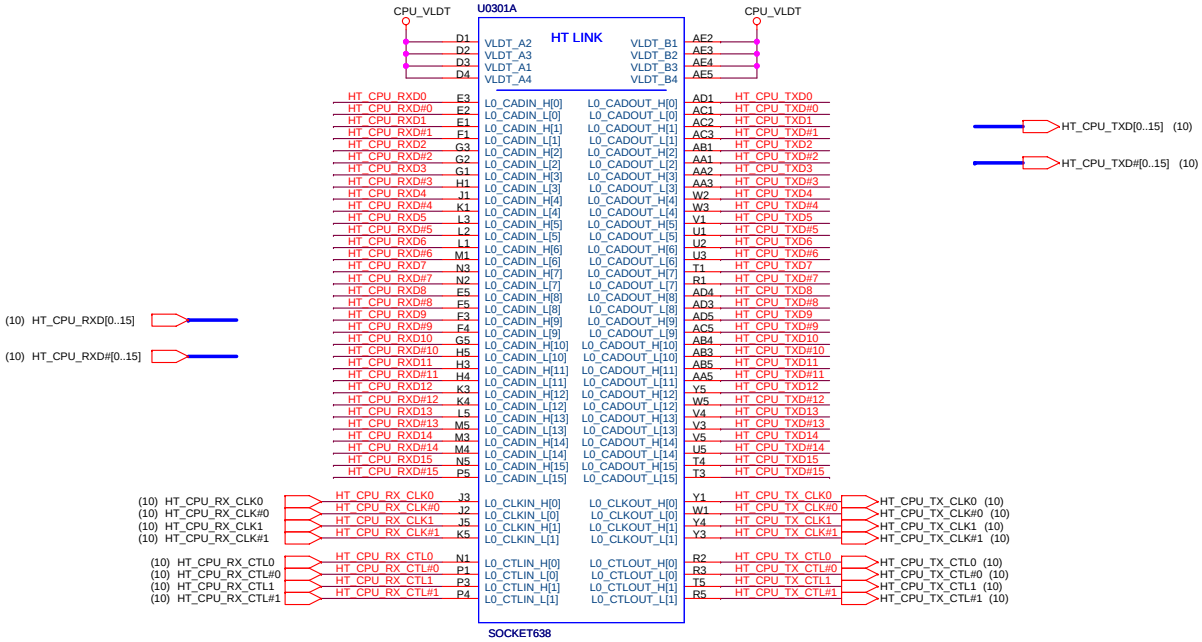
Date: Wednesday, April 08, 2009 Sheet 1 of 94

K40AB Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AB	Rev: R1.3
Date: Wednesday, April 08, 2009	Sheet 2 of 94	

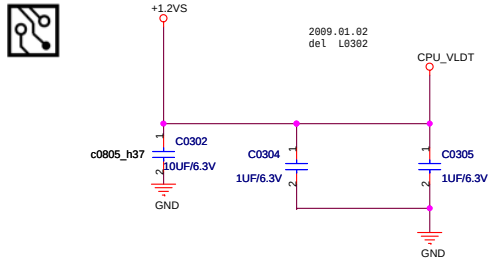
1.5A



Change P/N to 12G011306380

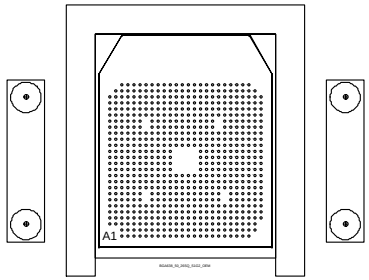
071113

Do not cross plane.



Place close to socket

*** If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**



ASUSTeK COMPUTER INC. NB1	Title : Griffin HT I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: K40AB	Rev: R1.3
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Processor Memory Interface

place close to PROCESSOR within 1.5 inch

(7) MEM_MA0_CLK7 — MEM_MA0_CLK_H7 — C0405 1.5PF/50V MLCC/+/-0.1PF — MEM_MA0_CLK_L7 — (7) MEM_MA0_CLK#7

(7) MEM_MA0_CLK1 — MEM_MA0_CLK_H1 — C0406 1.5PF/50V MLCC/+/-0.1PF — MEM_MA0_CLK_L1 — (7) MEM_MA0_CLK#1

071114

place close to PROCESSOR within 1.5 inch

(8) MEM_MB0_CLK7 — MEM_MB0_CLK_H7 — C0407 1.5PF/50V MLCC/+/-0.1PF — MEM_MB0_CLK_L7 — (8) MEM_MB0_CLK#7

(8) MEM_MB0_CLK1 — MEM_MB0_CLK_H1 — C0408 1.5PF/50V MLCC/+/-0.1PF — MEM_MB0_CLK_L1 — (8) MEM_MB0_CLK#1

0.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.8V — R0401 39.2OHM — M_ZP — AE10 — R0402 39.2OHM — M_ZN — AE10 — MEM_MA_RESET# — H16 — T0401 TPC28T

U0301B — MEM:CMD/CTRL/CLK — SOCKET638

+0.9V — D10, C10, B10, AD10 — VTT2, VTT8, VTT3, VTT1

M_ZP, M_ZN

RSVD8

(7,9) MEM_MA0_ODT0 — T19 — MA0_ODT[0]

(7,9) MEM_MA0_ODT1 — V22 — MA0_ODT[1]

TPC28T T0402 — MEM_MA1_ODT0 — U21 — MA1_ODT[0]

TPC28T T0403 — MEM_MA1_ODT1 — V19 — MA1_ODT[1]

(7,9) MEM_MA0_CS#0 — T20 — MA0_CS_L[0]

(7,9) MEM_MA0_CS#1 — U19 — MA0_CS_L[1]

U20 — MA1_CS_L[0]

V20 — MA1_CS_L[1]

(7,9) MEM_MA_CKE0 — J22 — MA_CKE[0]

(7,9) MEM_MA_CKE1 — J20 — MA_CKE[1]

N19 — MA_CLK_H[5]

MEM_MA0_CLK_H1 — N20 — MA_CLK_L[5]

MEM_MA0_CLK_L1 — F16 — MA_CLK_H[1]

MEM_MA0_CLK_H7 — F16 — MA_CLK_L[1]

MEM_MA0_CLK_L7 — Y16 — MA_CLK_H[7]

AA16 — MA_CLK_L[7]

P19 — MA_CLK_H[4]

P20 — MA_CLK_L[4]

(7,9) MEM_MA_ADD[0..15] — MEM_MA_ADD0 — N21 — MA_ADD[0]

MEM_MA_ADD1 — M20 — MA_ADD[1]

MEM_MA_ADD2 — N22 — MA_ADD[2]

MEM_MA_ADD3 — M19 — MA_ADD[3]

MEM_MA_ADD4 — M22 — MA_ADD[4]

MEM_MA_ADD5 — L20 — MA_ADD[5]

MEM_MA_ADD6 — M24 — MA_ADD[6]

MEM_MA_ADD7 — L21 — MA_ADD[7]

MEM_MA_ADD8 — L19 — MA_ADD[8]

MEM_MA_ADD9 — K22 — MA_ADD[9]

MEM_MA_ADD10 — R21 — MA_ADD[10]

MEM_MA_ADD11 — L22 — MA_ADD[11]

MEM_MA_ADD12 — K20 — MA_ADD[12]

MEM_MA_ADD13 — V24 — MA_ADD[13]

MEM_MA_ADD14 — K24 — MA_ADD[14]

MEM_MA_ADD15 — K19 — MA_ADD[15]

(7,9) MEM_MA_BANK0 — R20 — MA_BANK[0]

(7,9) MEM_MA_BANK1 — R23 — MA_BANK[1]

(7,9) MEM_MA_BANK2 — J21 — MA_BANK[2]

(7,9) MEM_MA_RAS# — R19 — MA_RAS_L

(7,9) MEM_MA_CAS# — T22 — MA_CAS_L

(7,9) MEM_MA_WE# — T24 — MA_WE_L

SOCKET638

+0.9V — W10, AC10, AB10, AA10, A10 — VTT4, VTT5, VTT6, VTT7, VTT9

Y10 — VTT_SENSE — 1 — T0417 TPC28T — 071115 — VTT_SENSE

CPU_M_VREF — W17 — M_VREF

B18 — MEM_MB_RESET# — TPC28T 1 — T0410 — RSVD6

W26 — MB0_ODT[0] — MEM_MB0_ODT0 (8,9)

W23 — MB0_ODT[1] — MEM_MB0_ODT1 (8,9)

Y26 — MEM_MB1_ODT0 — 1 — T0411 TPC28T — MB1_ODT[0]

V26 — MB0_CS_L[0] — MEM_MB0_CS#0 (8,9)

W25 — MB0_CS_L[1] — MEM_MB0_CS#1 (8,9)

U22 — MB1_CS_L[0]

J25 — MB_CKE[0] — MEM_MB_CKE0 (8,9)

H26 — MB_CKE[1] — MEM_MB_CKE1 (8,9)

P22 — MB_CLK_H[5]

R22 — MB_CLK_L[5]

A17 — MEM_MB0_CLK_H1 — MB_CLK_H[1]

A18 — MEM_MB0_CLK_L1 — MB_CLK_L[1]

AF18 — MEM_MB0_CLK_H7 — MB_CLK_H[7]

AF17 — MEM_MB0_CLK_L7 — MB_CLK_L[7]

R26 — MB_CLK_H[4]

R25 — MB_CLK_L[4]

P24 — MEM_MB_ADD0 — MB_ADD[0]

N24 — MEM_MB_ADD1 — MB_ADD[1]

P26 — MEM_MB_ADD2 — MB_ADD[2]

N23 — MEM_MB_ADD3 — MB_ADD[3]

N26 — MEM_MB_ADD4 — MB_ADD[4]

L23 — MEM_MB_ADD5 — MB_ADD[5]

N25 — MEM_MB_ADD6 — MB_ADD[6]

L24 — MEM_MB_ADD7 — MB_ADD[7]

M26 — MEM_MB_ADD8 — MB_ADD[8]

K26 — MEM_MB_ADD9 — MB_ADD[9]

T26 — MEM_MB_ADD10 — MB_ADD[10]

L26 — MEM_MB_ADD11 — MB_ADD[11]

L25 — MEM_MB_ADD12 — MB_ADD[12]

W24 — MEM_MB_ADD13 — MB_ADD[13]

J23 — MEM_MB_ADD14 — MB_ADD[14]

J24 — MEM_MB_ADD15 — MB_ADD[15]

MEM_MB_ADD[0..15] (8,9)

R24 — MB_BANK[0] — MEM_MB_BANK0 (8,9)

U26 — MB_BANK[1] — MEM_MB_BANK1 (8,9)

J26 — MB_BANK[2] — MEM_MB_BANK2 (8,9)

U25 — MB_RAS_L — MEM_MB_RAS# (8,9)

U24 — MB_CAS_L — MEM_MB_CAS# (8,9)

U23 — MB_WE_L — MEM_MB_WE# (8,9)

+1.8V — R0403 1KOhm 1% — CPU_M_VREF — C0403 0.1UF/16V — R0404 1KOhm 1% — GND

sensing point for op-amp feedback routed near CPU

PLACE CLOSE TO CPU

09/23 2.0

+0.9V — c0805_h37 — C0432 10UF/6.3V — C0433 10UF/6.3V — GND

+0.9V — C0430 0.1UF/16V — C0431 0.1UF/16V — GND

+0.9V — C0434 0.1UF/16V — C0435 0.1UF/16V — C0436 0.1UF/16V — C0437 0.1UF/16V — GND

(7) MEM_MA_DQS[0..7]

(7) MEM_MA_DQS#[0..7]

(8) MEM_MB_DQS[0..7]

(8) MEM_MB_DQS#[0..7]

U0301C — MEM:DATA — SOCKET638

To SODIMM socket 1

(8) MEM_MB_DATA[0..63]

MEM_MB_DATA0 — C11 — MB_DATA[0]
MEM_MB_DATA1 — A11 — MB_DATA[1]
MEM_MB_DATA2 — A14 — MB_DATA[2]
MEM_MB_DATA3 — B14 — MB_DATA[3]
MEM_MB_DATA4 — G11 — MB_DATA[4]
MEM_MB_DATA5 — E11 — MB_DATA[5]
MEM_MB_DATA6 — D12 — MB_DATA[6]
MEM_MB_DATA7 — A13 — MB_DATA[7]
MEM_MB_DATA8 — A15 — MB_DATA[8]
MEM_MB_DATA9 — A16 — MB_DATA[9]
MEM_MB_DATA10 — A19 — MB_DATA[10]
MEM_MB_DATA11 — A20 — MB_DATA[11]
MEM_MB_DATA12 — C14 — MB_DATA[12]
MEM_MB_DATA13 — D14 — MB_DATA[13]
MEM_MB_DATA14 — C18 — MB_DATA[14]
MEM_MB_DATA15 — D18 — MB_DATA[15]
MEM_MB_DATA16 — D20 — MB_DATA[16]
MEM_MB_DATA17 — A21 — MB_DATA[17]
MEM_MB_DATA18 — D24 — MB_DATA[18]
MEM_MB_DATA19 — C25 — MB_DATA[19]
MEM_MB_DATA20 — B20 — MB_DATA[20]
MEM_MB_DATA21 — C20 — MB_DATA[21]
MEM_MB_DATA22 — B24 — MB_DATA[22]
MEM_MB_DATA23 — C24 — MB_DATA[23]
MEM_MB_DATA24 — E23 — MB_DATA[24]
MEM_MB_DATA25 — E24 — MB_DATA[25]
MEM_MB_DATA26 — G25 — MB_DATA[26]
MEM_MB_DATA27 — G26 — MB_DATA[27]
MEM_MB_DATA28 — C26 — MB_DATA[28]
MEM_MB_DATA29 — D26 — MB_DATA[29]
MEM_MB_DATA30 — G23 — MB_DATA[30]
MEM_MB_DATA31 — G24 — MB_DATA[31]
MEM_MB_DATA32 — AA24 — MB_DATA[32]
MEM_MB_DATA33 — AA23 — MB_DATA[33]
MEM_MB_DATA34 — AD24 — MB_DATA[34]
MEM_MB_DATA35 — AE24 — MB_DATA[35]
MEM_MB_DATA36 — AA26 — MB_DATA[36]
MEM_MB_DATA37 — AA25 — MB_DATA[37]
MEM_MB_DATA38 — AD26 — MB_DATA[38]
MEM_MB_DATA39 — AE25 — MB_DATA[39]
MEM_MB_DATA40 — AC22 — MB_DATA[40]
MEM_MB_DATA41 — AD22 — MB_DATA[41]
MEM_MB_DATA42 — AE20 — MB_DATA[42]
MEM_MB_DATA43 — AF20 — MB_DATA[43]
MEM_MB_DATA44 — AF24 — MB_DATA[44]
MEM_MB_DATA45 — AF23 — MB_DATA[45]
MEM_MB_DATA46 — AC20 — MB_DATA[46]
MEM_MB_DATA47 — AD20 — MB_DATA[47]
MEM_MB_DATA48 — AD18 — MB_DATA[48]
MEM_MB_DATA49 — AE18 — MB_DATA[49]
MEM_MB_DATA50 — AC14 — MB_DATA[50]
MEM_MB_DATA51 — AD14 — MB_DATA[51]
MEM_MB_DATA52 — AF19 — MB_DATA[52]
MEM_MB_DATA53 — AC18 — MB_DATA[53]
MEM_MB_DATA54 — AF16 — MB_DATA[54]
MEM_MB_DATA55 — AF15 — MB_DATA[55]
MEM_MB_DATA56 — AF13 — MB_DATA[56]
MEM_MB_DATA57 — AC12 — MB_DATA[57]
MEM_MB_DATA58 — AB11 — MB_DATA[58]
MEM_MB_DATA59 — Y11 — MB_DATA[59]
MEM_MB_DATA60 — AE14 — MB_DATA[60]
MEM_MB_DATA61 — AF14 — MB_DATA[61]
MEM_MB_DATA62 — AF11 — MB_DATA[62]
MEM_MB_DATA63 — AD11 — MB_DATA[63]

MA_DATA[0..63] — MEM_MA_DATA[0..63] (7)

(8) MEM_MB_DM[0..7]

MEM_MB_DM0 — A12 — MB_DM[0]
MEM_MB_DM1 — B16 — MB_DM[1]
MEM_MB_DM2 — A22 — MB_DM[2]
MEM_MB_DM3 — E25 — MB_DM[3]
MEM_MB_DM4 — AB26 — MB_DM[4]
MEM_MB_DM5 — AE22 — MB_DM[5]
MEM_MB_DM6 — AC16 — MB_DM[6]
MEM_MB_DM7 — AD12 — MB_DM[7]

MA_DM[0..7] — MEM_MA_DM0 — E12
MEM_MA_DM1 — C15
MEM_MA_DM2 — E19
MEM_MA_DM3 — F24
MEM_MA_DM4 — AC24
MEM_MA_DM5 — Y19
MEM_MA_DM6 — AB16
MEM_MA_DM7 — Y13

MEM_MB_DQS0 — C12 — MB_DQS_H[0]
MEM_MB_DQS#0 — B12 — MB_DQS_L[0]
MEM_MB_DQS1 — D16 — MB_DQS_H[1]
MEM_MB_DQS#1 — C16 — MB_DQS_L[1]
MEM_MB_DQS2 — A24 — MB_DQS_H[2]
MEM_MB_DQS#2 — A23 — MB_DQS_L[2]
MEM_MB_DQS3 — F26 — MB_DQS_H[3]
MEM_MB_DQS#3 — E26 — MB_DQS_L[3]
MEM_MB_DQS4 — AC25 — MB_DQS_H[4]
MEM_MB_DQS#4 — AC26 — MB_DQS_L[4]
MEM_MB_DQS5 — AF21 — MB_DQS_H[5]
MEM_MB_DQS#5 — AF22 — MB_DQS_L[5]
MEM_MB_DQS6 — AE16 — MB_DQS_H[6]
MEM_MB_DQS#6 — AD16 — MB_DQS_L[6]
MEM_MB_DQS7 — AF12 — MB_DQS_H[7]
MEM_MB_DQS#7 — AE12 — MB_DQS_L[7]

MA_DQS_H[0..7] — MA_DQS_L[0..7] — MEM_MA_DQS0 — G13
MEM_MA_DQS#0 — H13
MEM_MA_DQS1 — G16
MEM_MA_DQS#1 — G15
MEM_MA_DQS2 — C22
MEM_MA_DQS#2 — C21
MEM_MA_DQS3 — G22
MEM_MA_DQS#3 — G21
MEM_MA_DQS4 — AD23
MEM_MA_DQS#4 — AC23
MEM_MA_DQS5 — AB19
MEM_MA_DQS#5 — AB20
MEM_MA_DQS6 — Y15
MEM_MA_DQS#6 — W15
MEM_MA_DQS7 — W12
MEM_MA_DQS#7 — W13

To SODIMM socket 0

MEM_MA_DATA0 — G12
MEM_MA_DATA1 — F12
MEM_MA_DATA2 — H14
MEM_MA_DATA3 — G14
MEM_MA_DATA4 — H11
MEM_MA_DATA5 — H12
MEM_MA_DATA6 — C13
MEM_MA_DATA7 — E13
MEM_MA_DATA8 — H15
MEM_MA_DATA9 — E15
MEM_MA_DATA10 — E17
MEM_MA_DATA11 — H17
MEM_MA_DATA12 — E14
MEM_MA_DATA13 — F14
MEM_MA_DATA14 — C17
MEM_MA_DATA15 — G17
MEM_MA_DATA16 — G18
MEM_MA_DATA17 — C19
MEM_MA_DATA18 — D22
MEM_MA_DATA19 — E20
MEM_MA_DATA20 — E18
MEM_MA_DATA21 — F18
MEM_MA_DATA22 — B22
MEM_MA_DATA23 — C23
MEM_MA_DATA24 — F20
MEM_MA_DATA25 — F22
MEM_MA_DATA26 — H24
MEM_MA_DATA27 — J19
MEM_MA_DATA28 — E21
MEM_MA_DATA29 — F22
MEM_MA_DATA30 — H20
MEM_MA_DATA31 — H22
MEM_MA_DATA32 — Y24
MEM_MA_DATA33 — AB24
MEM_MA_DATA34 — AB22
MEM_MA_DATA35 — AA21
MEM_MA_DATA36 — W22
MEM_MA_DATA37 — W21
MEM_MA_DATA38 — Y22
MEM_MA_DATA39 — AA22
MEM_MA_DATA40 — Y20
MEM_MA_DATA41 — AA20
MEM_MA_DATA42 — AA18
MEM_MA_DATA43 — B18
MEM_MA_DATA44 — AB21
MEM_MA_DATA45 — AD21
MEM_MA_DATA46 — AD19
MEM_MA_DATA47 — Y18
MEM_MA_DATA48 — AD17
MEM_MA_DATA49 — W16
MEM_MA_DATA50 — W14
MEM_MA_DATA51 — Y14
MEM_MA_DATA52 — Y17
MEM_MA_DATA53 — AB17
MEM_MA_DATA54 — AB15
MEM_MA_DATA55 — AD15
MEM_MA_DATA56 — AB13
MEM_MA_DATA57 — AD13
MEM_MA_DATA58 — Y12
MEM_MA_DATA59 — W11
MEM_MA_DATA60 — AB14
MEM_MA_DATA61 — AA14
MEM_MA_DATA62 — AB12
MEM_MA_DATA63 — AA12

ASUSTeK COMPUTER INC. NB1

Title : Griffin DDR2 MEMORY I/F

Engineer: <OrgAddr1>

Size: Custom | Project Name | Rev

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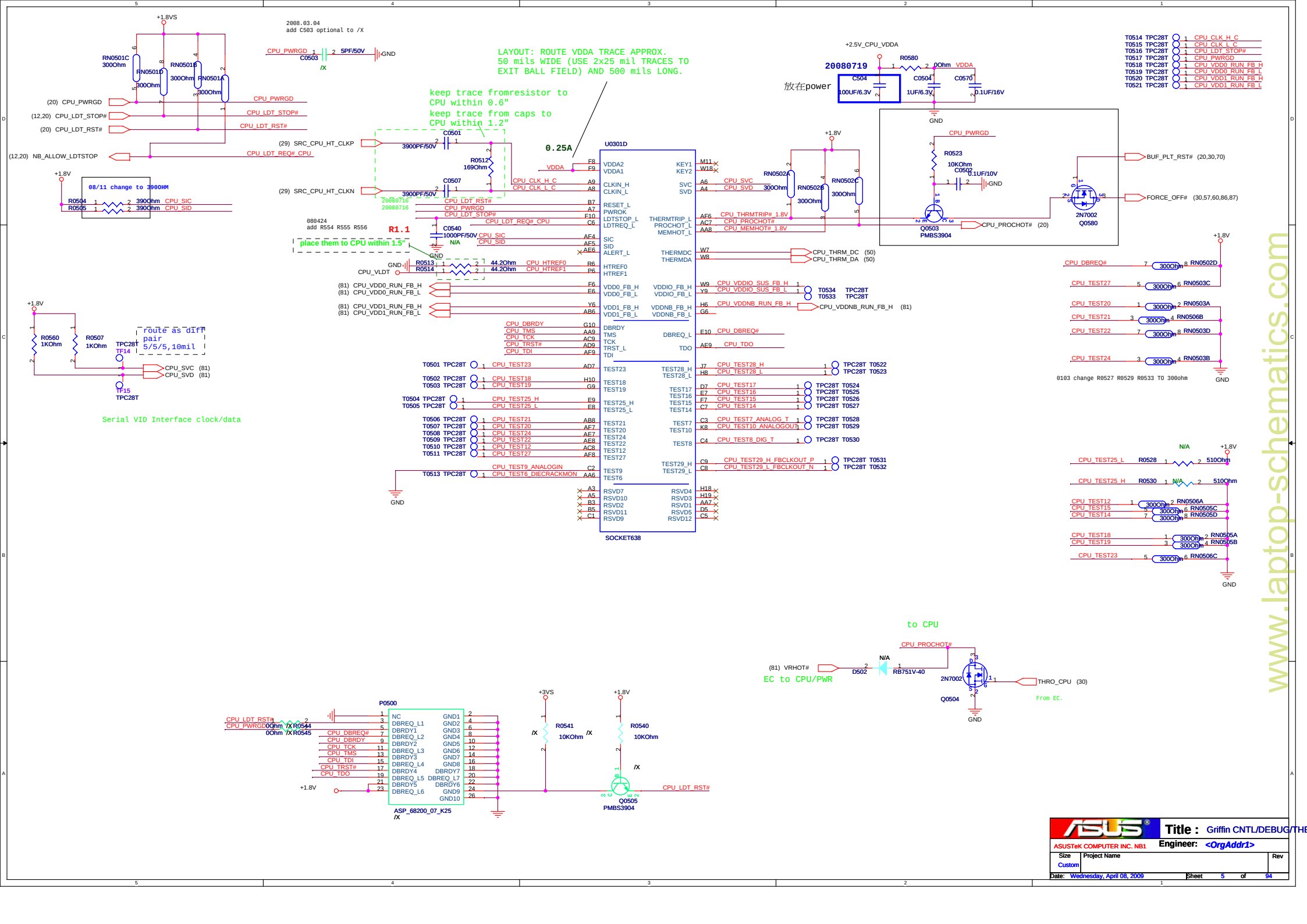
2008.03.04
add C503 optional to /X
LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
0.25A
place them to CPU within 1.5"
080424
add R554 R555 R556
R1.1
08/11 change to 300OHM
route as diff
pair
5/5/5,10mil
Serial VID Interface clock/data
SOCKET638
U0301D
放在power
20080719
0103 change R0527 R0529 R0533 TO 300ohm
EC to CPU/PWR
to CPU
From EC.
ASP_68200_07_K25
P0500
Title : Griffin CNTL/DEBUG/THE
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Project Name
Date: Wednesday, April 08, 2009
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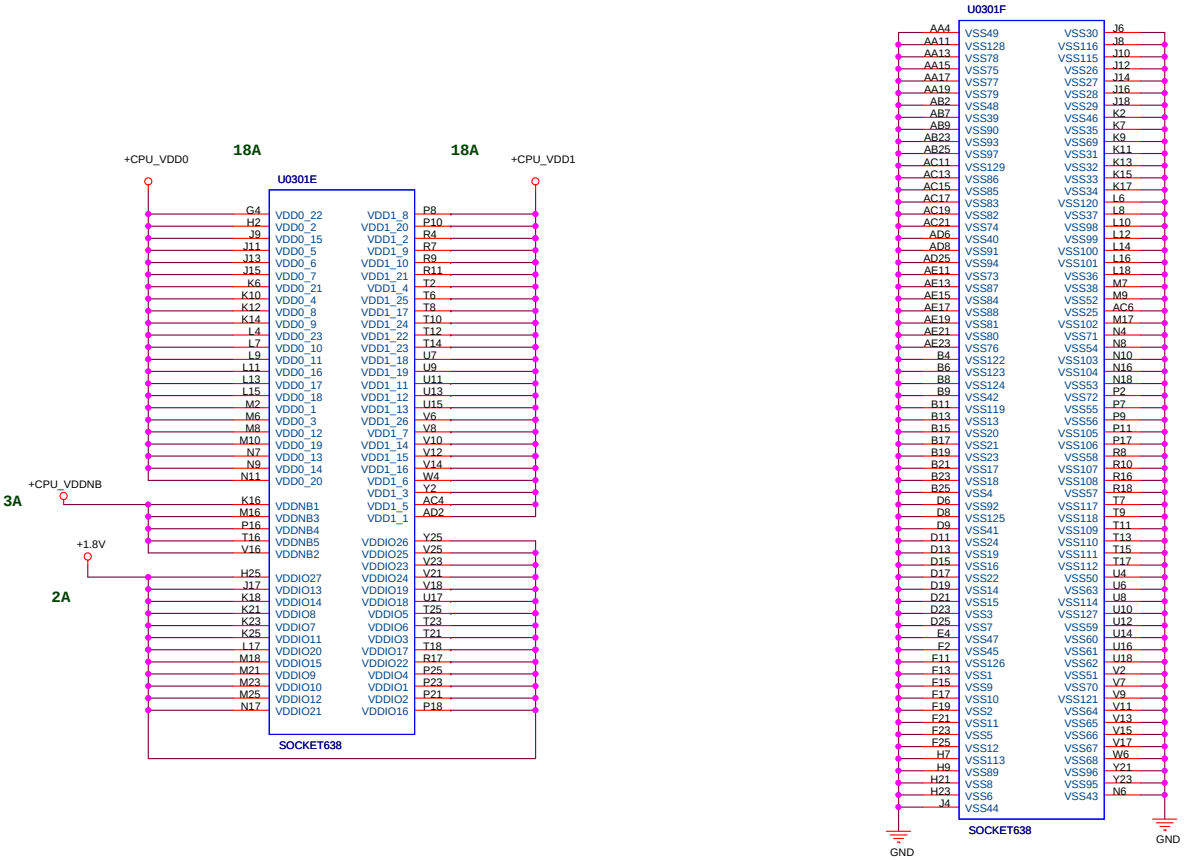
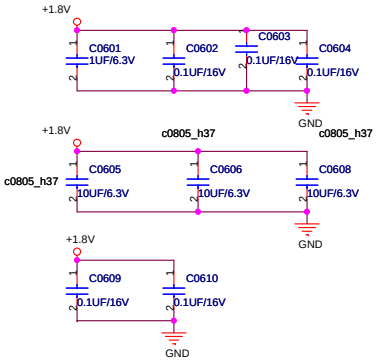
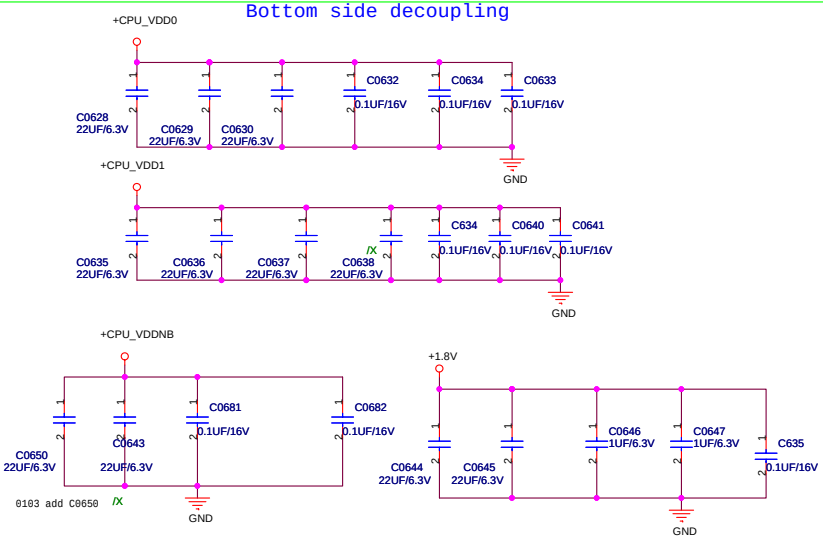


Decoupling between Processor and DIMMs, Place close to Porcessor as possible



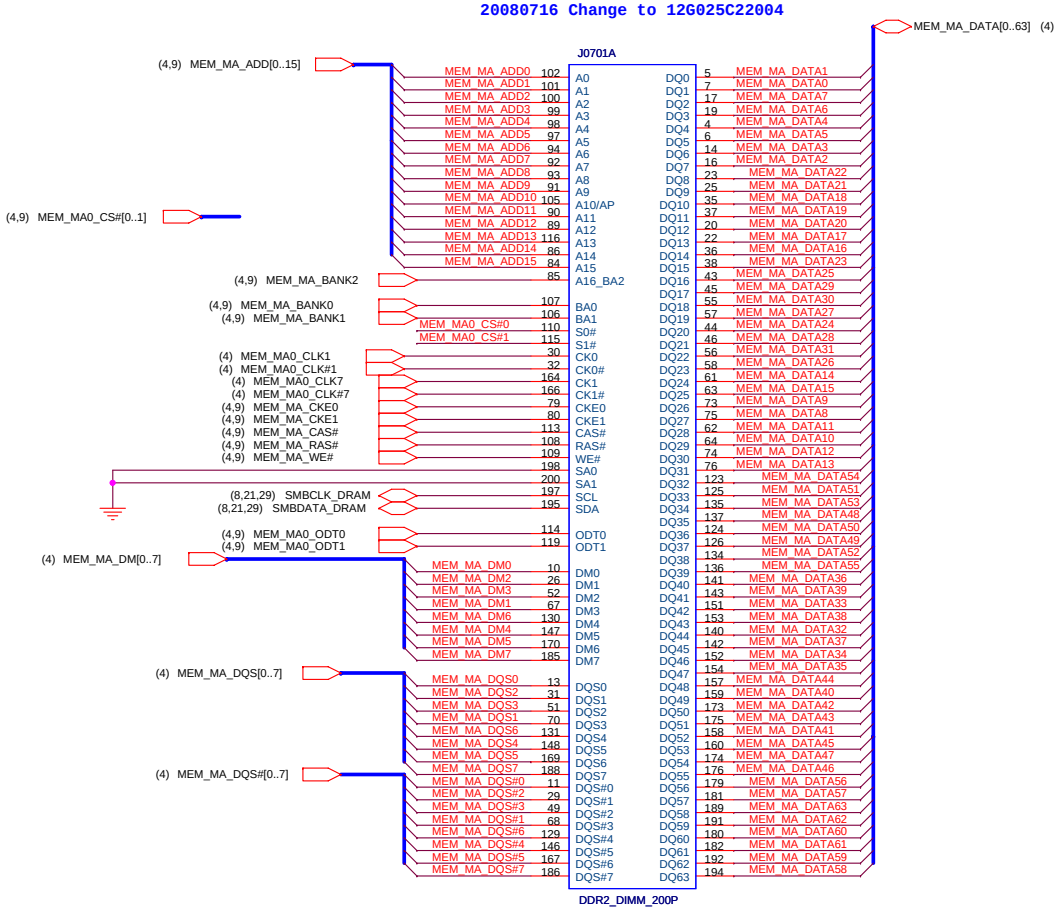
place close to socket

Bottom side decoupling

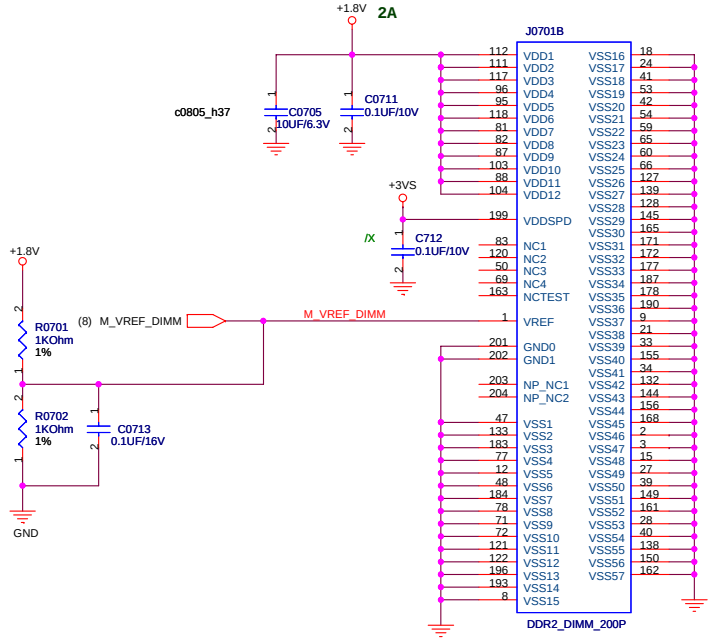


ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 6 of 94	

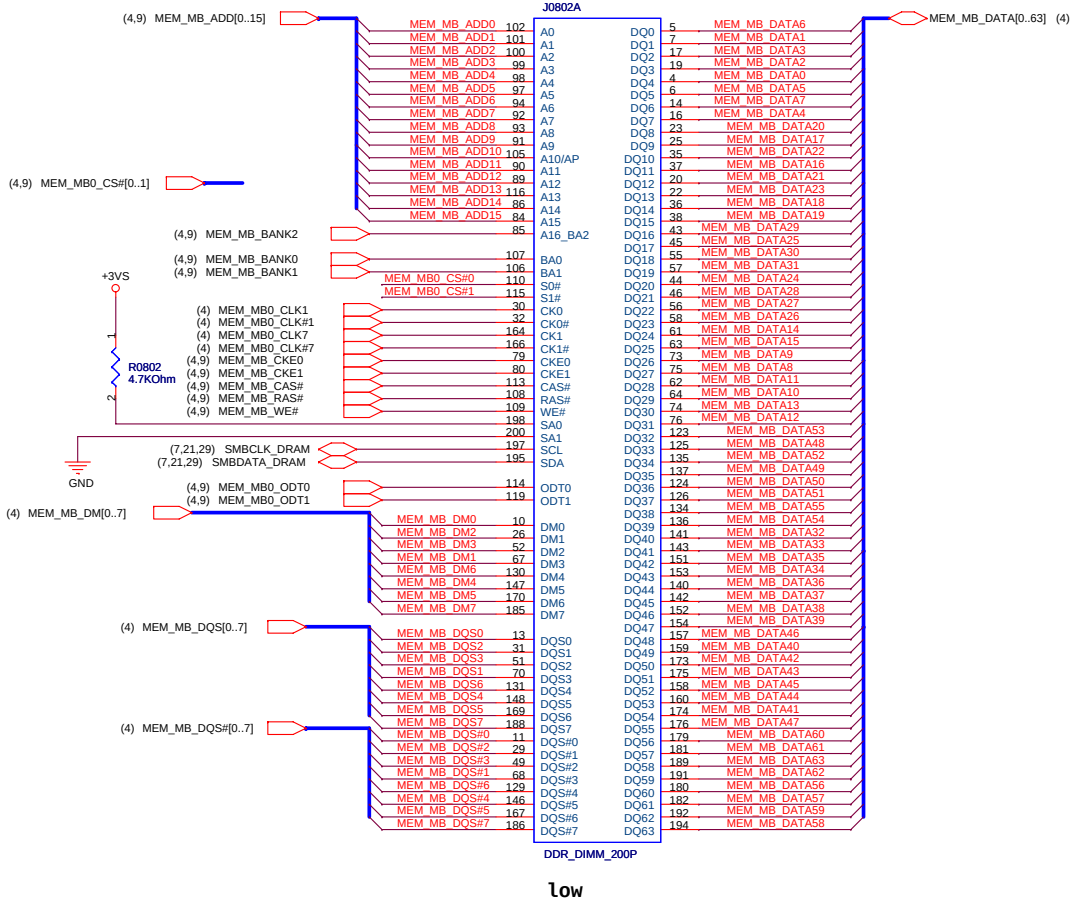
20080716 Change to 12G025C22004

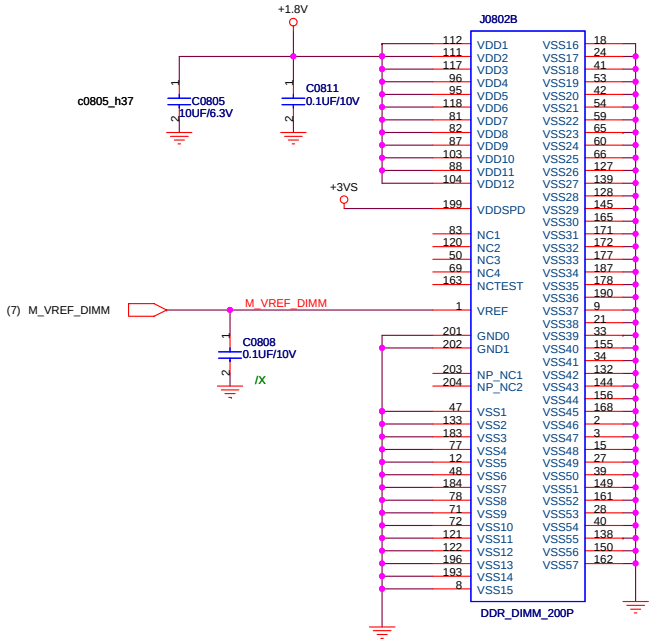


High

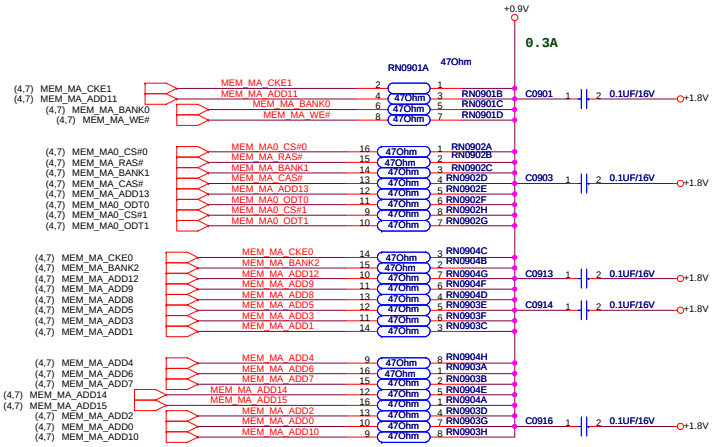


ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name		Rev
Date: Wednesday, April 08, 2009	Sheet 7 of 94		

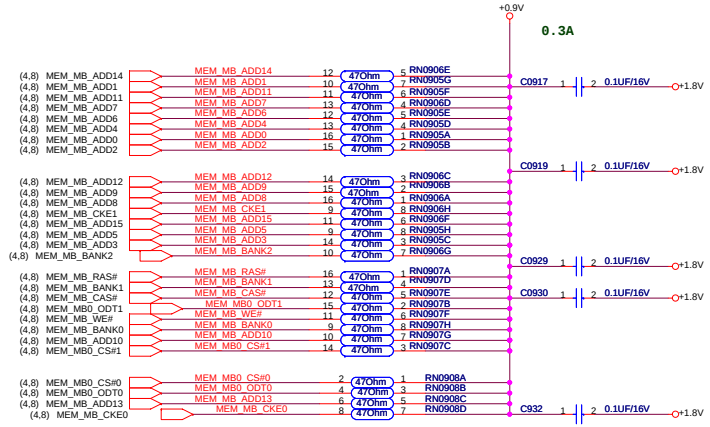


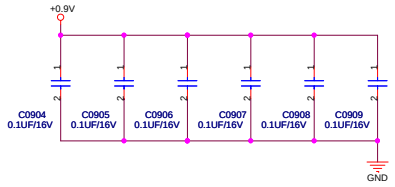


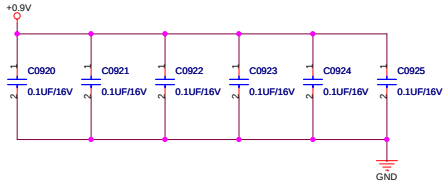
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 8 of 94	

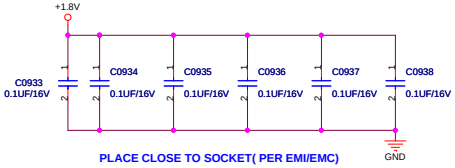


20080803 Remove R907









PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
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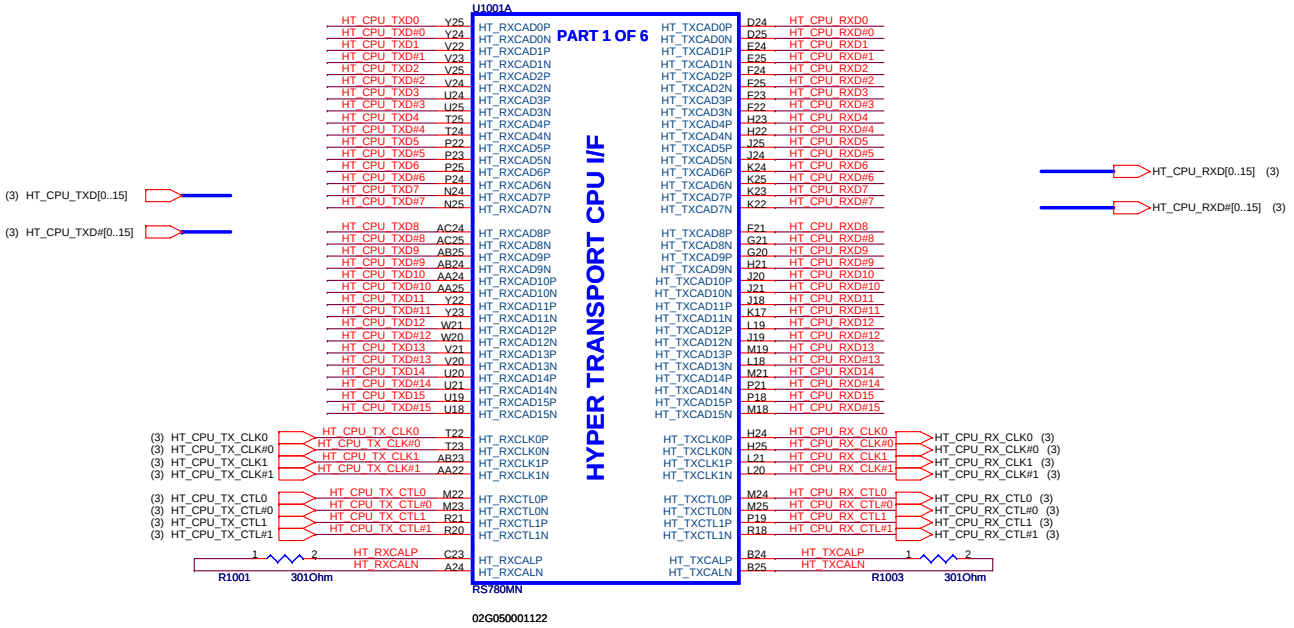
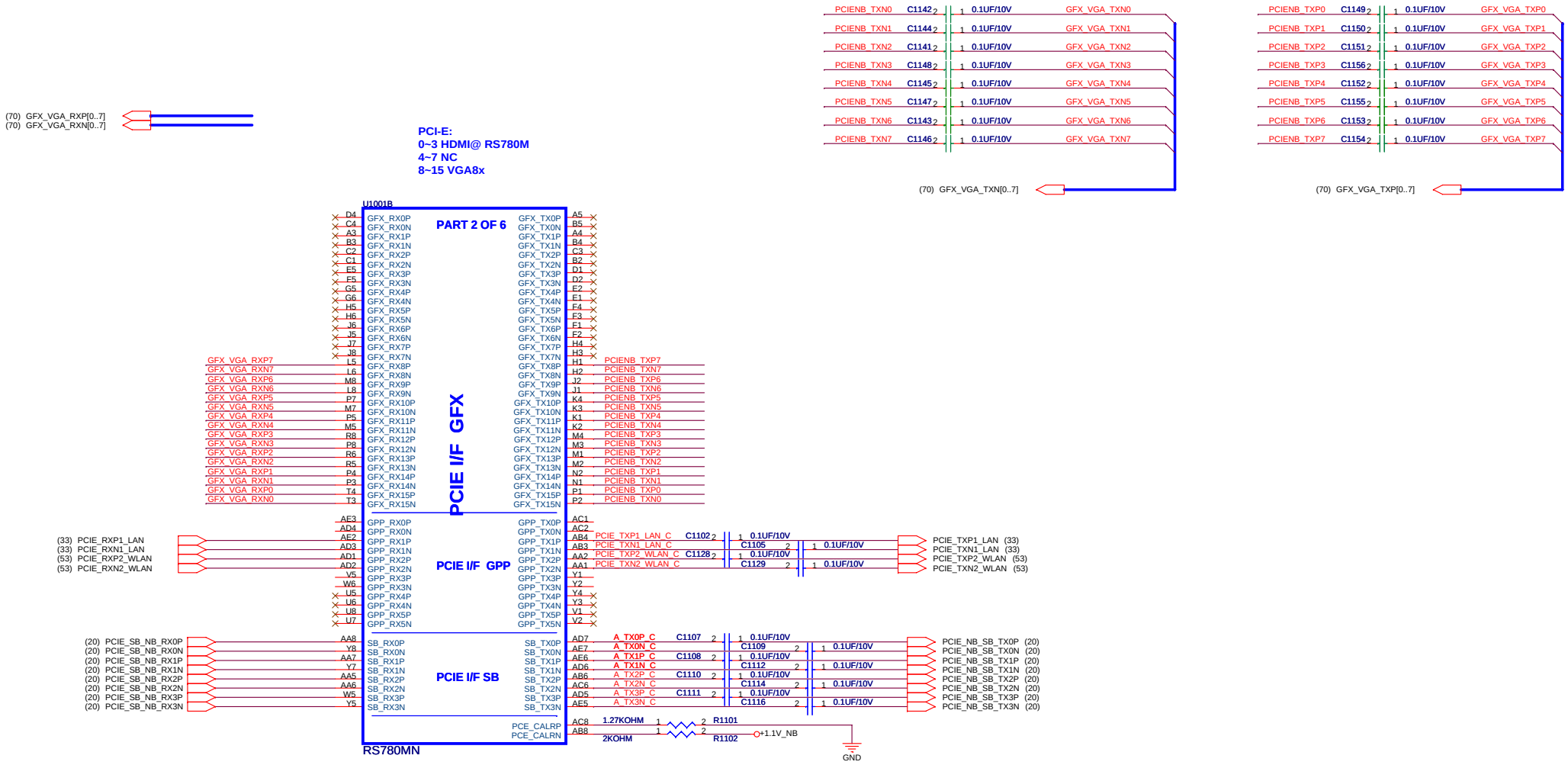
Title : DDR2_TERMINATIONS

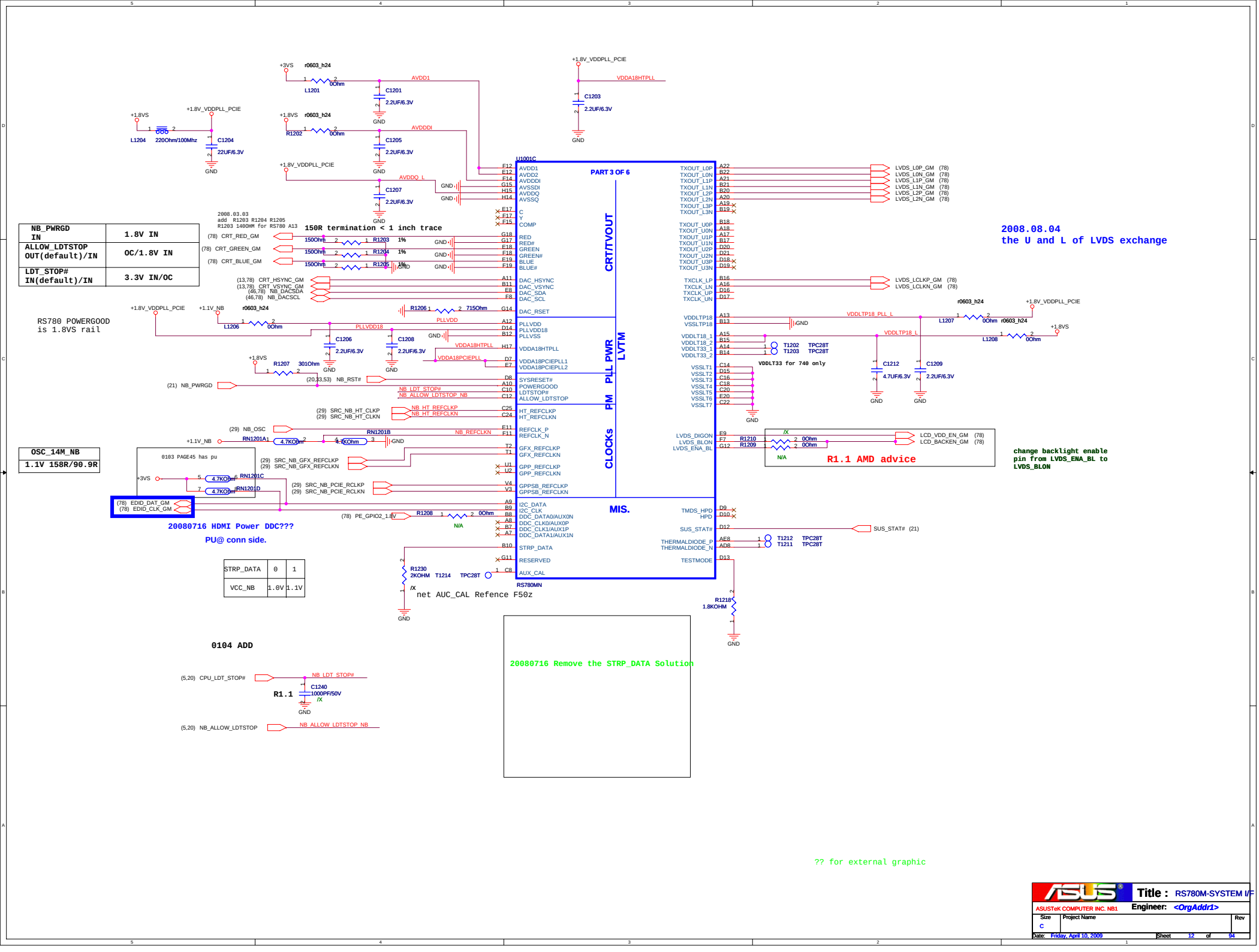


02G050001122

ASUSTeK COMPUTER INC. NB1	Title : RS780M-HT LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 10 of 94	



ASUSTeK COMPUTER INC. NB1	Title : RS780M-PCIE LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name		Rev
Date: Wednesday, April 08, 2009	Sheet 11 of 94		



www.laptop-schematics.com

Title :	RS780M-SYSTEM I/F
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: C	Project Name
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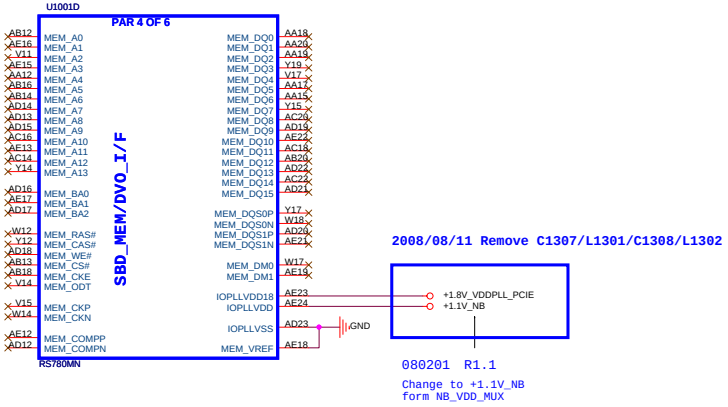
R1.11 080319

Change the NB Part number to RS780 (A13)



2008/08/11 Remove C1307/L1301/C1308/L1302

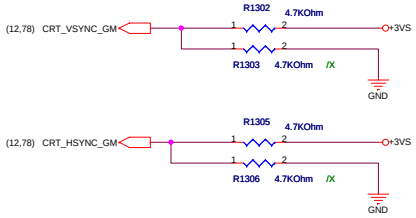
080201 R1.1

Change to +1.1V_NB
form NB_VDD_MUX

080118

Disable Side Port Memory

R1.1



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory

RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

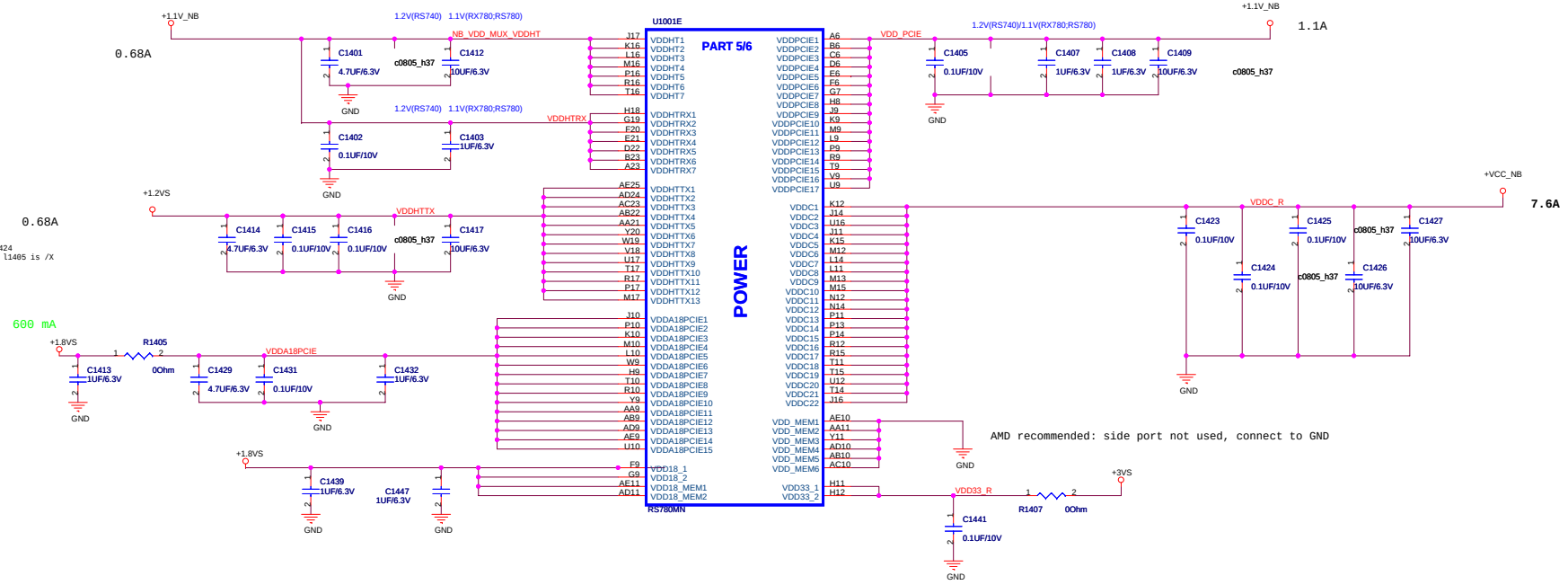
ASUSTeK COMPUTER INC. NB1

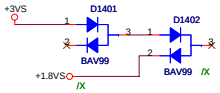
Title : RS780M-SPMEM/STRAPS

Engineer: <OrgAddr1>

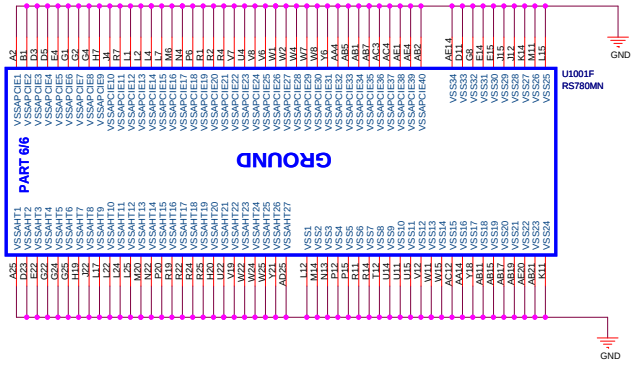
Size: C | Project Name | Rev

Date: Wednesday, April 08, 2009 | Sheet 13 of 94



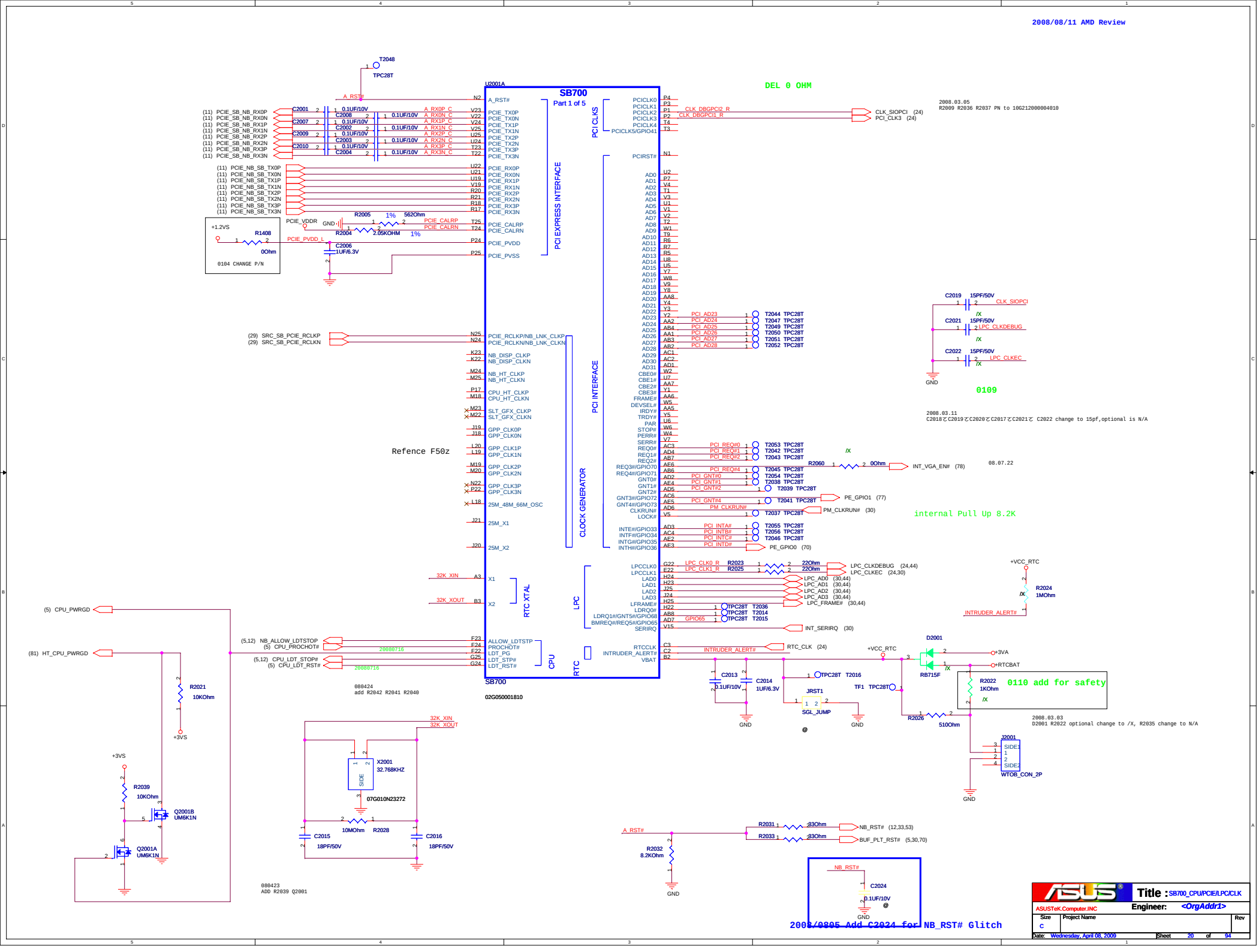


3.3V rails ramp high relative to 1.8V
Display and PLL rails. max 2.1V

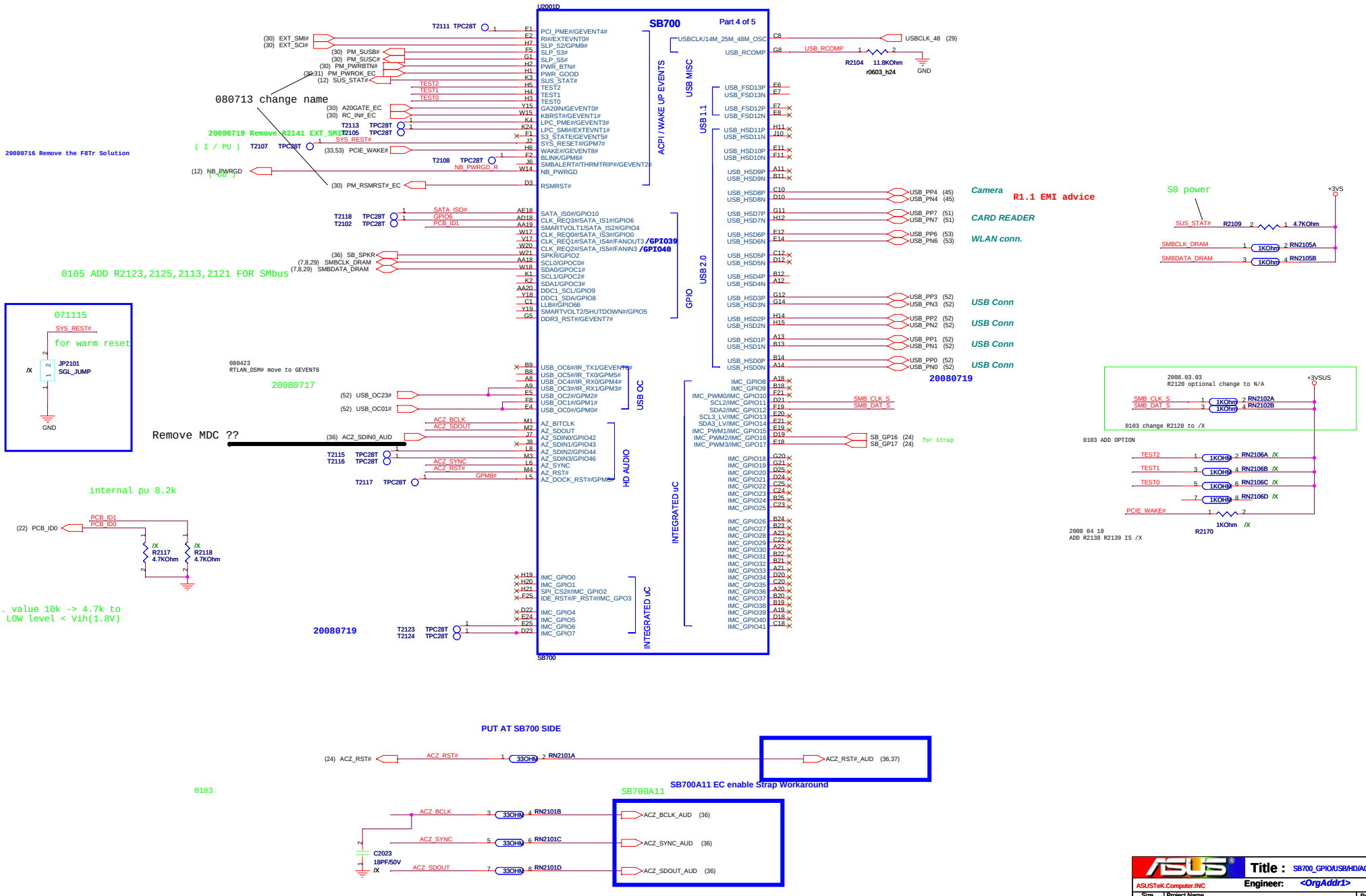


ASUSTeK COMPUTER INC. NB1	Title : RS780M-POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name		Rev
Date: Wednesday, April 08, 2009	Sheet 14 of 94		

2008/08/11 AMD Review



Title :	SB700_CPU/PCIE/LPC/CLK
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>
Size: C	Project Name
Rev	
Date: Wednesday, April 08, 2009	Sheet 20 of 94



ASUSTeK.Computer.INC	Title : SB700_GPIO/USB/HD/ACPI	
	Engineer: <OrgAddr1>	
Size: C	Project Name	Rev
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2008.03.03
R2208 R2209 R2210 R2211 R2212 R2213 from 4.99OHM to 0OHM

2008/08/11 Remove R2208/R2209/R2210/R2211/R2212/R2213

for SATA HDD

(51) SATA_TXP0_HDD
(51) SATA_TXN0_HDD
(51) SATA_RXN0_HDD
(51) SATA_RXP0_HDD

for SATA ODD

(51) SATA_TXP1
(51) SATA_TXN1
(51) SATA_RXN1
(51) SATA_RXP1

U2001B

SB700
Part 2 of 5

SERIAL ATA
SATA_TX0P AD9
SATA_TX0N AE9
SATA_RX0N AB10
SATA_RX0P AC10
SATA_TX1P AE10
SATA_TX1N AD10
SATA_RX1N AD11
SATA_RX1P AE11
SATA_TX2P AB12
SATA_TX2N AC12
SATA_RX2N AE12
SATA_RX2P AD12
SATA_TX3P AD13
SATA_TX3N AE13
SATA_RX3N AB14
SATA_RX3P AC14
SATA_TX4P AE14
SATA_TX4N AD14
SATA_RX4N AD15
SATA_RX4P AE15
SATA_TX5P AB16
SATA_TX5N AC16
SATA_RX5N AE16
SATA_RX5P AD16

ATA 66/100/133
IDE_IORDY AA24
IDE_IRQ AA25
IDE_A0 Y22
IDE_A1 AB23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AD25
IDE_IOR# AC25
IDE_IOW# AC24
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE23
IDE_D3/GPIO18 AC23
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AC20
IDE_D10/GPIO25 AD20
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23

SPI ROM
SPI_DI/GPIO12 G6
SPI_DO/GPIO11 D2
SPI_CLK/GPIO47 D1
SPI_HOLD#/GPIO31 F4
SPI_CS1#/GPIO32 F3
LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1

WLAN_ON (53)

WLAN_ON#----> WLAN_ON

FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7

PCB_ID0 (21)

HW MONITOR
FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6
TEMPIN2/GPIO63 A5
TEMPIN3/TALERT#/GPIO64 B5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7

GPIO61 T2228 TPC28T
TEMPIN_NB R2218 0Qhm
GPIO62 T2229 TPC28T
GPIO63 T2231 TPC28T /X
OS#_OC (30,50)
GPIO53 T2232 TPC28T
GPIO54
L_ISOLATE# (33)
WLAN_LED_ON (56)

SATA PWR
SATA_ACT#/GPIO67 W11
PLLVDD_SATA AA11
XTLVDD_SATA W12

SATA_CAL V12
SATA_X1 Y12
SATA_X2 AA12

AVDD F6
AVSS G7

SB700

Place SATA_CAL
RES very close
to ball of SB700

GND
R2201 1KOhm 1% 1% SATA_CAL
SATA_X1
R2205 10MOhm
SATA_X2
(31) SATA_LED#
X2201 25Mhz
PLLVDD_SATA
XTLVDD_SATA
C2209 27PF/50V N/A
C2210 27PF/50V N/A
GND

+1.2VS
+1.2VS_SATA
R2207 0Ohm
R2250 0Ohm /X
PLLVDD_SATA
C2211 1UF/10V
C2213 0.1UF/10V
R1.1

080423
C2211 C2212 TO 2.2U(0603)

+3VS
XTLVDD_SATA
C2217 0.1UF/10V
C2216 close
to the ball
of SB700

AVDD_HWM
+3VSUS
C2214 0.1UF/16V
/X
GND

GND trace at
least 10mil
wide

GPIO54:BIOS default
設爲GPI,disable LAN
設爲低電平！

WLAN_LED_ON
R2202 10KOhm
GND

TEMP_COMM
GND

ASUSTeK.Computer.INC	Title : SB700_PATA/SATA	
	Engineer: <OrgAddr1>	
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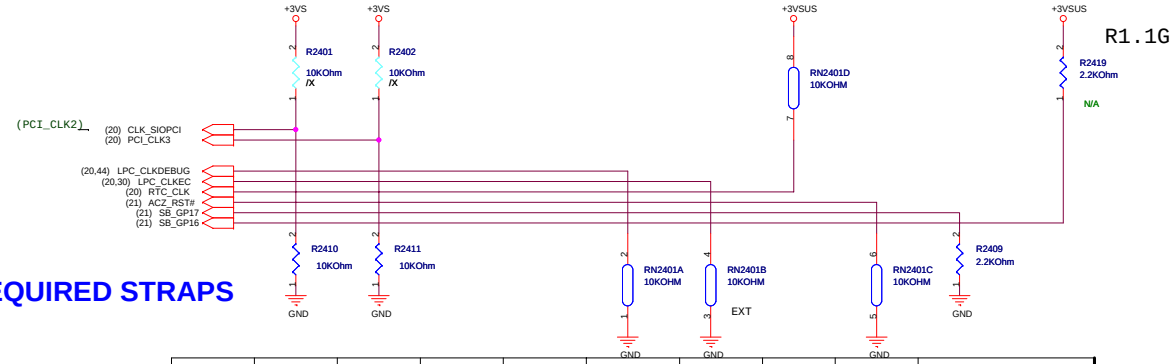
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEBUG	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	32-kHz clock ENABLED	INTERNAL RTC DEFAULT	Integrated Microcontroller ENABLED	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	32-kHz clock DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	Integrated Microcontroller DISABLED DEFAULT	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

ASUSTeK.Computer.INC
Title : SB700_STRAP
Engineer: <OrgAddr1>
Size: C
Project Name
Rev
Date: Wednesday, April 08, 2009
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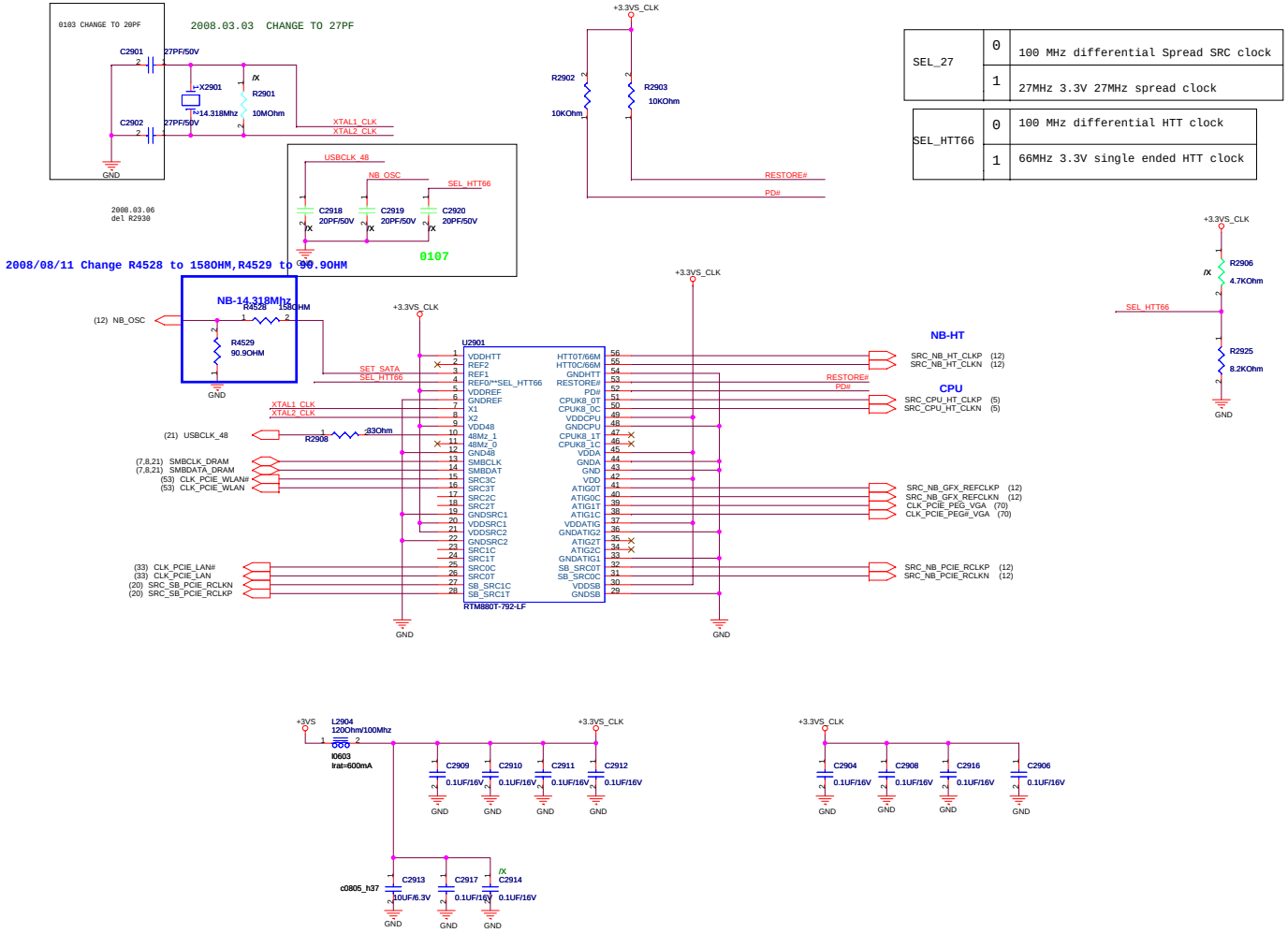

SEL_27		
	0	100 MHz differential Spread SRC clock
	1	27MHz 3.3V 27MHz spread clock

SEL_HTT66		
	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

<Variant Name>

ASUSTeK COMPUTER INC

Title : ICS9LPRS489AGLFT

Engineer:

Size	Project Name	Rev
A2		

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R2.05

Change RNX3001 from 47 ohm to 0 ohm .The RNX3001 with modification of RN4401 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

080131 R1.1
Check EC power

080130
R1.1
Change EC from IT8752 to IT8512

U3001 IT8512E-L

080712

080712 Internet

Batt1

Thermal sensor

R2.0 080401
Un-mount C3018 for ITE suggestion

080204 R1.1
IT8512 I~J

For IT8512 Power

R2.0 080327
Add test point for factory ICT test

R2.01 080411
Change P/N to 09G013120103

For PU / PD

080215 R1.1
change 4.7K P/N from 10G2124720040 to 10G2124720040

071115
Change pull up resistor from 10K to 47K ohm

R1.1G

080215 change P/N

For EC Reset

Note: close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R2.0 080327
Follow the design IP

For Instant Key

Note: Close to EC

080713 Add Coloren#

For X'tal

Note: Cload=12.5PF place close to EC

For EC Hardware Strap

I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

071116
Reserve for current leakage issue (Reference to F5R)

R3008 33Ohm
R3010 33Ohm

071129

R2.02 080519
Un-Mount R3059 and Q3002 for cost down

071207
AMD review

080713 ?????

EC Check (AC Auto Boot Issue)

071113
Change Net name from PM_RSMRST#

080123 R1.1

071113
Change Net name from PM_RSMRST#_EC

071113
Change Net name from PM_PWROK

071203
refer page31.

071113
Change Net name from PM_PWROK_EC

071116
Reserve "Auto power on" solution for ATI Chipset

ASUSTeK COMPUTER INC. NB1

Title : EC_IT8512 (1/2)

Engineer: <OrgAddr1>

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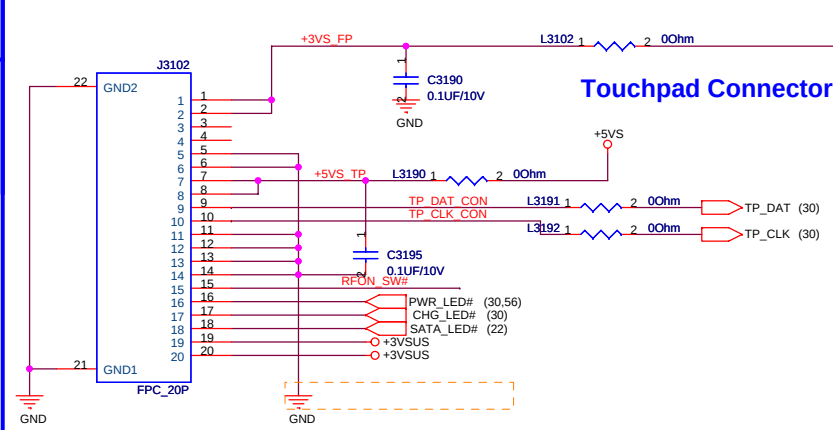
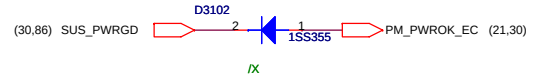
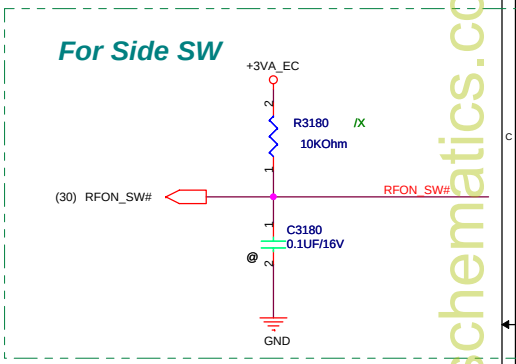




12G09103004P



close to connector

Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

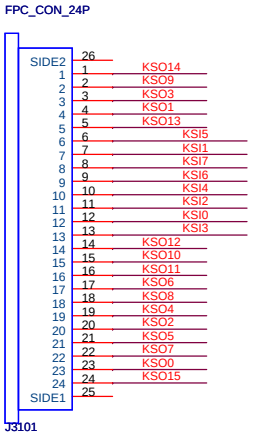
Keyboard Connector

KSO[15:0] (30)

KSI[7:0] (30)

F7/N1 Keyboard

R1.1G



12G182102402

11/02

ASUSTeK COMPUTER INC. NB1

Title : EC_IT8512 (2/2)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

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Title : POWER-ON SEQUENCE

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

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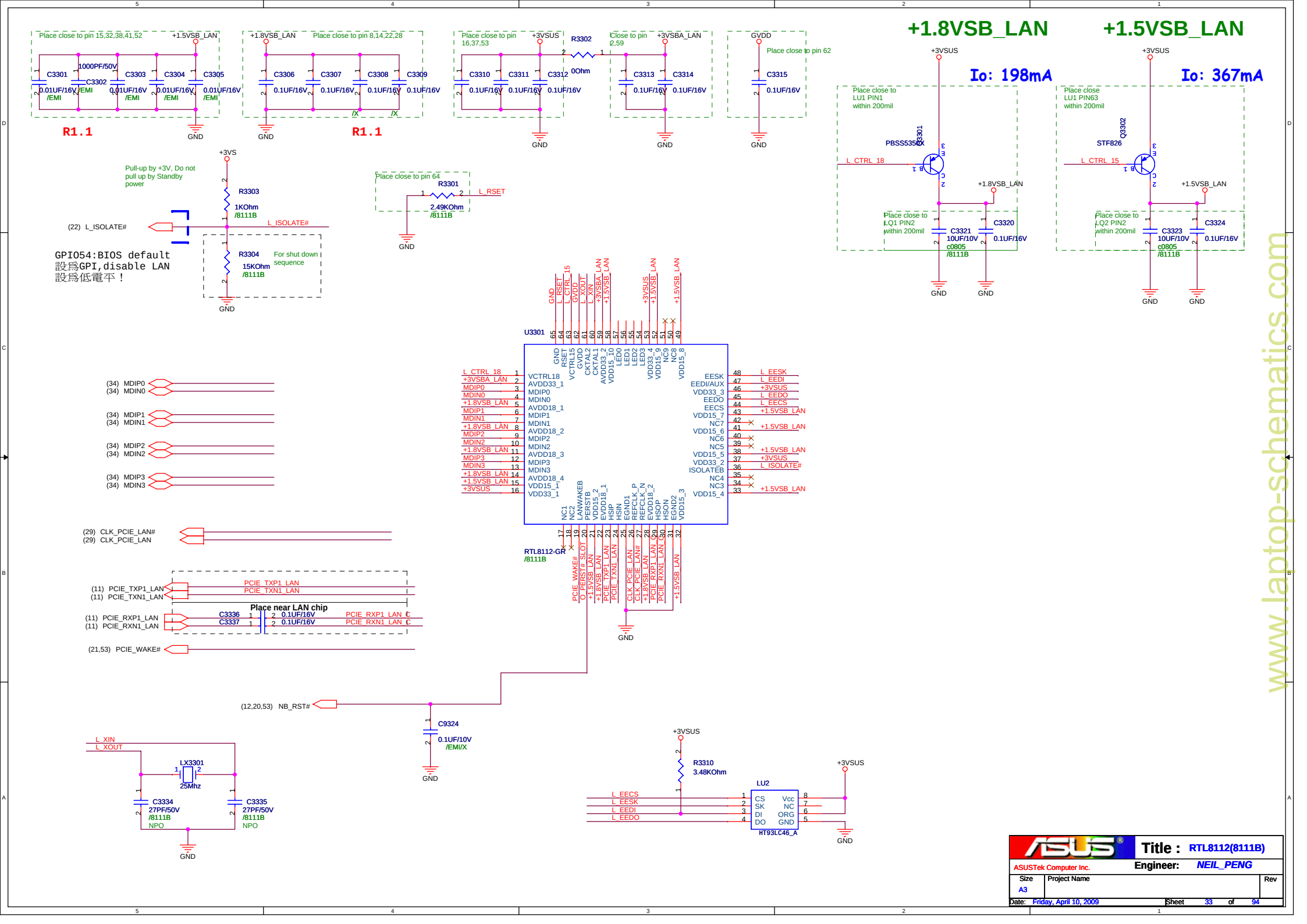
+1.8VSB_LAN
+1.5VSB_LAN
Io: 198mA
Io: 367mA
Place close to pin 15,32,38,41,52
Place close to pin 8,14,22,28
Place close to pin 16,37,53
Close to pin 2,59
Place close to pin 62
R1.1
R1.1
R3302
0Ohm
GPIO54:BIOS default
設爲GPI,disable LAN
設爲低電平！
Pull-up by +3V, Do not pull up by Standby power
R3303
1KOhm
/8111B
R3304
15KOhm
/8111B
For shut down sequence
Place close to pin 64
R3301
2.49KOhm
/8111B
L_RSET
L_ISOLATE#
Place close to LU1 PIN1 within 200mil
Place close to LU1 PIN63 within 200mil
Q3301
PBSS5350X
Q3302
STF826
L_CTRL_18
L_CTRL_15
Place close to LQ1 PIN2 within 200mil
Place close to LQ2 PIN2 within 200mil
C3321
10UF/10V
c0805
/8111B
C3320
0.1UF/16V
C3323
10UF/10V
c0805
/8111B
C3324
0.1UF/16V
U3301
RTL8112-GR
/8111B
Place near LAN chip
C9324
0.1UF/10V
/EMI/X
LX3301
25Mhz
C3334
27PF/50V
/8111B
NPO
C3335
27PF/50V
/8111B
NPO
R3310
3.48KOhm
LU2
HT93LC46_A
www.laptop-schematics.com
Title : RTL8112(8111B)
ASUSTek Computer Inc.
Engineer: NEIL_PENG
Size A3
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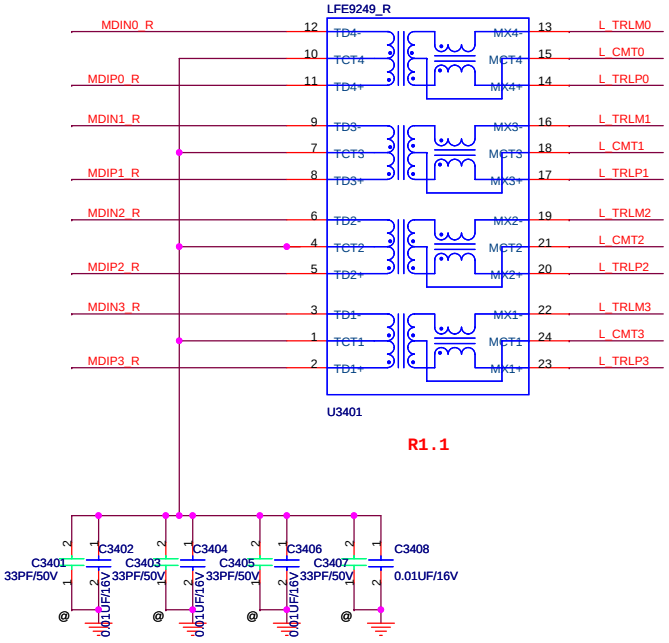
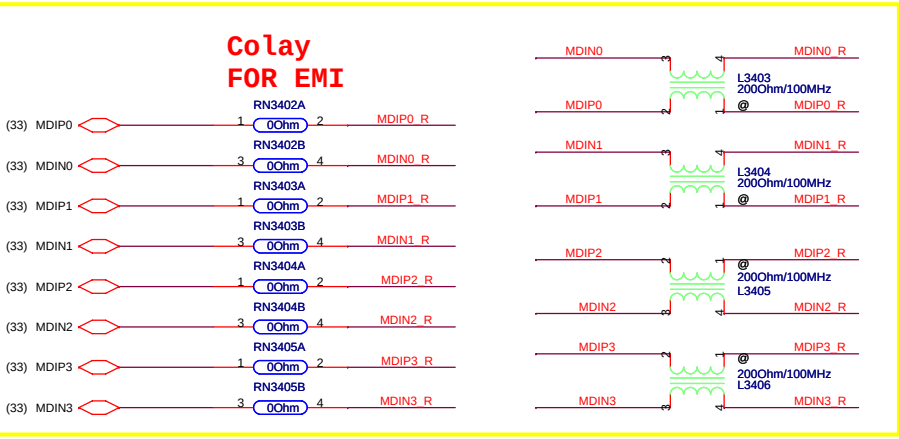
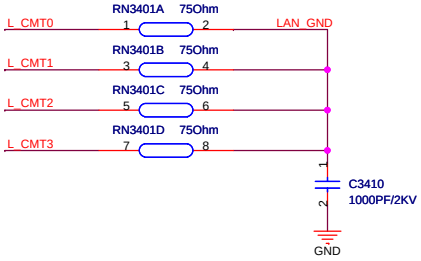
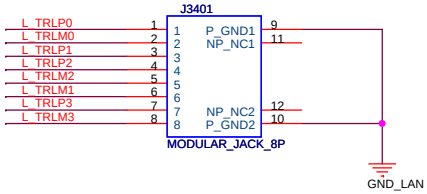
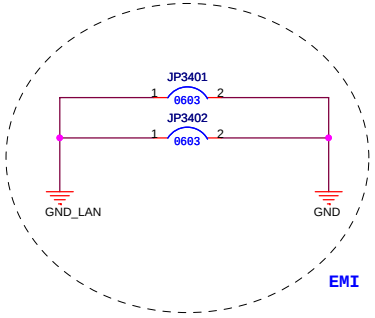


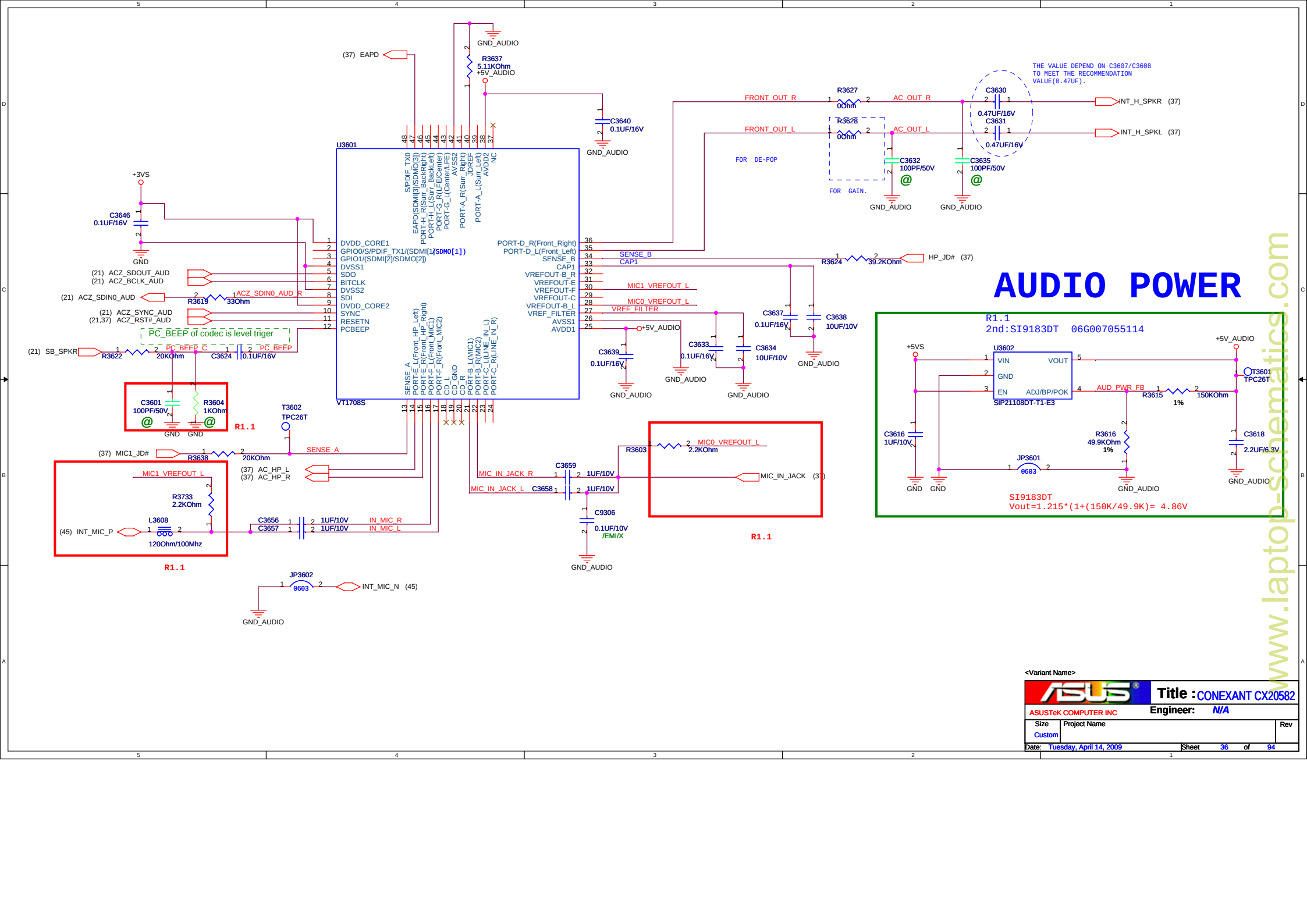




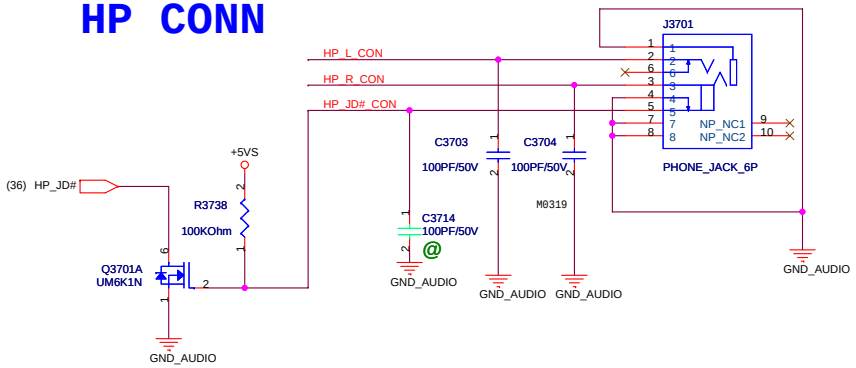




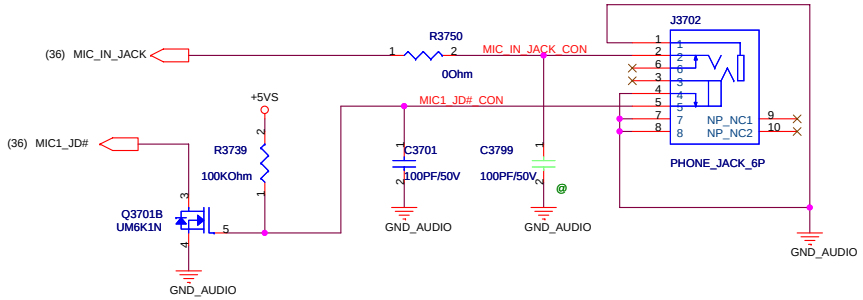
ASUSTeK COMPUTER INC. NB1	Title : RJ45	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 34 of 94	


AUDIO POWER
U3601
VT1708S
DVDD_CORE1
GPIO0/S/PDIF_TX1/(SDMI[1]/SDMO[1])
GPIO1/(SDMI[2]/SDMO[2])
DVSS1
SDO
BITCLK
DVSS2
SDI
DVDD_CORE2
SYNC
RESETN
PCBEEP
SPDIF_TX0
EAPD(SDMI[3]/SDMO[3])
PORT-H_R(Surr_Back(Right))
PORT-H_L(Surr_Back(Left))
PORT-G_R(LFE/Center)
PORT-G_L(Center/LFE)
AVSS2
PORT-A_R(Surr_Right)
JDREF
PORT-A_L(Surr_Left)
AVDD2
NC
PORT-D_R(Front_Right)
PORT-D_L(Front_Left)
SENSE_B
CAP1
VREFOUT-B_R
VREFOUT-E
VREFOUT-F
VREFOUT-C
VREFOUT-B_L
VREF_FILTER
AVSS1
AVDD1
SENSE_A
PORT-E_L(Front_HP_Left)
PORT-E_R(Front_HP_Right)
PORT-F_L(Front_MIC1)
PORT-F_R(Front_MIC2)
CD_L
CD_GND
CD_R
PORT-B_L(MIC1)
PORT-B_R(MIC2)
PORT-C_L(LINE_IN_L)
PORT-C_R(LINE_IN_R)
(37) EAPD
GND_AUDIO
R3637 5.11KOhm +5V_AUDIO
C3640 0.1UF/16V
+3VS
C3646 0.1UF/16V
GND
(21) ACZ_SDOUT_AUD
(21) ACZ_BCLK_AUD
(21) ACZ_SDIN0_AUD
ACZ_SDIN0_AUD_R
R3619 33Ohm
(21) ACZ_SYNC_AUD
(21,37) ACZ_RST#_AUD
PC_BEEP of codec is level triger
(21) SB_SPKR
R3622 20KOhm
PC_BEEP_C
C3624 0.1UF/16V
PC_BEEP
C3601 100PF/50V @
R3604 1KOhm @
R1.1
T3602 TPC26T
(37) MIC1_JD#
R3638 20KOhm
SENSE_A
(37) AC_HP_L
(37) AC_HP_R
MIC1_VREFOUT_L
R3733 2.2KOhm
L3608 120Ohm/100Mhz
(45) INT_MIC_P
C3656 1UF/10V
C3657 1UF/10V
IN_MIC_R
IN_MIC_L
R1.1
JP3602 0603
INT_MIC_N (45)
GND_AUDIO
FRONT_OUT_R
FRONT_OUT_L
R3627 0Ohm
R3628 0Ohm
AC_OUT_R
AC_OUT_L
FOR DE-POP
FOR GAIN.
C3632 100PF/50V @
C3635 100PF/50V @
C3630 0.47UF/16V
C3631 0.47UF/16V
THE VALUE DEPEND ON C3607/C3608
TO MEET THE RECOMMENDATION
VALUE(0.47UF).
INT_H_SPKR (37)
INT_H_SPKL (37)
SENSE_B
CAP1
R3624 39.2KOhm
HP_JD# (37)
MIC1_VREFOUT_L
MIC0_VREFOUT_L
VREF_FILTER
+5V_AUDIO
C3639 0.1UF/16V
C3633 0.1UF/16V
C3634 10UF/10V
C3637 0.1UF/16V
C3638 10UF/10V
MIC_IN_JACK_R
MIC_IN_JACK_L
C3658
C3659 1UF/10V
1UF/10V
R3603 2.2KOhm
MIC0_VREFOUT_L
MIC_IN_JACK (37)
C9306 0.1UF/10V /EMI/X
R1.1
R1.1
2nd:SI9183DT 06G007055114
+5VS
U3602
VIN
VOUT
GND
EN
ADJ/BP/POK
SIP21108DT-T1-E3
AUD_PWR_FB
R3615 150KOhm 1%
T3601 TPC26T
C3616 1UF/10V
R3616 49.9KOhm 1%
JP3601 0603
C3618 2.2UF/6.3V
SI9183DT
Vout=1.215*(1+(150K/49.9K)= 4.86V
www.laptop-schematics.com
<Variant Name>
Title : CONEXANT CX20582
ASUSTeK COMPUTER INC
Engineer: N/A
Size Custom
Project Name
Rev
Date: Tuesday, April 14, 2009
Sheet 36 of 94

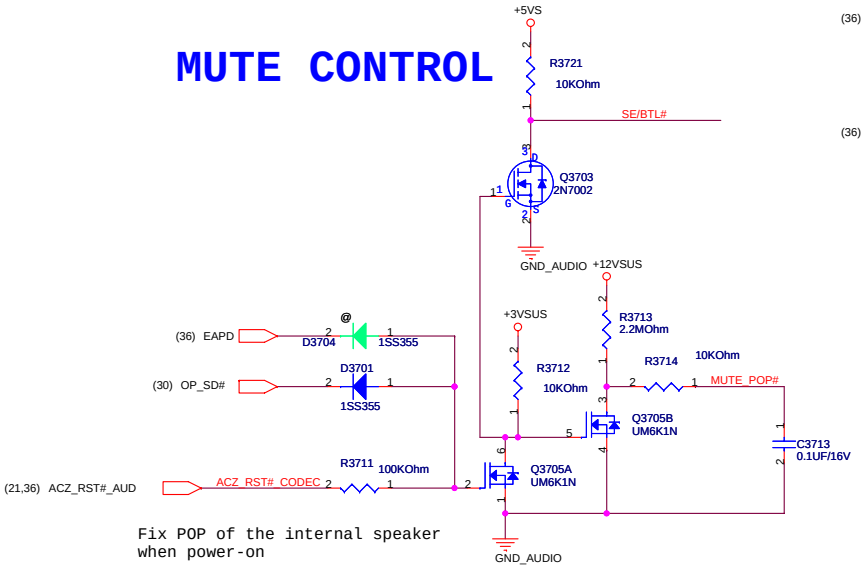
HP CONN

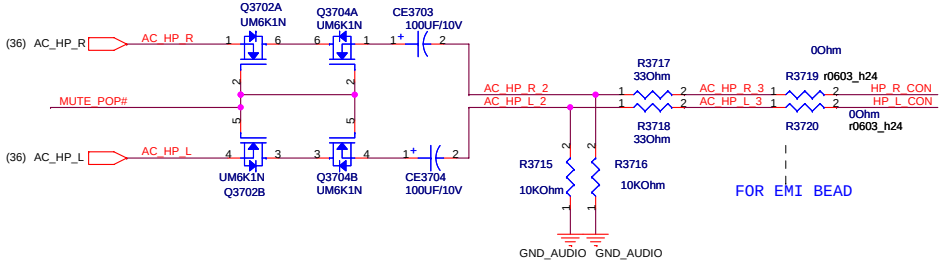


External MIC CONN

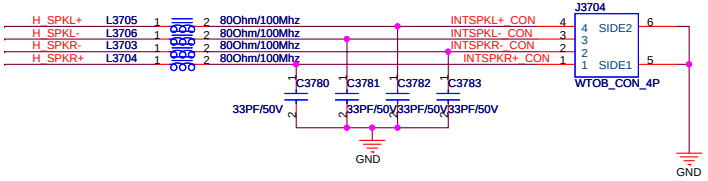


MUTE CONTROL



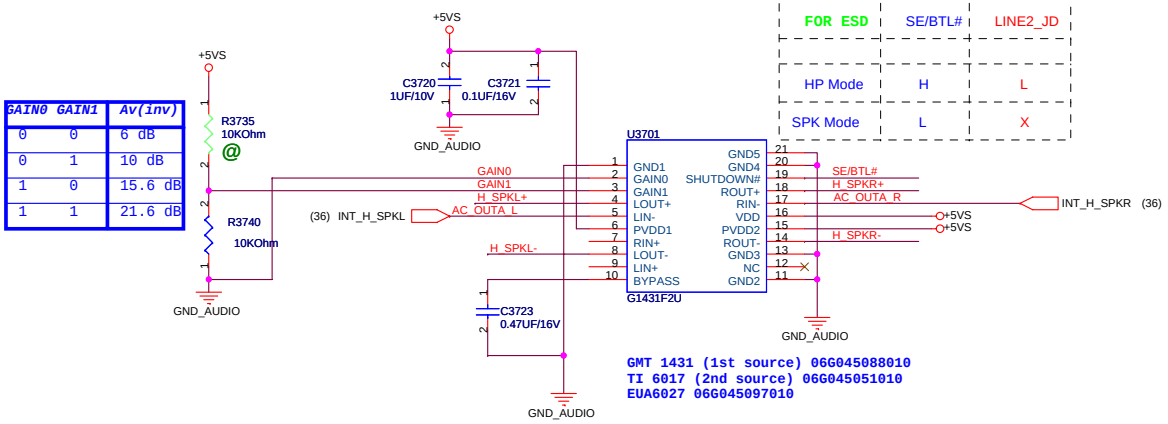


SPEAKER CONNECTOR(2W)

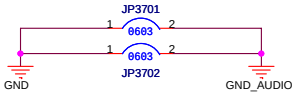


SPEAKER AMP

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



FOR ESD	SE/BTL#	LINE2_JD
HP Mode	H	L
SPK Mode	L	X



GMT 1431 (1st source) 06G045088010
TI 6017 (2nd source) 06G045051010
EUA6027 06G045097010

ASUSTeK COMPUTER INC. NB1

Title : AUDIO HP/MIC

Engineer: N/A

Size	Project Name	Rev
Custom		

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Title : MIC&LINEIN

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom		

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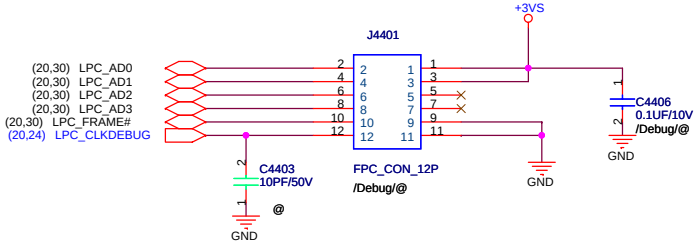


If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

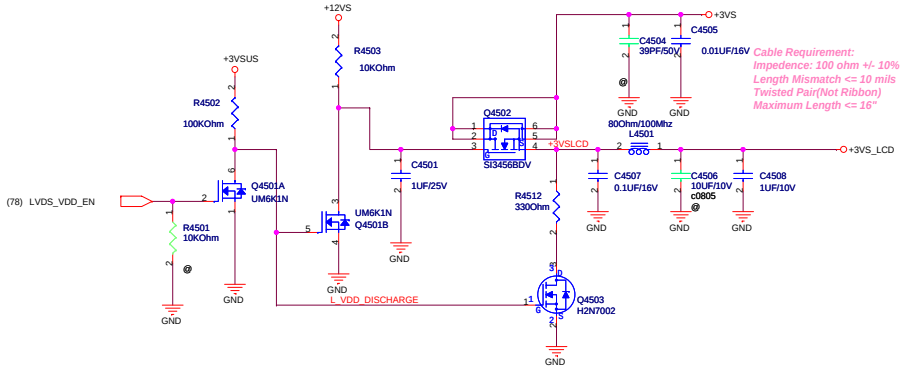
For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

ASUSTeK COMPUTER INC. NB1	Title : DEBUG	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 44 of 94	

LCD Backlight Control

LCD Power



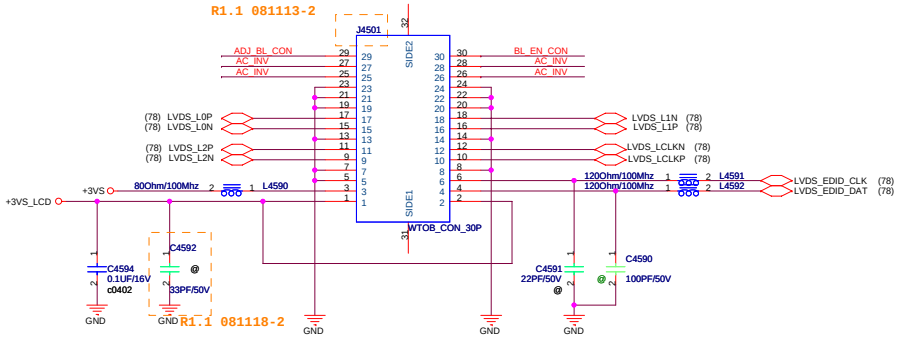
LVDS_LCLKN — C4502 10PF/50V N/A — LVDS_LCLKP

11/19

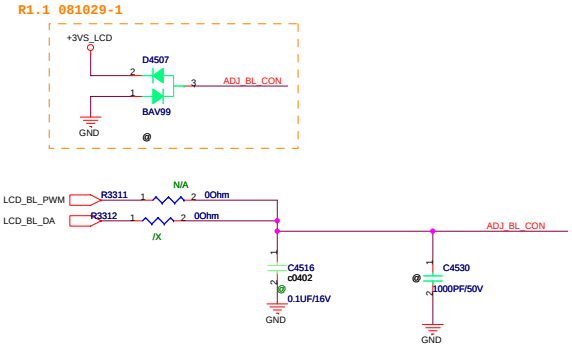
11/19

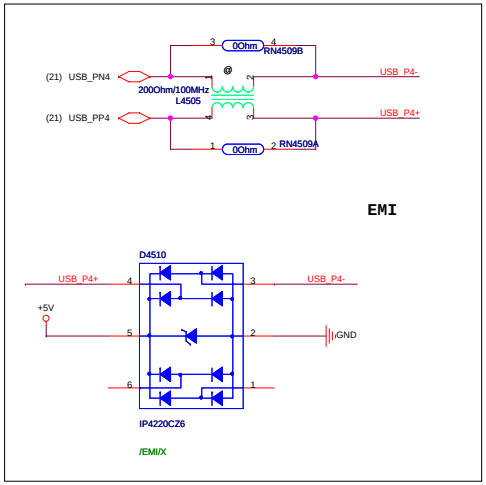
check

LED PANEL LVDS Interface

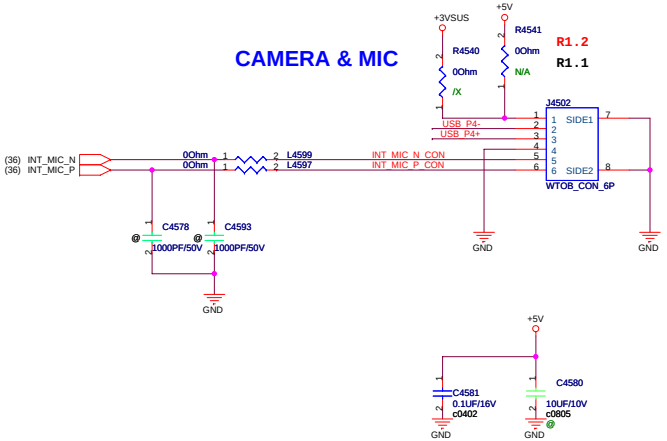


INVERTER
Interface/Speaker CONN.

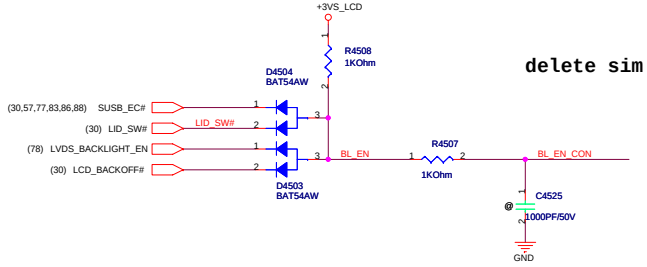




CAMERA & MIC

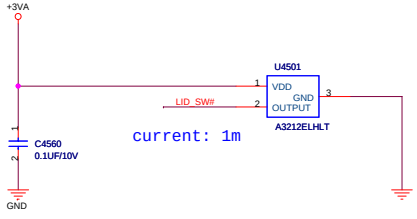


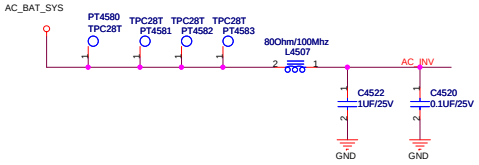
delete sim card function 20080804



Hall effect switch

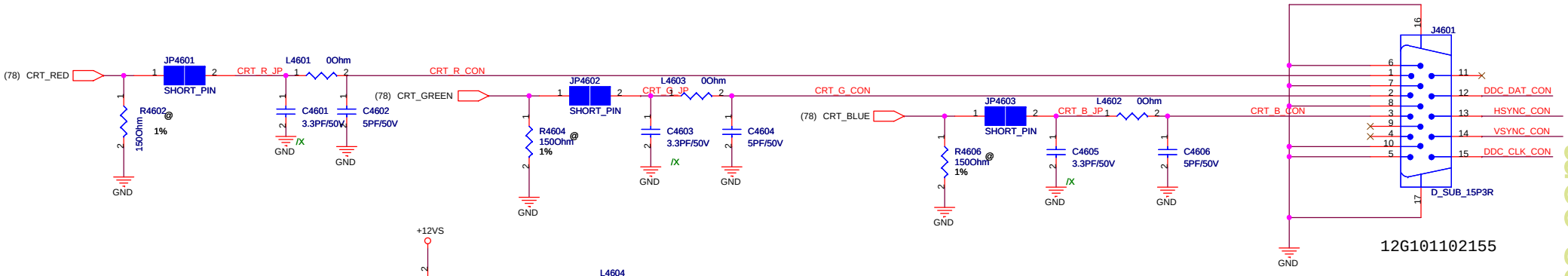
current: 2m



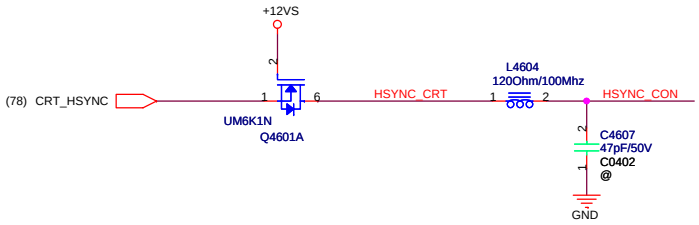


ASUSTeK COMPUTER INC. NB1	Title: LVDS & Inverter CON	
	Engineer: <OrgAddr1>	
Size: C	Project Name	Rev
Date: Thursday, April 09, 2009	Sheet 45 of 94	

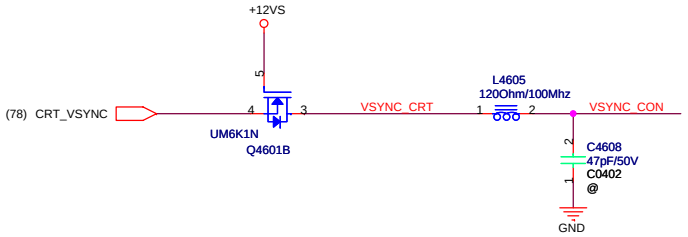
R1.1　VGA部分調整：L4601、L4602、L4603調成0 ohm，C4601、C4603、C4605改爲"/X", C4602、C4604、C4606改成5PF.

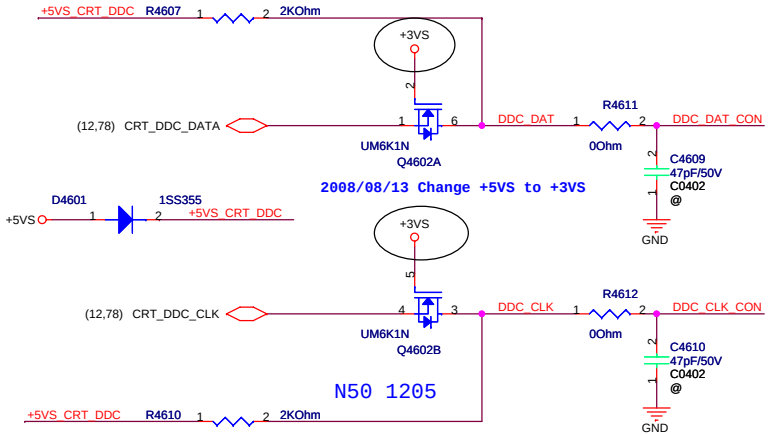


12G101102155

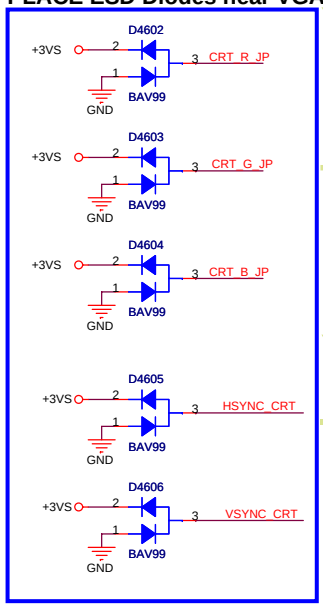


2008/0807 Remove U4601/U4602



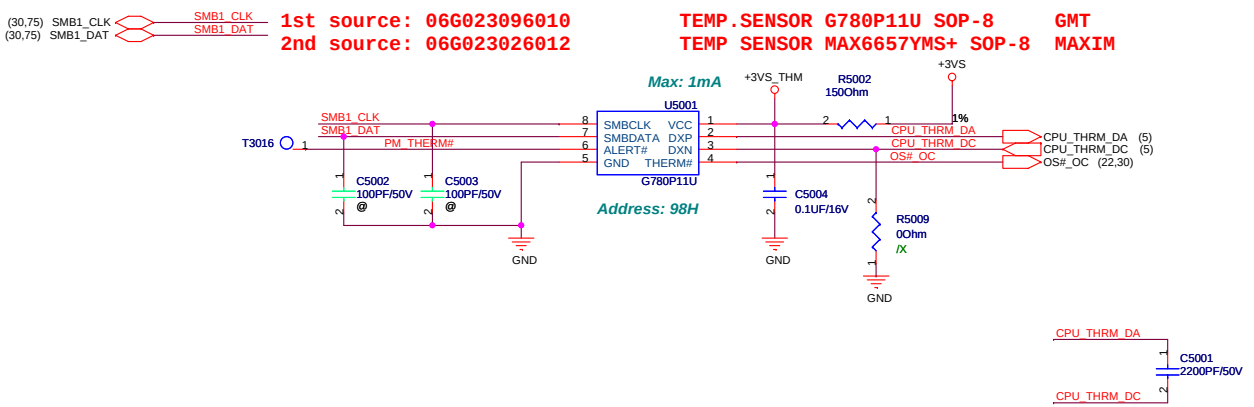


PLACE ESD Diodes near VGA port

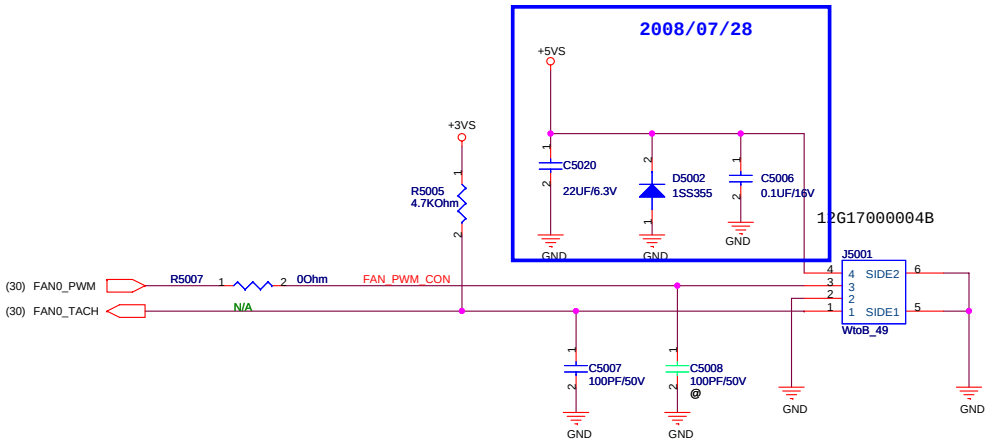


ASUSTeK COMPUTER INC. NB1	Title : CRT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 46 of 94	

Thermal Sensor



DC FAN Control



ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
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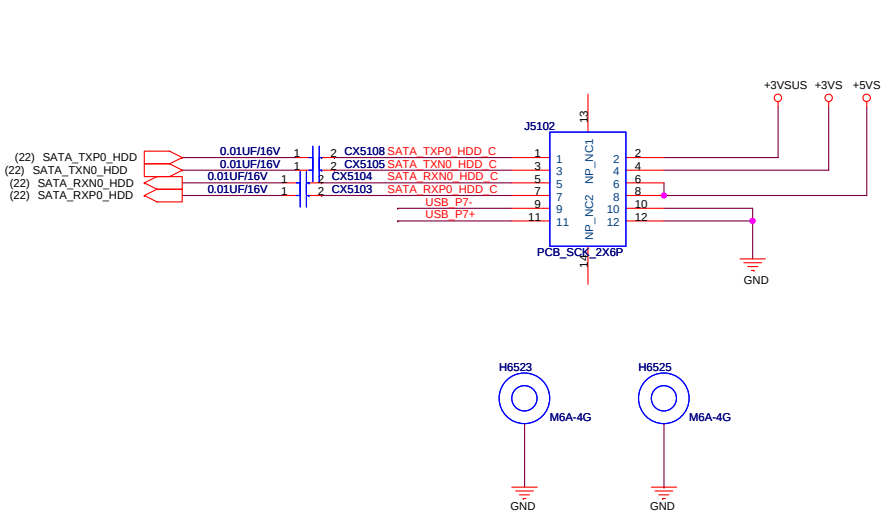
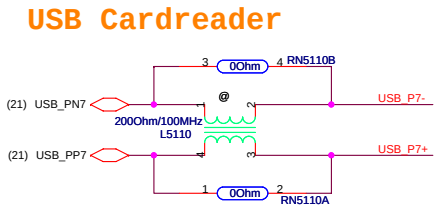
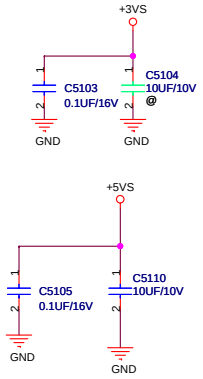
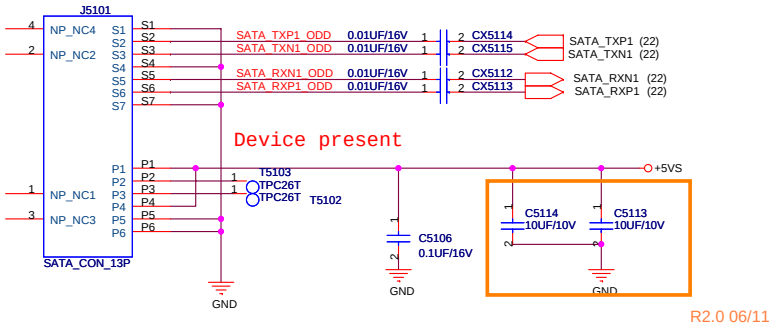
SATA HDD







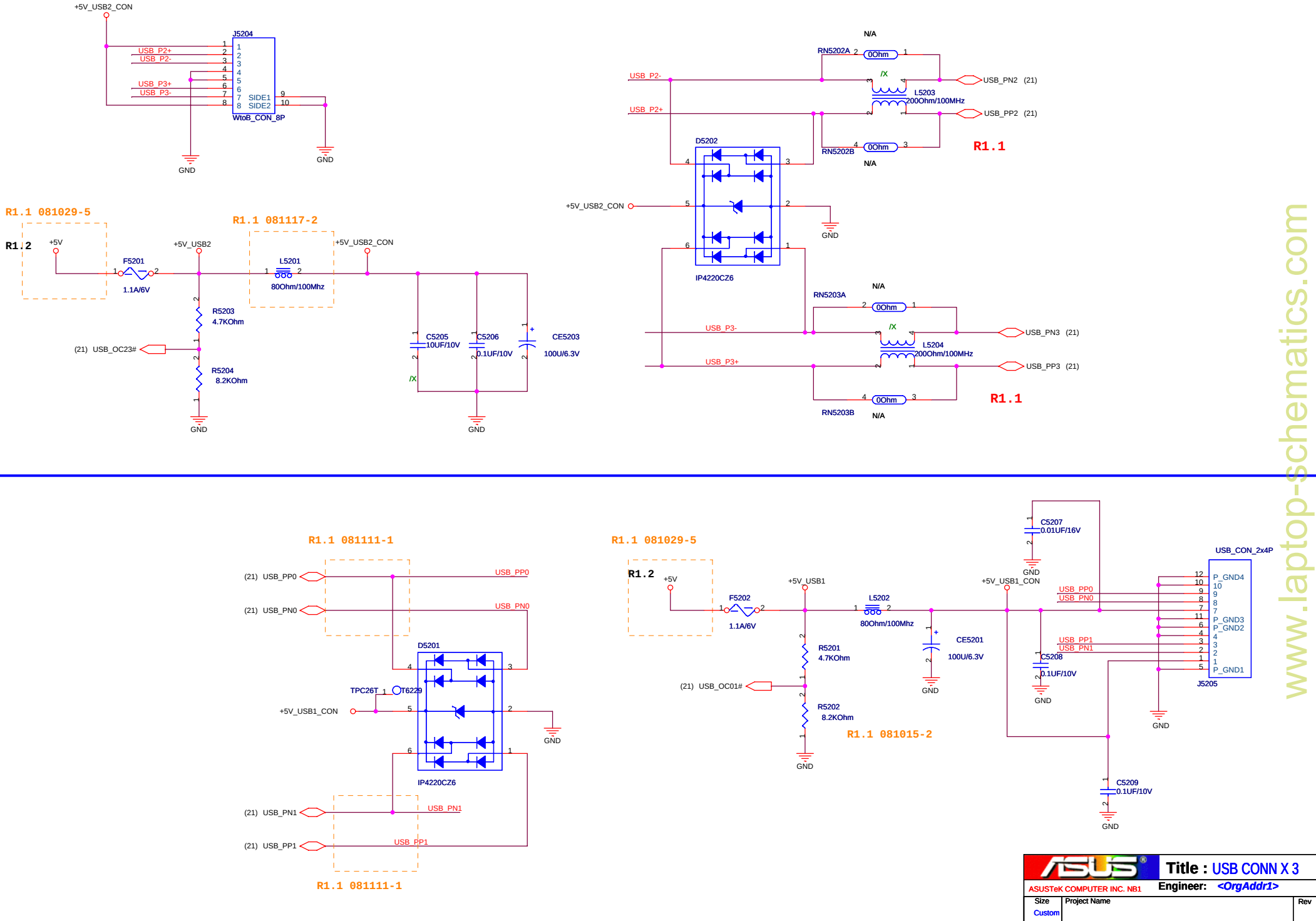
ODD



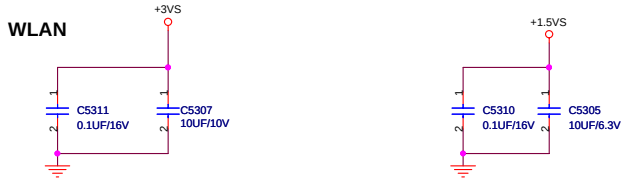
R2.0 06/11

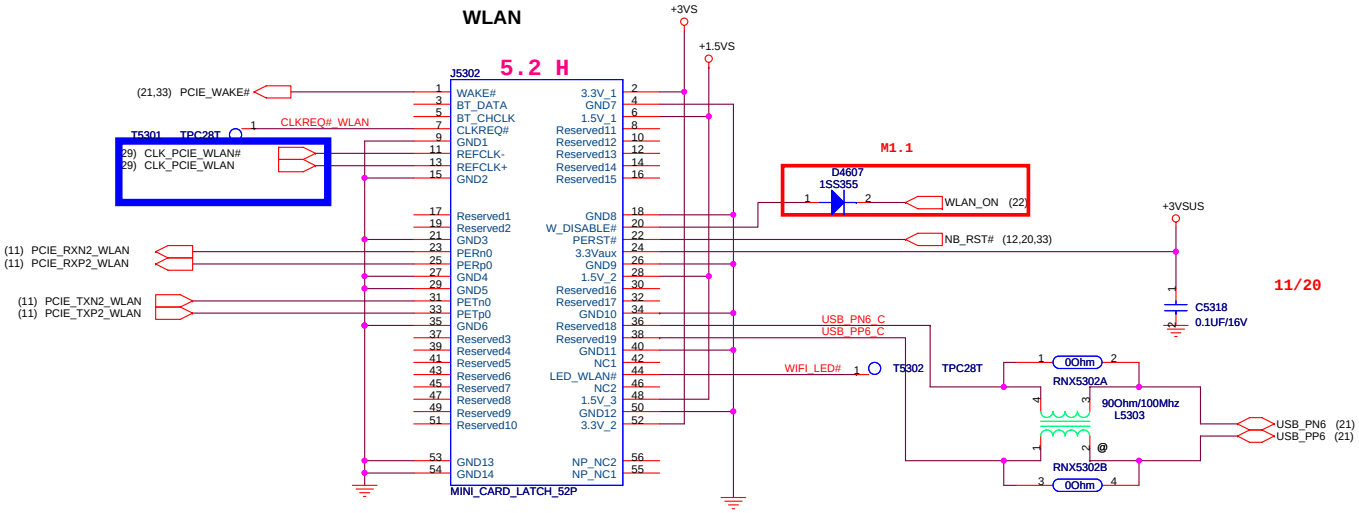
ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 51 of 94	

USB IO Board



ASUSTeK COMPUTER INC. NB1	Title : USB CONN X 3	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 52 of 94	

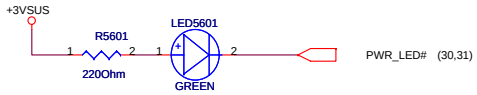




ASUSTeK COMPUTER INC. NB1	Title : Minicard card & Nut	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 53 of 94	

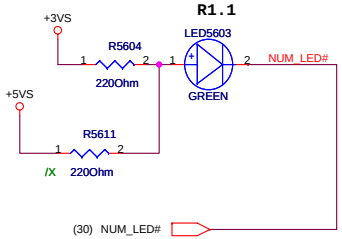
For Power LED

3/13 Orange

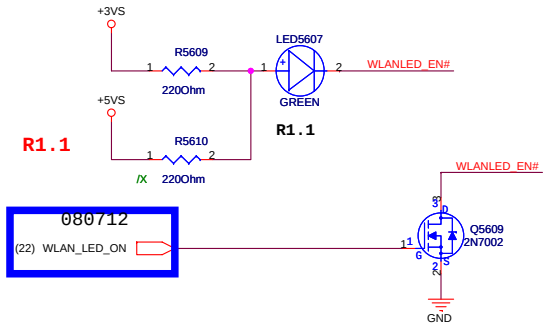


R1.1

For Number Lock

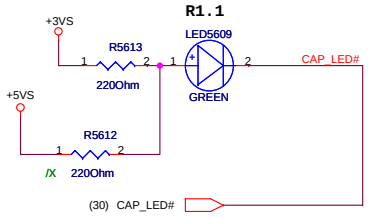


For WireLess LED

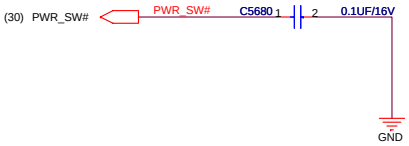


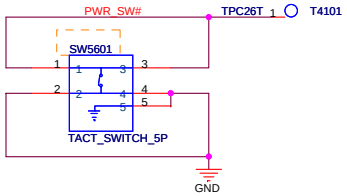
2008/07/30 Remove 3G Function

For Caps. Lock



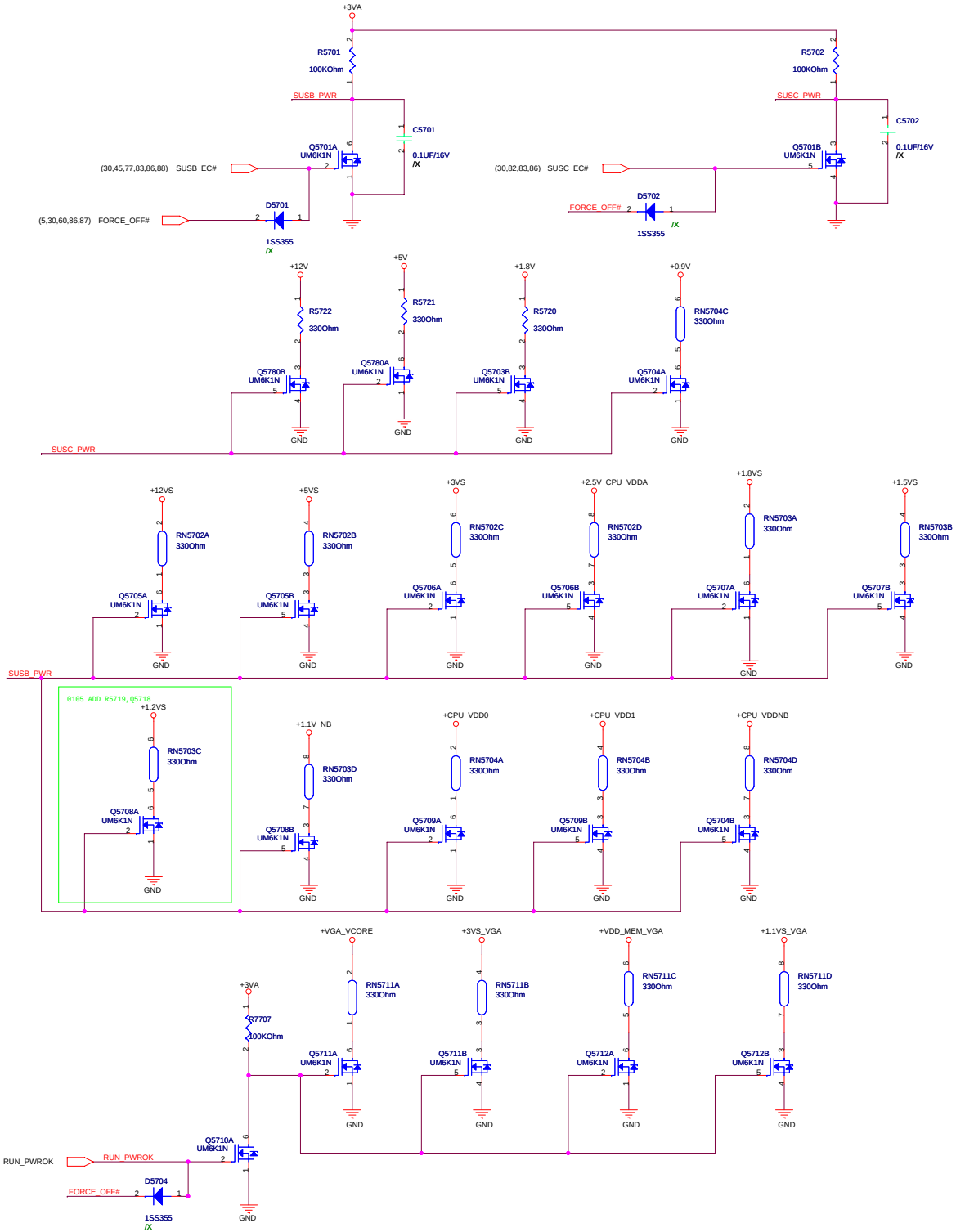
SW





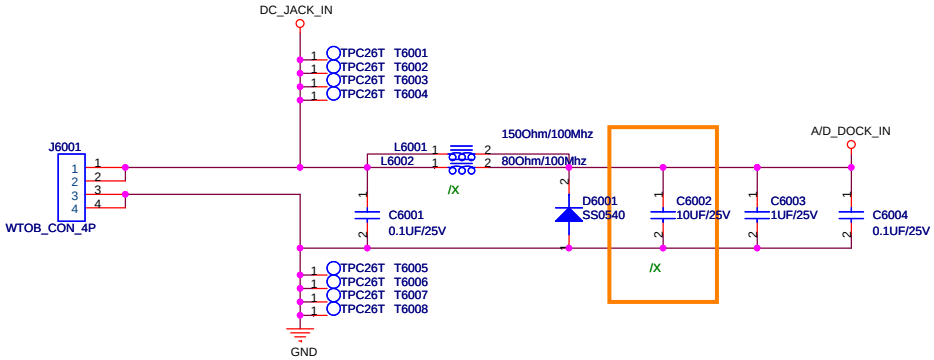
SHUT_DOWN#

ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 56 of 94	

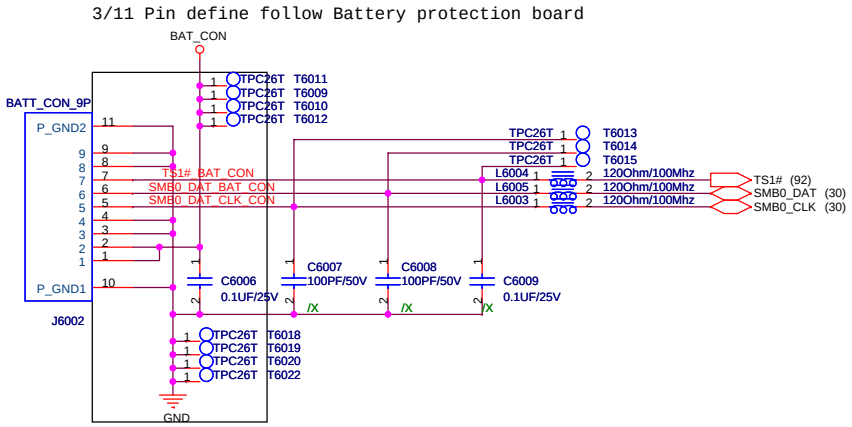


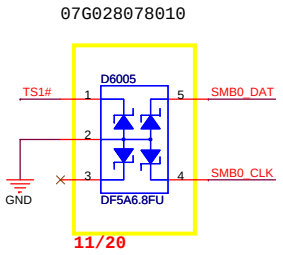
ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 57 of 94	

DC IN

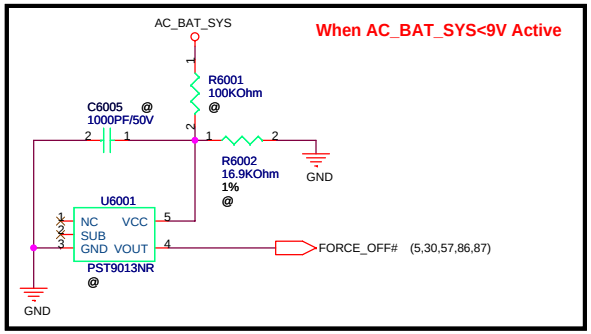


BAT IN





Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
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Hole-A

H6501
HOLE_NPTH

Hole-B

H6502
HOLE_NPTH

H6503
HOLE_NPTH

H6504
HOLE_NPTH

Hole-C

H6505
O83X71DO83X71N

Spring

S6501
EMI_SPRING_PAD
/X
GND

R1.2

Hole-D

H6509
CT276CB197ID138

H6510
CT276CB197ID138

H6511
CT276CB197ID138

H6512
CT276CB197ID138

GND

Hole-E

H6514
CT256B315D91N

H6506
CT256B315D91N

H6507
CT256RB276X287D91N

H6508
CT256B220D91N

GND

R1.1

H6516
CT256B315D91N

GND_AUDIO

Hole-F

H6517
CT256B220D91N

H6520
CT256B220D91N

GND

H6518
CRT266X256D91N

GND

H6519
RT335X305D91N

GND

H6521
CT256B220D91N

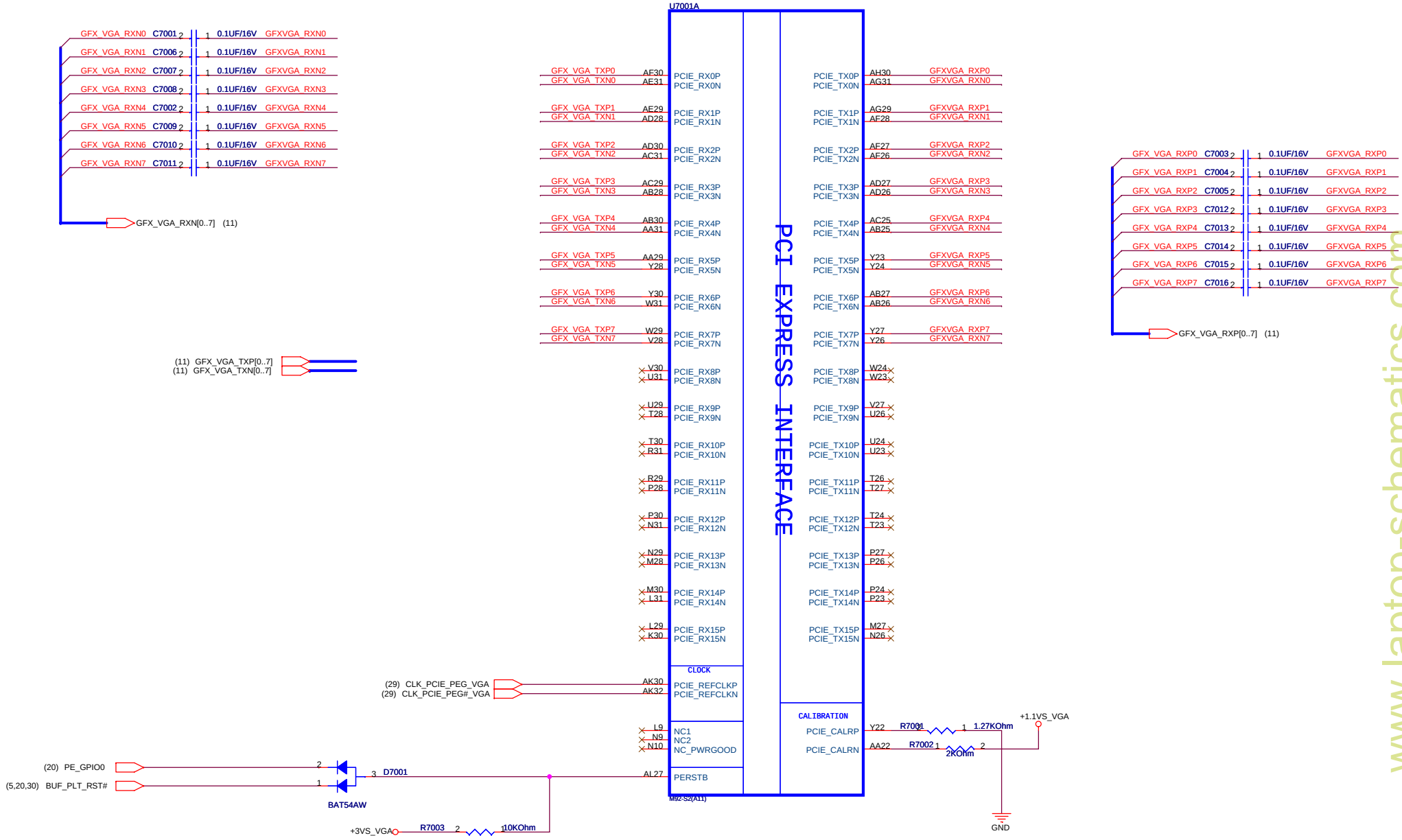
H6522
CT256B220D91N

H6513
CT256B220D91N

H6515
CT256B220D91N

GND

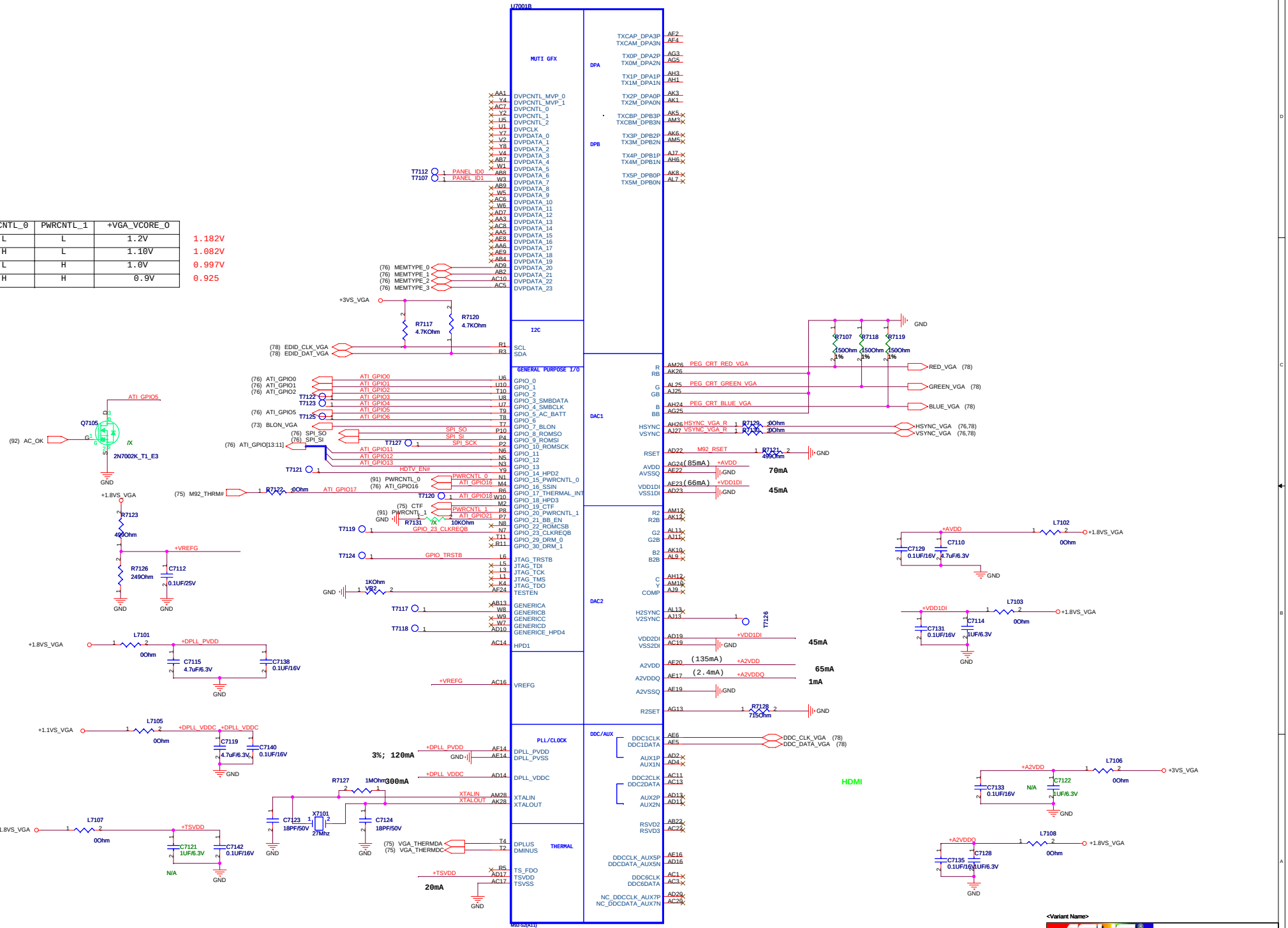
ASUSTeK COMPUTER INC. NB1	Title MDC NUT & Hinksink NUT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name	Rev
Date: Wednesday, April 08, 2009	Sheet 65 of 94	



<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer:	
Size: Custom	Project Name: N11	Rev: 1.0T
Date: Wednesday, April 08, 2009	Sheet 70 of 94	

PWRCNTL_0	PWRCNTL_1	+VGA_VCORE_O	
L	L	1.2V	1.182V
H	L	1.10V	1.082V
L	H	1.0V	0.997V
H	H	0.9V	0.925



<Variant Name>

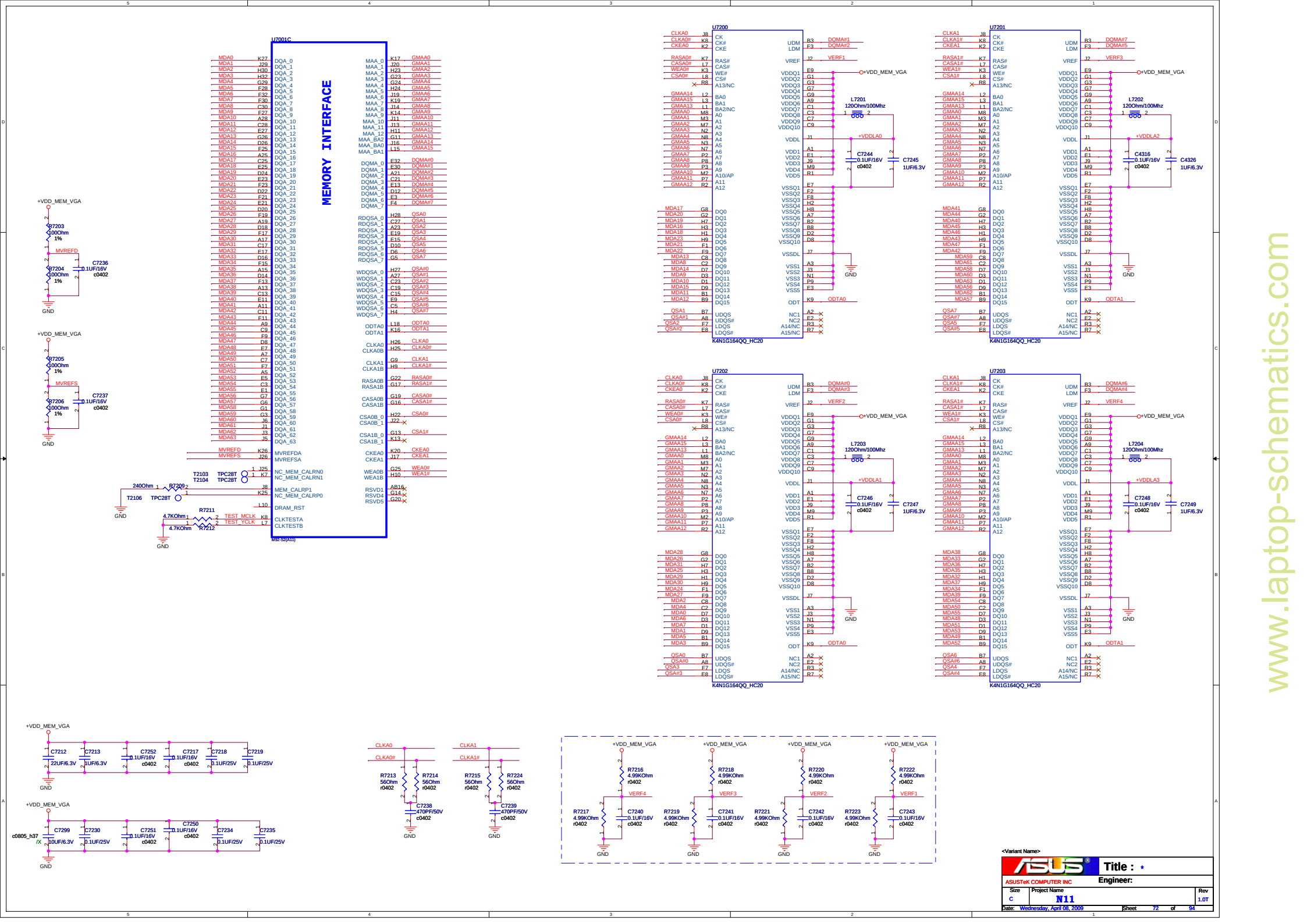
Title : *

Engineer:

ASUSTeK COMPUTER INC.

Size	Project Name	Rev
C	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 71 of 94



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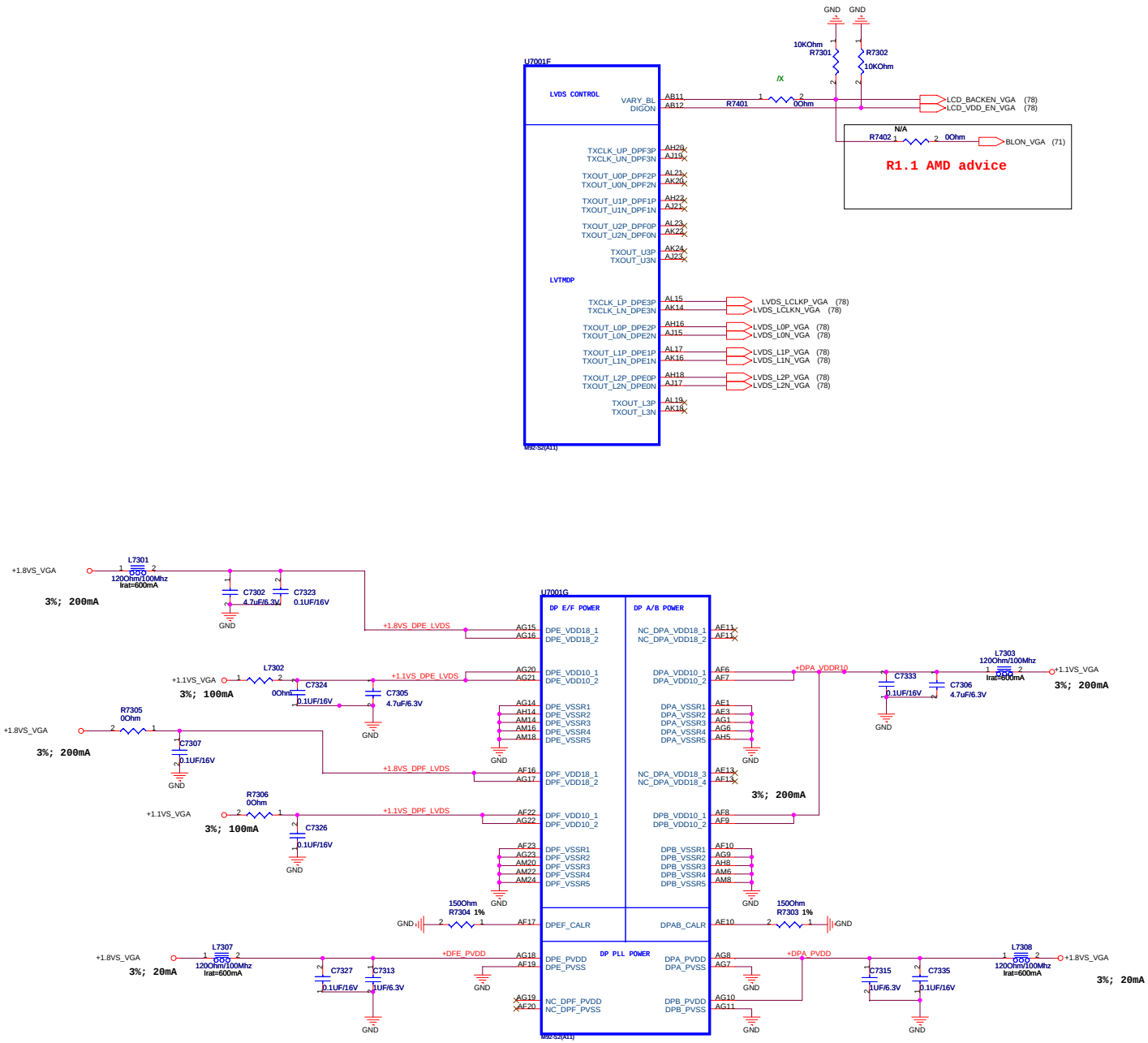
ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 72 of 94



<Variant Name>

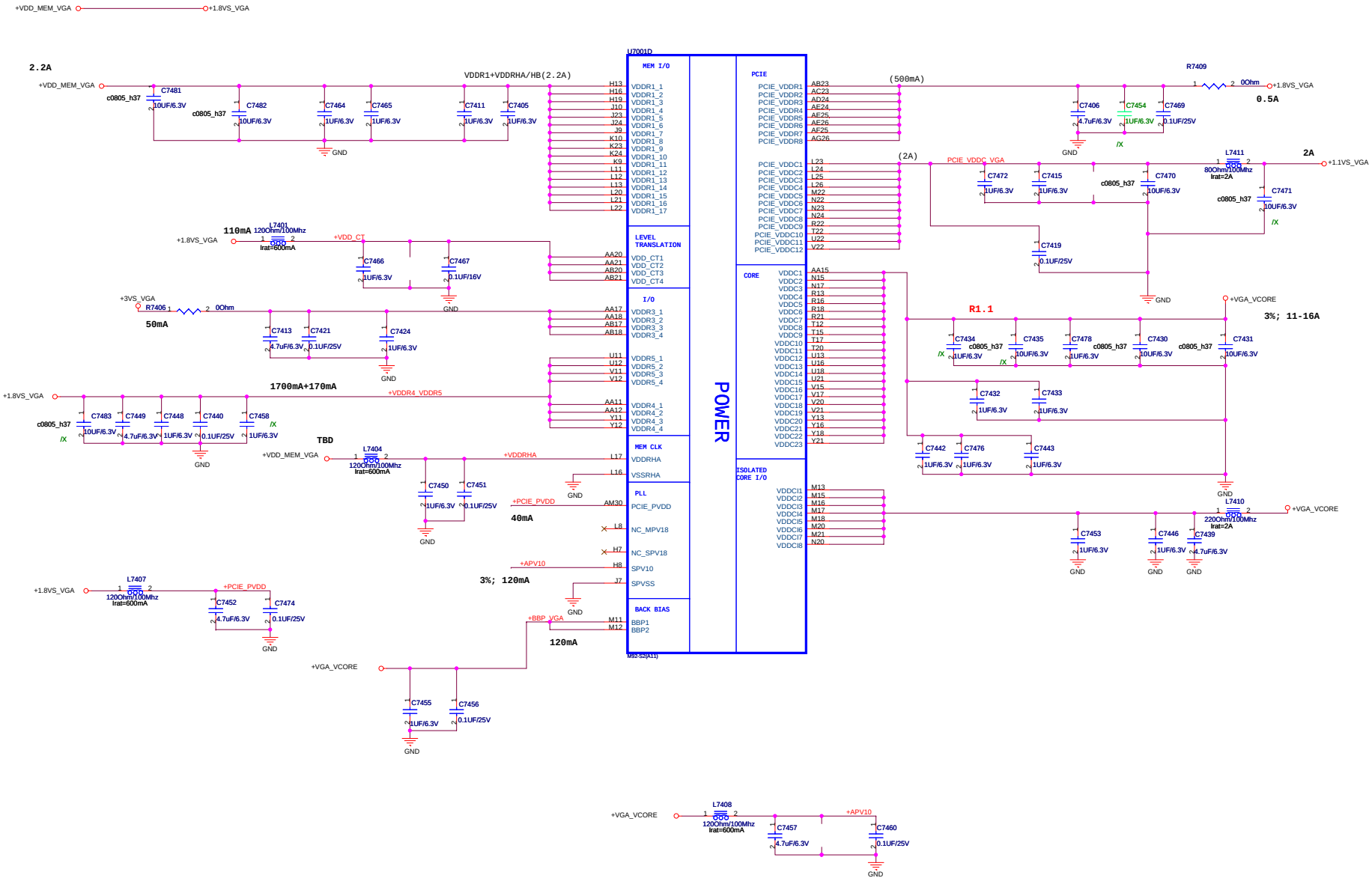
ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 73 of 94



<Variant Name>

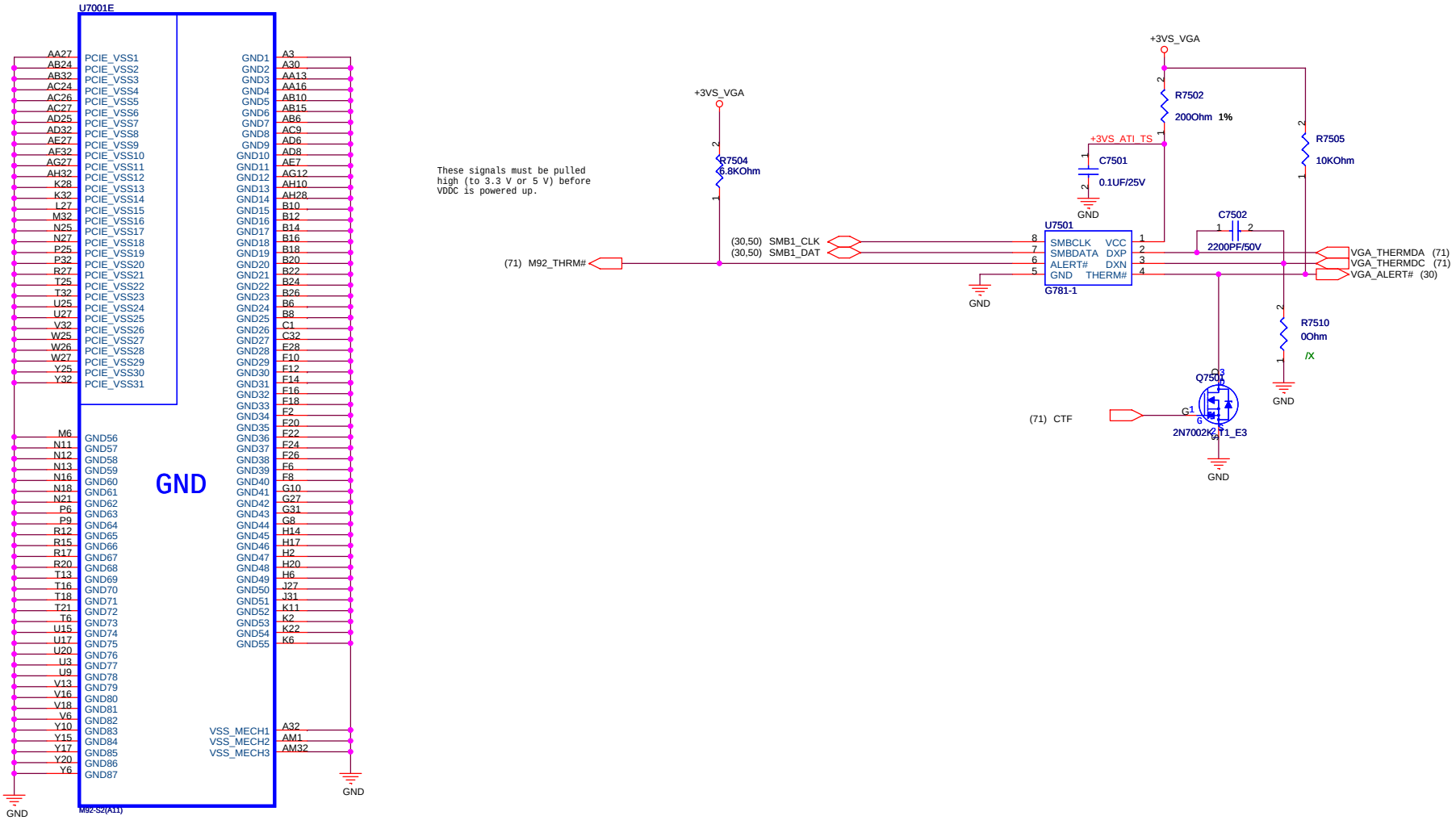
ASUSTeK COMPUTER INC.

Title : *

Engineer:

Size	Project Name	Rev
C	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 74 of 94



<Variant Name>

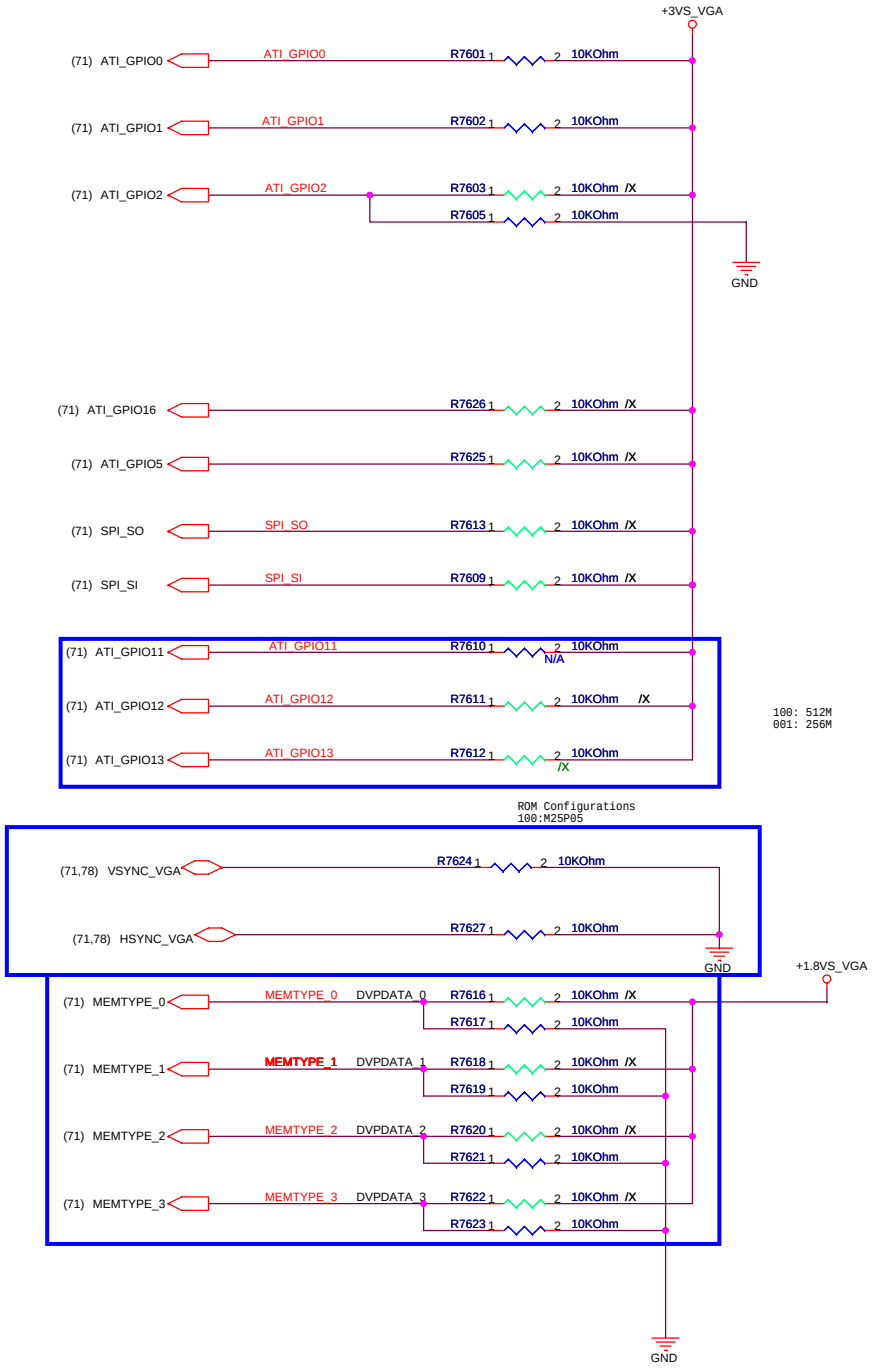
ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

Date: Wednesday, April 08, 2009 Sheet 75 of 94



GPIO(0) - TX_PWRS_ENB (Transmitter Power Savings Enable)
0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

GPIO_1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable)
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for Desktop)

GPIO_2 - BIF_GEN2_EN (5.0 GT/s Enable)
0 : Default. (Driver Controlled Gen2)
1 : Strap Controlled Gen2

GPIO(11,13,12) - CONFIG[2..0]

CONFIG[2]	100 - 512Kbit	M25P05A	(ST)
	101 - 1Mbit	M25P10A	(ST)
	101 - 2Mbit	M25P20	(ST)
CONFIG[1]	101 - 4Mbit	M25P40	(ST)
	101 - 8Mbit	M25P80	(ST)
CONFIG[0]	100 - 512Kbit	Pm25LV512	(Chingis)
	101 - 1Mbit	Pm25LV010	(Chingis)

GPIO_8 - BIF_CLK_PM_EN
0 - Disable CLKREQ# power management capability
1 - Enable CLKREQ# power management capability

GPIO_5 - AMD BOARD FEATURES I
0: 1 RANK OF MEMORY 1: 2 RANKS OF MEMORY

GPIO_16 - AMD BOARD FEATURES II
BANK SELECT;

GPIO_7 - TV OUT STANDARD
0 - PAL TVO
1 - NTSC TVO

V2SYNC - VIP_DEVICE_STRAP_EN
0: Driver would ignore the value sampled on VHAD_0 during reset
1: Driver would use the value sampled at reset from VHAD_0 to determine whether or not a VIP slave device (e.g. Theater chip) is connected (i.e. 0 indicates yes, 1 indicates no).

GPIO_9 - VGA DISABLE : 1 for disable (set to 0 for normal operation)

HSYNC;VSYNC - AUD[1:0]
00 - No audio function
01 - Audio for DisplayPort and HDMI if adapter is detected
10 - Audio for DisplayPort only
11 - Audio for both DisplayPort and HDMI.

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR2 Memory Type	Channel Size
Infineon (Qimonda)	0000	0	64M*16	
Samsung	0001	1	64M*16	
Hynix				
Micron				

<Variant Name>

ASUSTeK COMPUTER INC

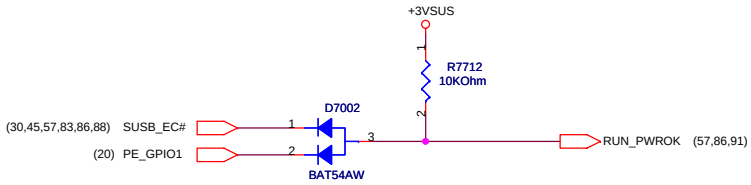
Title : *

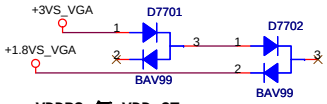
Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

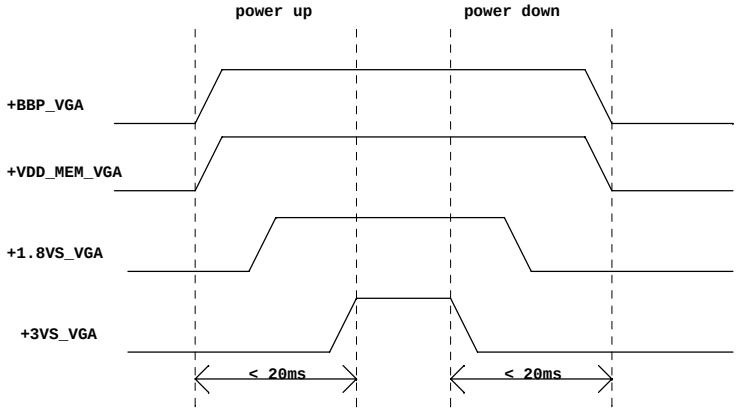
Date: Thursday, April 09, 2009 Sheet 76 of 94

GPIO_21_BB_EN	+BBP
0	1.1V
1	1.5V





VDDR3 每 VDD_CT
< 2V



1.1-V rails should ramp before, or together with the 1.8-V rails.
The 1.1-V nominal voltage rails should never lag the 1.8-V nominal
voltage rails by more than 1.1 V within a 1 ms window.

<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	N11	1.0T

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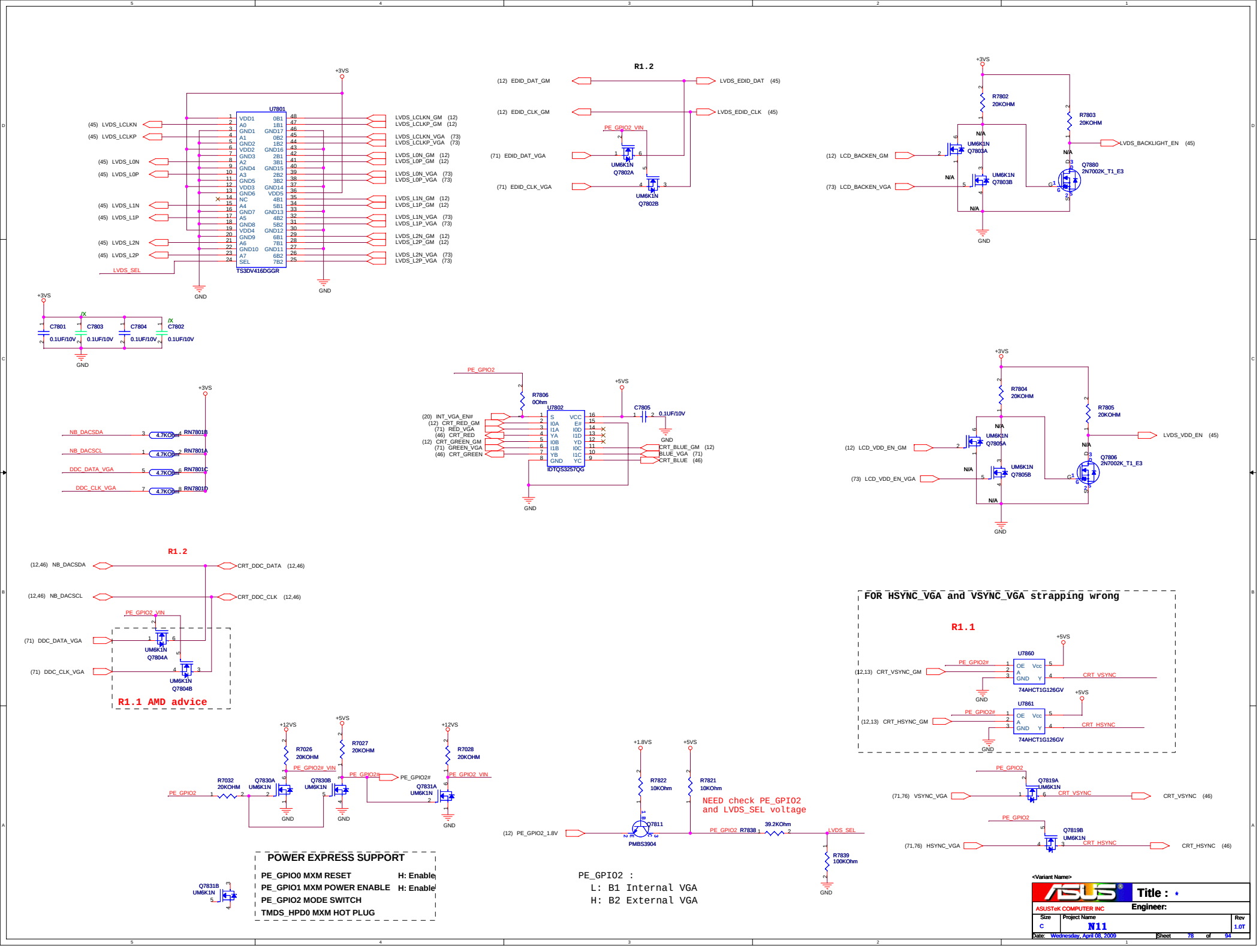
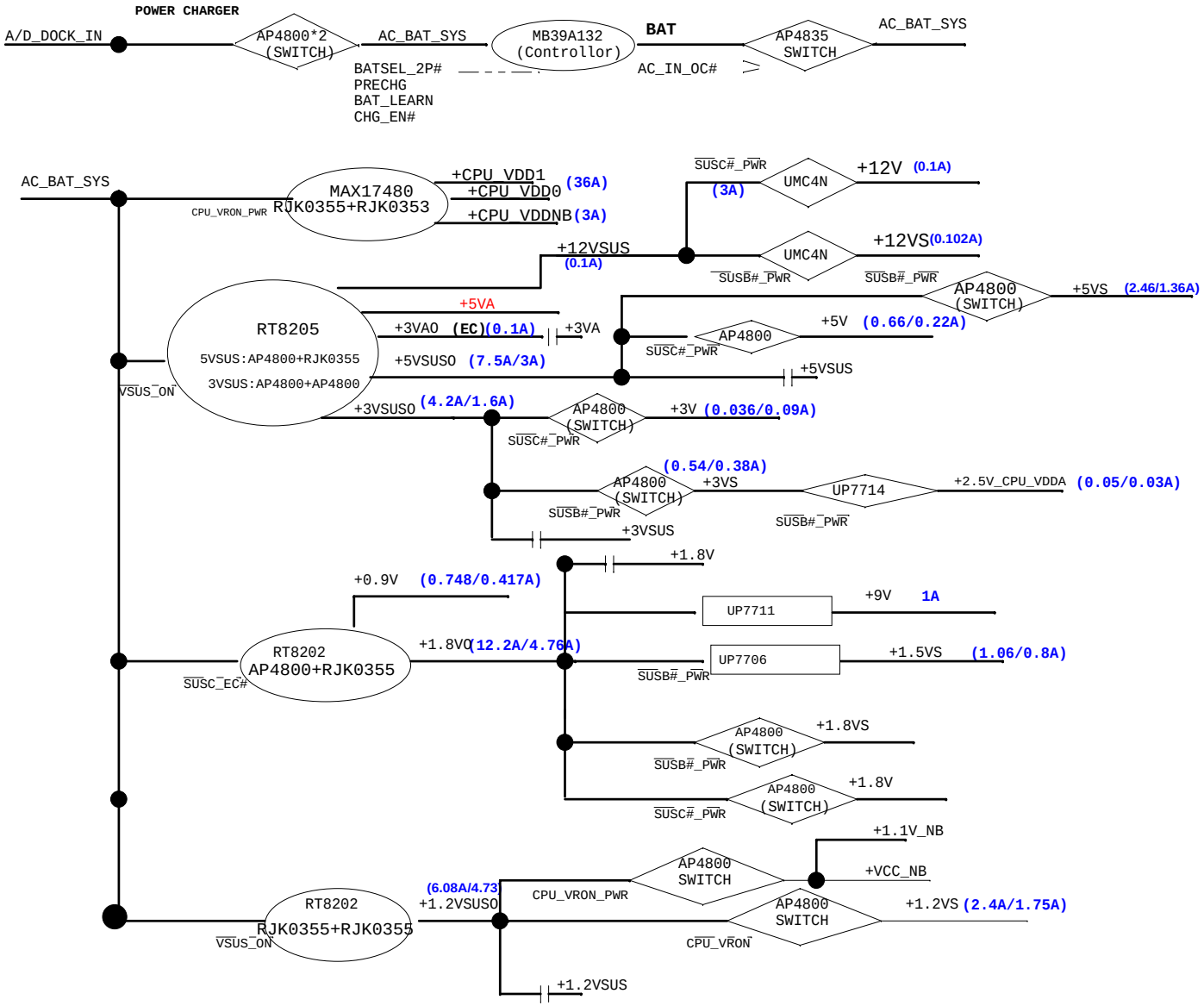




<Variant Name>

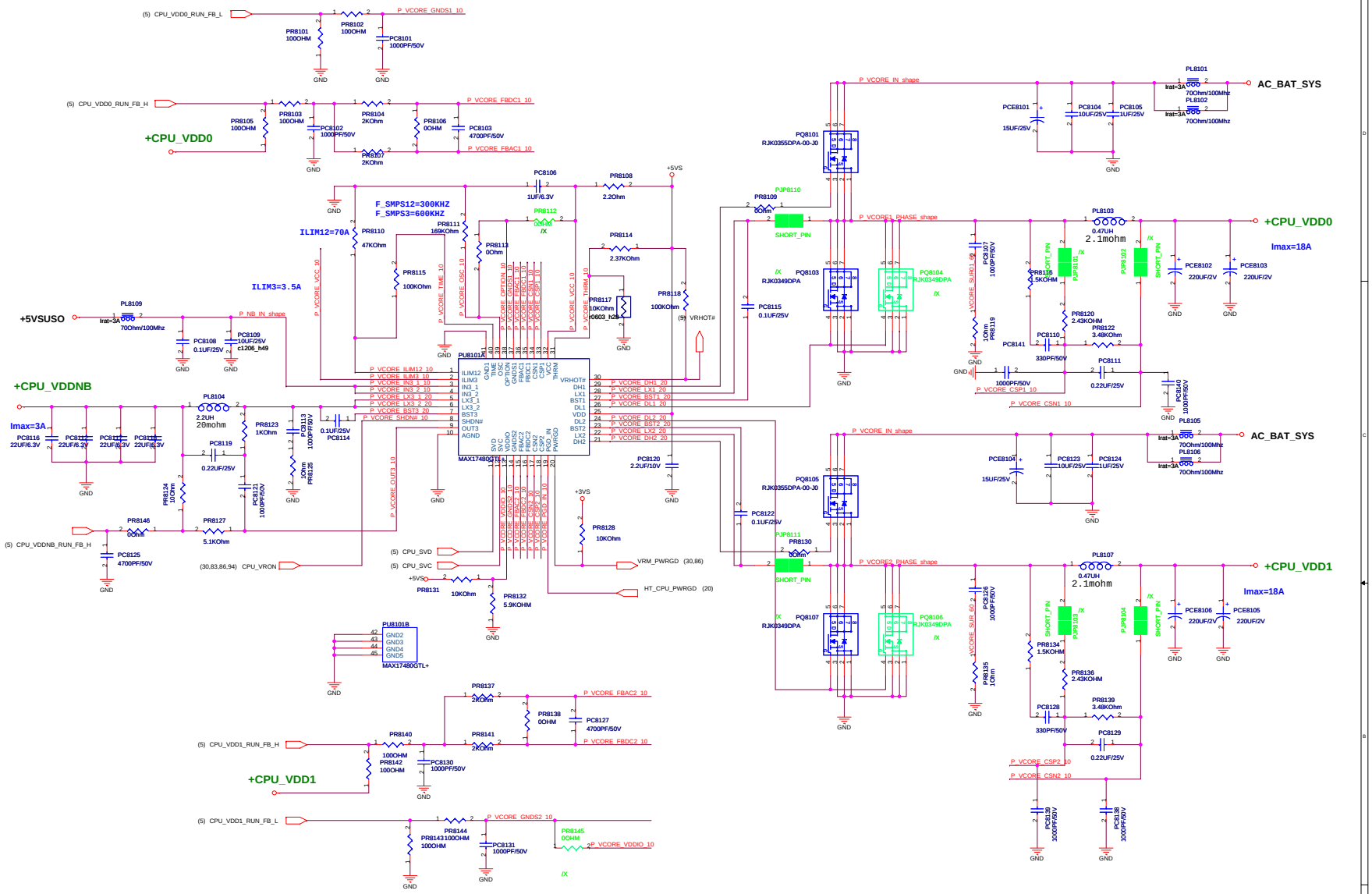
Title : Power_ FLOW

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
A	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 80 of 94



<Variant Name>

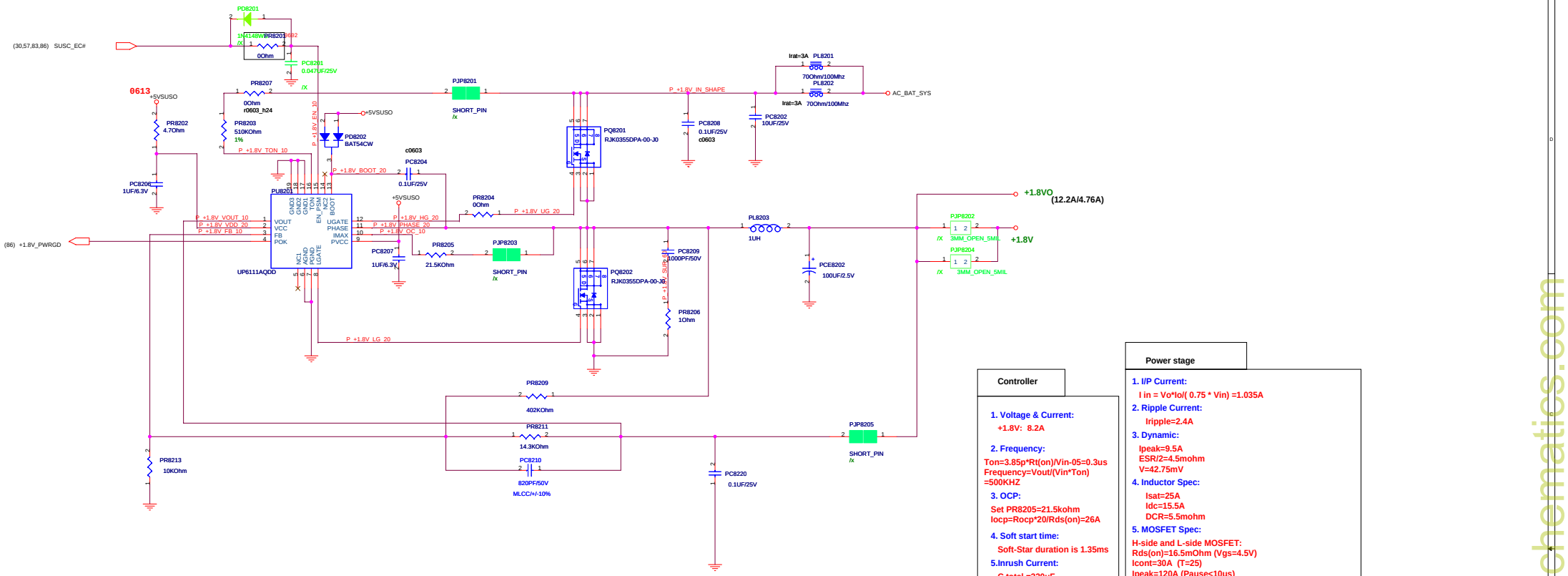
Title : +VCORE

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 81 of 94

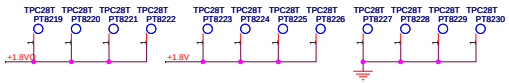


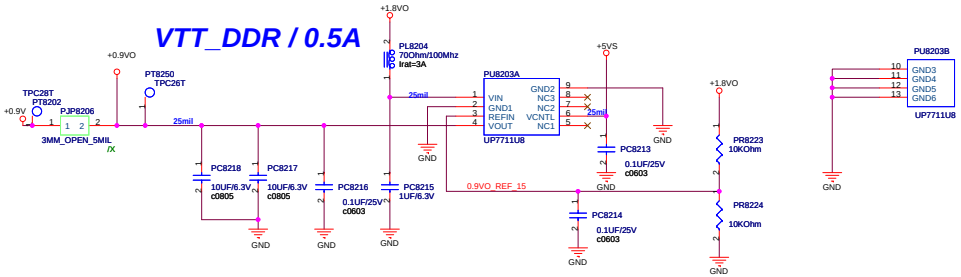
Controller

1. Voltage & Current:
   +1.8V: 8.2A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8205=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.035A
2. Ripple Current:
   Iripple=2.4A
3. Dynamic:
   Ipeak=9.5A
   ESR/2=4.5mohm
   V=42.75mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)





<Variant Name>

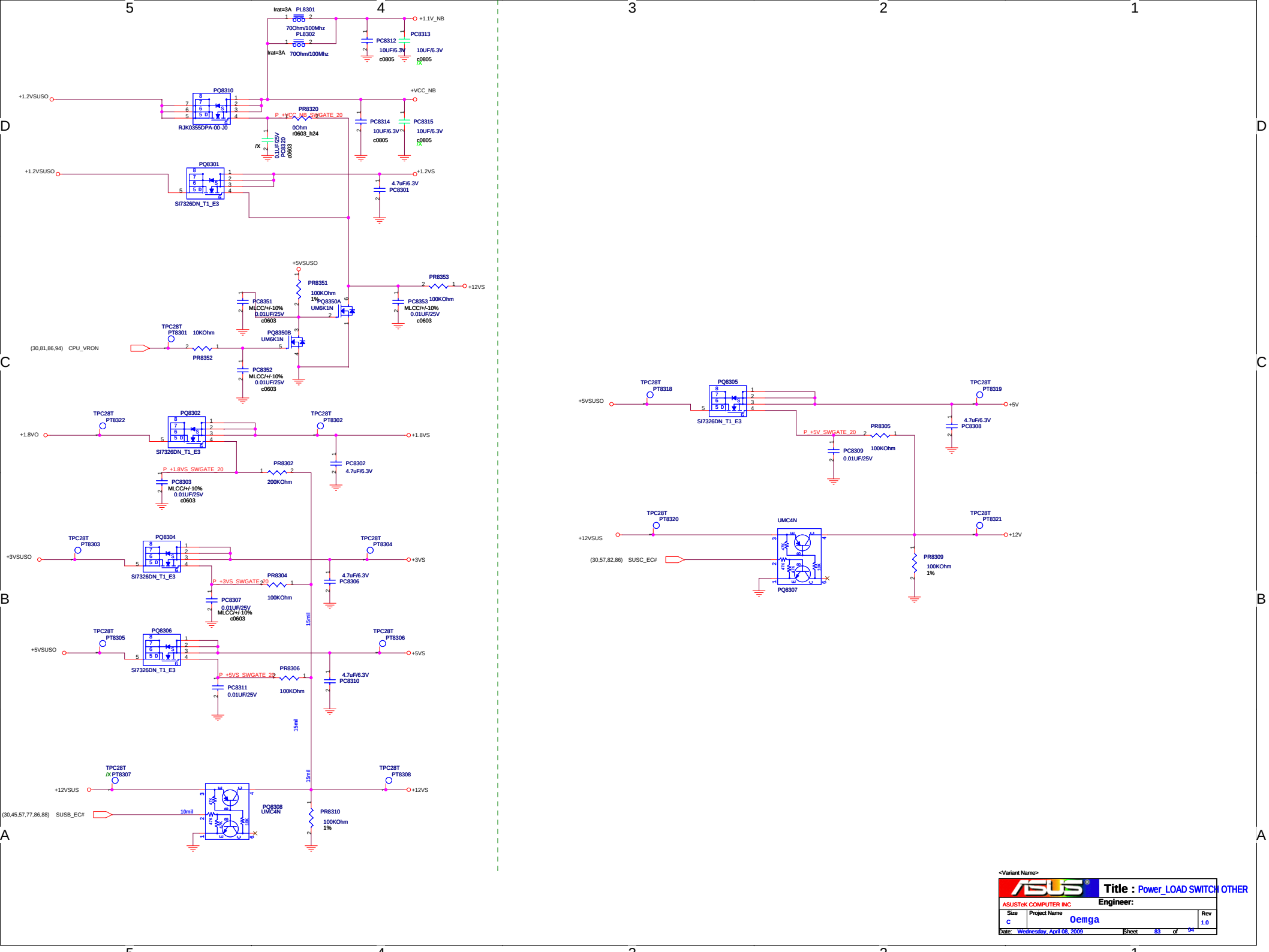
ASUSTeK COMPUTER INC

Title : Power_+1.8V&+0.9V

Engineer:

Size	Project Name	Rev
A2	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 82 of 94



<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_LOAD SWITCH OTHER

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 83 of 94

<Variant Name>

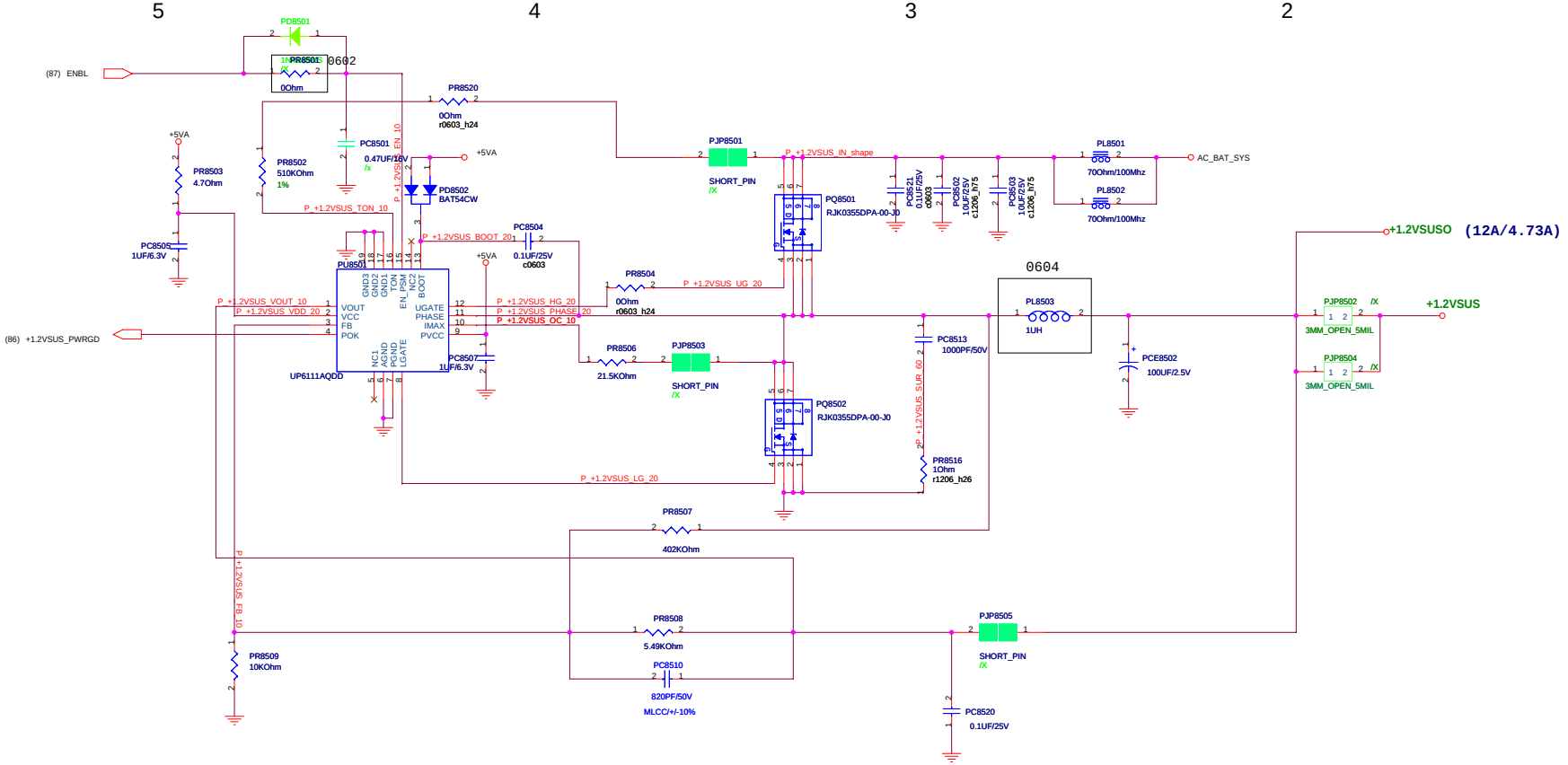
Title : Power_Charger

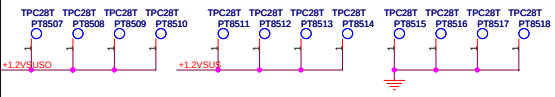
ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Wednesday, April 08, 2009 Sheet 84 of 94





Controller

1. Voltage & Current:
   +1.2VSUS: 10.5A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

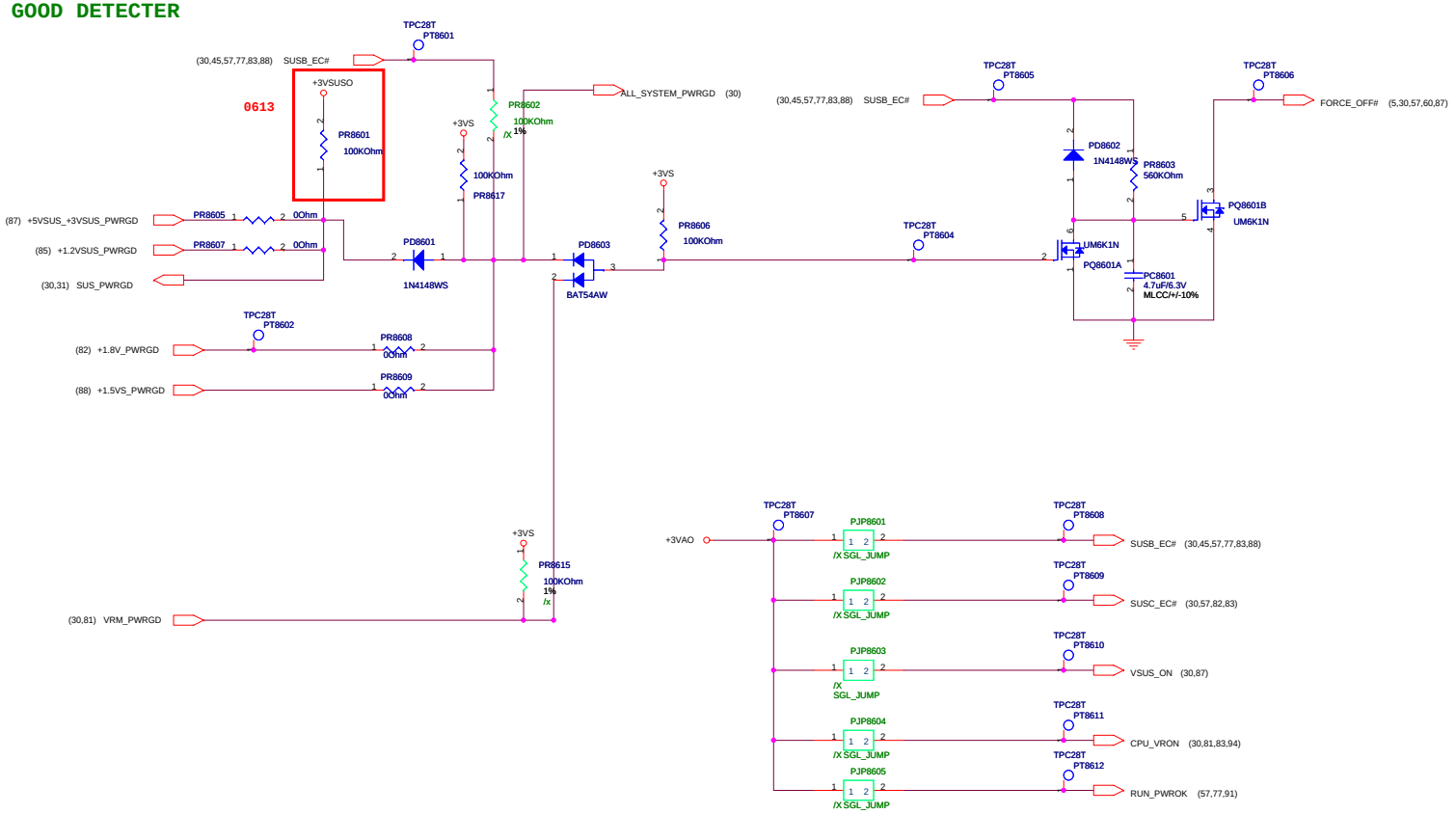
1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=2.5A
3. Dynamic:
   Ipeak=6.35
   ESR/2=4.5mohm
   V=28.575mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

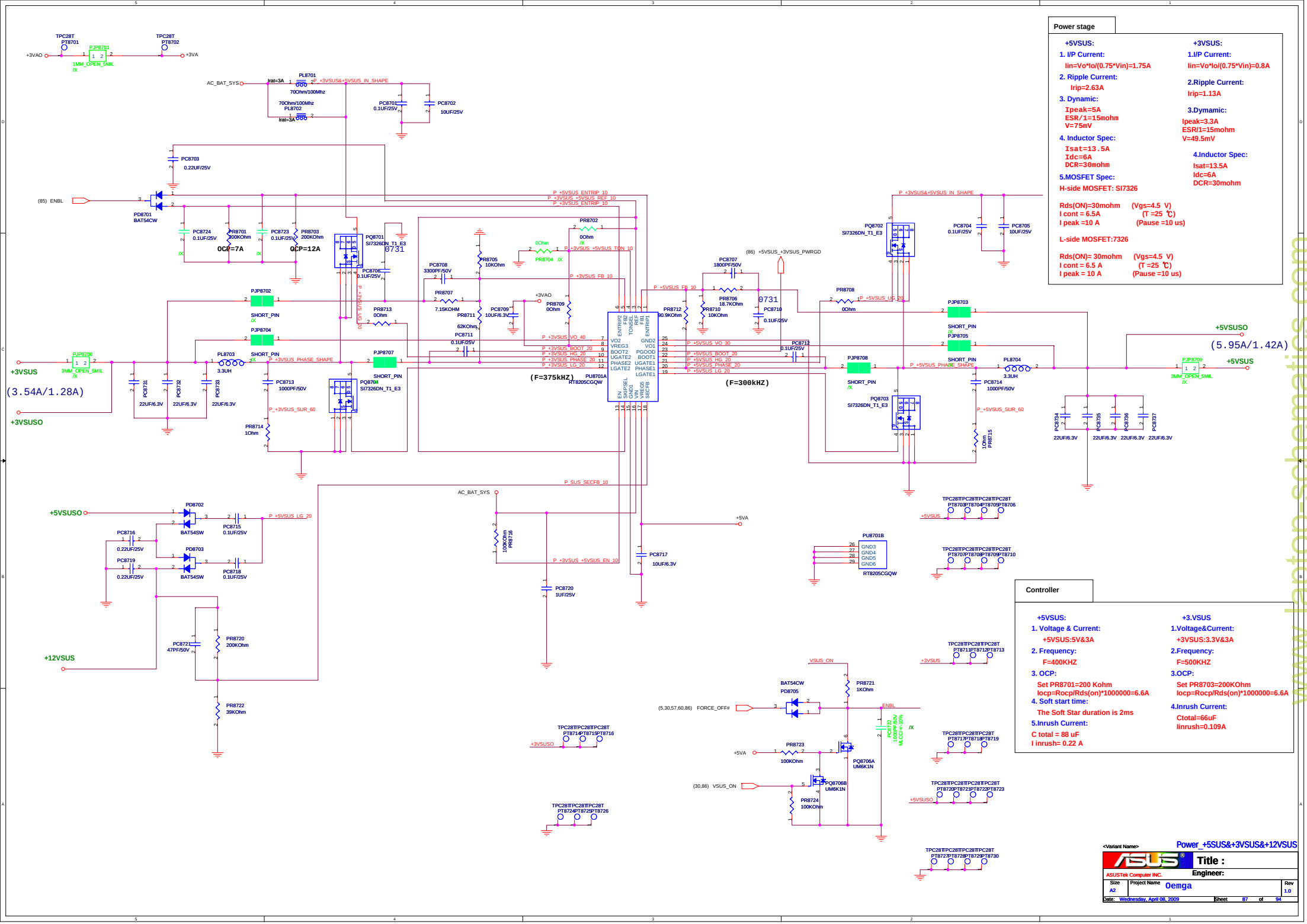
ASUSTeK COMPUTER INC	Title : Power_1.2VSUS	
	Engineer:	
Size: C	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 85 of 94	

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_GOOD_DETECTER	
	Engineer:	
Size: C	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 86 of 94	


Power stage
+5VSUS:
1. I/P Current:
Iin=Vo*Io/(0.75*Vin)=1.75A
2. Ripple Current:
Irip=2.63A
3. Dynamic:
Ipeak=5A
ESR/1=15mohm
V=75mV
4. Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
5.MOSFET Spec:
H-side MOSFET: SI7326
Rds(ON)=30mohm (Vgs=4.5 V)
I cont = 6.5A (T =25 ℃)
I peak =10 A (Pause =10 us)
L-side MOSFET:7326
Rds(ON)= 30mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25 ℃)
I peak = 10 A (Pause =10 us)
+3VSUS:
1.I/P Current:
Iin=Vo*Io/(0.75*Vin)=0.8A
2.Ripple Current:
Irip=1.13A
3.Dymamic:
Ipeak=3.3A
ESR/1=15mohm
V=49.5mV
4.Inductor Spec:
Isat=13.5A
Idc=6A
DCR=30mohm
Controller
+5VSUS:
1. Voltage & Current:
+5VSUS:5V&3A
2. Frequency:
F=400KHZ
3. OCP:
Set PR8701=200 Kohm
Iocp=Rocp/Rds(on)*1000000=6.6A
4. Soft start time:
The Soft Star duration is 2ms
5.Inrush Current:
C total = 88 uF
I inrush= 0.22 A
+3.VSUS
1.Voltage&Current:
+3VSUS:3.3V&3A
2.Frequency:
F=500KHZ
3.OCP:
Set PR8703=200KOhm
Iocp=Rocp/Rds(on)*1000000=6.6A
4.Inrush Current:
Ctotal=66uF
Iinrush=0.109A
+3VSUS
(3.54A/1.28A)
+5VSUSO
(5.95A/1.42A)
+5VSUS
+12VSUS
OCP=7A
OCP=12A
(F=375kHZ)
(F=300kHZ)
AC_BAT_SYS
PU8701A RT8205CGQW
PU8701B RT8205CGQW
PQ8701 SI7326DN_T1_E3
PQ8702 SI7326DN_T1_E3
PQ8703 SI7326DN_T1_E3
PQ8704 SI7326DN_T1_E3
PQ8706A UM6K1N
PQ8706B UM6K1N
PD8701 BAT54CW
PD8702 BAT54SW
PD8703 BAT54SW
PD8705 BAT54CW
PL8701 70Ohm/100Mhz
PL8703 3.3UH
PL8704 3.3UH
ENBL
VSUS_ON
FORCE_OFF#
<Variant Name>
Power_+5SUS&+3VSUS&+12VSUS
Title :
ASUSTek Computer INC.
Engineer:
Size A2
Project Name Oemga
Rev 1.0
Date: Wednesday, April 08, 2009
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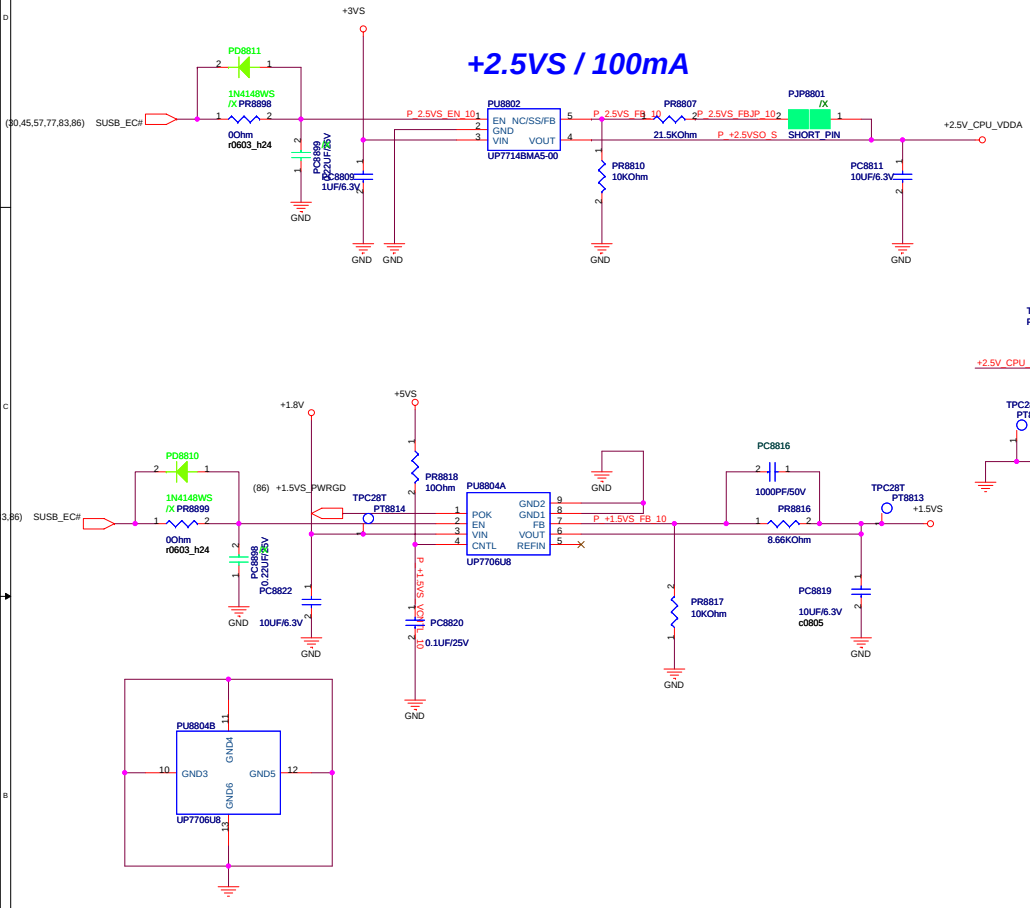
www.laptop-schematics.com



2.5V @ 0.2A

1. Dropout Voltage:

△V = 0.21V (Io =0.3A)

2. Current Limit:

I limit =320mA

3. Continue Current:

I cont = 300mA

4. Power Dissipation:

Rthjc = 250℃/W

Pd = 0.4W

5. EN Voltage:

V rising = 2V

V falling = 0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us

C total =10uF

I inrush = 0.063A

+1.5VS @ 1.2A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =4A

3. Continue Current:

I cont = 2A

4. Power Dissipation:

Rthjc = 52℃/W

Pd =1.9W

5. EN Voltage:

V rising = 1.4V

V falling = 0.8V

6. Supply Voltage:

Vcc =5V

7. Inrush current:

T ss = 400us

C total =10uF

I inrush = 0.063A

<Variant Name> Power_+2.5V&+1.5VS&+1.1V_NB

Title :

ASUSTek Computer INC. Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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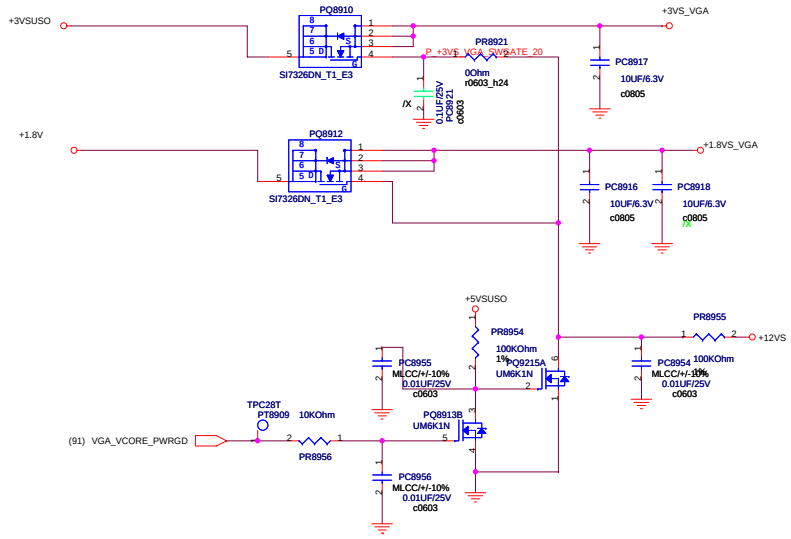


<Variant Name>

Title :

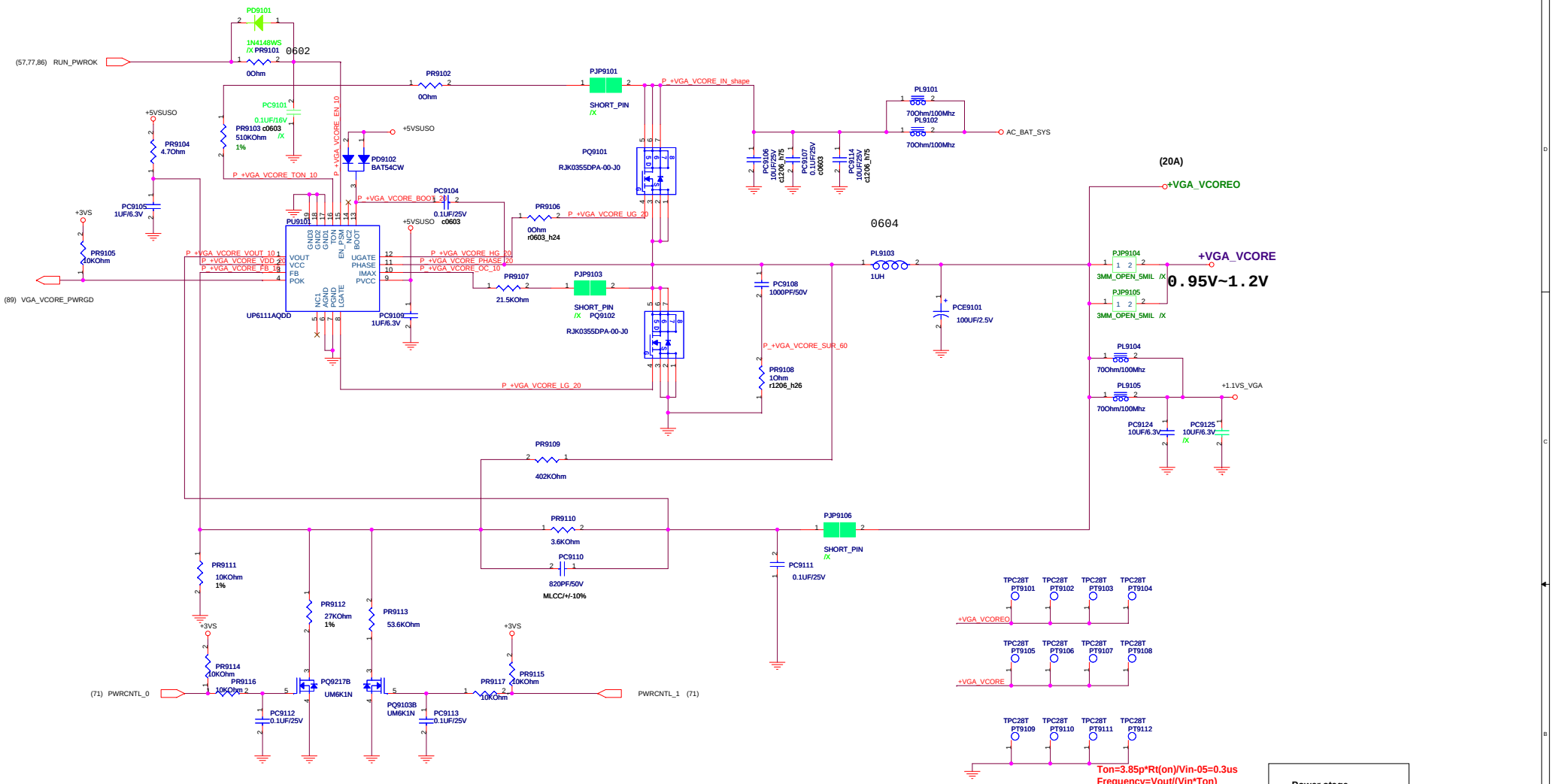
ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
C	Oemga	1.0

Date: Wednesday, April 08, 2009 Sheet 89 of 94

ASUSTek Computer INC.	Title :	
	Engineer:	
Size: Custom	Project Name: Oemga	Rev: 1.0
Date: Wednesday, April 08, 2009	Sheet 90 of 94	



PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	1.02	-5%
0	1	1.071	Normal
1	0	1.12	+5%
1	1	1.171	+10%

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
~500KHZ

Controller

1. Voltage & Current:
   +1.2VSUS: 16A
2. Frequency:
3. OCP:
   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =220uF
   I inrush=0.163A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =0.85A
2. Ripple Current:
   Iripple=3.74A
3. Dynamic:
   Ipeak=6.1A
   ESR/2=4.5mohm
   V=27.5mohm
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

Title : Power_+VGA_VCORE

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
C	Oemga	1.0

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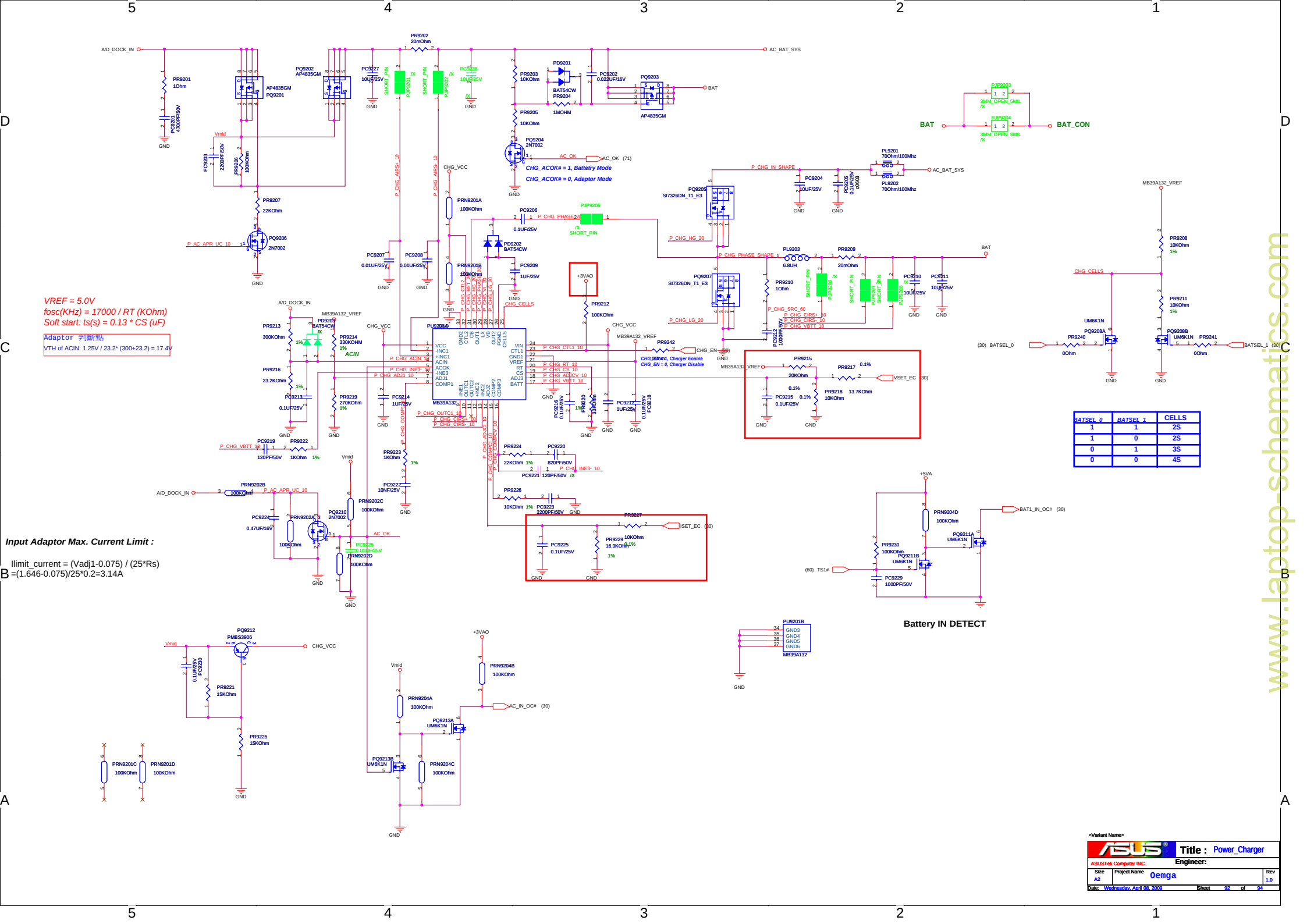
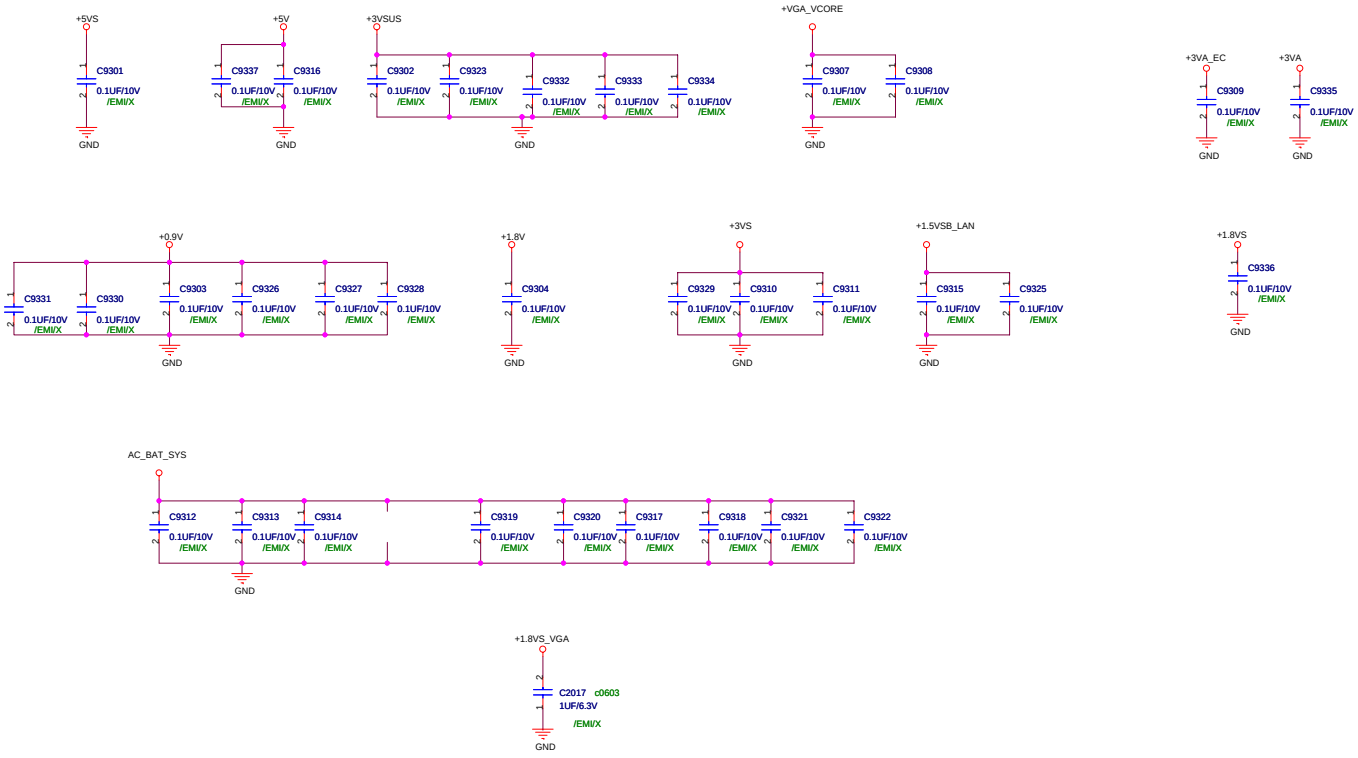

VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
Adaptor 判斷點
VTH of ACIN: 1.25V / 23.2* (300+23.2) = 17.4V
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25*0.2=3.14A
CHG_ACOK# = 1, Battery Mode
CHG_ACOK# = 0, Adaptor Mode
CHG_EN = 1, Charger Enable
CHG_EN = 0, Charger Disable
ACIN
Battery IN DETECT
BATSEL_0 BATSEL_1 CELLS
1 1 2S
1 0 2S
0 1 3S
0 0 4S
A/D_DOCK_IN
AC_BAT_SYS
BAT
BAT_CON
CHG_VCC
Vmid
+3VAO
+5VA
GND
MB39A132
MB39A132_VREF
AC_OK
ISET_EC (30)
VSET_EC (30)
CHG_EN (30)
AC_IN_OC# (30)
BAT1_IN_OC# (30)
TS1# (60)
BATSEL_0 (30)
BATSEL_1 (30)
Title : Power_Charger
ASUSTek Computer INC.
Engineer:
Size A2
Project Name Oemga
Rev 1.0
Date: Wednesday, April 08, 2009
Sheet 92 of 94
<Variant Name>
www.laptop-schematics.com



<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
C		

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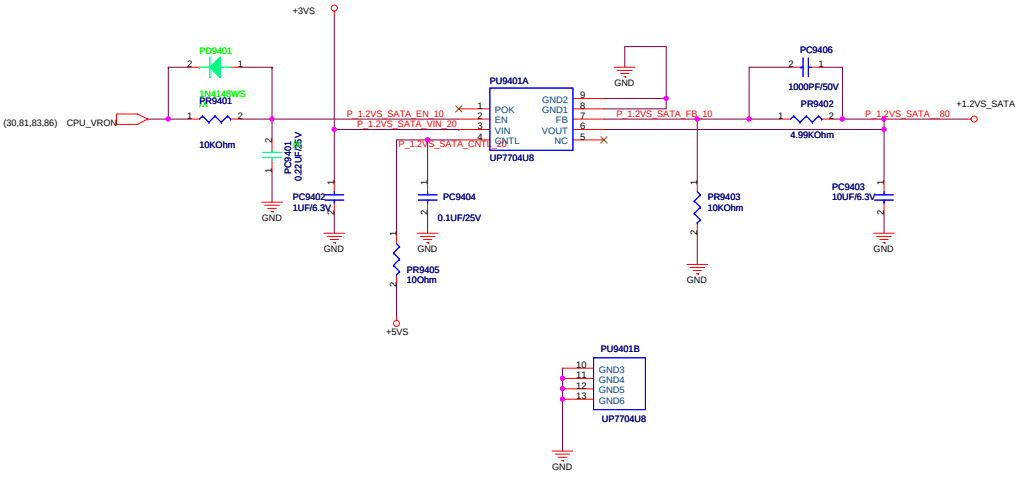

+1.2VS_SATA /

220mA/350mA

1.2V @ 0.1A

1. Dropout Voltage:

△V = 0.3V (Io =2A)

2. Current Limit:

I limit =2.5A

3. Continue Current:

I cont = 2A

4. Power Dissipation:

Rthjc =52℃/W
Pd = 1.8W

5. EN Voltage:

V rising = 2V
V falling =
0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush =
0.063A

<Variant Name>

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
C		

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