1.5A

CPU_VLDT

U0301A

HT LINK

D1	VLDT_A2	VLDT_B1	AE2
D2	VLDT_A3	VLDT_B2	AE3
D3	VLDT_A1	VLDT_B3	AE4
D4	VLDT_A4	VLDT_B4	AE5

HT_CPU_RXD0	E3	L0_CADIN_H[0]	L0_CADOUT_H[0]	AD1	HT_CPU_TXD0
HT_CPU_RXD#0	E2	L0_CADIN_L[0]	L0_CADOUT_L[0]	AC1	HT_CPU_TXD#0
HT_CPU_RXD1	E1	L0_CADIN_H[1]	L0_CADOUT_H[1]	AC2	HT_CPU_TXD1
HT_CPU_RXD#1	F1	L0_CADIN_L[1]	L0_CADOUT_L[1]	AC3	HT_CPU_TXD#1
HT_CPU_RXD2	G3	L0_CADIN_H[2]	L0_CADOUT_H[2]	AB1	HT_CPU_TXD2
HT_CPU_RXD#2	G2	L0_CADIN_L[2]	L0_CADOUT_L[2]	AA1	HT_CPU_TXD#2
HT_CPU_RXD3	G1	L0_CADIN_H[3]	L0_CADOUT_H[3]	AA2	HT_CPU_TXD3
HT_CPU_RXD#3	H1	L0_CADIN_L[3]	L0_CADOUT_L[3]	AA3	HT_CPU_TXD#3
HT_CPU_RXD4	J1	L0_CADIN_H[4]	L0_CADOUT_H[4]	W2	HT_CPU_TXD4
HT_CPU_RXD#4	K1	L0_CADIN_L[4]	L0_CADOUT_L[4]	W3	HT_CPU_TXD#4
HT_CPU_RXD5	L3	L0_CADIN_H[5]	L0_CADOUT_H[5]	V1	HT_CPU_TXD5
HT_CPU_RXD#5	L2	L0_CADIN_L[5]	L0_CADOUT_L[5]	U1	HT_CPU_TXD#5
HT_CPU_RXD6	L1	L0_CADIN_H[6]	L0_CADOUT_H[6]	U2	HT_CPU_TXD6
HT_CPU_RXD#6	M1	L0_CADIN_L[6]	L0_CADOUT_L[6]	U3	HT_CPU_TXD#6
HT_CPU_RXD7	N3	L0_CADIN_H[7]	L0_CADOUT_H[7]	T1	HT_CPU_TXD7
HT_CPU_RXD#7	N2	L0_CADIN_L[7]	L0_CADOUT_L[7]	R1	HT_CPU_TXD#7
HT_CPU_RXD8	E5	L0_CADIN_H[8]	L0_CADOUT_H[8]	AD4	HT_CPU_TXD8
HT_CPU_RXD#8	F5	L0_CADIN_L[8]	L0_CADOUT_L[8]	AD3	HT_CPU_TXD#8
HT_CPU_RXD9	F3	L0_CADIN_H[9]	L0_CADOUT_H[9]	AD5	HT_CPU_TXD9
HT_CPU_RXD#9	F4	L0_CADIN_L[9]	L0_CADOUT_L[9]	AC5	HT_CPU_TXD#9
HT_CPU_RXD10	G5	L0_CADIN_H[10]	L0_CADOUT_H[10]	AB4	HT_CPU_TXD10
HT_CPU_RXD#10	H5	L0_CADIN_L[10]	L0_CADOUT_L[10]	AB3	HT_CPU_TXD#10
HT_CPU_RXD11	H3	L0_CADIN_H[11]	L0_CADOUT_H[11]	AB5	HT_CPU_TXD11
HT_CPU_RXD#11	H4	L0_CADIN_L[11]	L0_CADOUT_L[11]	AA5	HT_CPU_TXD#11
HT_CPU_RXD12	K3	L0_CADIN_H[12]	L0_CADOUT_H[12]	Y5	HT_CPU_TXD12
HT_CPU_RXD#12	K4	L0_CADIN_L[12]	L0_CADOUT_L[12]	W5	HT_CPU_TXD#12
HT_CPU_RXD13	L5	L0_CADIN_H[13]	L0_CADOUT_H[13]	V4	HT_CPU_TXD13
HT_CPU_RXD#13	M5	L0_CADIN_L[13]	L0_CADOUT_L[13]	V3	HT_CPU_TXD#13
HT_CPU_RXD14	M3	L0_CADIN_H[14]	L0_CADOUT_H[14]	V5	HT_CPU_TXD14
HT_CPU_RXD#14	M4	L0_CADIN_L[14]	L0_CADOUT_L[14]	U5	HT_CPU_TXD#14
HT_CPU_RXD15	N5	L0_CADIN_H[15]	L0_CADOUT_H[15]	T4	HT_CPU_TXD15
HT_CPU_RXD#15	P5	L0_CADIN_L[15]	L0_CADOUT_L[15]	T3	HT_CPU_TXD#15

10 HT_CPU_RXD[0..15]

10 HT_CPU_RXD#[0..15]

HT_CPU_TXD[0..15] 10

HT_CPU_TXD#[0..15] 10

10 HT_CPU_RX_CLK0	HT_CPU_RX_CLK0	J3	L0_CLKIN_H[0]	L0_CLKOUT_H[0]	Y1	HT_CPU_TX_CLK0	HT_CPU_TX_CLK0 10
10 HT_CPU_RX_CLK#0	HT_CPU_RX_CLK#0	J2	L0_CLKIN_L[0]	L0_CLKOUT_L[0]	W1	HT_CPU_TX_CLK#0	HT_CPU_TX_CLK#0 10
10 HT_CPU_RX_CLK1	HT_CPU_RX_CLK1	J5	L0_CLKIN_H[1]	L0_CLKOUT_H[1]	Y4	HT_CPU_TX_CLK1	HT_CPU_TX_CLK1 10
10 HT_CPU_RX_CLK#1	HT_CPU_RX_CLK#1	K5	L0_CLKIN_L[1]	L0_CLKOUT_L[1]	Y3	HT_CPU_TX_CLK#1	HT_CPU_TX_CLK#1 10
10 HT_CPU_RX_CTL0	HT_CPU_RX_CTL0	N1	L0_CTLIN_H[0]	L0_CTLOUT_H[0]	R2	HT_CPU_TX_CTL0	HT_CPU_TX_CTL0 10
10 HT_CPU_RX_CTL#0	HT_CPU_RX_CTL#0	P1	L0_CTLIN_L[0]	L0_CTLOUT_L[0]	R3	HT_CPU_TX_CTL#0	HT_CPU_TX_CTL#0 10
10 HT_CPU_RX_CTL1	HT_CPU_RX_CTL1	P3	L0_CTLIN_H[1]	L0_CTLOUT_H[1]	T5	HT_CPU_TX_CTL1	HT_CPU_TX_CTL1 10
10 HT_CPU_RX_CTL#1	HT_CPU_RX_CTL#1	P4	L0_CTLIN_L[1]	L0_CTLOUT_L[1]	R5	HT_CPU_TX_CTL#1	HT_CPU_TX_CTL#1 10

SOCKET638

Change P/N to 12G011306380

071113

Do not cross plane.

+1.1VS

1MM_OPEN_5MIL

JP301

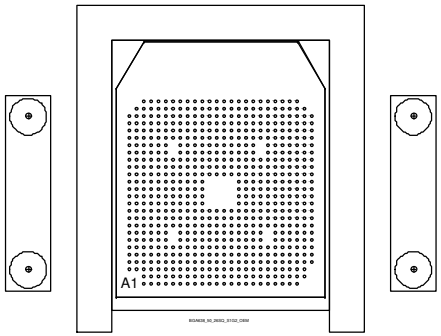
CPU_VLDT

C0302	C0303	C0304	C0305	C0306	C0308	C0307
c0805_h37	c0805_h37	c0805_h37			180PF/50V	180PF/50V
10UF/6.3V	10UF/6.3V	10UF/6.3V	0.1UF/16V	0.1UF/16V		

GND GND

Place close to socket

* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



ASUSTeK COMPUTER INC. NB1

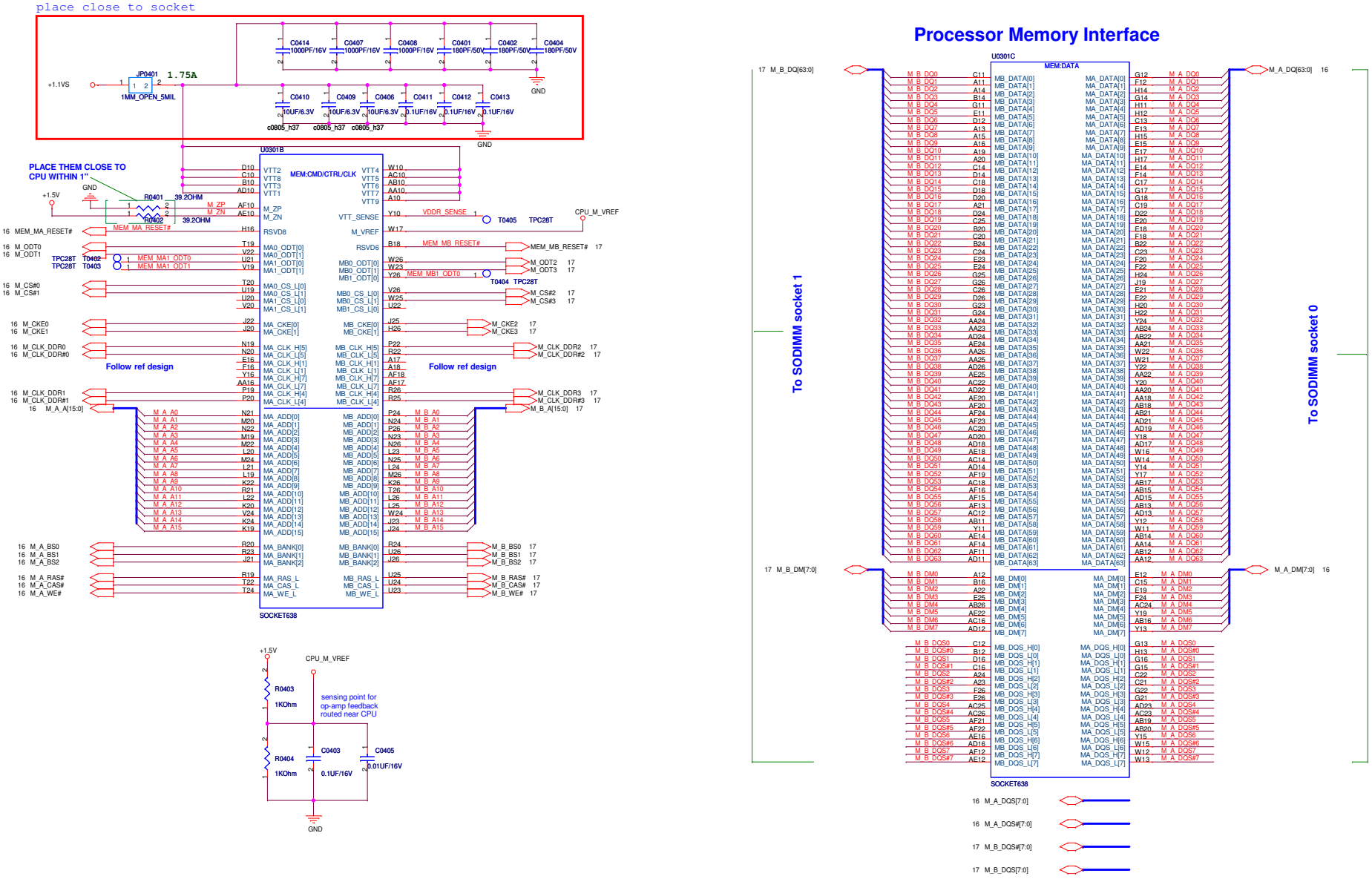
Title : Griffin HT I/F

Engineer: Vincent_Chiang

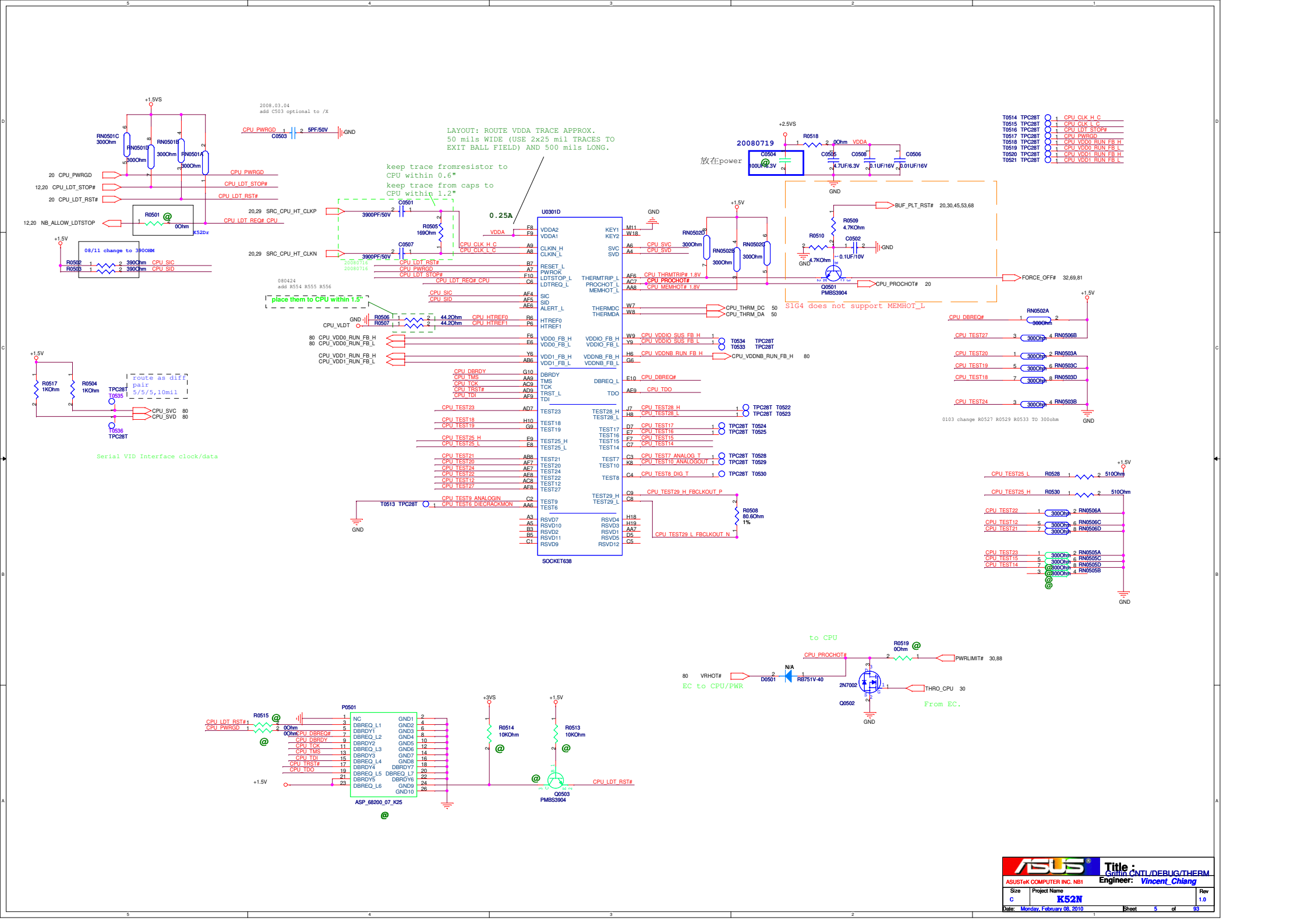
Size	Project Name	Rev
B	K52N	1.0

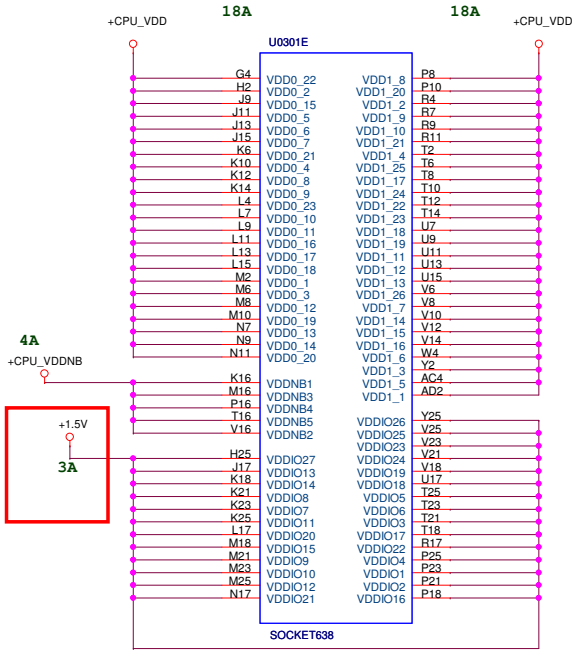
Date: Monday, February 08, 2010 Sheet 3 of 93

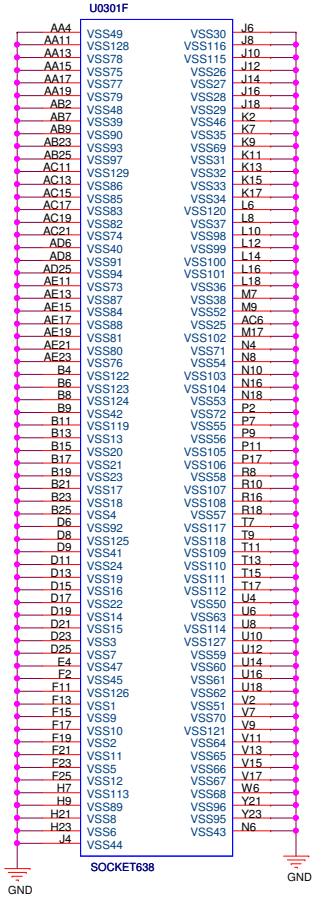
Processor Memory Interface



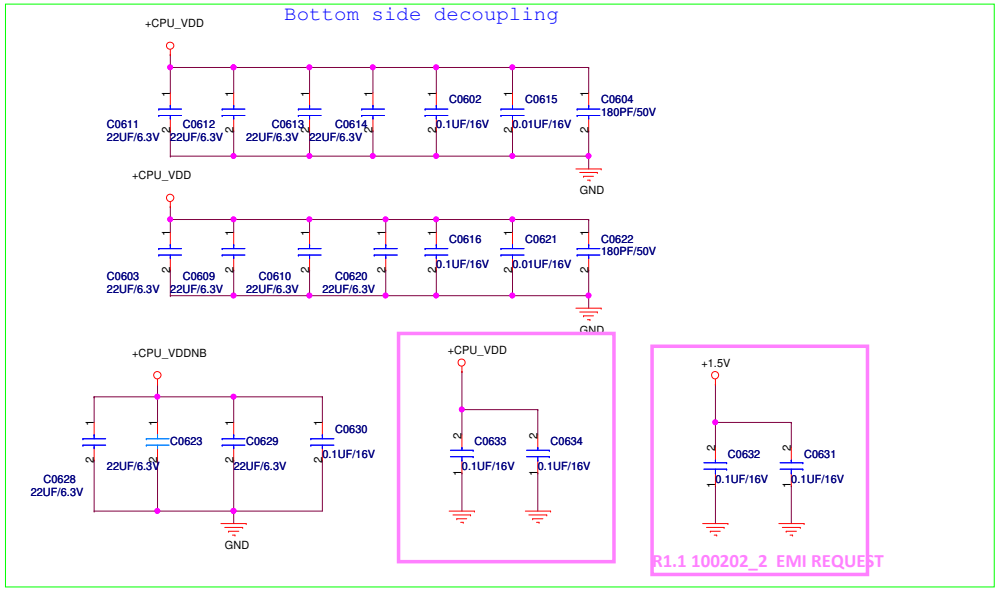
Title:	Intel Yonah DDR2 MEMORY I/F		
ASUSTeK COMPUTER INC. NB1		Engineer:	Vincent_Chiang
Size: C	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 4 of 93		

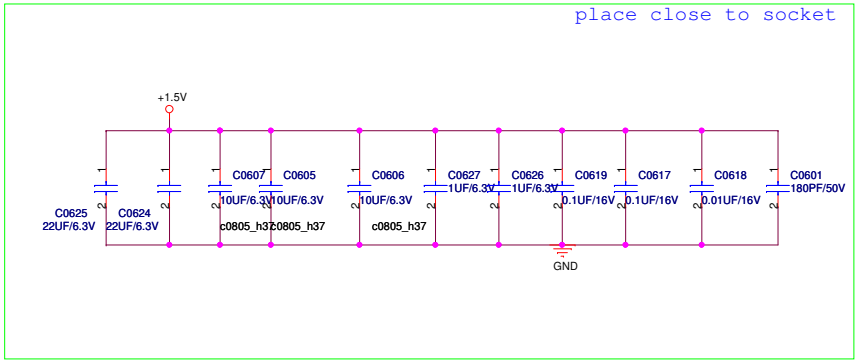

LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
0.25A
place them to CPU within 1.5"
route as diff
pair
5/5/5,10mil
08/11 change to 390OHM
Serial VID Interface clock/data
U0301D
SOCKET638
P0501
ASP_68200_07_K25
放在power
20080719
S1G4 does not support MEMHOT_L
0103 change R0527 R0529 R0533 TO 300ohm
to CPU
EC to CPU/PWR
From EC.
Title : Griffin CNTL/DEBUG/THERM
Engineer: Vincent_Chiang
ASUSTeK COMPUTER INC. NB1
Size C
Project Name K52N
Rev 1.0
Date: Monday, February 08, 2010
Sheet 5 of 93



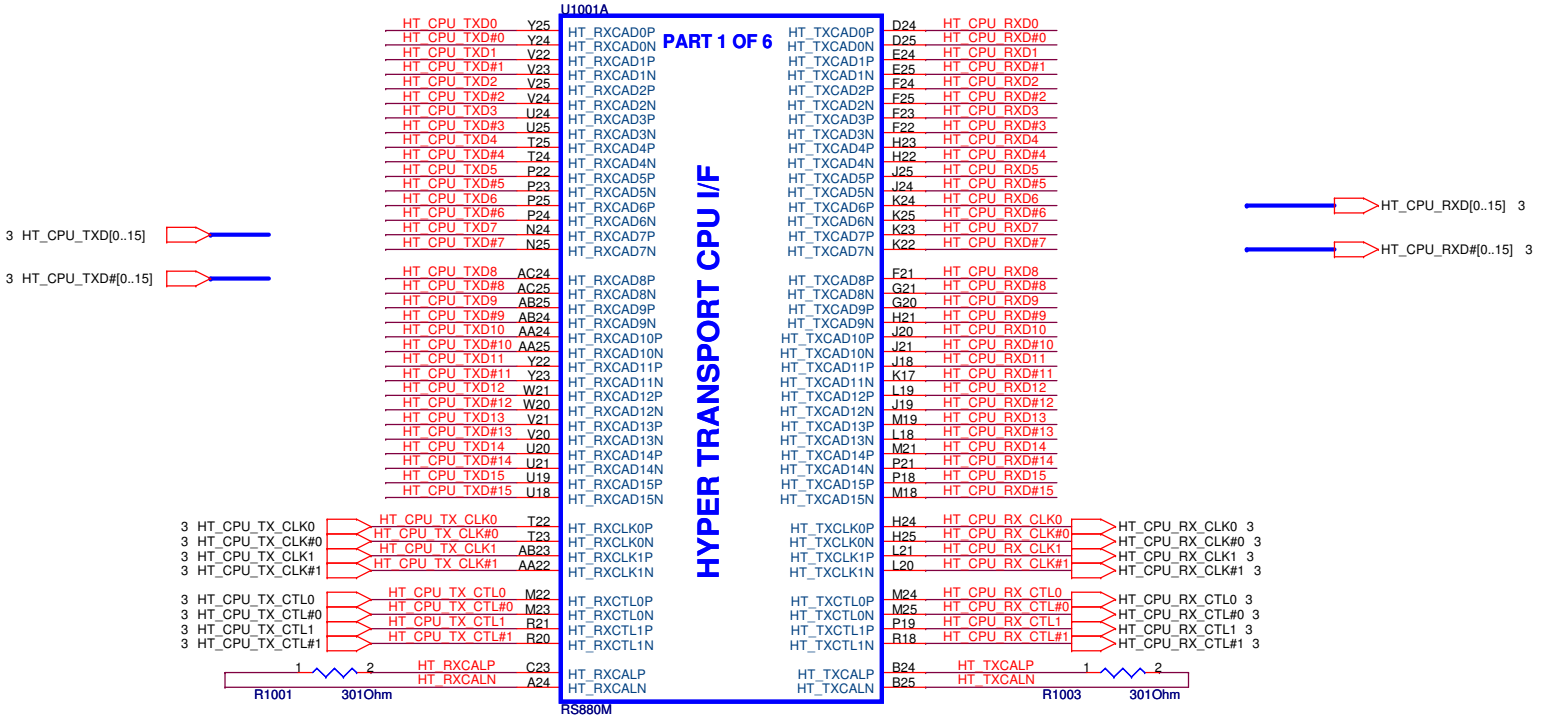


Decoupling between Processor and DIMMs, Place close to Porcessor as possible

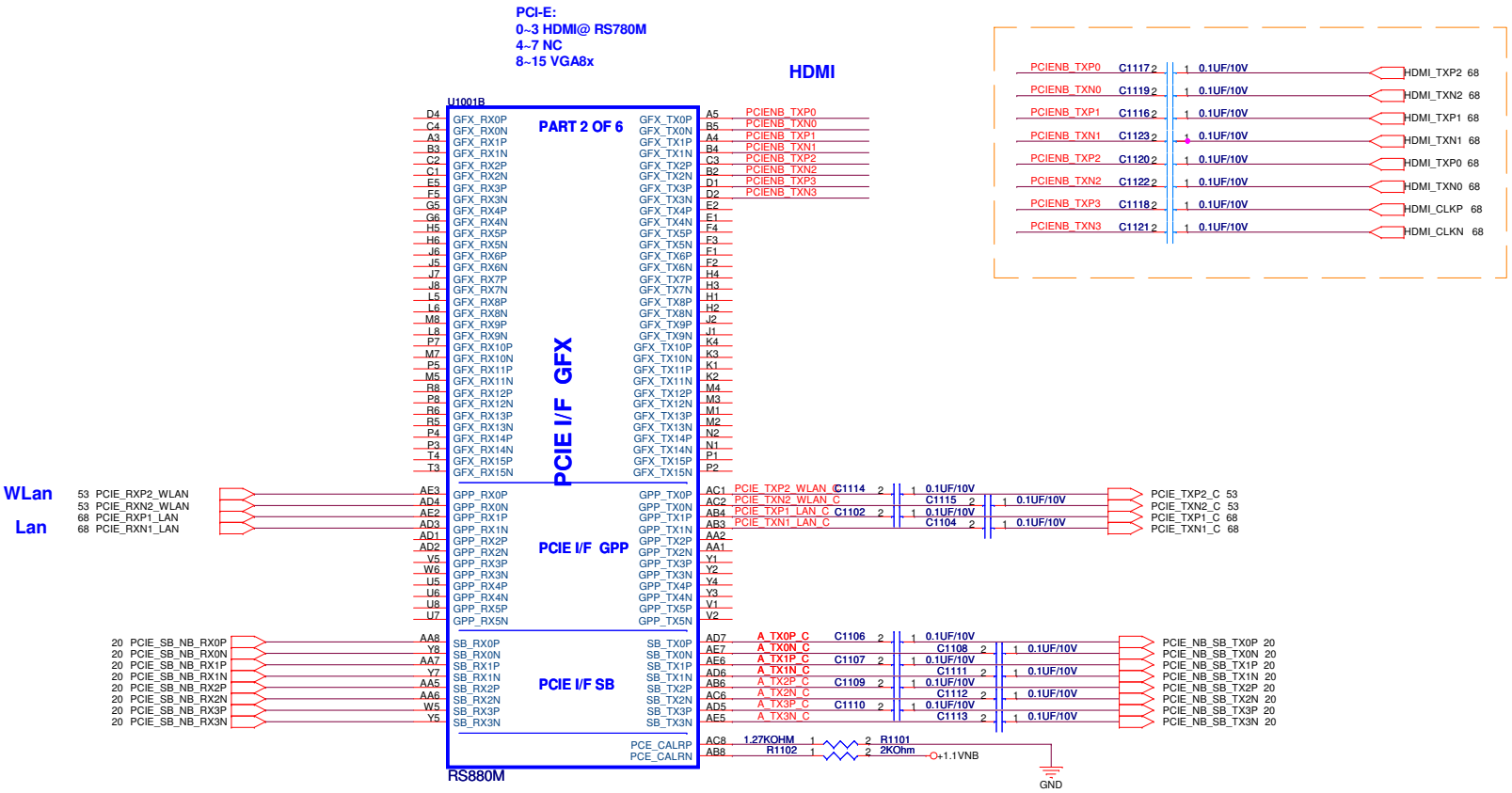




ASUSTeK COMPUTER INC. NB1	Title : Griffin POWER	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 6 of 93	



ASUSTeK COMPUTER INC. NB1	Title : RS880M-HT LINK I/F	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 10 of 93	



ASUSTeK COMPUTER INC. NB1	Title : RS880M-PCIE LINK I/F		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 11 of 93		

NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC/1.8V IN
LDT_STOP# IN(default)/IN	3.3V IN/OC

RS780 POWERGOOD is 1.8VS rail

Single channel

U1001C — RS880M — PART 3 OF 6

CRT/TVOUT: AVDD1, AVDD2, AVDDDI, AVSSDI, AVDDQ, AVSSQ, RESERVED1–4, RED, RED#, GREEN, GREEN#, BLUE, BLUE#, DAC_HSYNC, DAC_VSYNC, DAC_SDA, DAC_SCL, DAC_RSET

PLL PWR: PLLVDD, PLLVDD18, PLLVSS, VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

PM LVTM: SYSRESET#, POWERGOOD, LDTSTOP#, ALLOW_LDTSTOP

CLOCKs: HT_REFCLKP, HT_REFCLKN, REFCLK_P, REFCLK_N, GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP, GPPSB_REFCLKN

MIS.: I2C_DATA, I2C_CLK, DDC_DATA0/AUX0N, DDC_CLK0/AUX0P, DDC_CLK1/AUX1P, DDC_DATA1/AUX1N, STRP_DATA, AUX_CAL

TXOUT_L0P/L0N/L1P/L1N/L2P/L2N/L3P/L3N → LVDS_L0P_GPU … LVDS_L2N_GPU 45

TXOUT_U0P/U0N/U1P/U1N/U2P/U2N/U3P/U3N

TXCLK_LP/LN/UP/UN → LVDS_LCLKP_GPU, LVDS_LCLKN_GPU 45

VDDLTP18, VSSLTP18, VDDLTP18_PLL_L, VDDLTT18_1/2, VDDLT33_1/2 (VDDLT33 for 740 only), VSSLT1–7

LVDS_DIGON, LVDS_BLON, LVDS_ENA_BL → L_VDD_EN_GPU, NB_LCD_BL_PWM, L_BACKEN_GPU 45

TMDS_HPD, HPD → HDMI_HP 68

SUS_STAT# → SUS_STAT# 21

THERMALDIODE_P/N → T1205 TPC28T, T1204 TPC28T

TESTMODE

Check the VDDLT33 power connection

PR

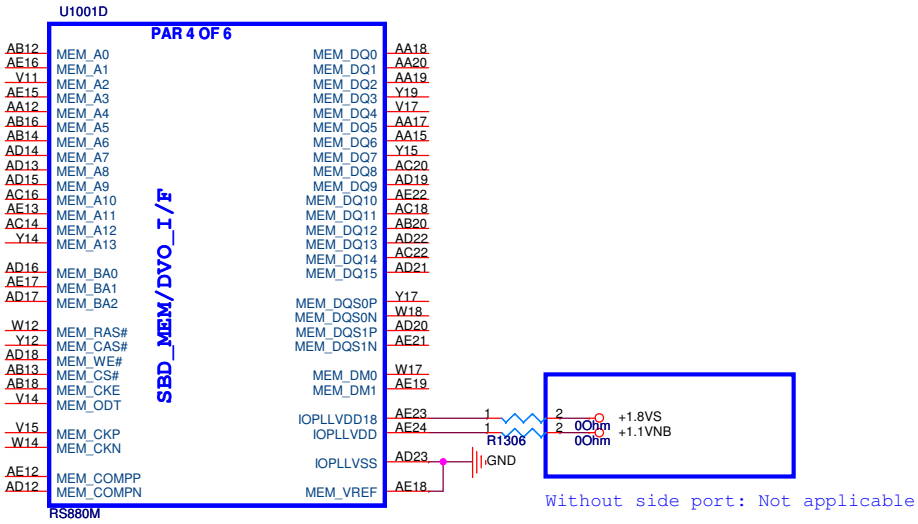
net AUC_CAL Refence F50z

STRP_DATA	0	1
VCC_NB	.95V	1.1V

R1.1 100127_1 Change EDID CLK/DAT Circuit

K52Dr

Title :	RS880M-SYSTEM I/F
ASUSTeK COMPUTER INC. NB1	Engineer: Vincent_Chiang
Size: Custom	Project Name: K52N
Rev: 1.0	
Date: Monday, February 08, 2010	Sheet 12 of 93



Without side port: Not applicable

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

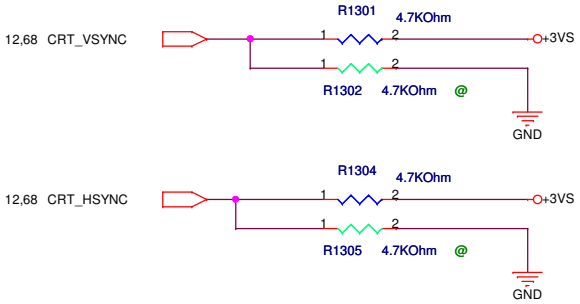
STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

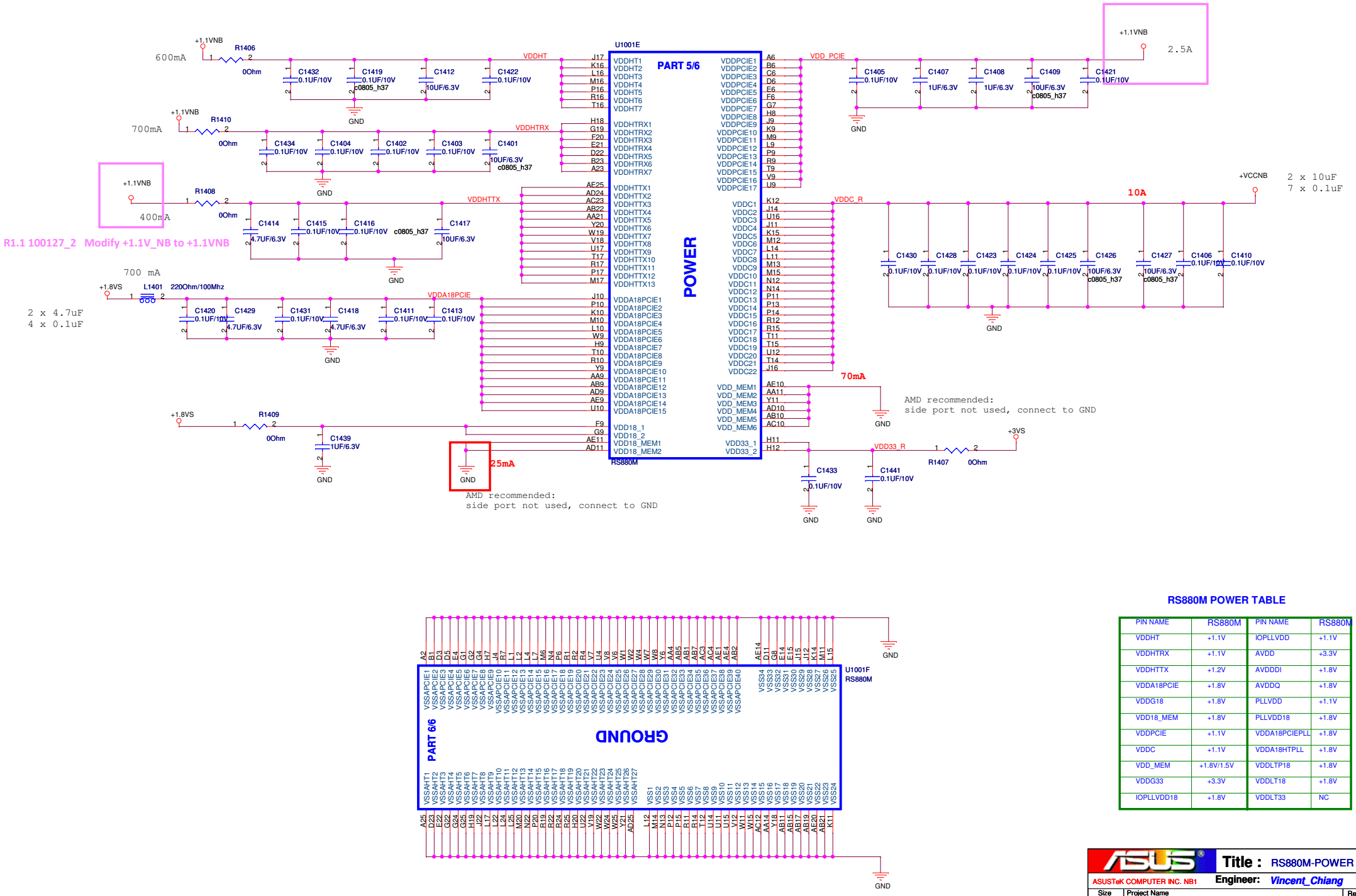
RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

080118
Disable Side Port Memory
R1.1



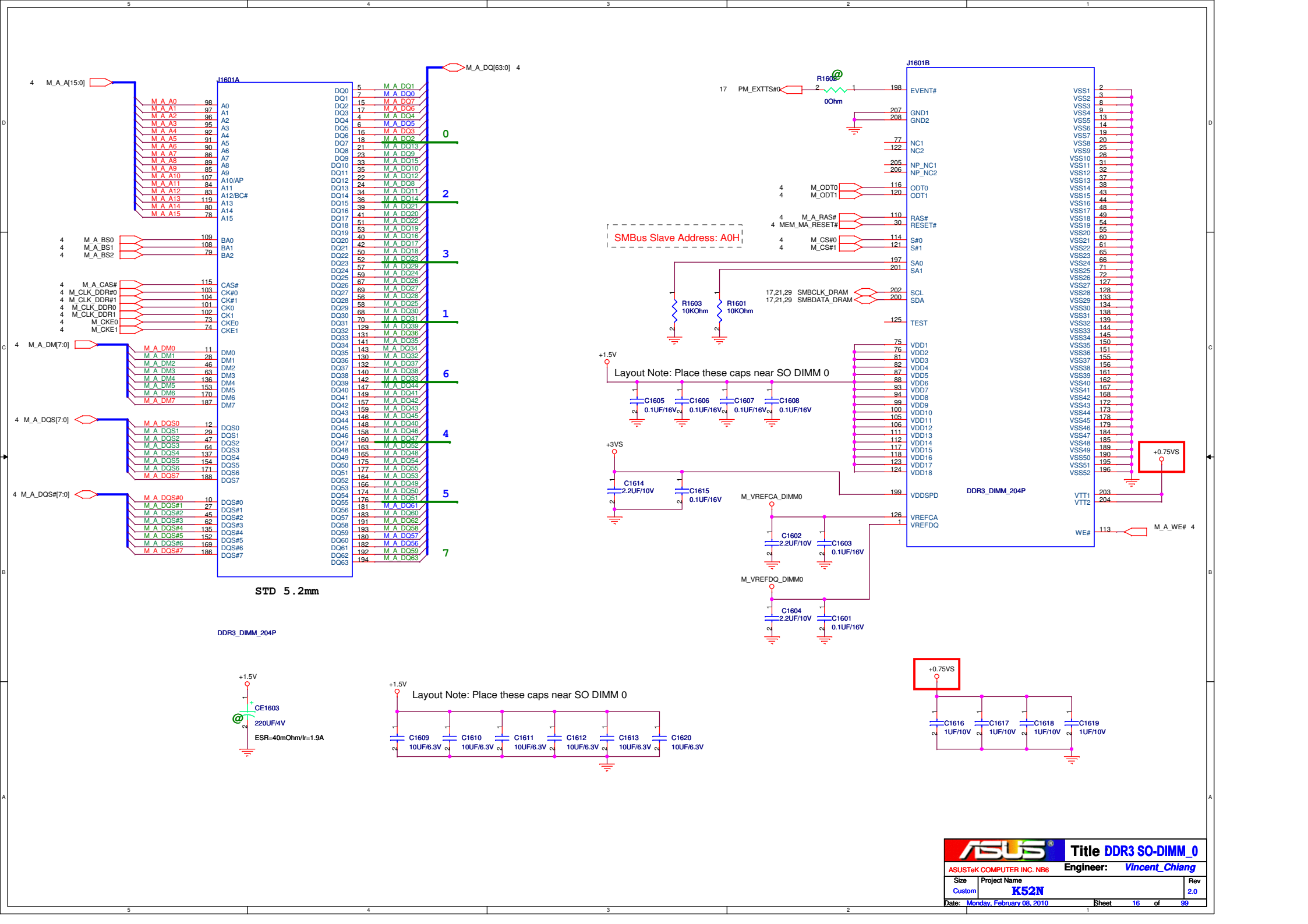
ASUSTeK COMPUTER INC. NB1	Title : RS880M-SPMEM/STRAPS	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 13 of 93	



RS880M POWER TABLE

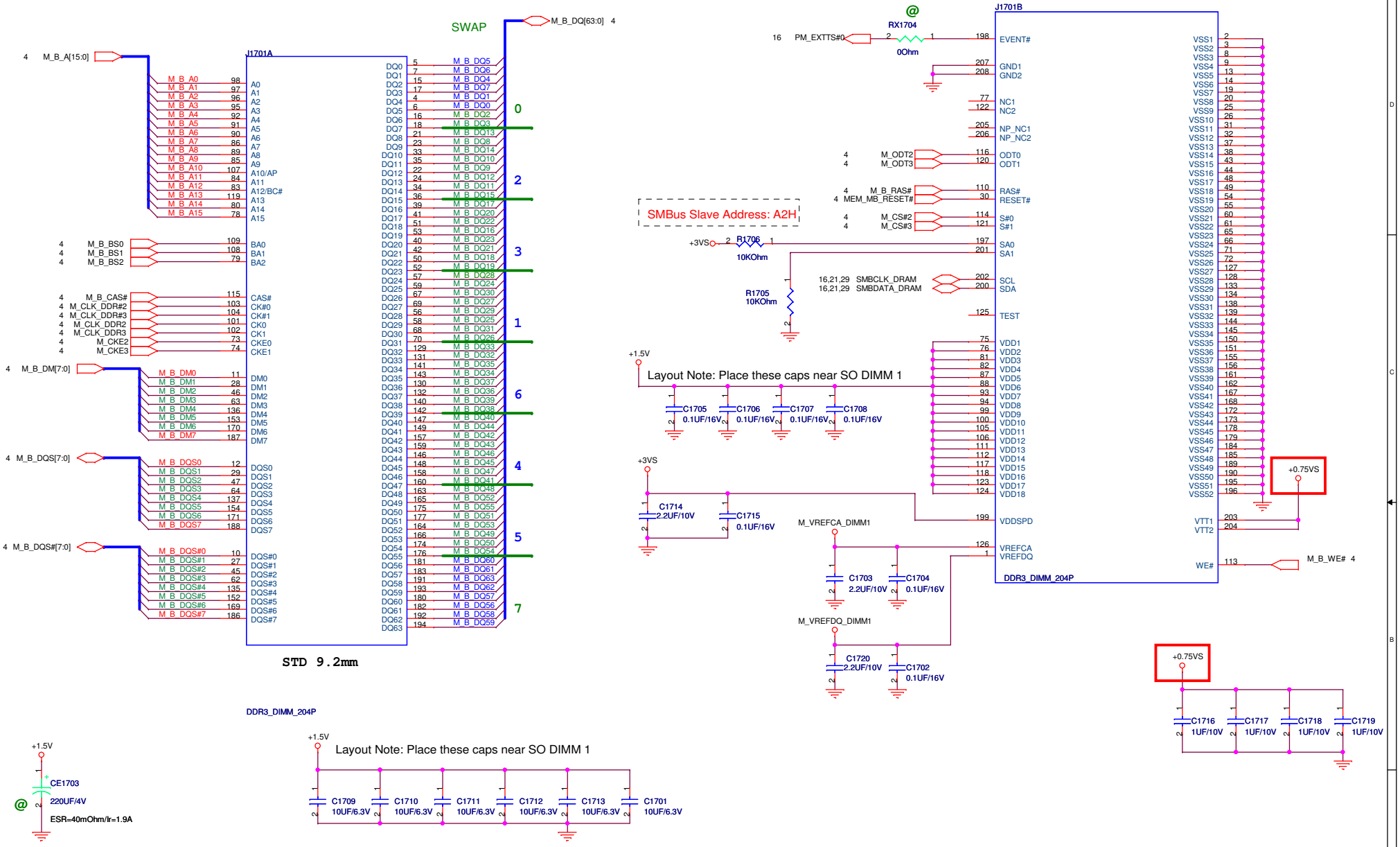
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

ASUSTeK COMPUTER INC. NB1	Title : RS880M-POWER		
	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 14 of 93		



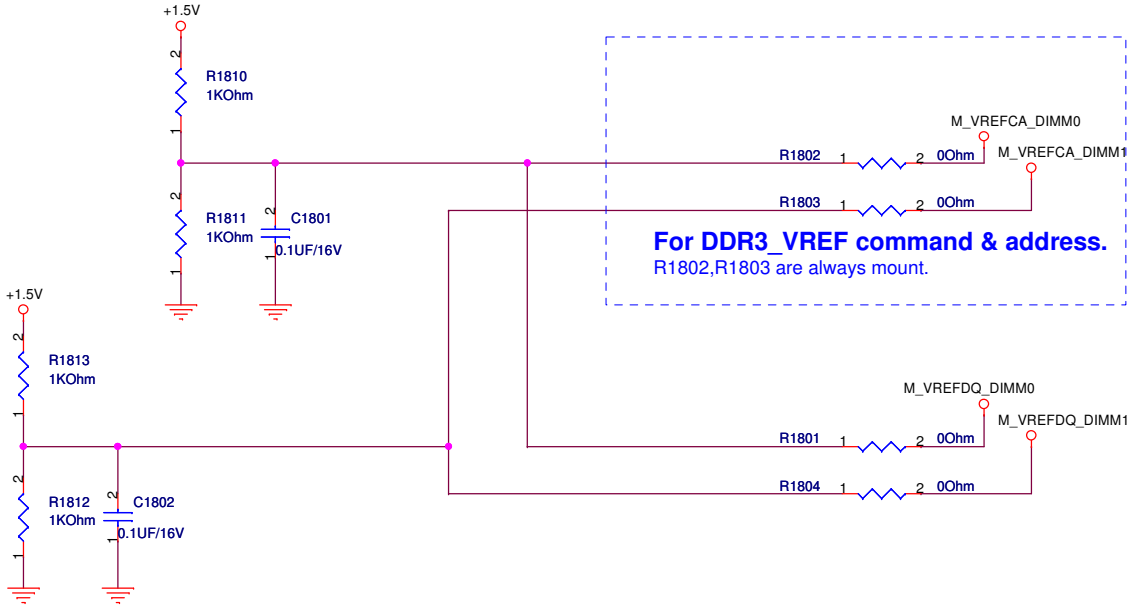
ASUSTeK COMPUTER INC. NB6	Engineer: Vincent_Chiang		
Size: Custom	Project Name: K52N		Rev: 2.0
Date: Monday, February 08, 2010	Sheet 16 of 99		

Title: DDR3 SO-DIMM_0

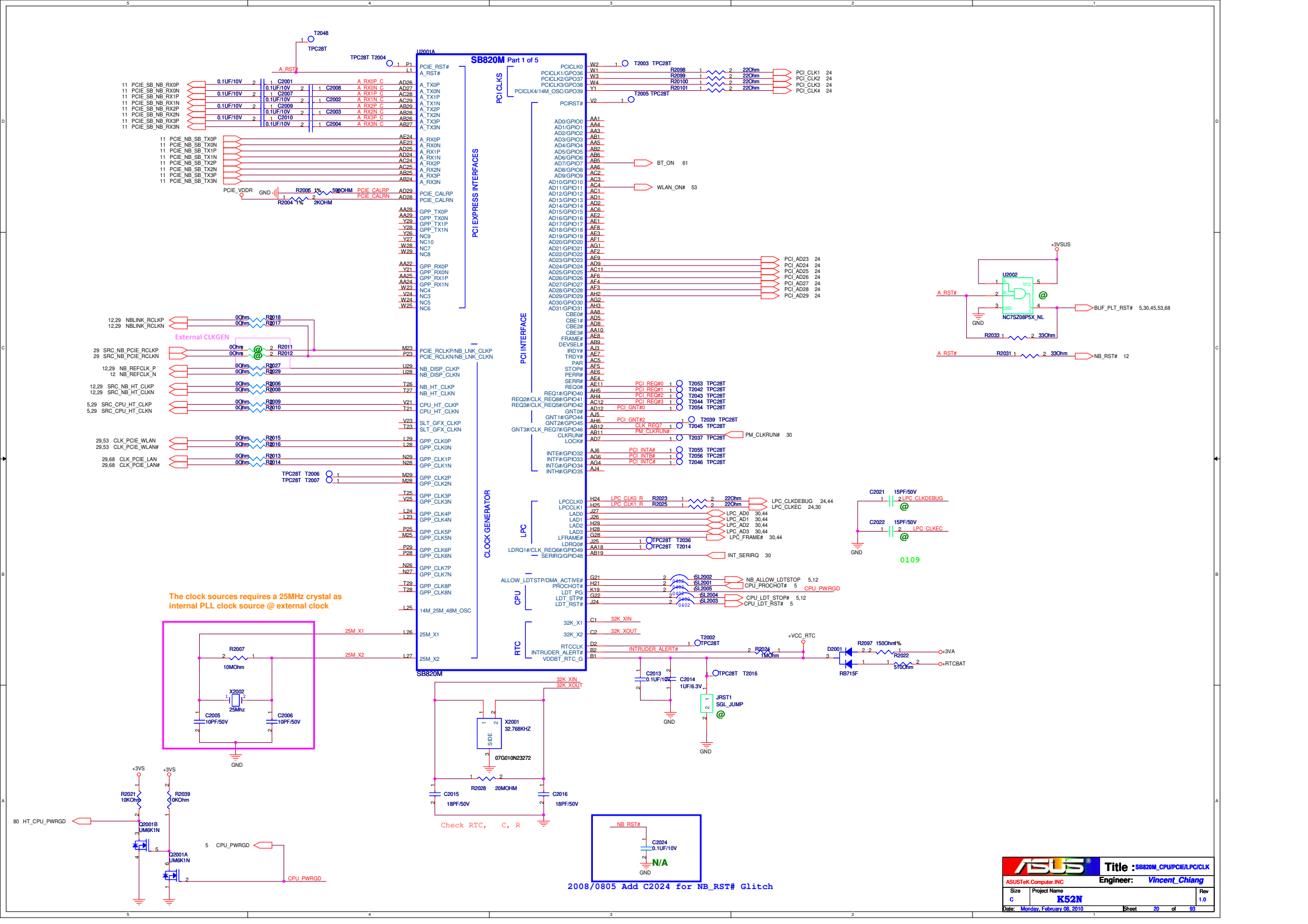


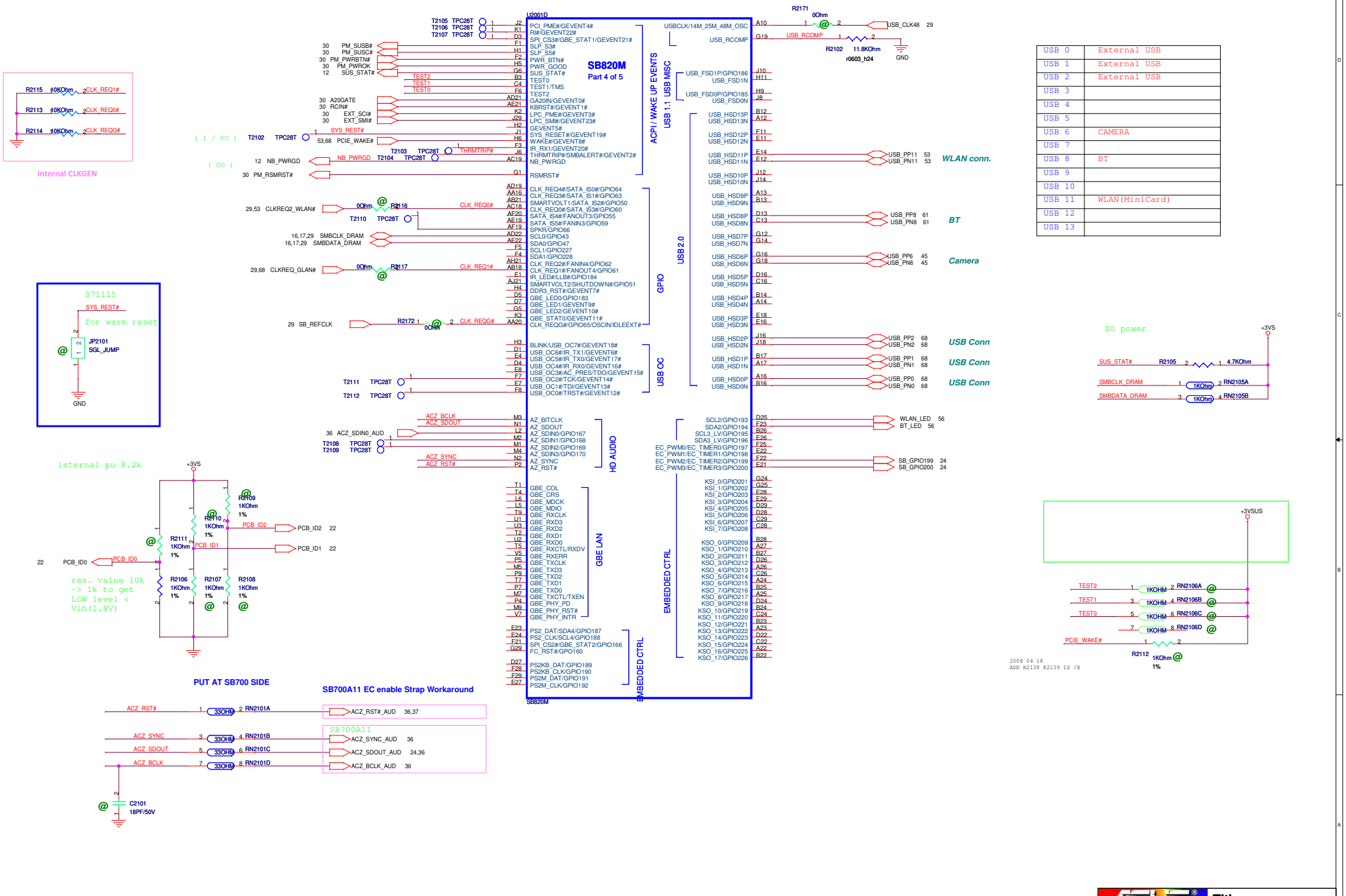
ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 17 of 99	

DDR3 Vref



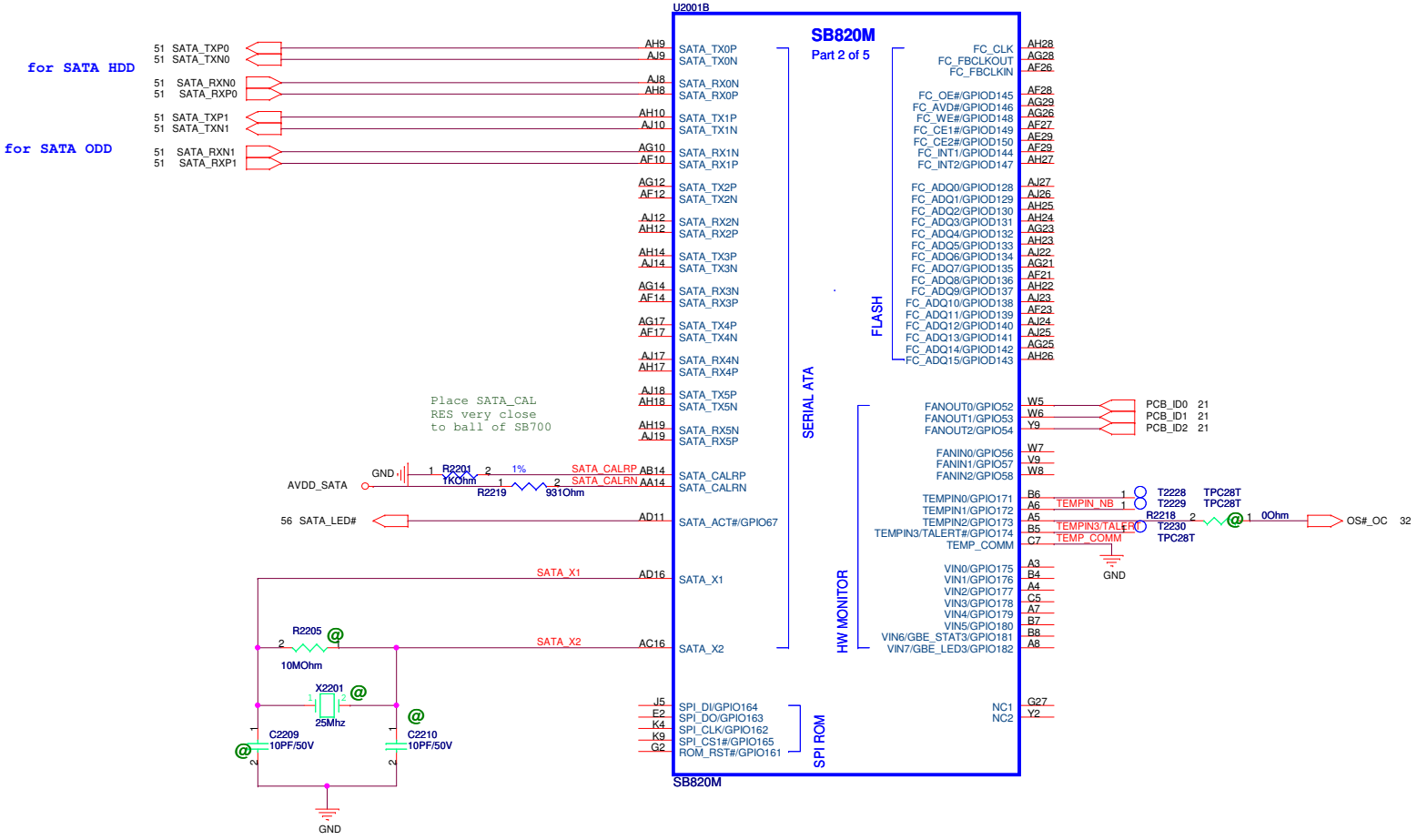
ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 18 of 99	


SB820M Part 1 of 5
U2001A
SB820M
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
PCI CLKS
LPC
CPU
RTC
External CLKGEN
The clock sources requires a 25MHz crystal as internal PLL clock source @ external CLK
Check RTC, C, R
2008/0805 Add C2024 for NB_RST# Glitch
Title : SB820M_CPU/PCIE/LPC/CLK
ASUSTeK.Computer.INC
Engineer: Vincent_Chiang
Project Name K52N
Rev 1.0
Date: Monday, February 08, 2010
Sheet 20 of 93



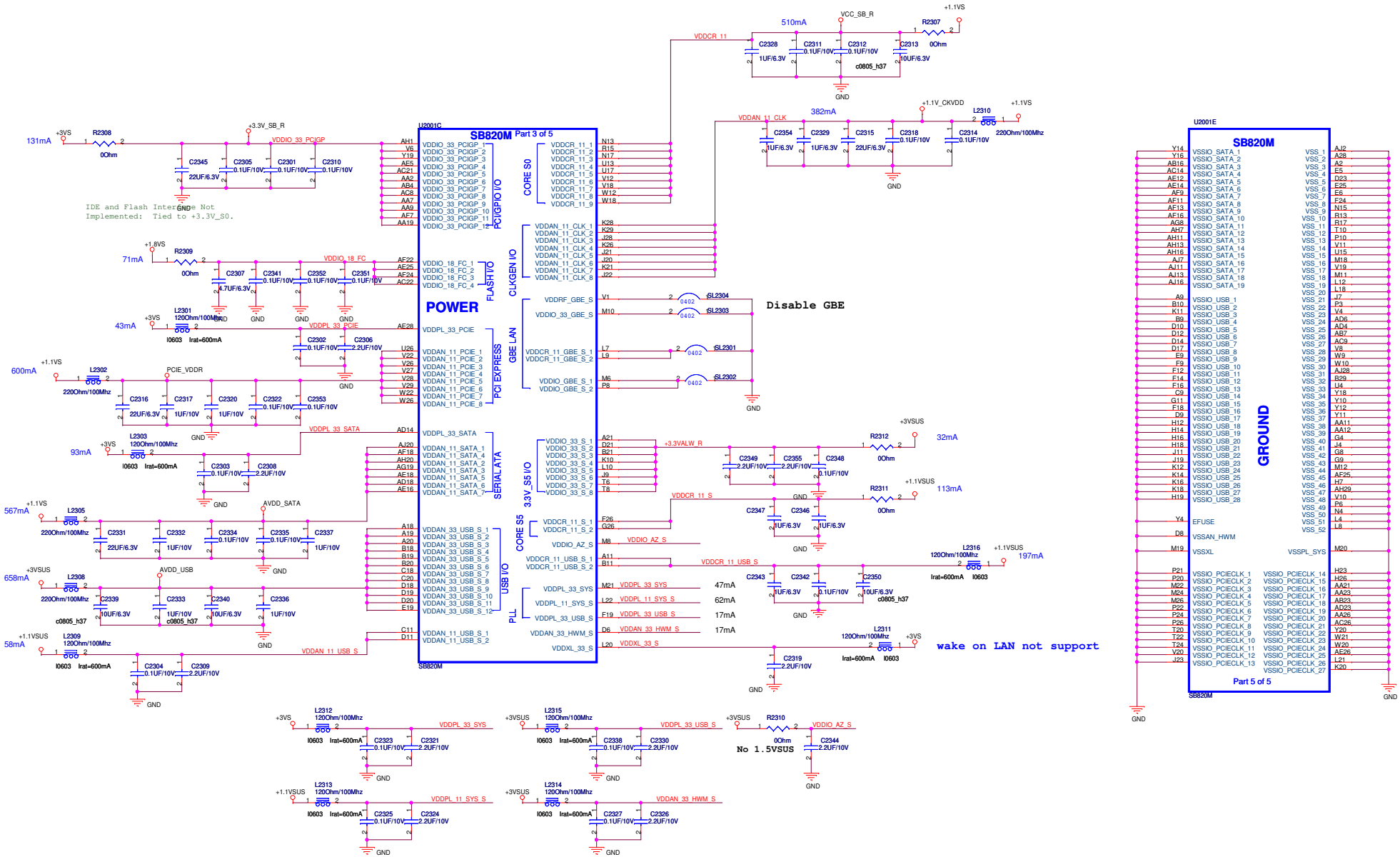
USB 0	External USB
USB 1	External USB
USB 2	External USB
USB 3	
USB 4	
USB 5	
USB 6	CAMERA
USB 7	
USB 8	BT
USB 9	
USB 10	
USB 11	WLAN(MiniCard)
USB 12	
USB 13	

ASUSTeK.Computer.INC	Title :	SB700_GPIO/USB/HD/ACPI	
	Engineer:	Vincent_Chiang	
Size: C	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 21 of 93		

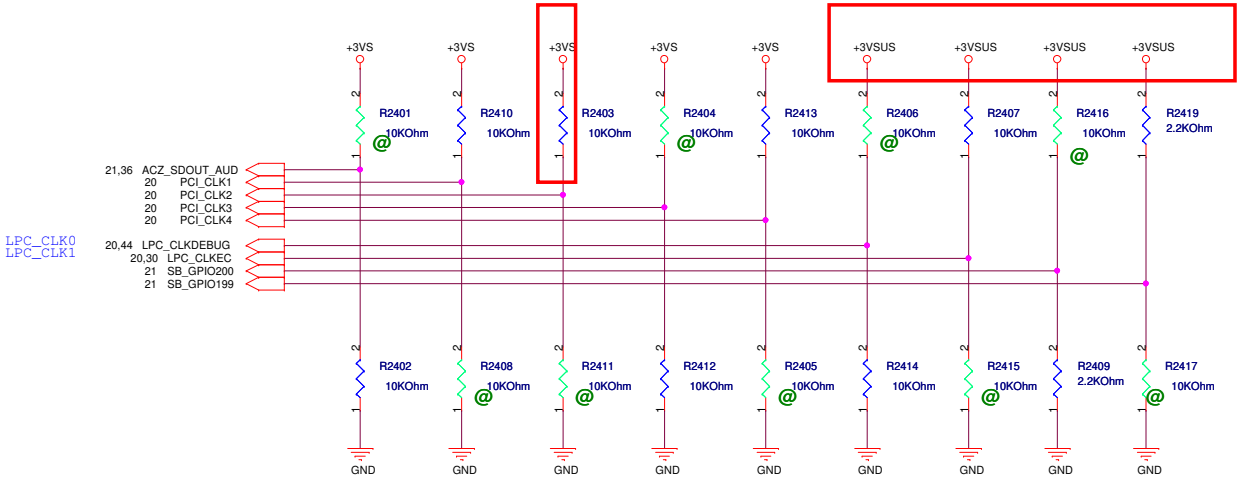


ASUSTeK.Computer.INC	Title : SB820M_PATA/SATA	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 22 of 93	

Check power Level and state

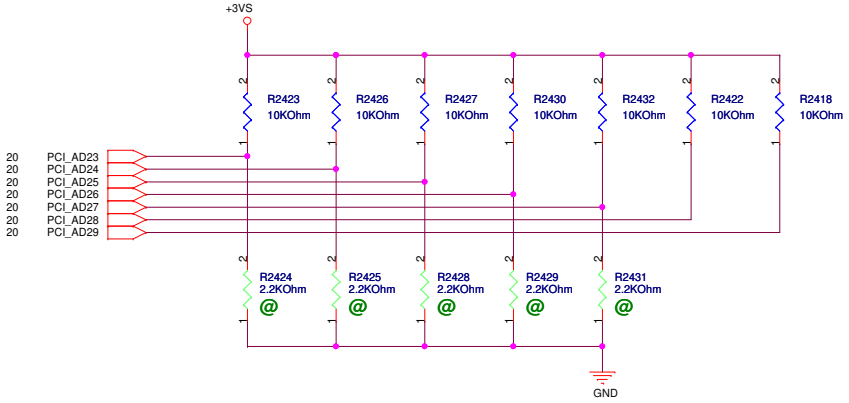


ASUSTeK.Computer.INC	Title : SB820M_POWER		
	Engineer: Vincent_Chiang		
Size: C	Project Name: K52N		Rev: 1.0
Date: Monday, February 08, 2010	Sheet 23 of 93		



REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled Modify	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

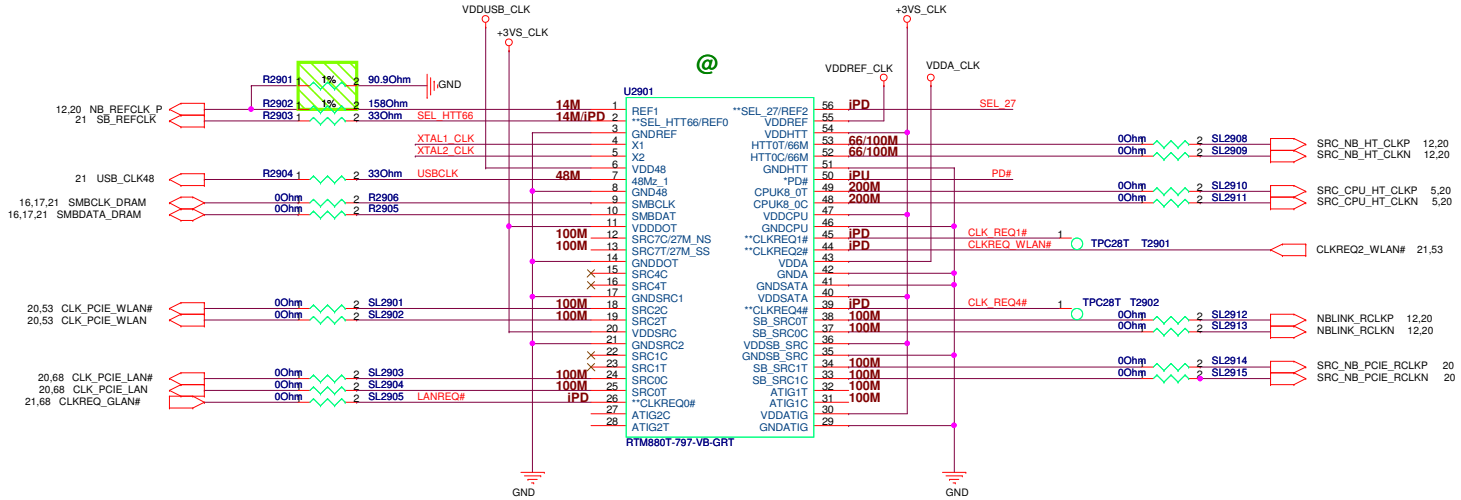
ASUSTeK.Computer.INC

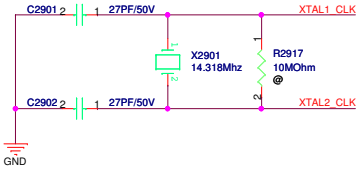
Title : SB820M_STRAP

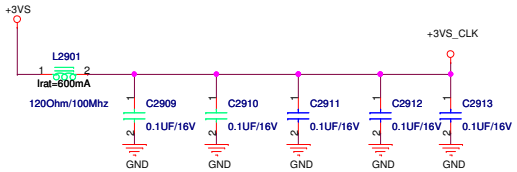
Engineer: Vincent_Chiang

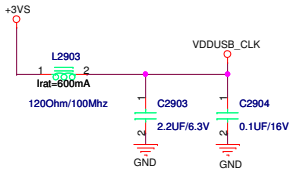
Size	Project Name	Rev
Custom	K52N	1.0

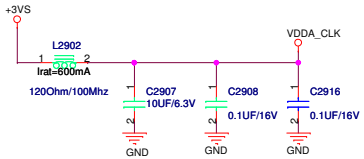
Date: Monday, February 08, 2010 Sheet 24 of 93

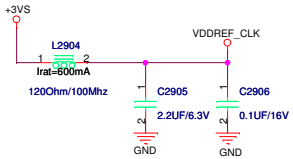


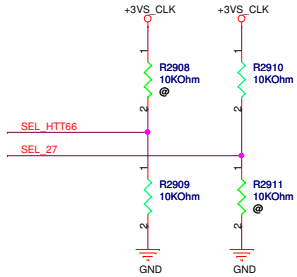






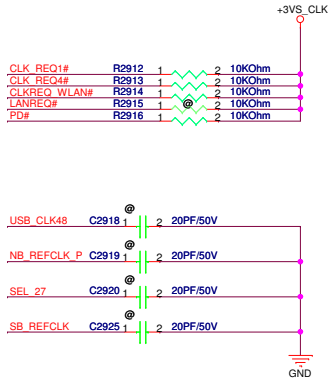






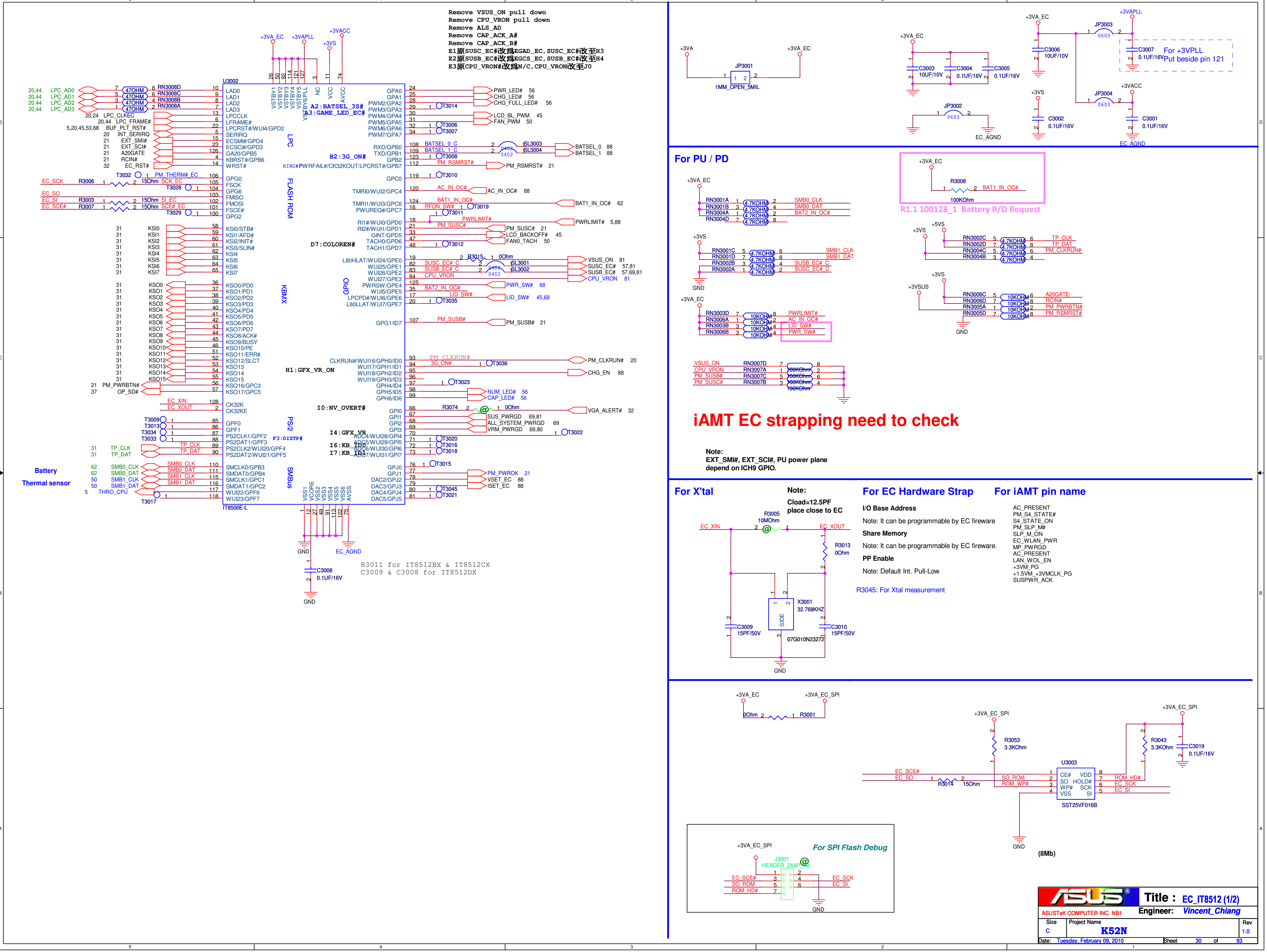
SEL_HTT66
0 : 100 MHz differential HTT clock (Default)
1 : 66MHz single ended HTT clock

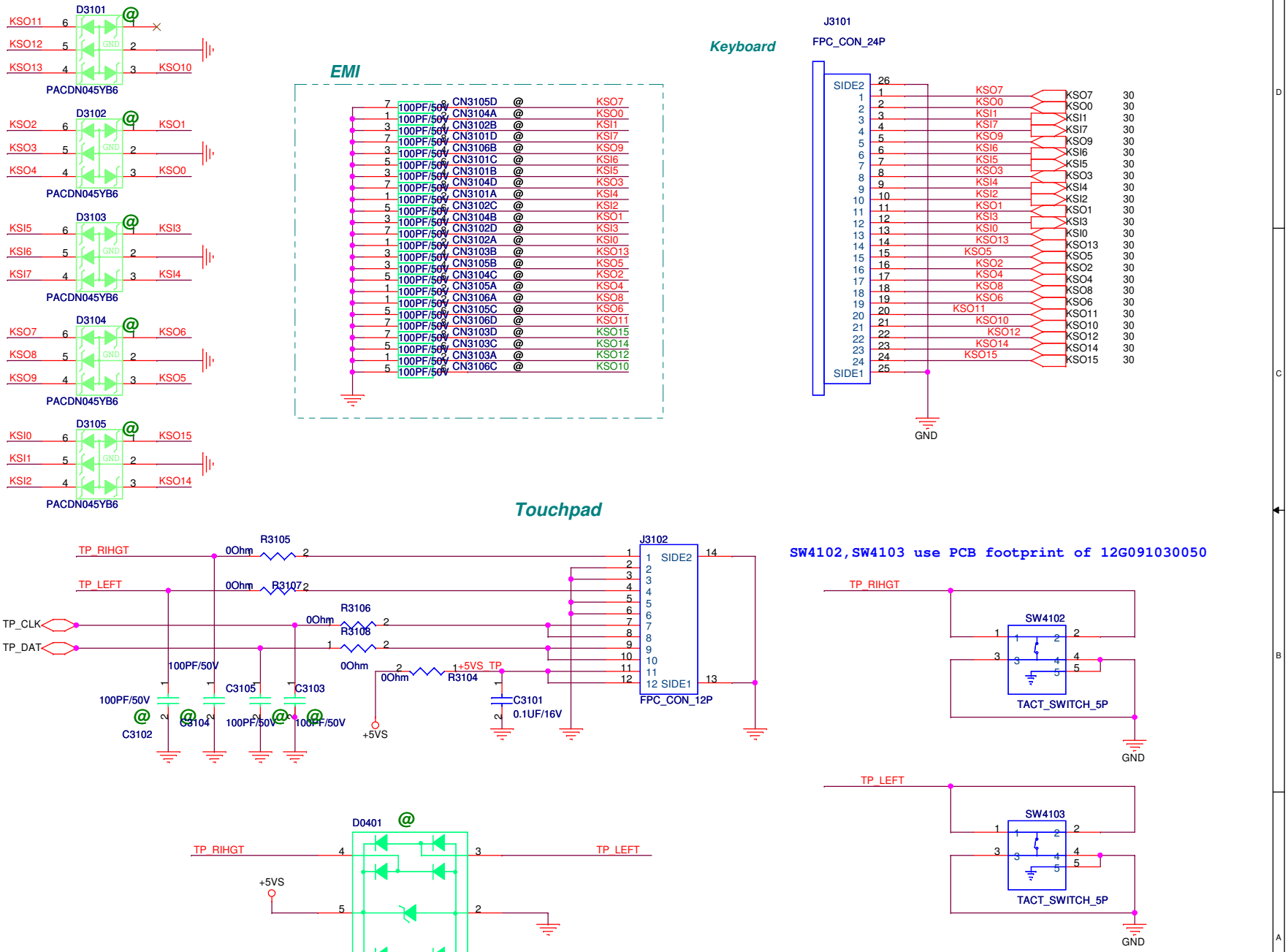
SEL_27
0 : 100 MHz differential Spread SRC clock
1 : 27MHz spread/non-spreading single clock (Default)



<Variant Name>

ASUSTeK COMPUTER INC	Title : ICS9LPRS489AGLFT	
	Engineer:	
Size: Custom	Project Name: K51AB	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 29 of 93	

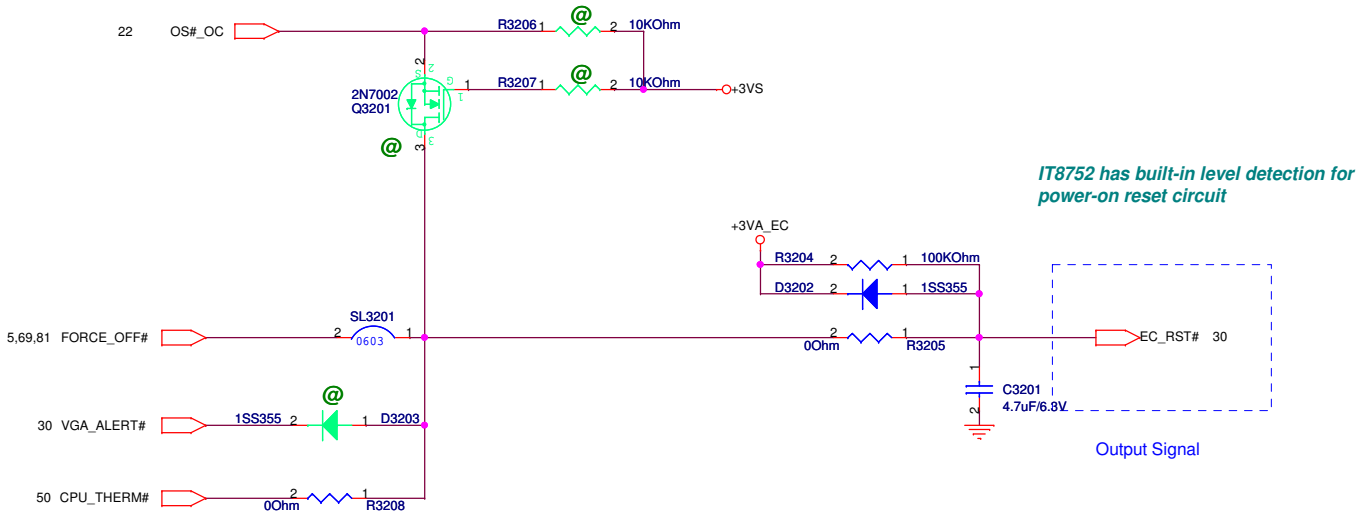

Remove VSUS_ON pull down
Remove CPU_VRON pull down
Remove ALS_AD
Remove CAP_ACK_A#
Remove CAP_ACK_B#
E1原SUSC_EC#改為EGAD_EC,SUSC_EC#改至H3
E2原SUSB_EC#改為EGCS_EC,SUSB_EC#改至H4
E3原CPU_VRON#改為N/C,CPU_VRON改至J0
U3002
IT8500E-L
R3011 for IT8512BX & IT8512CX
C3009 & C3008 for IT8512DX
Battery
Thermal sensor
For +3VPLL
Put beside pin 121
For PU / PD
R1.1 100128_1 Battery R/D Request
iAMT EC strapping need to check
Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.
For X'tal
Note:
Cload=12.5PF
place close to EC
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
R3045: For Xtal measurement
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
For SPI Flash Debug
SST25VF016B
(8Mb)
ASUSTeK COMPUTER INC. NB1
Title : EC_IT8512 (1/2)
Engineer: Vincent_Chiang
Size C
Project Name K52N
Rev 1.0
Date: Tuesday, February 09, 2010
Sheet 30 of 93



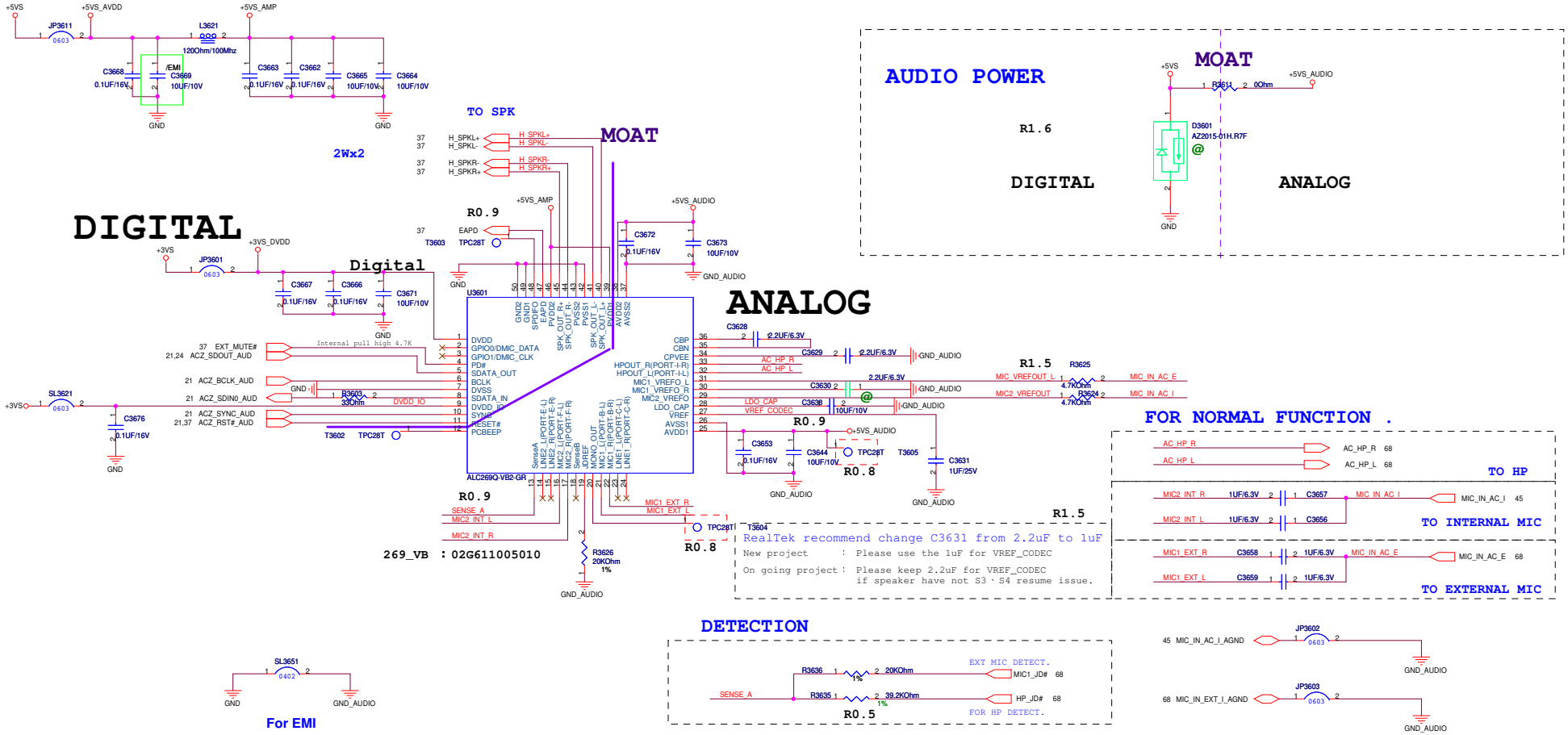
ASUSTeK COMPUTER INC. NB4	Title : EC_IT8541(2/2)KB, TP	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 31 of 99	

Thermal Policy

Main Board



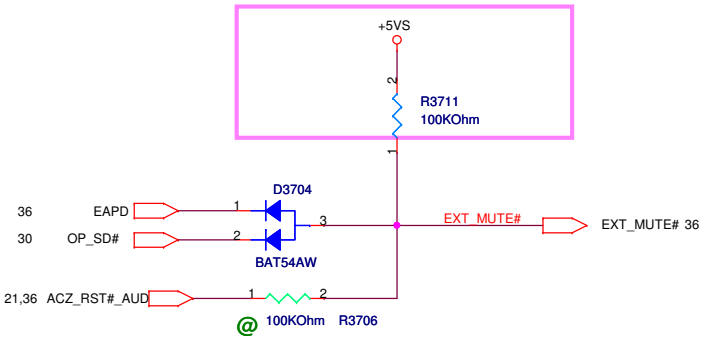
ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 32 of 99	



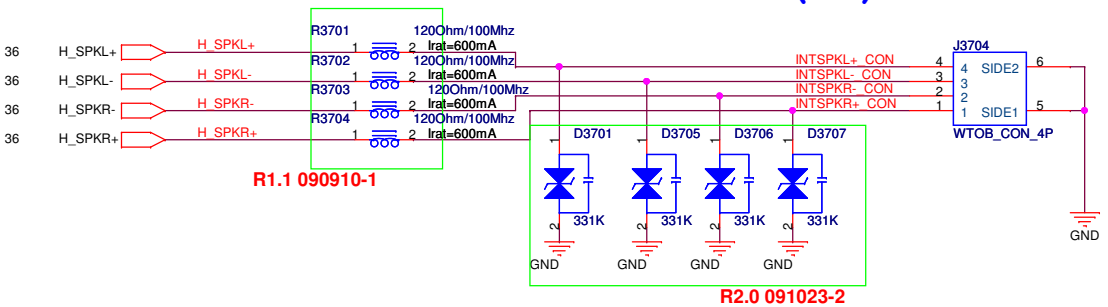
<variant_name>

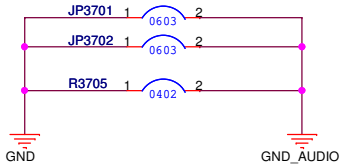
ASUSTeK COMPUTER INC. NB2	Title : CODEC ALC 269	
	Engineer: Leon	
Size: C	Project Name: K52Jr	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 36 of 99	

R1.1 100129_1 Change +3VS to +5VS



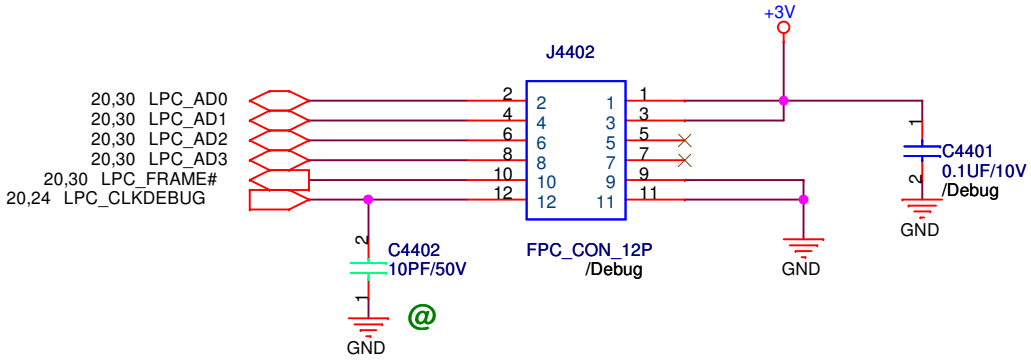
SPEAKER CONNECTOR (2W)



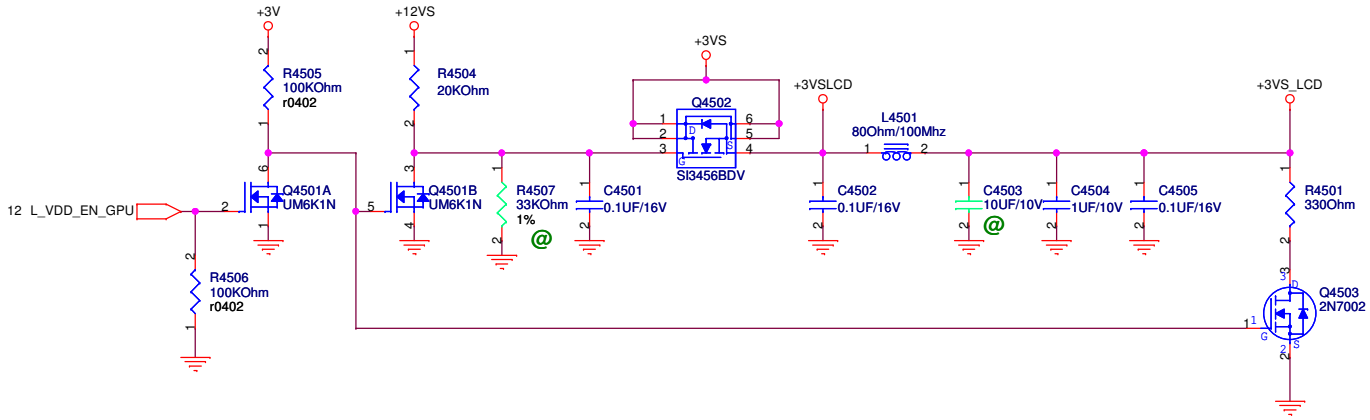


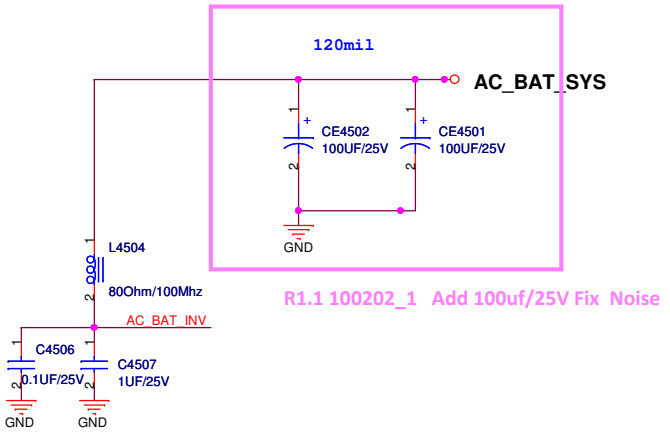
ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP	
	Engineer: Leon	
Size: B	Project Name: K52Jr	Rev: 2.0
Date: Monday, February 08, 2010	Sheet 37 of 99	

LPC Debug Port



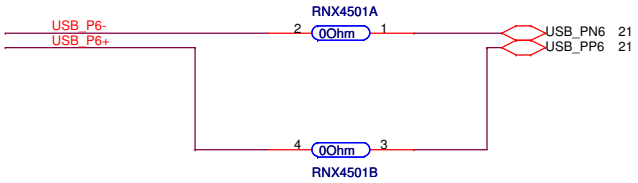
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 44 of 99	

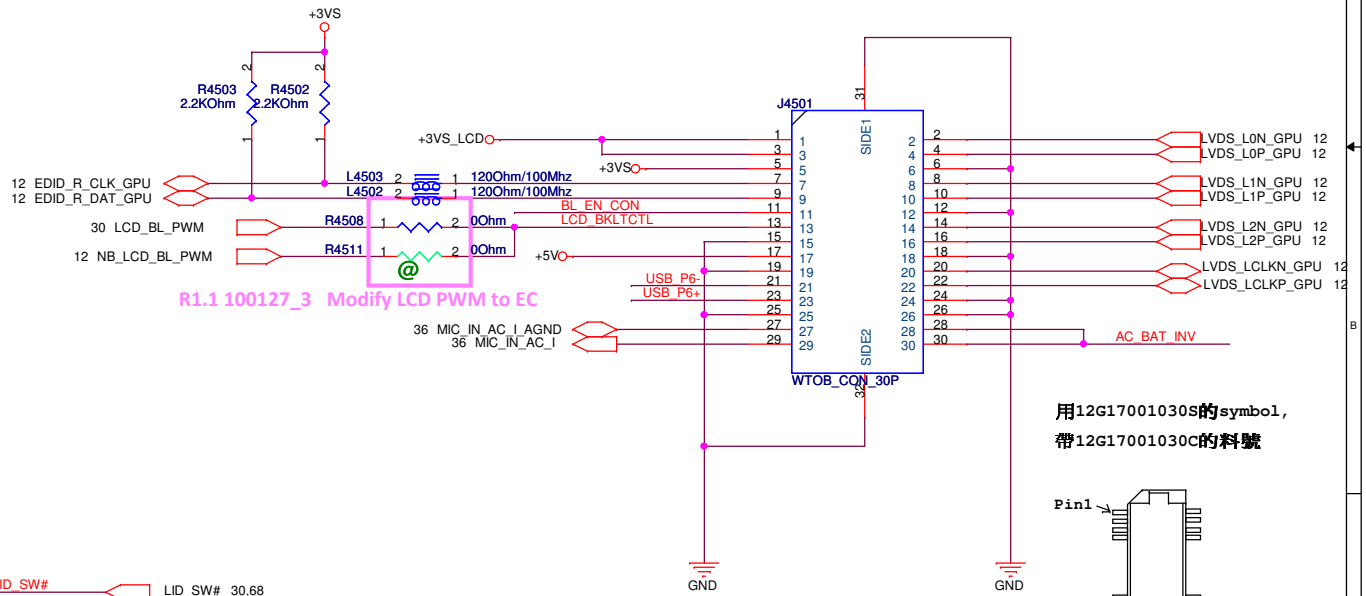




R1.1 100202_1 Add 100uf/25V Fix Noise

CAMERA & MIC

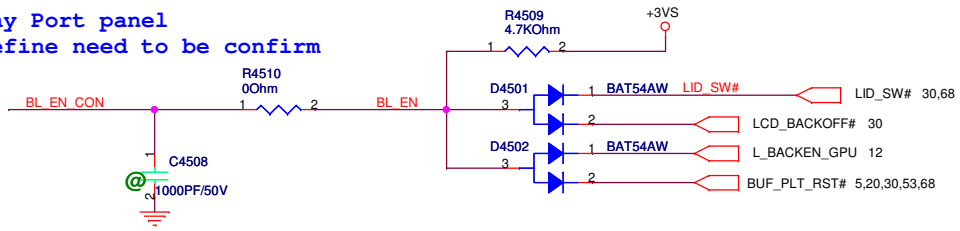




R1.1 100127_3 Modify LCD PWM to EC

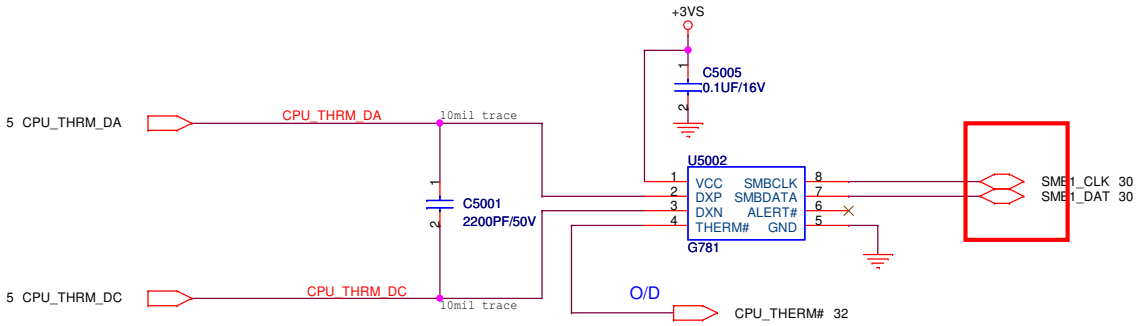
用12G17001030S的symbol,
帶12G17001030C的料號

Display Port panel pin define need to be confirm



ASUSTeK COMPUTER INC. NB4	Title : CRT_LCD Panel	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 45 of 99	

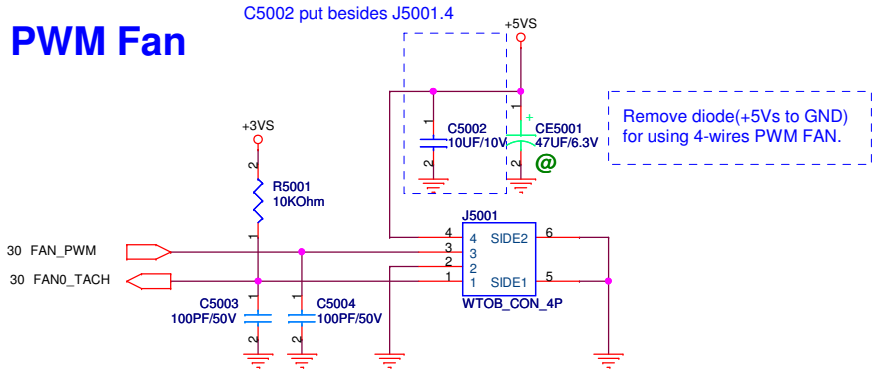
CPU Thermal Sensor



SMBUS addr=1001100x (98)

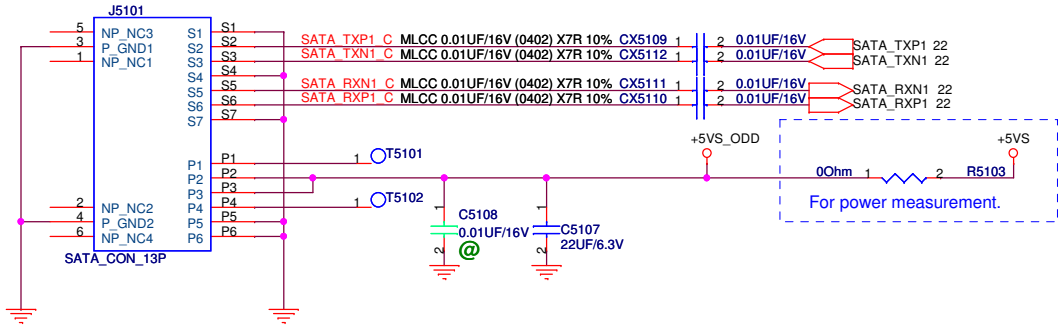
U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan

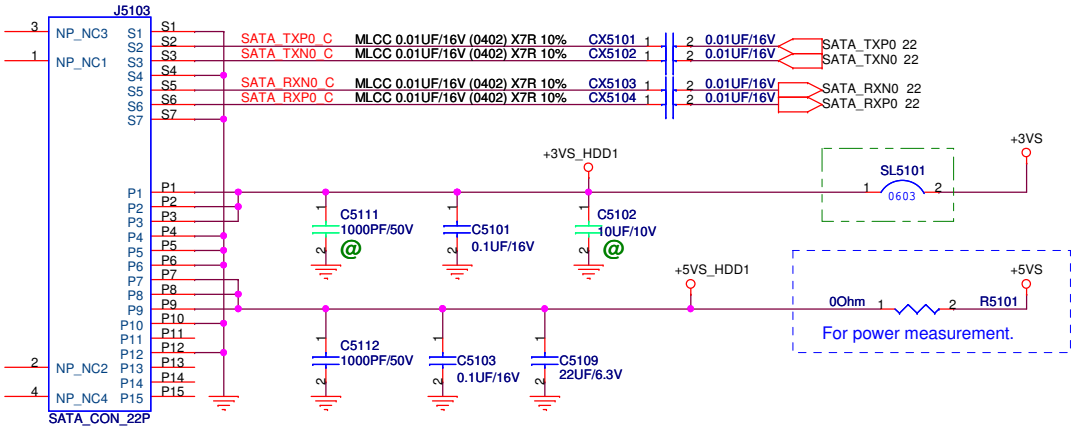


ASUSTeK COMPUTER INC. NB4	Title : FAN_Fan & Sensor	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 50 of 99	

ODD



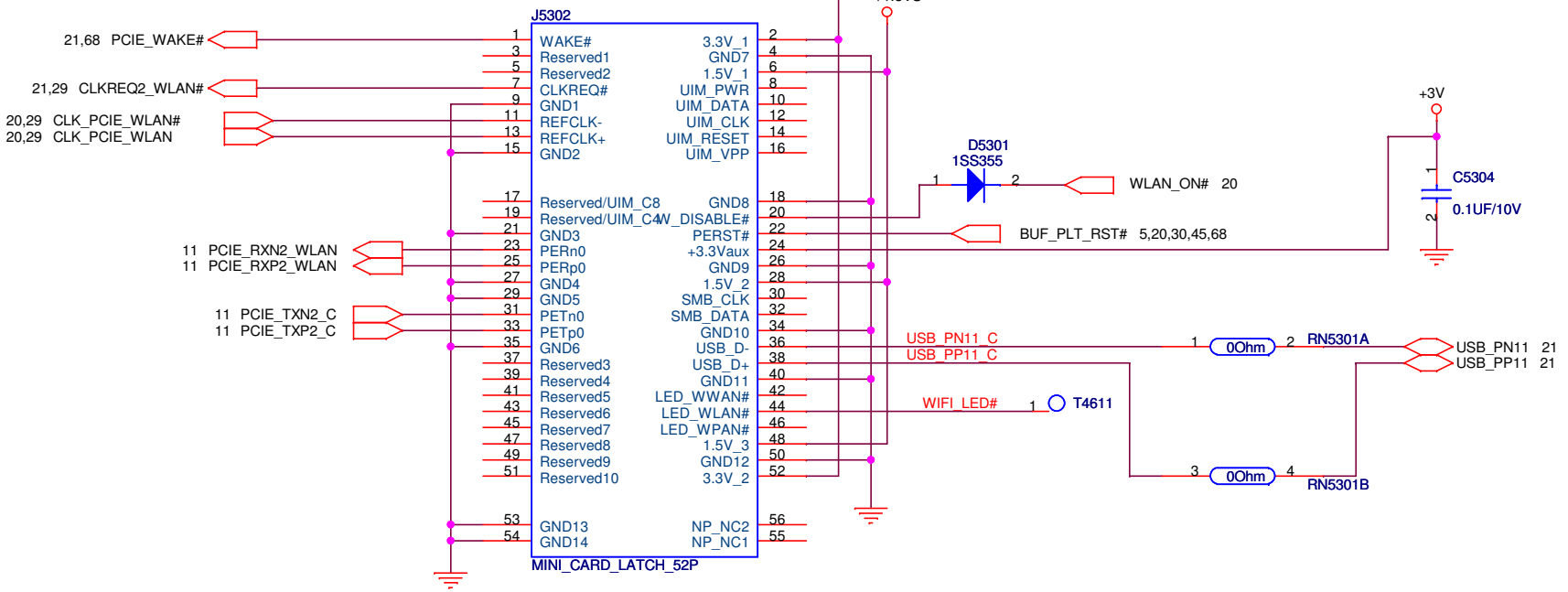
HDD (1st)



ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 51 of 99	

Suppport wake from S3 only

使用12G03010052F symbol

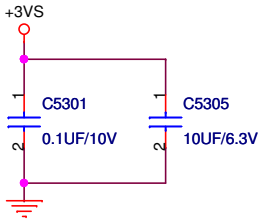


WLAN

WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

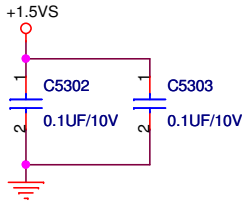
Place 10UF near +3VAUX_WLAN source side.



WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

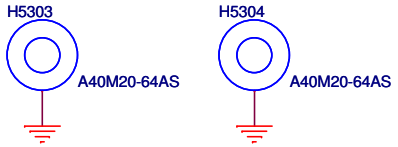


WLAN nuts:

Minicard spec R1.2:

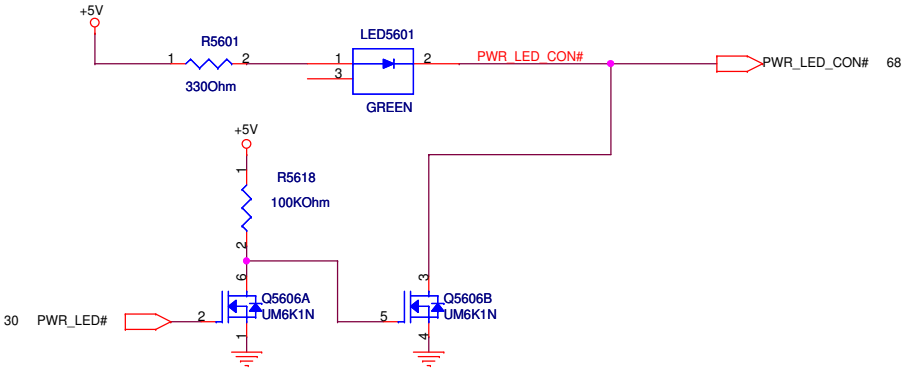
Full size card= 2pcs.

Half size card= 2pcs.

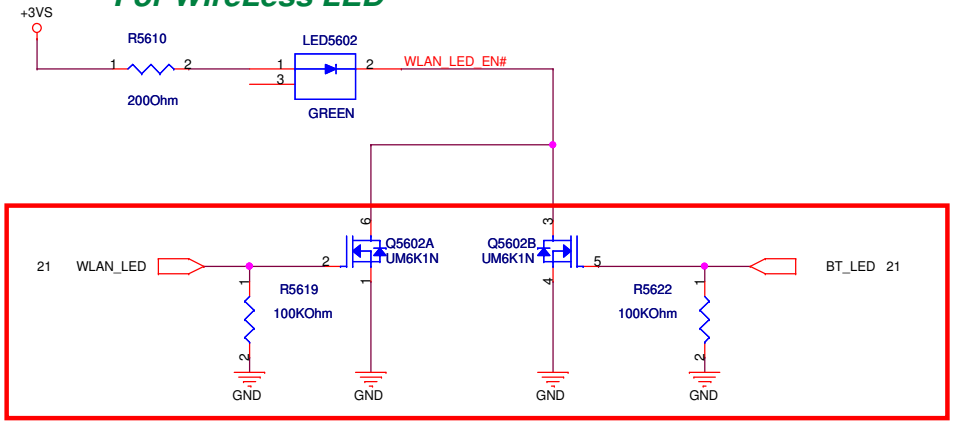


ASUSTeK COMPUTER INC. NB6	Title : MINICARD(WLAN)	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 53 of 99	

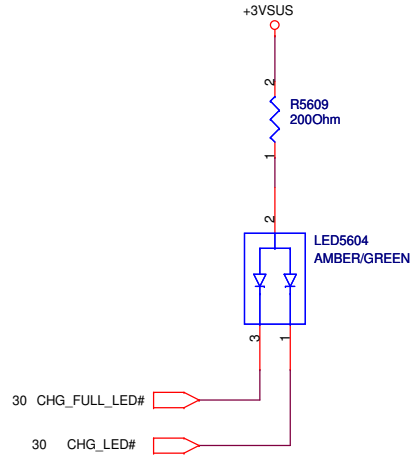
For POWER LED



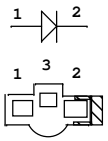
For WireLess LED



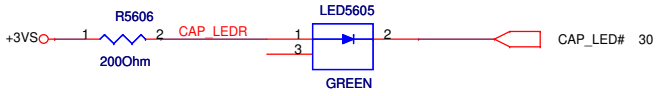
Charge LED



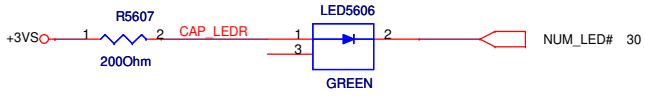
Side Light LED symbol



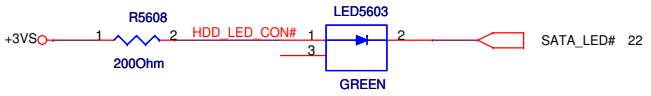
Cap. Lock LED



for Num Lock



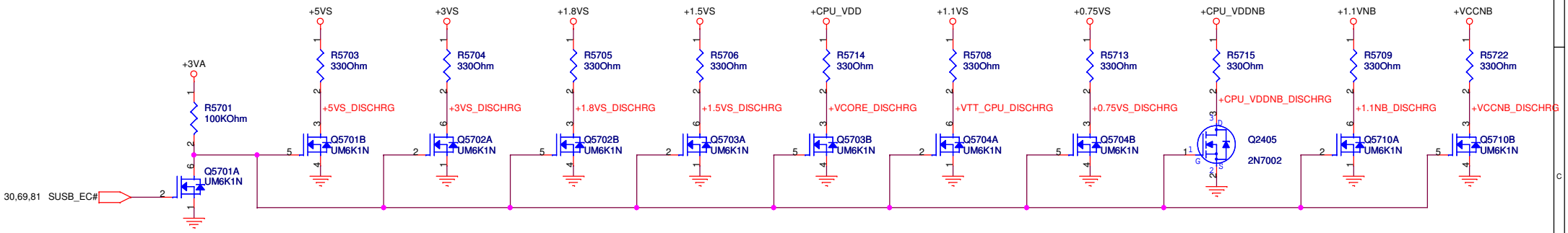
HDD LED

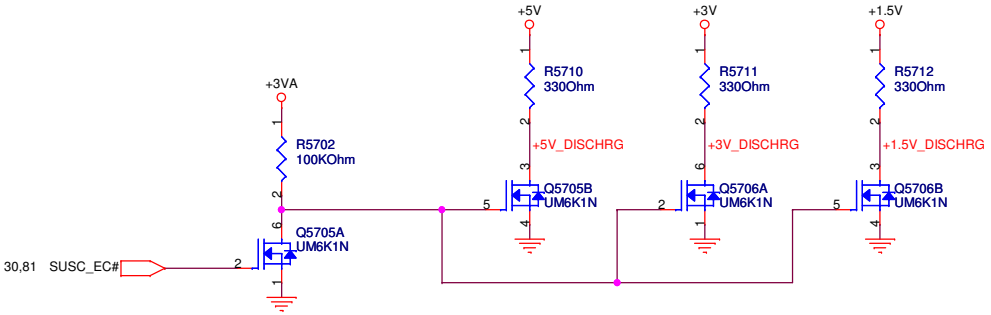


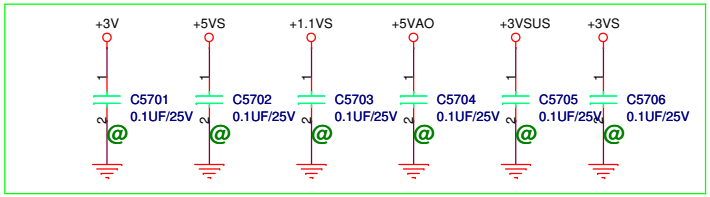
ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 56 of 99	

Main Board

Remove +2.5Vs is for ATI GFX

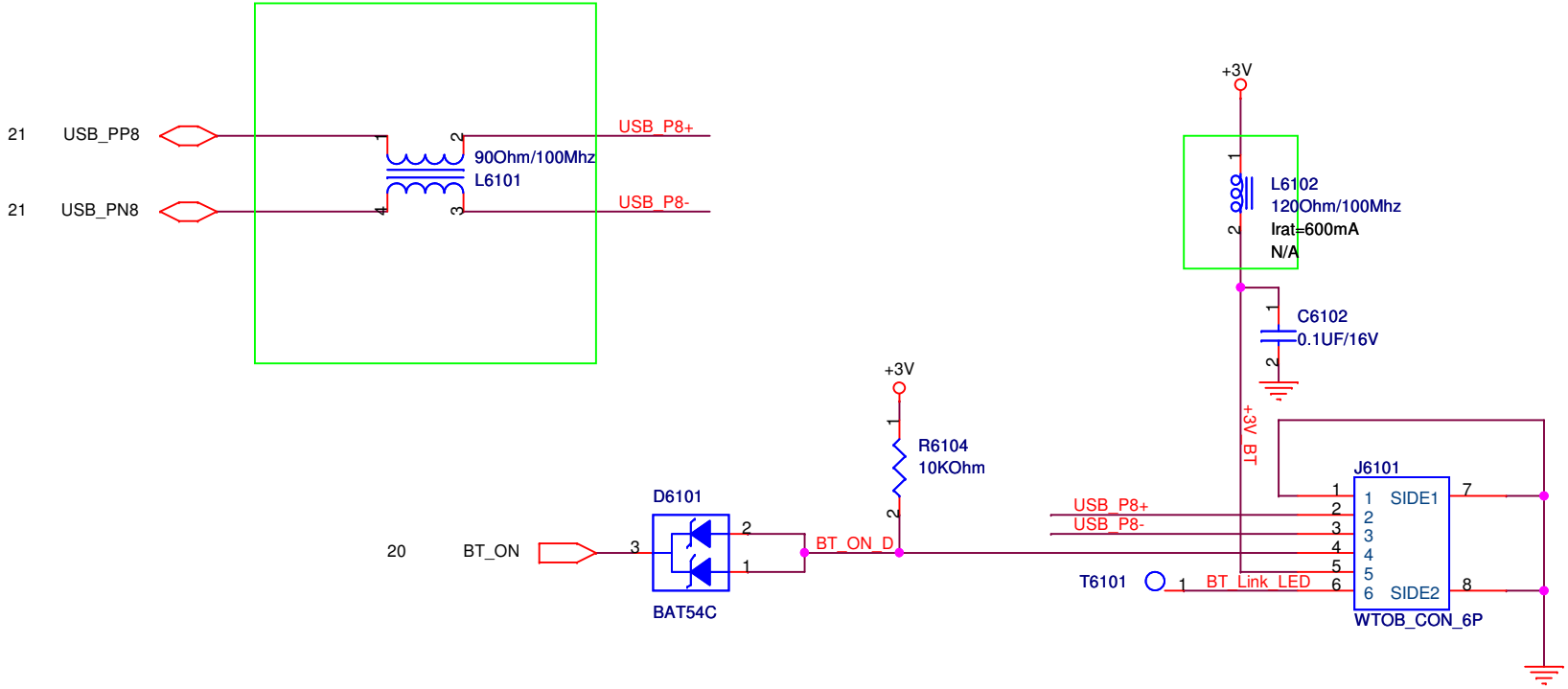






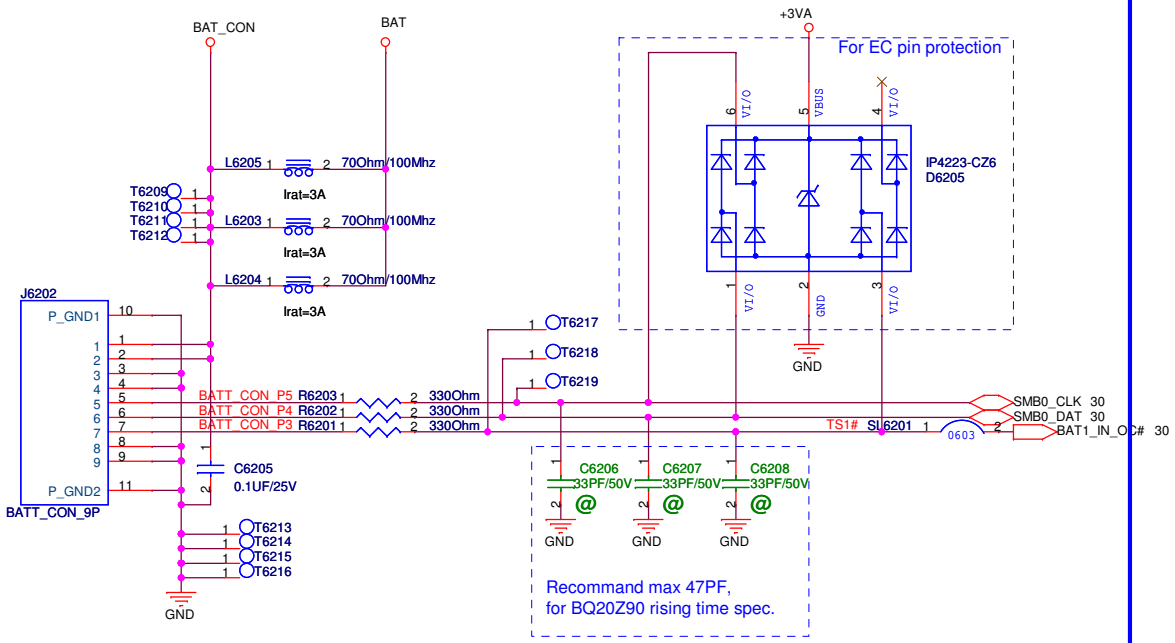
ASUSTeK COMPUTER INC. NB4	Title : DSG_Discharge	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 57 of 99	

BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 61 of 99	

Battery Connector

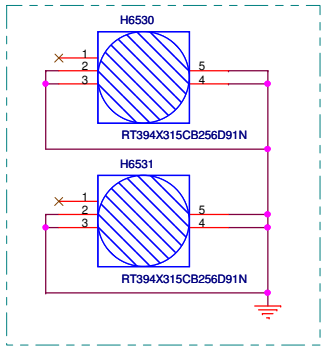


Total count: 11 pcs

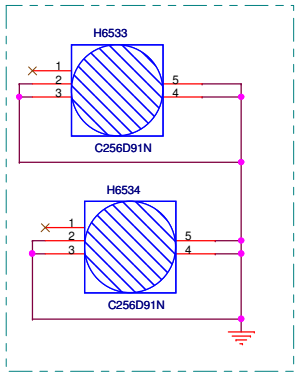
ASUSTeK COMPUTER INC. NB4	Title : DC_DC & BAT Conn.	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 62 of 99	

Main Board

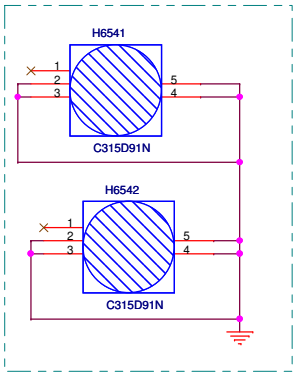
Screw Hole A



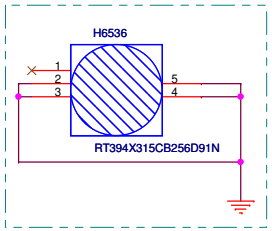
Screw Hole B



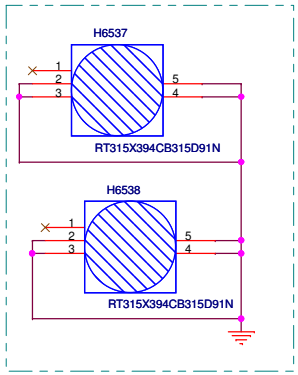
Screw Hole I



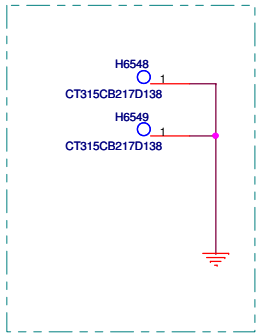
Screw Hole C



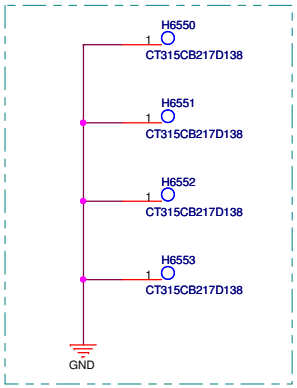
Screw Hole F



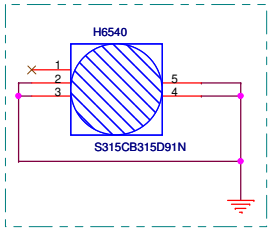
Screw Hole E



Screw from k52JR

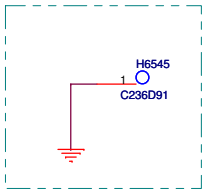


Screw Hole H



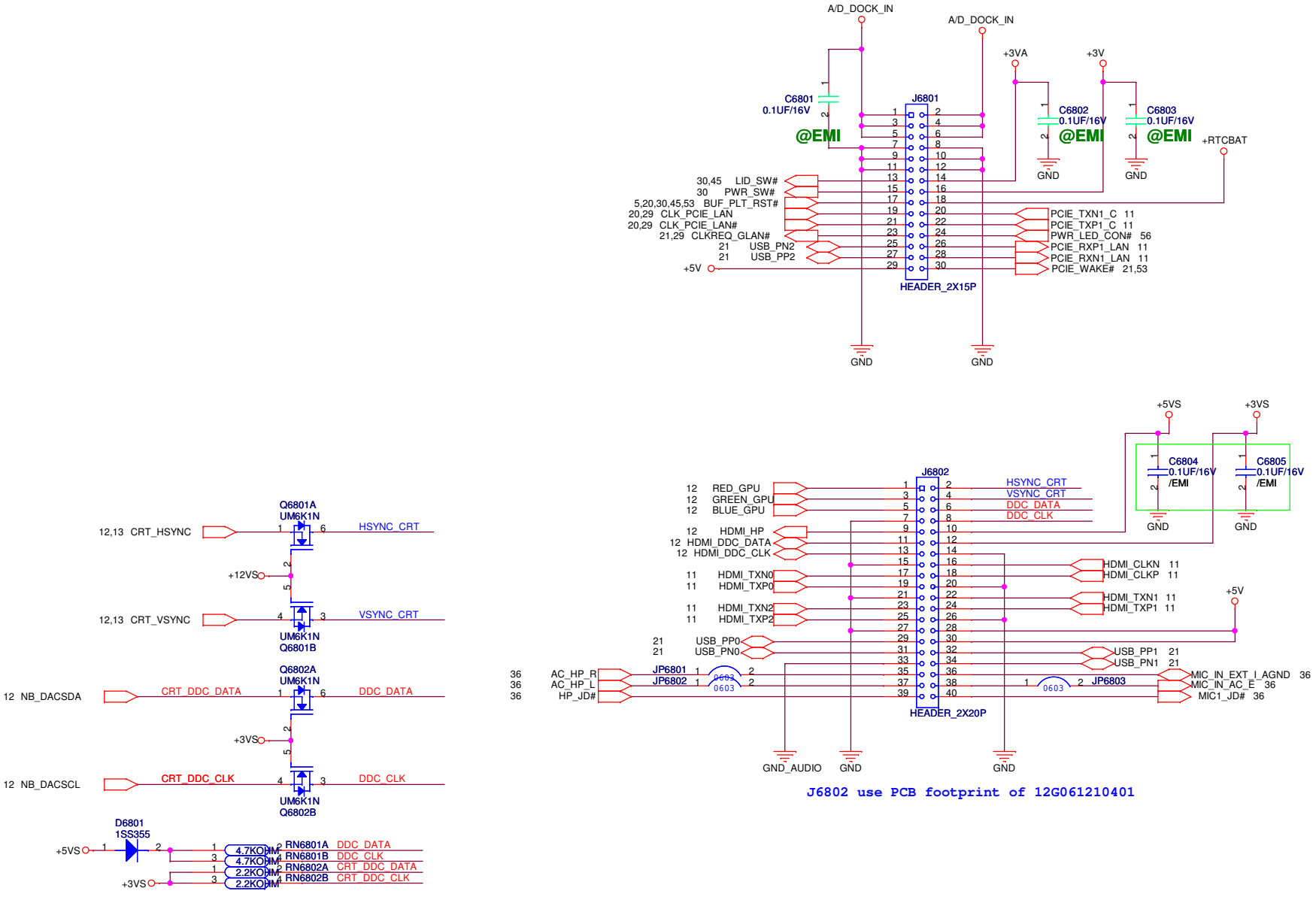
Tooling Hole K

Screw Hole O



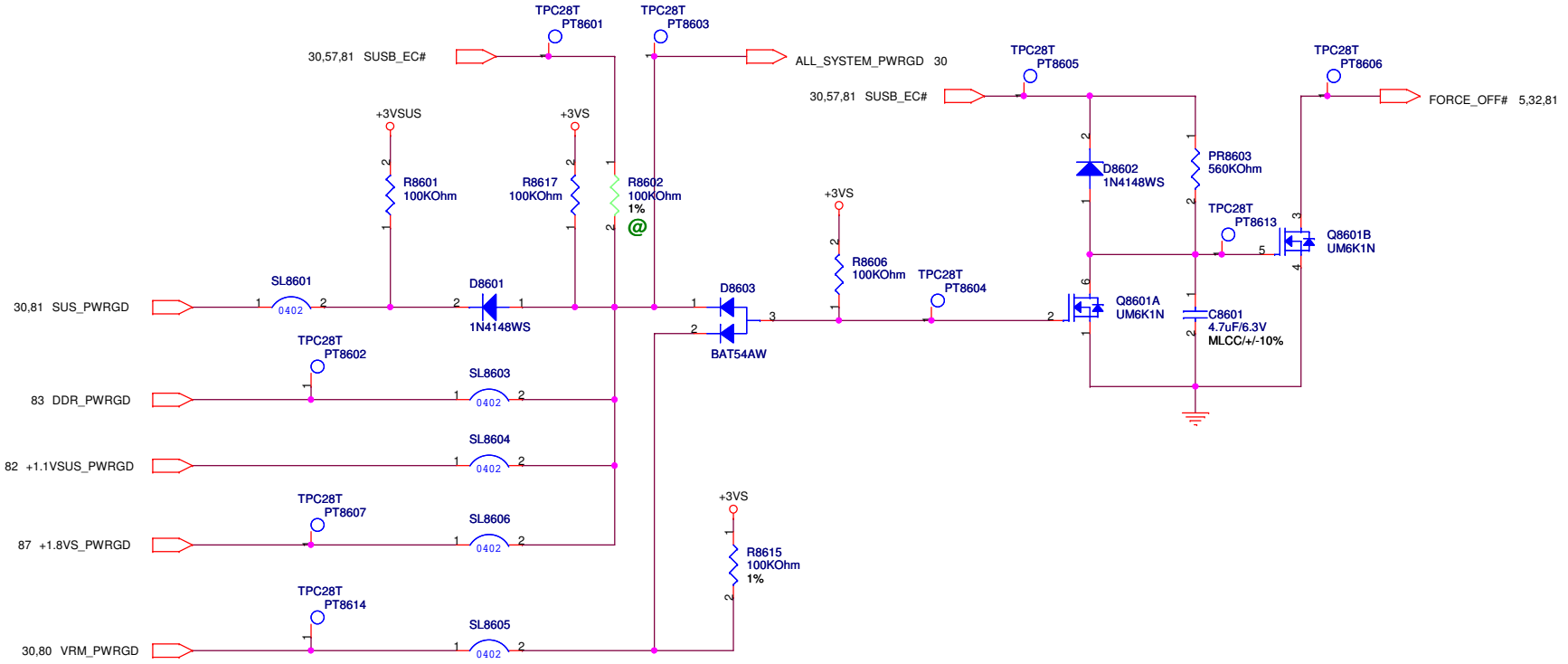
Tooling Hole L

ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: Vincent_Chiang	
Size: Custom	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 65 of 99	



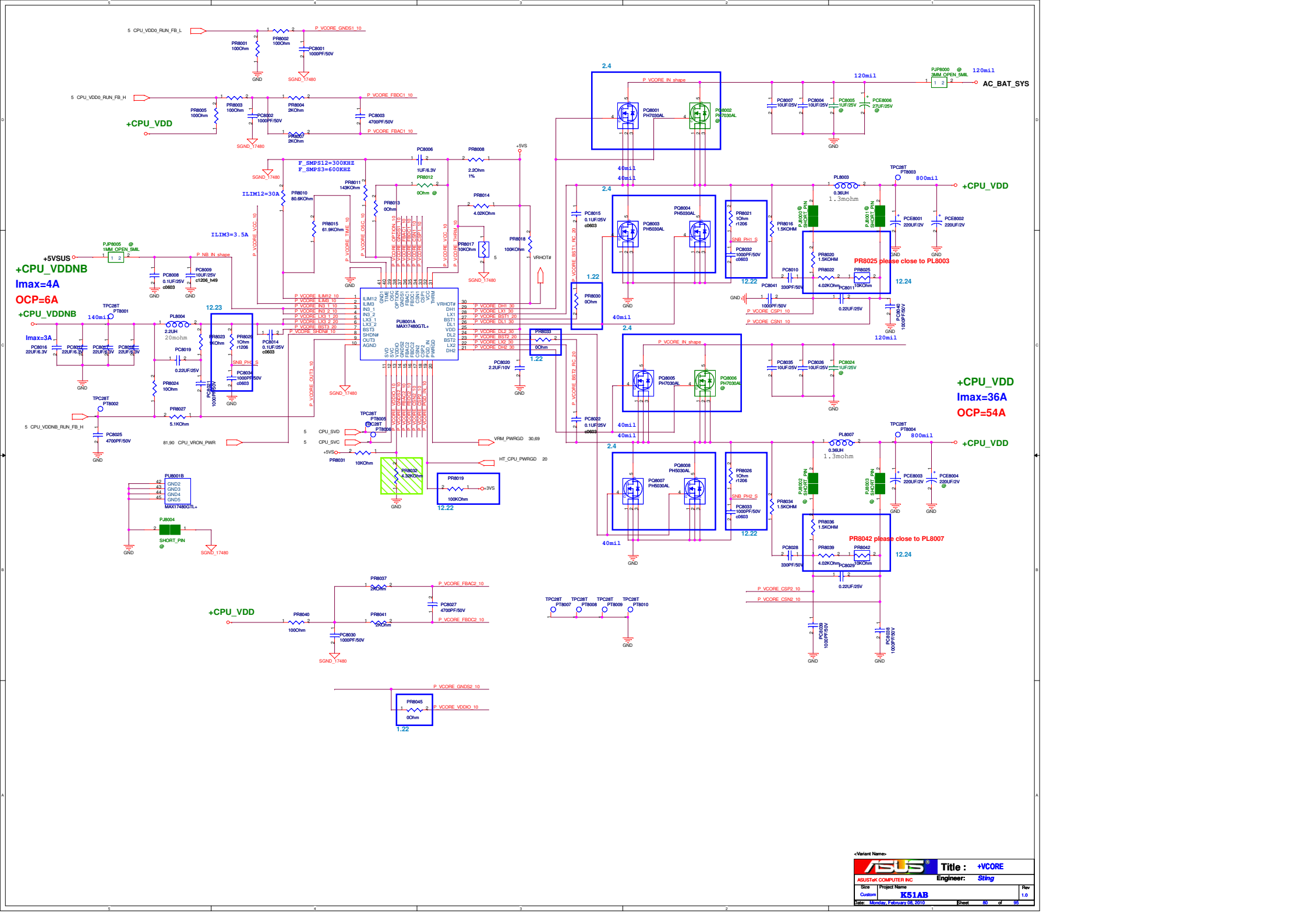
ASUSTeK COMPUTER INC. NB4	Title : IO Connector	
	Engineer: Vincent_Chiang	
Size: B	Project Name: K52N	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 68 of 99	

POWER GOOD DETECTER

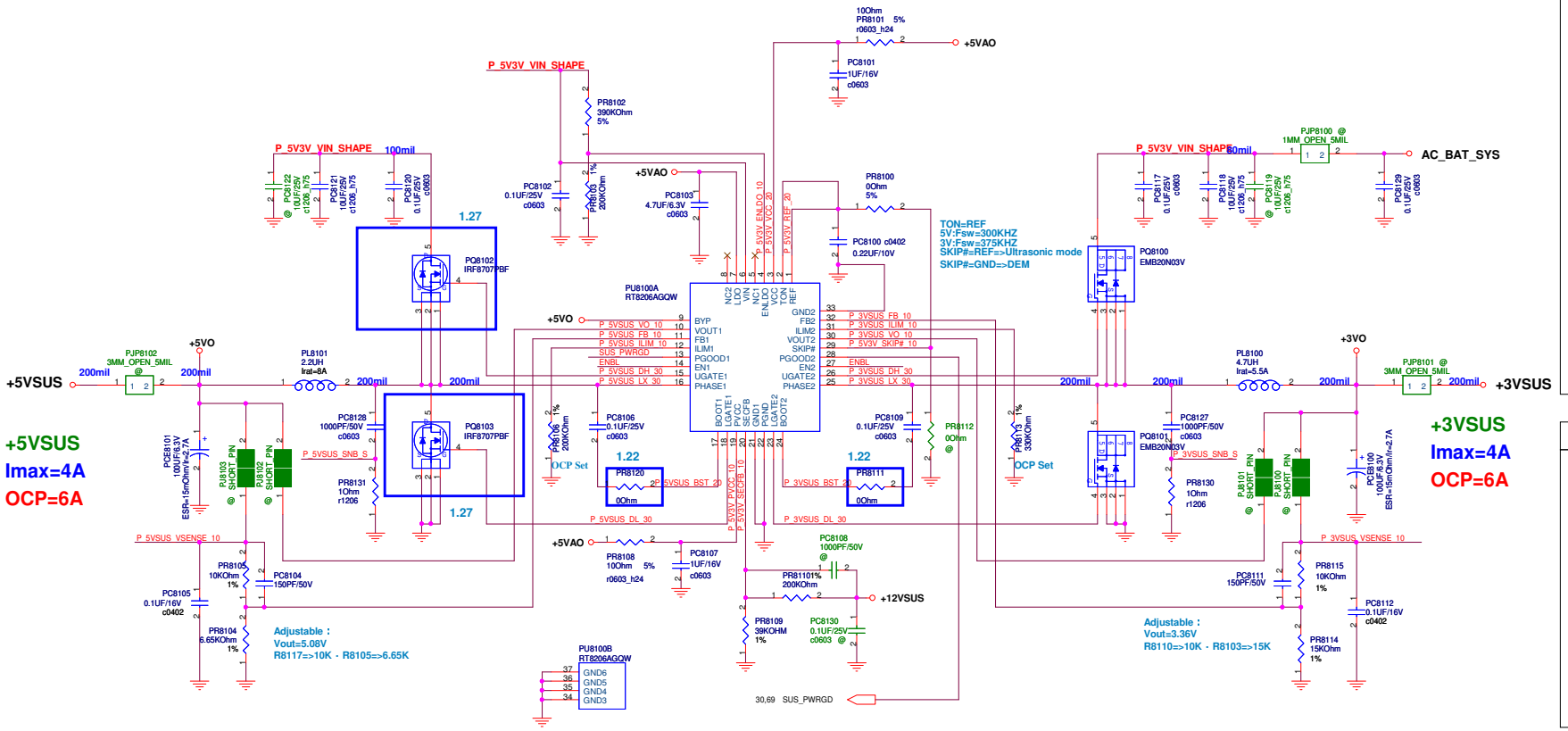


<Variant Name>

ASUSTeK COMPUTER INC	Title : GOOD_DETECTER	
	Engineer: Vincent_Chiang	
Size: B	Project Name	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 69 of 95	


+CPU_VDDNB
Imax=4A
OCP=6A
+CPU_VDD
Imax=36A
OCP=54A
AC_BAT_SYS
+5VSUS
+CPU_VDD
F_SMPS12=300KHZ
F_SMPS3=600KHZ
ILIM12=30A
ILIM3=3.5A
PR8025 please close to PL8003
PR8042 please close to PL8007
MAX17480GTL+
PU8001A
PU8001B
PJ8004
SHORT_PIN
VRM_PWRGD 30,69
HT_CPU_PWRGD 20
81,90 CPU_VRON_PWR
5 CPU_SVD
5 CPU_SVC
5 CPU_VDD0_RUN_FB_L
5 CPU_VDD0_RUN_FB_H
5 CPU_VDDNB_RUN_FB_H
SGND_17480
GND
Title : +VCORE
ASUSTeK COMPUTER INC.
Engineer: Sting
Project Name
K51AB
Rev 1.0
Monday, February 08, 2010
Sheet 80 of 85

+5VSUS / +3VSUS POWER SUPPLY



Power stage

+5VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.96A
2. Ripple Current:
   Irip=2.61A
3. Ripple Voltage:
   ESR/1=15mohm
   V=39.15mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm
5. MOSFET Spec:
   H-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)
   L-side MOSFET: FDMC8884
   Rds(ON)=30mohm (Vgs=4.5 V)
   I cont = 9A (T =25 ℃)
   I peak =15A (Pause =10 us)

+3VSUS:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.96A
2. Ripple Current:
   Irip=1.55A
3. Ripple Voltage:
   ESR/1=15mohm
   V=23.25mV
4. Inductor Spec:
   Isat=6.2A
   Idc=4.6A
   DCR=36mohm

Controller

+5VSUS:

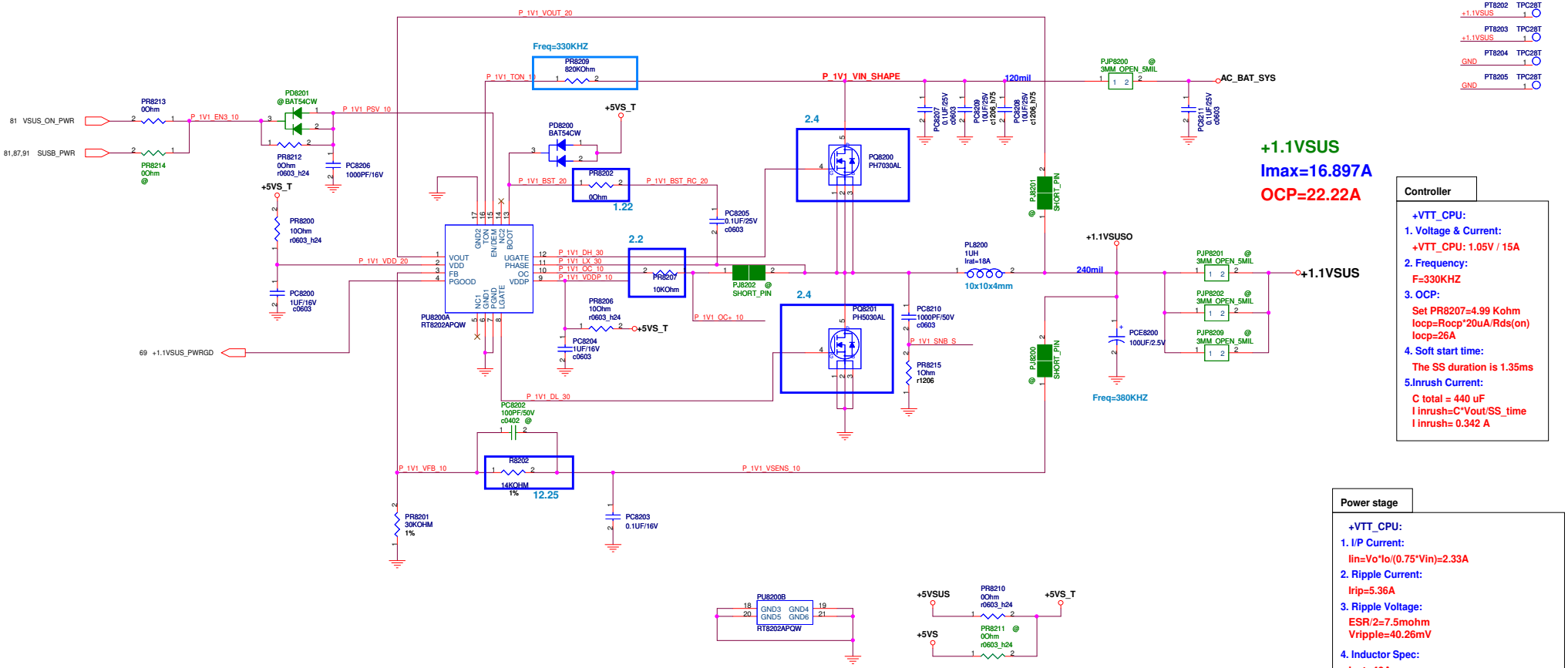
1. Voltage & Current:
   +5VSUS: 5V / 4A
2. Frequency:
   F=300KHZ
3. OCP:
   Set PR8106=357 Kohm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Soft start time:
   The Soft Start duration is 2ms
5. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.25 A

+3.VSUS

1. Voltage&Current:
   +3VSUS: 3.3V / 4A
2. Frequency:
   F=375KHZ
3. OCP:
   Set PR8113=357KOhm
   Iocp=5uA*Rocp/10*Rds(on)
   Iocp=6A
4. Inrush Current:
   C total = 100 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.165 A

<Variant Name>
ASUSTeK COMPUTER INC. NB
Title : POWER_SYSTEM
Engineer: Matt_Wang
Size: Custom
Project Name: Design_IP
Rev: 1.0
Date: Monday, February 08, 2010
Sheet 81 of 95

+1.1VSUS POWER SUPPLY



Controller

+VTT_CPU:

1. Voltage & Current:
   +VTT_CPU: 1.05V / 15A
2. Frequency:
   F=330KHZ
3. OCP:
   Set PR8207=4.99 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=26A
4. Soft start time:
   The SS duration is 1.35ms
5. Inrush Current:
   C total = 440 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.342 A

Power stage

+VTT_CPU:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.33A
2. Ripple Current:
   Irip=5.36A
3. Ripple Voltage:
   ESR/2=7.5mohm
   Vripple=40.26mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.6mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0353DPA

   Rds(ON)=7.6mohm (Vgs=4.5 V)
   I cont = 35A (T =25 ℃)
   I peak =140 A (Pause =10 us)

<Variant Name>

Title : POWER_I/O_+VCCP

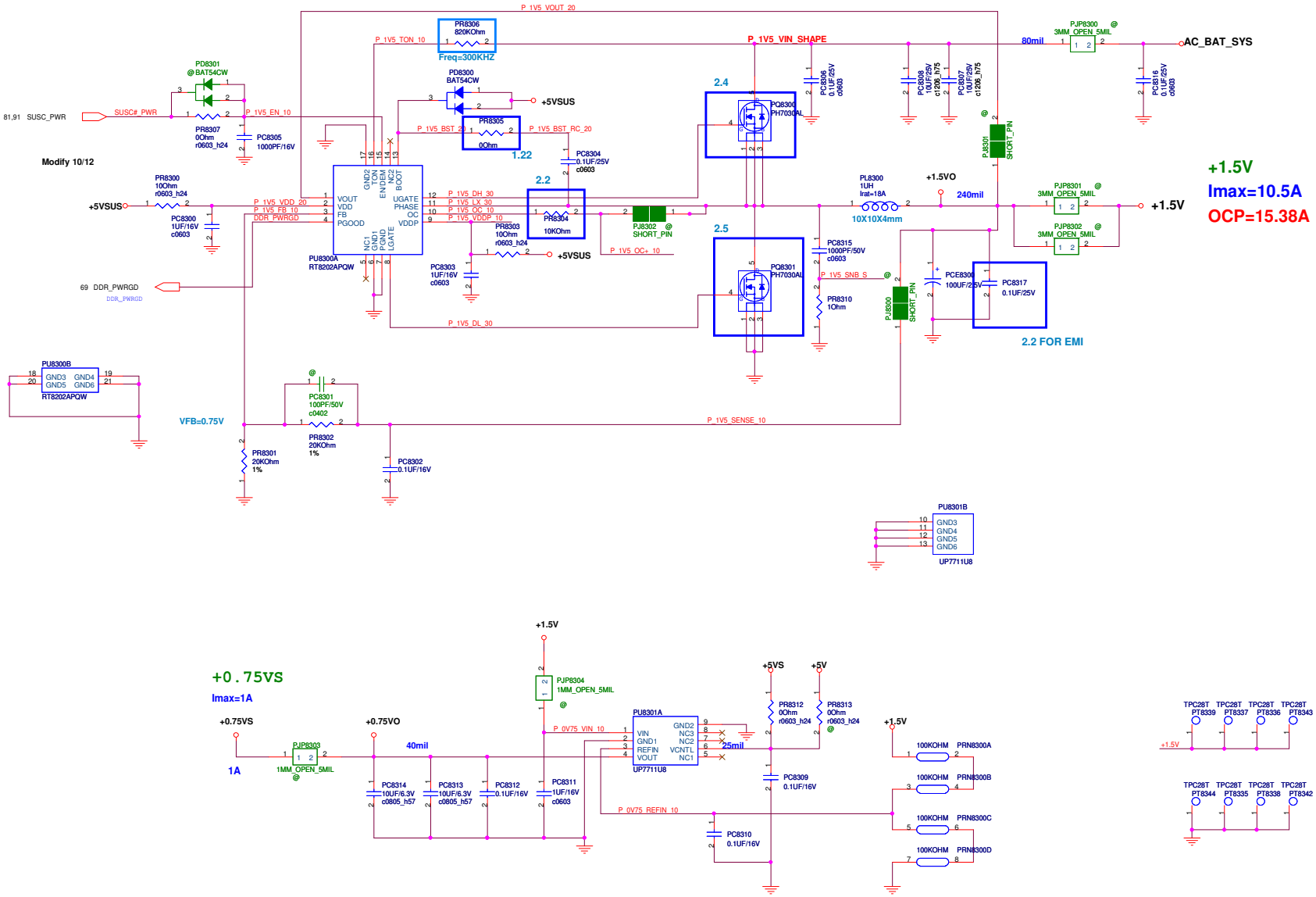
ASUSTeK COMPUTER INC. NB

Engineer: Matt_Wang

Size	Project Name	Rev
Custom	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 82 of 95

+1.5V & +0.75VS POWER SUPPLY



Power stage

DDR III:

1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=2.22A
2. Ripple Current:
   Irip=4.62A
3. Ripple Voltage:
   ESR/1=15mohm
   V=69.3mV
4. Inductor Spec:
   Isat=12.7A
   Idc=9.5A
   DCR=8.5mohm
5. MOSFET Spec:
   H-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

   L-side MOSFET: RJK0355DPA

   Rds(ON)=16.5mohm (Vgs=4.5 V)
   I cont = 30A (T =25 ℃)
   I peak =120 A (Pause =10 us)

Controller

DDR III:

1. Voltage & Current:
   +1.5V: 1.5V / 10A
2. Frequency:
   F=300KHZ
3. OCP:
   Set R8302=12 Kohm
   Iocp=Rocp*20uA/Rds(on)
   Iocp=14.3A
4. Soft start time:
   The Soft Start duration is 1.35ms
5. Inrush Current:
   C total = 220 uF
   I inrush=C*Vout/SS_time
   I inrush= 0.244 A

1. Voltage & Current:
   +0.75V: 0.75V / 1A

<Variant Name>

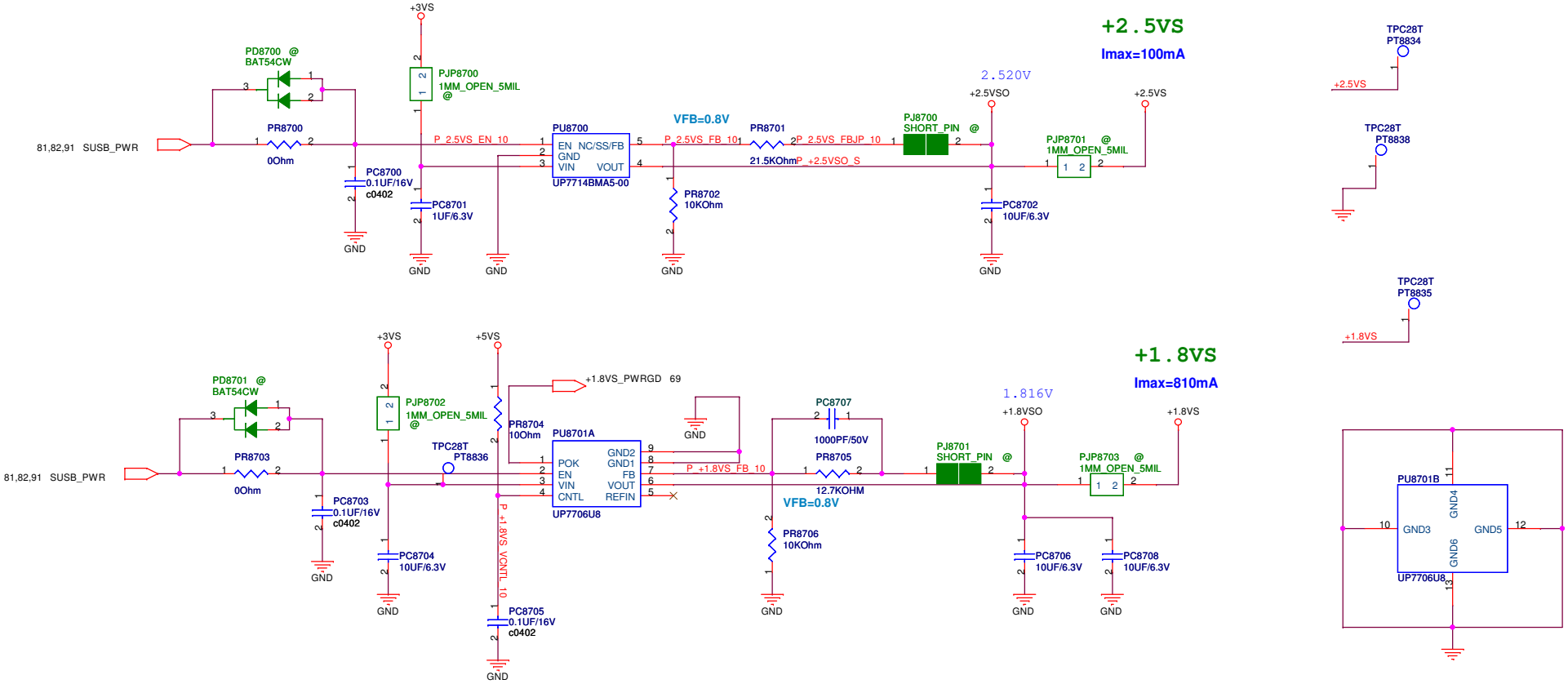
ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR

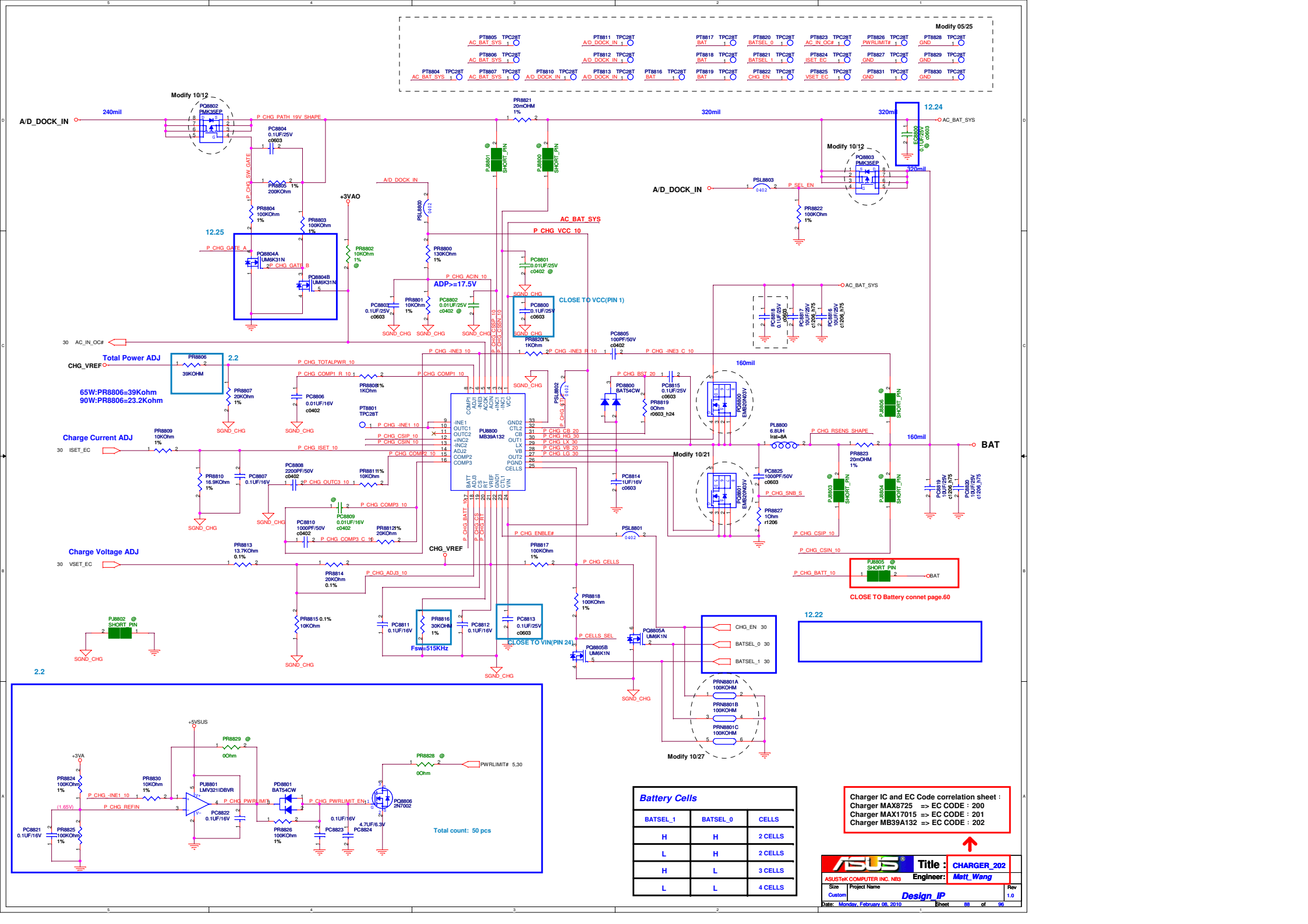
Engineer: Matt_Wang

Size	Project Name	Rev
Custom	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 83 of 95



ASUSTek Computer INC.	Title :	
	Engineer:	
Size: A3	Project Name: Oemga	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 87 of 95	


Modify 05/25
PT8805 TPC28T AC_BAT_SYS
PT8806 TPC28T AC_BAT_SYS
PT8804 TPC28T AC_BAT_SYS
PT8807 TPC28T AC_BAT_SYS
PT8811 TPC28T A/D_DOCK_IN
PT8812 TPC28T A/D_DOCK_IN
PT8810 TPC28T A/D_DOCK_IN
PT8813 TPC28T A/D_DOCK_IN
PT8816 TPC28T BAT
PT8817 TPC28T BAT
PT8818 TPC28T BAT
PT8819 TPC28T BAT
PT8820 TPC28T BATSEL_0
PT8821 TPC28T BATSEL_1
PT8822 TPC28T CHG_EN
PT8823 TPC28T AC_IN_OC#
PT8824 TPC28T ISET_EC
PT8825 TPC28T VSET_EC
PT8826 TPC28T PWRLIMIT#
PT8827 TPC28T GND
PT8831 TPC28T GND
PT8828 TPC28T GND
PT8829 TPC28T GND
PT8830 TPC28T GND
A/D_DOCK_IN
240mil
Modify 10/12
PQ8802 PMK35EP
P_CHG_PATH_19V_SHAPE
PC8804 0.1UF/25V c0603
P_CHG_SW_GATE
PR8805 200KOhm
PR8804 100KOhm 1%
PR8803 100KOhm 1%
+3VAO
12.25
P_CHG_GATE_A
PQ8804A UM6K31N
P_CHG_GATE_B
PQ8804B UM6K31N
PR8802 10KOhm 1%
PR8821 20mOHM 1%
PJ8801 @ SHORT_PIN
PJ8800 @ SHORT_PIN
AC_BAT_SYS
320mil
12.24
PC8809 0.01UF/25V c0603
Modify 10/12
PQ8803 PMK35EP
PSL8803 0402
P_SEL_EN
PR8822 100KOhm 1%
PSL8800 0402
PR8800 130KOhm 1%
P_CHG_ACIN_10
ADP>=17.5V
P_CHG_VCC_10
PC8801 0.01UF/25V c0402 @
SGND_CHG
CLOSE TO VCC(PIN 1)
PC8800 0.1UF/25V c0603
PC8803 0.1UF/25V c0603
PR8801 10KOhm 1%
PC8802 0.01UF/25V c0402 @
P_CHG_CSSP_10
P_CHG_CSSN_10
PC8818 0.1UF/25V c0603
PC8817 10UF/25V c1206_h75
PC8816 10UF/25V c1206_h75
30 AC_IN_OC#
Total Power ADJ
CHG_VREF
PR8806 39KOHM 2.2
65W:PR8806=39Kohm
90W:PR8806=23.2Kohm
PR8807 20KOhm 1%
P_CHG_TOTALPWR_10
P_CHG_COMP1_R_10
PR8808 1KOhm 1%
P_CHG_COMP1_10
PC8806 0.01UF/16V c0402
P_CHG_-INE3_10
PR8820 1KOhm 1%
P_CHG_-INE3_R_10
PC8805 100PF/50V c0402
P_CHG_-INE3_C_10
160mil
PD8800 BAT54CW
PC8815 0.1UF/25V c0603
PR8819 0Ohm c0603_h24
PQ8800 EMB20N03V
PJ8806 @ SHORT_PIN
Charge Current ADJ
30 ISET_EC
PR8809 10KOhm 1%
P_CHG_ISET_10
PR8810 16.9KOhm 1%
PC8807 0.1UF/16V
PC8808 2200PF/50V c0402
P_CHG_OUTC3_10
PR8811 10KOhm 1%
P_CHG_-INE1_10
P_CHG_CSIP_10
P_CHG_CSIN_10
P_CHG_COMP2_10
PU8800 MB39A132
P_CHG_CB_20
P_CHG_HG_30
P_CHG_LX_30
P_CHG_VB_20
P_CHG_LG_30
PSL8802 0402
P_CHG_BST_20
PC8814 1UF/16V c0603
Modify 10/21
PL8800 6.8UH Irat=8A
P_CHG_RSENS_SHAPE
160mil
BAT
PR8823 20mOHM 1%
PC8825 1000PF/50V c0603
P_CHG_SNB_S
PR8827 1Ohm r1206
PQ8801 EMB20N03V
PJ8803 @ SHORT_PIN
PJ8804 @ SHORT_PIN
PC8819 10UF/25V c1206_h75
PC8820 10UF/25V c1206_h75
PC8809 0.01UF/16V c0402
PC8810 1000PF/50V c0402
P_CHG_COMP3_10
P_CHG_COMP3_C_10
PR8812 1% 20KOhm
P_CHG_BATT_10
P_CHG_CS
P_CHG_RT
P_CHG_ENBLE#
PSL8801 0402
Charge Voltage ADJ
30 VSET_EC
PR8813 13.7KOhm 0.1%
CHG_VREF
PR8817 100KOhm 1%
P_CHG_CELLS
PR8814 20KOhm 0.1%
P_CHG_ADJ3_10
PR8815 0.1% 10KOhm
PC8811 0.1UF/16V
PR8816 30KOHM 1%
Fsw=515KHz
PC8812 0.1UF/16V
PC8813 0.1UF/25V c0603
CLOSE TO VIN(PIN 24)
PJ8805 @ SHORT_PIN
CLOSE TO Battery connet page.60
PJ8802 @ SHORT_PIN
PR8818 100KOhm 1%
P_CELLS_SEL
PQ8805A UM6K1N
PQ8805B UM6K1N
CHG_EN 30
BATSEL_0 30
BATSEL_1 30
12.22
PRN8801A 100KOHM
PRN8801B 100KOHM
PRN8801C 100KOHM
Modify 10/27
2.2
+5VSUS
PR8829 @ 0Ohm
+3VA
PR8824 100KOhm 1%
PR8830 10KOhm 1%
PU8801 LMV321IDBVR
P_CHG_-INE1_10
(1.65V)
P_CHG_REFIN
P_CHG_PWRLIMIT
PD8801 BAT54CW
P_CHG_PWRLIMIT_EN
PQ8806 2N7002
PR8828 @ 0Ohm
PWRLIMIT# 5,30
PC8821 0.1UF/16V
PR8825 100KOhm 1%
PC8822 0.1UF/16V
PR8826 100KOhm 1%
PC8823 0.1UF/16V
PC8824 4.7UF/6.3V
Total count: 50 pcs
Battery Cells
BATSEL_1 | BATSEL_0 | CELLS
H | H | 2 CELLS
L | H | 2 CELLS
H | L | 3 CELLS
L | L | 4 CELLS
Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202
ASUSTeK COMPUTER INC. NB3
Title : CHARGER_202
Engineer: Matt_Wang
Size: Custom
Project Name: Design_IP
Rev: 1.0
Date: Monday, February 08, 2010
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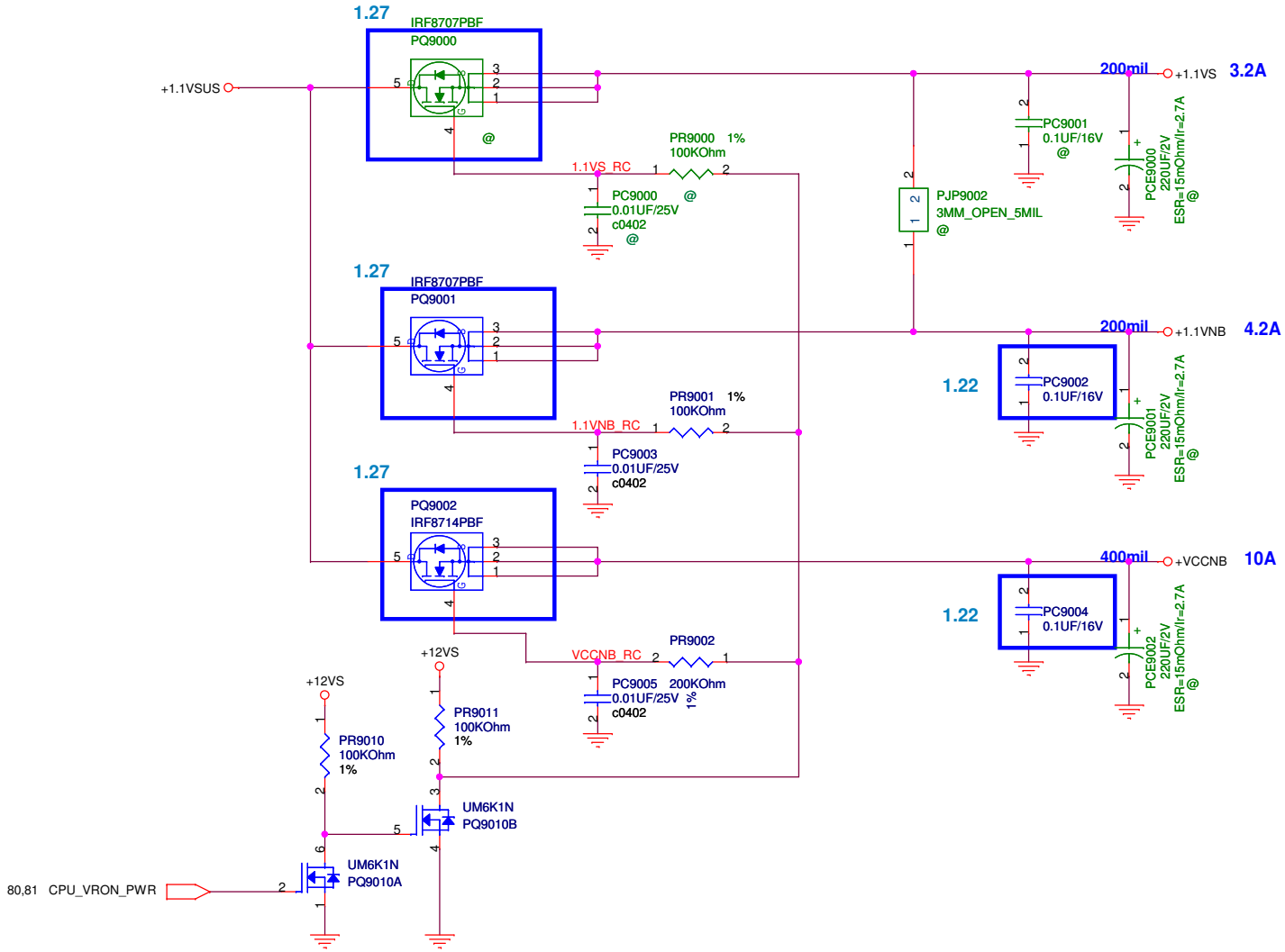
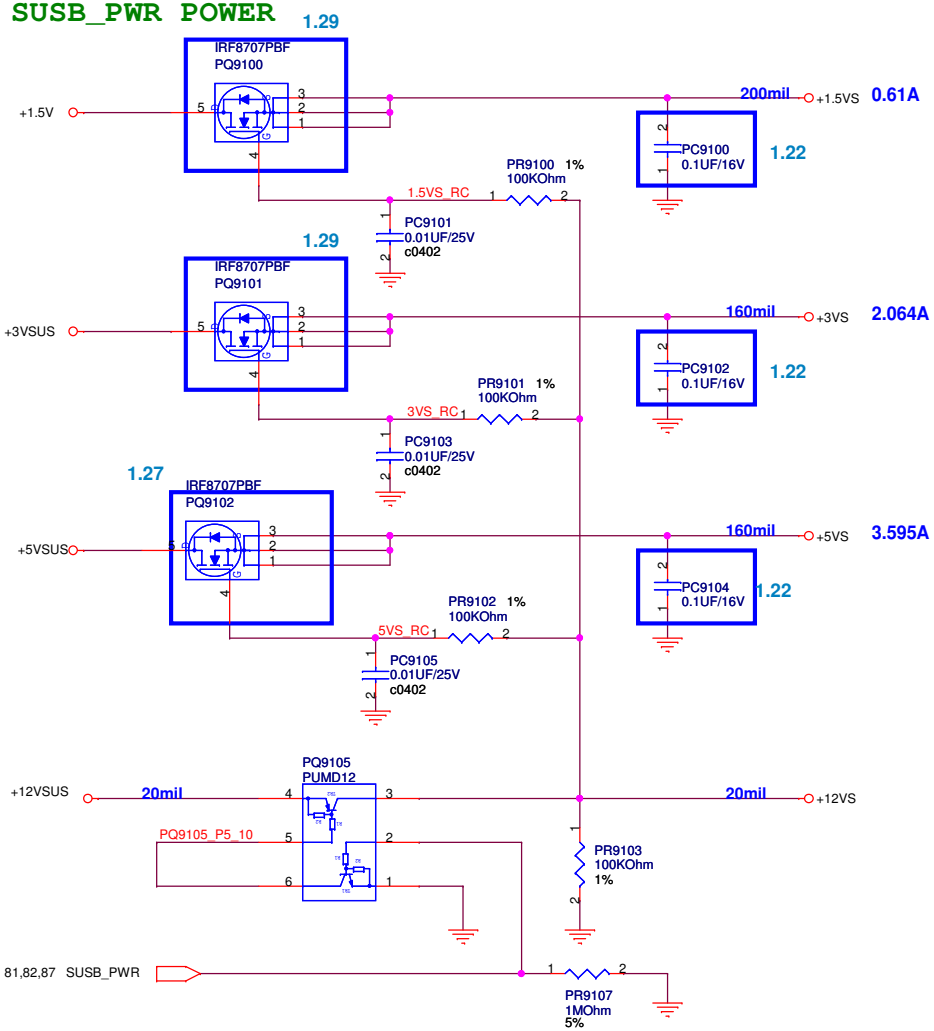
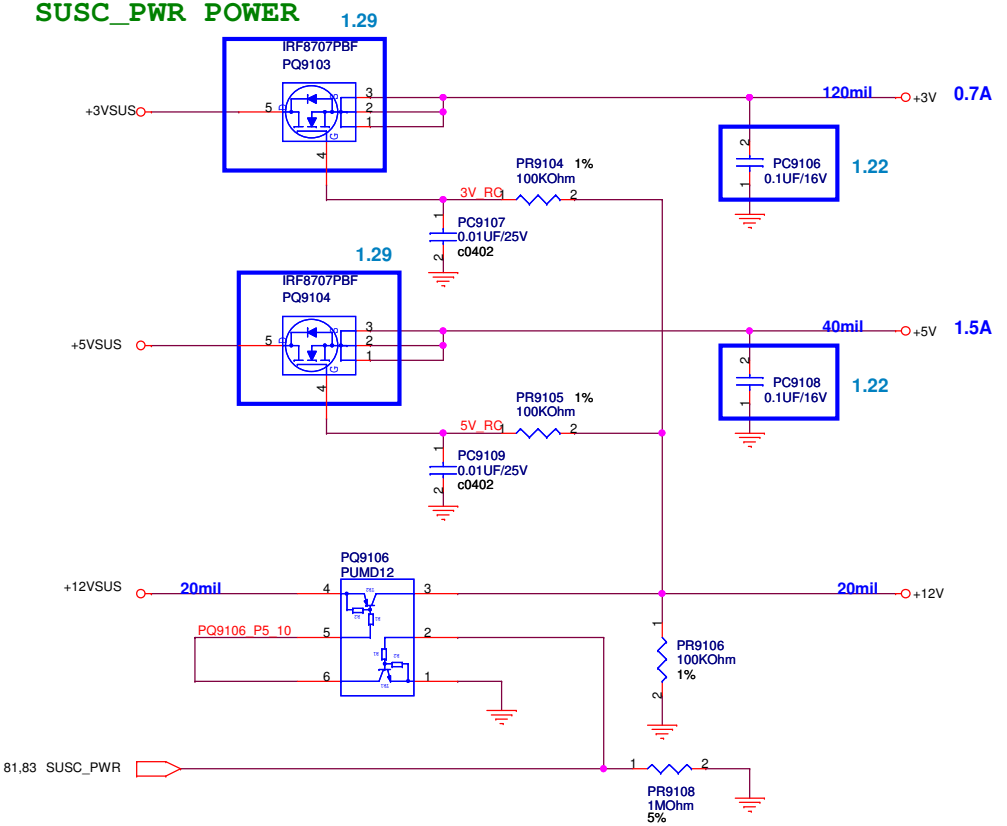


<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Matt_Wang	
Size: Custom	Project Name: Design_IP	Rev: 1.0
Date: Monday, February 08, 2010	Sheet 90 of 95	





<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_LOAD SWITCH

Engineer: Matt_Wang

Size	Project Name	Rev
B	Design_IP	1.0

Date: Monday, February 08, 2010 Sheet 91 of 95