

P4M890T-M

Rev : 1.0

1	Cover Page
2	Block Diagram
3	CPU P4-775(FSB)
4	CPU P4-775(PWR, GND)
5	Clock Generator, Clock Buffer
6	Power (CPU Vcore)
7	Power (DC to DC)
8	VDIMM & DDR VTT
9	NB P4M890 (CPU)
10	NB P4M890 (MEM)
11	NB P4M890 (PCI-E, V-Link)
12	NB P4M890 (VGA)
13	DDR II SLOT1
14	DDR II SLOT2
15	DDR Terminator
16	PCI Express Slot X16, X1, CNR slot
17	SB VT8237R+/8237A/8237S(PCI, USB)
18	SB VT8237R+/8237A/8237S(IDE, GPIO, AC-Link, SATA)
19	SB VT8237R+/8237A/8237S(V-Link, MII, ROM)
20	LAN PHY(VT6103L)
21	Super IO(ITE8712F/KX,8718), FDD
22	PCI 1, PCI 2
23	USB, PS2, IDE
24	COM*2, LPT, VGA
25	Front Panel, FAN, ATX24P
26	AUDIO(ALC655/ALC883),Chip
27	AUDIO(ALC655/ALC883),Connector
28	CLOCK DIAGRAM
29	POWER SEQUENCE

8237R+,ALC655

8237A,ALC883

8237R+,ALC655

8237A,ALC883

8237R+,ALC655

Schematics	PCB Lead-Free 244*210*1.6 -2116	BOM	SVID:1019(ECS) SSID:2171(Q71) Schedule			
			Schematics	Layout	Gerber Out	M/B return
A	15-Q71-010010 Green	RoHS 81-605-Q71000	11/16~11/28	11/28~12/30 chipset delay	12/30	35/20/20
A		RoHS 81-605-Q71001				10/10
B	15-Q71-010020 Purple	RoHS 81-605-Q71010	2/10	2/13	2/24	30/10
B	Purple	RoHS 81-605-Q71011				20/10
1.0	15-Q71-011000 Purple	RoHS 89-206-Q71100	4/10		6/19	100/50/10
1.0						

GPIO

IC	GPIO(PIN)	Function	Note
VT 8237R+	GPIO23(P21)	-IDE2 cable detect	
	GPIO8(AC9)	-IDE1 cable detect	
	GPIO18(Y4)	-PCIE PME SCI	
	GPIO19(U23)	-PCIE Hot Plug SCI	
	GPIO7(R2)	-TBL(Top Block Lock)	default=0
	GPIO10(R25)	V_DIMM volt adjust 0	
	GPIO11(T23)	V_DIMM volt adjust 1	
	GPIO5(AC7)	-WP_ROM	default=1
	GPIO29	PCIE reset	
	IO 8712KX	GP25(22)	CPU volt adjust 0
GP26(21)		CPU volt adjust 1	
GP40(79)		CTRL PS2 volt in S5	default=1
GP23(24)		CTRL over clock	1:enable
GP10(84)		MSG LED1	
GP53(77)		MSG LED2	
GP20(27)		CFG1	default=0
GP21(26)		CFG2	default=0

Rev:A Initial version

1. Base on P4M800PRO-M(1.0A) to modify.

Rev:A->B

- Delete 1394, add CNR slot.
- DDR2 termination resistor:68 ohm->47 ohm.
- Add BA0,BA1,BA2 termination resistor.
- Change V_DIMM MOSFET from S08 to TO-251.
- NB:add 22UF on VCCA33HCK,VCCA33MCK.
- Modify CPU thermal trip circuit.
- Jp1 pull high to VCC5 on ITE 8712F/KX.
- ALC883:modify circuit for Vista.
- Add GPIO29 control PCIE reset.
- INT_H pull down.
- Saving EEPROM of LAN.

Rev:B->1.0

- VR11
- Co-layout VT8237S
- AUDIO capcitor modify.
- VCC3 transfer to +1.5V_NB
- CPU voltage adjustment.
- add F_MIC2.
- Modify clock gen's enable
- Change SIO:-PCI_RST5 to -PCI_RST3.



Elitegroup Computer Systems

Title		Cover Page	
Size	Document Number	Rev	
Custom	P4M890T-M	1.0	
Date:	Tuesday, June 20, 2006	Sheet	1 of 29

05A
PWM
 Richtek 9245A
 +Richtek 9602
 VRM10.X 6

P4, Pentium-D
 LGA775 (SMD)
 1066MHz 3,4

Clock Gen.
ICS 953002DF
 5
 (Realtek RTM866-890)

VGA CON 24
 24

PCIE GFX x16 16
 16

PCIE x1 16
 16

VIA NB:P4M890
 AGTL+ P4 CPU I/F
 DDR 400/DDR2 533
 INTEGRATED GRAPHICS
 (UniChrome Pro)
 1 X16 PCIE VIDEO I/F
 1 X16 V-Link I/F WITH SB
 9,10,11,12

Clock Buffer
ICS 9P936AF
 5
 (Realtek RTM682-800)

Unbuffered
DDR II-DIMM
 13,14,15
DDR2-533 Single Channel
 (Non ECC)

(Pin to Pin P4M900)
 i)DDR2 667
 ii)Int. DeltaChrome/DX9 support

RJ45
 (左黃右綠) 20
 20

LAN PHY
VT6103L
(TQFP48) 20
 20

USB2.0*8 23
 23

KB& MS 23
 23

VT8237R +/ VT8237A
 (Pin to Pin)
 USB2.0 (4+4)
 SATA (2 PORTS)
 AC97(VT8237R+)
 HD(VT8237A)
 ATA 66/100/133
 ACPI 2.0
 PCI/PCI BDGE
 LPC I/F 17,18,19

ALC655/ ALC883 26,27
 26,27

CNR slot 16
 16

SATA*2 18
 18

IDE*2 23
 23

IN OUT
MIC
C/B
S/S

Revision List	
ITE8712	
ITE8716	add Dual sourcing
ITE8718	add PECI(CPU temp:digital)
ITE8726	add K8 power sequence

Revision List(All pin to pin)	
VT8237CD	First released
VT8237R	LAN PHY license.
VT8237R+	SATA II detect support
VT8237A	HD support
VT8237S	SATA II,HD support

PCI SLOT*2 22
 22

ITE LPC SIO 8712F/IX,KX 21
 21

FLASH BIOS 4M 19
 19

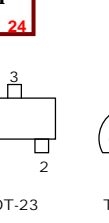
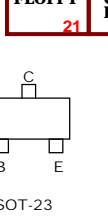
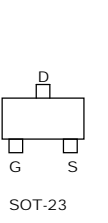
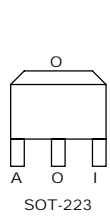
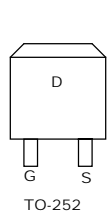
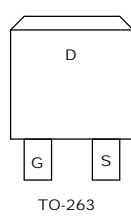
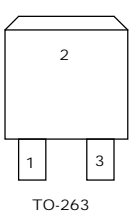
FLOPPY 21
COM LPT 24
 21 24

	Impedance	PCB 2116
USB_P0+/-	(45/90)	20/7.5/7.5/7.5/20 20/7.5/7.5/7.5/20(VIA excel) 7.5/7.5/7.5(50/90 guide)
LAN RX+/- TX+/-	(50/100)	24/6/9/6/24 24/6/9/6/24(VIA excel) 8/12/8(47/91 guide)
SATA	(50/100)	20/5/7/7/20 20/5/7/7/20(VIA excel) group mismatch 5 mil.
R.G.B	NB->RES (37.5) RES->CON (75)	20/12/20/12/20/12/20 20/5/20/5/20/5/20 Put 75 ohm on NB

PCI Bus Resource			
PCI1	AD19	INTA,BCD	REQ0
PCI2	AD20	INTB,CDA	REQ1

1U-04(最大耐壓6.3V) 1U-06(BOM常用料耐壓10V)
 0.1U-04(最大耐壓16V) 0.1U-06(BOM常用料耐壓25V)

22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
680U/?DE	8*8 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



Elitegroup Computer Systems

Title: **Block Diagram**

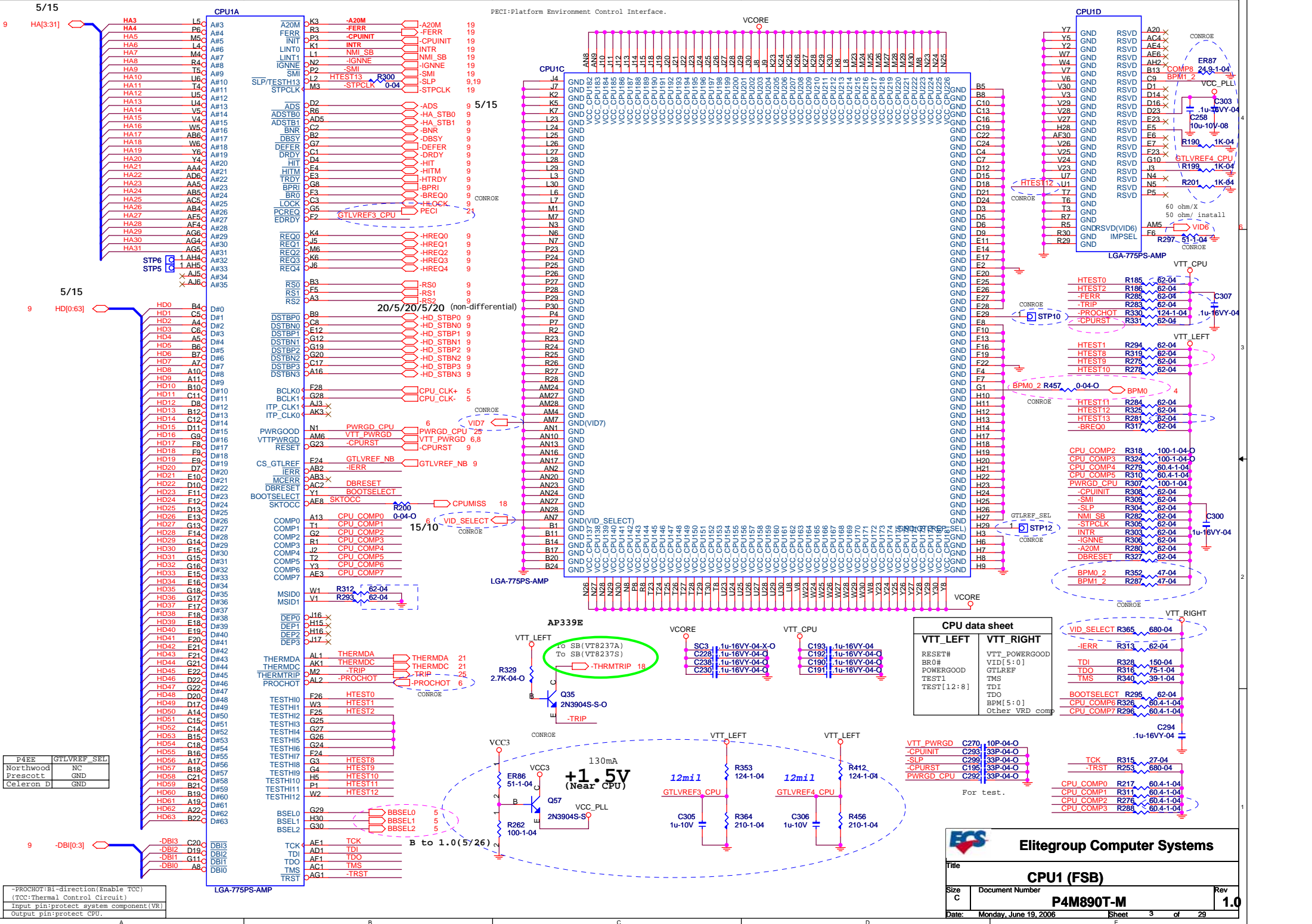
Size: Custom Document Number

Date: Tuesday, May 30, 2006

Sheet: 2 of 29

Rev: **1.0**

P4M890T-M



VTT_LEFT	VTT_RIGHT
RESET#	VTT_POWERGOOD
BRO#	VID[5:0]
POWERGOOD	GTLREF
TEST1	TMS
TEST[2:8]	TDI
	TDO
	VID[5:0]
	Other: VRD comp

Elitegroup Computer Systems

Title: **CPU1 (FSB)**

Document Number: **P4M890T-M**

Date: Monday, June 19, 2006

Sheet 3 of 29

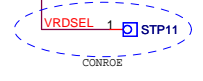
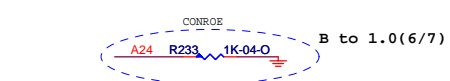
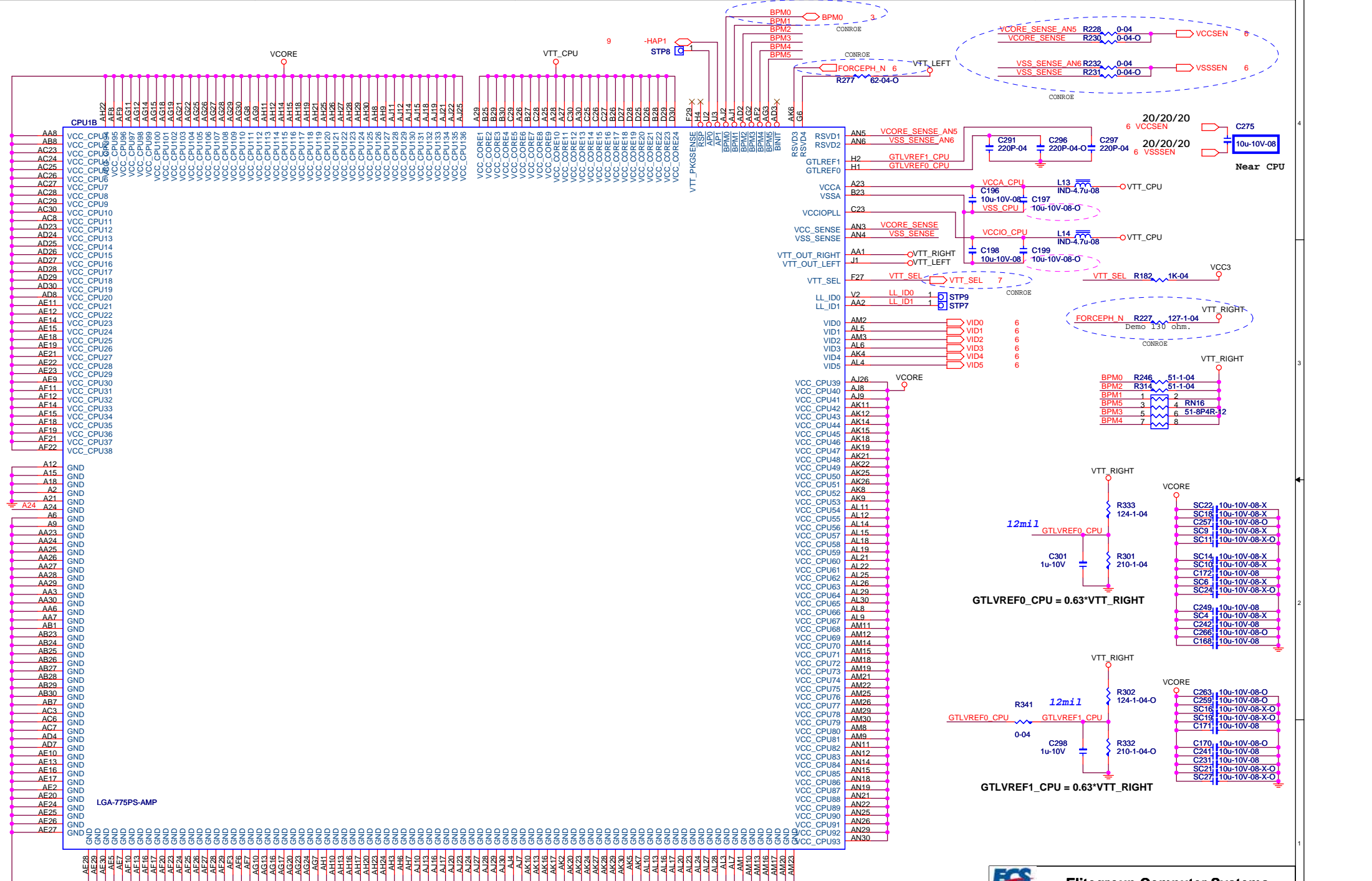
Rev: 1.0

P4EE	GTLVREF_SEL
Northwood	NC
Prescott	GND
Celeron D	GND

-PROCHOT: B1-direction (Enable FCC)
(FCC: Thermal Control Circuit)

Input pin: protect system component (VR)

Output pin: protect CPU.

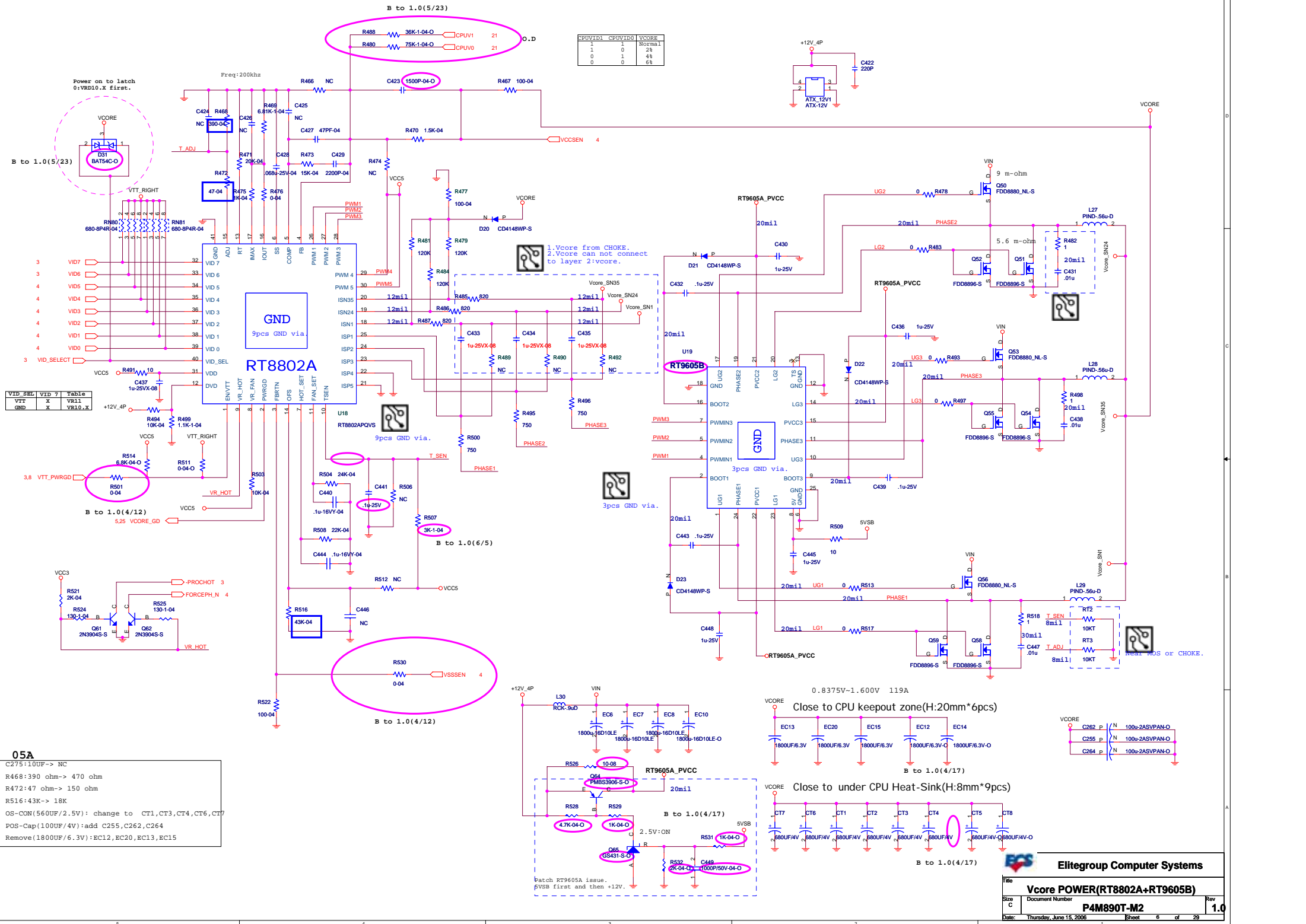


Elitegroup Computer Systems

Title: **CPU P4-775 (PWR, GND)**

Size C Document Number: **P4M890T-M** Rev: **1.0**

Date: Thursday, June 15, 2006 Sheet 4 of 29



CPUV1DI	CPUV1DO	VCORE
1	1	Normal
1	0	28
0	1	48
0	0	63

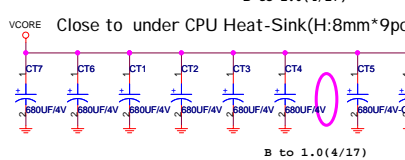
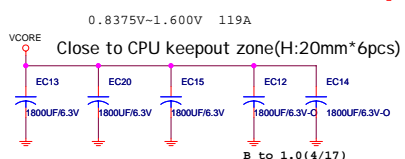
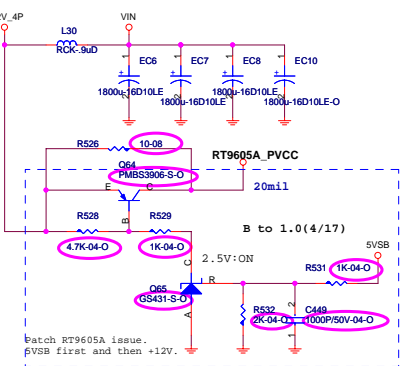
VID	SEL	VID	Table
VTT	X	VR11	
GND	X	VR10.X	

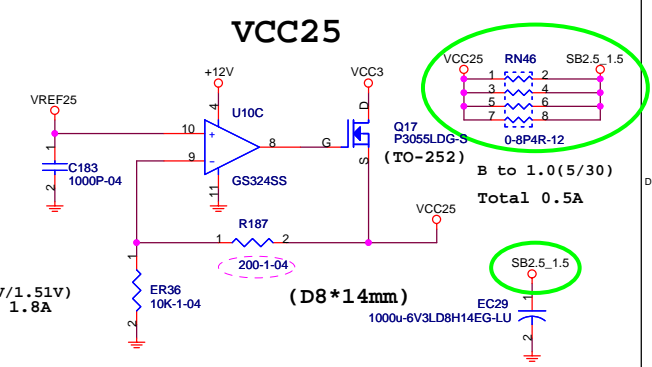
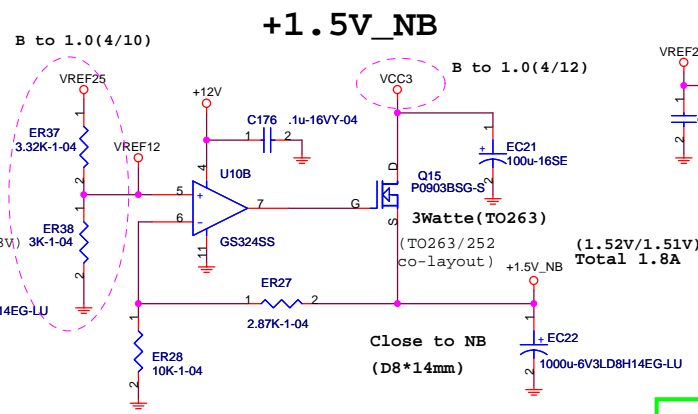
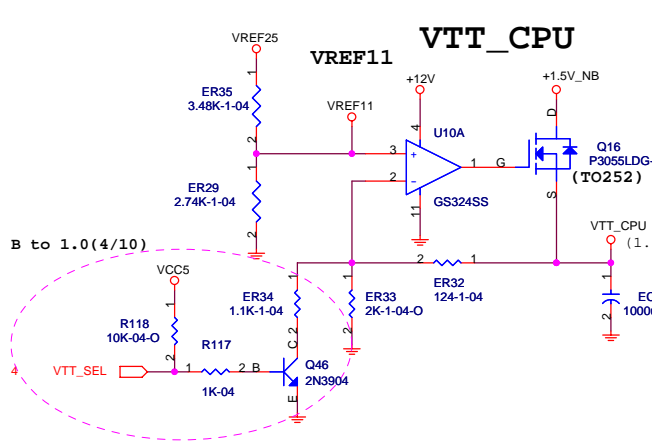
05A

C275:100UF-> NC
 R468:390 ohm-> 470 ohm
 R472:47 ohm-> 150 ohm
 R516:43K-> 18K
 OS-CON(560UF/2.5V): change to CT1,CT3,CT4,CT6,CT7
 POS-Cap(100UF/4V):add C255,C262,C264
 Remove(1800UF/6.3V): EC12, EC20, EC13, EC15

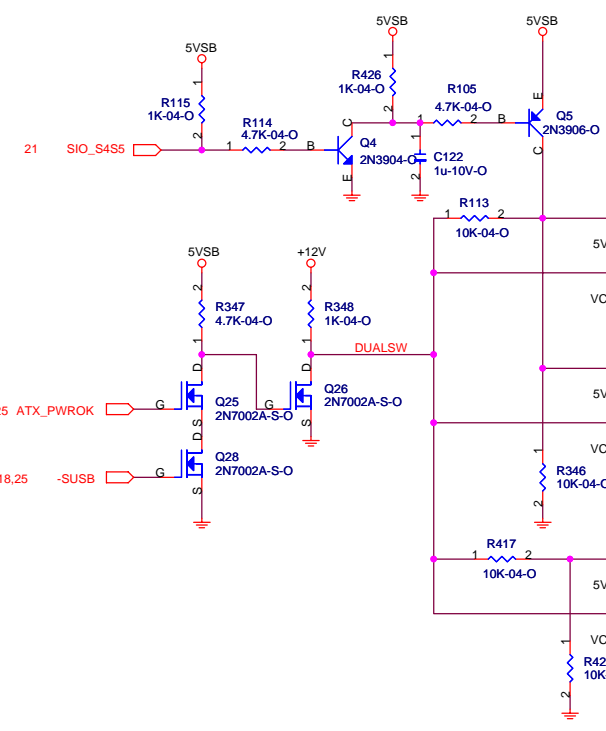
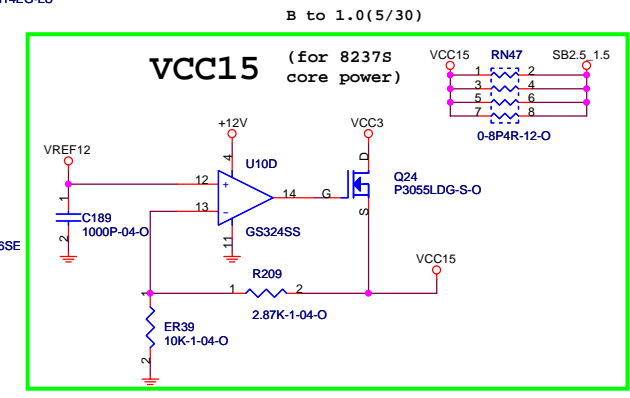
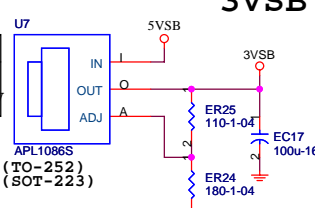
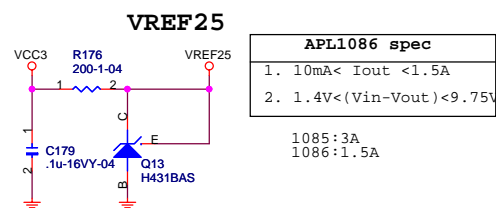
1.Vcore from CHOKE.
 2.Vcore can not connect to layer 2:vcore.

near POS or CHOKE.

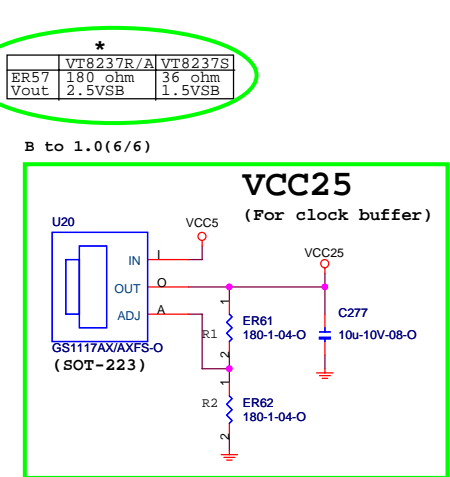
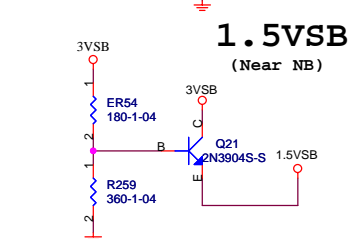
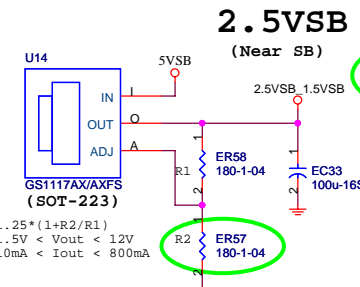
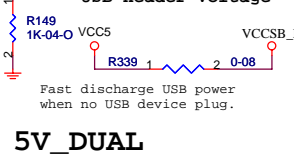
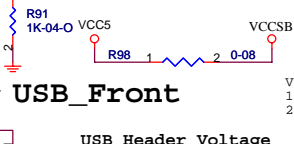
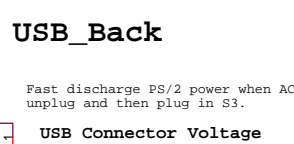




Status	Target	Super I/O F/GXS
AC plug	5V_DUAL=0	SIO_S4S5=0D=1
S0,S1	5V_DUAL=VCC	SIO_S4S5=1
S3	5V_DUAL=5VSB	SIO_S4S5=0
S4,S5	5V_DUAL=5VSB	SIO_S4S5=0
S4,S5	5V_DUAL=0	SIO_S4S5=1



Vds	Id
P-ch	30V 8.5A
N-ch	-30V -3A



Elitegroup Computer Systems

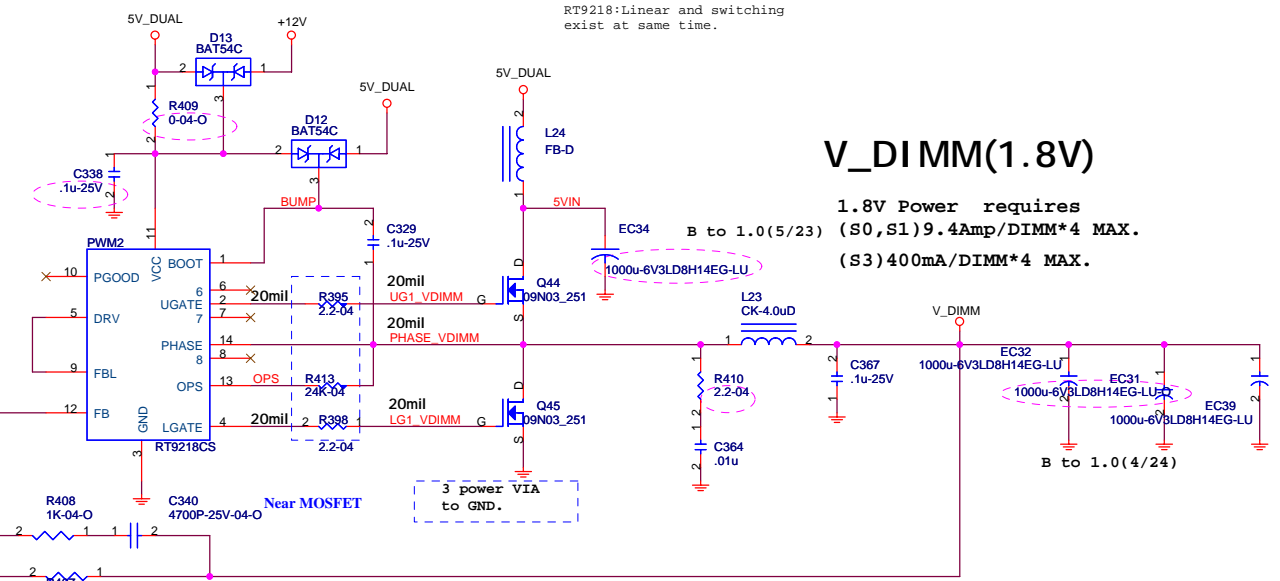
Title: **POWER (DC to DC)**

Size: Document Number **P4M890T-M** Rev: **1.0**

Date: Thursday, June 15, 2006 Sheet 7 of 29

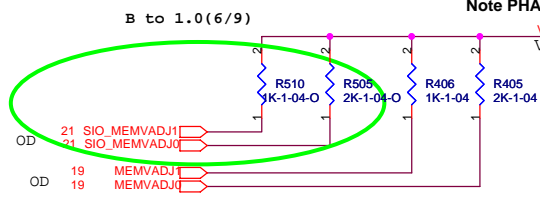
Dual N-CH
 APM7312 Vds=20V Vgs=16V
 *AO4812 Vds=30V Vgs=20V Id=6.9A
 RT9218: Linear and switching exist at same time.

MEMVADJ1	MEMVADJ0	V_DIMM
0	0	Normal (1.8V)
0	1	+50mV (1.85V)
1	0	+100mV (1.90V)
1	1	+150mV (1.95V)



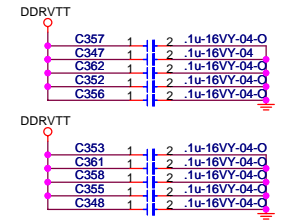
V_DIMM(1.8V)

1.8V Power requires
 B to 1.0(5/23) (S0, S1) 9.4Amp/DIMM*4 MAX.
 (S3) 400mA/DIMM*4 MAX.



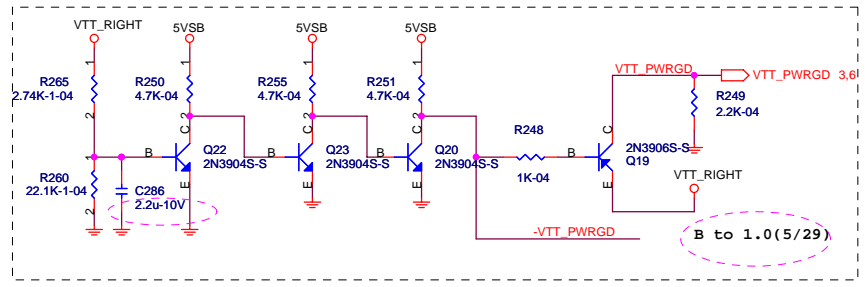
$$\frac{0.8}{100} = \frac{V_{out}}{(100+127)}$$

$$V_{out} = 1.816V$$

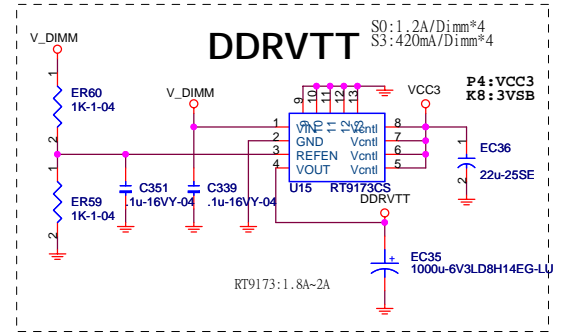
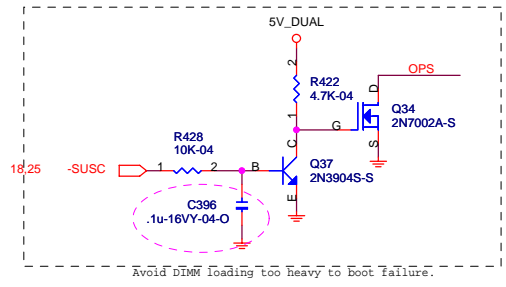


For VTT Power Good Signal

(VTT to VTT_PWRGD delay time: 1~20ms)



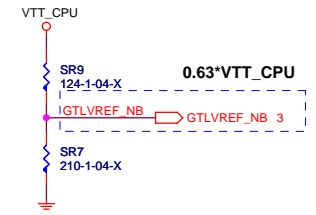
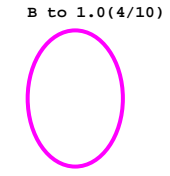
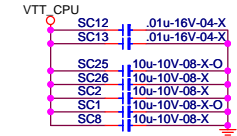
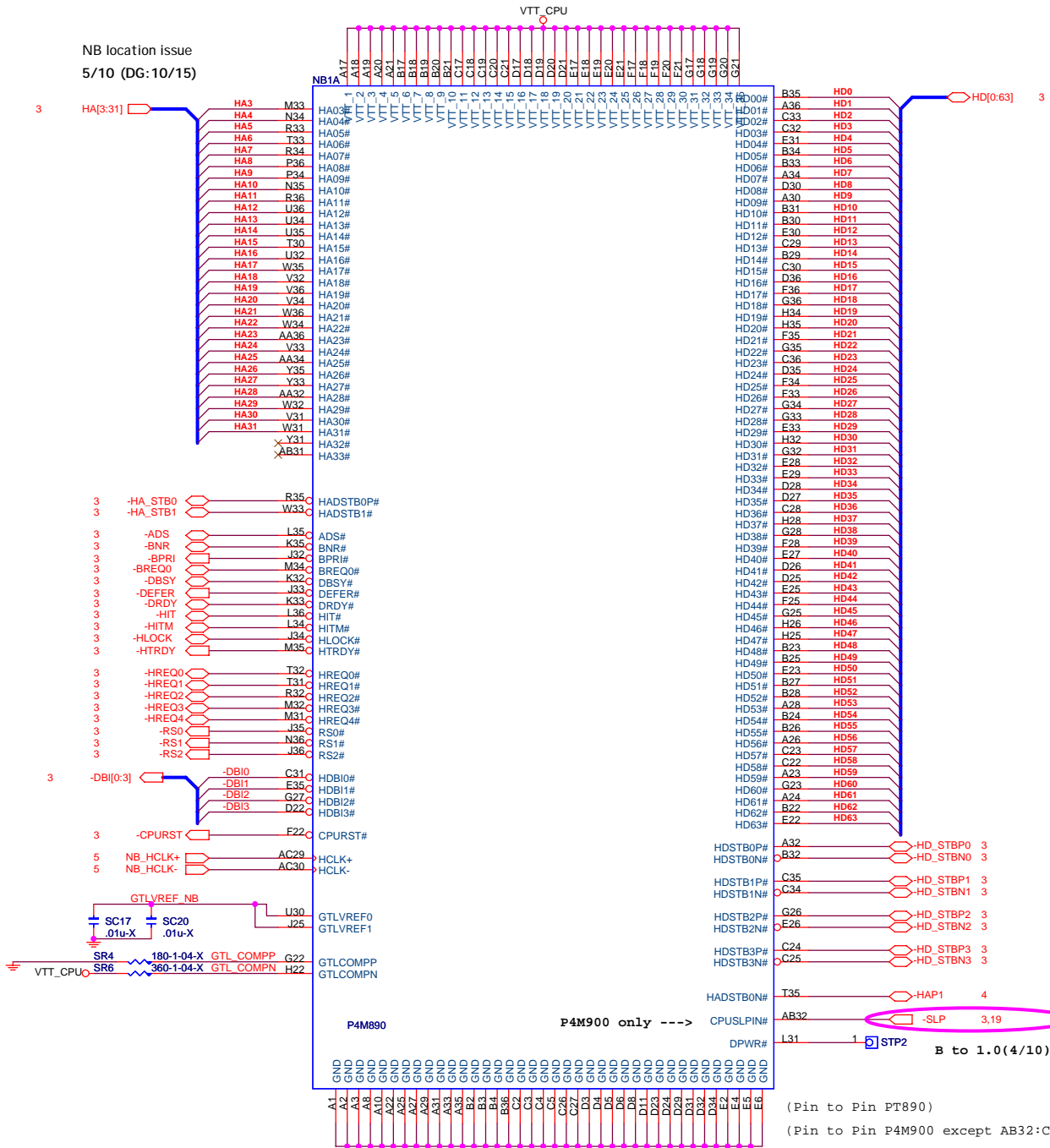
S5: disable V_DIMM



Elitegroup Computer Systems

Title			Rev
VDIMM & DDR VTT			
Size	Document Number	Rev	
Custom	P4M890T-M	1.0	
Date:	Thursday, June 15, 2006	Sheet	8 of 29

NB location issue
5/10 (DG:10/15)



	P4M890	P4M900
pin(AB32)	NC	CPUSLPIN#

(Pin to Pin PT890)
(Pin to Pin P4M900 except AB32:CPUSLPIN#)
i) DDR2 667
ii) Int. DeltaChrome/DX9 support

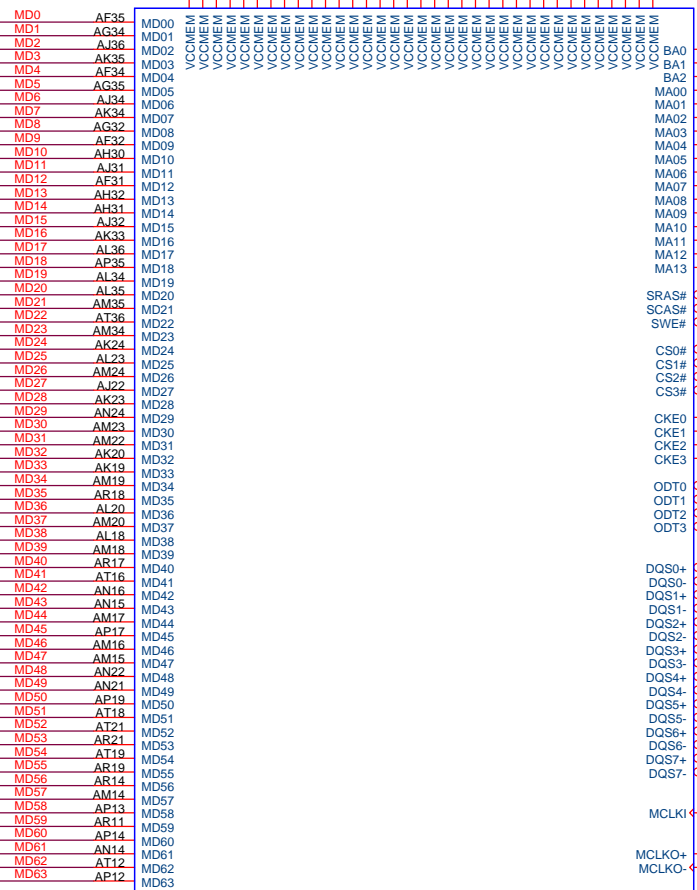
Elitegroup Computer Systems

Title: **NB1 (HOST)**

Size C Document Number: **P4M890T-M** Rev: **1.0**

Date: Thursday, June 15, 2006 Sheet 9 of 29

10/15
13,14 MD[0:63]



P4M890



NB location issue
5/10 (DG:10/15)

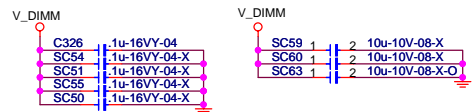
5/10(DG:10/15)

Differential Signal
15/10/15/10/15(DG)

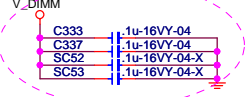
MCLK_FB = D2CLKx + 2 inch

MCLKO+/- as short as possible

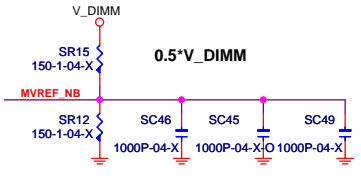
Strap low for DDR.



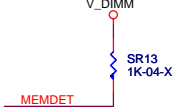
Near Chip:P4M890



Near DIMM slot



0.5*V_DIMM



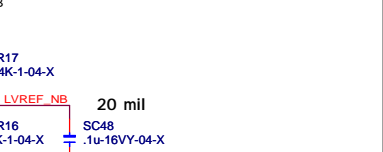
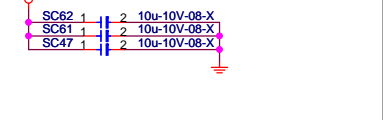
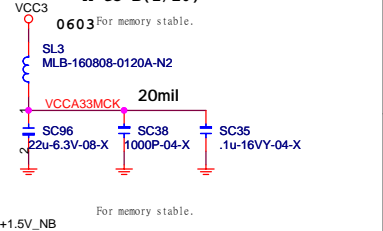
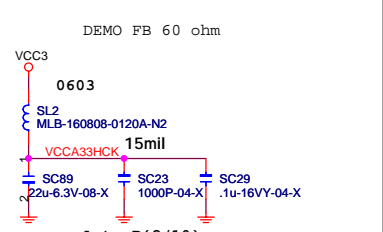
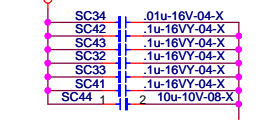
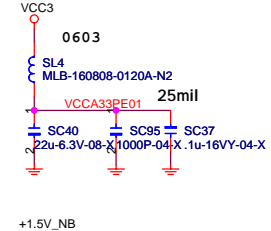
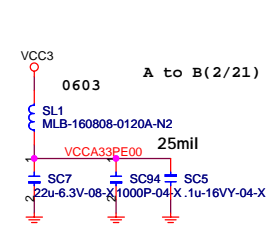
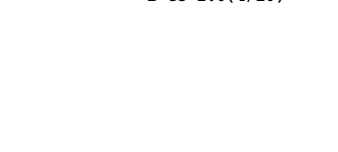
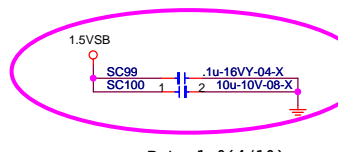
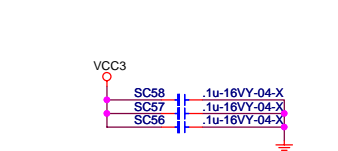
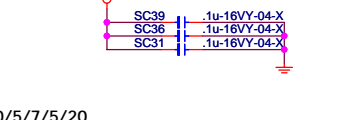
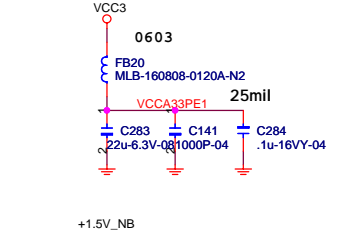
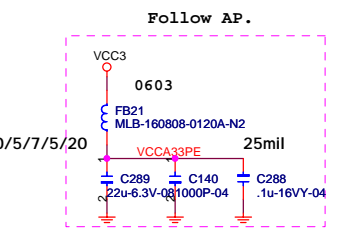
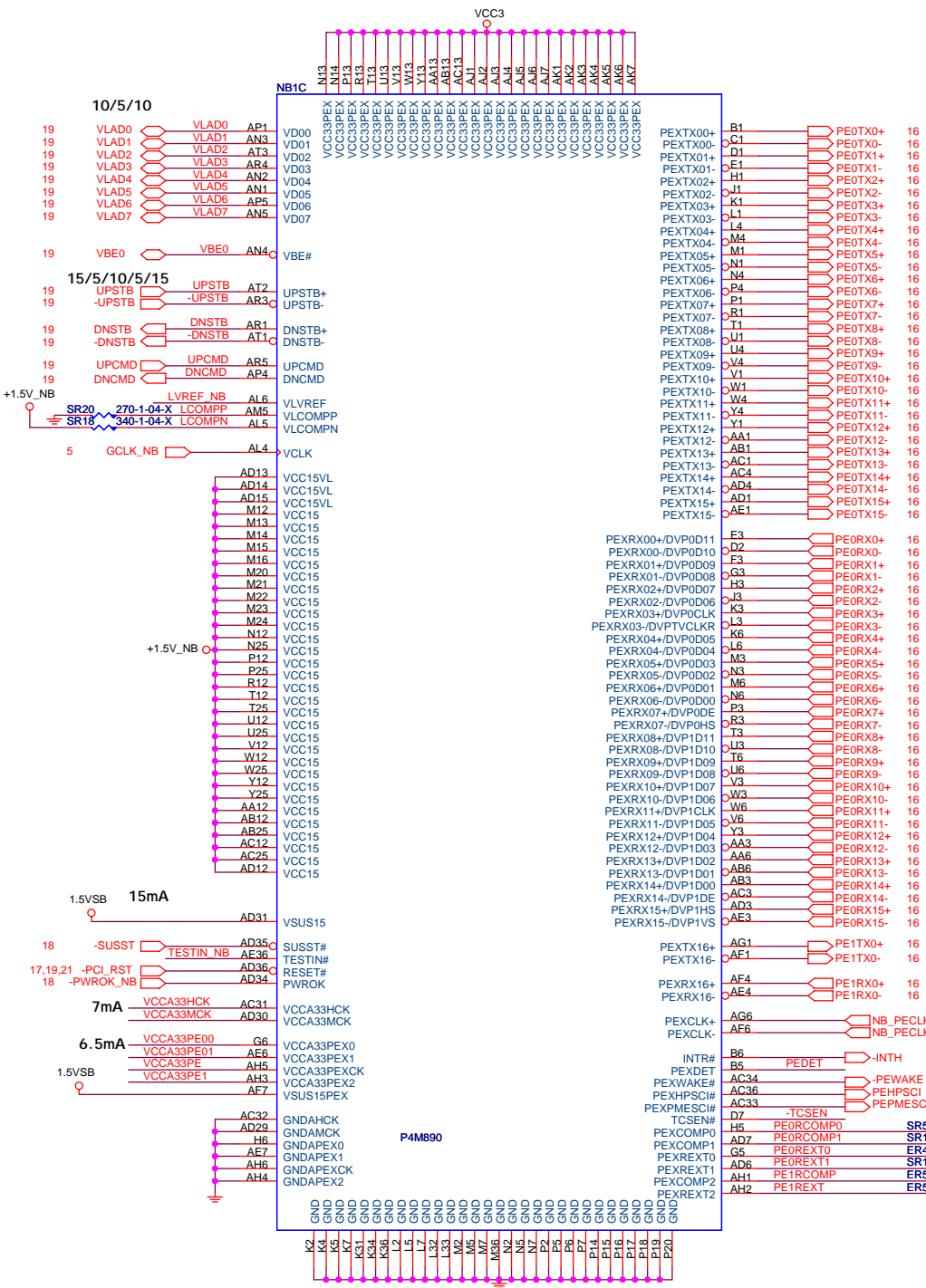
1: DDR2
0: DDR1

Elitegroup Computer Systems

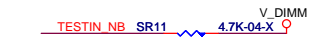
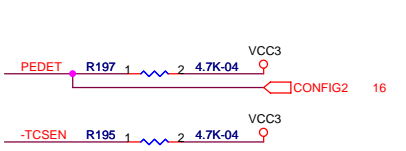
Title: **NB2 (Memory)**

Size C: Document Number **P4M890T-M** Rev **1.0**

Date: Thursday, June 15, 2006 Sheet 10 of 29



Strapping For NB_TEST Mode				
TESTIN	BISTIN	RBF	WBF	
1	1	x	x	
Disable all TEST mode				

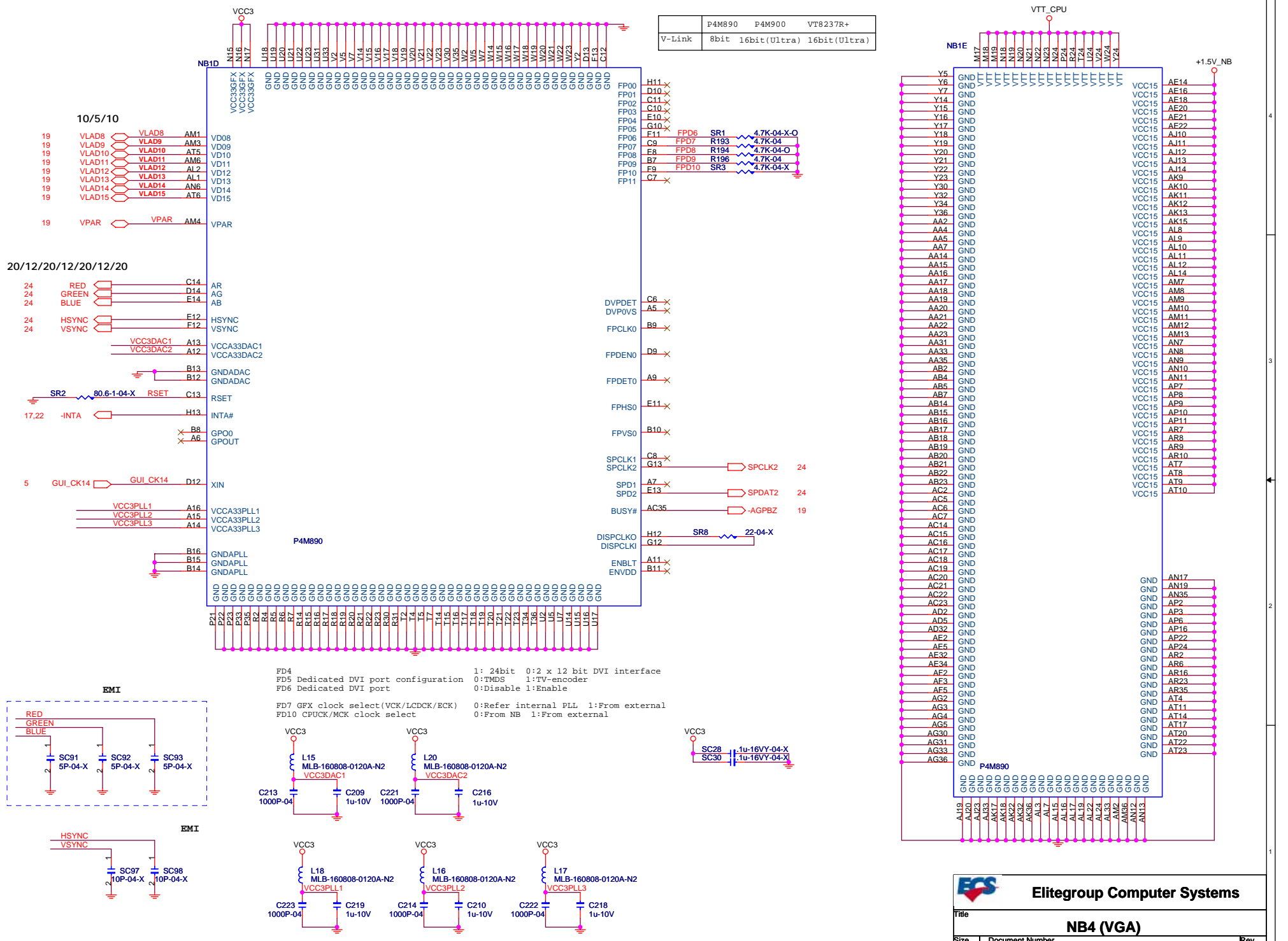


Elitegroup Computer Systems

Title: **NB3 (PCIE, VLINK)**

Size C Document Number: **P4M890T-M** Rev: **1.0**

Date: Thursday, June 15, 2006 Sheet 11 of 29



Elitegroup Computer Systems

Title: **NB4 (VGA)**

Size: Custom Document Number

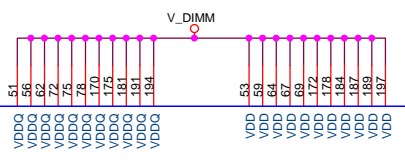
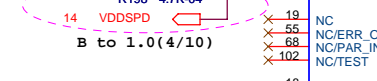
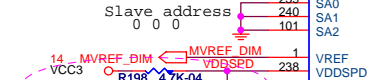
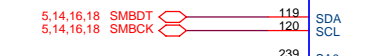
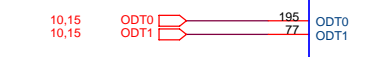
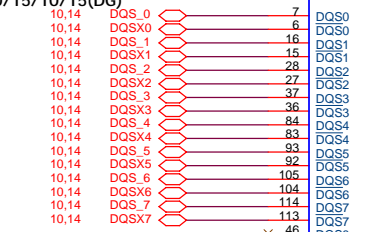
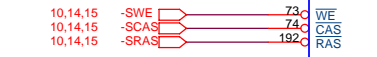
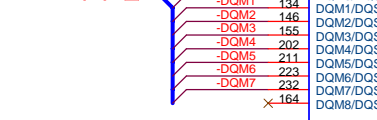
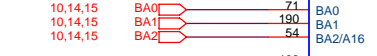
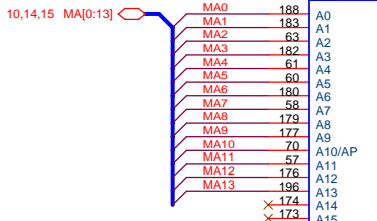
Part Number: **P4M890T-M**

Date: Thursday, June 15, 2006

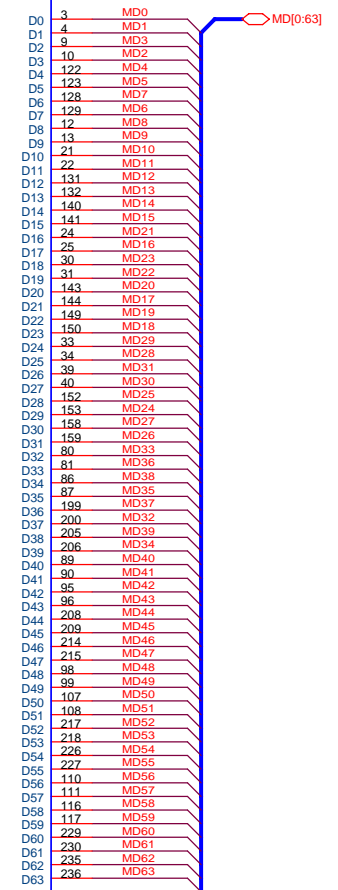
Sheet: 12 of 29

Rev: **1.0**

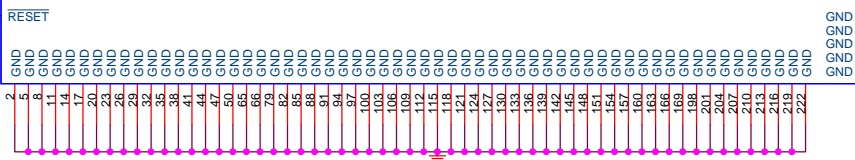
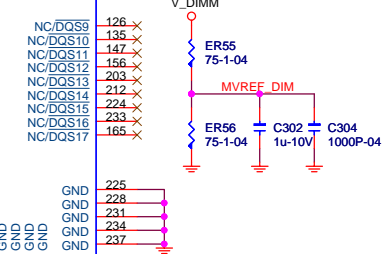
NB location issue
5/10 (DG:10/15)



10/15



12.5mV		12.5mV	
VID[4:0]:125	VCORE	VID[4:0]:125	VCORE
11111X	No CPU	110011	1.225
010100	0.8375	110010	1.2375
010011	0.850	110001	1.250
010010	0.8625	110000	1.2625
010001	0.875	101111	1.275
010000	0.8875	101110	1.2875
001111	0.900	101101	1.300
001110	0.9125	101100	1.3125
001101	0.925	101011	1.325
001100	0.9375	101010	1.3375
001011	0.950	101001	1.350
001010	0.9625	101000	1.3625
001001	0.975	100111	1.375
001000	0.9875	100110	1.3875
000111	1.000	100101	1.400
000110	1.0125	100100	1.4125
000101	1.025	100011	1.425
000100	1.0375	100010	1.4375
000011	1.050	100001	1.450
000010	1.0625	100000	1.4625
000001	1.075	011111	1.475
000000	1.0875	011110	1.4875
111101	1.100	011101	1.500
111100	1.1125	011100	1.5125
111011	1.125	011011	1.525
111010	1.1375	011010	1.5375
111001	1.150	011001	1.550
111000	1.1625	011000	1.5625
110111	1.175	010111	1.575
110110	1.1875	010110	1.5875
110101	1.200	010101	1.600
110100	1.2125		



Elitegroup Computer Systems

Title: **DDR II Slot1**

Size: Document Number
Custom: **P4M890T-M**

Date: Thursday, June 15, 2006

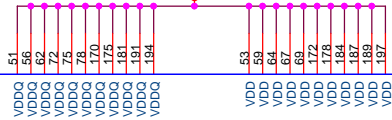
Sheet 13 of 29

Rev: **1.0**

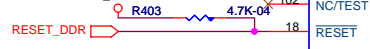
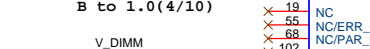
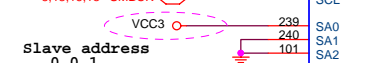
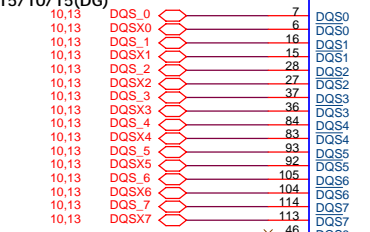
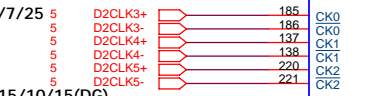
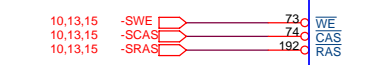
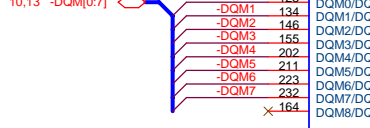
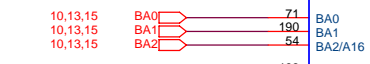
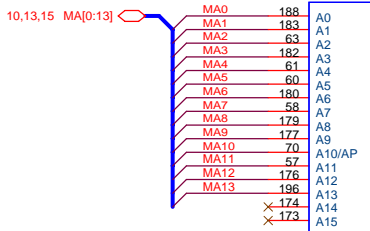
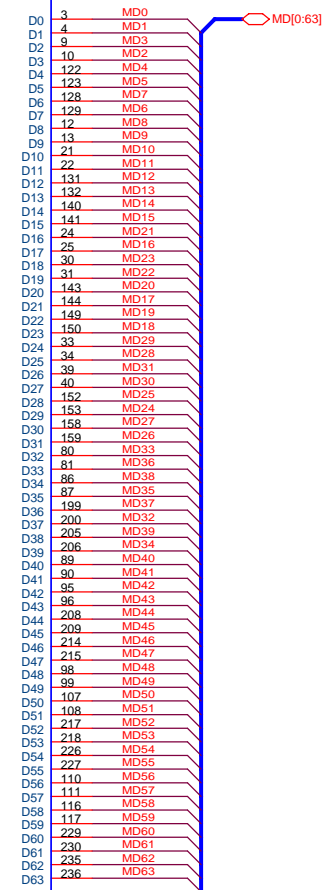
NB location issue
5/10 (DG:10/15)

V_DIMM

DDRII2



10/15

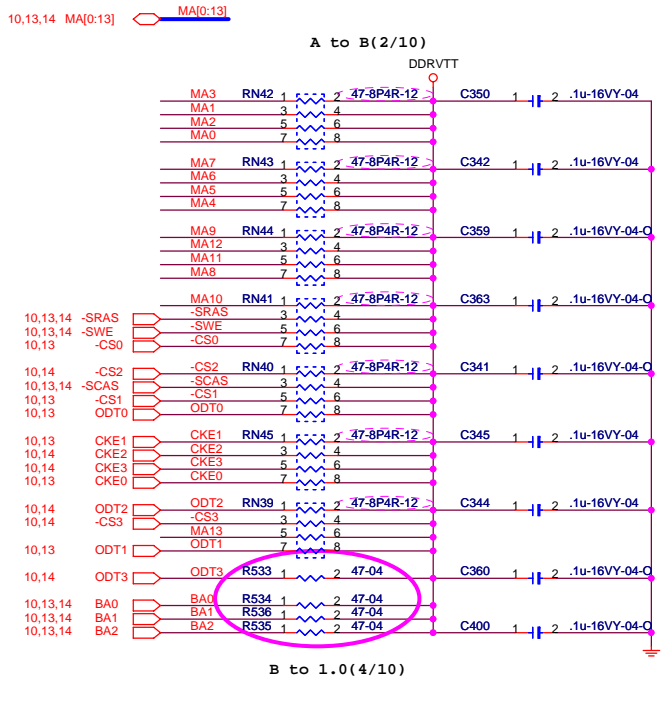
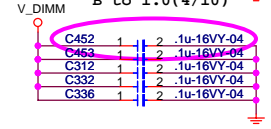
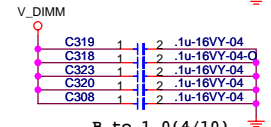
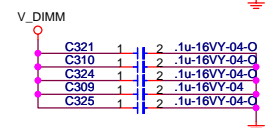
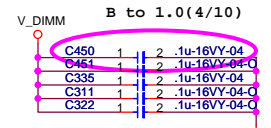
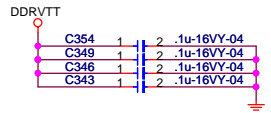


ECS Elitegroup Computer Systems

Title: **DDR2 SLOT2**

Size: Custom Document Number: **P4M890T-M** Rev: **1.0**

Date: Thursday, June 15, 2006 Sheet 14 of 29



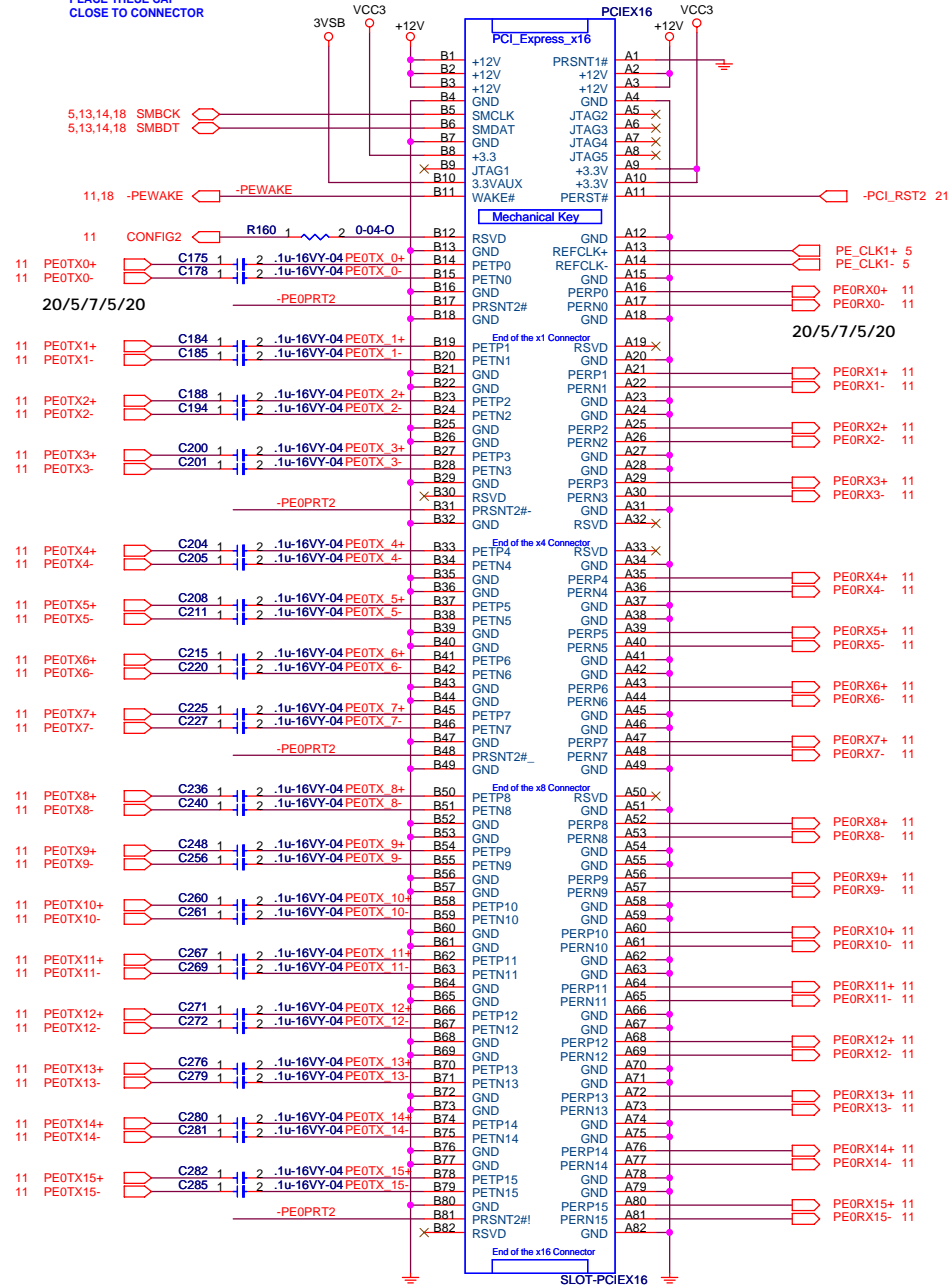
VIA demo board:33 ohm



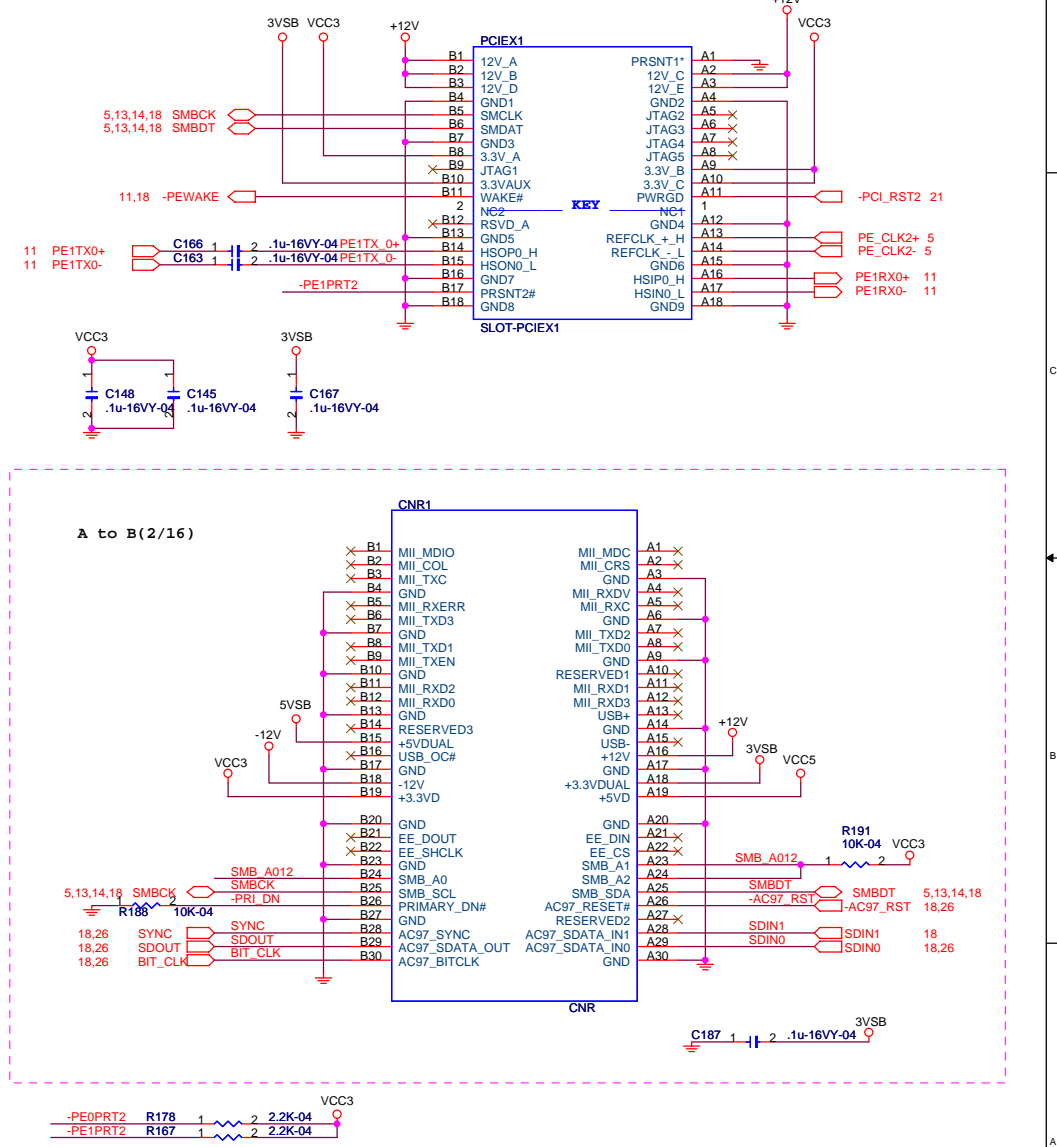
PCI_Express_X16

+12V: 5.5Amp
+3.3V: 3Amp

PLACE THESE CAP
CLOSE TO CONNECTOR



PCI_Express_X1



The system board designer determines the pull-up voltage.

JTAG	Test Access Port and Boundary Scan Architecture.
PRSNT	1. Add-in card presence detect pin. 2. For hot plug add-in card. (power off when you remove or insert)

Elitegroup Computer Systems

Title: **PCI Express Slot X16, X1, CNR**

Size: Custom | Document Number: **P4M890T-M** | Rev: **1.0**

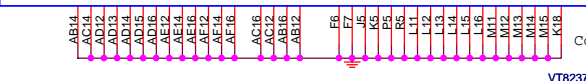
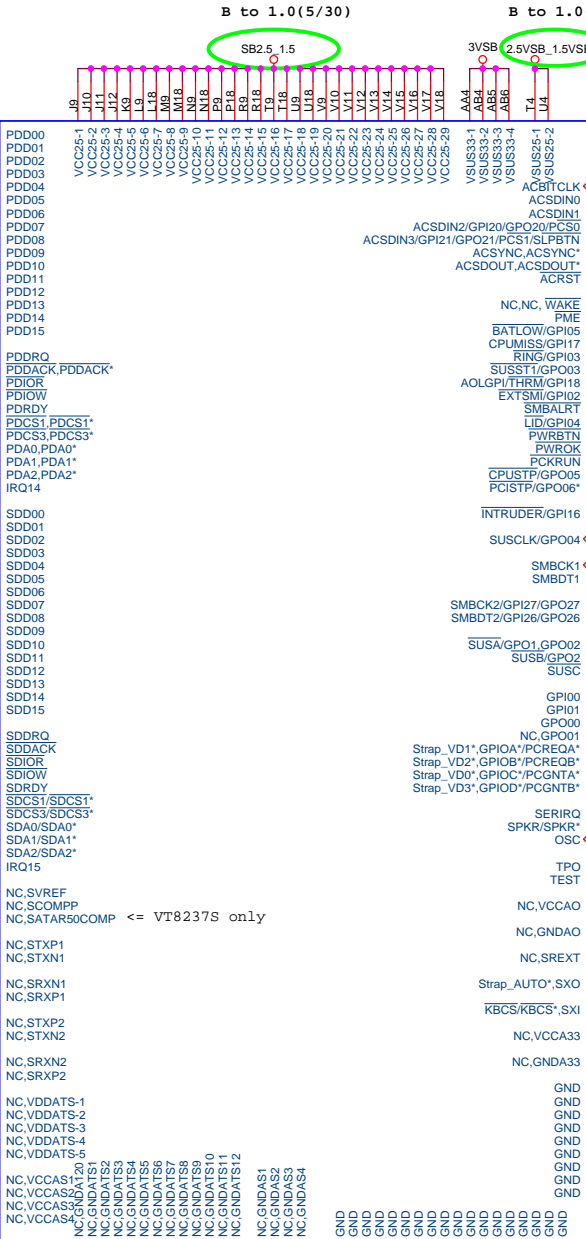
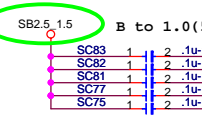
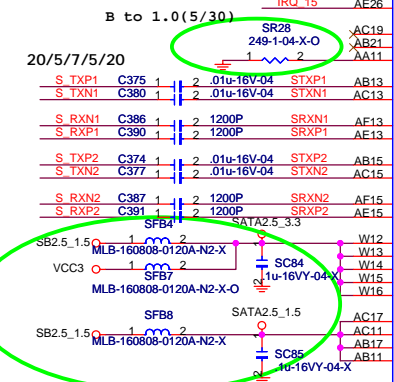
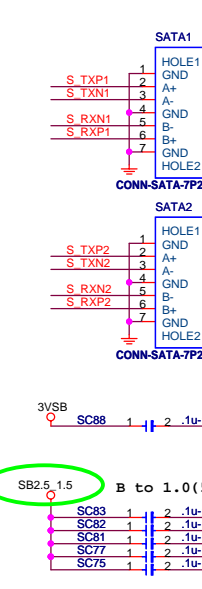
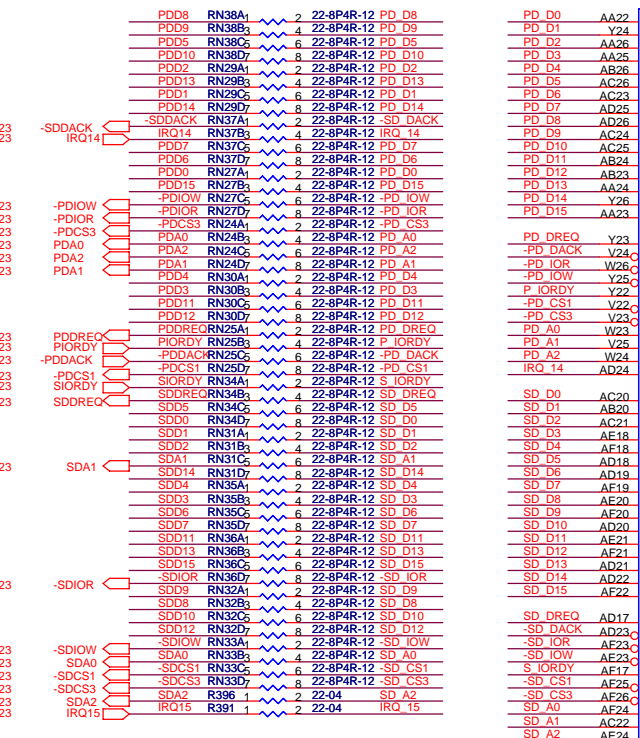
Date: Thursday, June 15, 2006 | Sheet: 16 of 29

23 PDD[15:0]

23 SDD[15:0]

I2E damping resistors	VT8237R+	VT8237A
	Required	change to 0 ohm (Internal pull 22)

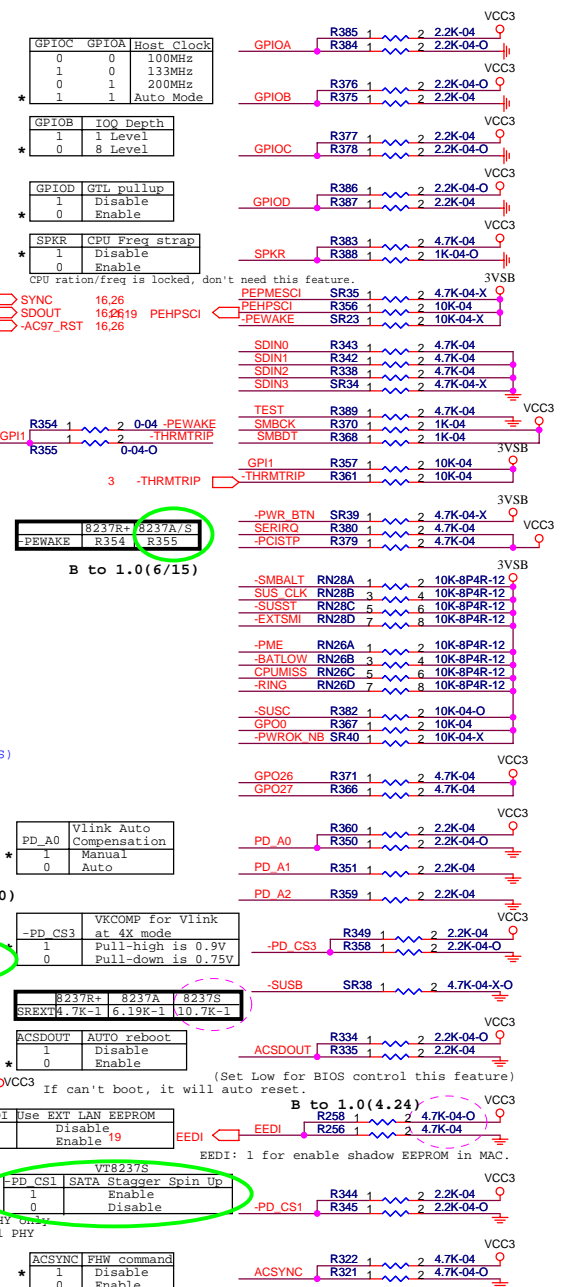
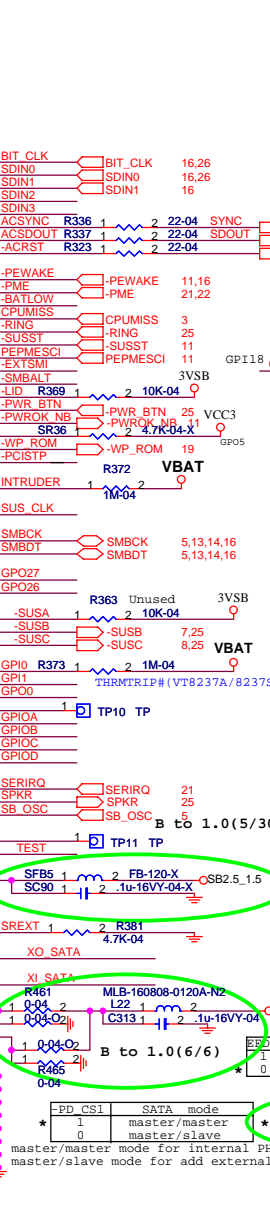
ALL: 10/5/10



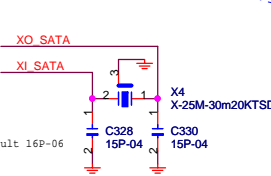
VT8237R+/VT8237A
PEPMESCI connect to GP118
PEHPSCI connect to GP119

	8237R+	8237A
-PEWAKE	GP118 (AC2)	-WAKE (V5)
PEPMESCI	GP118	GP118
PEHPSCI	GP119	GP119
-THRMTrip	NA	GP11 (AC2)

Pin 8237R	8237A
V5	NC
Y4	GP118
U23	GP119



-PD DACK	8237R+	8237A/8237S
External SATA PHY	1:Disable	N/A

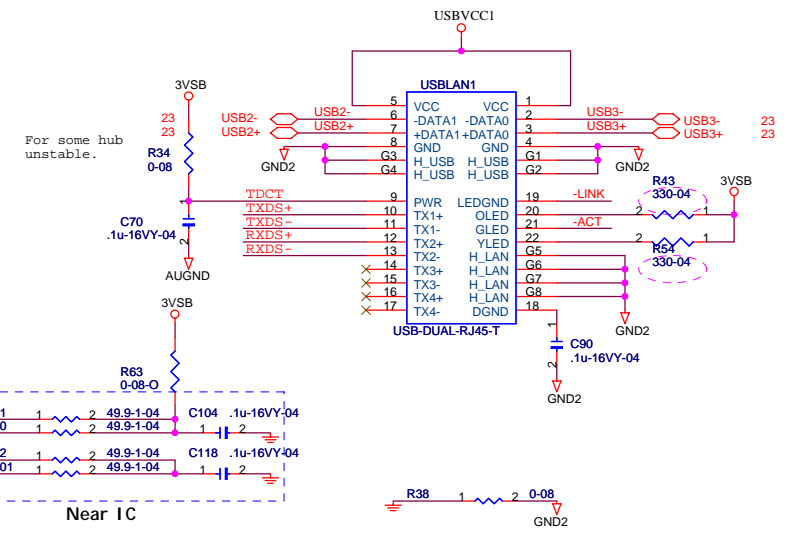
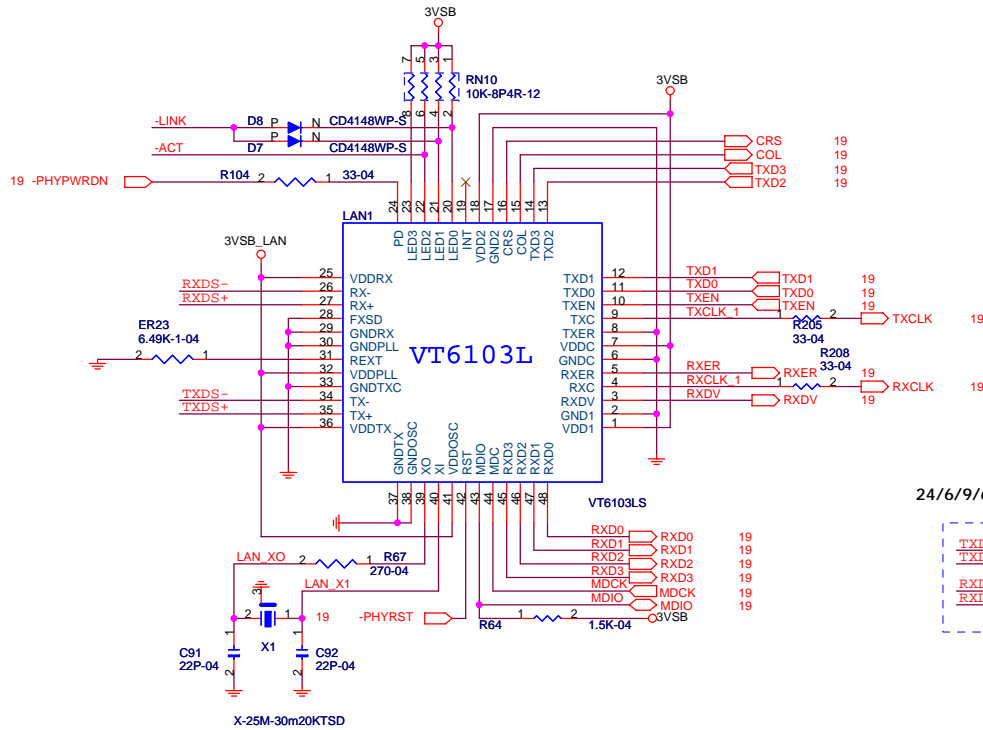
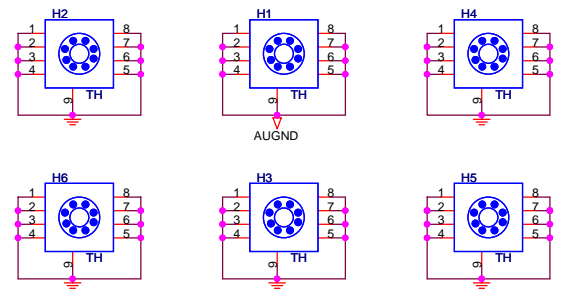
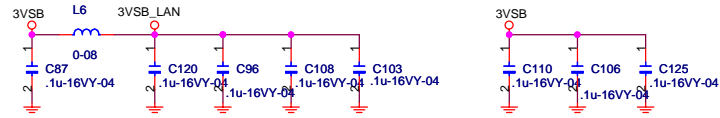


Elitegroup Computer Systems

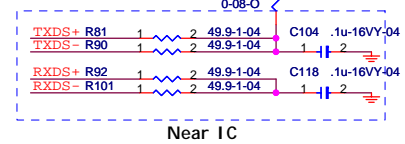
SB (IDE, GPIO, AC-LINK)

Size: Custom Document Number: P4M890T-M Rev: 1.0

Date: Thursday, June 15, 2006 Sheet: 18 of 29



24/6/9/6/24



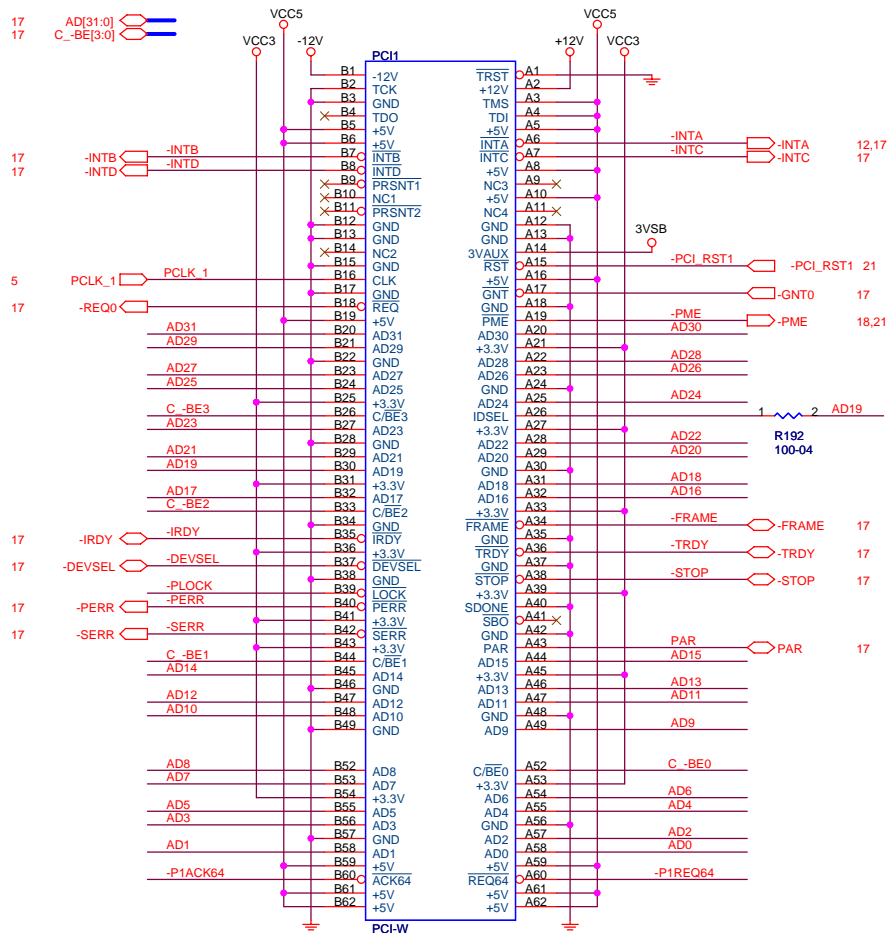
	LED0	LED1	LED2	LED3	
00	LINK /ACT	SPEED	DUPLEX	COL	
01	PWR /TXACT	LINK /RXACT	SPEED	DUPLEX	
* 10	SPEED 100	SPEED 10	ACT	DUPLEX	Default
11	PWR /TXACT	LINK /RXACT	SPEED	COL	

Elitegroup Computer Systems

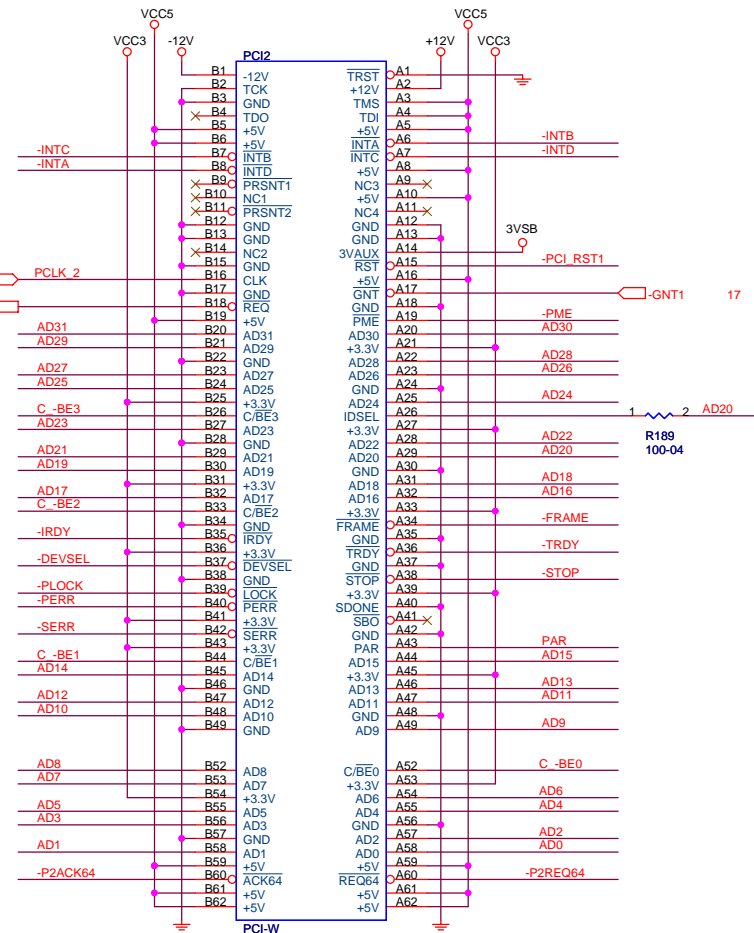
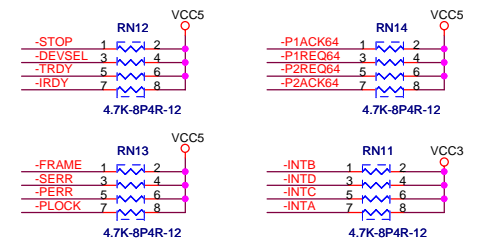
Title: **LAN (VT6103L)**

Size: Custom Document Number: **P4M890T-M** Rev: **1.0**

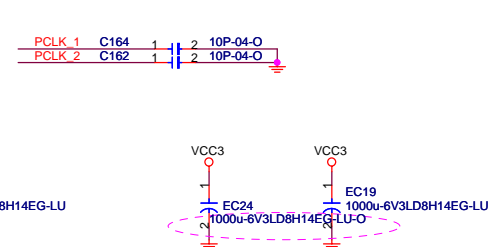
Date: Thursday, June 15, 2006 Sheet: 20 of 29




**INT:A
IDSEL:AD19**

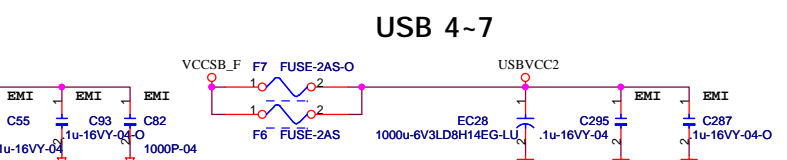
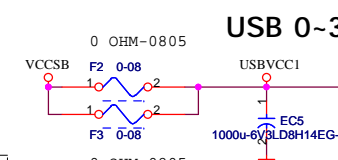
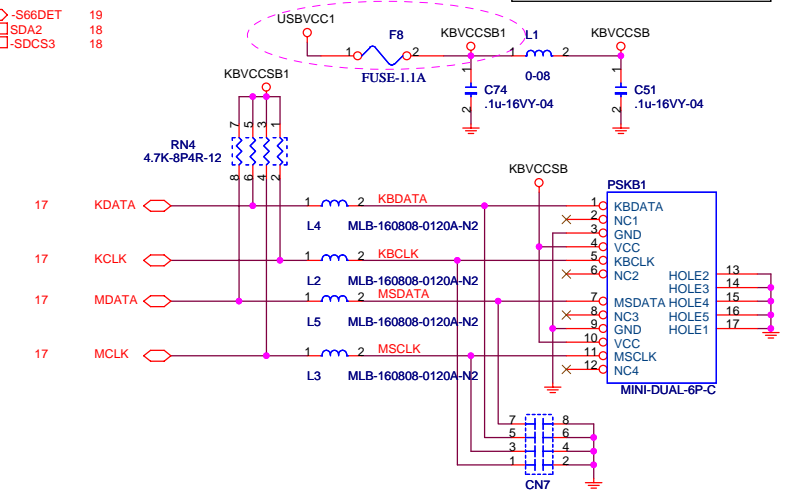
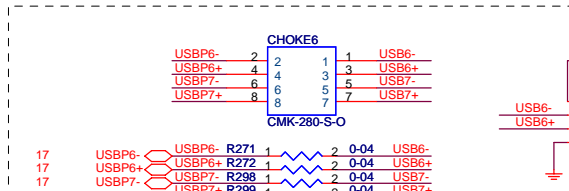
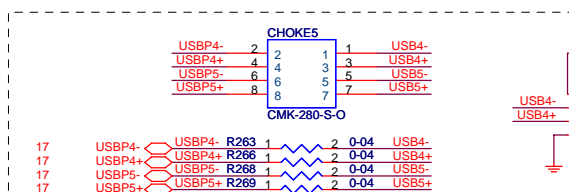
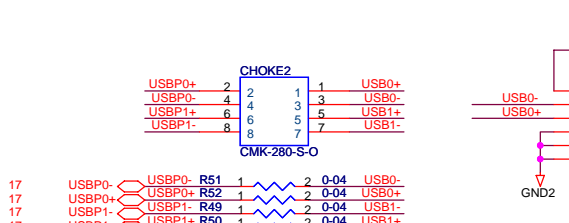
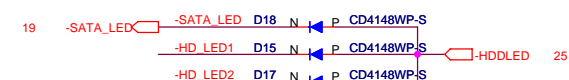
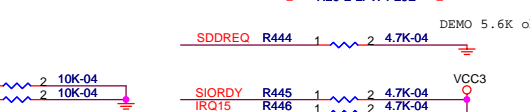
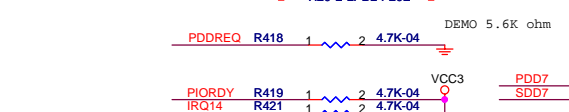
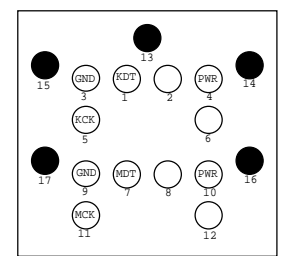
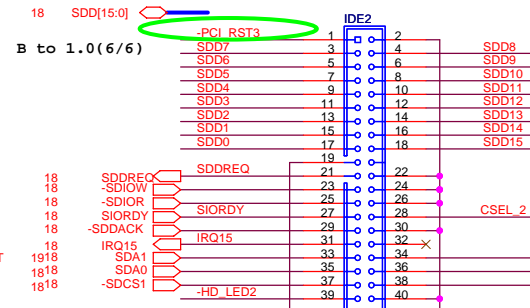
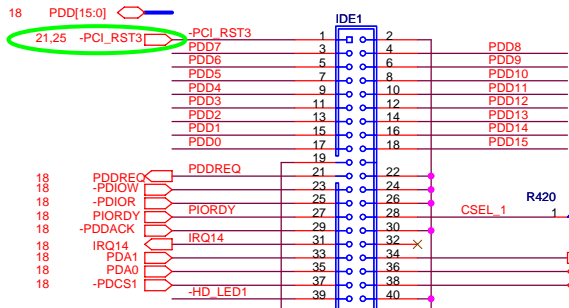


**INT:B
IDSEL:AD20**



B to 1.0 (5/23)

 Elitegroup Computer Systems		
Title PCI 1 & PCI 2		
Size Custom		Document Number P4M890T-M
Date: Thursday, June 15, 2006		Rev 1.0
Sheet 22		of 29



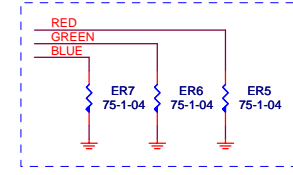
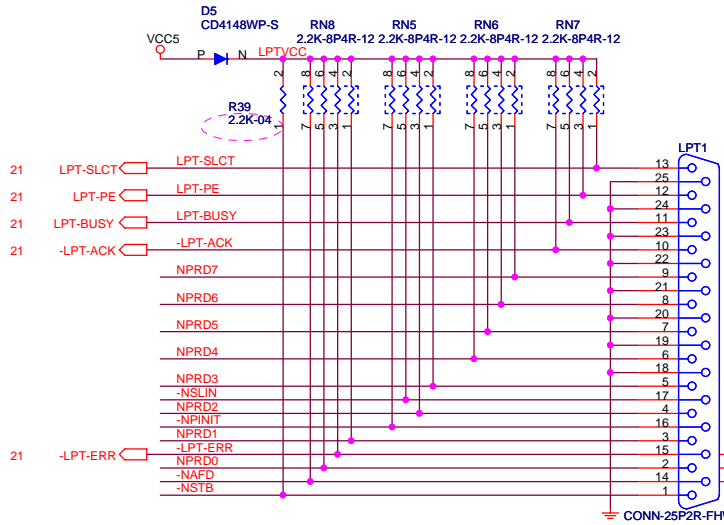
Elitegroup Computer Systems

Title: **USB, PS2, IDE**

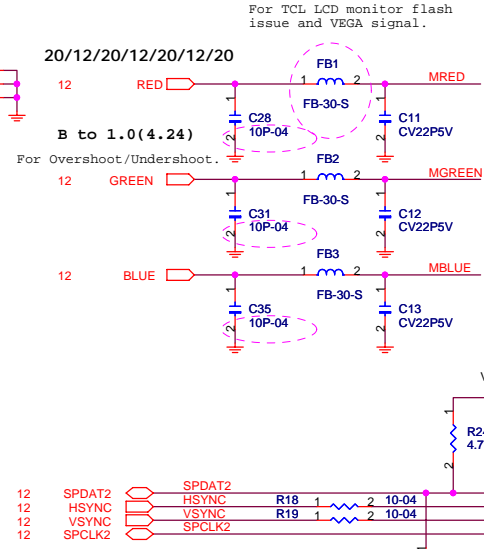
Size: Document Number **P4M890T-M** Rev **1.0**

Date: Thursday, June 15, 2006 Sheet 23 of 29

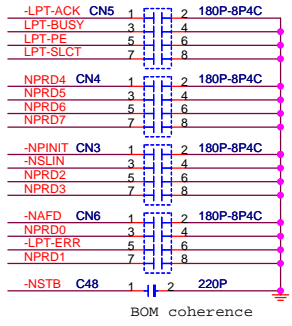
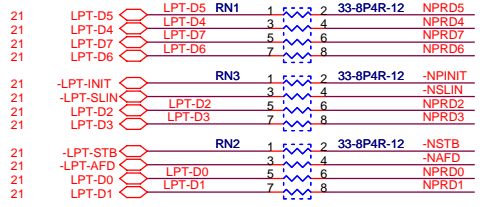
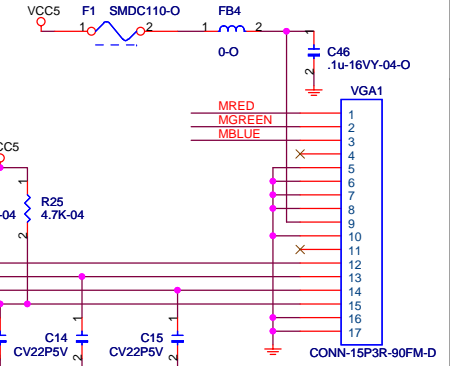
LPT



Closed to VGA connector (follow DG).

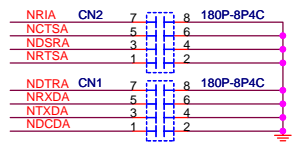
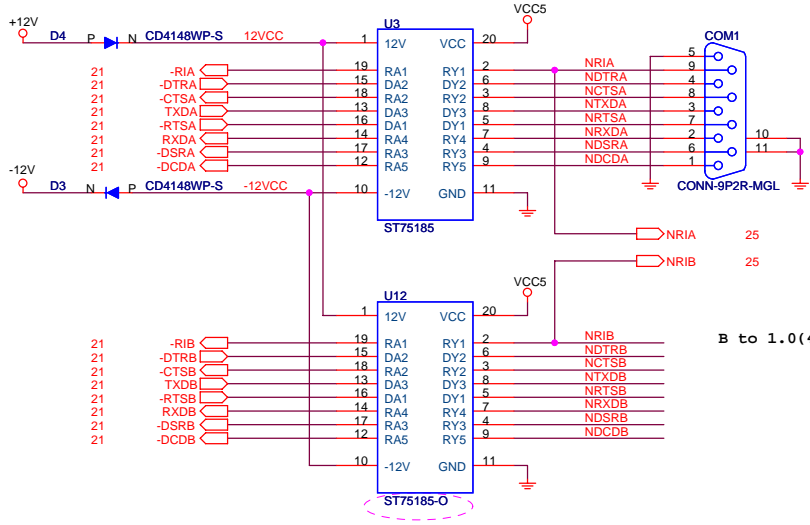


VGA

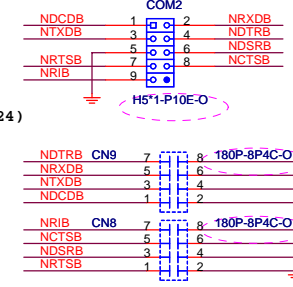


BOM coherence

COM 1



COM 2



B to 1.0 (4.24)

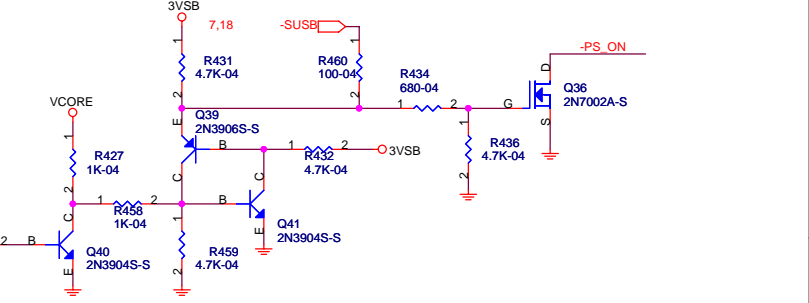
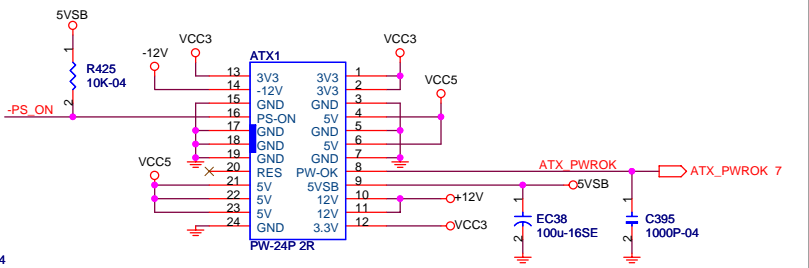
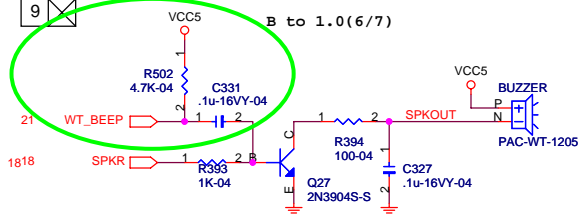
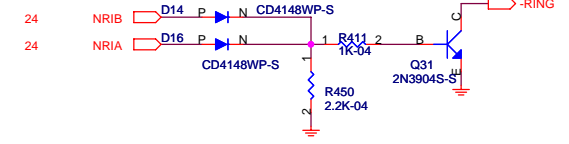
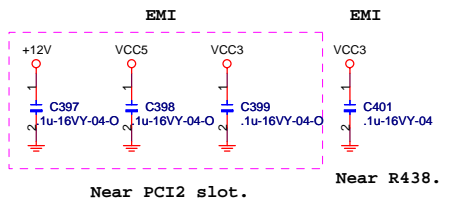
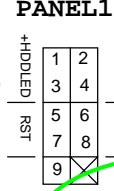
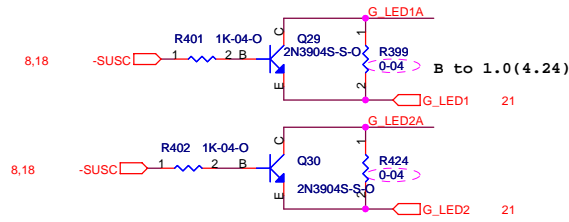
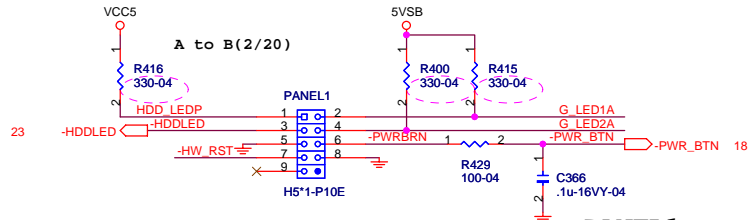
Elitegroup Computer Systems

COM, LPT, VGA

P4M890T-M

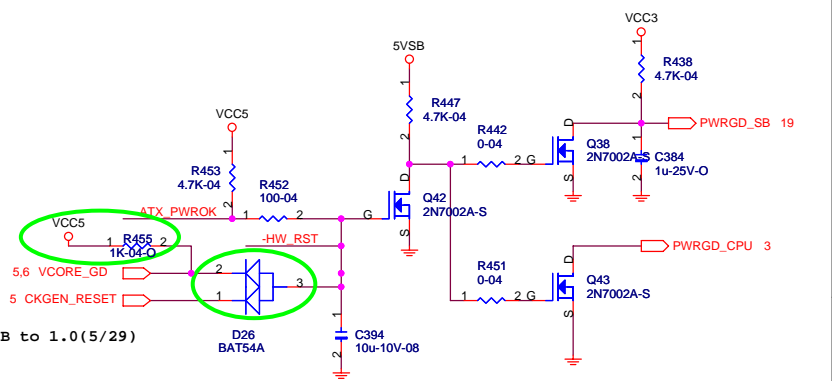
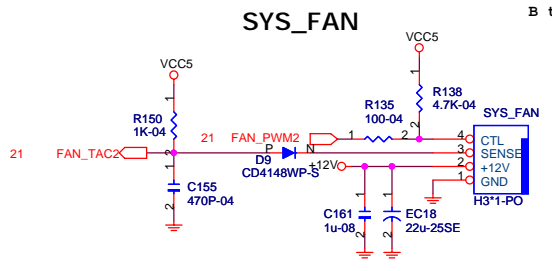
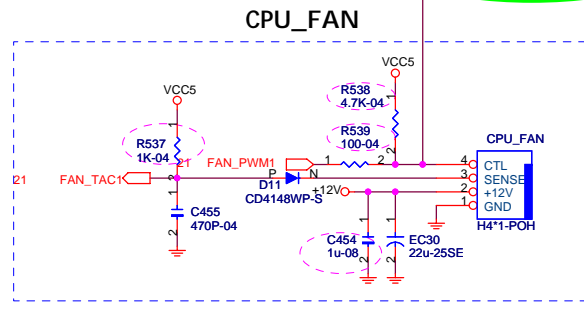
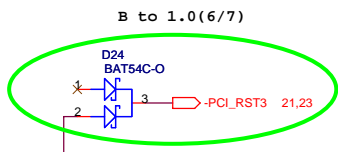
Rev **1.0**

Date: Thursday, June 15, 2006 Sheet 24 of 29



-RSMRST	-SUSST1	-SUSA	-SUSB	-SUSC	MODE
0	0	0	0	0	Mechanical off
1	0	0	0	0	S4/S5
1	0	0	0	1	S3
1	0	0	1	1	S1
1	0	1	1	1	S0 (ON)

	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking Yellow	Dark
LSJ1(1,2)	Dark	Dark Blinking	Light	Dark
SJ1(1,3)(2,3)	Light		Blinking	Dark
GLEDD1	HIGH	HIGH	LOW	HIGH
GLEDD2	LOW	LOW	SWITCH	HIGH



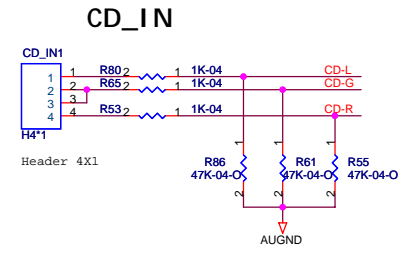
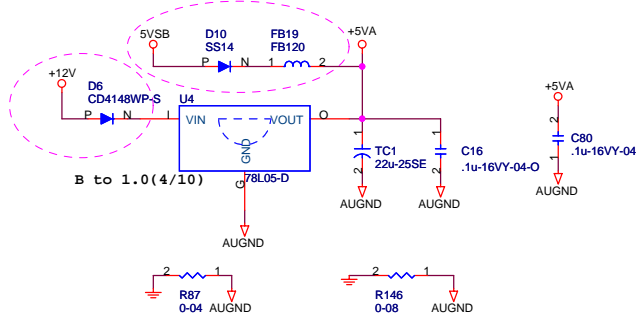
For reset button hang "FF" issue.

Elitegroup Computer Systems

Title: **FRONT PANEL, FAN, ATX24P**

Size: Custom Document Number: **P4M890T-M** Rev: **1.0**

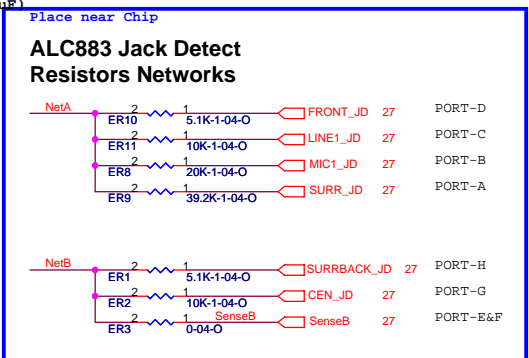
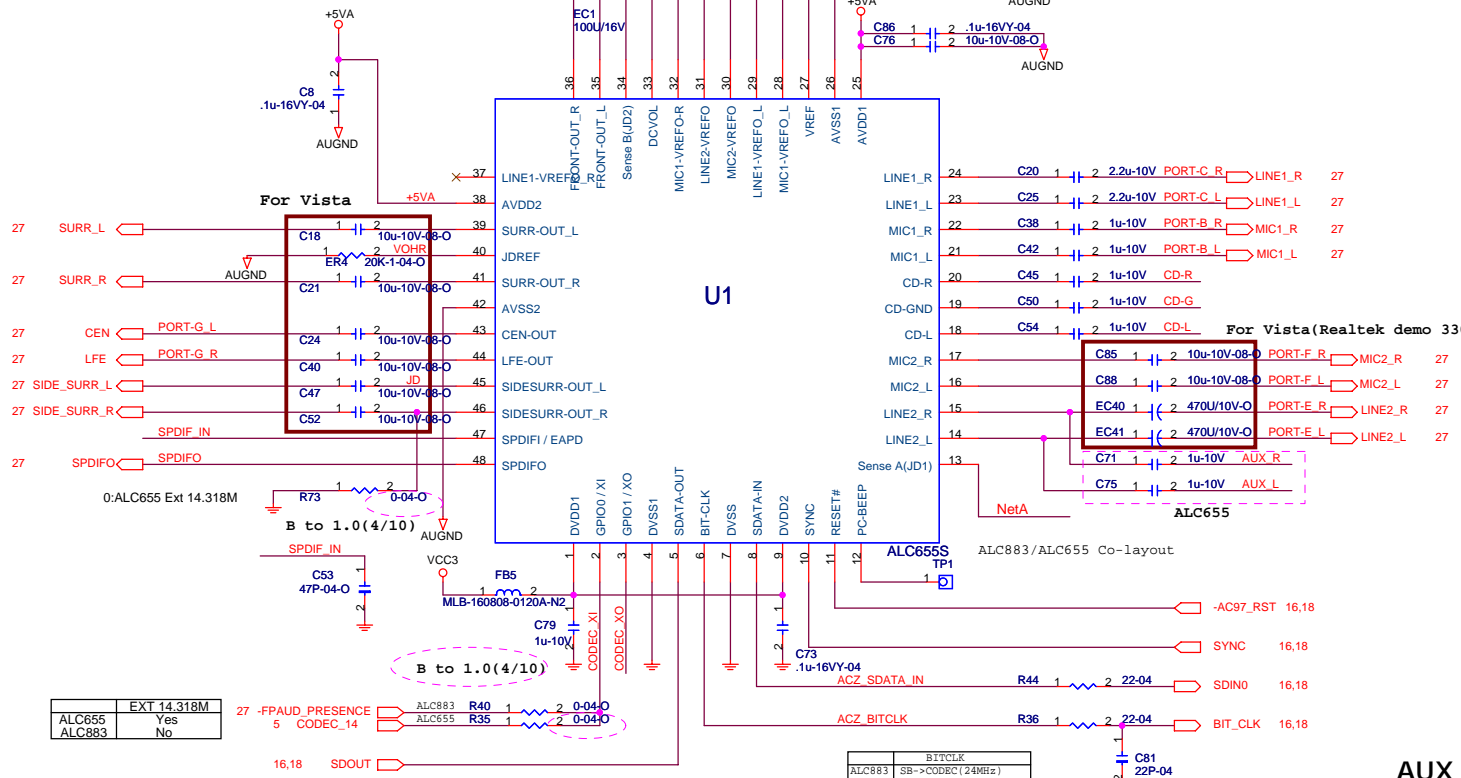
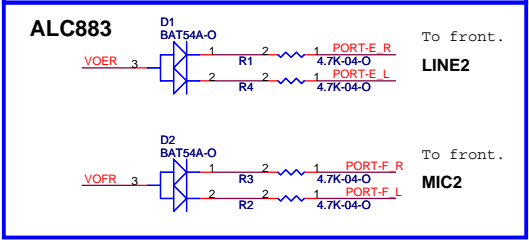
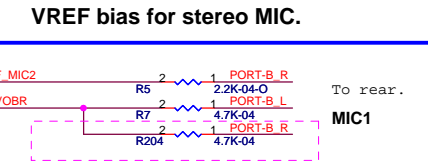
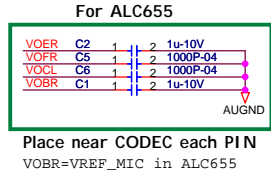
Date: Thursday, June 15, 2006 Sheet 25 of 29



	ALC655	ALC883
R5	X	2.2K
R7	4.7K	2.2K
R204	4.7K	X

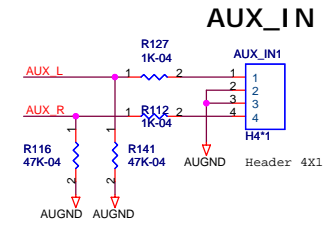
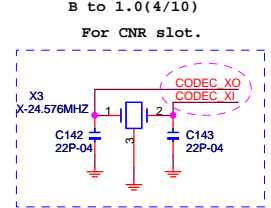
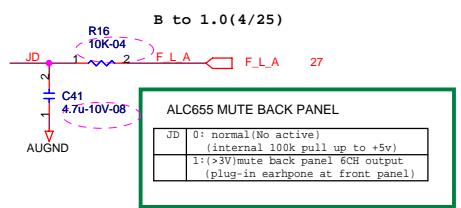
	EC1EC2
ALC655	100uF/16V
ALC883	470uF/10V

For Vista (Realtek demo 330uF) EC2 100uF/16V



	EXT 14.318M
ALC655	Yes
ALC883	No

	BITCLK
ALC883	SB->CODEC(14MHz)
ALC655	CODEC->SB(12.288MHz)

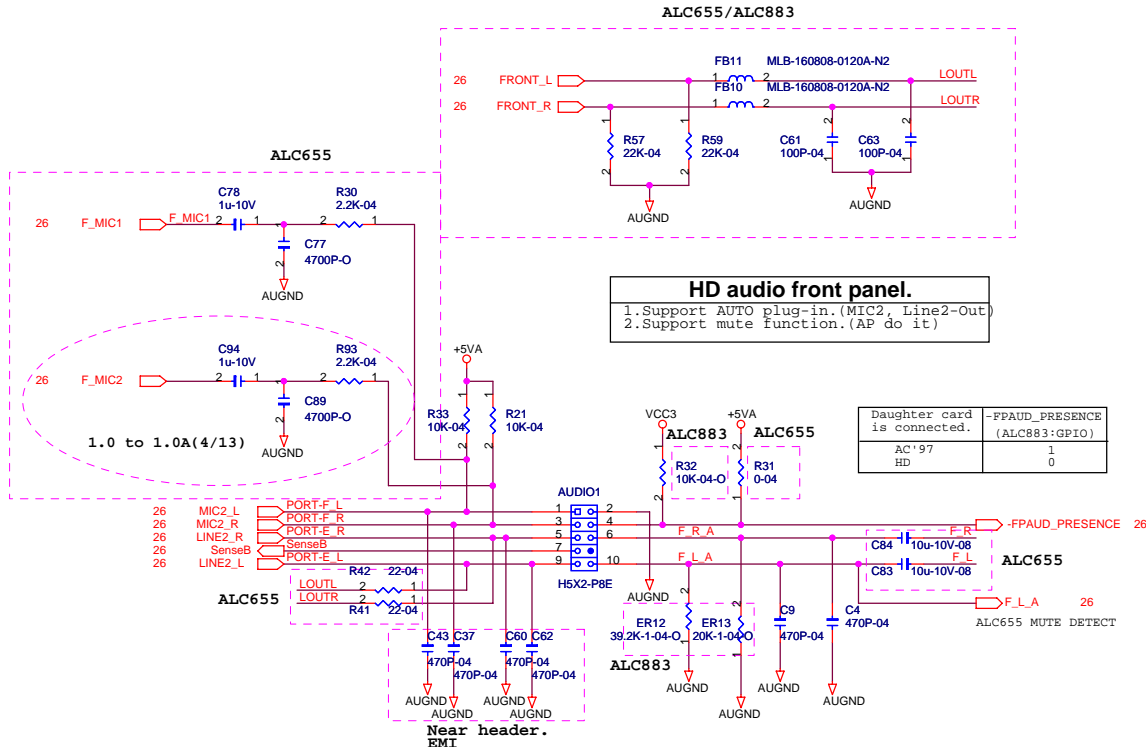


Elitegroup Computer Systems

ALC883 & ALC655 Chipset

Size: Document Number
 Custom: P4M890T-M
 Date: Monday, June 19, 2006
 Sheet: 26 of 29

Rev: 1.0

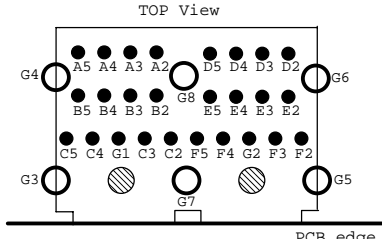
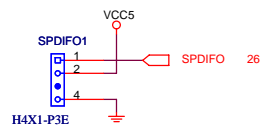


HD audio front panel.
 1.Support AUTO plug-in.(MIC2, Line2-Out)
 2.Support mute function.(AP do it)

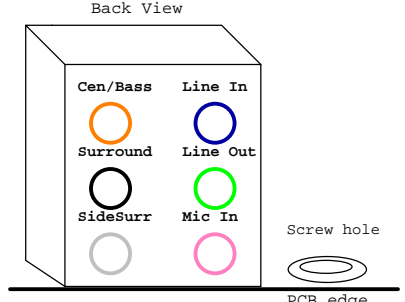
Daughter card is connected.	-FPAUD_PRESENCE (ALC883:GPIO)
AC'97	1
HD	0

Near header.
EMI

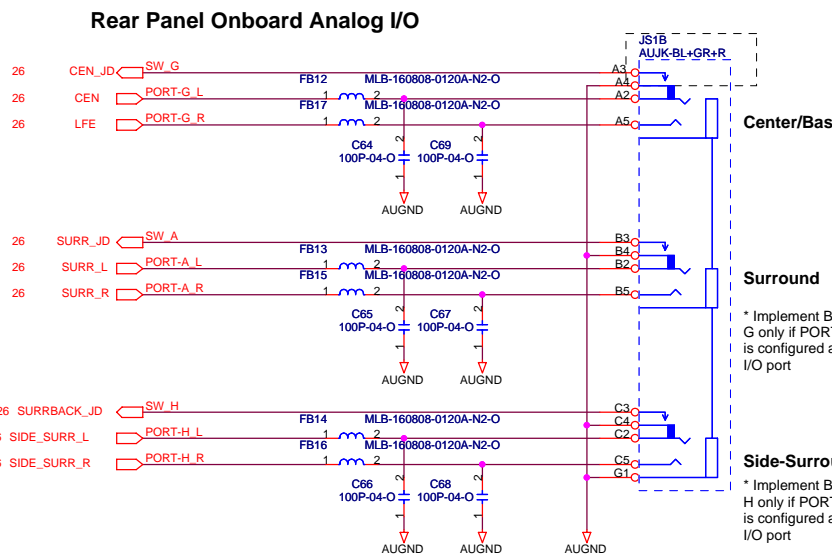
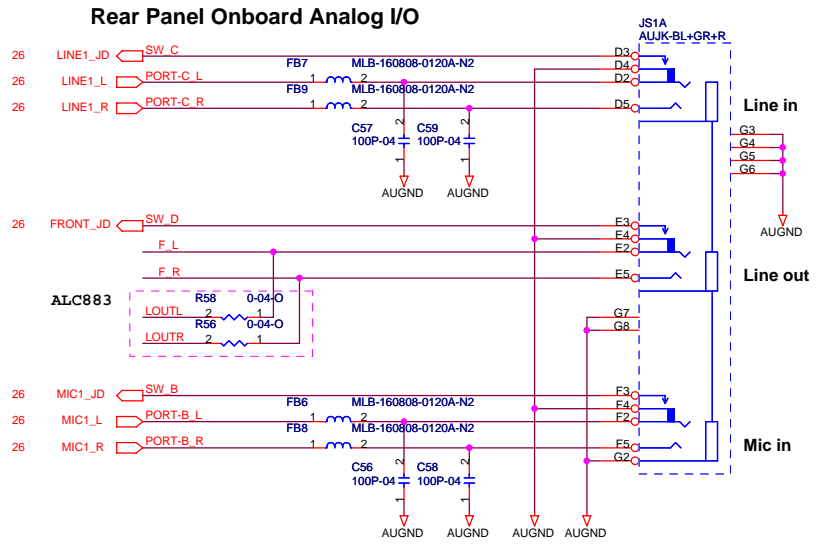
SPDIF Out



Cen/LFE: Center/Lower Frequency Enhancement (Bass)



HD connector
 1.Pin x3,x4 Normal open(Combo Jack).
 2.Pin x3 ,x4 short if jack is plug-in.
 3.Support Semi-AUTO plug-in.(Line-In, Line-Out, Mic)



	ALC655	ALC883
JS1	6-CH	8-CH
AUDIO1 header	Purple	Green
AUDIO1(5-6,9-10)	Short	NC

Elitegroup Computer Systems

ALC883 & ALC655 Connector

File: P4M890T-M Rev 1.0

Size: Custom Document Number

Date: Thursday, June 15, 2006 Sheet 27 of 29

