



G31T-M3

Rev :1.0

(P4 LGA775P Processor with DDR2 SDRAM Mainboard)

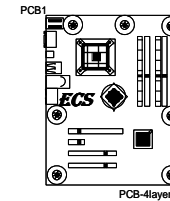
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REVISION HISTORY:

Rev	Date	Notes
A	1/2	First Release
1.0	2/19	Page 9: Add C160,C161,BC113 Page 20: C120,C121 change from 15PF to 10PF Page 23: Add BC5 Page 25: Add RT2,R68 Page 27: Delete R60,ER1,ER2,ER7,ER8 Page 28: Delete R231, Add C159

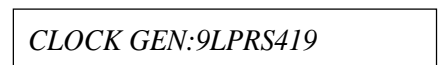
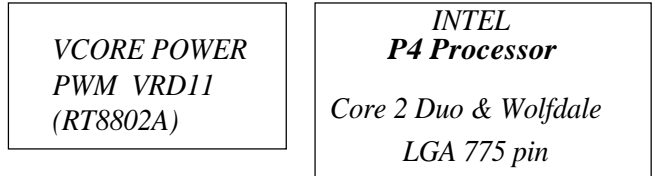


PCB-4layer

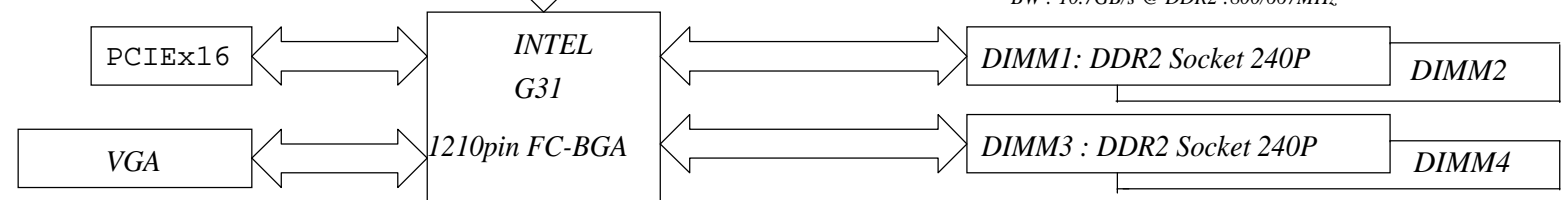
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

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Title: Cover Sheet		
Size: Custom	Document Number: G31T-M3	Rev: 1.0
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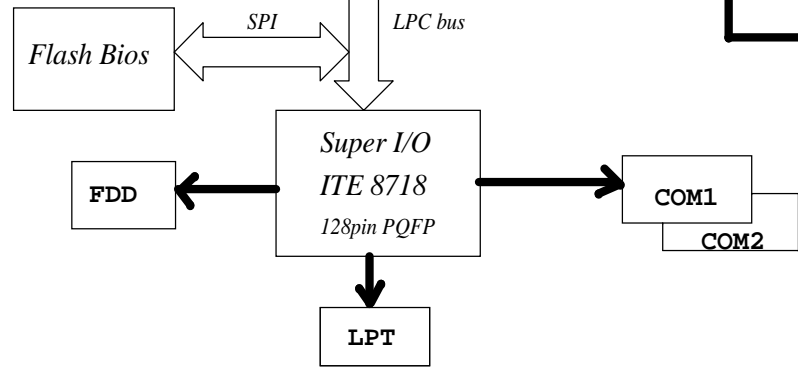
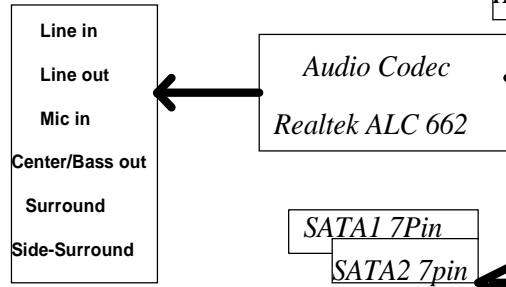
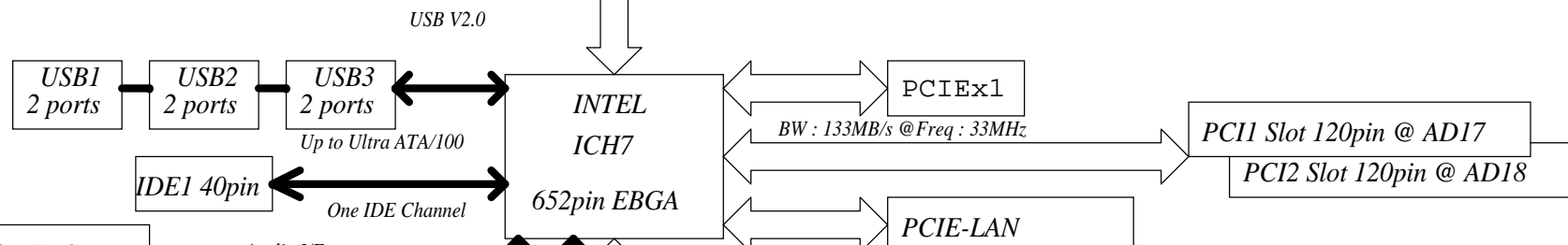
DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1



12/14新增
FSB : 1333MHz & Freq : 333MHz
FSB : 1066MHz & Freq : 266MHz
FSB : 800MHz & Freq : 200MHz



Analog Display
RAMDAC: 400MHz
Resolutions Up To 2048x1536@75Hz

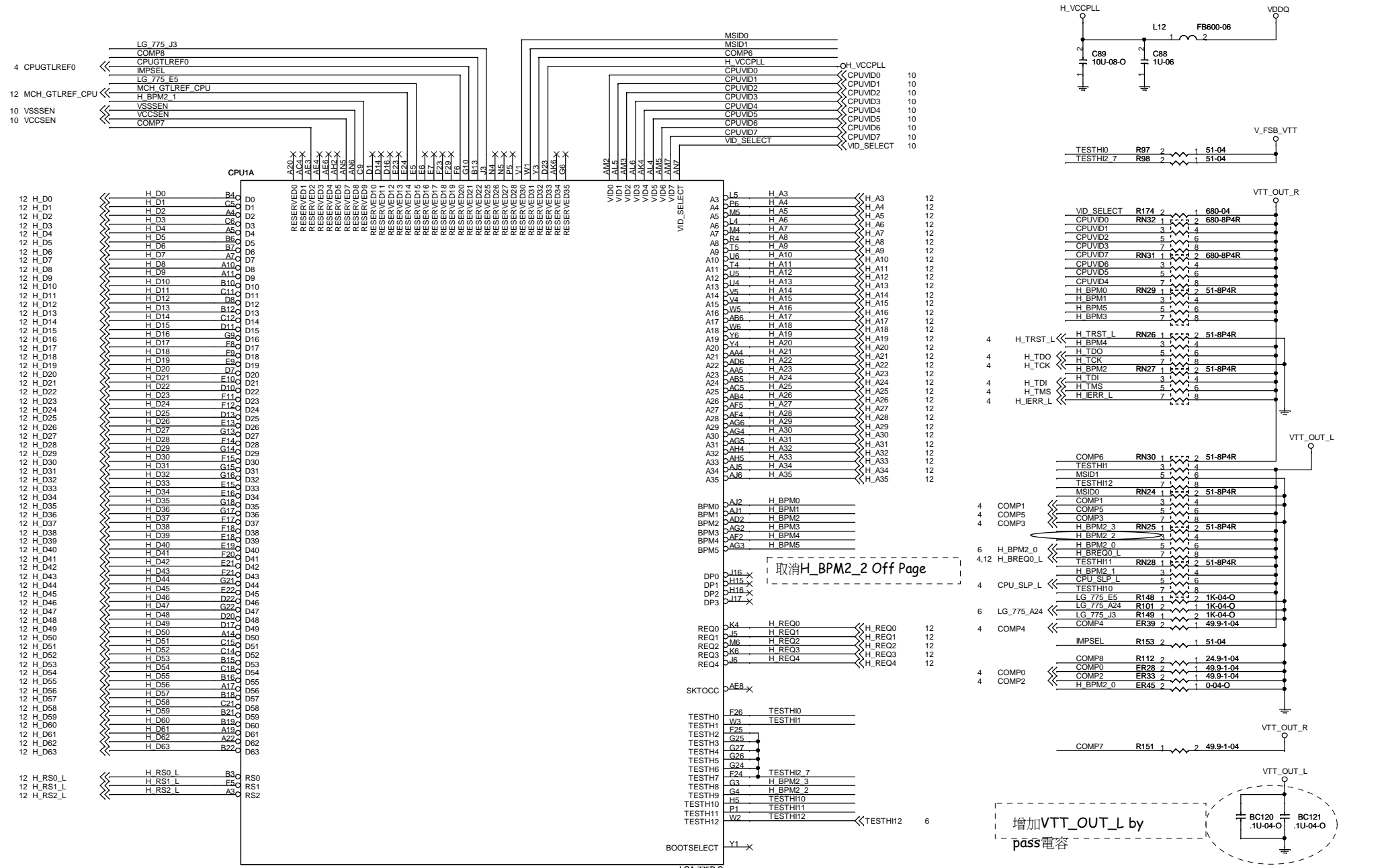


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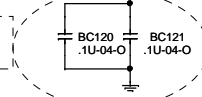
Title: **System Block Diagram**

Size: Document Number **G31T-M3** Rev **1.0**

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增加VTT_OUT_L by
pass電容



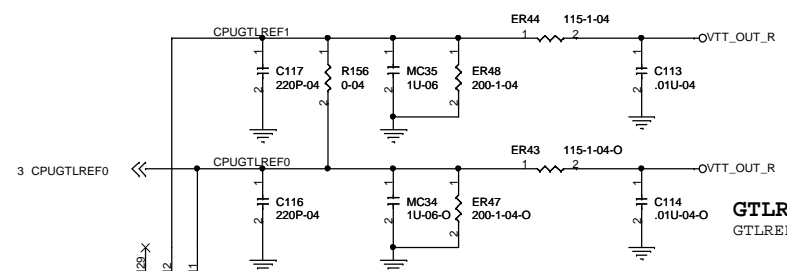
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Title: **P4 LGA775P Part A**

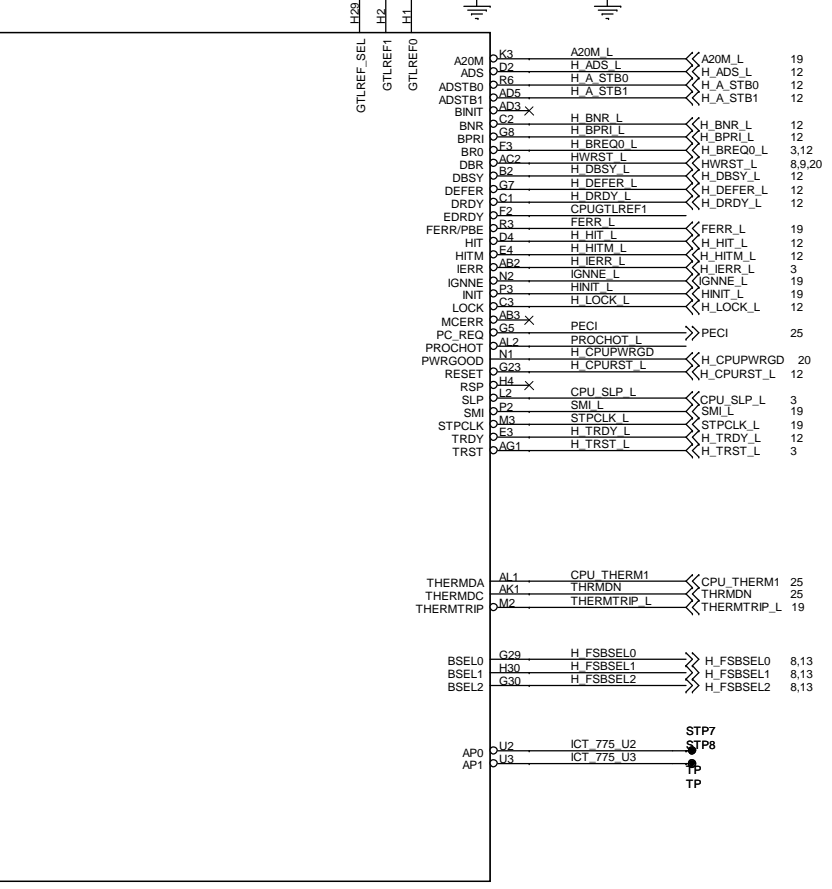
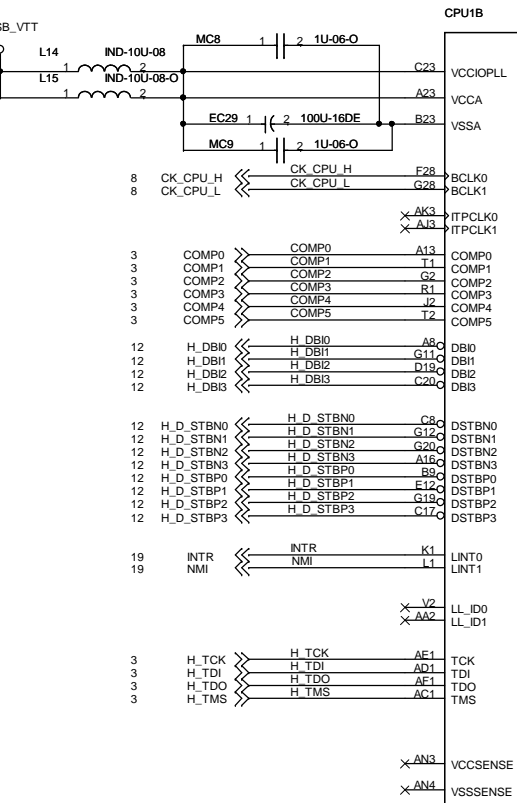
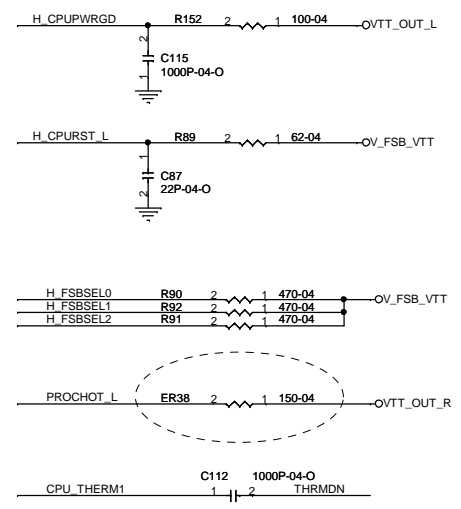
Size: Document Number **G3IT-M3** Rev **1.0**

Customer: **G3IT-M3**

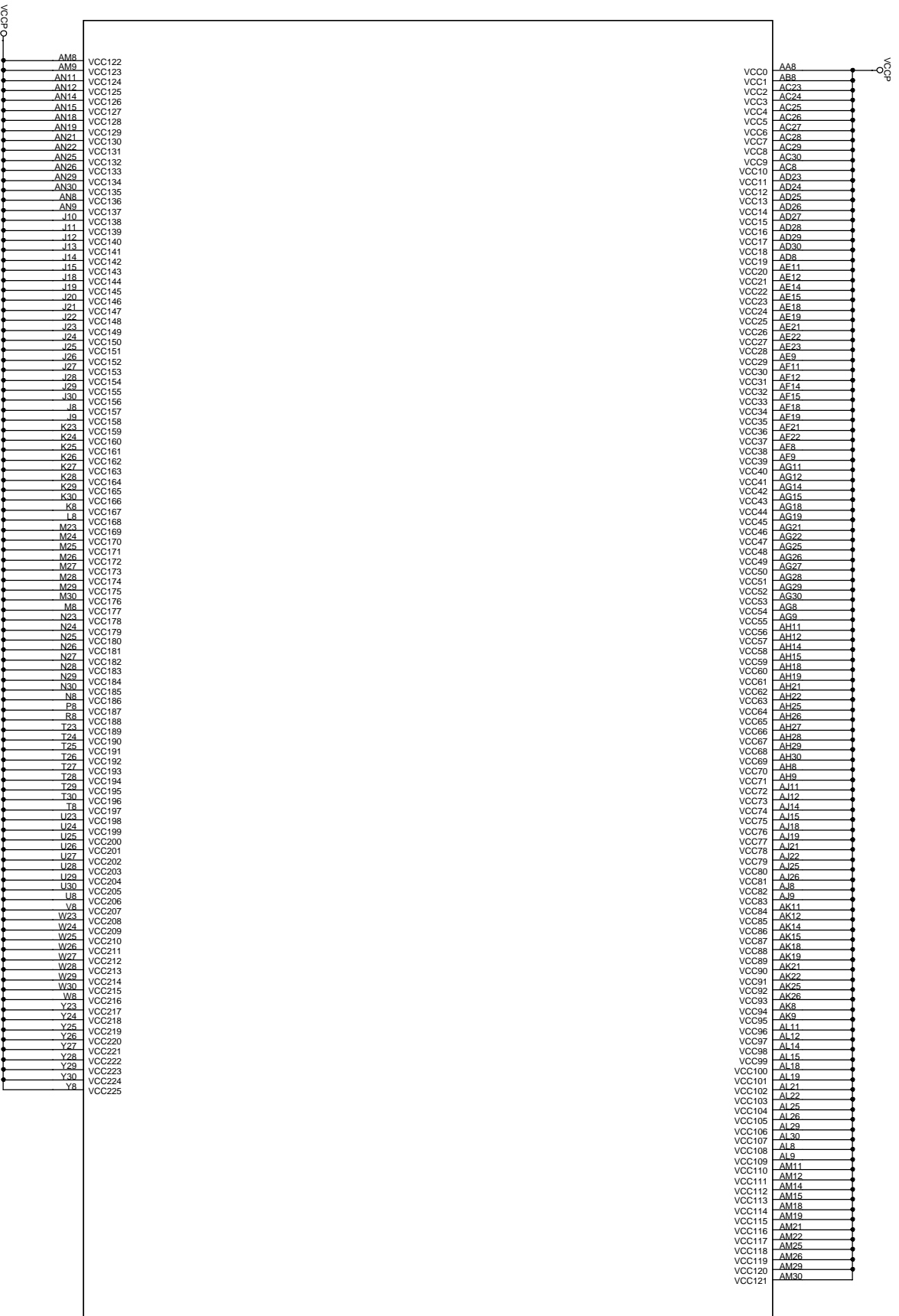
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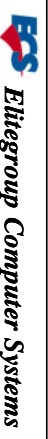
GTLREF = 0.63 * VTT = 0.76V
 GTLREF GENERATION CIRCUITS



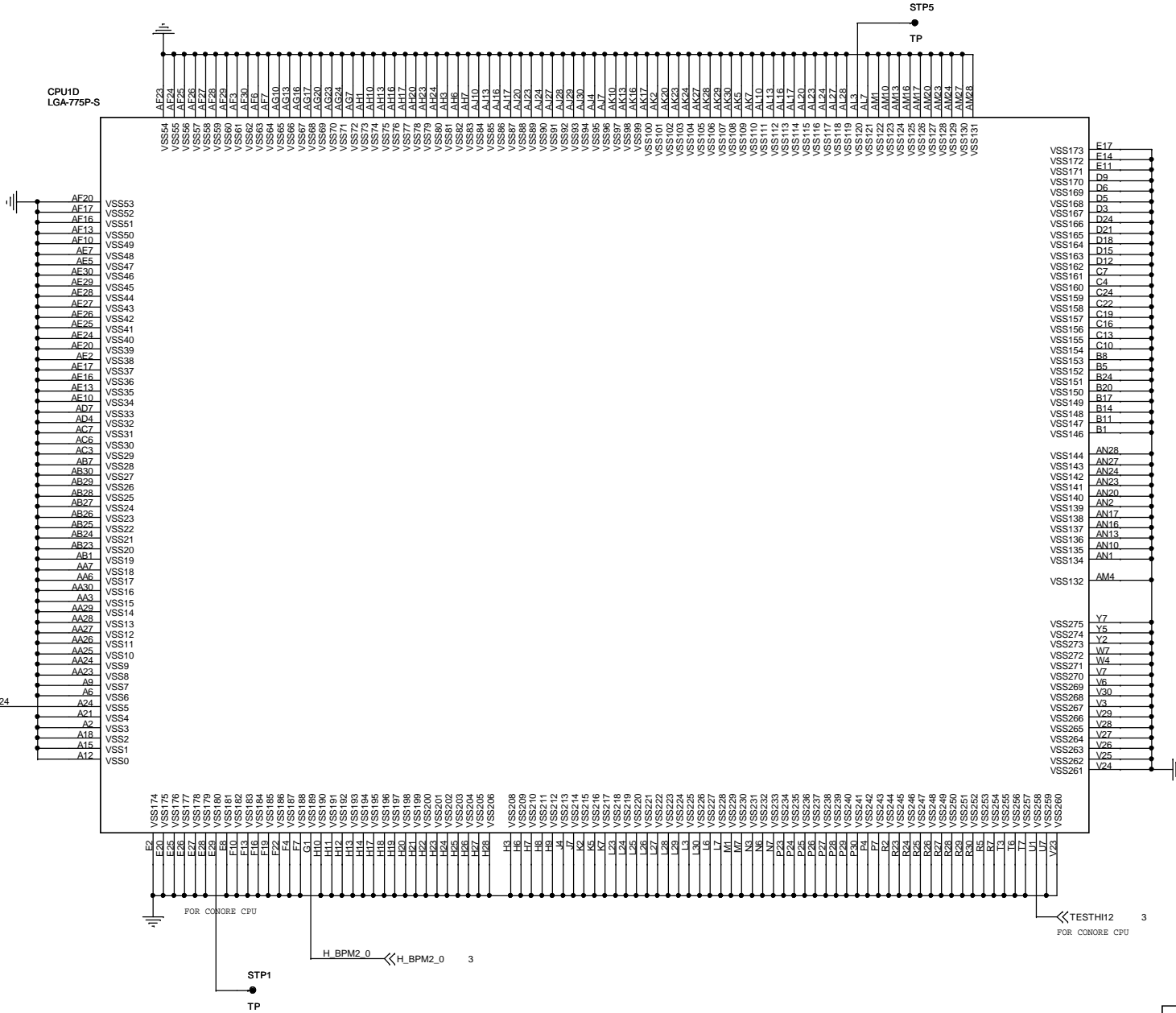
LGA-775P-S



CPU IC
LG4775-S



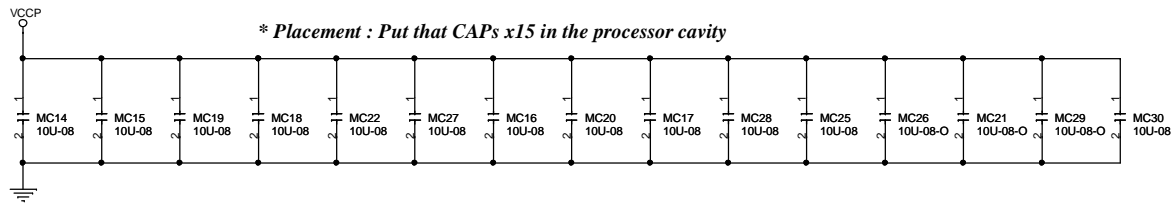
Title		P4 LG4775P Part C	
Size		Document Number	
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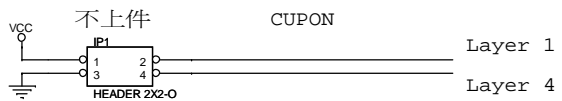
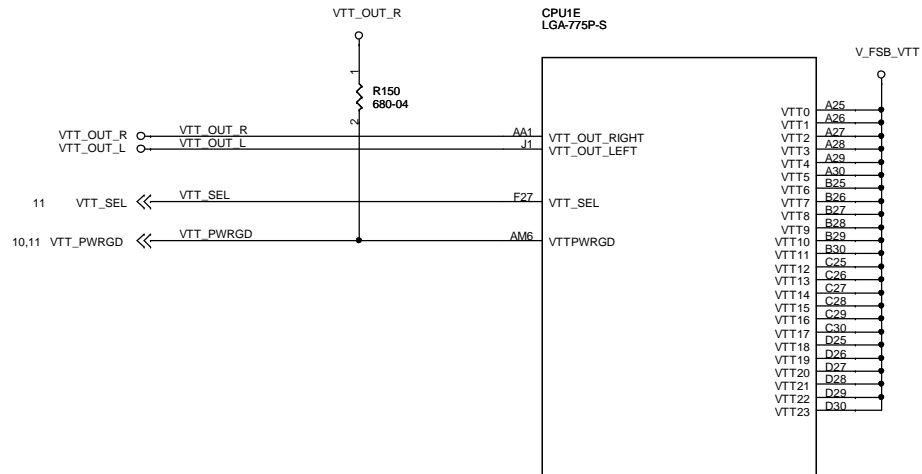
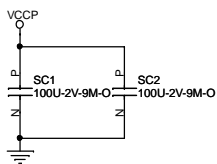
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Title: P4 LGA775P Part D

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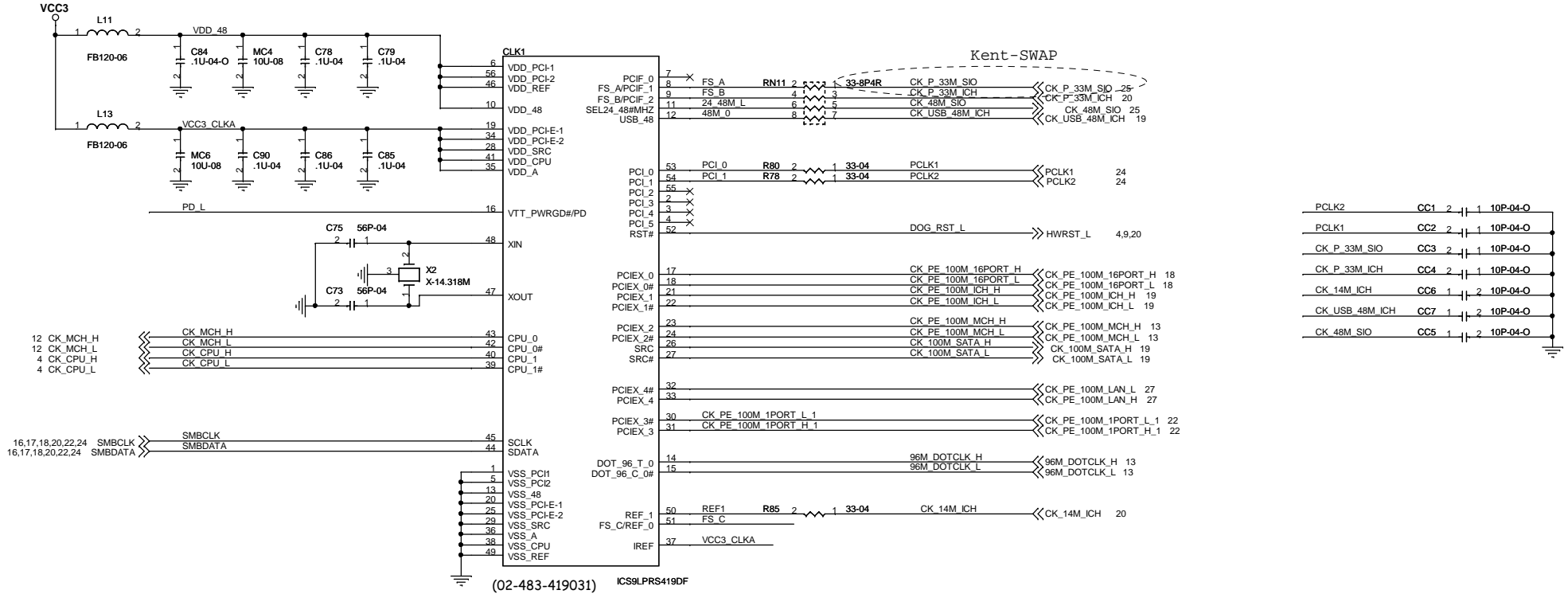
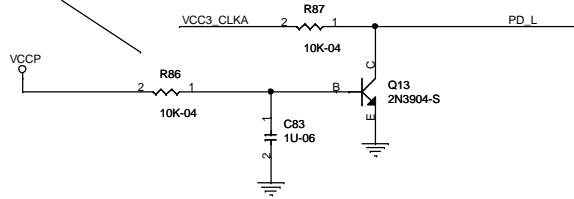


* Placement : Put that CAPs x2 on solder side



1080 : trace width 4 mil 50 ohm
 Trace Length 3150 mils
 Spacing: 1.clearance to itself 50/4/50(S:W:S)
 2.clearance to other signal 3W

Short(2-3) for VRM_PWRGD onto CONORE CPU timing



BSEL TABLE

2 1 0 FSB FREQUENCY

0 0 1	133 MHZ (533)
0 1 0	200 MHZ (800)
0 0 0	266 MHZ (1066)

FS_C	R84	2	1	10K-04	H	FSBSEL2	H_FSBSEL2	4,13
FS_B	R81	2	1	10K-04	H	FSBSEL1	H_FSBSEL1	4,13
FS_A	R82	2	1	10K-04	H	FSBSEL0	H_FSBSEL0	4,13

Swap PCIEX16 and SATA clock
Change ICH clk to pin 8

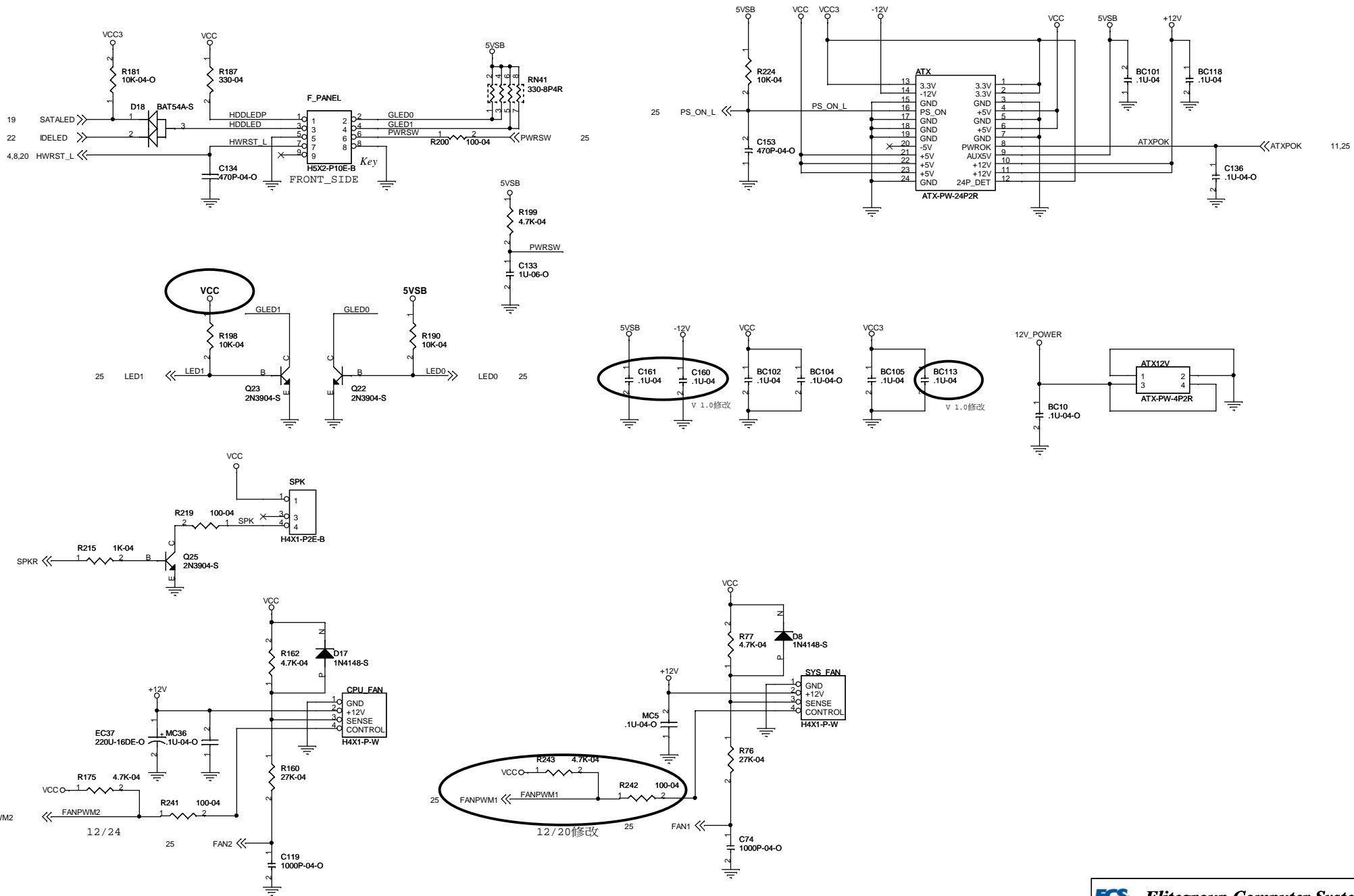
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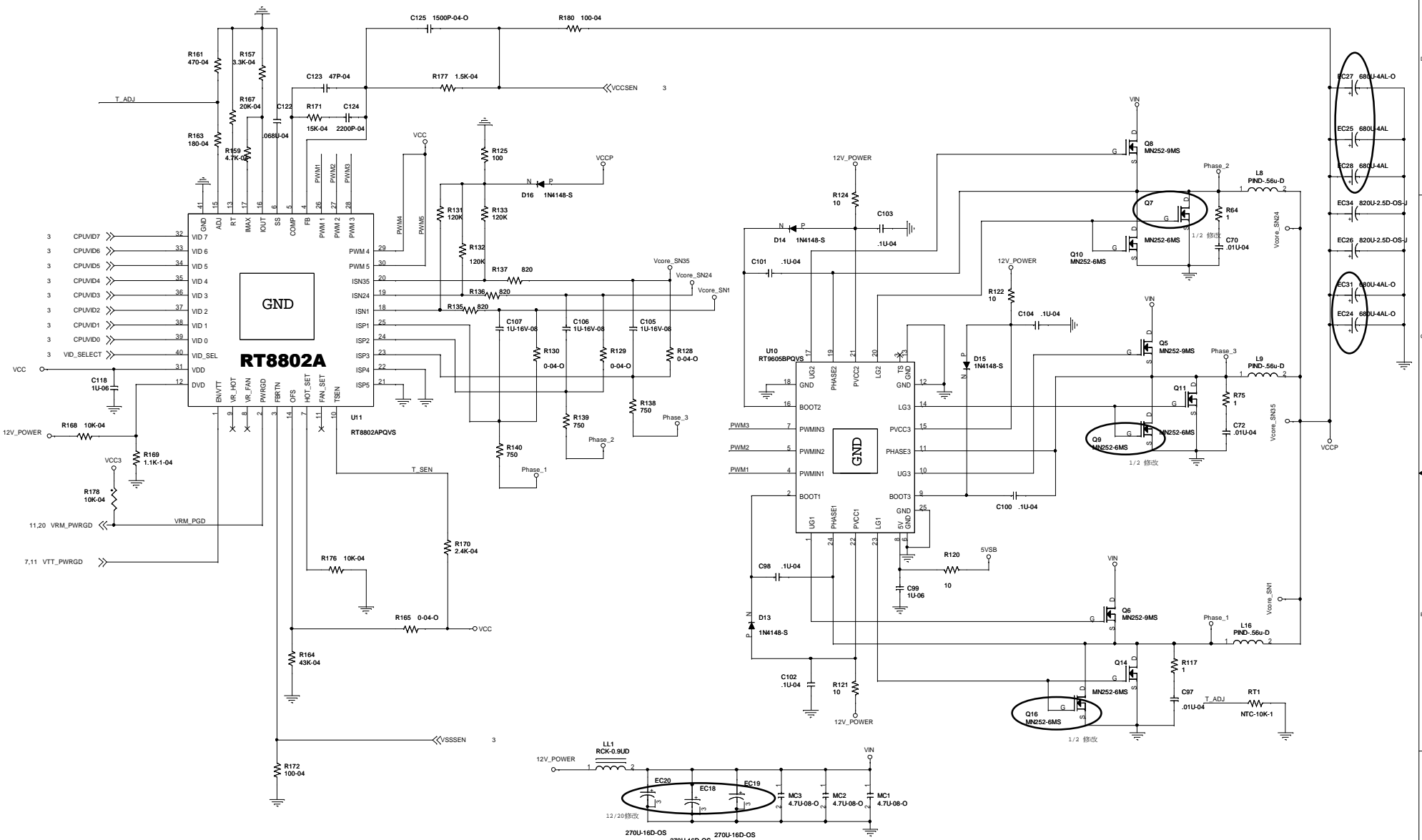
Title: **Clock Generator(CK410)**

Size: Document Number **G31T-M3** Rev: **1.0**

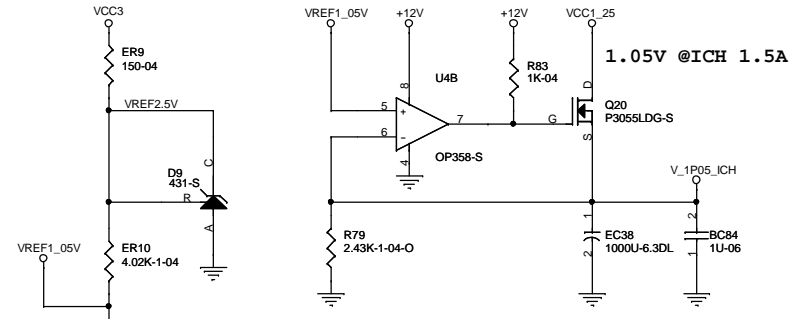
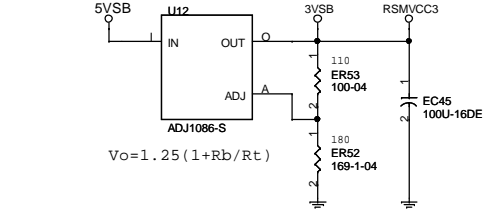
Customer: **G31T-M3**

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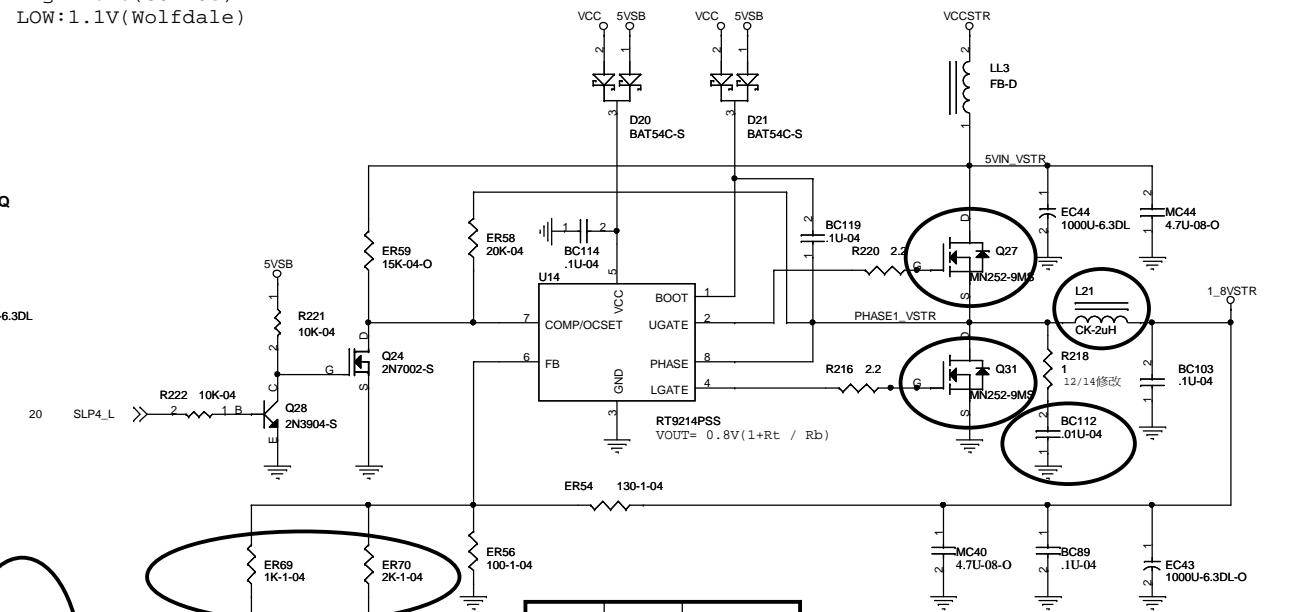
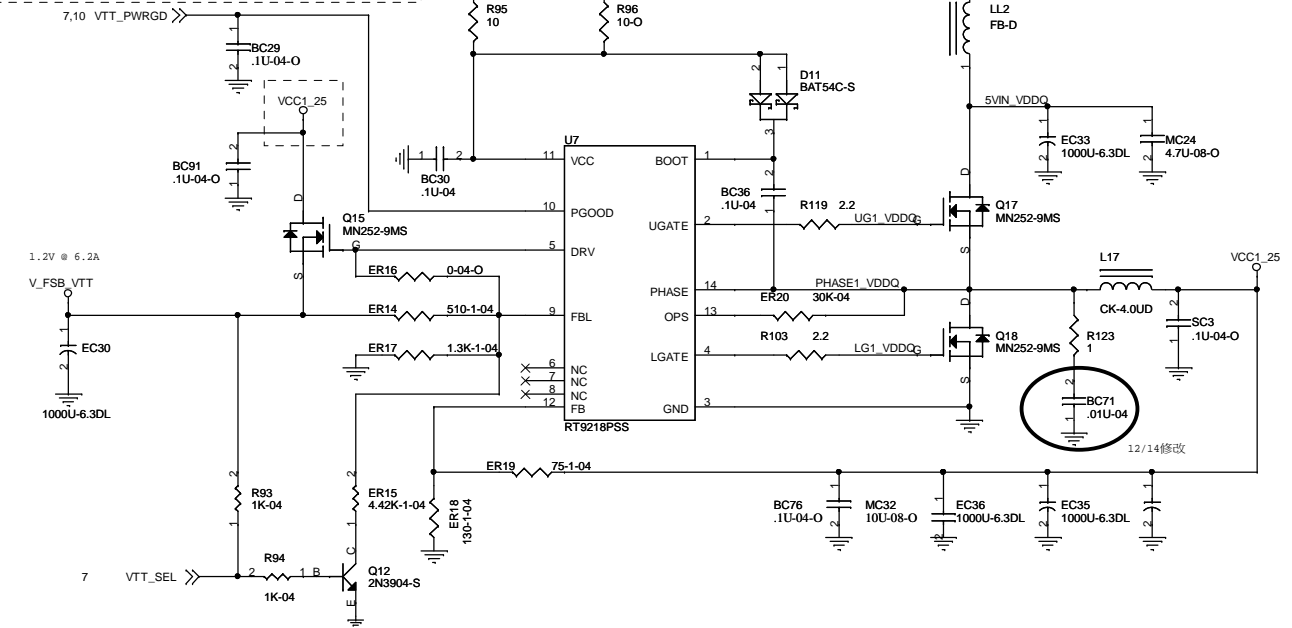
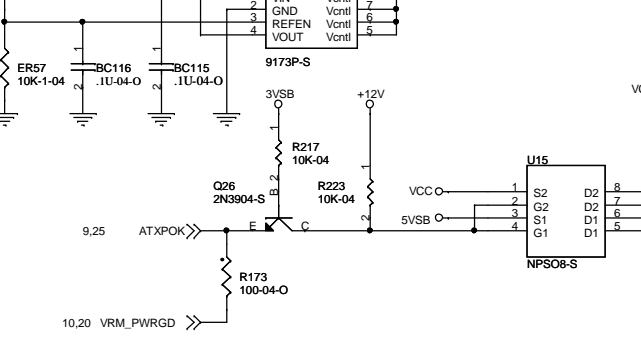
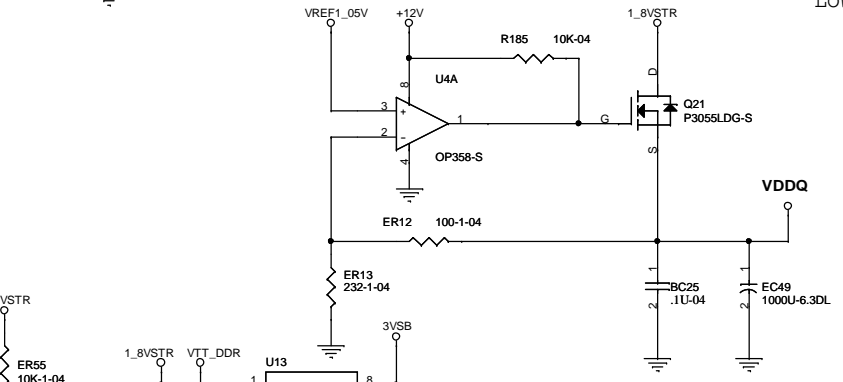


修改V_FSB_VTT電源從VCC1_25轉出
 Q15料號改成03-050-745282Rds(on)=8.5m ohm



(VDDQ 1.5V/1.8A)

High: 1.2V (Conroe)
 Low: 1.1V (Wolfdale)



GP41	GP10	1_8VSTR
1	1	1.85V
1	0	1.9V
0	1	1.95V
0	0	2.0V

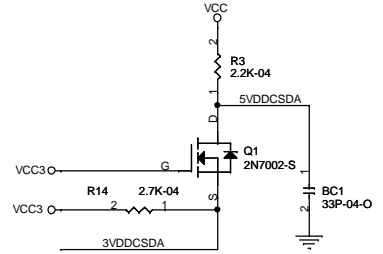
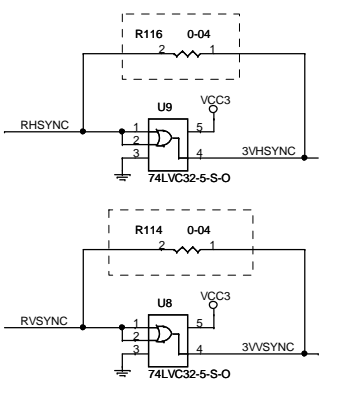
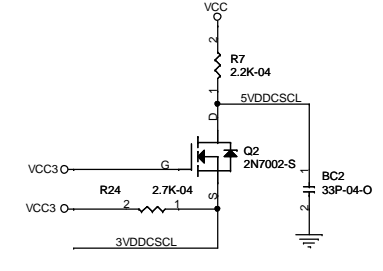
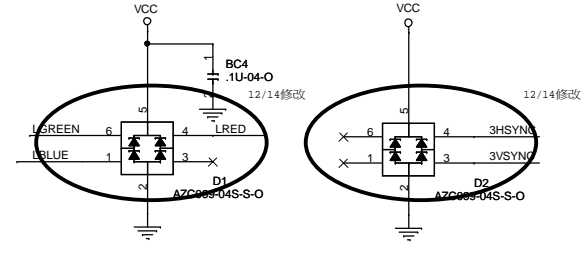
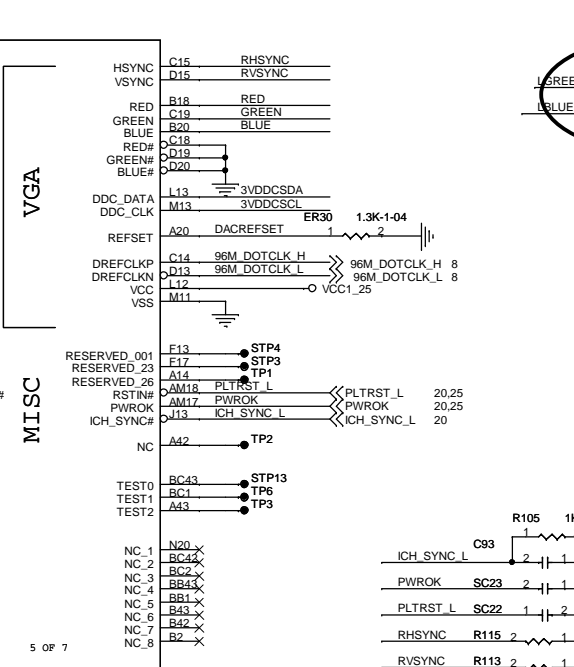
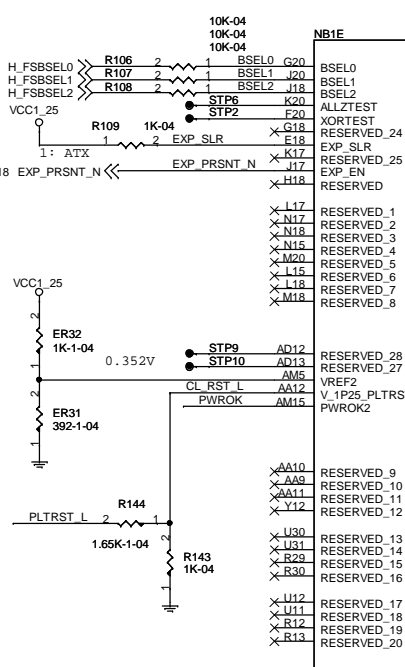
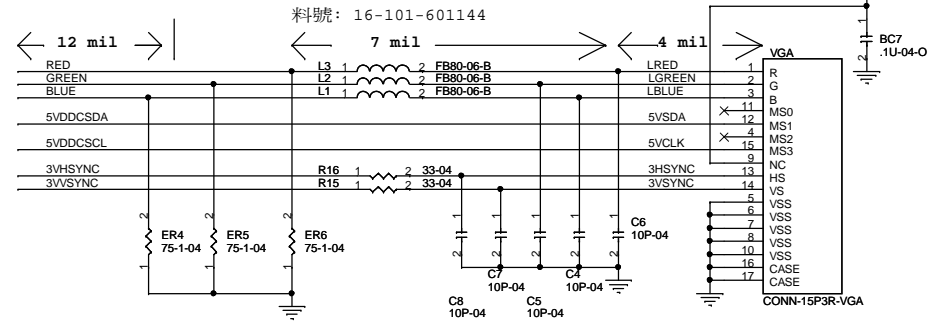
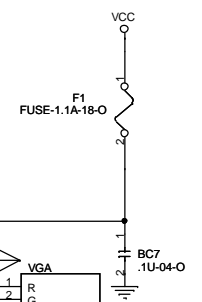
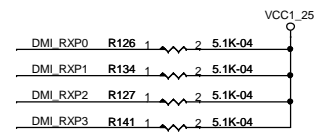
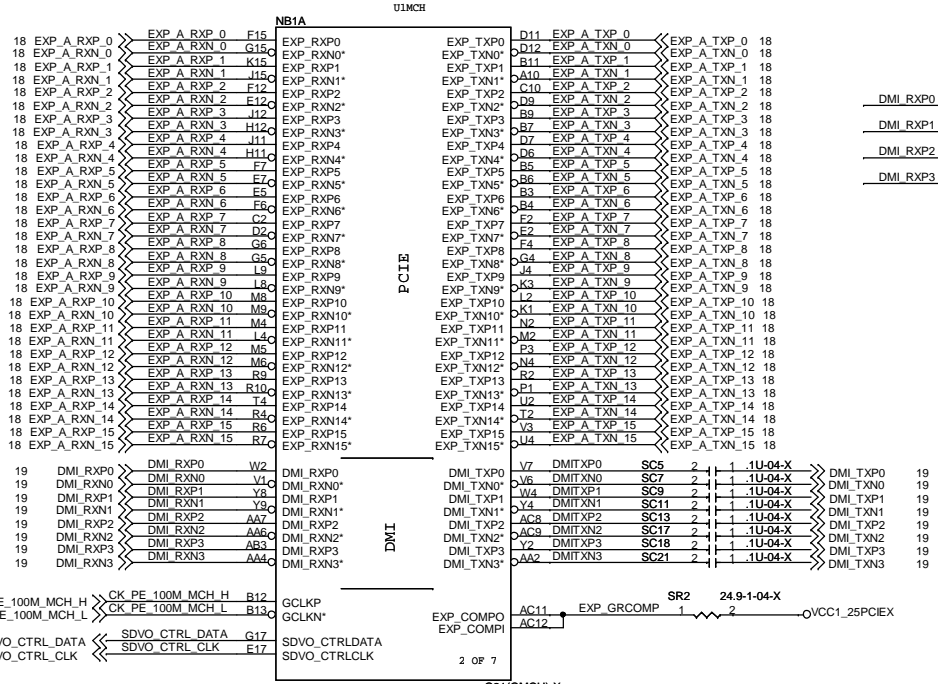
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Title: **MIS DC-DC**

Size: Document Number **G31T-M3** Rev 1.0

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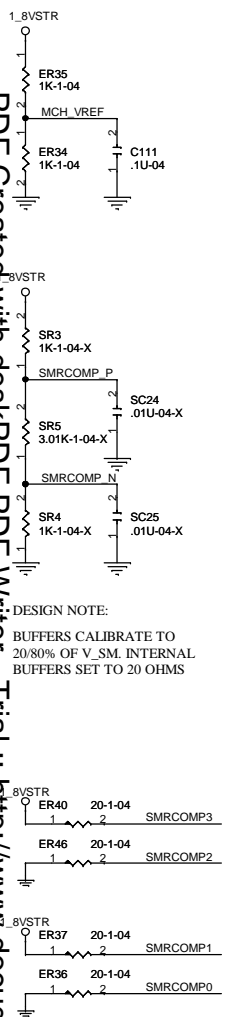


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Title: **G31(MCH) PCIE/DMI/VGA**

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DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_SM INTERNAL
BUFFERS SET TO 20 OHMS

NB1C		U1MCH		NB1D		U1MCH	
MAAA_0 BA31	SMA_A0	SDQS_A0	AU4 DOS H A0	MAAB_0 BB17	SMA_B0	SDQS_B0	AU6 DOS H B0
MAAA_1 BR25	SMA_A1	SDQS_A0#	AR3 DQS L_A0	MAAB_1 AY17	SMA_B1	SDQS_B0#	AU5 DQS L_B0
MAAA_2 BA26	SMA_A2	SDM_A0	AR2 MPD_A0	MAAB_2 BA17	SMA_B2	SDM_B0	AR7 MPD_B0
MAAA_3 BA25	SMA_A3			MAAB_3 BC16	SMA_B3		
MAAA_4 AY25	SMA_A4	SDQ_A0	AR5 MD A0	MAAB_4 AW15	SMA_B4	SDQ_B0	AN7 MD B0
MAAA_5 BA23	SMA_A5	SDQ_A1	AR4 MD A1	MAAB_5 BA15	SMA_B5	SDQ_B1	AN8 MD B1
MAAA_6 AY24	SMA_A6	SDQ_A2	AV3 MD A2	MAAB_6 BB15	SMA_B6	SDQ_B2	AW5 MD B2
MAAA_7 AY23	SMA_A7	SDQ_A3	AV2 MD A3	MAAB_7 BA14	SMA_B7	SDQ_B3	AW7 MD B3
MAAA_8 BR23	SMA_A8	SDQ_A4	AP3 MD A4	MAAB_8 AY15	SMA_B8	SDQ_B4	AN5 MD B4
MAAA_9 BA22	SMA_A9	SDQ_A5	AP2 MD A5	MAAB_9 BB14	SMA_B9	SDQ_B5	AN6 MD B5
MAAA_10 AY33	SMA_A10	SDQ_A6	AU1 MD A6	MAAB_10 AW18	SMA_B10	SDQ_B6	AN9 MD B6
MAAA_11 BR22	SMA_A11	SDQ_A7	AV4 MD A7	MAAB_11 BB13	SMA_B11	SDQ_B7	AU7 MD B7
MAAA_12 AW21	SMA_A12			MAAB_12 BA13	SMA_B12		
MAAA_13 AY38	SMA_A13	SDQS_A1	BB3 DOS H A1	MAAB_13 AY29	SMA_B13	SDQS_B1	AR12 DOS H B1
MAAA_14 BA21	SMA_A14	SDQS_A1#	BA4 DQS L_A1	MAAB_14 AY13	SMA_B14	SDQS_B1#	AR12 DQS L_B1
		SDM_A1	BA2 MPD_A1			SDM_B1	AW9 MPD_B1
SWE_L A BR34C	SWE_A#			SWE_L B BA27C	SWE_B#		
SCAS_L A AY35C	SCAS_A#	SDQ_A8	AY2 MD A8	SCAS_L B AW29C	SCAS_B#	SDQ_B8	AT11 MD B8
SRAS_L A BR33C	SRAS_A#	SDQ_A9	AY3 MD A9	SRAS_L B AW26C	SRAS_B#	SDQ_B9	AU11 MD B9
		SDQ_A10	BB5 MD A10			SDQ_B10	AP13 MD B10
SBSA_0 BA33	SBS_A0	SDQ_A11	AY6 MD A11	SBSB_0 AY19	SBS_B0	SDQ_B11	AR13 MD B11
SBSA_1 AW32	SBS_A1	SDQ_A12	AW2 MD A12	SBSB_1 BA18	SBS_B1	SDQ_B12	AR11 MD B12
SBSA_2 BR21	SBS_A2	SDQ_A13	AW3 MD A13	SBSB_2 BC12	SBS_B2	SDQ_B13	AU9 MD B13
		SDQ_A14	BA5 MD A14			SDQ_B14	AV12 MD B14
CSA_L0 AW35C	SCS_A0#	SDQ_A15	BB4 MD A15	CSB_L0 BB27C	SCS_B0#	SDQ_B15	AU12 MD B15
CSA_L1 BA35C	SCS_A1#			CSB_L1 BR27C	SCS_B1#		
	RESERVED_11	SDQS_A2	BB9 DOS H A2		RESERVED_13	SDQS_B2	AP15 DOS H B2
	RESERVED_12	SDQS_A2#	BA9 DQS L_A2		RESERVED_10	SDQS_B2#	AR15 DQS L_B2
		SDM_A2	AY9 MPD_A2			SDM_B2	AW13 MPD_B2
CKEA_0 BC20	SCKE_A0	SDQ_A16	AY7 MD A16	CKEB_0 AY12	SCKE_B0	SDQ_B16	AU15 MD B16
CKEA_1 AY20	SCKE_A1	SDQ_A17	BC7 MD A17	CKEB_1 AW12	SCKE_B1	SDQ_B17	AU13 MD B17
	RESERVED_9	SDQ_A18	AW11 MD A18		RESERVED_11	SDQ_B18	AU17 MD B18
	RESERVED_10	SDQ_A19	AY11 MD A19	ODTB_0 BA11	RESERVED_12	SDQ_B19	AT17 MD B19
ODTA_0 AY37	SODT_A0	SDQ_A20	BB6 MD A20	ODTB_1 BA29	SODT_B0	SDQ_B20	AU13 MD B20
ODTA_1 BA38	SODT_A1	SDQ_A21	BA6 MD A21	ODTB_0 BA29	SODT_B1	SDQ_B21	AM13 MD B21
	RESERVED_2	SDQ_A22	BA10 MD A22	ODTB_1 BA30	RESERVED_14	SDQ_B22	AV15 MD B22
	RESERVED_1	SDQ_A23	BB10 MD A23	BB31	RESERVED_15	SDQ_B23	AW17 MD B23
DCLKA_H0 AU31	SCLK_A0#	SDQS_A3	AT20 DQS H A3	DCLKB_H0 AV31	SCLK_B0	SDQS_B3	AT24 DQS H B3
DCLKA_L0 AR31C	SCLK_A0#	SDQS_A3#	AU18 DQS L_A3	DCLKB_L0 AW31C	SCLK_B0#	SDQS_B3#	AU26 DQS L_B3
DCLKA_H1 AP27	SCLK_A1	SDM_A3	AN18 MPD_A3	DCLKB_L1 AT27C	SCLK_B1	SDM_B3	AP23 MPD_B3
DCLKA_L1 AN27C	SCLK_A1#			DCLKB_H2 AV32	SCLK_B1#		
DCLKA_H2 AV33C	SCLK_A2	SDQ_A24	AT18 MD A24	DCLKB_L2 AW32	SCLK_B2	SDQ_B24	AV24 MD B24
DCLKA_L2 AW33C	SCLK_A2#	SDQ_A25	AR18 MD A25		SCLK_B2#	SDQ_B25	AT23 MD B25
AP29	RESERVED_3	SDQ_A26	AU21 MD A26	AU29	RESERVED_16	SDQ_B26	AT26 MD B26
AP31C	RESERVED_4	SDQ_A27	AT21 MD A27	AR29C	RESERVED_17	SDQ_B27	AP26 MD B27
AM26	RESERVED_5	SDQ_A28	AP17 MD A28	AV29	RESERVED_18	SDQ_B28	AW23 MD B28
AM27C	RESERVED_6	SDQ_A29	AN17 MD A29	AW27	RESERVED_19	SDQ_B29	AW23 MD B29
AT33	RESERVED_7	SDQ_A30	AP20 MD A30	AN33	RESERVED_20	SDQ_B30	AR24 MD B30
AU33C	RESERVED_8	SDQ_A31	AV20 MD A31	AP32	RESERVED_21	SDQ_B31	AN26 MD B31
SDQS_A4	AR41 DOS H A4						
SDQS_A4#	AR40 DQS L_A4						
SDM_A4	AU43 MPD_A4						
		SDQ_A32	AV42 MD A32				
		SDQ_A33	AU40 MD A33				
		SDQ_A34	AP42 MD A34				
		SDQ_A35	AN39 MD A35				
		SDQ_A36	AV40 MD A36				
		SDQ_A37	AV41 MD A37				
		SDQ_A38	AR42 MD A38				
		SDQ_A39	AP41 MD A39				
SDQS_A5	AL41 DOS H A5						
SDQS_A5#	AL40 DQS L_A5						
SDM_A5	AM43 MPD_A5						
		SDQ_A40	AN41 MD A40				
		SDQ_A41	AM39 MD A41				
		SDQ_A42	AK42 MD A42				
		SDQ_A43	AK41 MD A43				
		SDQ_A44	AN40 MD A44				
		SDQ_A45	AN42 MD A45				
		SDQ_A46	AL42 MD A46				
		SDQ_A47	AL39 MD A47				
SDQS_A6	AG42 DOS H A6						
SDQS_A6#	AG41 DQS L_A6						
SDM_A6	AG40 MPD_A6						
		SDQ_A48	AJ40 MD A48				
		SDQ_A49	AH43 MD A49				
		SDQ_A50	AF39 MD A50				
		SDQ_A51	AE40 MD A51				
		SDQ_A52	AJ42 MD A52				
		SDQ_A53	AJ41 MD A53				
		SDQ_A54	AF41 MD A54				
		SDQ_A55	AF42 MD A55				
SDQS_A7	AC42 DOS H A7						
SDQS_A7#	AC41 DQS L_A7						
SDM_A7	AC40 MPD_A7						
		SDQ_A56	AD40 MD A56				
		SDQ_A57	AD43 MD A57				
		SDQ_A58	AR41 MD A58				
		SDQ_A59	AA40 MD A59				
		SDQ_A60	AE42 MD A60				
		SDQ_A61	AE41 MD A61				
		SDQ_A62	AC39 MD A62				
		SDQ_A63	AB42 MD A63				

DDR_0

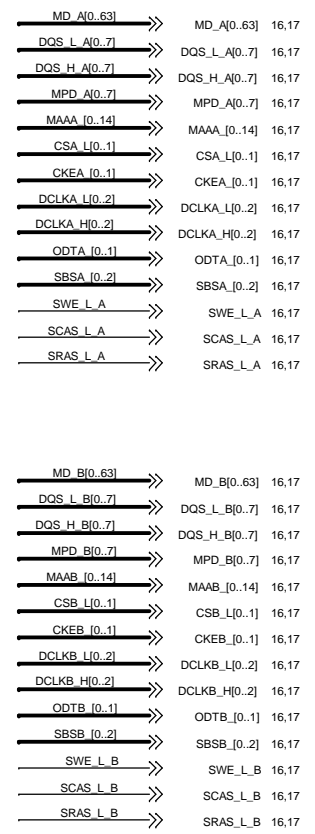
AN21G RESERVED

G31(GMCH)-X

NB1D		U1MCH	
MAAB_0 BB17	SMA_B0	SDQS_B0	AU6 DOS H B0
MAAB_1 AY17	SMA_B1	SDQS_B0#	AU5 DQS L_B0
MAAB_2 BA17	SMA_B2	SDM_B0	AR7 MPD_B0
MAAB_3 BC16	SMA_B3		
MAAB_4 AW15	SMA_B4	SDQ_B0	AN7 MD B0
MAAB_5 BA15	SMA_B5	SDQ_B1	AN8 MD B1
MAAB_6 BB15	SMA_B6	SDQ_B2	AW5 MD B2
MAAB_7 BA14	SMA_B7	SDQ_B3	AW7 MD B3
MAAB_8 AY15	SMA_B8	SDQ_B4	AN5 MD B4
MAAB_9 BB14	SMA_B9	SDQ_B5	AN6 MD B5
MAAB_10 AW18	SMA_B10	SDQ_B6	AN9 MD B6
MAAB_11 BB13	SMA_B11	SDQ_B7	AU7 MD B7
MAAB_12 BA13	SMA_B12		
MAAB_13 AY29	SMA_B13	SDQS_B1	AR12 DOS H B1
MAAB_14 AY13	SMA_B14	SDQS_B1#	AR12 DQS L_B1
		SDM_B1	AW9 MPD_B1
SWE_L B BA27C	SWE_B#		
SCAS_L B AW29C	SCAS_B#	SDQ_B8	AT11 MD B8
SRAS_L B AW26C	SRAS_B#	SDQ_B9	AU11 MD B9
		SDQ_B10	AP13 MD B10
SBSB_0 AY19	SBS_B0	SDQ_B11	AR13 MD B11
SBSB_1 BA18	SBS_B1	SDQ_B12	AR11 MD B12
SBSB_2 BC12	SBS_B2	SDQ_B13	AU9 MD B13
		SDQ_B14	AV12 MD B14
		SDQ_B15	AU12 MD B15
CSB_L0 BB27C	SCS_B0#		
CSB_L1 BR27C	SCS_B1#	SDQS_B2	AP15 DOS H B2
	RESERVED_13	SDQS_B2#	AR15 DQS L_B2
	RESERVED_10	SDM_B2	AW13 MPD_B2
CKEB_0 AY12	SCKE_B0	SDQ_B16	AU15 MD B16
CKEB_1 AW12	SCKE_B1	SDQ_B17	AU13 MD B17
	RESERVED_11	SDQ_B18	AU17 MD B18
ODTB_0 BA11	RESERVED_12	SDQ_B19	AT17 MD B19
ODTB_1 BA29	SODT_B0	SDQ_B20	AU13 MD B20
	SODT_B1	SDQ_B21	AM13 MD B21
	RESERVED_14	SDQ_B22	AV15 MD B22
	RESERVED_15	SDQ_B23	AW17 MD B23
DCLKB_H0 AV31	SCLK_B0	SDQS_B3	AT24 DQS H B3
DCLKB_L0 AW31C	SCLK_B0#	SDQS_B3#	AU26 DQS L_B3
DCLKB_H1 AU27	SCLK_B1	SDM_B3	AP23 MPD_B3
DCLKB_L1 AT27C	SCLK_B1#		
DCLKB_H2 AV32	SCLK_B2	SDQ_B24	AV24 MD B24
DCLKB_L2 AW32	SCLK_B2#	SDQ_B25	AT23 MD B25
	RESERVED_16	SDQ_B26	AT26 MD B26
AU29	RESERVED_17	SDQ_B27	AP26 MD B27
AR29C	RESERVED_18	SDQ_B28	AW23 MD B28
AV29	RESERVED_19	SDQ_B29	AW23 MD B29
AW27	RESERVED_20	SDQ_B30	AR24 MD B30
AN33	RESERVED_21	SDQ_B31	AN26 MD B31
AP32			
		SDQS_B4	AW39 DOS H B4
		SDQS_B4#	AU39 DQS L_B4
		SDM_B4	AL37 MPD_B4
		SDQ_B32	AW37 MD B32
		SDQ_B33	AV38 MD B33
		SDQ_B34	AN36 MD B34
		SDQ_B35	AN37 MD B35
		SDQ_B36	AL35 MD B36
		SDQ_B37	AR35 MD B37
		SDQ_B38	AN35 MD B38
		SDQ_B39	AR37 MD B39
		SDQS_B5	AL35 DOS H B5
		SDQS_B5#	AL34 DQS L_B5
		SDM_B5	AM37 MPD_B5
		SDQ_B40	AM35 MD B40
		SDQ_B41	AM38 MD B41
		SDQ_B42	AL34 MD B42
		SDQ_B43	AL38 MD B43
		SDQ_B44	AR39 MD B44
		SDQ_B45	AM34 MD B45
		SDQ_B46	AL37 MD B46
		SDQ_B47	AL32 MD B47
		SDQS_B6	AG35 DOS H B6
		SDQS_B6#	AG36 DQS L_B6
		SDM_B6	AG39 MPD_B6
		SDQ_B48	AG38 MD B48
		SDQ_B49	AJ38 MD B49
		SDQ_B50	AF35 MD B50
		SDQ_B51	AF33 MD B51
		SDQ_B52	AJ37 MD B52
		SDQ_B53	AL35 MD B53
		SDQ_B54	AG33 MD B54
		SDQ_B55	AF34 MD B55
		SDQS_B7	AC36 DOS H B7
		SDQS_B7#	AC37 DQS L_B7
		SDM_B7	AD38 MPD_B7
		SDQ_B56	AD36 MD B56
		SDQ_B57	AC33 MD B57
		SDQ_B58	AA34 MD B58
		SDQ_B59	AA36 MD B59
		SDQ_B60	AD34 MD B60
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DDR_1

G31(GMCH)-X



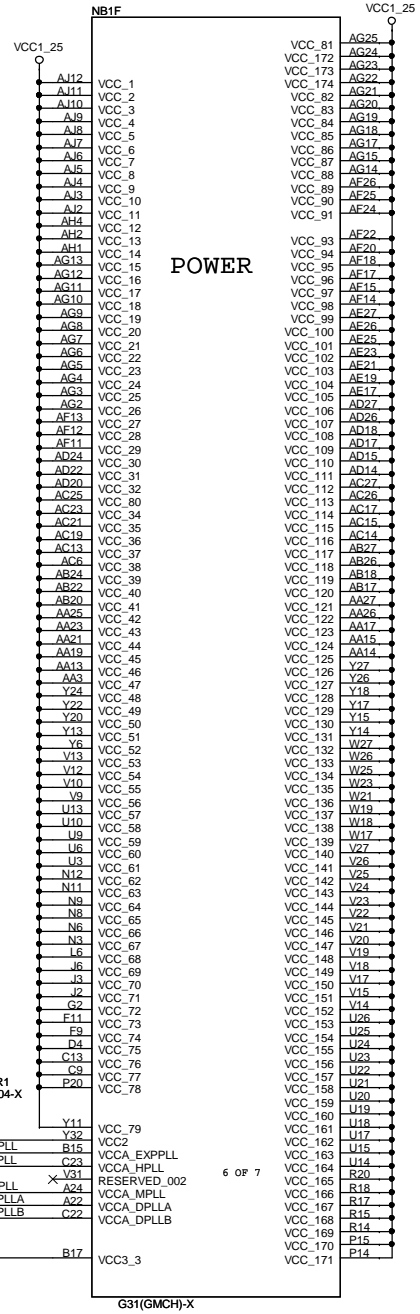
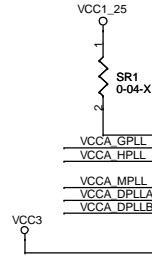
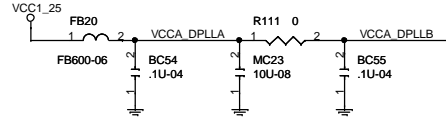
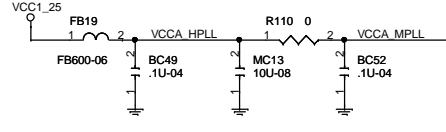
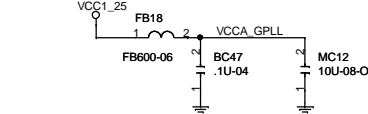
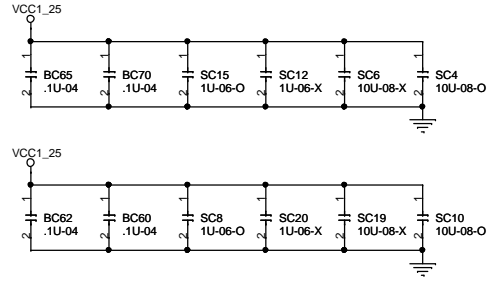
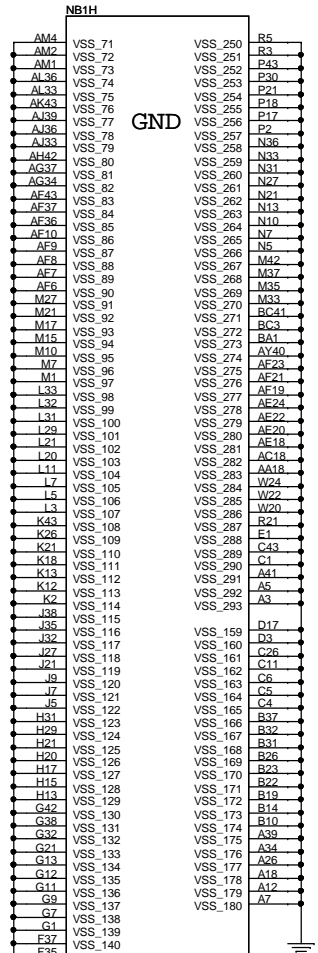
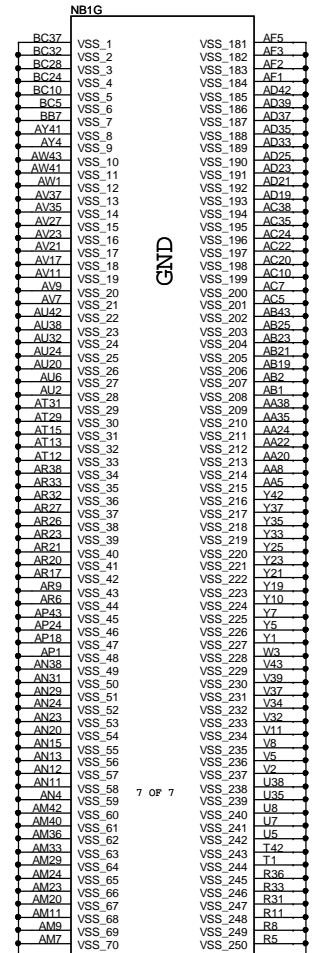
Elitegroup Computer Systems

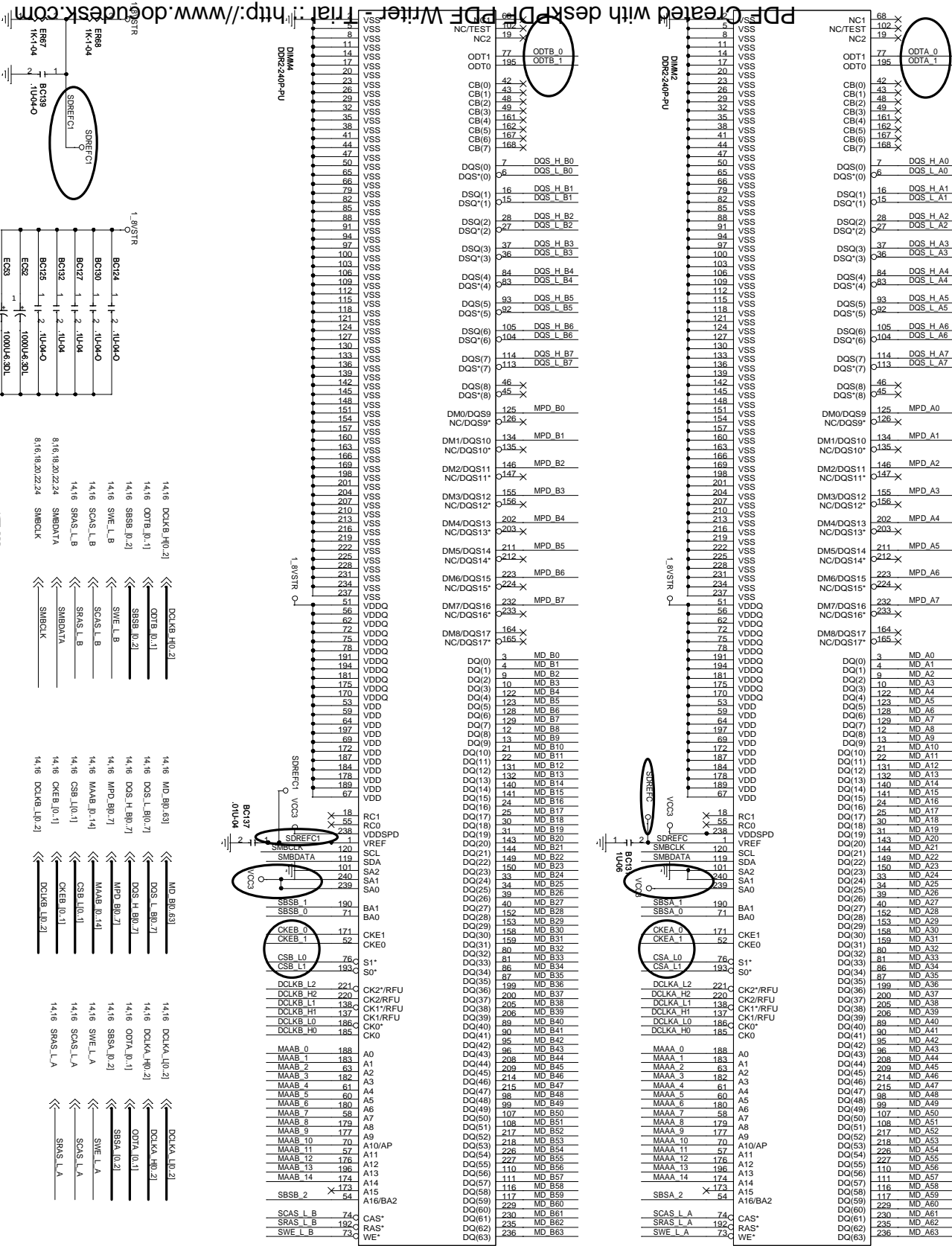
G31(MCH) MEMORY

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Size: Document Number **G31-M3** Rev: 1.0

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1416 MD_0(A0_0)	MD_0(A0_0)
1416 DQS_L_0(A0_1)	DQCKA_H0_2
1416 DQS_H_0(A0_7)	DQCKA_H0_2
1416 DQS_L_0(A0_7)	DQCKA_H0_2
1416 DQS_H_0(A0_7)	DQCKA_H0_2
1416 MPD_0(A0_7)	DQCKA_H0_2
1416 MAAB_0(A1)	DQCKA_H0_2
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1416 MAAB_4(A4)	DQCKA_H0_2
1416 MAAB_5(A5)	DQCKA_H0_2
1416 MAAB_6(A6)	DQCKA_H0_2
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1416 CKEA_15(A16)	DQCKA_H0_2
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1416 SRAS_L_B	RAS*
1416 SWE_L_B	WE*

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DDIMM 3&4 (DDR SDRAMs)

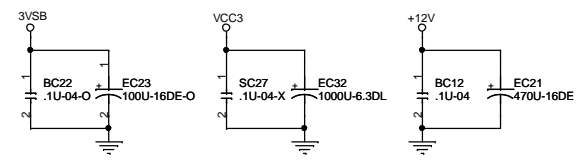
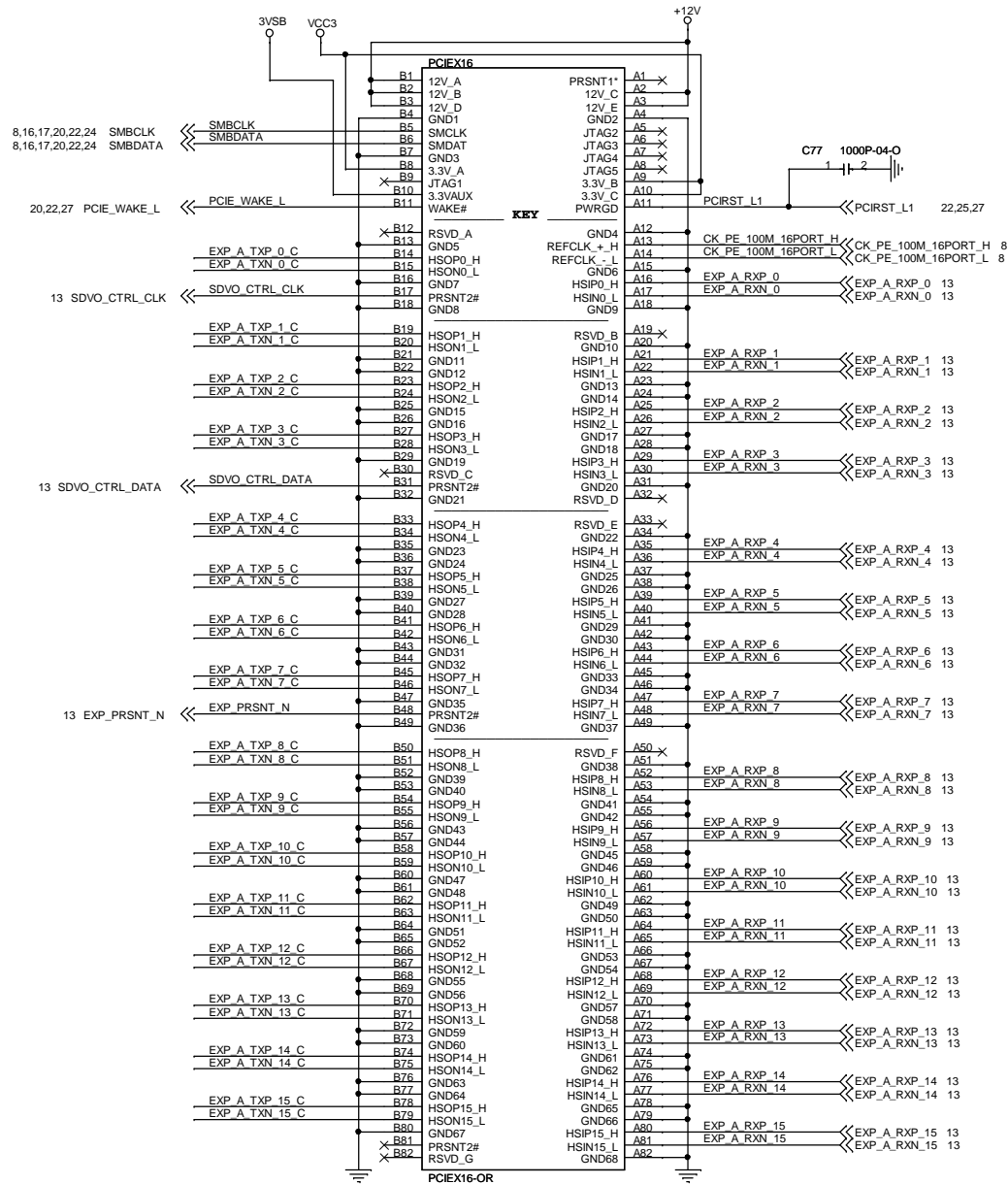
Document Number: **G31T-M3**

Version: February 20, 2008

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http://www.docudesk.com



EXP A TXP 0 C	BC28	1	2	.1U-04	EXP A TXP 0	EXP A TXP 0	13
EXP A TXN 0 C	BC27	1	2	.1U-04	EXP A TXN 0	EXP A TXN 0	13
EXP A TXP 1 C	BC31	1	2	.1U-04	EXP A TXP 1	EXP A TXP 1	13
EXP A TXN 1 C	BC32	1	2	.1U-04	EXP A TXN 1	EXP A TXN 1	13
EXP A TXP 2 C	BC33	1	2	.1U-04	EXP A TXP 2	EXP A TXP 2	13
EXP A TXN 2 C	BC34	1	2	.1U-04	EXP A TXN 2	EXP A TXN 2	13
EXP A TXP 3 C	BC35	1	2	.1U-04	EXP A TXP 3	EXP A TXP 3	13
EXP A TXN 3 C	BC37	1	2	.1U-04	EXP A TXN 3	EXP A TXN 3	13
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EXP A TXN 8 C	BC58	1	2	.1U-04	EXP A TXN 8	EXP A TXN 8	13
EXP A TXP 9 C	BC59	1	2	.1U-04	EXP A TXP 9	EXP A TXP 9	13
EXP A TXN 9 C	BC61	1	2	.1U-04	EXP A TXN 9	EXP A TXN 9	13
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EXP A TXN 13 C	BC72	1	2	.1U-04	EXP A TXN 13	EXP A TXN 13	13
EXP A TXP 14 C	BC75	1	2	.1U-04	EXP A TXP 14	EXP A TXP 14	13
EXP A TXN 14 C	BC74	1	2	.1U-04	EXP A TXN 14	EXP A TXN 14	13
EXP A TXP 15 C	BC78	1	2	.1U-04	EXP A TXP 15	EXP A TXP 15	13
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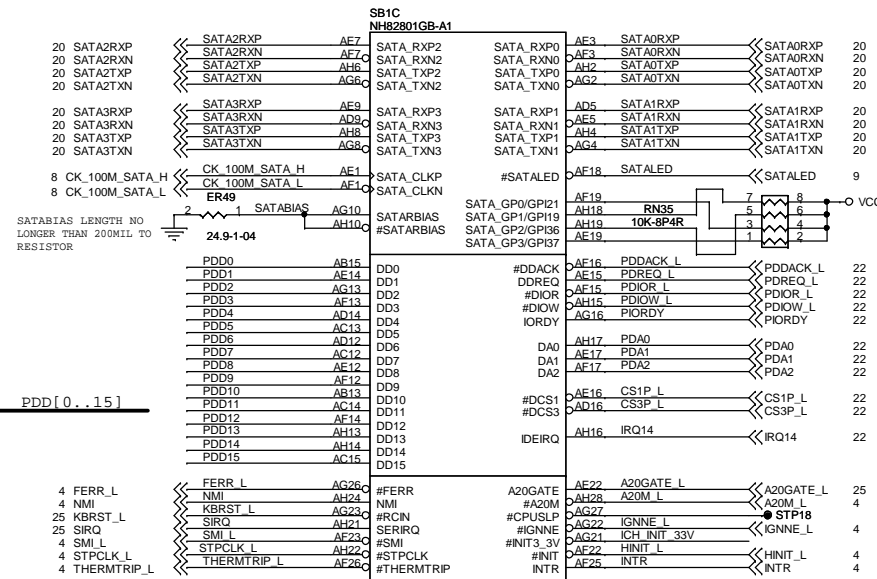
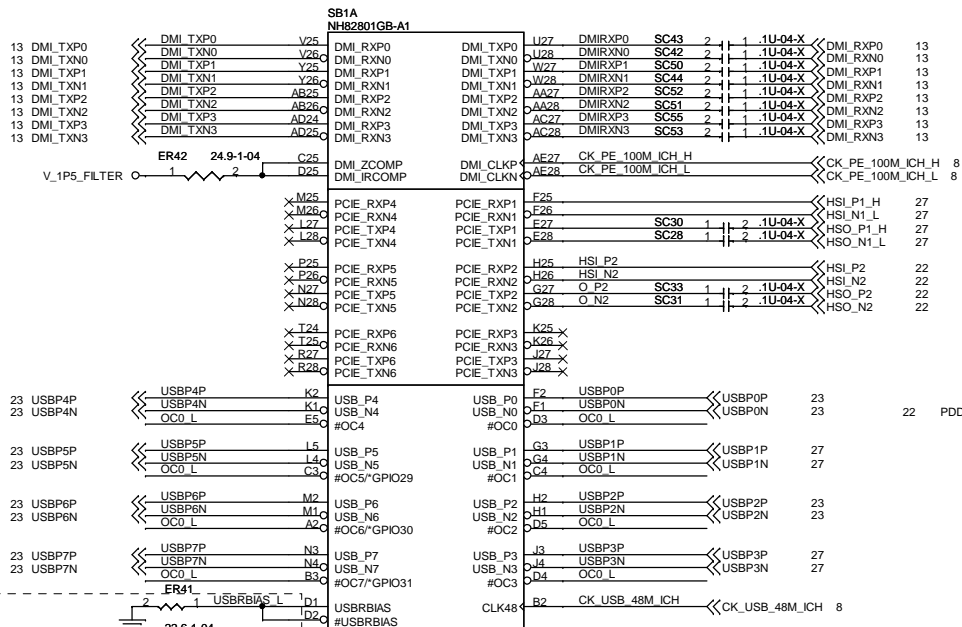
ECS Elitegroup Computer Systems

Title: **PCIEX16 slot**

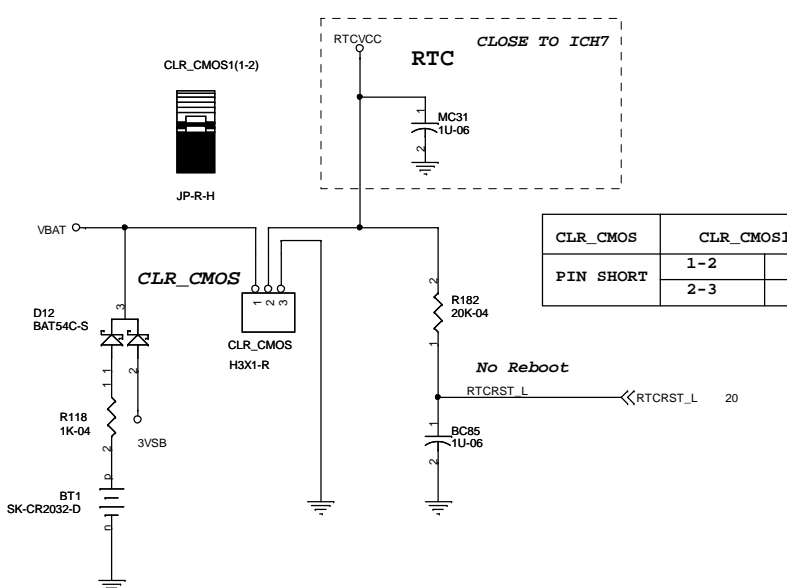
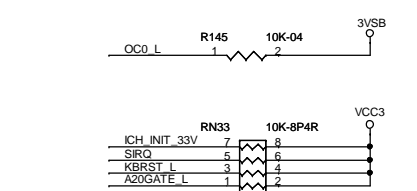
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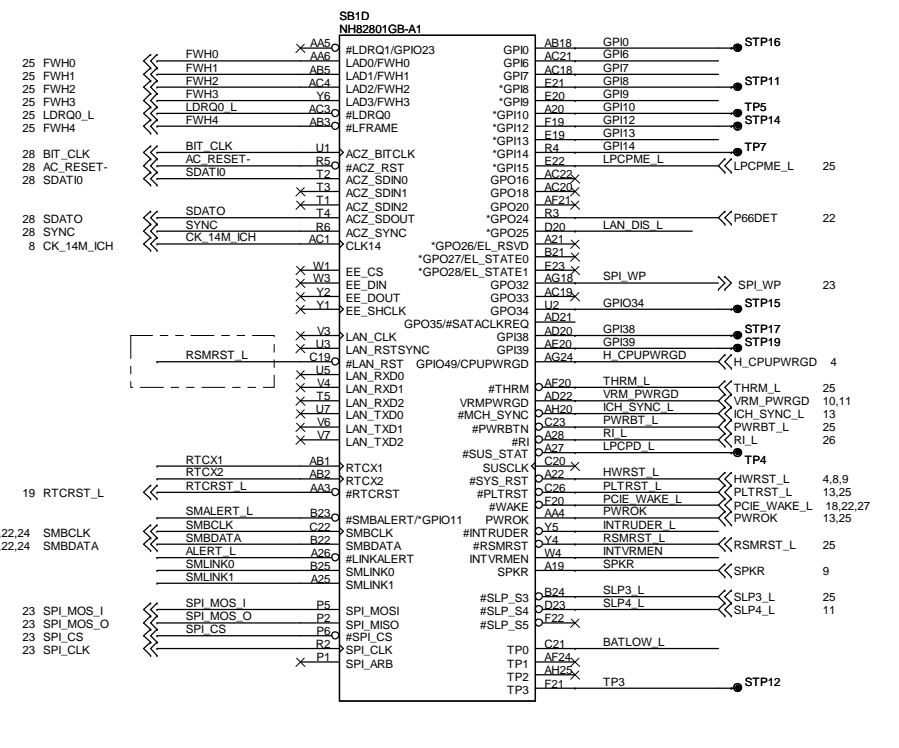
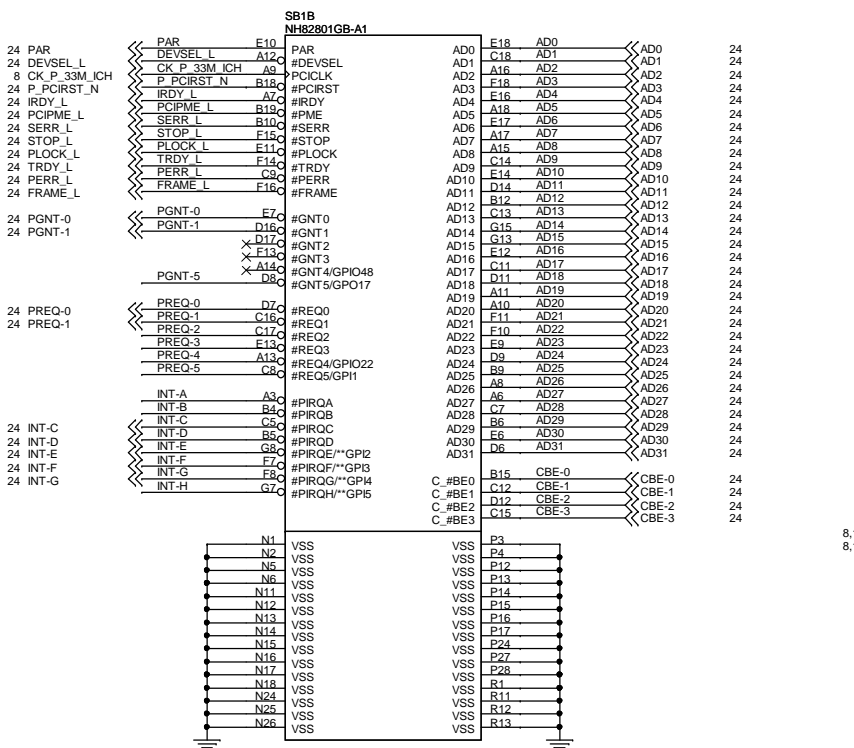
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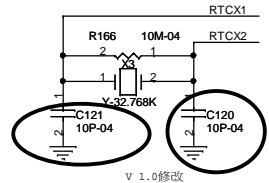
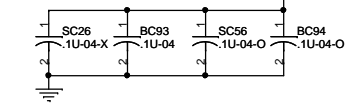
Must routing a trace to 22.6ohm pad, Don't direct connect with USBRBIAS_L (two trace must < 500 mils)



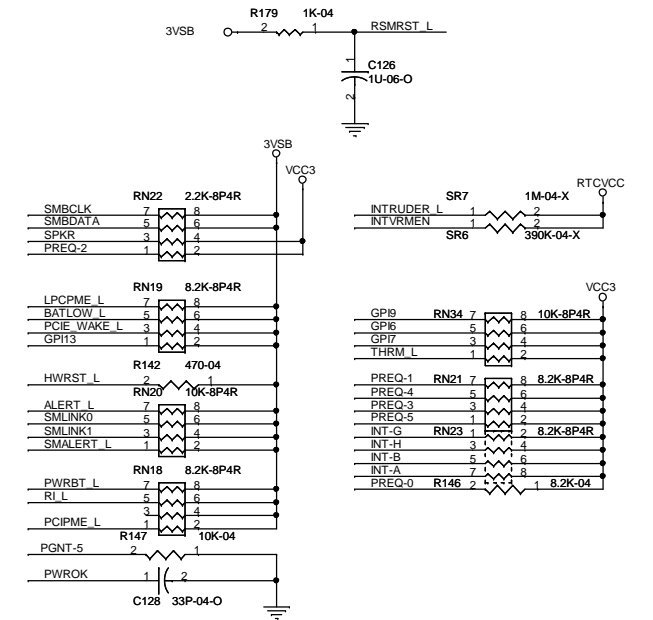
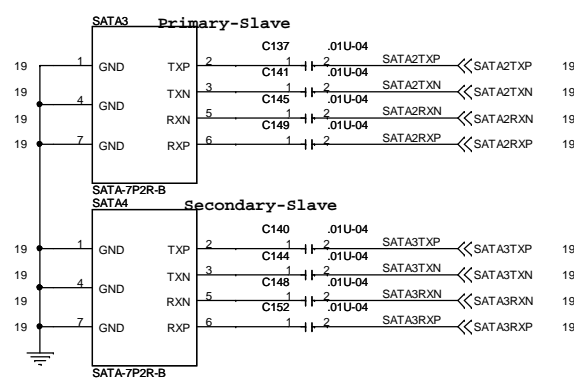
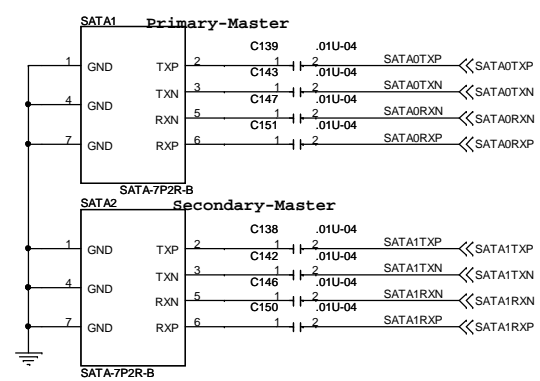
CLR_CMOS	CLR_CMOS1	
	PIN SHORT	
1-2		NORMAL
2-3		CLEAR CMOS



CAD NOTE:
PLACE 1 EACH NEAR A3 & F1.
PLACE REMAINDER ANYWHERE.

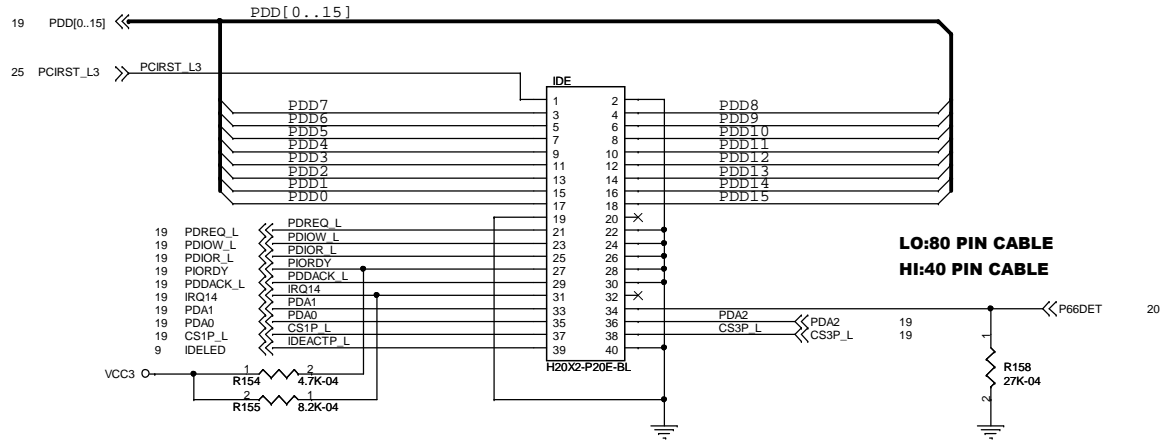


For 103
X3(wire)
XTAL-JW

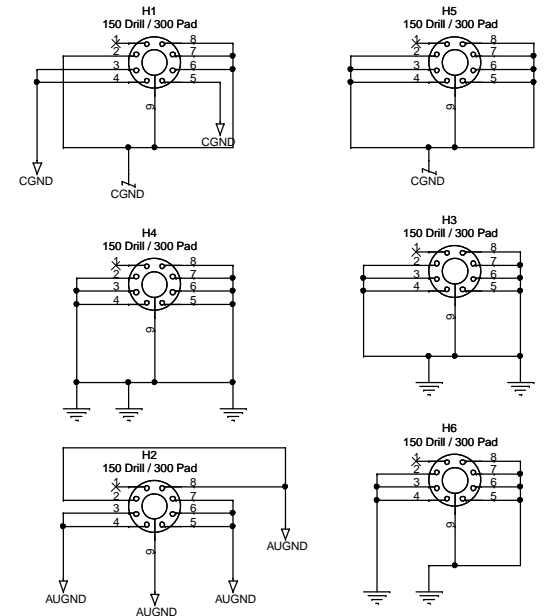
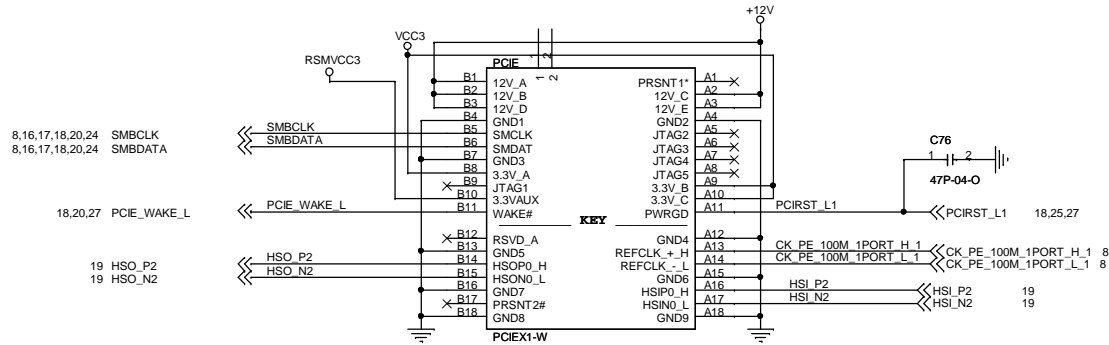
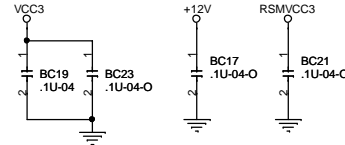


增加R240 PULL
LOW

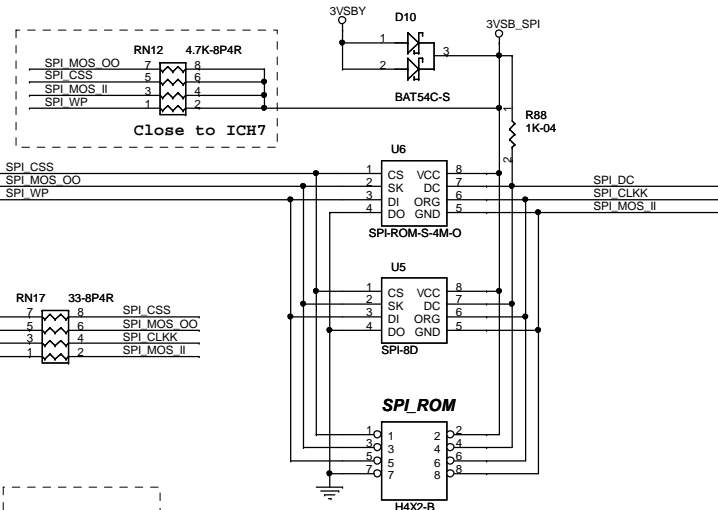
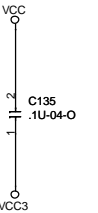
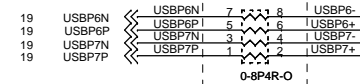
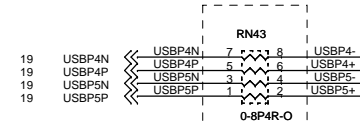
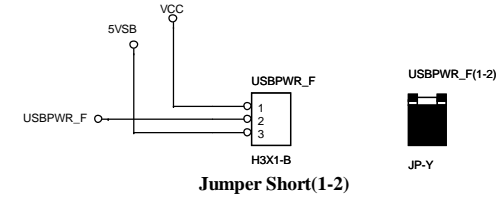
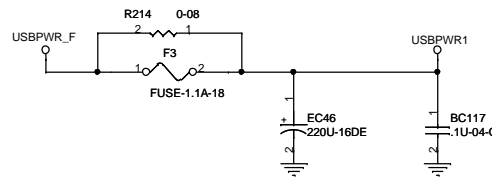
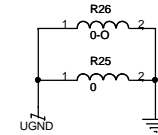
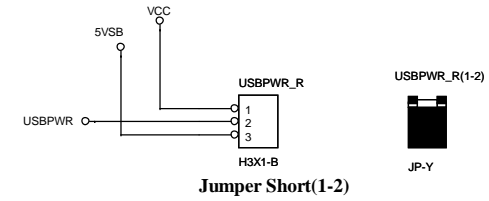
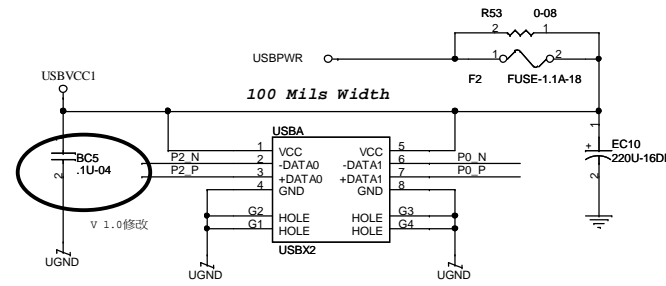
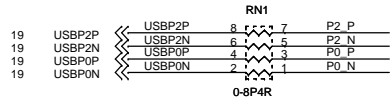
Elitegroup Computer Systems
ICH7 PCI/SPI/OTHER
G3IT-M3
 Date: Wednesday, February 20, 2008 Sheet 20 of 32



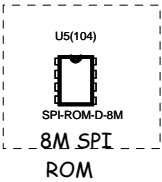
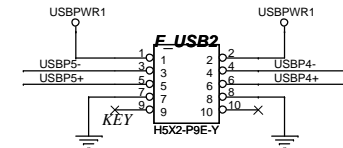
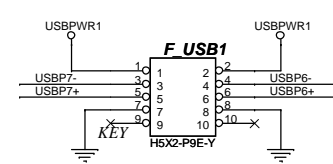
DATA LINES SHOULD BE MATCHED TO STROBES (PDIOR_L , PIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.



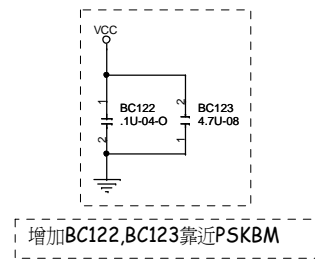
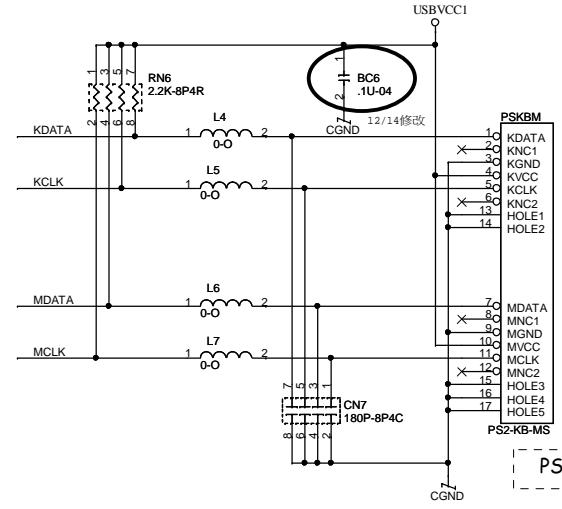
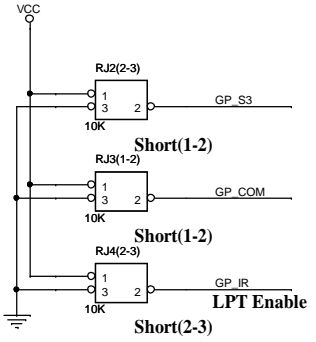
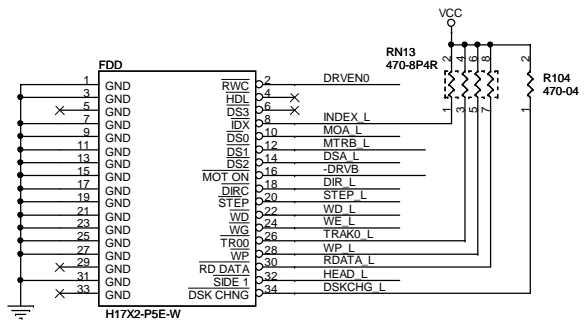
REAR_SIDE



改footprint=8P4R-SHORT短路在一起

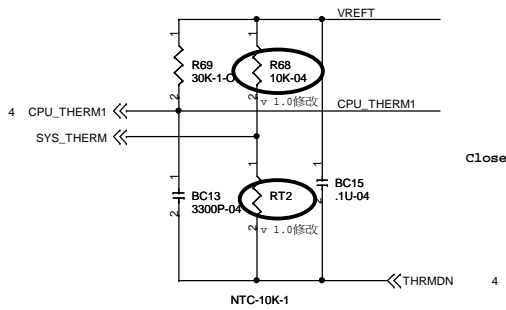


Title USB/SPI/Rear IO		
Size Custom	Document Number G31T-M3	Rev 1.0
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PS2-KB-MS改成無彈片

THERM. SENSING

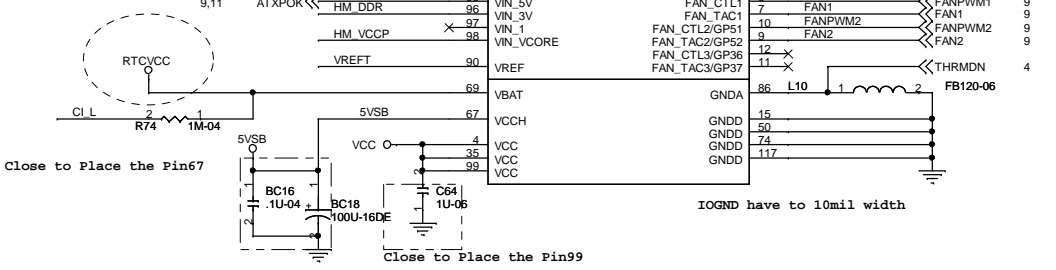
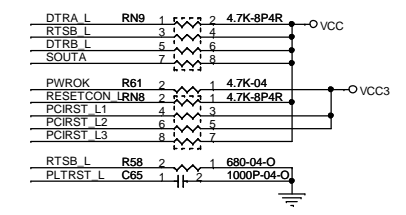
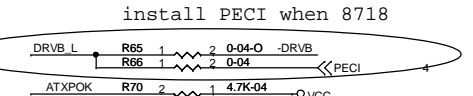


R69改不上件, BC13改成3300P-04

修改U3 Value:8718F

U3		I8718F-S GX-L	
20	LDR00_L	LDR00_L	38
19	SIRQ	SIRQ	39
13,20	PLTRST_L	PLTRST_L	37C
8	CK_P_33M_SIO	CK_P_33M_SIO	47
8	CK_48M_SIO	CK_48M_SIO	48
26	DCDA_L	DCDA_L	118
26	RIA_L	RIA_L	119
26	CTSA_L	CTSA_L	120
26	DTRA_L	DTRA_L	121
26	DTRA_L	DTRA_L	122
26	RTSA_L	RTSA_L	123
26	DSRA_L	DSRA_L	124
26	SOUTA	SOUTA	125
26	SINA	SINA	125
26	SLCT	SLCT	100
26	PE	PE	101
26	BUSY	BUSY	102
26	ACK_L	ACK_L	103
26	SLIN_L	SLIN_L	104
26	SLIN_L	SLIN_L	105
26	ERR_L	ERR_L	106
26	AFD_L	AFD_L	107
26	STB_L	STB_L	108
26	DRVEN0	DRVEN0	51
26	MOA_L	MOA_L	52
26	MTRB_L	MTRB_L	53
26	DSA_L	DSA_L	54
26	DRVB_L	DRVB_L	55
26	WD_L	WD_L	56
26	DIR_L	DIR_L	57
26	STEP#	STEP#	58
20	RSMRST_L	RSMRST#	85
13,20,27	PCIRST_L1	PCIRST#	31
11	PCIRST_L2	PCIRST#	32
22	PCIRST_L3	PCIRST#	33
11	GP10	GP10	84
9	LED0	LED0	77
9	LED1	LED1	78
11	GP41	GP41	78
19	A20GATE_L	A20GATE_L	46
27	JSACX/GP20	JSACX/GP24	23
25	JSACY/GP21	JSACY/GP25	22
24	JSAB1/GP22	JSAB1/GP26	20
24	JSAB2/GP23	JSAB2/GP27	20
28	MDIOUT/GP17	MDIOUT/GP17	70
29	MDIIN/GP16	MDIIN/GP16	66
91	VIN_5VSB	VIN_5VSB	89
92	VIN_VDDQ	VIN_VDDQ	88
93	VIN_+12V	VIN_+12V	87
94	VIN_4	VIN_4	8
95	VIN_5V	VIN_5V	7
96	VIN_3V	VIN_3V	6
97	VIN_1	VIN_1	5
98	VIN_VCORE	VIN_VCORE	4
90	VREF	VREF	69
67	VBAT	VBAT	67
4	VCCH	VCCH	4
35	VCC	VCC	35
99	VCC	VCC	99
86	IOGND	IOGND	86
15	GND	GND	15
50	GND	GND	50
74	GND	GND	74
117	GND	GND	117

12/18修改



Close to Place the Pin67

Close to Place the Pin99

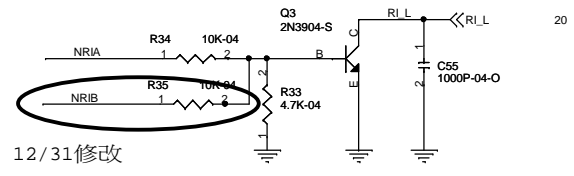
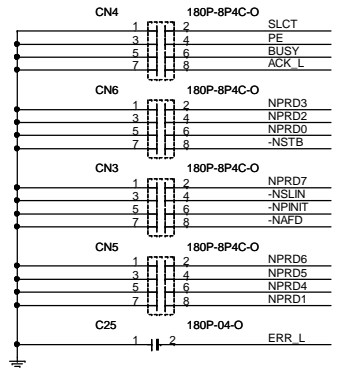
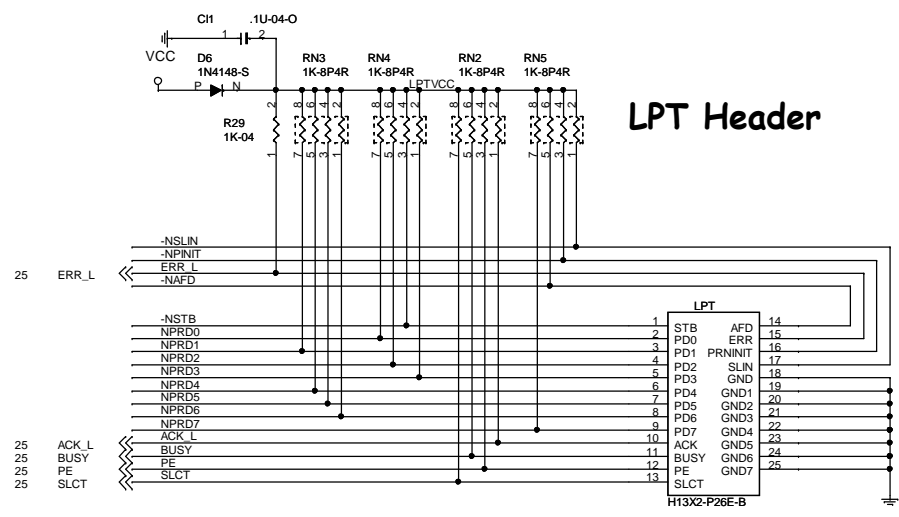
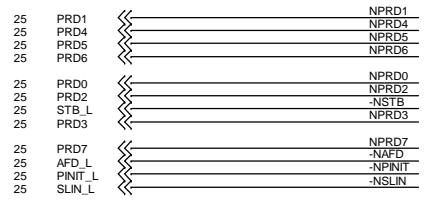
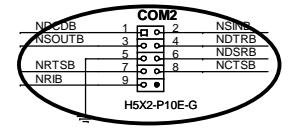
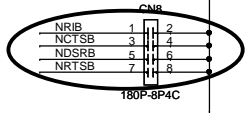
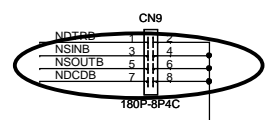
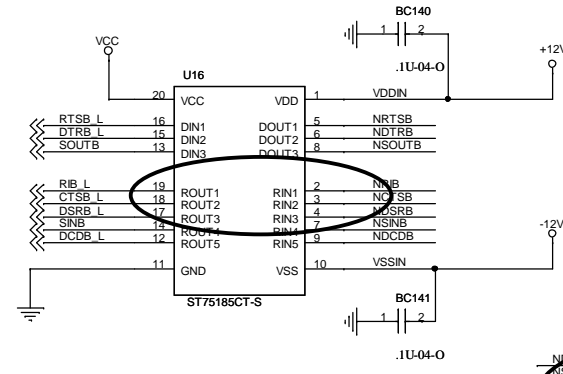
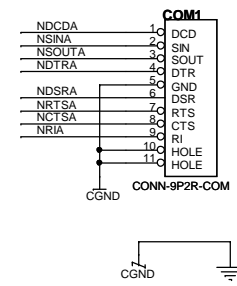
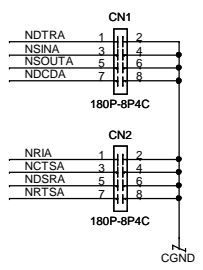
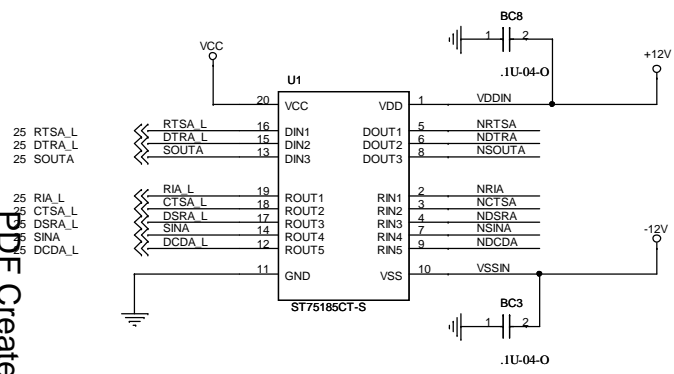
Elitegroup Computer Systems

Title: **LPC_FDD/KB/M**

Size: Document Number **G3IT-M3** Rev **1.0**

Date: Wednesday, February 20, 2008 Sheet 25 of 32

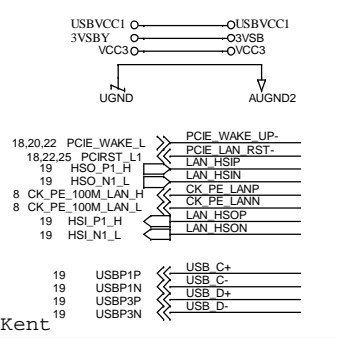
PDF Created with deskPDF Writer - Trial :: http://www.docudesk.com



12/31修改

Elitegroup Computer Systems		
I/O Ports		
Title	G31T-M3	
Size	Document Number	Rev
Custom	G31T-M3	1.0
Date:	Wednesday, February 20, 2008	Sheet 26 of 32

External Connection



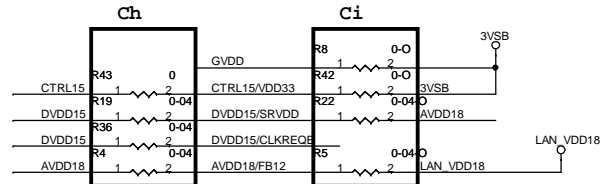
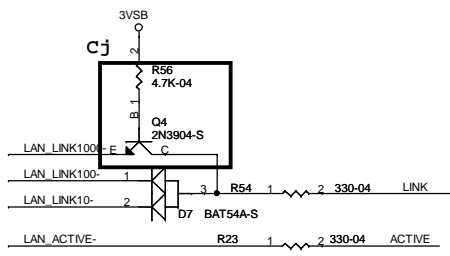
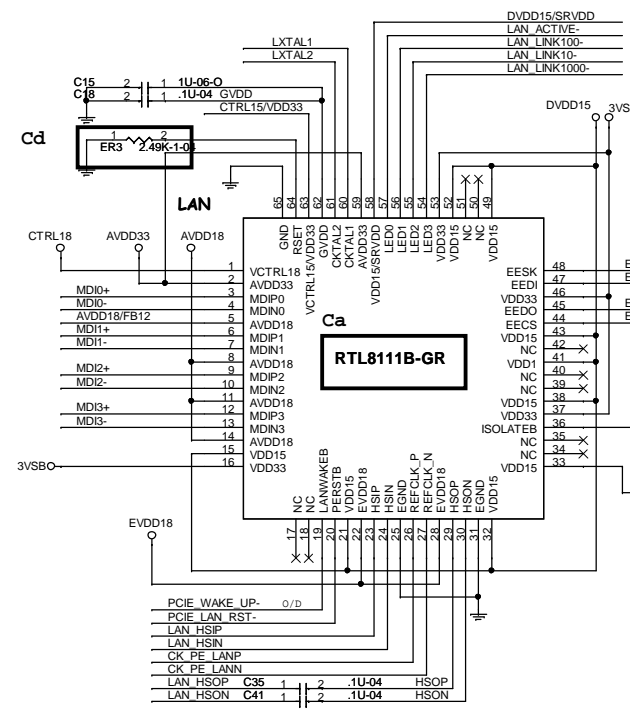
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When you found some bug, please inform Ren(ext:665) to update circuit.

Part Difference

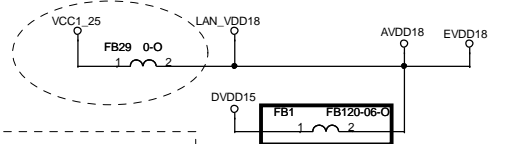
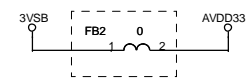
	RTL8101E-GR 10/100M	RTL8111C-GR 1000M	RTL8111B-GR 1000M
Part 1	RTL8101E-GR	RTL8111C-GR	RTL8111B-GR
Part 2	V	X	X
Part 3	X	V	X
Part 4	2K-1-04	2.49K-1-04	2.49K-1-04
Part 5	.01U-04	0-04	0-04
Part 6	V	X	X
Part 7	V	X	V
Part 8	X	V	X
Part 9	X	V	V
Part 10	USBX2-LAN-100	USBX2-LAN-1000	USBX2-LAN-1000
Part 11	X	X	HA8550-D
Part 12	0	chock+EC50	X

Power Difference

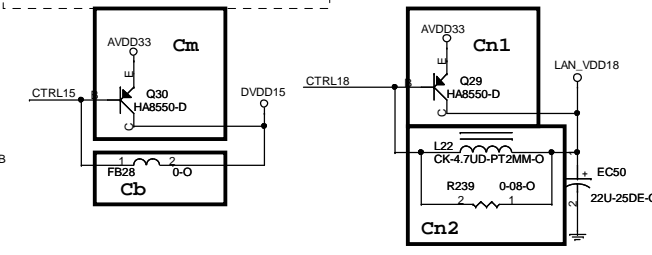
	RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V



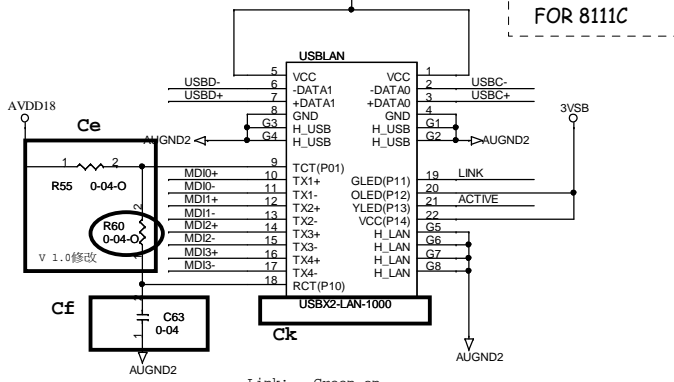
修改FB2 為0-06



修改Q29,Q30 ORCED LIB PNP

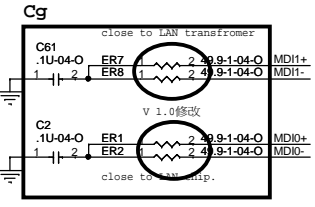


增加CHOCK FOR 8111C



Link: Green on
Active: Yellow blinking

USB C+	8	7	7	USB C+
USB C-	6	5	5	USBC-
USB D+	4	3	3	USBD+
USB D-	2	1	1	USBD-



Elitegroup Computer Systems

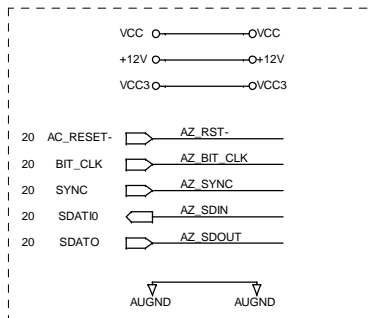
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Size: Document Number **631T-M3** Rev **1.0**

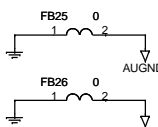
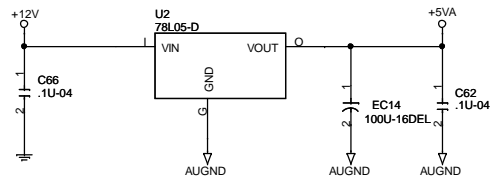
Custom: **631T-M3**

Date: Wednesday, February 20, 2008 Sheet 27 of 32

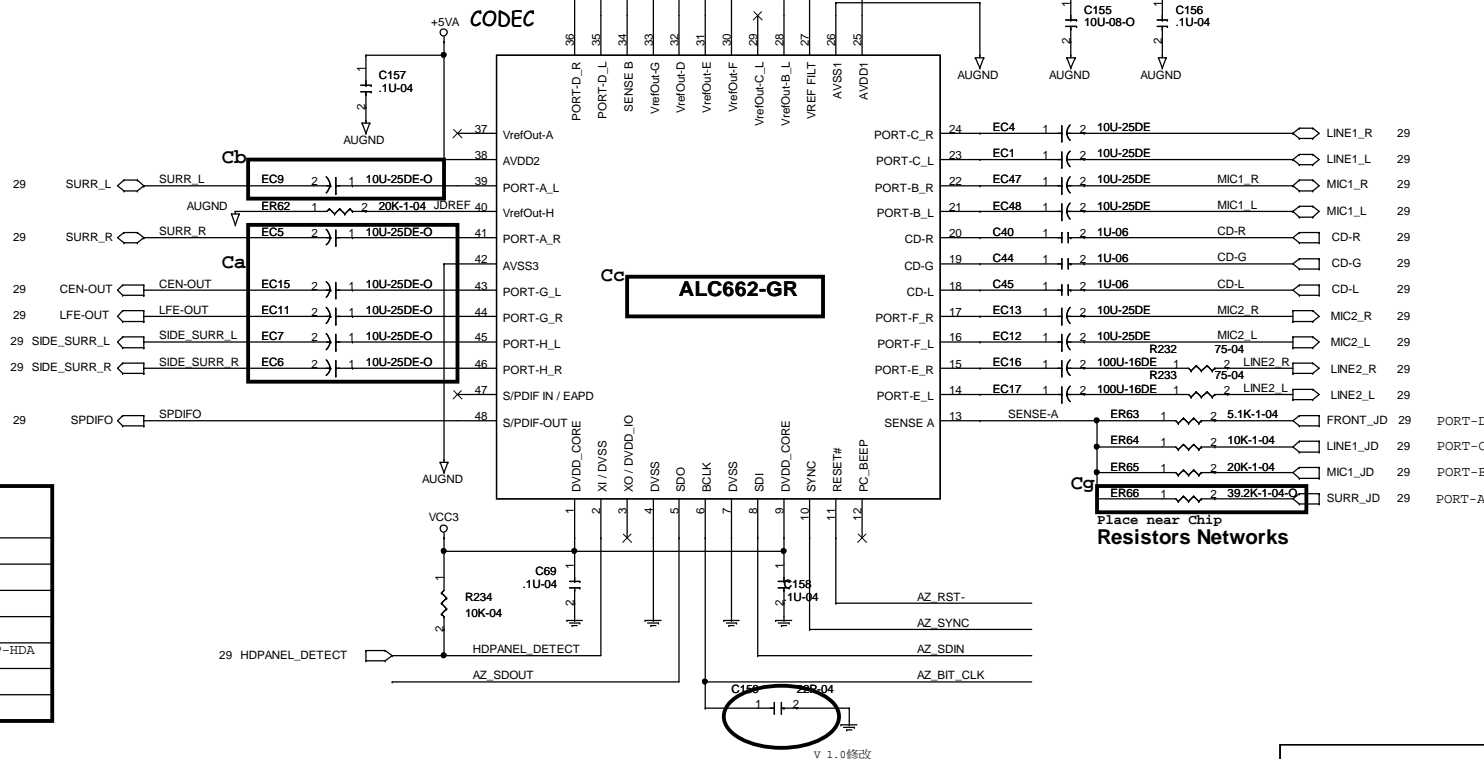
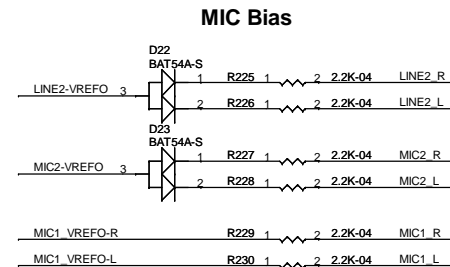
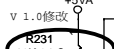
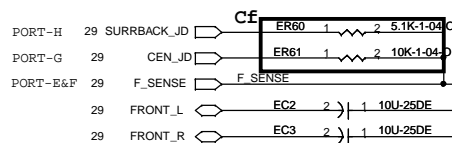
External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.



Place near Chip
Resistors Networks



BOM Difference

Location	ALC883 7.1 Ch	ALC662 5.1 CH
Ca	V	X
Cb	V	X
Cc	ALC883	ALC662
Cd	V	X
Ce	AUDIO-6P	AUDIO-3P-HDA
Cf	V	X
Cg	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

ECS Elitegroup Computer Systems

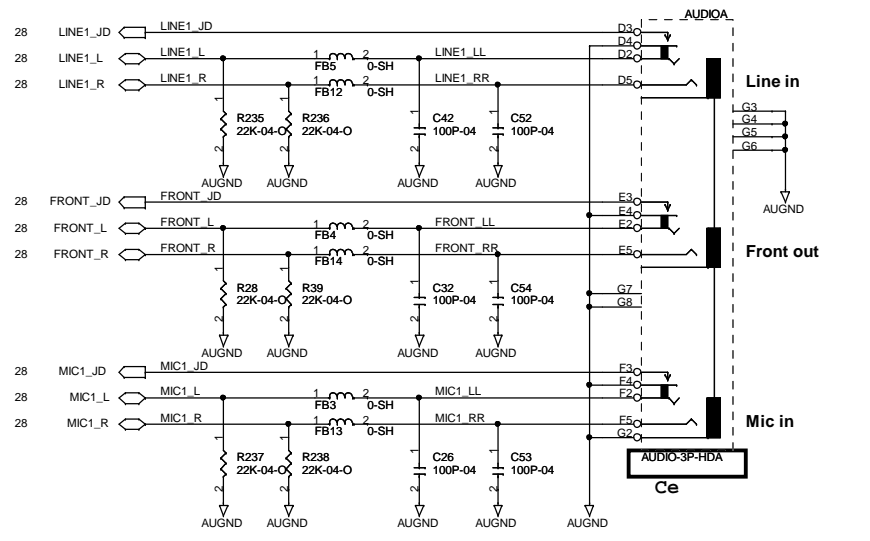
File: **AUDIO ALC883/ALC662 (CHIP)**

Size: Document Number **G31T-M3** Rev: **1.0**

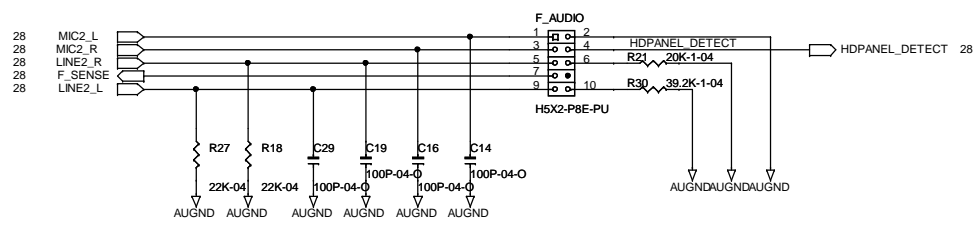
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Date: Wednesday, February 20, 2008 Sheet 28 of 32

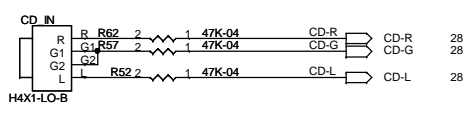
REAR-AUDIO



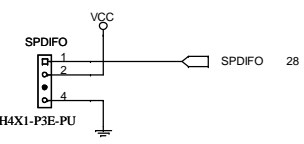
FRONT-AUDIO



CD_IN



SPDIF-OUT



Cd

