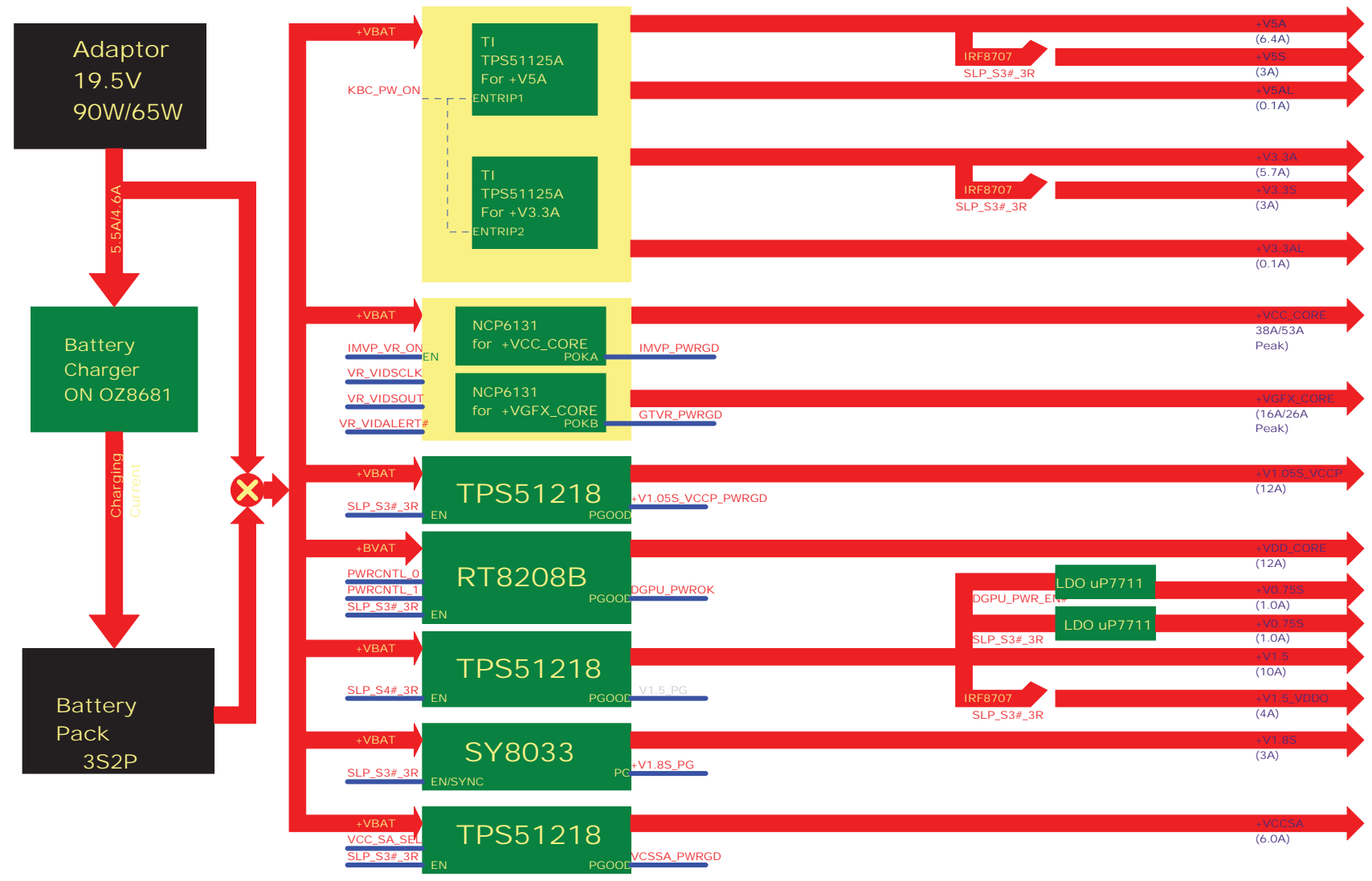
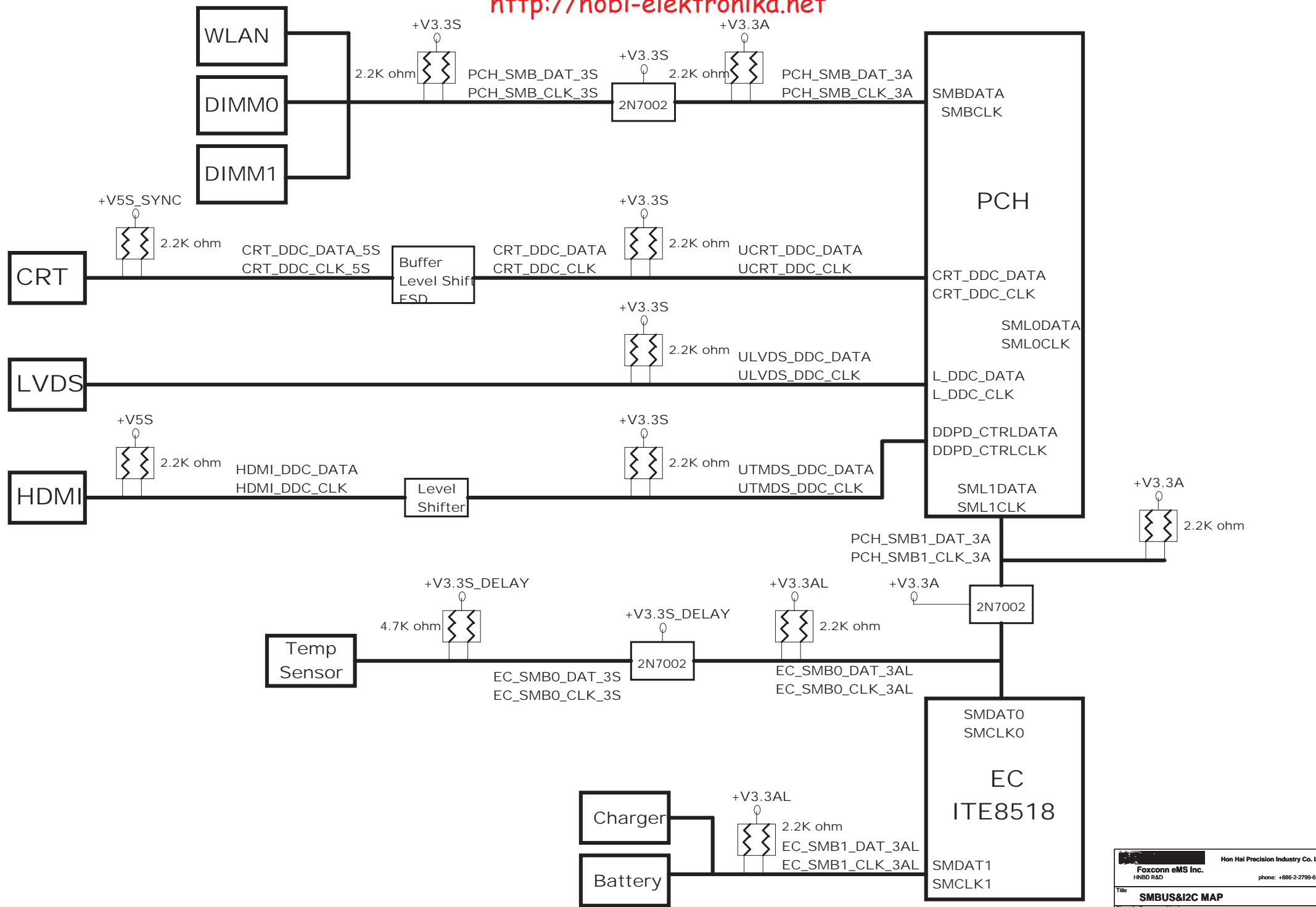



POWER MAP

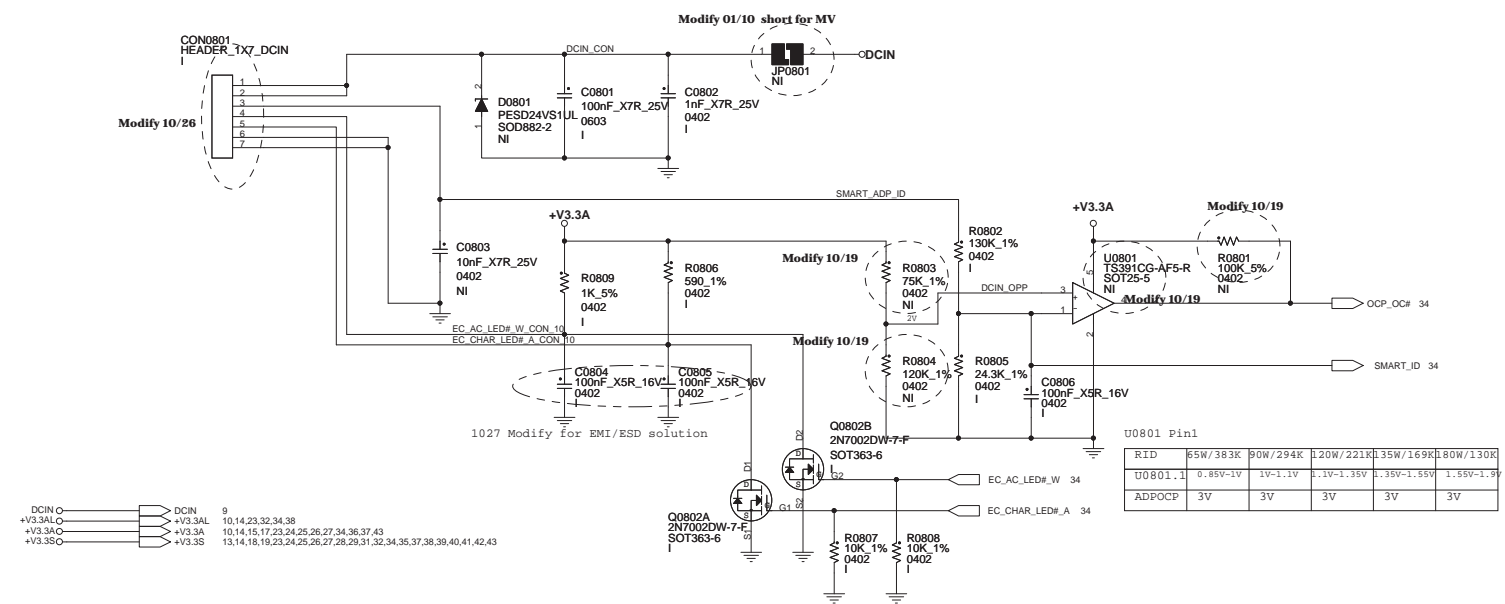




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HNBD R&D			
Title			
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Size	Document Number		Rev
A	CHICAGO		MV
Page Modified: Tuesday, March 08, 2011		08:28:58 (UTC/GMT)	Sheet 7 of 43

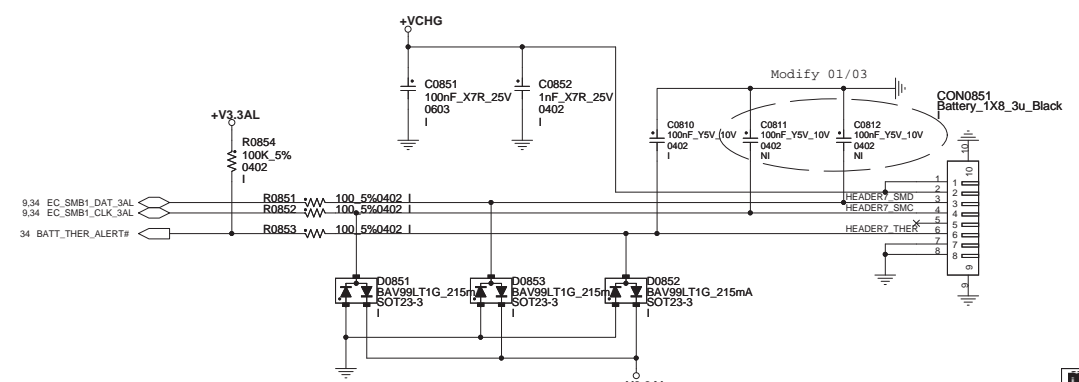
DC_JACK WIRE TO BOARD CONNECTOR

2010.1203.0

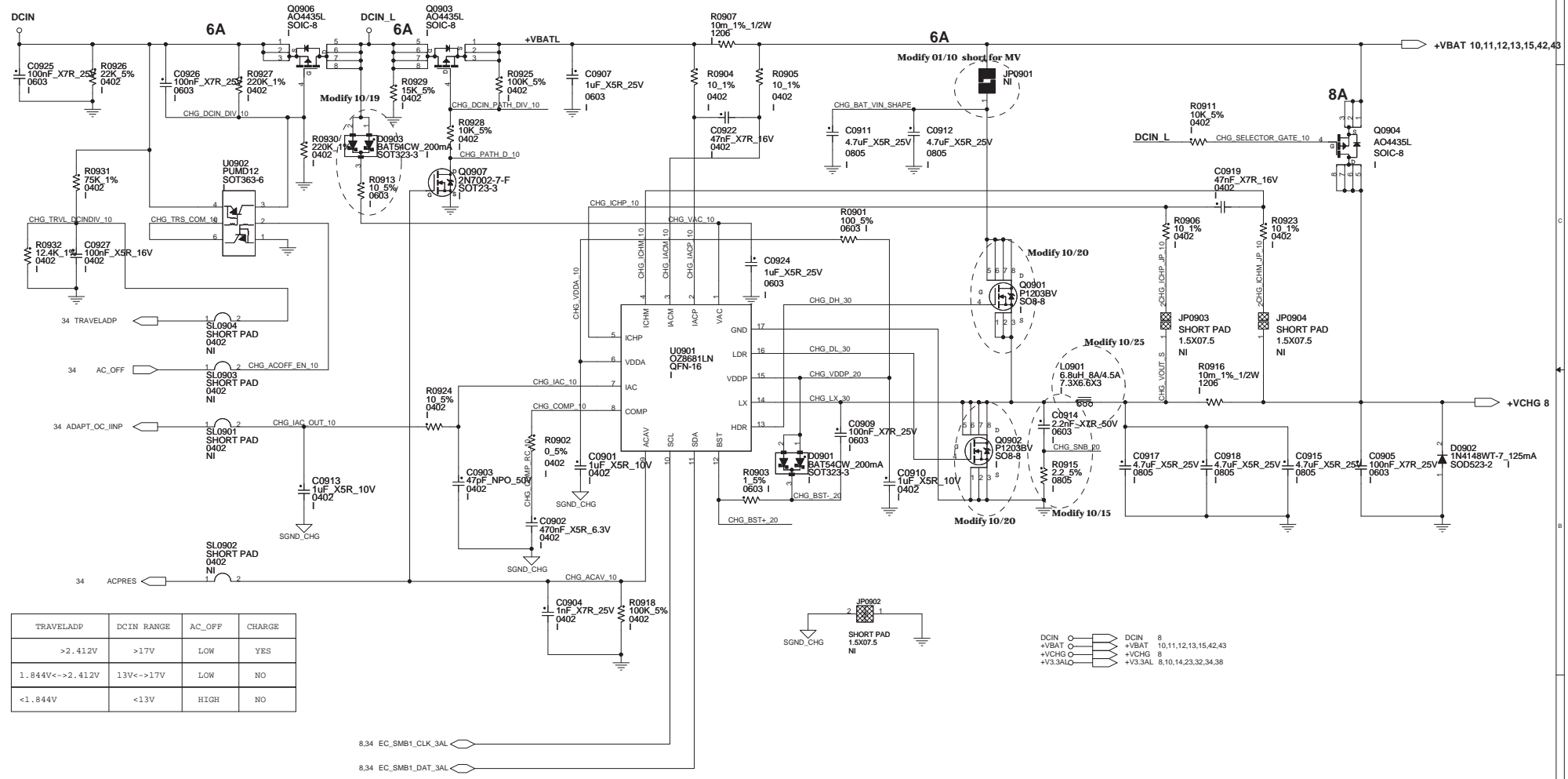


BATTERY CONNECTOR

2010.0914.0



BATTERY CHARGER



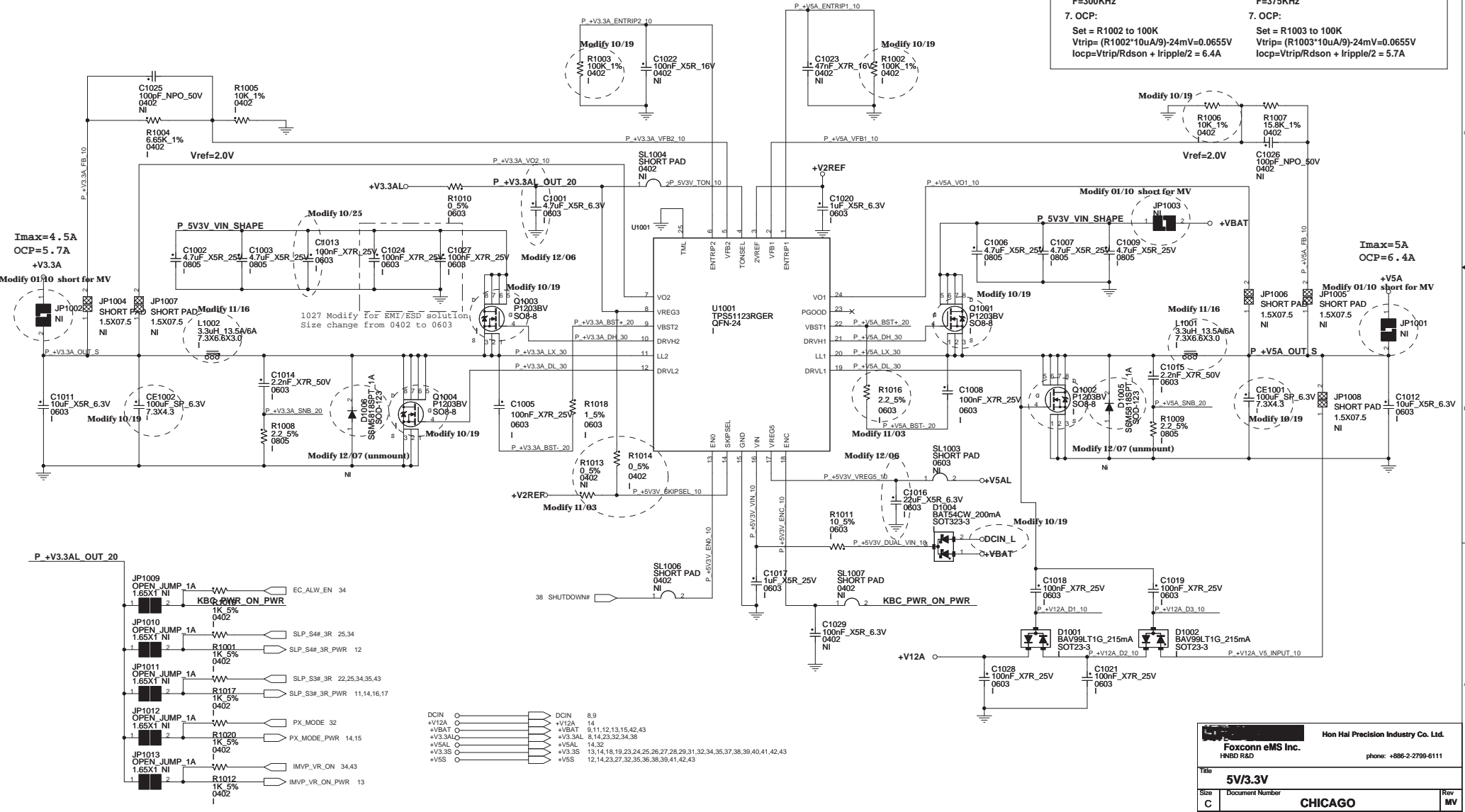
TRAVELADP	DCIN RANGE	AC_OFF	CHARGE
>2.412V	>17V	LOW	YES
1.844V<->2.412V	13V<->17V	LOW	NO
<1.844V	<13V	HIGH	NO

- DCIN 8
- +VBAT 10,11,12,13,15,42,43
- +VCHG 8
- +V3.AL0 8,10,14,23,32,34,38

+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$ 2. Ripple Current: $I_{rip} = 3.72A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 55.8mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 11A$ ($T = 25^\circ C$) $I_{peak} = 88A$ (Pause = 10 us) 6. Frequency: $F = 300KHz$ 7. OCP: $Set = R1002 \text{ to } 100K$ $V_{trip} = (R1002 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple}/2 = 6.4A$	+V3.3A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$ 2. Ripple Current: $I_{rip} = 2.21A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 33.15mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: L-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 11A$ ($T = 25^\circ C$) $I_{peak} = 88A$ (Pause = 10 us) 6. Frequency: $F = 375KHz$ 7. OCP: $Set = R1003 \text{ to } 100K$ $V_{trip} = (R1003 \cdot 10uA/9) - 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple}/2 = 5.7A$
---	--



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Title: **5V/3.3V**

Size	Document Number	Rev
C	CHICAGO	MV

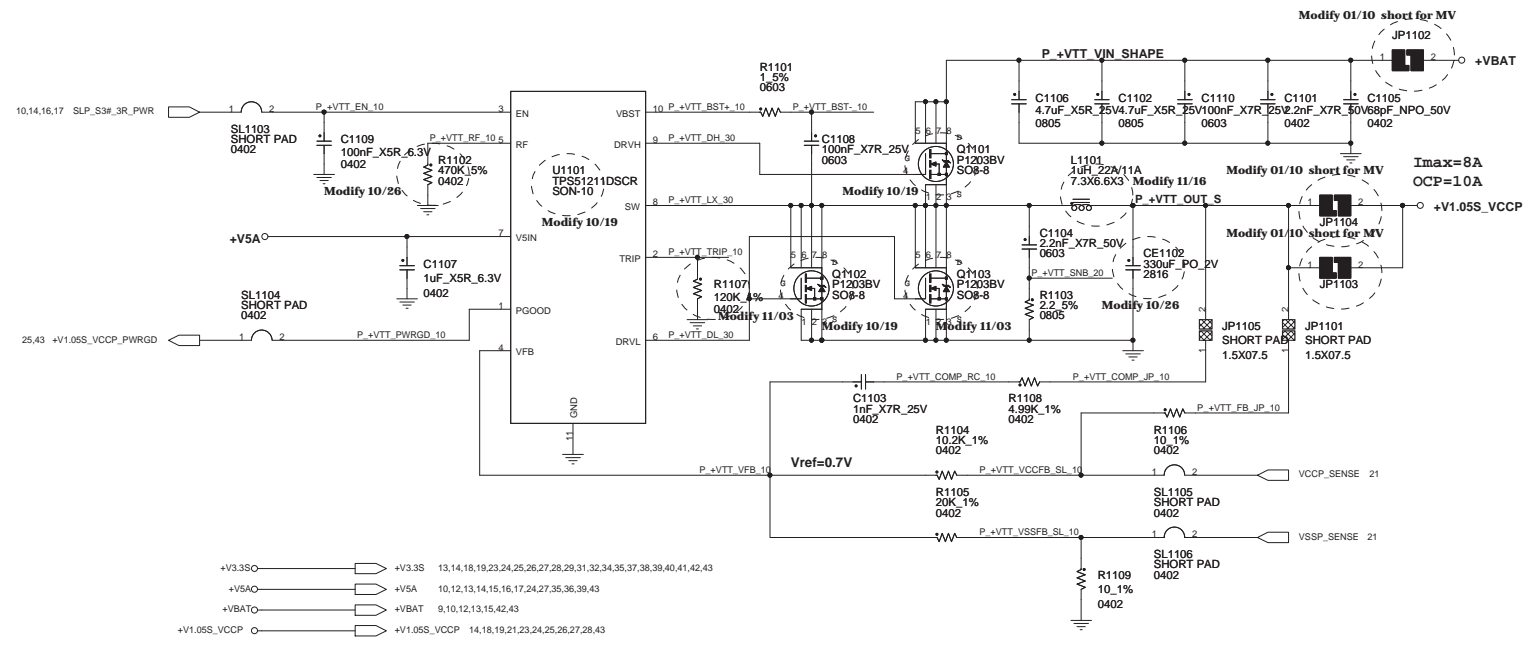
Page Modified: Tuesday, March 09, 2011 08:28:59 (UTC+08:00) Sheet 10 of 43

+VTT POWER SUPPLY

2010.1103.0

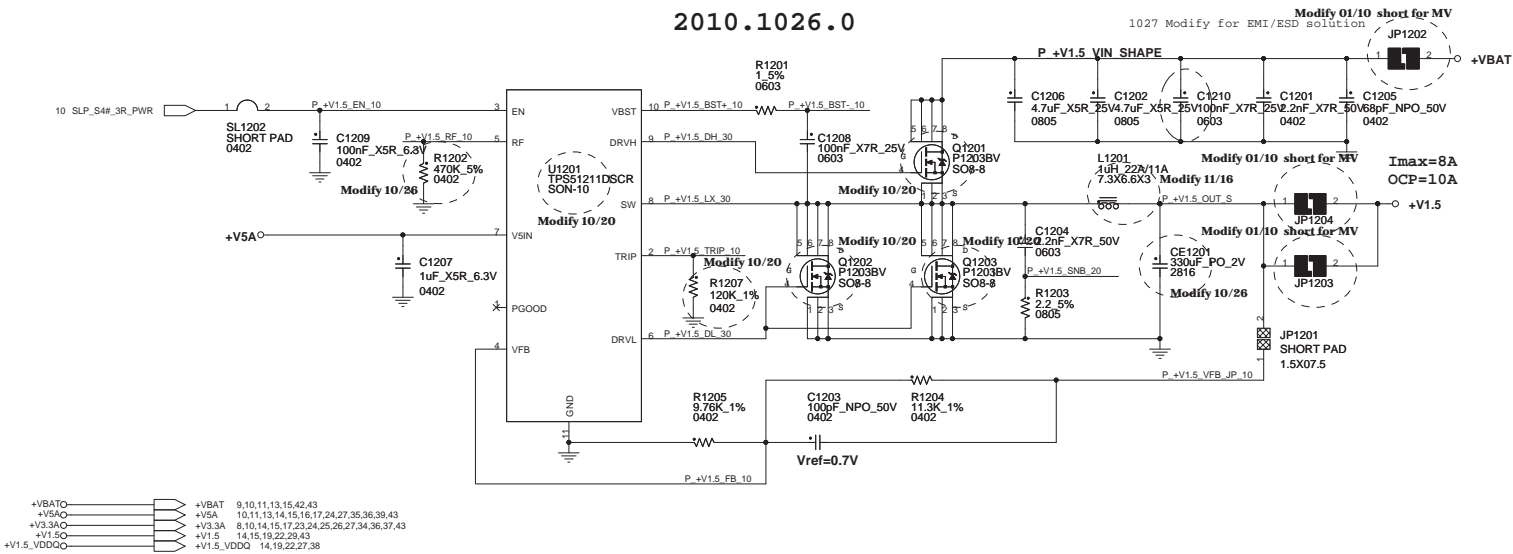
- +V1.05S_VCCP:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.24A$
 - Ripple Current:**
 $I_{rip} = 3.42A$
 - Ripple Voltage:**
 $ESR/1 = 9mohm$
 $V_{rip} = 30.78mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3mohm$
 - MOSFET Spec:**

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
$R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$)	$R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$)
$I_{cont} = 11A$ ($T = 25^\circ C$)	$I_{cont} = 11A$ ($T = 25^\circ C$)
$I_{peak} = 88A$ (Pause = 10 us)	$I_{peak} = 88A$ (Pause = 10 us)
 - Frequency:**
 $F = 290KHz$ ($R1102 = 0ohm$)
 - OCP:**
 Set = R1107 to 120K
 $V_{trip} = R1107 \cdot 10uA = 1.2V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{ds(on)}) + I_{ripple} / 2 = 10A$



+V1.5 POWER SUPPLY

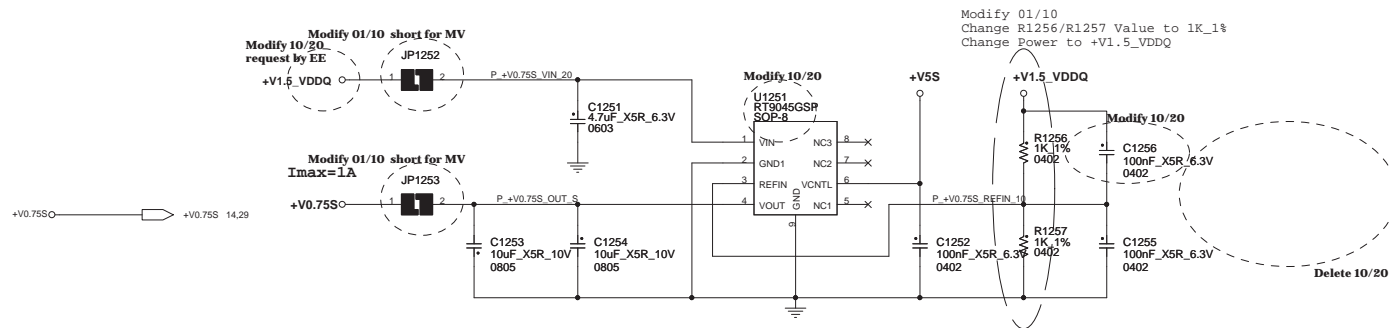
2010.1026.0



- +V1.5:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.78A$
 - Ripple Current:**
 $I_{rip} = 3.34A$
 - Ripple Voltage:**
 $ESR/1 = 9m\Omega$
 $V_{rip} = 30.6mV$
 - Inductor Spec:**
 $I_{sat} = 36A$
 $I_{dc} = 18A$
 $DCR = 3.3m\Omega$
 $OCF = 1.0A$
 - MOSFET Spec:**
 H-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 L-side MOSFET: IRF8707PBF
 $R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 11A$ ($T = 25^\circ C$)
 $I_{peak} = 88A$ (Pause = 10 us)
 - Frequency:**
 $F = 290KHz$ ($R_{0902} = 0\Omega$)
 - OCP:**
 Set = R1207 to 120K
 $V_{trip} = R1207 \cdot 10\mu A = 1.2V$
 $I_{ocp} = (V_{trip} / 8 \cdot R_{dson}) + I_{ripple} / 2 = 10A$

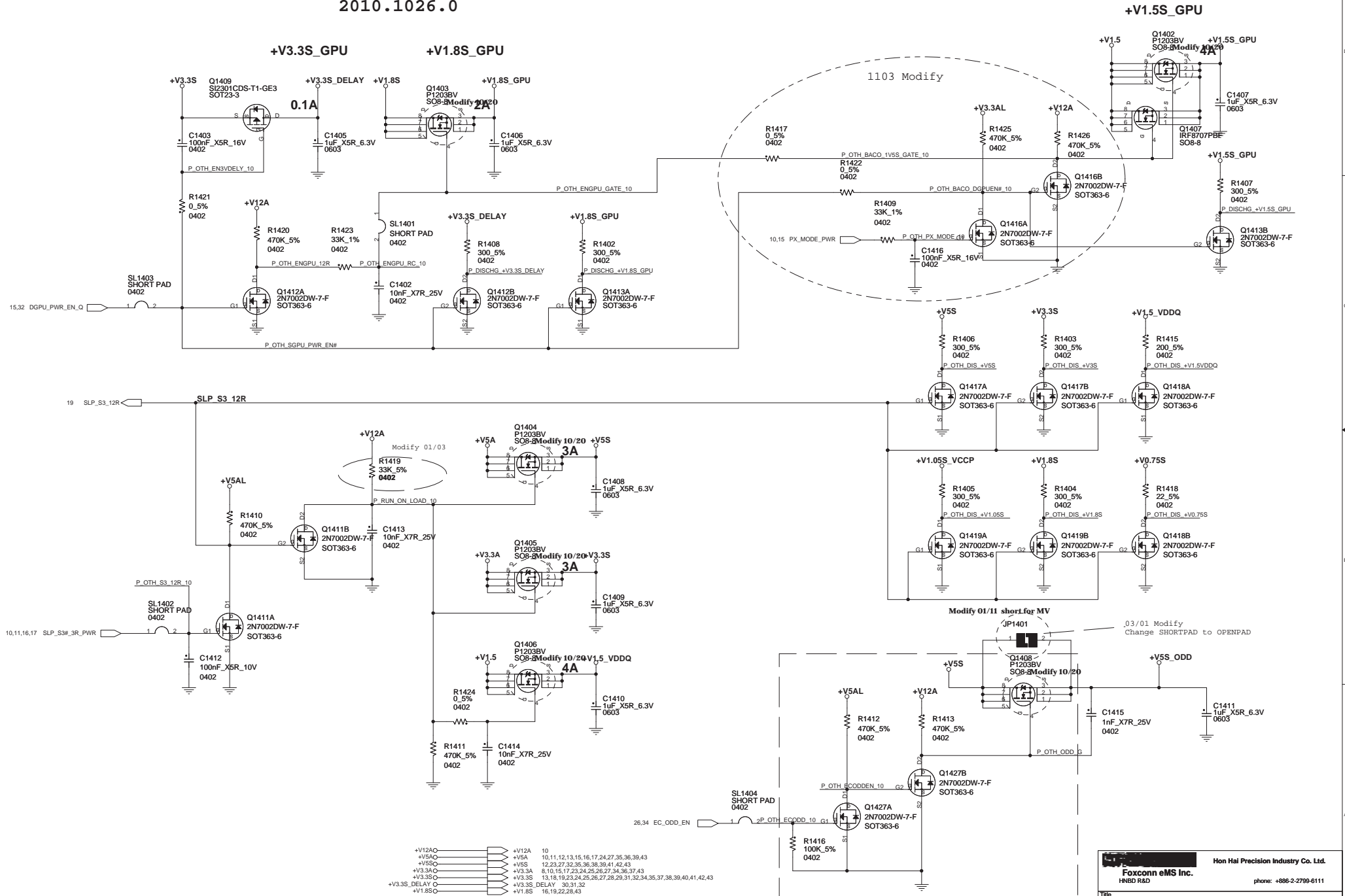
+V0.75S POWER SUPPLY

2010.1026.0



OTHER POWER / DISCHARGE CIRCUITS

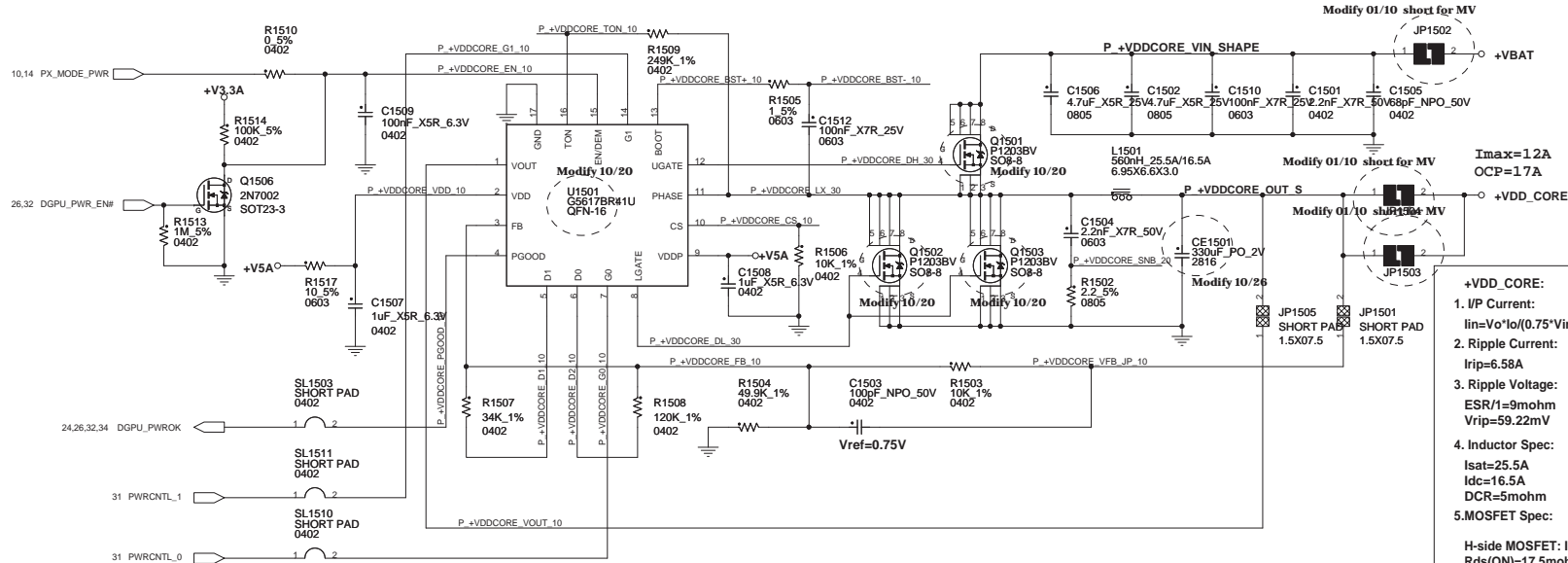
2010.1026.0



- +V12AO → +V12A 10
- +V5AO → +V5A 10,11,12,13,15,16,17,24,27,35,36,39,43
- +V5S → +V5S 12,23,27,32,35,36,38,39,41,42,43
- +V3.3AC → +V3.3A 8,10,15,17,23,24,25,26,27,34,36,37,43
- +V3.3C → +V3.3S 15,16,18,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
- +V3.3S_DELAY → +V3.3S_DELAY 30,31,32
- +V1.8S → +V1.8S 16,19,22,28,43

http://hobi-elektronika.net +VDD_CORE POWER SUPPLY

2010.1026.0

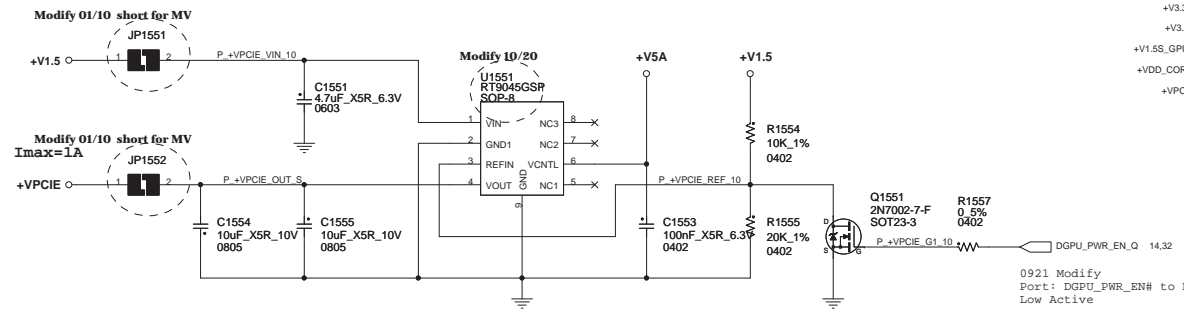


PWRCNTL_1	PWRCNTL_0	VDD_CORE
0	---	1.121V
---	---	---
1	---	0.9V
---	---	---

- +VDD_CORE:**
- 1. I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.48A$
 - 2. Ripple Current:**
 $I_{rip} = 6.58A$
 - 3. Ripple Voltage:**
 $ESR/1 = 9m\Omega$
 $V_{rip} = 59.22mV$
 - 4. Inductor Spec:**
 $I_{sat} = 25.5A$
 $I_{dc} = 16.5A$
 $DCR = 5m\Omega$
 - 5. MOSFET Spec:**

H-side MOSFET: IRF8707PBF	L-side MOSFET: IRF8707PBF
$R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)	$R_{ds(ON)} = 17.5m\Omega$ ($V_{gs} = 4.5V$)
$I_{cont} = 11A$ ($T = 25^\circ C$)	$I_{cont} = 11A$ ($T = 25^\circ C$)
$I_{peak} = 88A$ (Pause = 10 us)	$I_{peak} = 88A$ (Pause = 10 us)
 - 6. Frequency:**
 $TON = 9.6 \cdot P \cdot R1509 \cdot (VOUT + 0.1) / (VIN - 0.3) + 50ns = 206ns$
 $F = VOUT / (VIN \cdot TON) = 286KHz$
 - 7. OCP:**
 Set = R1506 to 10K
 $V_{trip} = R1206 \cdot 10uA = 0.1V$
 $I_{ocp} = (V_{trip} / R_{dson}) + I_{ripple} / 2 = 17A$

2010.1020.0 +VPCIE POWER SUPPLY



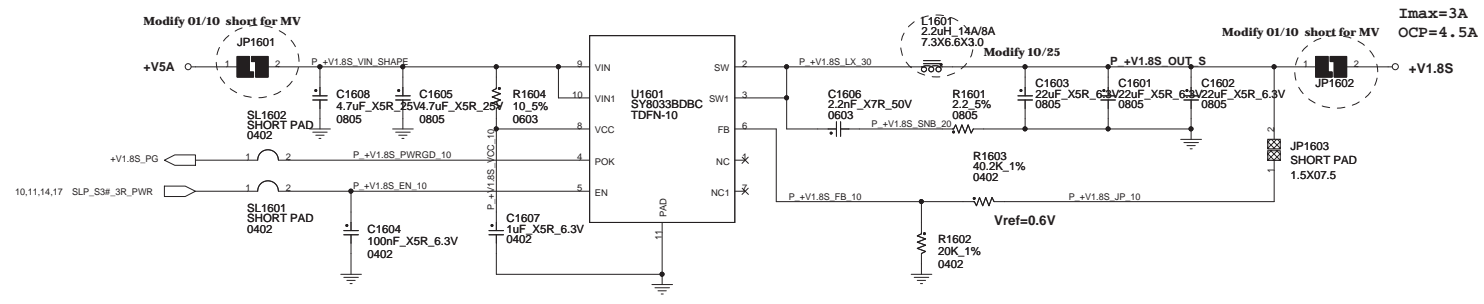
- +VBATC → +VBAT 9,10,11,12,13,42,43
- +V5A0 → +V5A 10,11,12,13,14,16,17,24,27,35,36,39,43
- +V3.3A → +V3.3A 8,10,14,17,23,24,25,26,27,34,36,37,43
- +V3.3S → +V3.3S 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
- +V1.5S_GPU → +V1.5S_GPU 14,30,32,33,43
- +VDD_CORE → +VDD_CORE 32,43
- +VPCIE → +VPCIE 30,31,32,43

0921 Modify
 Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
 Low Active

+V1.8S POWER SUPPLY

2010.1025.0

- +V1.8S:**
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$
 - Ripple Current:**
 $I_{rip} = 0.53A$
 - Ripple Voltage:**
 $ESR/3 = 3.3m\Omega$
 $V_{rip} = 1.75mV$
 - Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 20m\Omega$
 - MOSFET Spec:**
H-side P-MOSFET: $R_{ds(ON)} = 110m\Omega$ ($V_{gs} = 4.5V$)
L-side N-MOSFET: $R_{ds(ON)} = 75m\Omega$ ($V_{gs} = 4.5V$)
 - Frequency:**
 $F = 1MHz$ (min=800KHz, max=1.2MHz)
 - OCP:**
 $I_{ocp} = 4A(\min) / 4.5A(\text{typ}) / 5A(\text{max})$

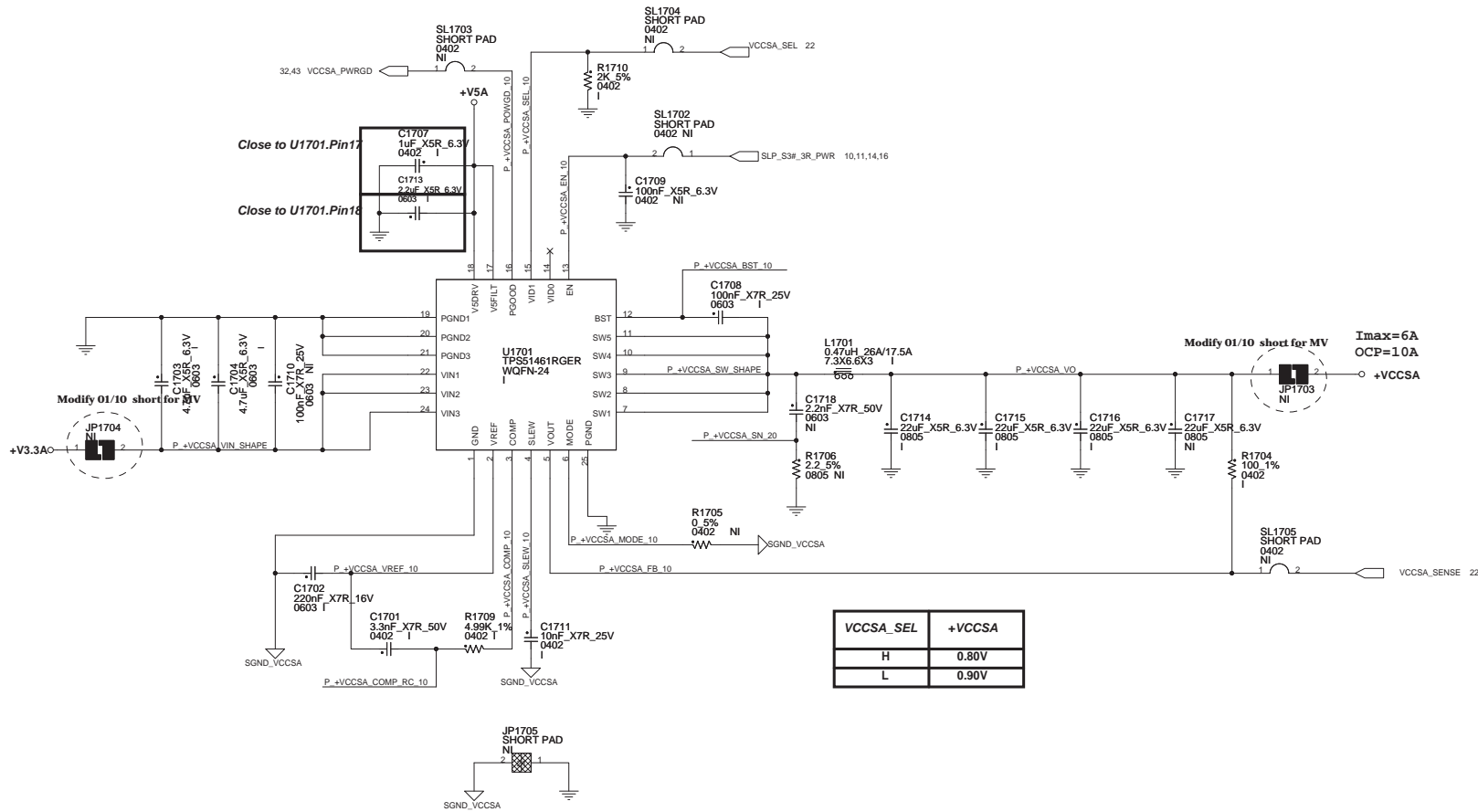


+VCCSA POWER SUPPLY

2010.1026.0

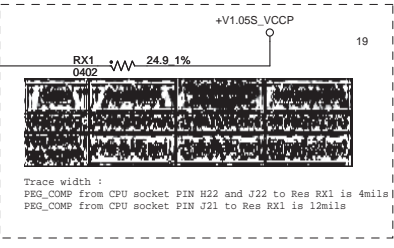
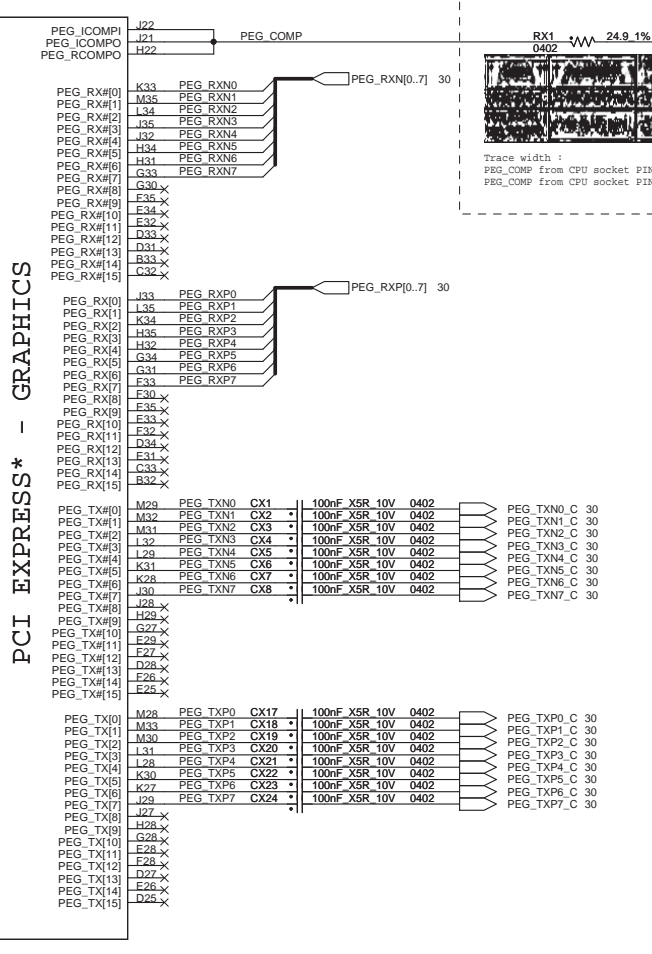
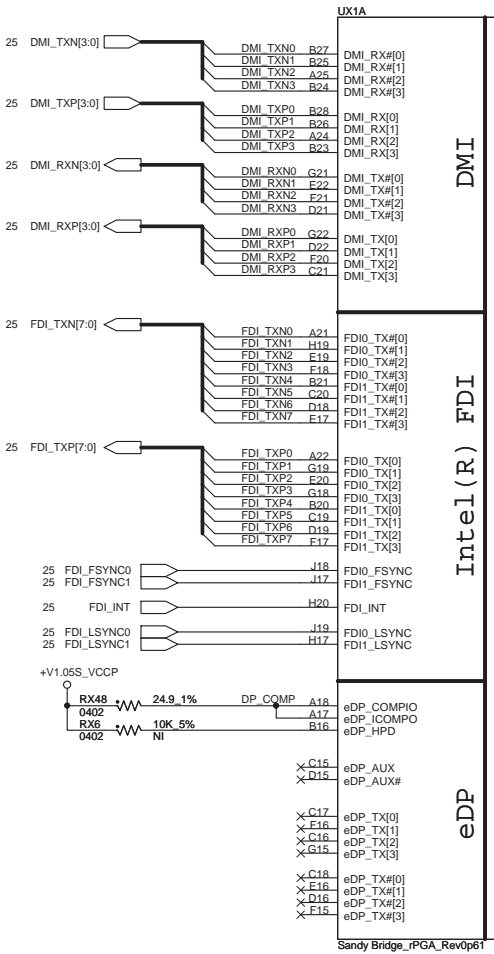
- +VCCSA:
- 1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.18A$
- 2. Ripple Current:
 $I_{rip} = 1.39A$
- 3. Ripple Voltage:
 $ESR/4 = 1mohm$
 $V_{rip} = 1.39mV$
- 4. Inductor Spec:
 $I_{sat} = 26A$
 $I_{dc} = 17.5A$
 $DCR = 4.2mohm$
- 5. MOSFET Spec:

- 6. Frequency:
 $F = 1MHz$ (R1705=Open)
- 7. OCP:
Min : 6A / Typ : 7.5A

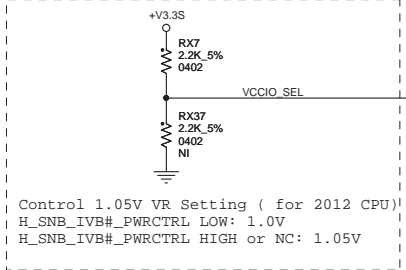


VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

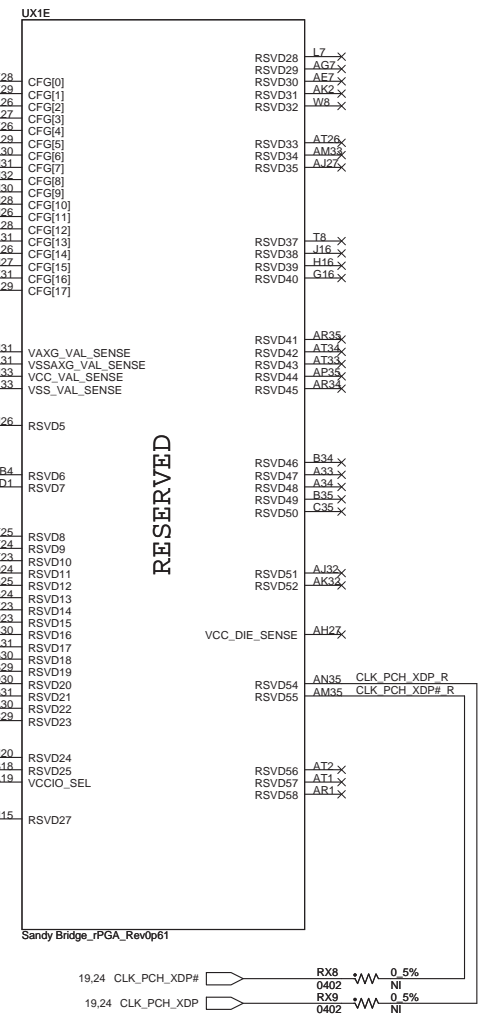
+V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43



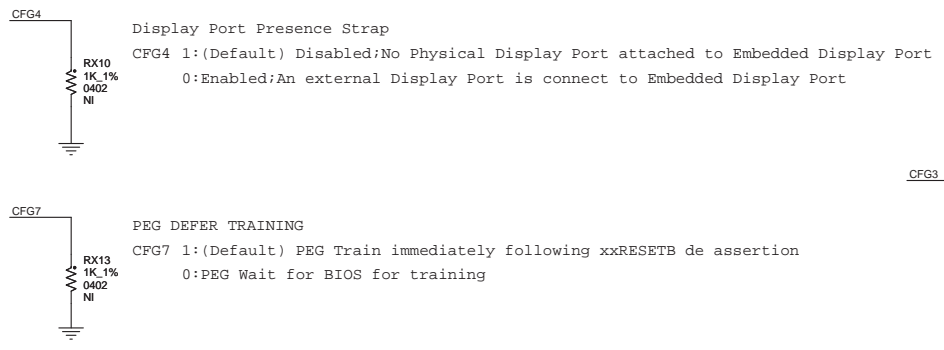
Trace width : PEG_COMP from CPU socket PIN J22 and H22 to Res RX1 is 4mils PEG_COMP from CPU socket PIN J21 to Res RX1 is 12mils



Control 1.05V VR Setting (for 2012 CPU) H_SNB_IVB#_PWRCTRL LOW: 1.0V H_SNB_IVB#_PWRCTRL HIGH or NC: 1.05V

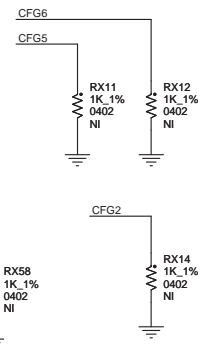


RESERVED



Display Port Presence Strap
CFG4 1:(Default) Disabled/No Physical Display Port attached to Embedded Display Port
0:Enabled/An external Display Port is connect to Embedded Display Port

PEG DEFER TRAINING
CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion
0:PEG Wait for BIOS for training



PCIE Port Bifurcation Straps
CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled)

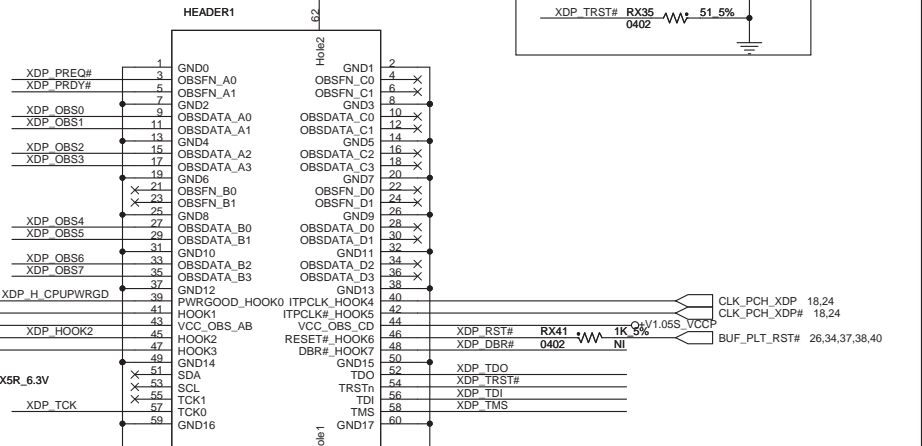
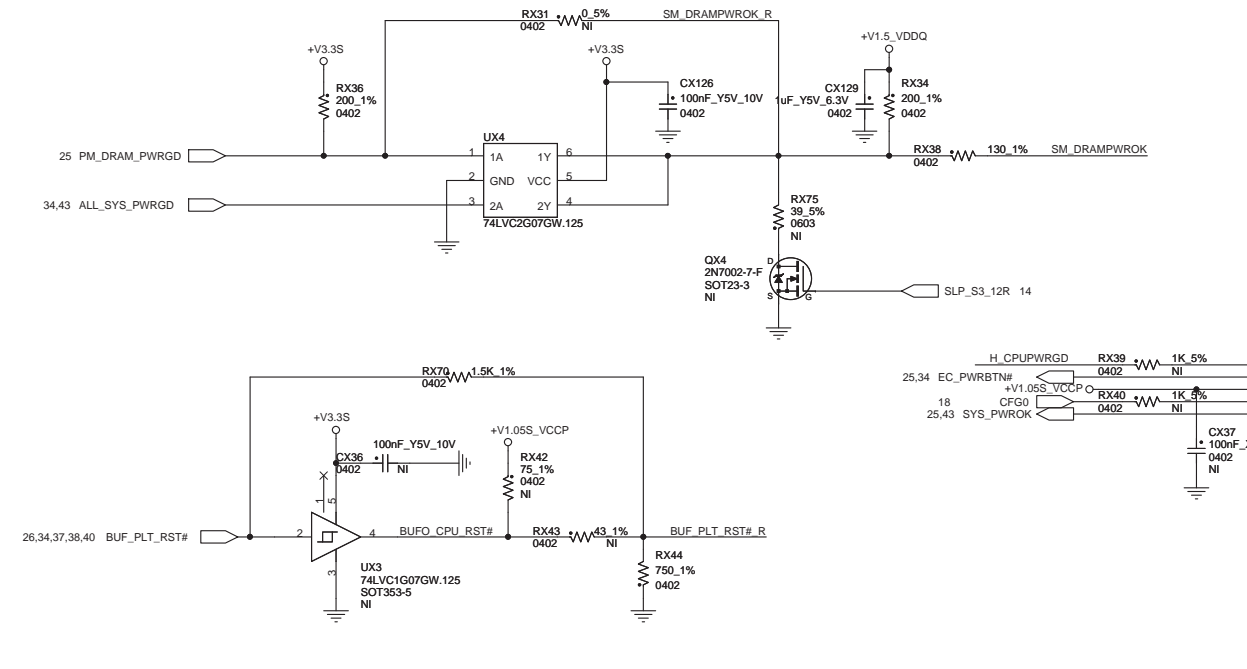
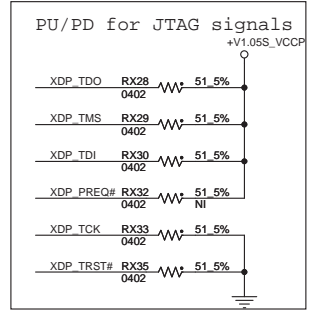
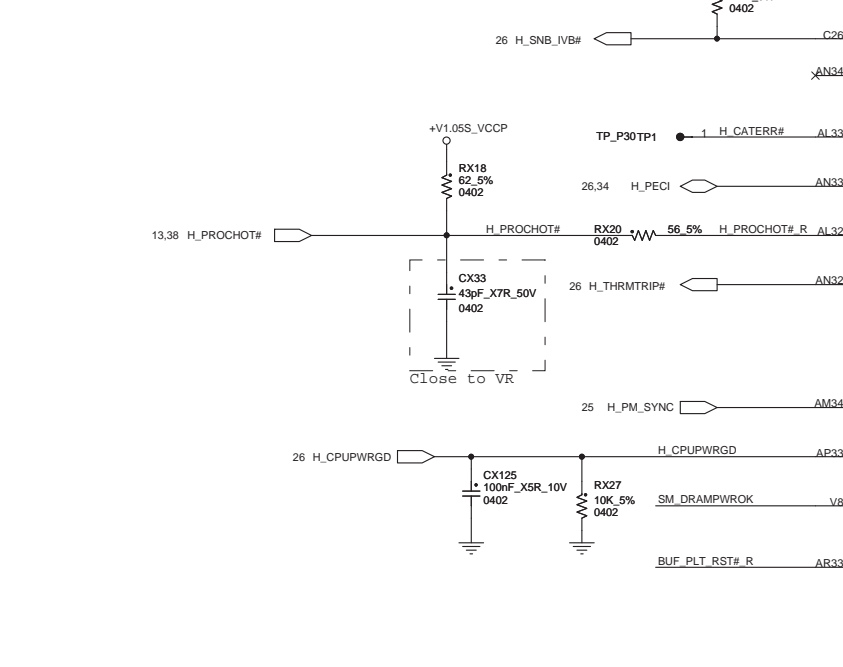
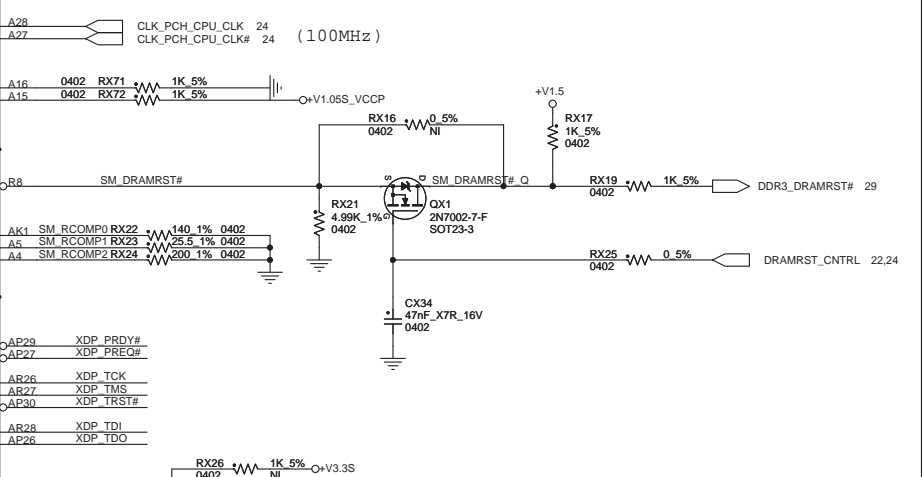
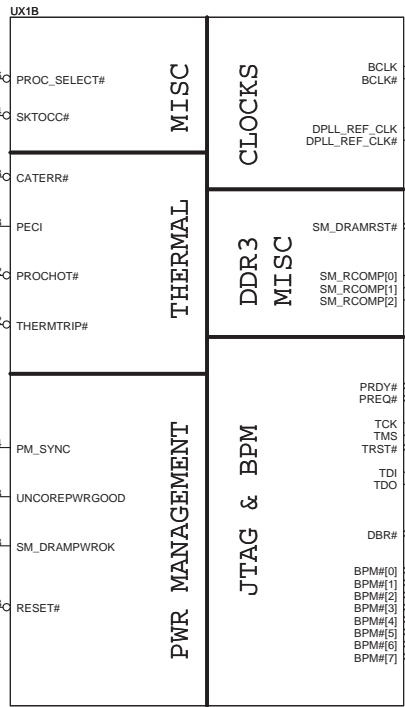
PEG Static Lane Reversal - CFG2 is for the 16x
CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition
0:Lane Reversed

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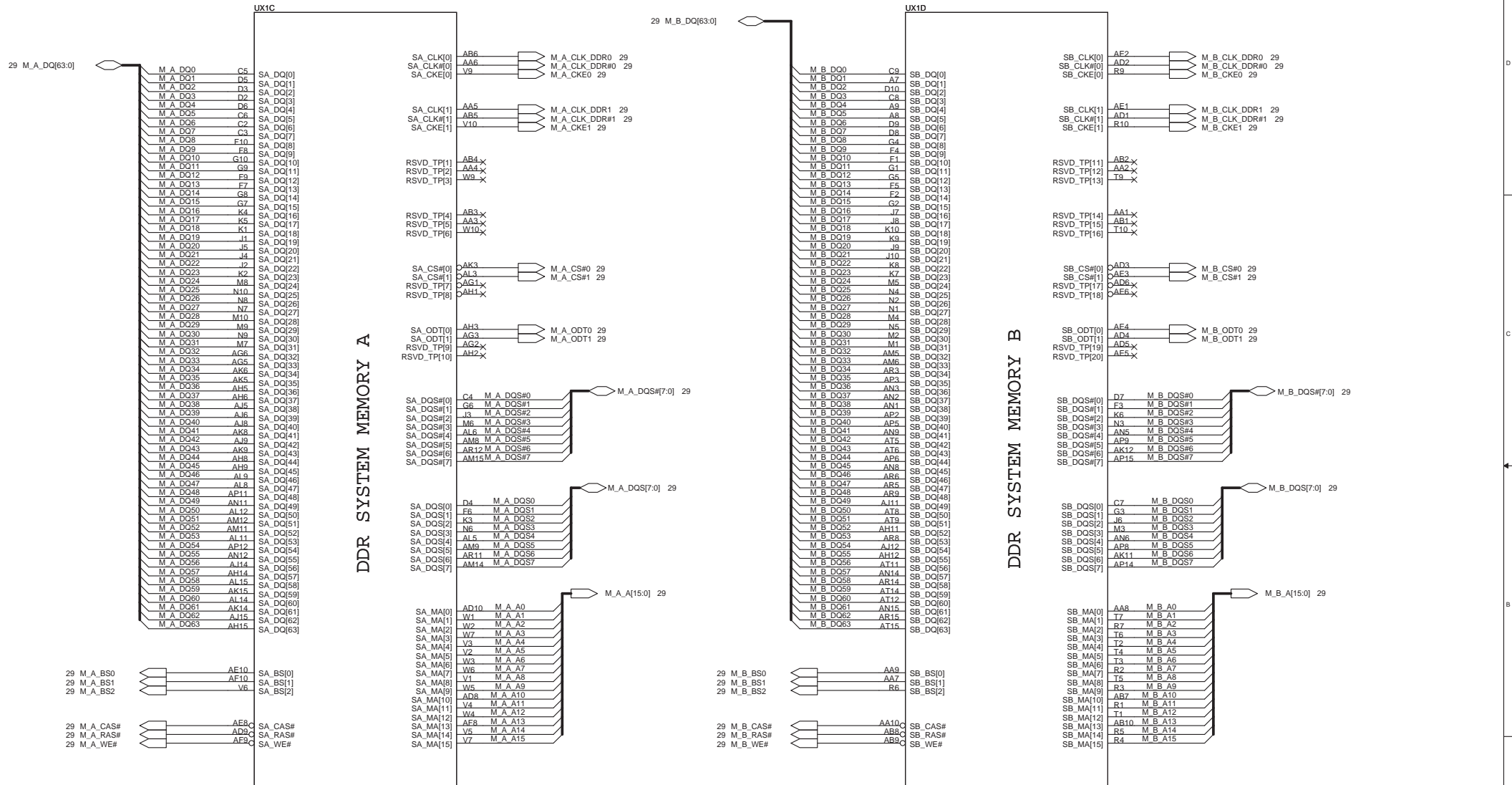
Title: **PROCESSOR(1 of 5)**

Size: Document Number
Custom **CHICAGO** Rev: MV

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Sandy Bridge_rPGA_RevOp61

Sandy Bridge_rPGA_RevOp61

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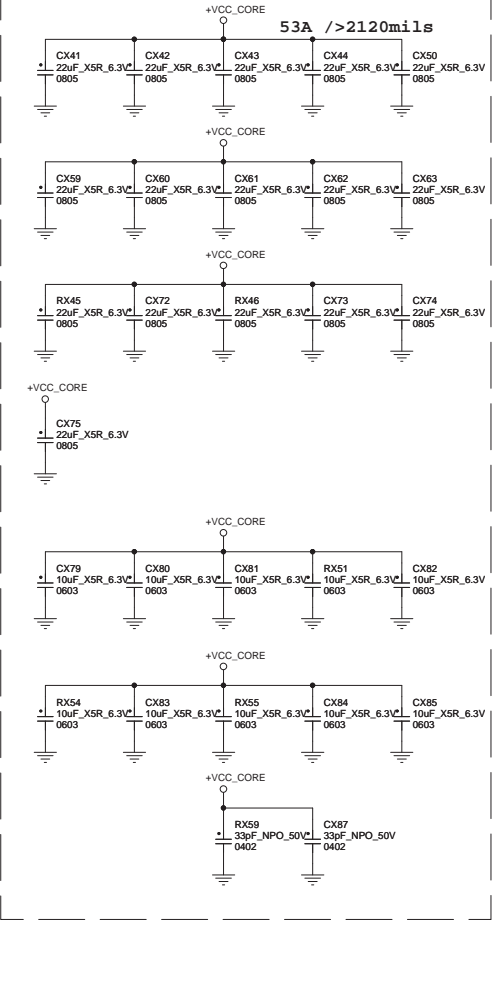
Title: **PROCESSOR(3 of 5)**

Size: Document Number
 Custom **CHICAGO** Rev **MV**

Page Modified: Tuesday, March 08, 2011 08:29:00 (UTC/GMT) Sheet 20 of 43

+V1.05S_VCCP O +V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43
+VCC_CORE O +VCC_CORE 13,18,43

FOR VCC:
4x 330 µF Bottom Edge,
10x 0603 10 µF Bottom Cavity,
8x 0805 22 µF Top Cavity,
8x 0805 22 µF Top Edge,



- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AE35 VCC11
- AE34 VCC12
- AE33 VCC13
- AE32 VCC14
- AE31 VCC15
- AE30 VCC16
- AE29 VCC17
- AE28 VCC18
- AE27 VCC19
- AE26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC34 VCC31
- AC33 VCC32
- AC32 VCC33
- AC31 VCC34
- AC30 VCC35
- AC29 VCC36
- AC28 VCC37
- AC27 VCC38
- AC26 VCC39
- AA35 VCC40
- AA34 VCC41
- AA33 VCC42
- AA32 VCC43
- AA31 VCC44
- AA30 VCC45
- AA29 VCC46
- AA28 VCC47
- AA27 VCC48
- AA26 VCC49
- Y35 VCC50
- Y34 VCC51
- Y33 VCC52
- Y32 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- V35 VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- U34 VCC70
- U33 VCC71
- U32 VCC72
- U31 VCC73
- U30 VCC74
- U29 VCC75
- U28 VCC76
- U27 VCC77
- U26 VCC78
- R35 VCC79
- R34 VCC80
- R33 VCC81
- R32 VCC82
- R31 VCC83
- R30 VCC84
- R29 VCC85
- R28 VCC86
- R27 VCC87
- R26 VCC88
- P34 VCC89
- P33 VCC90
- P32 VCC91
- P31 VCC92
- P30 VCC93
- P29 VCC94
- P28 VCC95
- P27 VCC96
- P26 VCC97
- P25 VCC98
- P24 VCC99
- P23 VCC100

POWER

PEG AND DDR

CORE SUPPLY

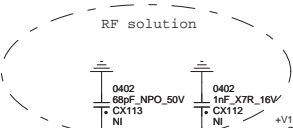
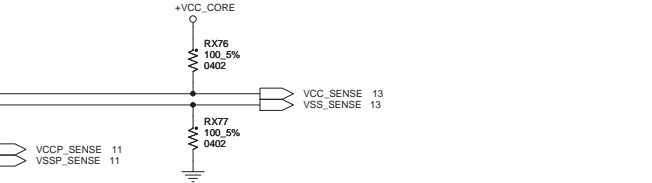
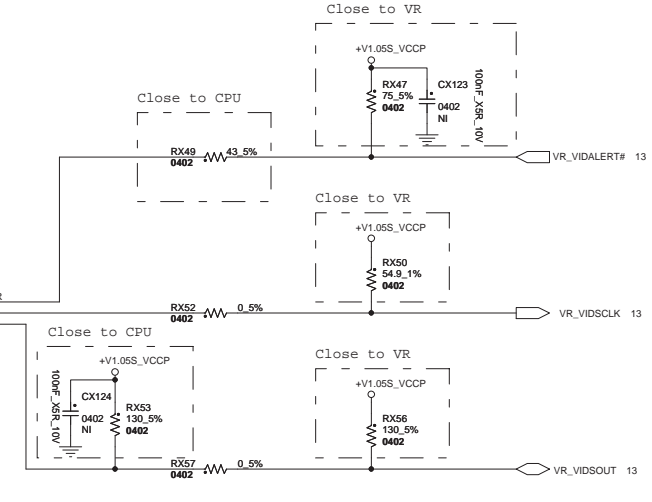
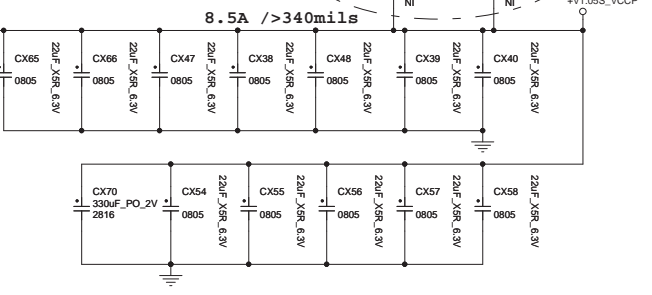
SVID

SENSE LINES

- AH13 VCCIO1
- AH10 VCCIO2
- AC10 VCCIO3
- Y10 VCCIO4
- V10 VCCIO5
- L10 VCCIO6
- F10 VCCIO7
- L10 VCCIO8
- J14 VCCIO9
- J13 VCCIO10
- J12 VCCIO11
- J11 VCCIO12
- H14 VCCIO13
- H12 VCCIO14
- H11 VCCIO15
- G14 VCCIO16
- G13 VCCIO17
- G12 VCCIO18
- E14 VCCIO19
- F13 VCCIO20
- F12 VCCIO21
- F11 VCCIO22
- E14 VCCIO23
- E11 VCCIO24
- D14 VCCIO25
- D13 VCCIO26
- D12 VCCIO27
- D11 VCCIO28
- C14 VCCIO29
- C13 VCCIO30
- C12 VCCIO31
- C11 VCCIO32
- B14 VCCIO33
- B12 VCCIO34
- A14 VCCIO35
- A13 VCCIO36
- A12 VCCIO37
- A11 VCCIO38
- J23 VCCIO39

- AJ29 VR_SVID_ALERT# R
- AJ30 VR_SVID_CLK R
- AJ28 VR_SVID_DATA R
- AJ35 VCC_SENSE
- AJ34 VSS_SENSE
- B10 VCCIO_SENSE
- A10 VSSIO_SENSE

FOR VCCIO:
2x 330 µF,
5x 0805 22 µF Bottom Cavity,
7x 0805 22 µF Top Cavity,

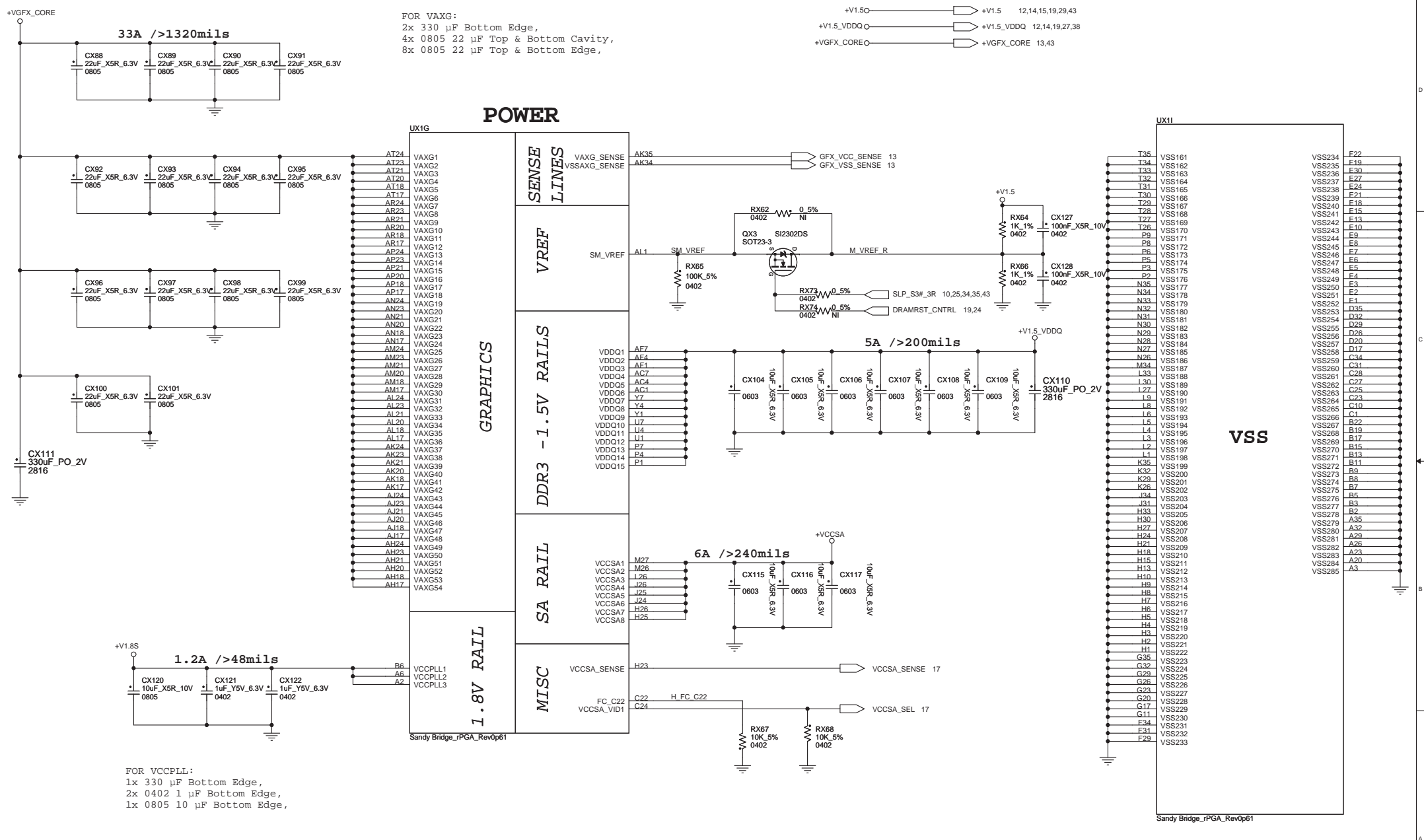


- AT35 VSS1
- AT32 VSS2
- AT29 VSS3
- AT27 VSS4
- AT25 VSS5
- AT22 VSS6
- AT19 VSS7
- AT16 VSS8
- AT13 VSS9
- AT7 VSS10
- AT7 VSS11
- AT4 VSS12
- AT3 VSS13
- AR25 VSS14
- AR22 VSS15
- AR19 VSS16
- AR16 VSS17
- AR13 VSS18
- AR10 VSS19
- AR7 VSS20
- AR4 VSS21
- AR2 VSS22
- AP34 VSS23
- AP31 VSS24
- AP28 VSS25
- AP25 VSS26
- AP22 VSS27
- AP19 VSS28
- AP16 VSS29
- AP13 VSS30
- AP10 VSS31
- AP7 VSS32
- AP4 VSS33
- AP1 VSS34
- AN30 VSS35
- AN27 VSS36
- AN25 VSS37
- AN22 VSS38
- AN19 VSS39
- AN16 VSS40
- AN13 VSS41
- AN10 VSS42
- AN7 VSS43
- AN4 VSS44
- AM29 VSS45
- AM25 VSS46
- AM22 VSS47
- AM19 VSS48
- AM16 VSS49
- AM13 VSS50
- AM10 VSS51
- AM7 VSS52
- AM4 VSS53
- AM2 VSS54
- AM2 VSS55
- AM1 VSS56
- AL34 VSS57
- AL31 VSS58
- AL28 VSS59
- AL25 VSS60
- AL22 VSS61
- AL19 VSS62
- AL16 VSS63
- AL13 VSS64
- AL10 VSS65
- AL7 VSS66
- AL4 VSS67
- AL2 VSS68
- AK33 VSS69
- AK30 VSS70
- AK27 VSS71
- AK25 VSS72
- AK22 VSS73
- AK19 VSS74
- AK16 VSS75
- AK13 VSS76
- AK10 VSS77
- AK7 VSS78
- AK4 VSS79
- AL25 VSS80
- VSS81 AJ22
- VSS82 AJ19
- VSS83 AJ16
- VSS84 AJ13
- VSS85 AJ10
- VSS86 AJ7
- VSS87 AJ4
- VSS88 AJ3
- VSS89 AJ1
- VSS90 AJ35
- VSS91 AH35
- VSS92 AH34
- VSS93 AH32
- VSS94 AH30
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- VSS96 AH28
- VSS97 AH27
- VSS98 AH25
- VSS99 AH22
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- VSS101 AH16
- VSS102 AH7
- VSS103 AG9
- VSS104 AG9
- VSS105 AG8
- VSS106 AE6
- VSS107 AE6
- VSS108 AF6
- VSS109 AE2
- VSS110 AE2
- VSS111 AE35
- VSS112 AE34
- VSS113 AE33
- VSS114 AE32
- VSS115 AE31
- VSS116 AE29
- VSS117 AE28
- VSS118 AE28
- VSS119 AE27
- VSS120 AE26
- VSS121 AE9
- VSS122 AD7
- VSS123 AC9
- VSS124 AC8
- VSS125 AC6
- VSS126 AC6
- VSS127 AC5
- VSS128 AC2
- VSS129 AB35
- VSS130 AB34
- VSS131 AB33
- VSS132 AB32
- VSS133 AB31
- VSS134 AB30
- VSS135 AB29
- VSS136 AB28
- VSS137 AB27
- VSS138 AB26
- VSS139 Y9
- VSS140 Y6
- VSS141 Y6
- VSS142 Y5
- VSS143 Y3
- VSS144 Y2
- VSS145 W35
- VSS146 W34
- VSS147 W33
- VSS148 W32
- VSS149 W31
- VSS150 W30
- VSS151 W29
- VSS152 W28
- VSS153 W27
- VSS154 W26
- VSS155 U9
- VSS156 U6
- VSS157 U6
- VSS158 U5
- VSS159 U3
- VSS160 U2

VSS

Sandy Bridge_rPGA_Rev0p61

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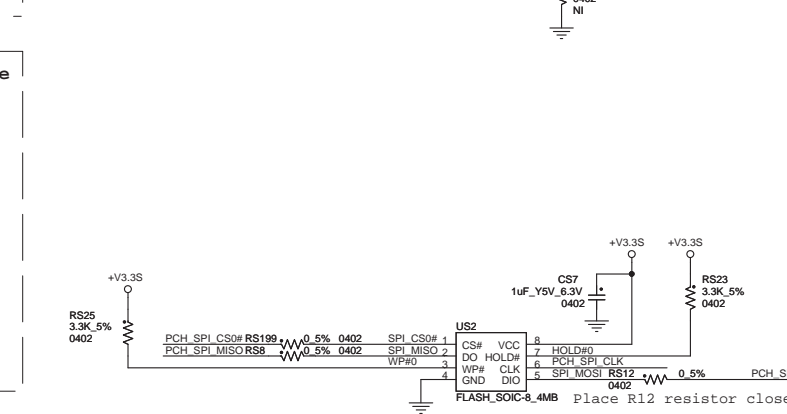
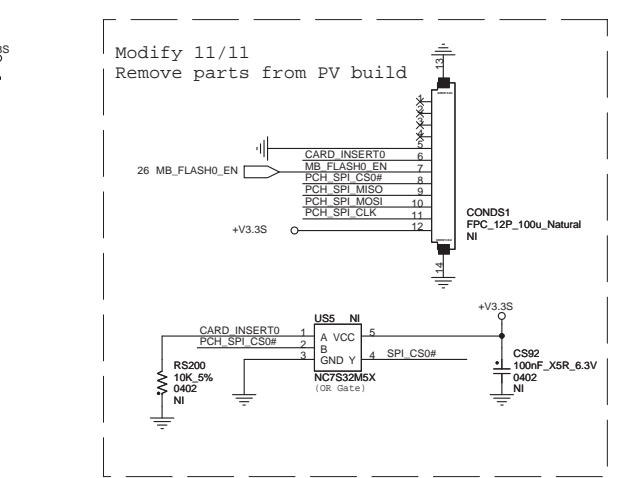
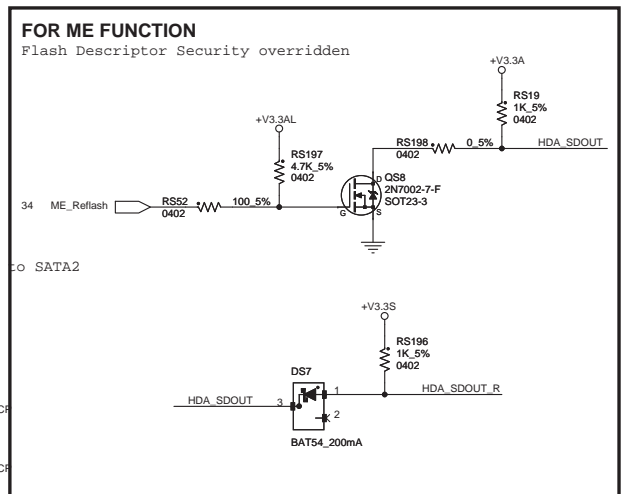
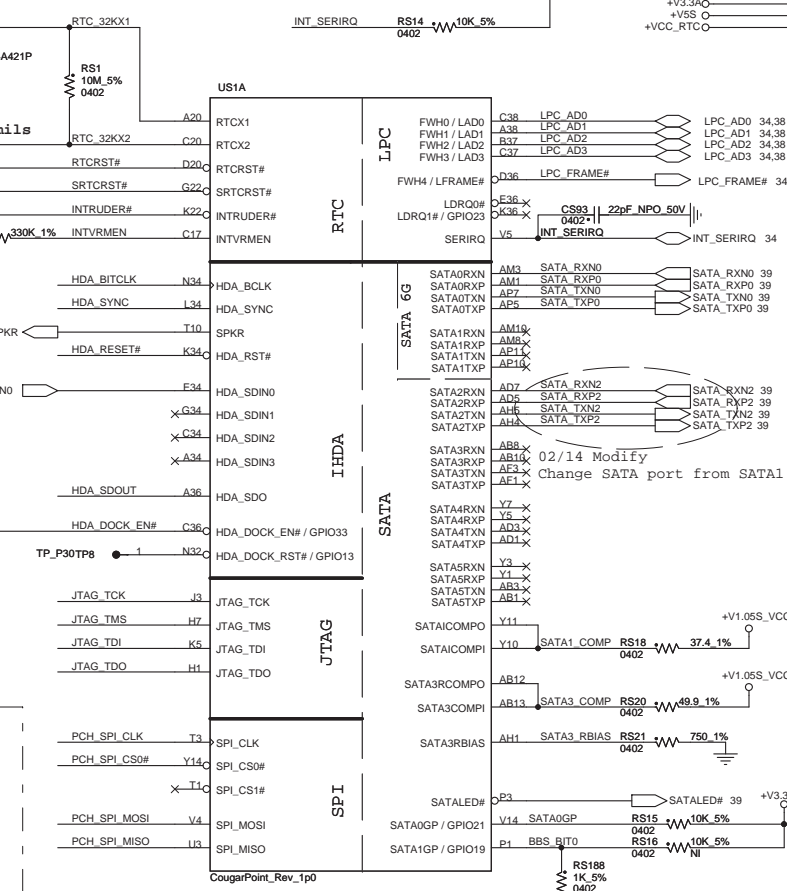
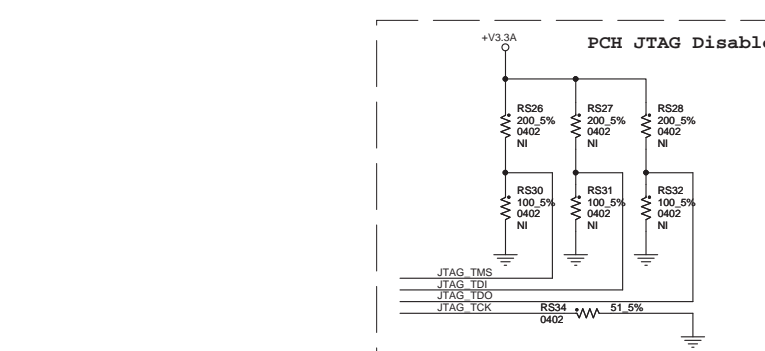
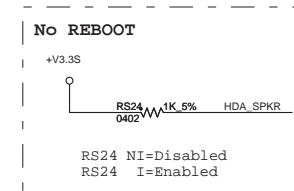
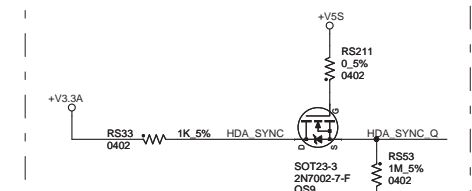
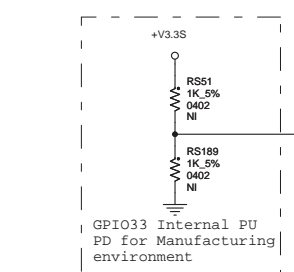
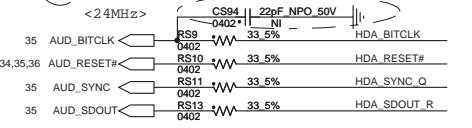
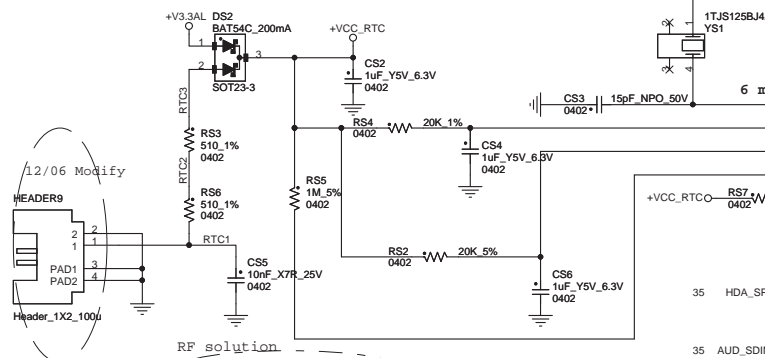
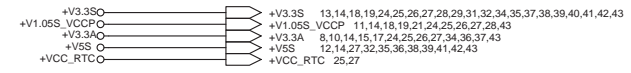
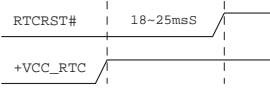
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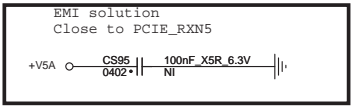
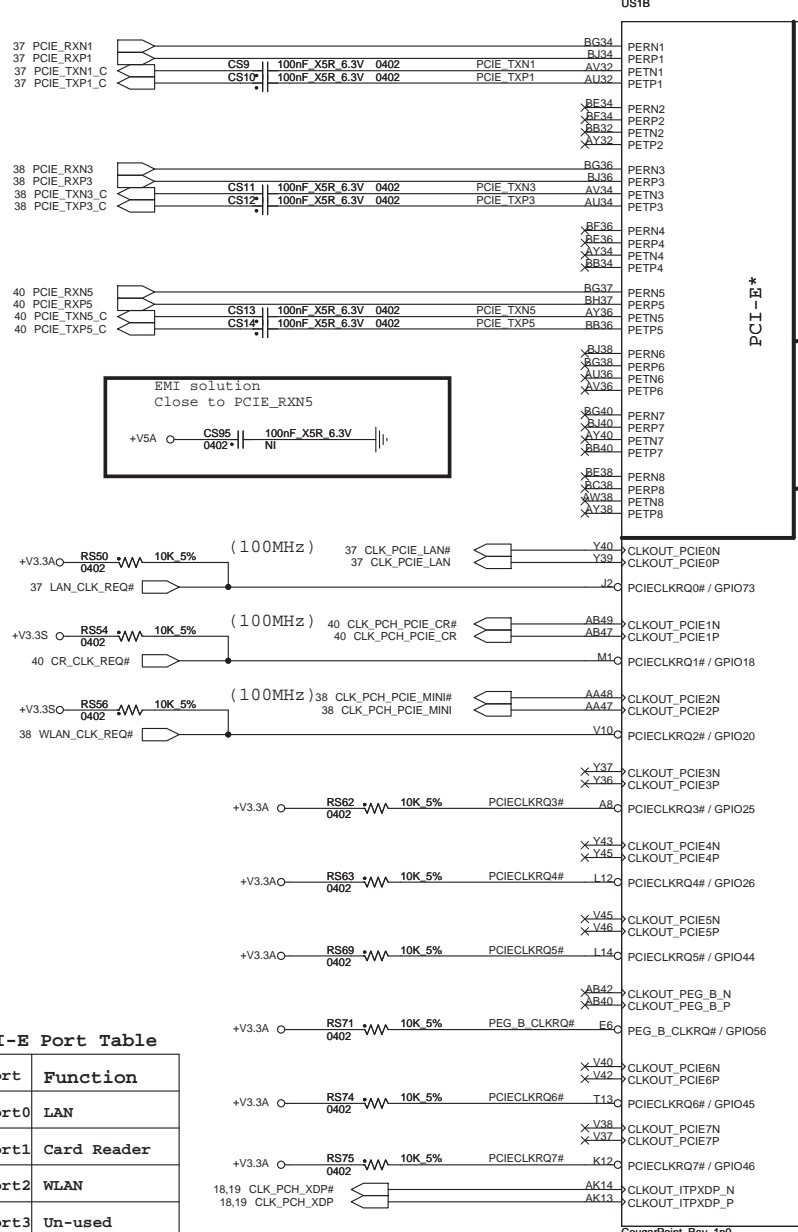
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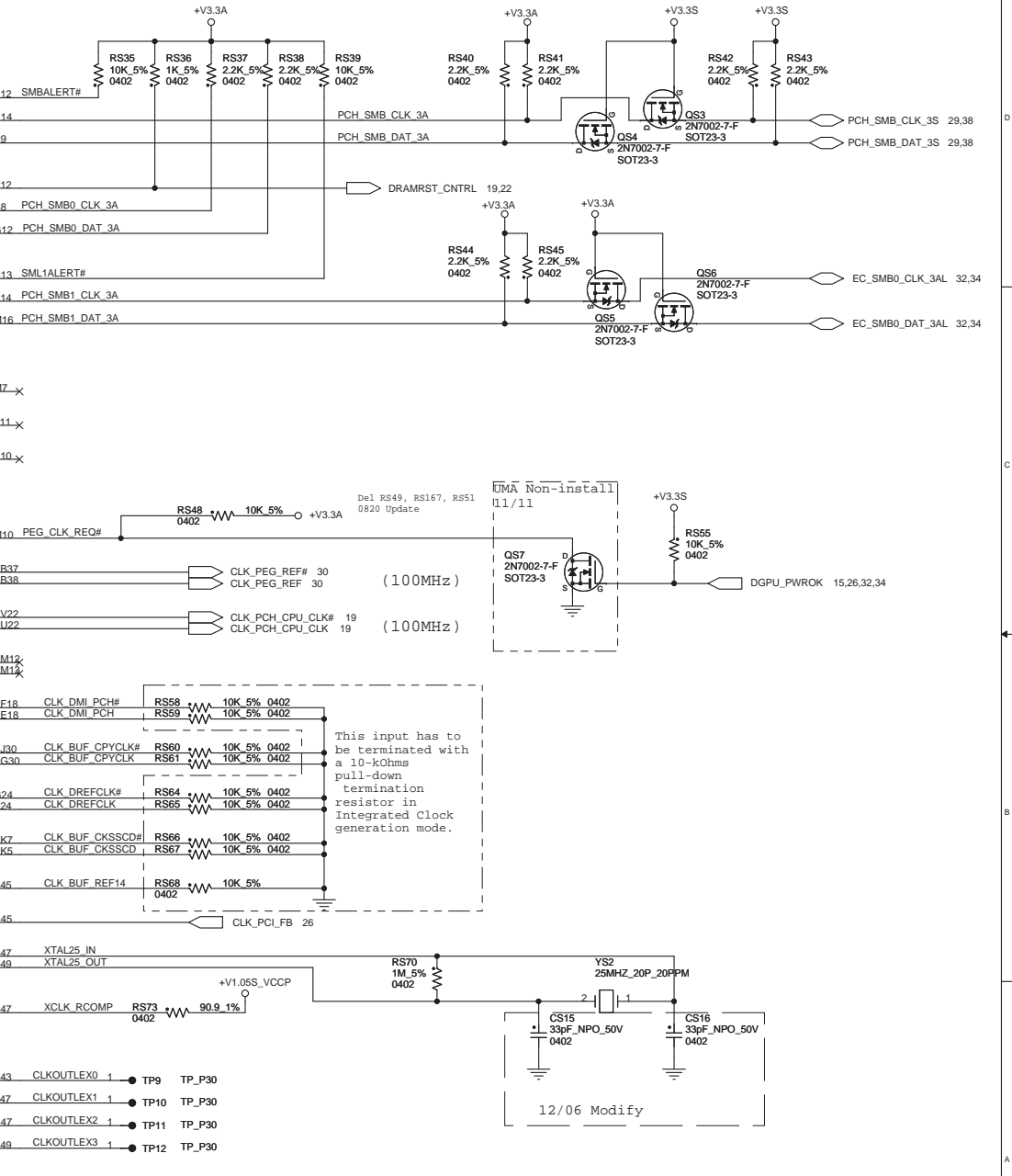
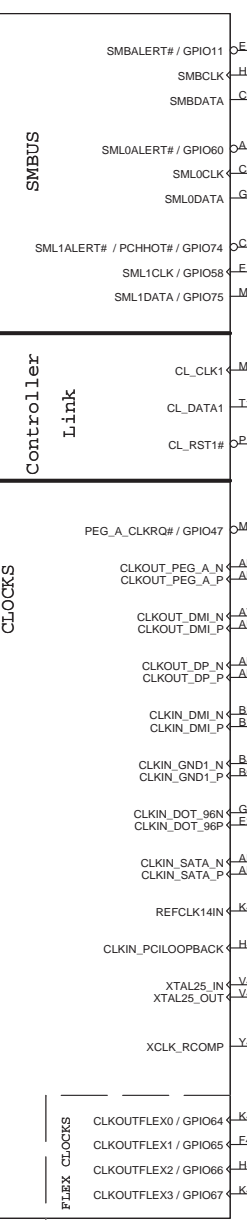
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PCI-E Port Table

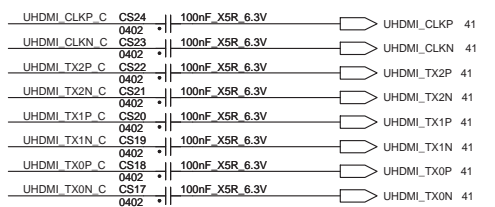
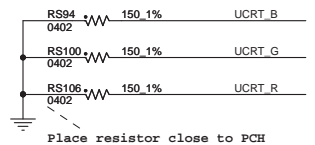
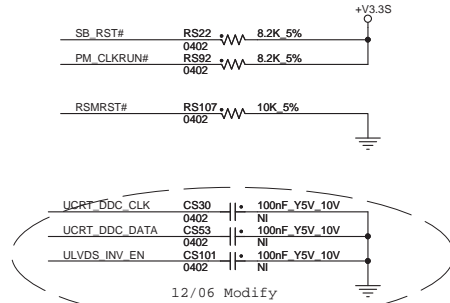
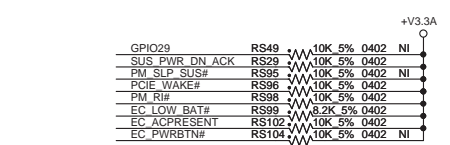
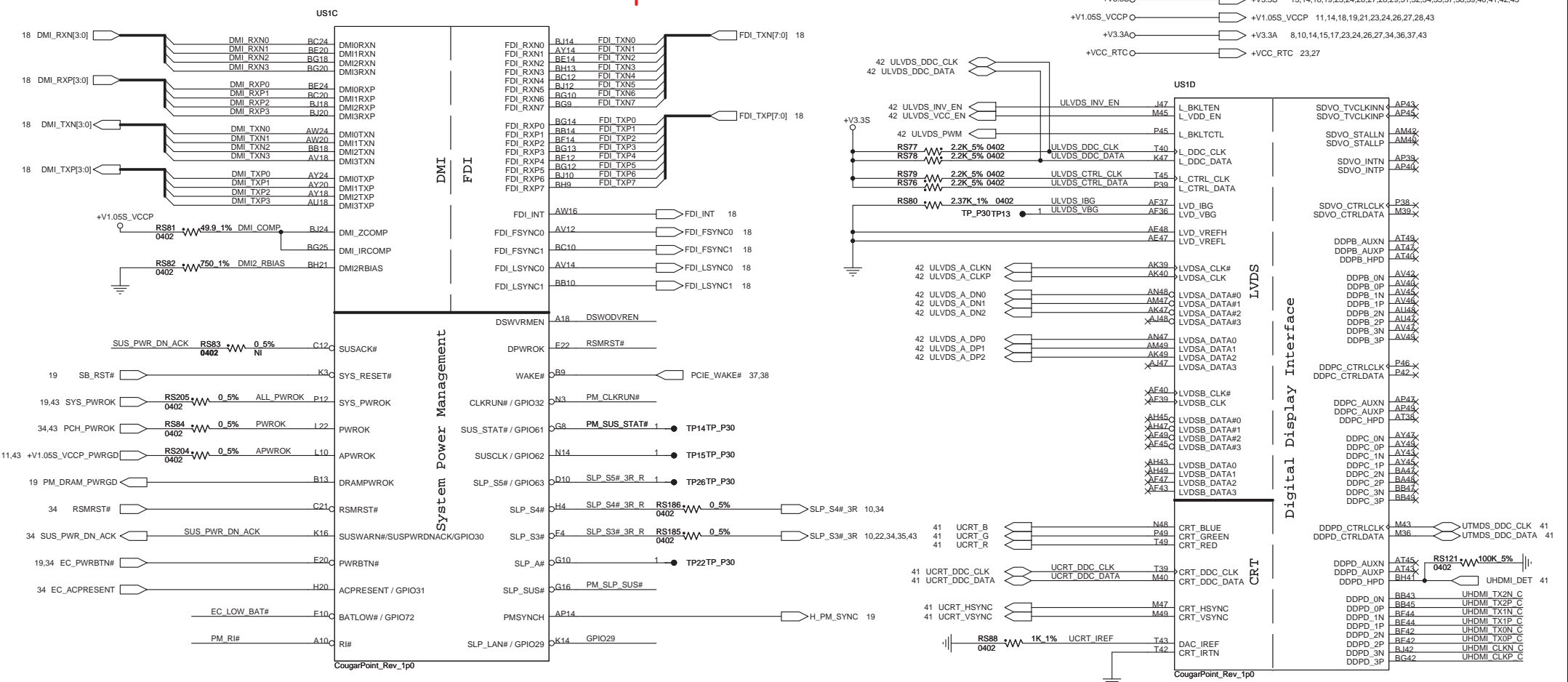
Port	Function
Port0	LAN
Port1	Card Reader
Port2	WLAN
Port3	Un-used
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used



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DSWODVREN - on Die DSW VR Enable

RS97	RS103	
I	NI	Enabled
NI	I	Disabled

Modify CS30/CS53/CS101 to non-stuff on 01/11

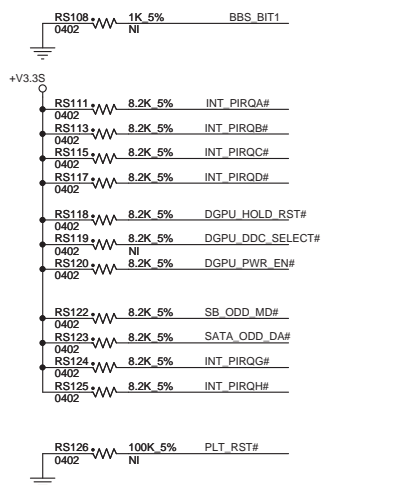
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Title: **CougarPoint(3 of 6)**

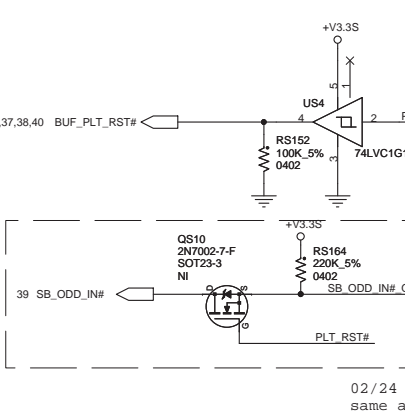
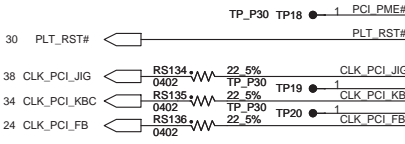
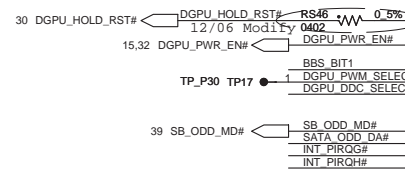
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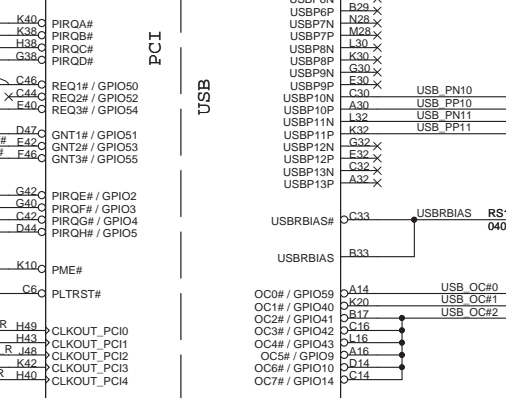
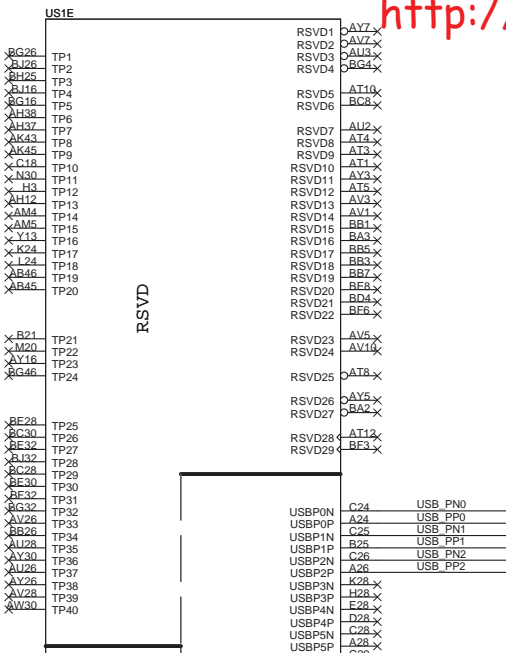
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



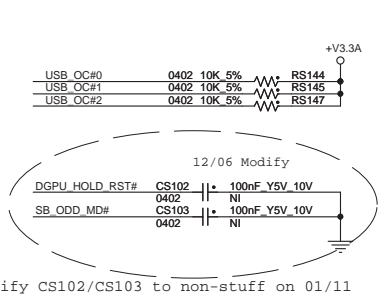
Del RS121 8.2Kohm to +V3.3S
0820 Update



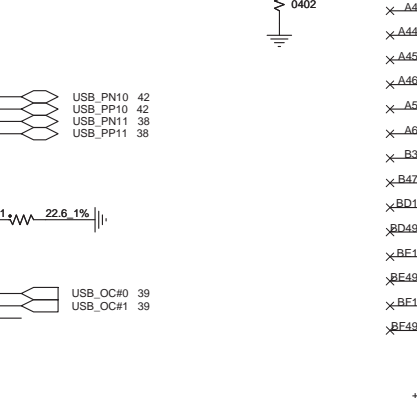
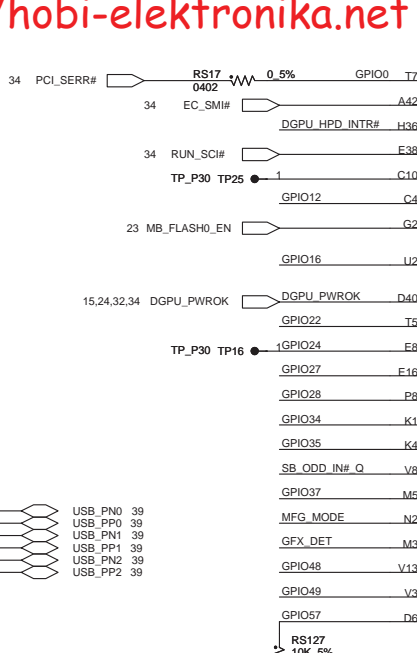
02/24 Modify same as the PV build



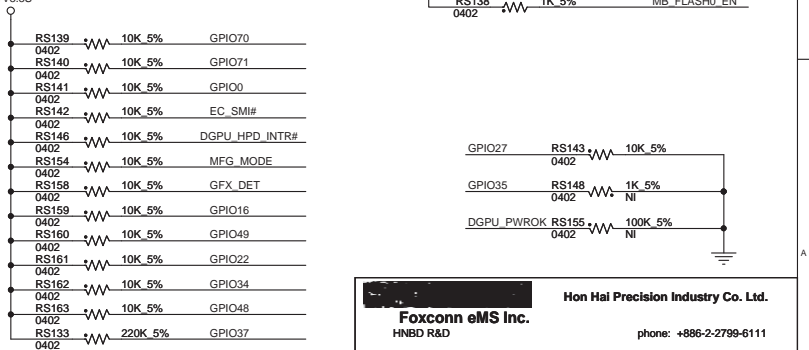
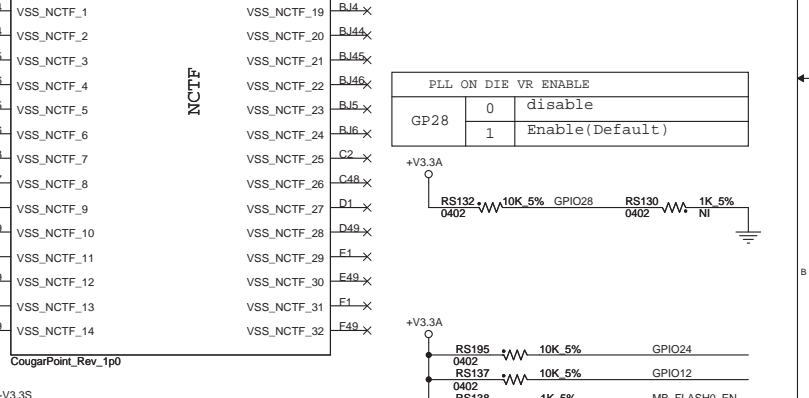
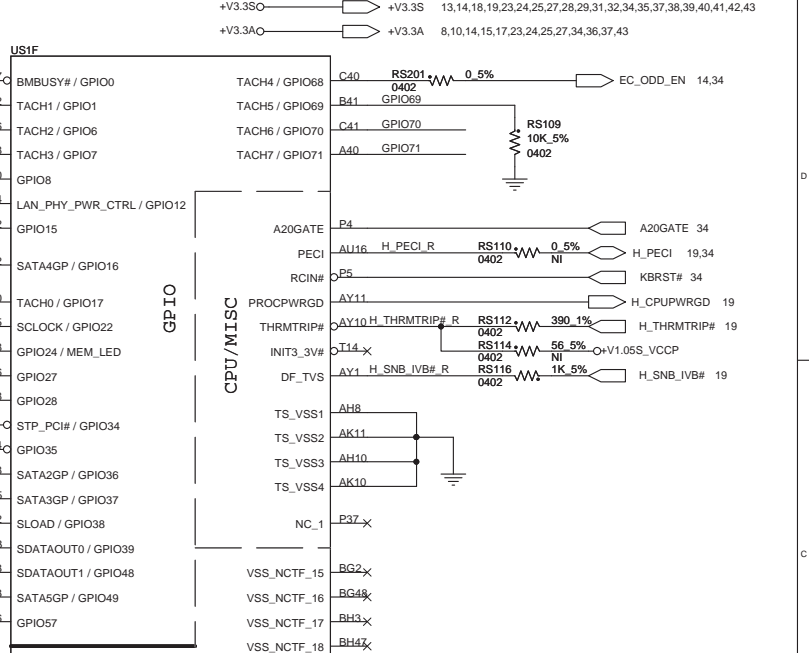
CougarPoint_Rev_1p0



Modify CS102/CS103 to non-stuff on 01/11



USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	
PORT-3	NC	OC1#
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	



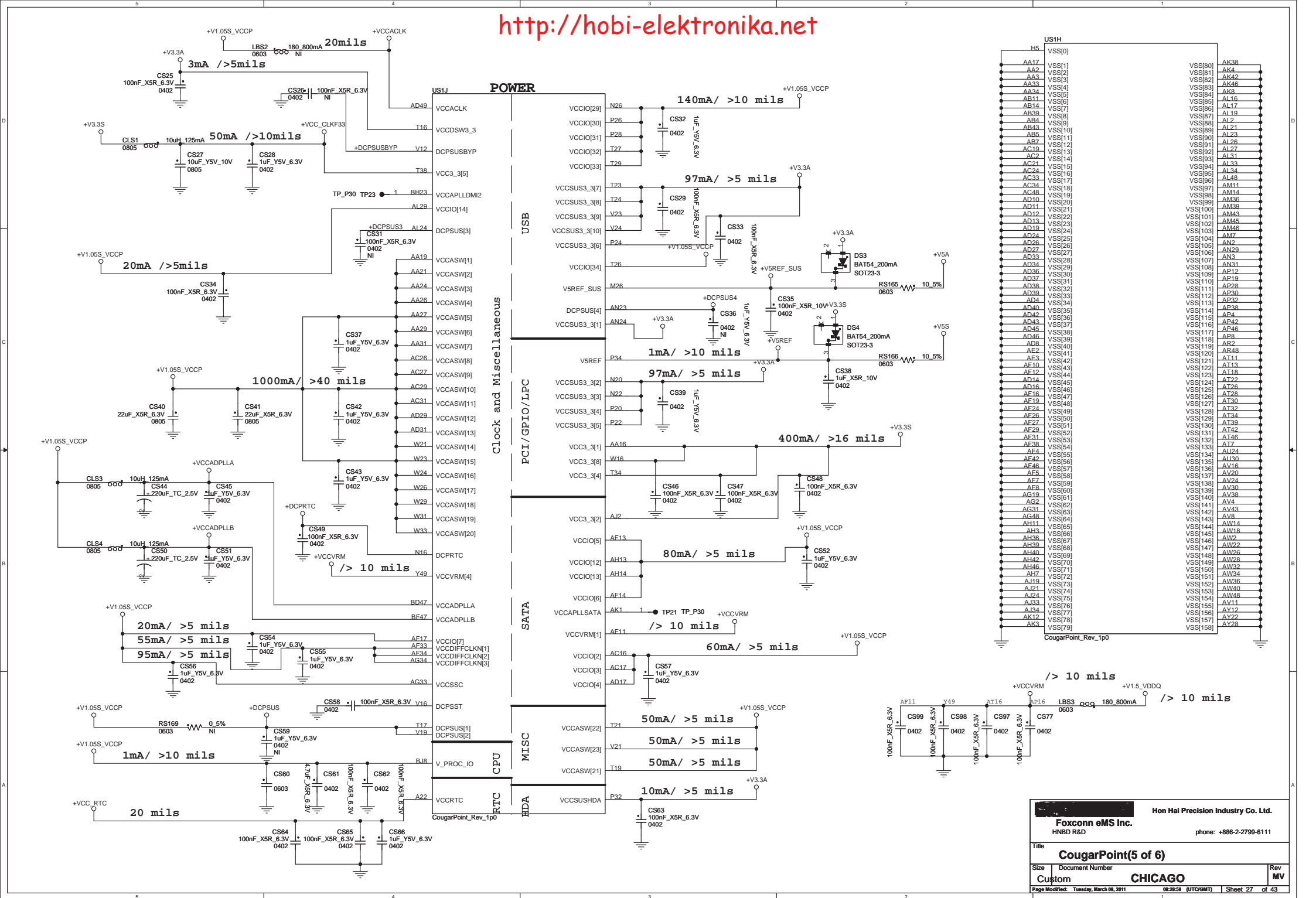
PLL ON DIE VR ENABLE		
GP28	0	disable
	1	Enable(Default)

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US1H		
H5	VSS1[0]	
AA17	VSS1[1]	VSS8[0] AK38
AA2	VSS1[2]	VSS8[1] AK4
AA3	VSS1[3]	VSS8[2] AK42
AA33	VSS1[4]	VSS8[3] AK46
AA34	VSS1[5]	VSS8[4] AK6
AB11	VSS1[6]	VSS8[5] AL16
AB14	VSS1[7]	VSS8[6] AL17
AB39	VSS1[8]	VSS8[7] AL19
AB4	VSS1[9]	VSS8[8] AL2
AB43	VSS1[10]	VSS8[9] AL21
AB5	VSS1[11]	VSS8[10] AL23
AB7	VSS1[12]	VSS8[11] AL26
AC19	VSS1[13]	VSS8[12] AL27
AC2	VSS1[14]	VSS8[13] AL31
AC21	VSS1[15]	VSS8[14] AL33
AC24	VSS1[16]	VSS8[15] AL34
AC33	VSS1[17]	VSS8[16] AL48
AC34	VSS1[18]	VSS8[17] AM11
AC48	VSS1[19]	VSS8[18] AM14
AD10	VSS1[20]	VSS8[19] AM36
AD11	VSS1[21]	VSS8[20] AM39
AD12	VSS1[22]	VSS8[21] AM45
AD13	VSS1[23]	VSS8[22] AM46
AD19	VSS1[24]	VSS8[23] AM7
AD24	VSS1[25]	VSS8[24] AN29
AD27	VSS1[26]	VSS8[25] AN3
AD33	VSS1[27]	VSS8[26] AN31
AD34	VSS1[28]	VSS8[27] AP19
AD38	VSS1[29]	VSS8[28] AP28
AD39	VSS1[30]	VSS8[29] AP30
AD4	VSS1[31]	VSS8[30] AP32
AD40	VSS1[32]	VSS8[31] AP34
AD42	VSS1[33]	VSS8[32] AP42
AD43	VSS1[34]	VSS8[33] AP46
AD45	VSS1[35]	VSS8[34] AP6
AD46	VSS1[36]	VSS8[35] AR2
AD8	VSS1[37]	VSS8[36] AR48
AE2	VSS1[38]	VSS8[37] AT11
AE3	VSS1[39]	VSS8[38] AT13
AE10	VSS1[40]	VSS8[39] AT18
AE12	VSS1[41]	VSS8[40] AT22
AE14	VSS1[42]	VSS8[41] AT26
AE16	VSS1[43]	VSS8[42] AT28
AE19	VSS1[44]	VSS8[43] AT30
AE24	VSS1[45]	VSS8[44] AT32
AE26	VSS1[46]	VSS8[45] AT34
AE27	VSS1[47]	VSS8[46] AT39
AE29	VSS1[48]	VSS8[47] AT42
AE31	VSS1[49]	VSS8[48] AT46
AE38	VSS1[50]	VSS8[49] AT7
AF4	VSS1[51]	VSS8[50] AU24
AF42	VSS1[52]	VSS8[51] AU30
AF46	VSS1[53]	VSS8[52] AV16
AF5	VSS1[54]	VSS8[53] AV20
AF7	VSS1[55]	VSS8[54] AV24
AF8	VSS1[56]	VSS8[55] AV30
AG19	VSS1[57]	VSS8[56] AV4
AG2	VSS1[58]	VSS8[57] AV44
AG31	VSS1[59]	VSS8[58] AV43
AG48	VSS1[60]	VSS8[59] AV8
AH11	VSS1[61]	VSS8[60] AW14
AH3	VSS1[62]	VSS8[61] AW2
AH36	VSS1[63]	VSS8[62] AW22
AH39	VSS1[64]	VSS8[63] AW26
AH40	VSS1[65]	VSS8[64] AW28
AH42	VSS1[66]	VSS8[65] AW32
AH46	VSS1[67]	VSS8[66] AW34
AH7	VSS1[68]	VSS8[67] AW36
AJ19	VSS1[69]	VSS8[68] AW40
AJ21	VSS1[70]	VSS8[69] AW48
AJ24	VSS1[71]	VSS8[70] AV11
AJ33	VSS1[72]	VSS8[71] AY12
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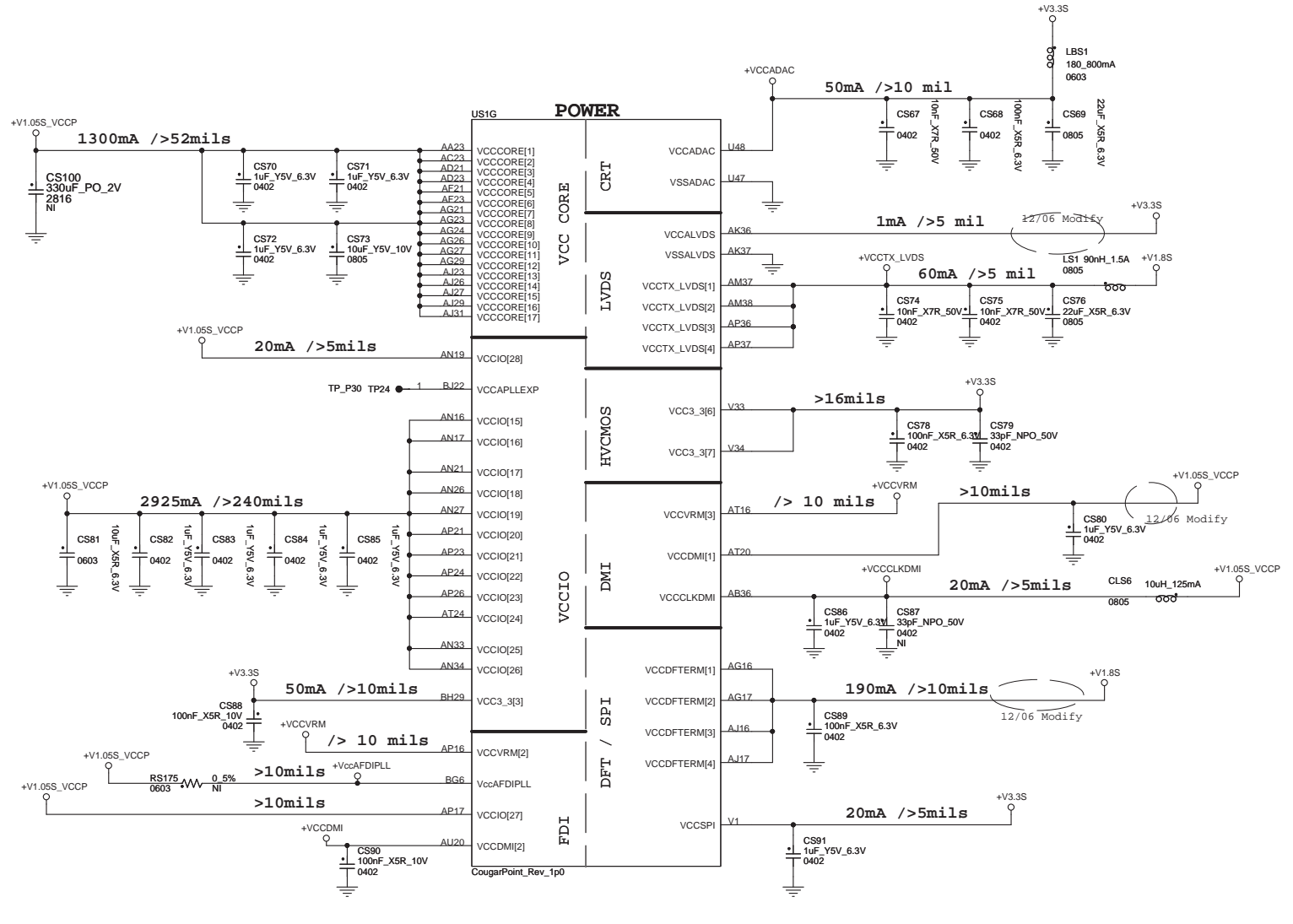
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US11			
AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K39
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L26
B31	VSS168	VSS268	L28
B35	VSS169	VSS269	L36
B39	VSS170	VSS270	L48
B7	VSS171	VSS271	M12
F45	VSS172	VSS272	M16
BB12	VSS173	VSS273	M18
BB16	VSS174	VSS274	M22
BB20	VSS175	VSS275	M24
BB22	VSS176	VSS276	M30
BB24	VSS177	VSS277	M32
BB28	VSS178	VSS278	M34
BB30	VSS179	VSS279	M38
BB38	VSS180	VSS280	M4
BB4	VSS181	VSS281	M42
BB46	VSS182	VSS282	M46
BC14	VSS183	VSS283	M8
BC18	VSS184	VSS284	M8
BC2	VSS185	VSS285	N18
BC22	VSS186	VSS286	N47
BC26	VSS187	VSS287	P11
BC32	VSS188	VSS288	P18
BC34	VSS189	VSS289	P33
BC36	VSS190	VSS290	P40
BC40	VSS191	VSS291	P43
BC42	VSS192	VSS292	P47
BC48	VSS193	VSS293	P7
BD46	VSS194	VSS294	P2
BD5	VSS195	VSS295	R48
BE22	VSS196	VSS296	T37
BE26	VSS197	VSS297	T4
BE40	VSS198	VSS298	T4
BE10	VSS199	VSS299	T4
BE12	VSS200	VSS300	W34
BE16	VSS201	VSS301	W46
BE20	VSS202	VSS302	W47
BE22	VSS203	VSS303	X8
BE24	VSS204	VSS304	V11
BE26	VSS205	VSS305	V17
BE28	VSS206	VSS306	V26
BD3	VSS207	VSS307	V27
BE30	VSS208	VSS308	V29
BE38	VSS209	VSS309	V31
BE40	VSS210	VSS310	V36
BE8	VSS211	VSS311	V38
BG17	VSS212	VSS312	V43
BG24	VSS213	VSS313	V7
RG33	VSS214	VSS314	W17
RG44	VSS215	VSS315	W19
BG8	VSS216	VSS316	W2
BH11	VSS217	VSS317	W27
BH15	VSS218	VSS318	W48
BH17	VSS219	VSS319	Y12
BH19	VSS220	VSS320	Y38
H10	VSS221	VSS321	Y4
BH27	VSS222	VSS322	Y42
BH31	VSS223	VSS323	Y46
BH33	VSS224	VSS324	Y8
BH35	VSS225	VSS325	Y8
BH39	VSS226	VSS326	Y29
BH43	VSS227	VSS327	Y41
BH7	VSS228	VSS328	N24
D3	VSS229	VSS329	AJ3
D12	VSS230	VSS330	AD47
D16	VSS231	VSS331	B43
D18	VSS232	VSS332	BE10
D22	VSS233	VSS333	G14
D24	VSS234	VSS334	H16
D26	VSS235	VSS335	T36
D30	VSS236	VSS336	RG22
D32	VSS237	VSS337	RG24
D34	VSS238	VSS338	RG24
D38	VSS239	VSS339	C22
D42	VSS240	VSS340	AP13
DR	VSS241	VSS341	M14
E18	VSS242	VSS342	AP3
G18	VSS243	VSS343	AP1
G20	VSS244	VSS344	BE16
G26	VSS245	VSS345	BC16
G28	VSS246	VSS346	RG28
G38	VSS247	VSS347	BJ28
G48	VSS248	VSS348	
H12	VSS249	VSS349	
H18	VSS250	VSS350	
H22	VSS251	VSS351	
H24	VSS252		
H26	VSS253		
H30	VSS254		
H32	VSS255		
H34	VSS256		
F3	VSS257		
	VSS258		



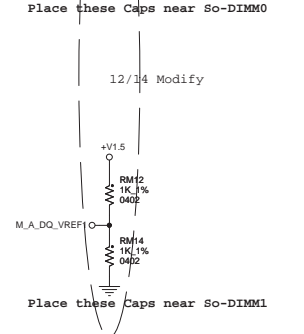
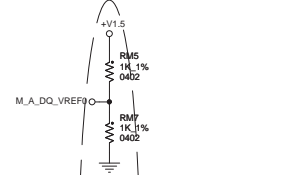
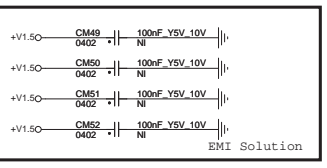
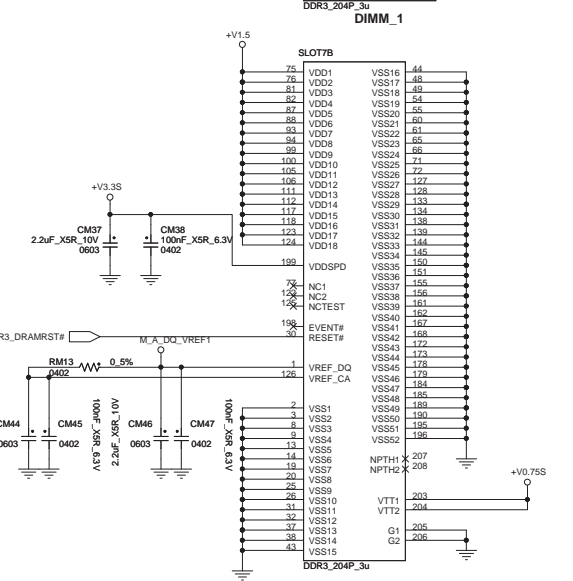
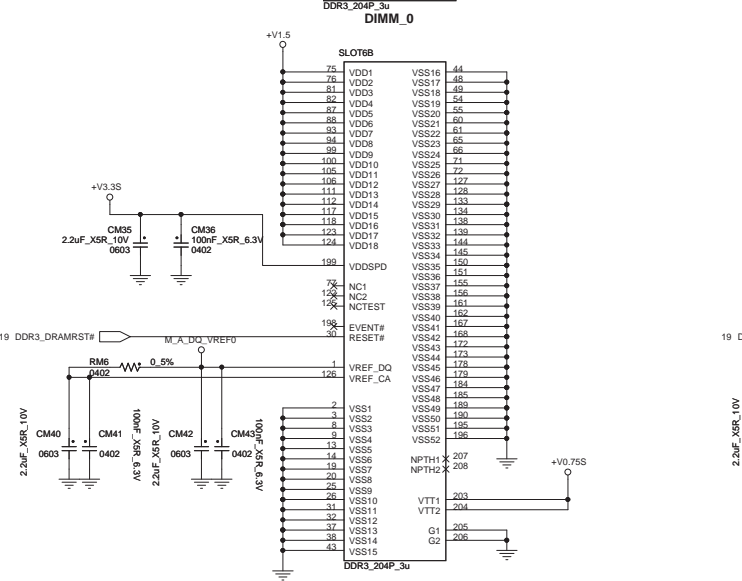
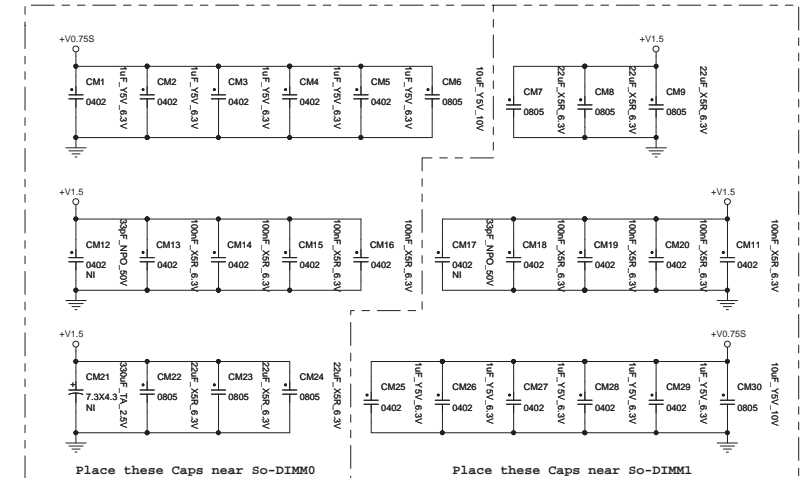
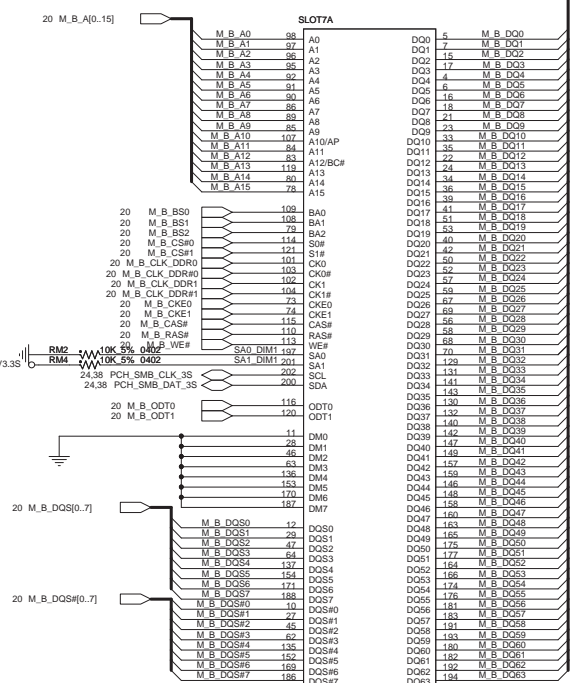
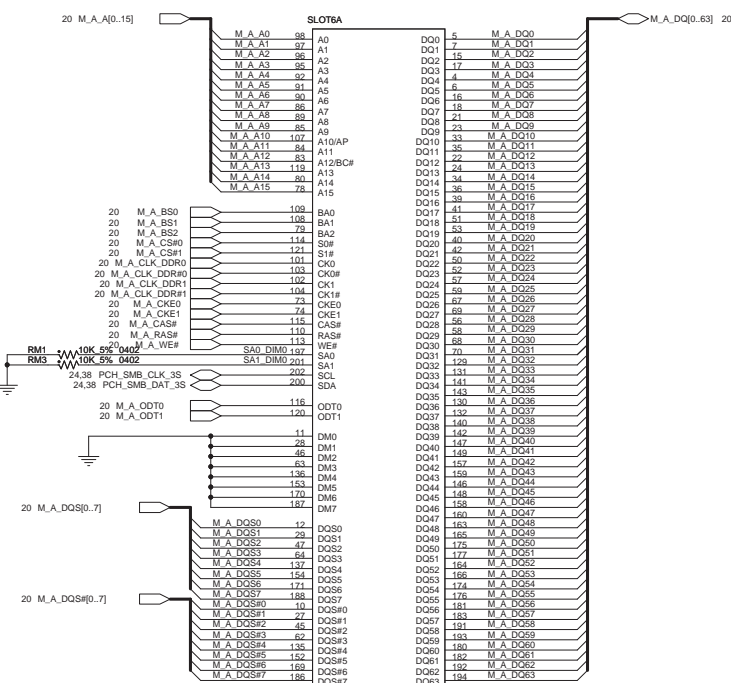
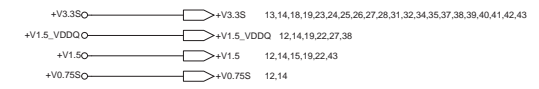
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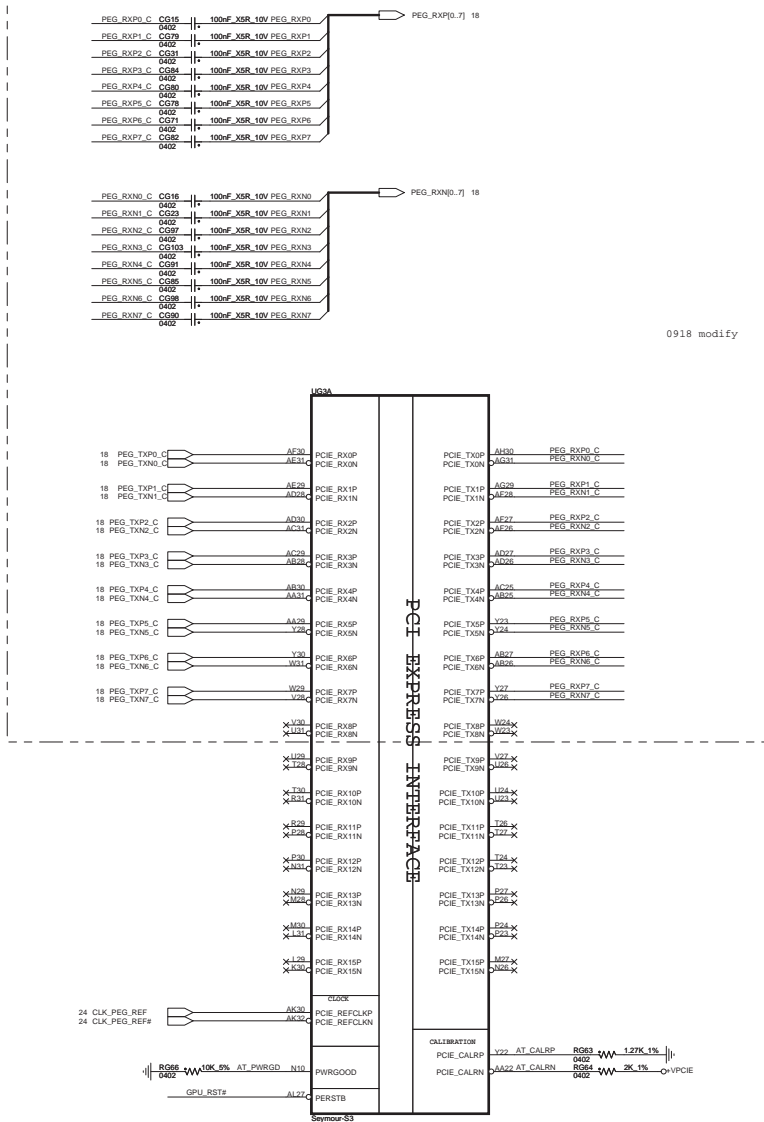
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Title: **CougarPoint(6 of 6)**

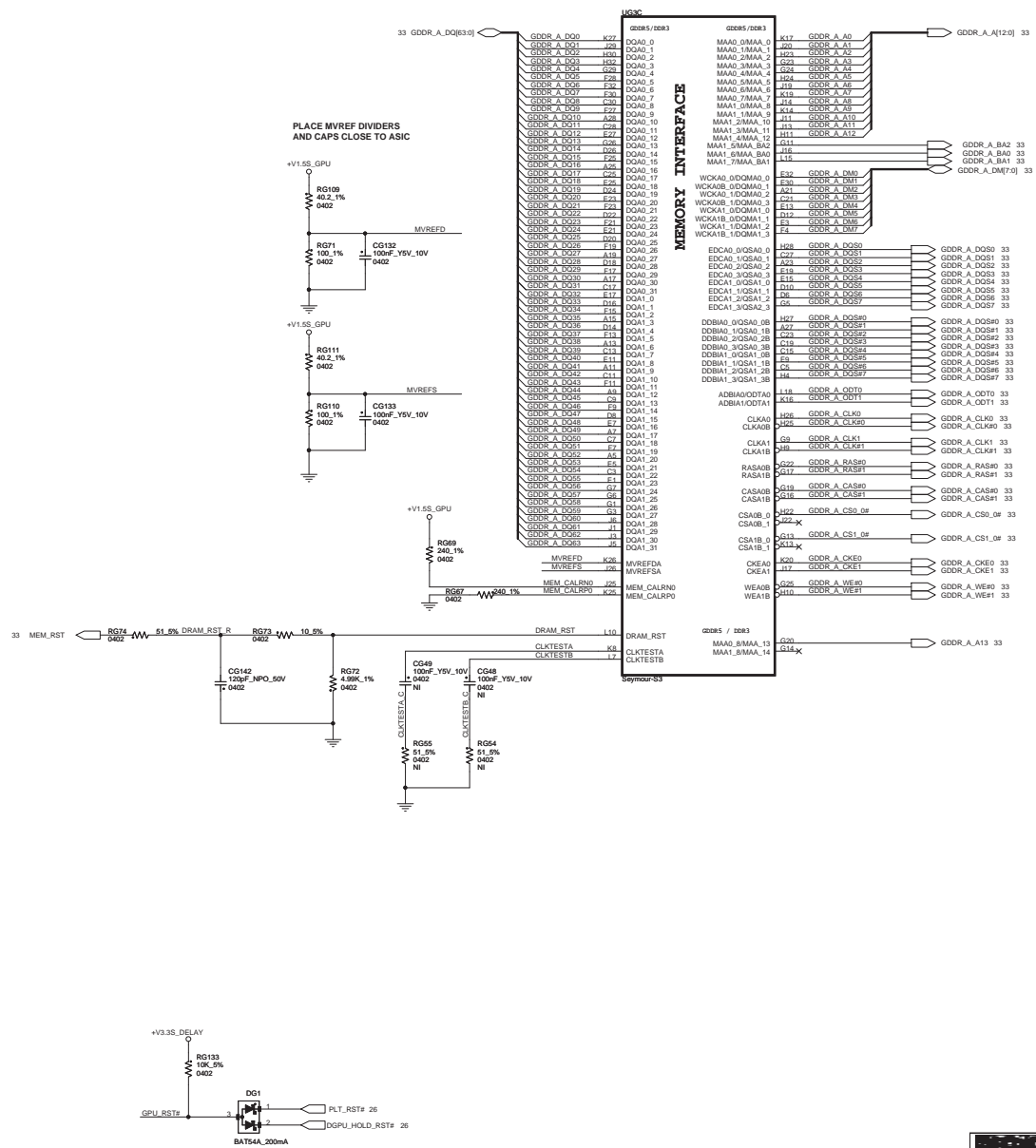
Size	Document Number	Rev
Custom	CHICAGO	MV

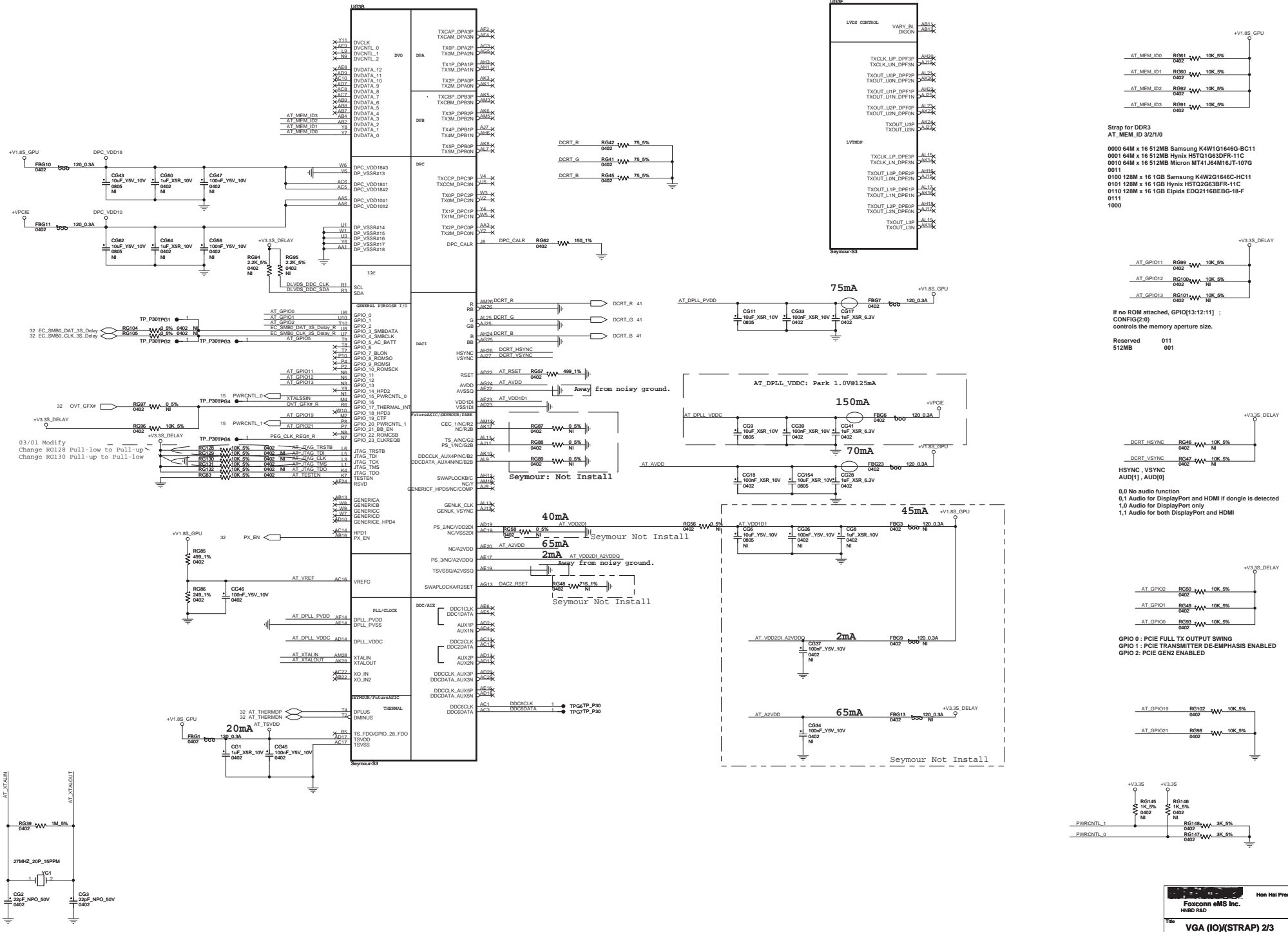
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC/GMT) Sheet 28 of 43





0918 modify





Strap for DDR3
AT_MEM_ID 3/2/1/0

- 0000 64M x 16 S12MB Samsung K4W1G1646G-9C11
- 0001 64M x 16 S12MB Hynix H5TQ1G63DFR-11C
- 0010 64M x 16 S12MB Micron MT41J64M16JT-107G
- 0011 0100 128M x 16 1GB Samsung K4W2G1646G-HC11
- 0100 128M x 16 1GB Hynix H5TQ2G63BFR-11C
- 0110 128M x 16 1GB Elpida EDQ2116BEGG-18-F
- 0111 1000

If no ROM attached, GPIO[13:12:11] ;
CONFIG(2:0)
controls the memory aperture size.

Reserved 011
512MB 001

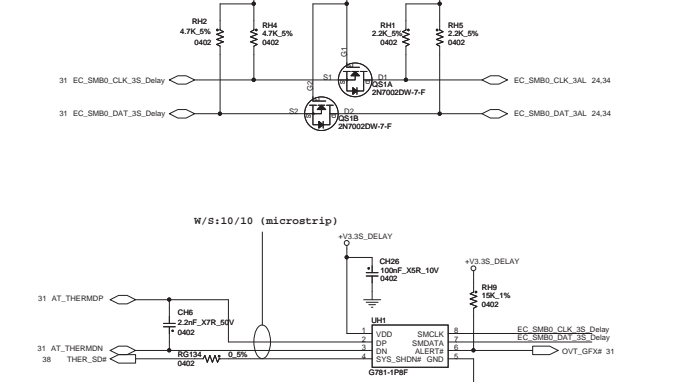
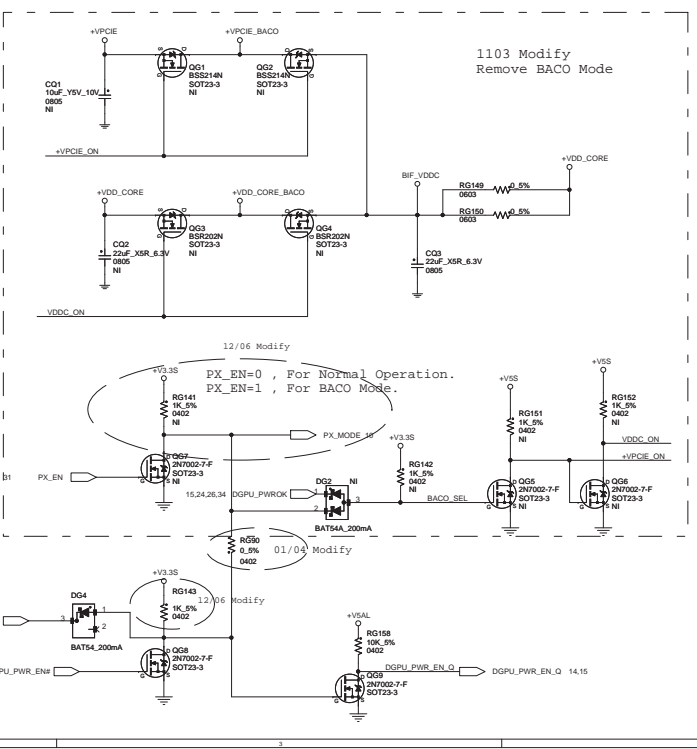
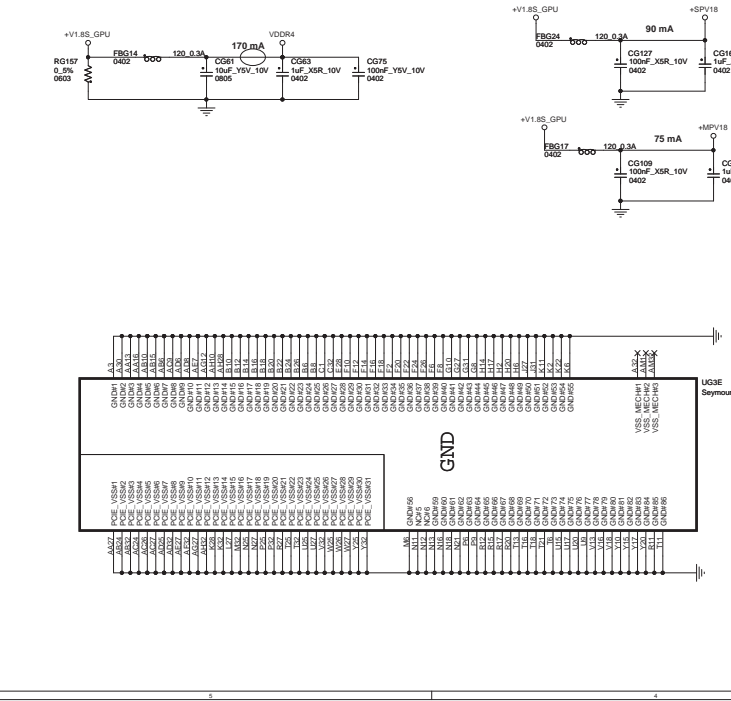
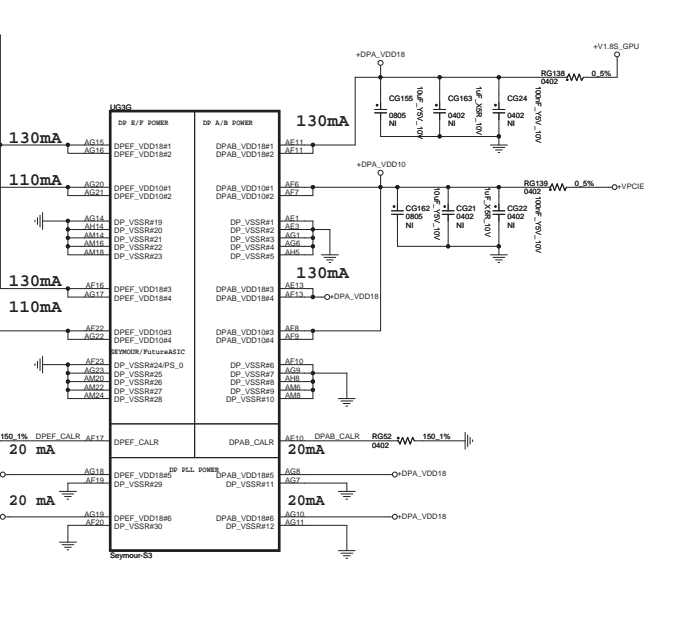
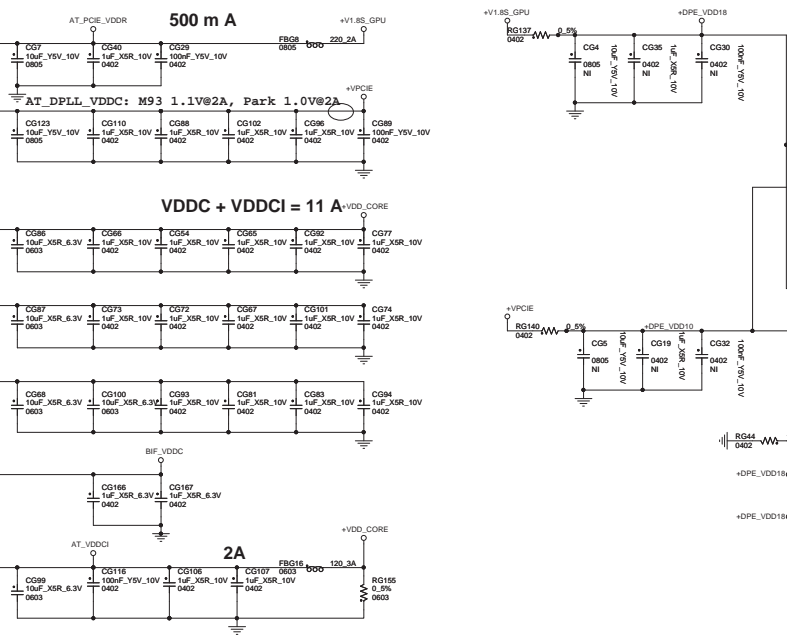
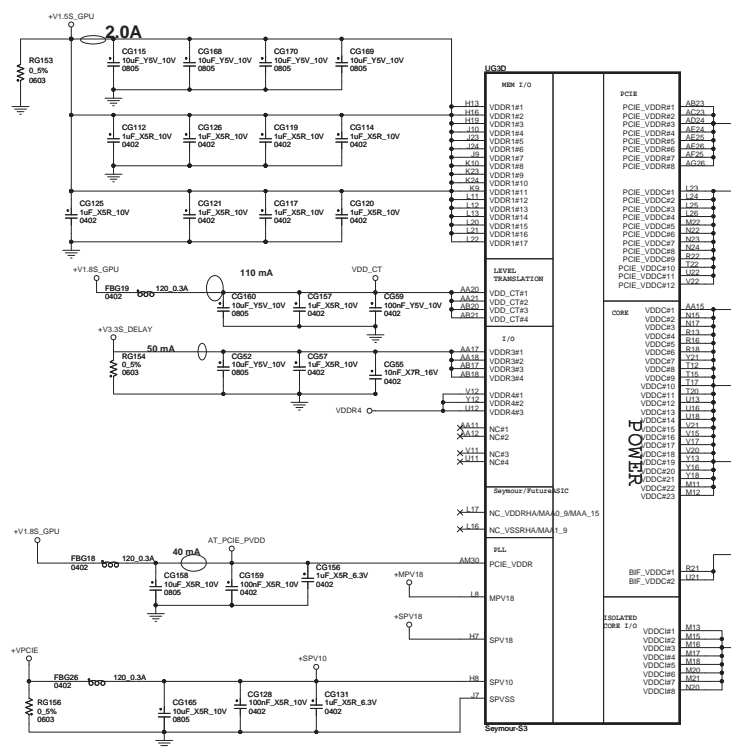
0.0 No audio function
0.1 Audio for DisplayPort and HDMI if dongle is detected
1.0 Audio for DisplayPort only
1.1 Audio for both DisplayPort and HDMI

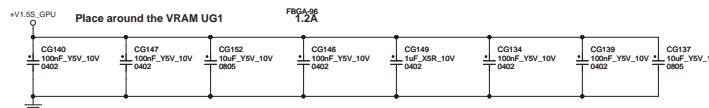
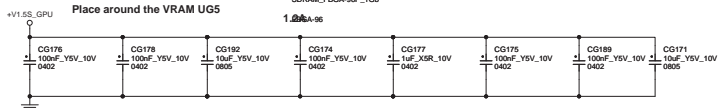
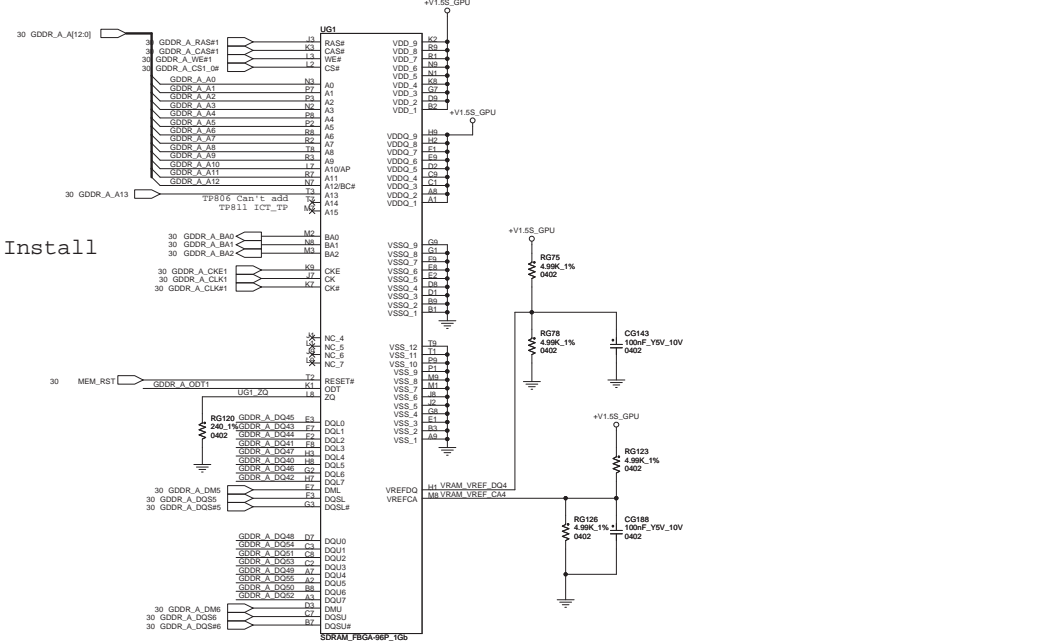
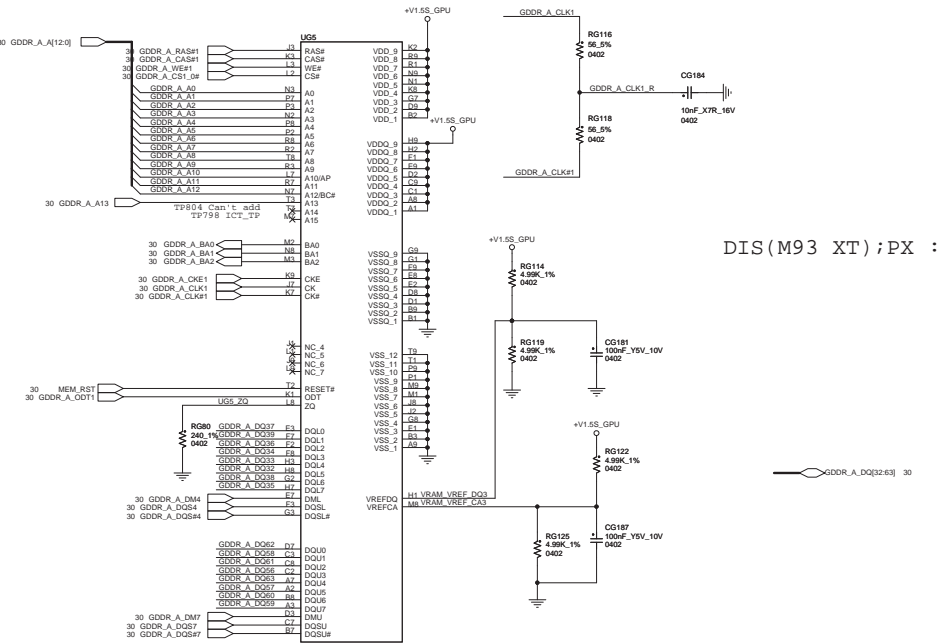
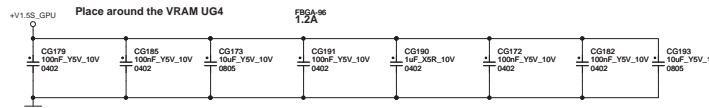
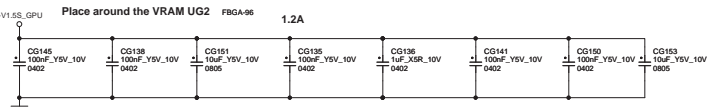
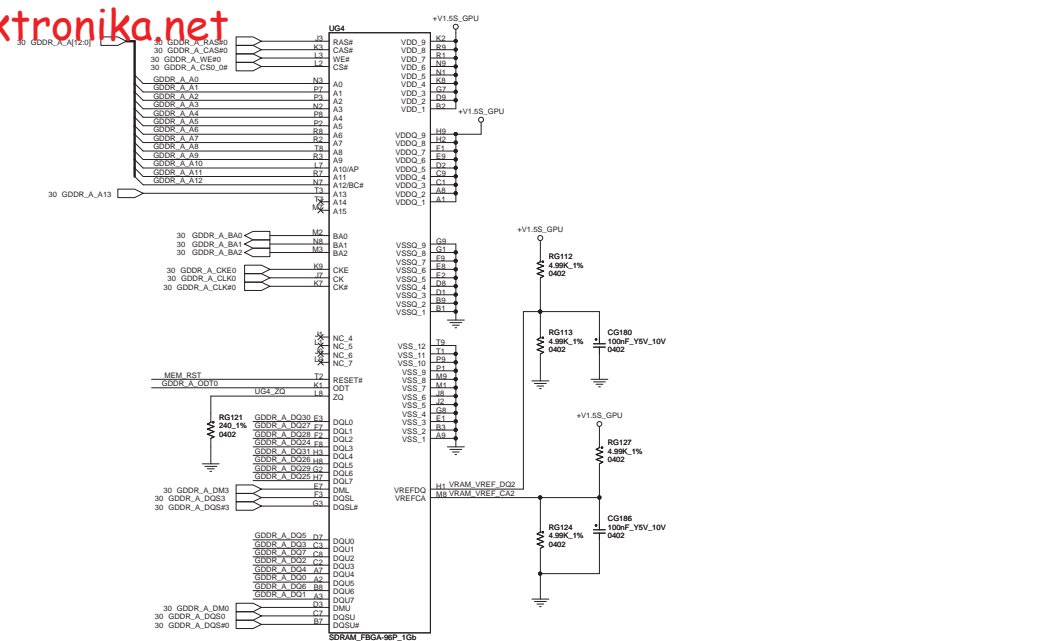
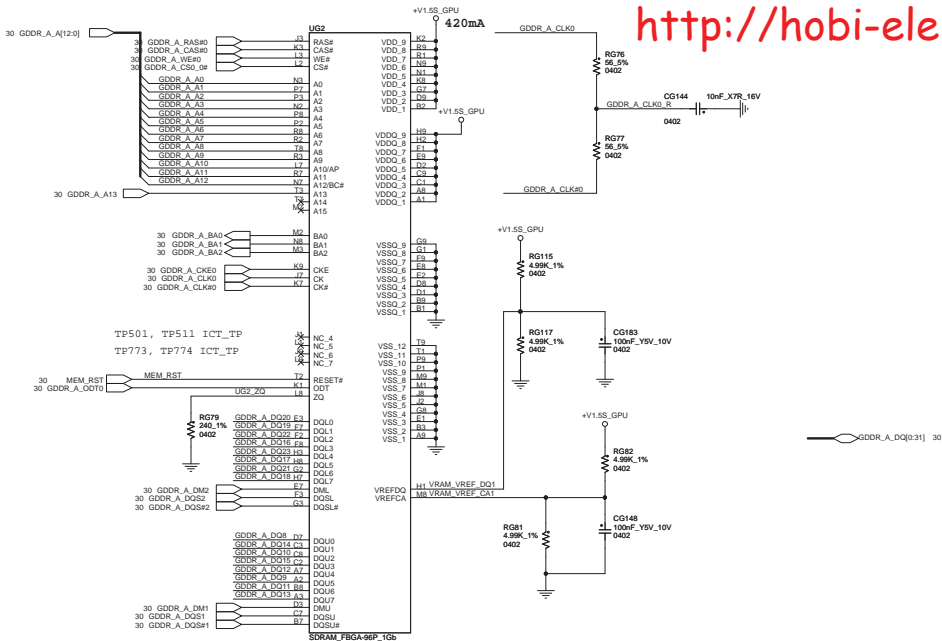
GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

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Title: **VGA IO(STRAP) 2/3**
Doc Number: **CHICAGO**
Rev: **MW**

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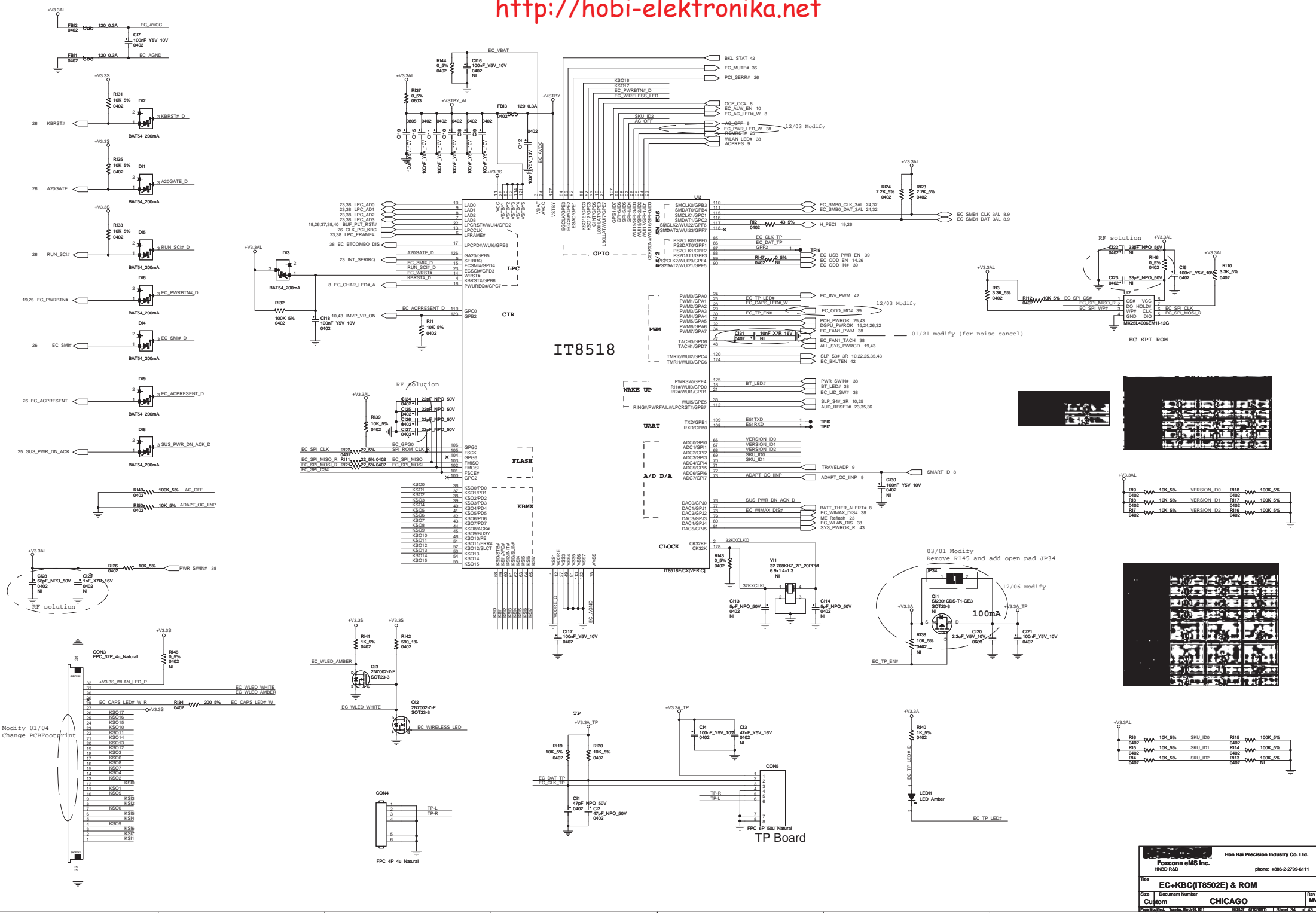




DIS(M93 XT);PX : Install

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File	VRAM (DDR3)	Doc	Doc Number
Customer	CHICAGO	Rev	MW

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IT518

Modify 01/04
Change PCB footprint

REF solution

REF solution

REF solution

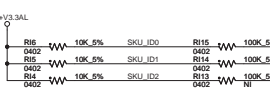
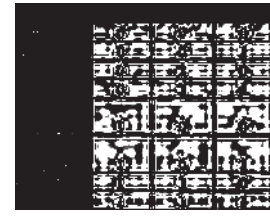
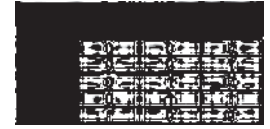
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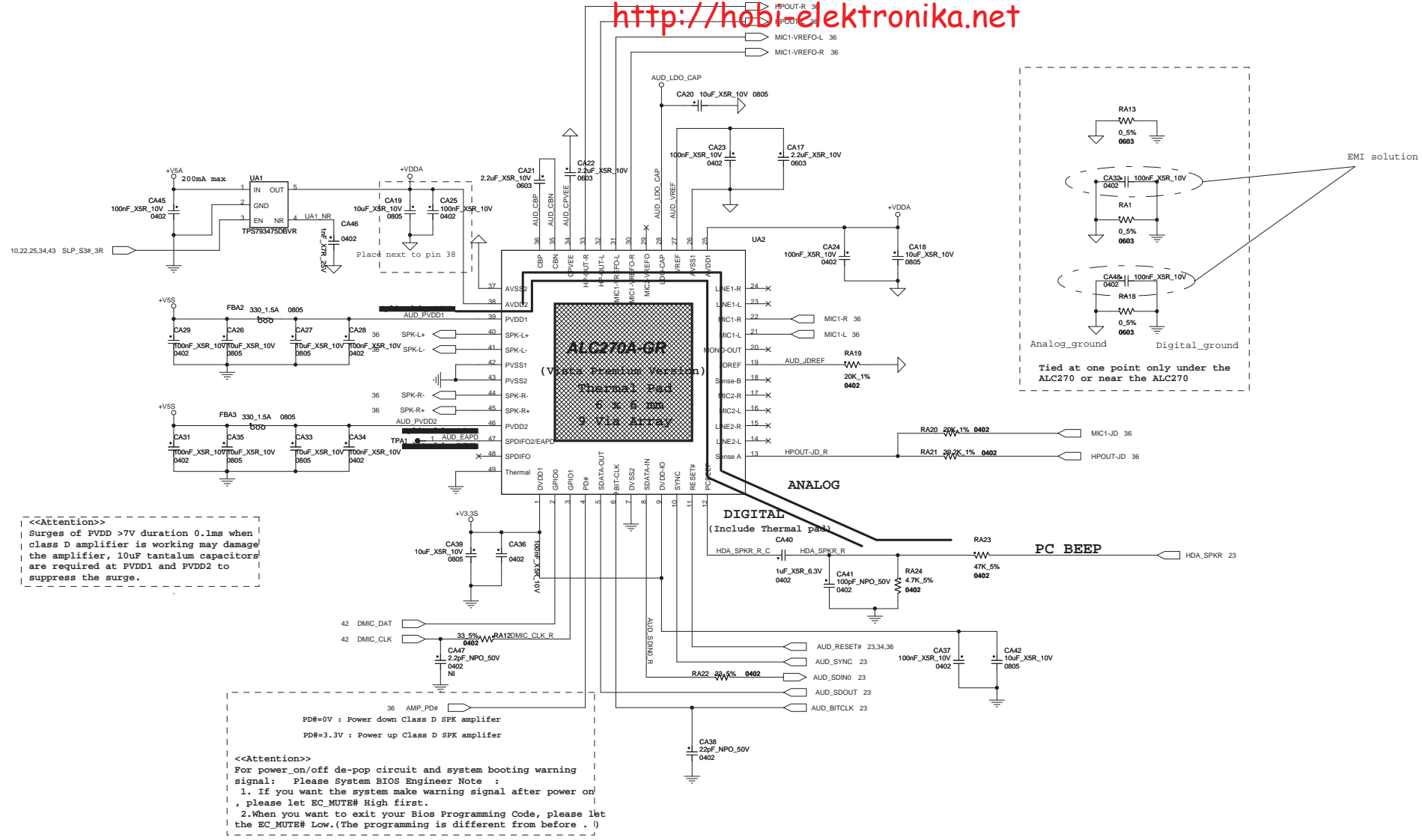
REF solution

REF solution

REF solution

REF solution

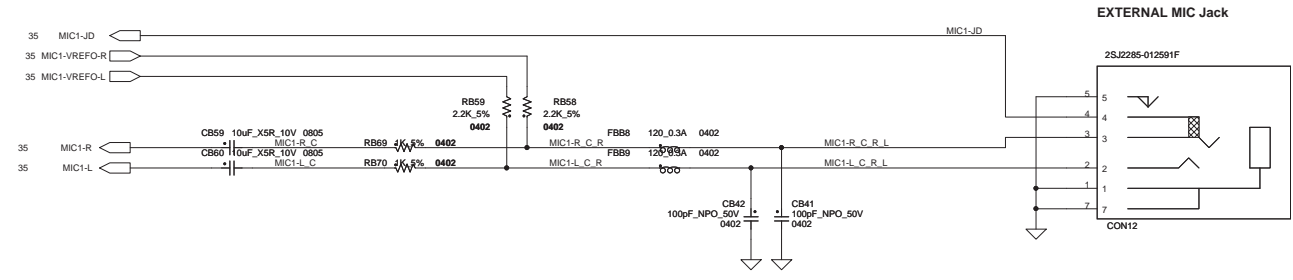
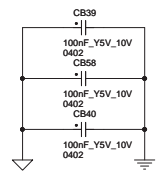
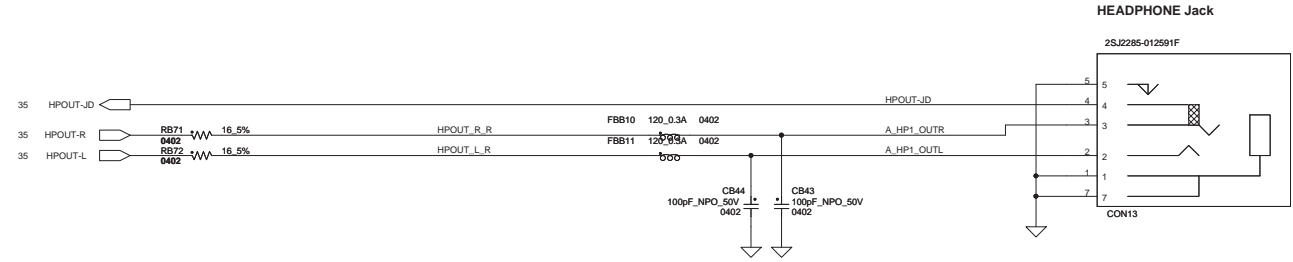
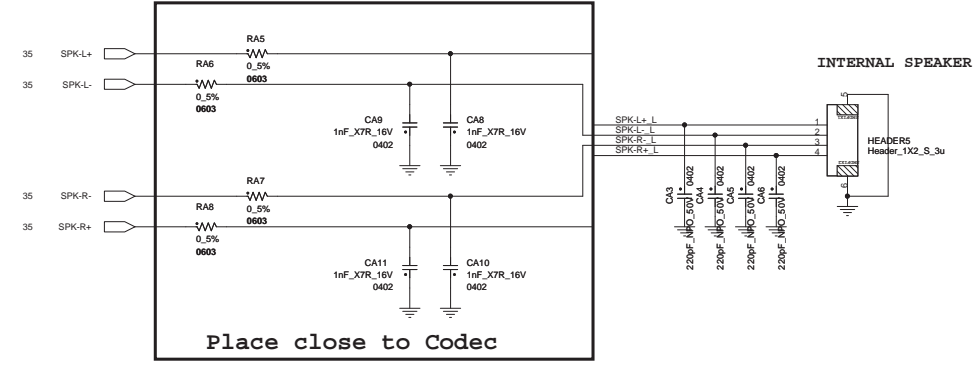
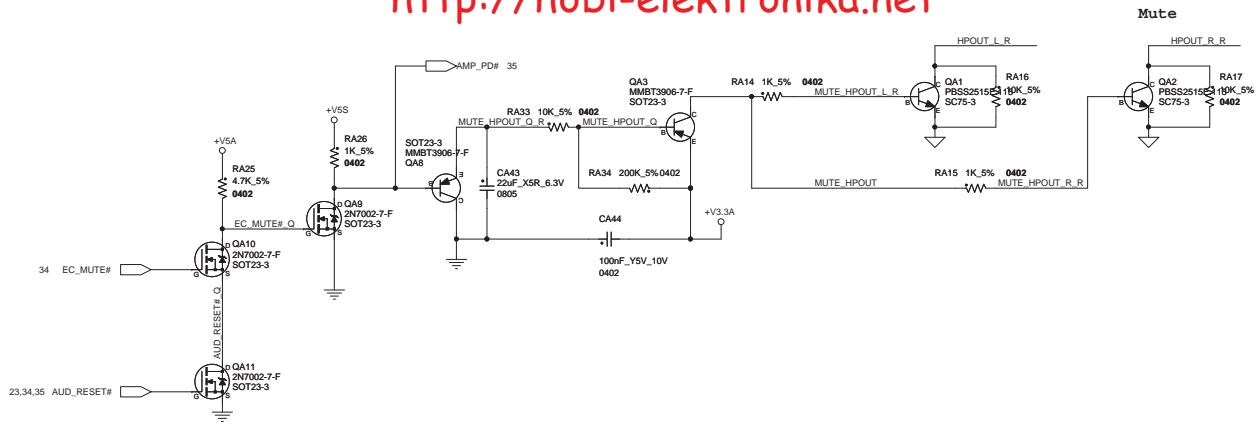


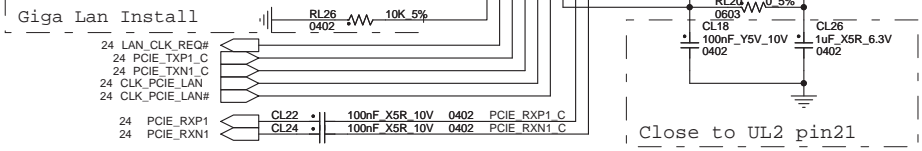
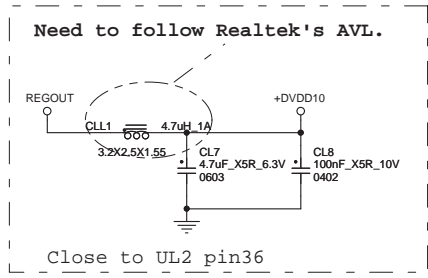
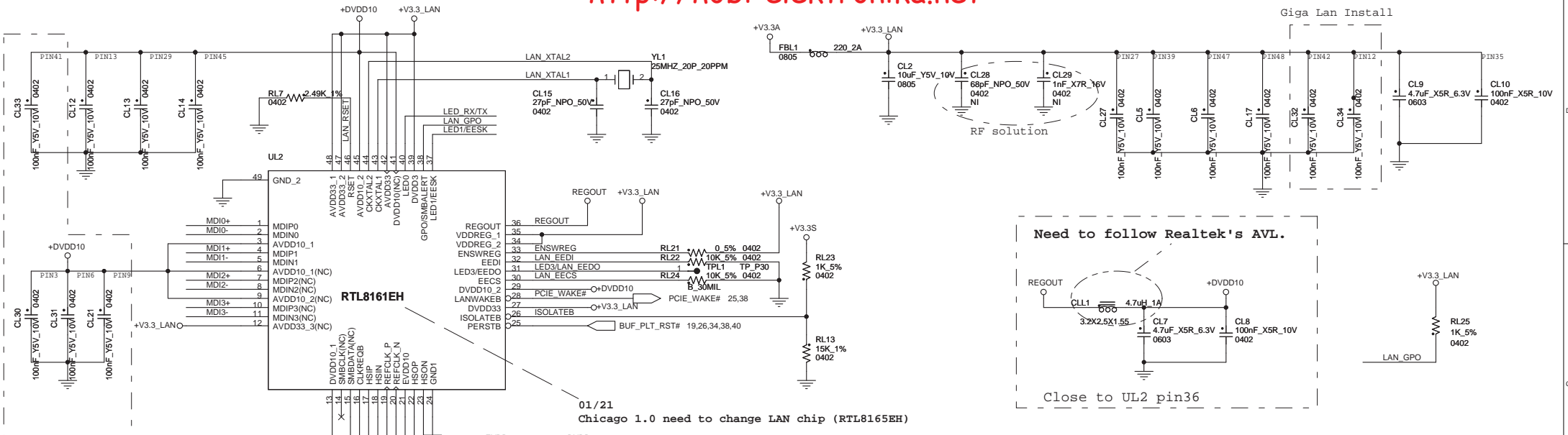


<<Attention>>
 Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

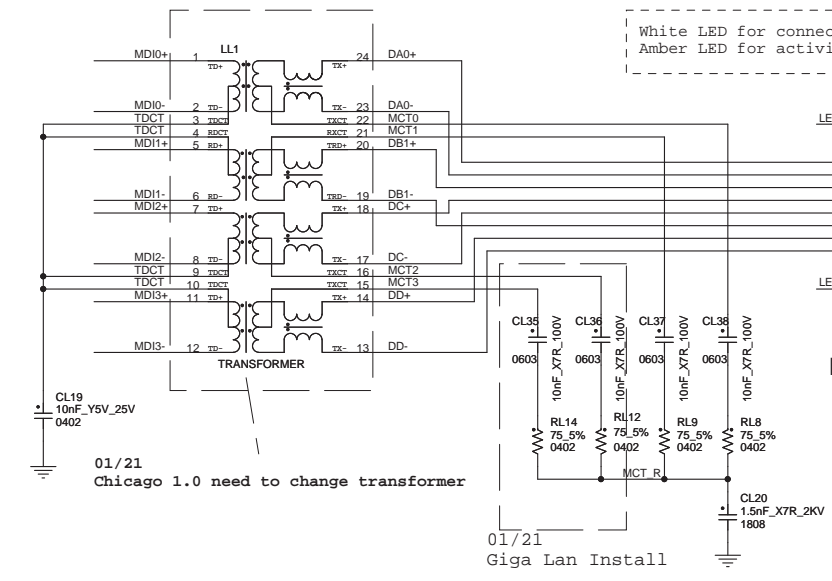
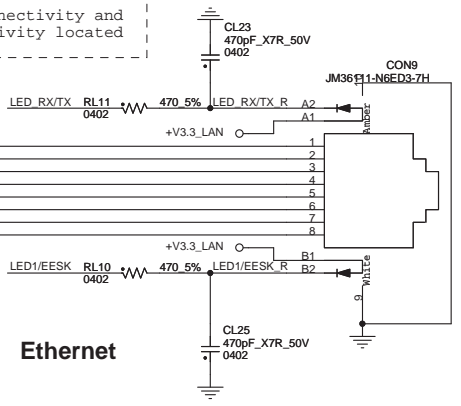
36 AMP_PD#
 PD#=0V : Power down Class D SPK amplifier
 PD#=3.3V : Power up Class D SPK amplifier

<<Attention>>
 For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
 1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
 2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)





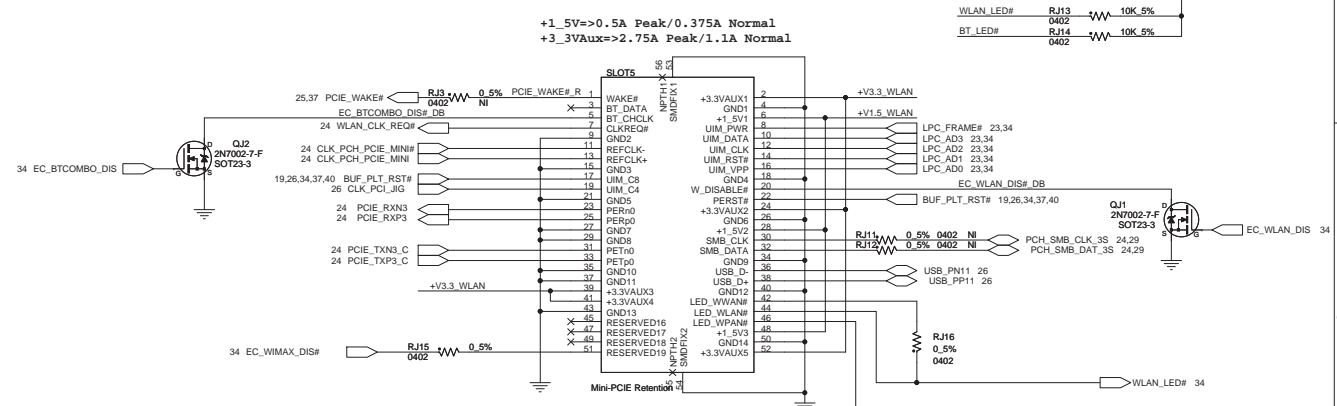
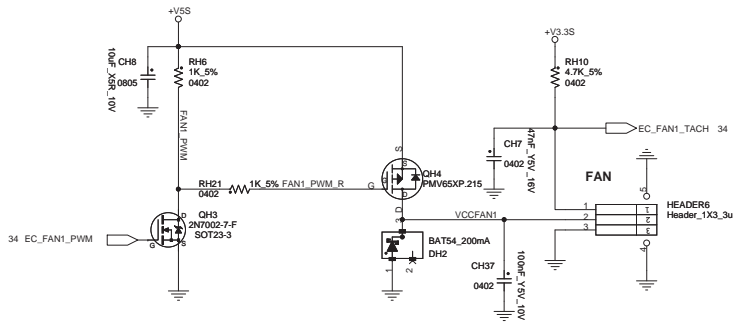
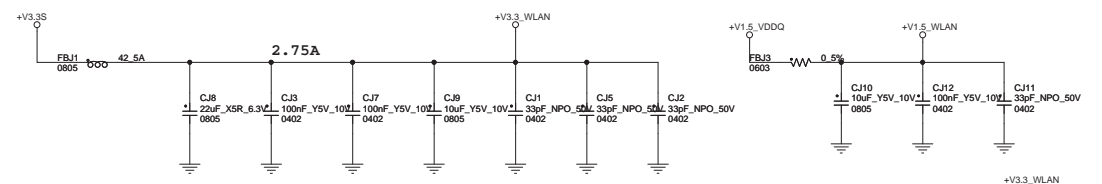
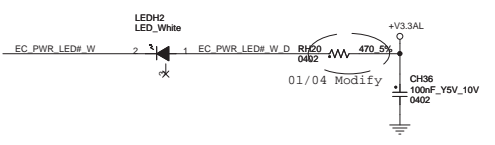
White LED for connectivity and Amber LED for activity located



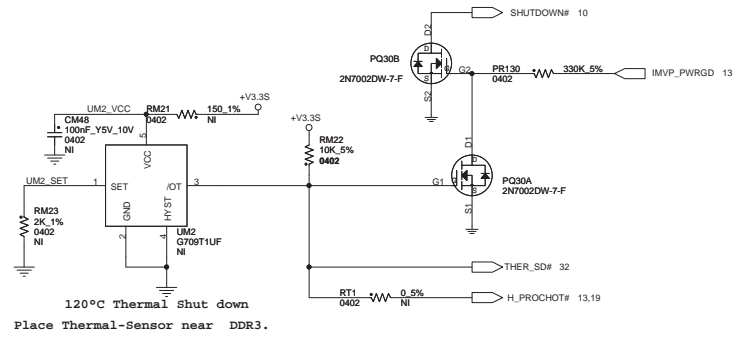
01/21 Giga Lan Install



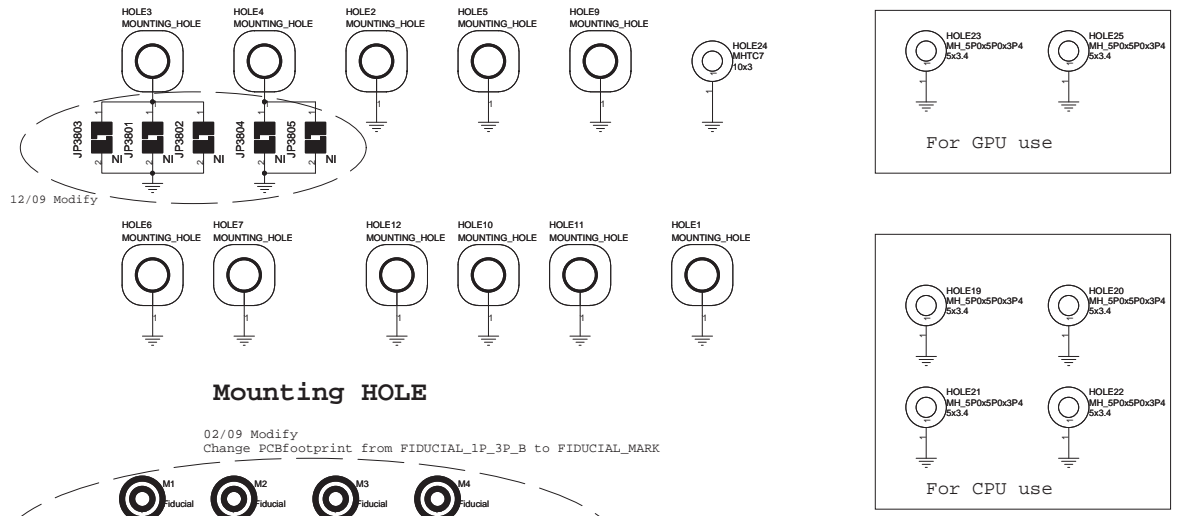
		Hon Hai Precision Industry Co. Ltd. HNBDR&D phone: +886-2-2799-6111	
Title LAN (RTL8165EH)			
Size Custom		Document Number Rev	
Page Modified: Tuesday, March 06, 2011		08:28:59 (UTC/GMT) Sheet 37 of 43	



Half Mini Card for WLAN



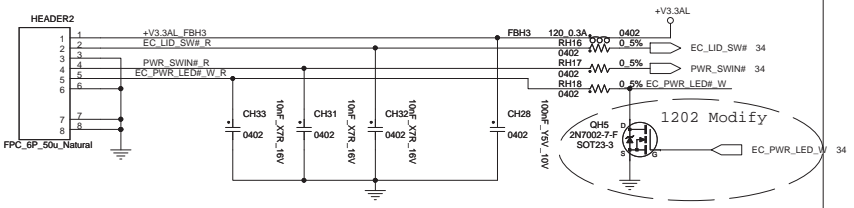
120°C Thermal Shut down
Place Thermal-Sensor near DDR3.

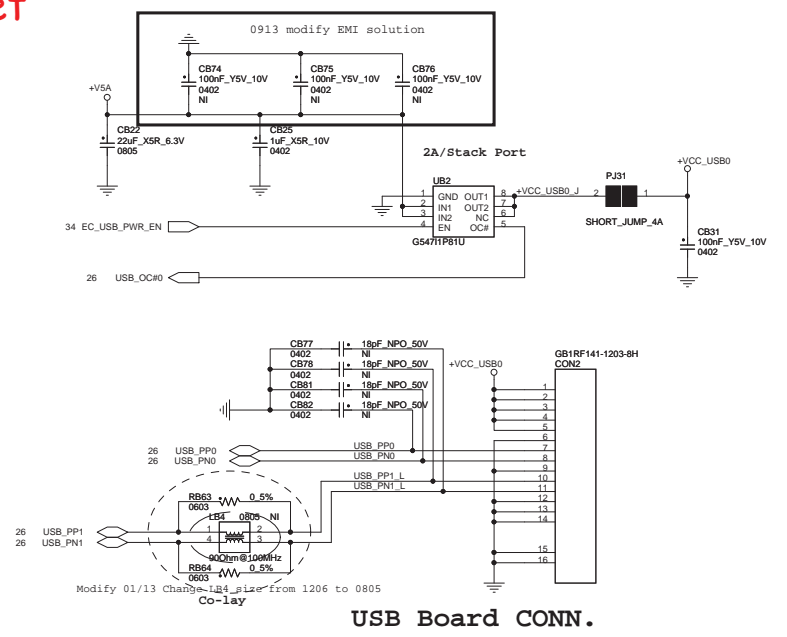
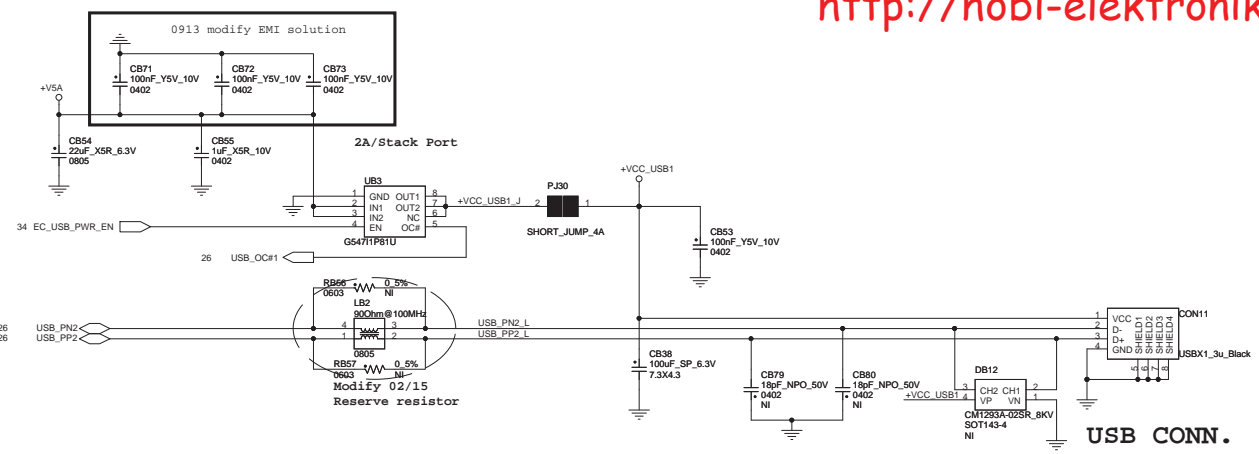


Mounting HOLE

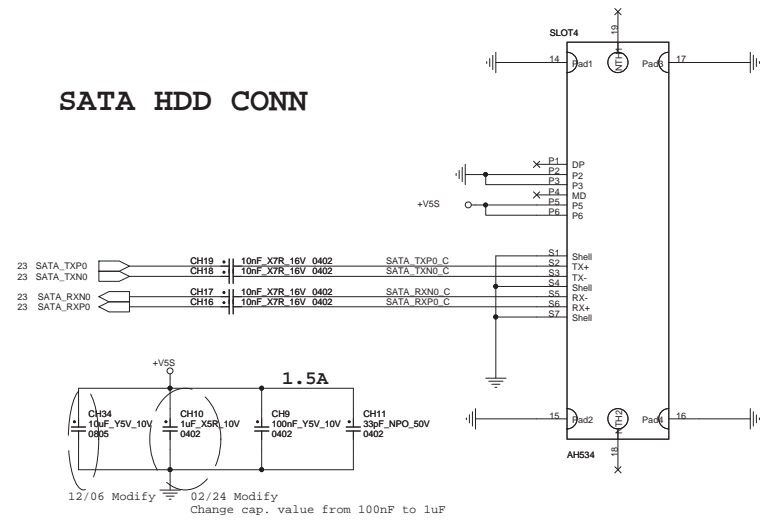
Fiducial Mark

PWR Board CONN.

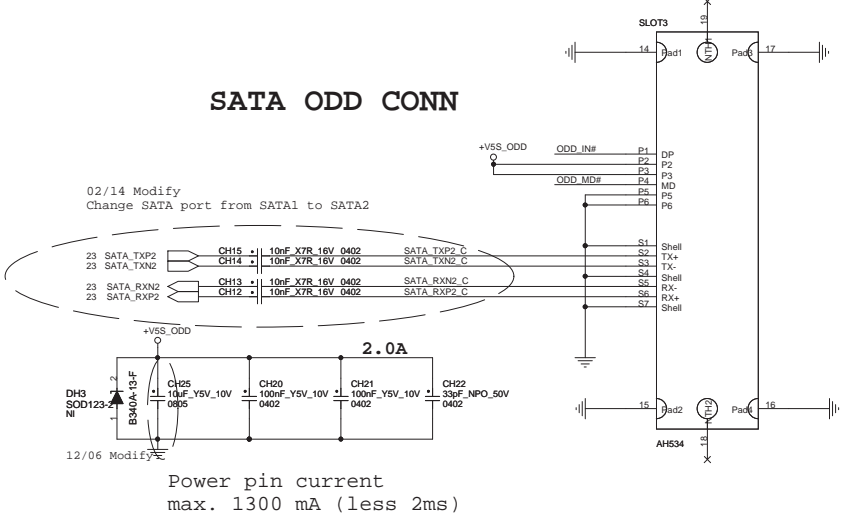




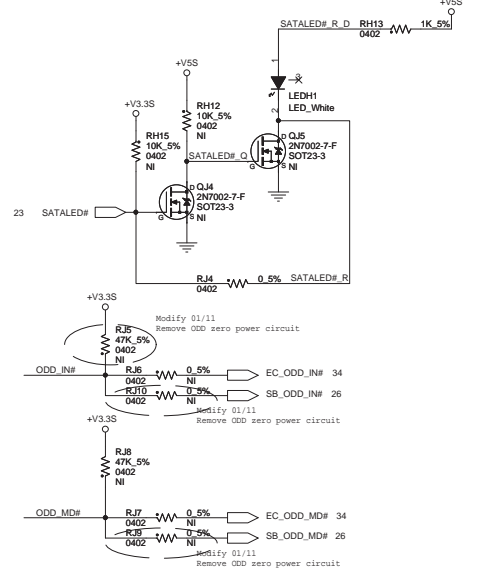
SATA HDD CONN

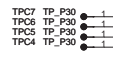
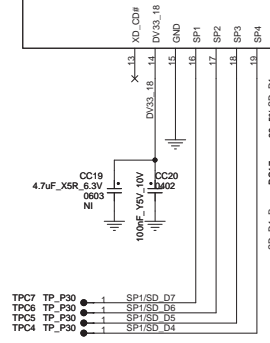
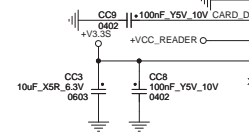
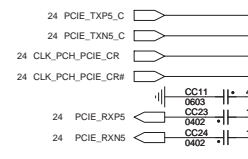
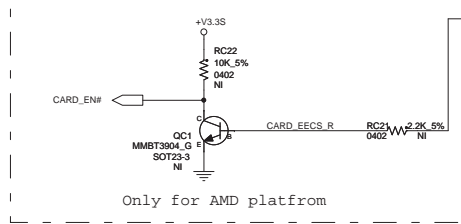


SATA ODD CONN

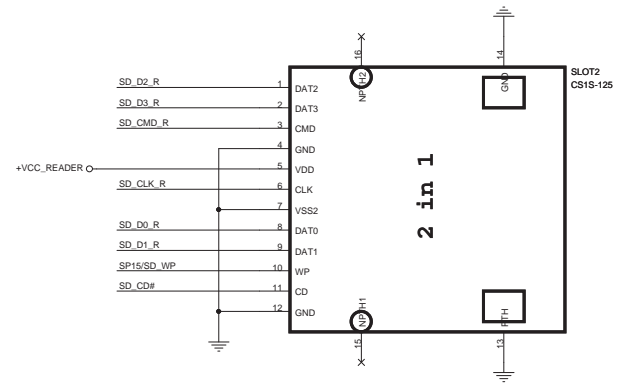
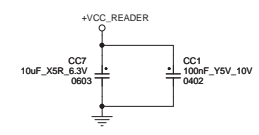


HDD/ODD Status LED



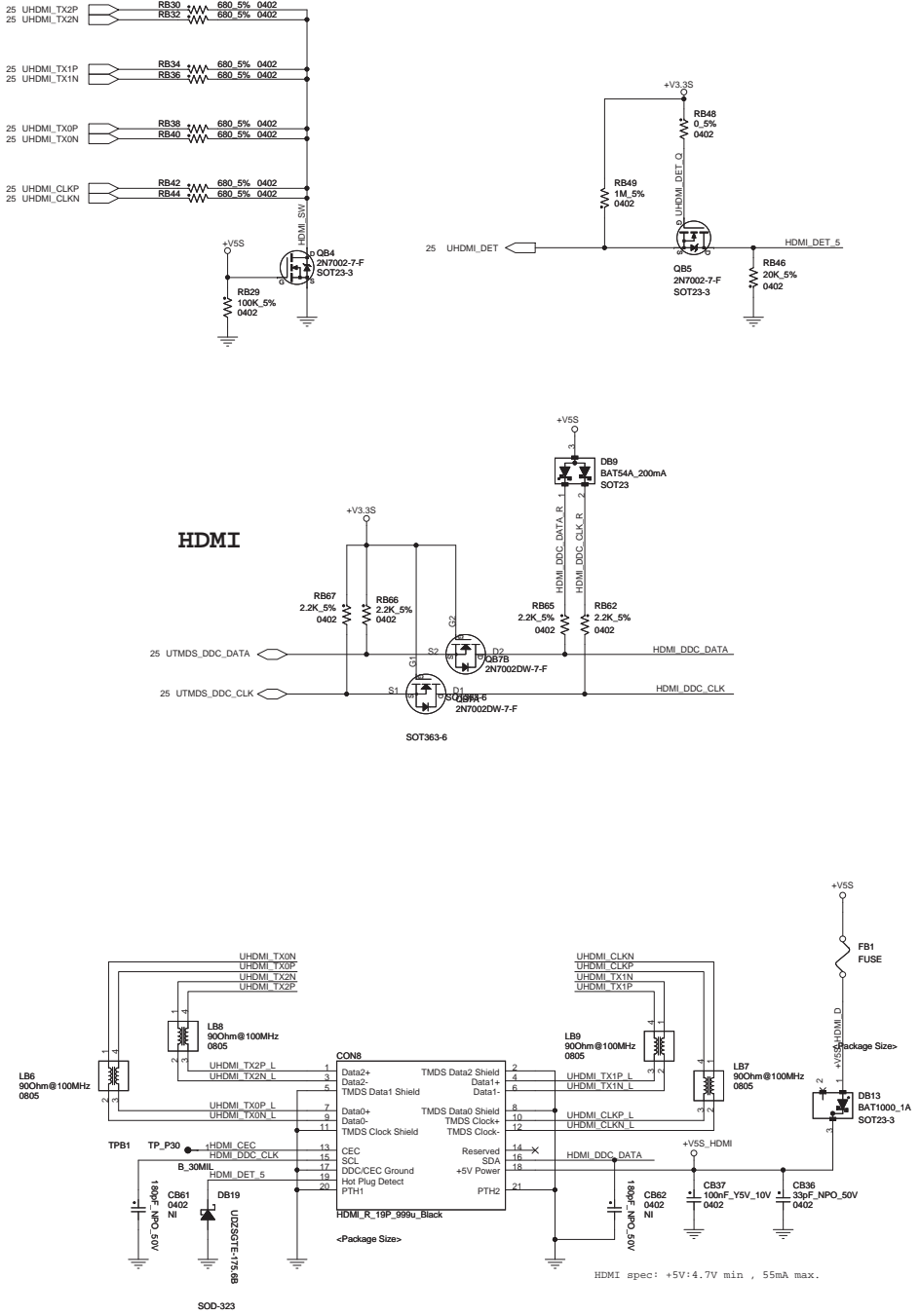


1/24 Modify Check with EMI/ESDMax



RC14-RC19, CC10 close to chip pin!

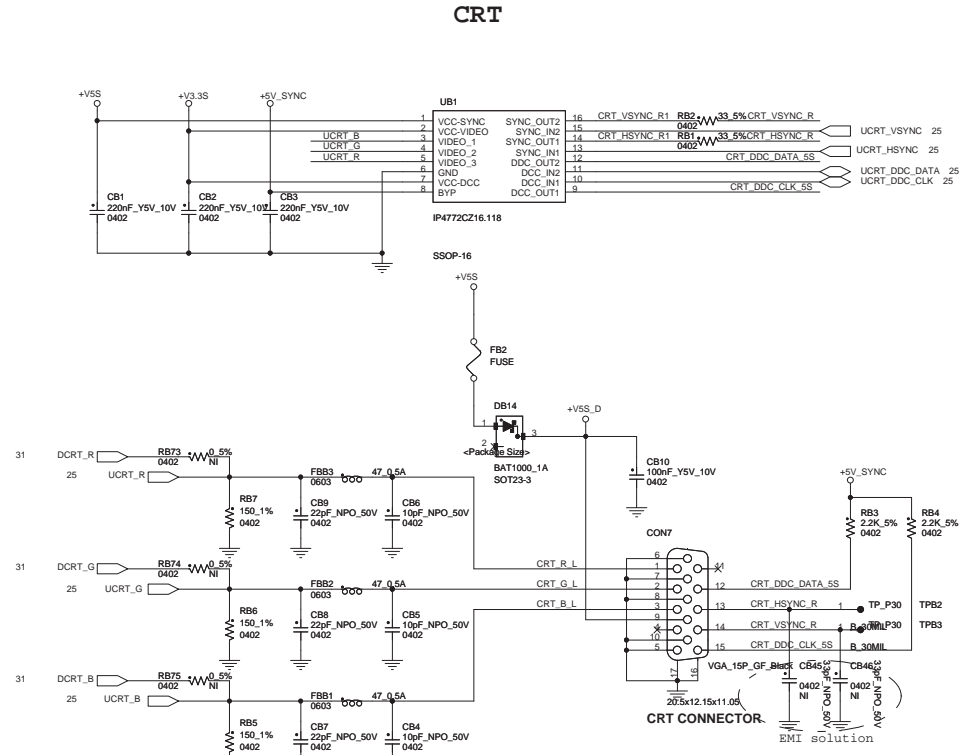
EMI/ESD Solution



HDMI

SOD-323

HDMI spec: +5V:4.7V min , 55mA max.



CRT

CRT CONNECTOR

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HDMI & CRT			
Size	Document Number	Rev	
Custom			
Page Modified: Tuesday, March 08, 2011 08:28:59 (UTC+08:00) Sheet 41 of 43			

