


# P900-A00 DESIGN -- G73, 256 MB DDR2, VGA, DVI -I, HDTV

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skid	VARIANT	NVPN	ASSEMBLY
B	0000	600-10900-0000-000	G73 400/400MHz 256MB 128bit DDR2 16MX16 DVI-I+VGA+HDTVOUT
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2	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
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PAGE DETAIL	TABLE OF CONTENTS & REVISION HISTORY

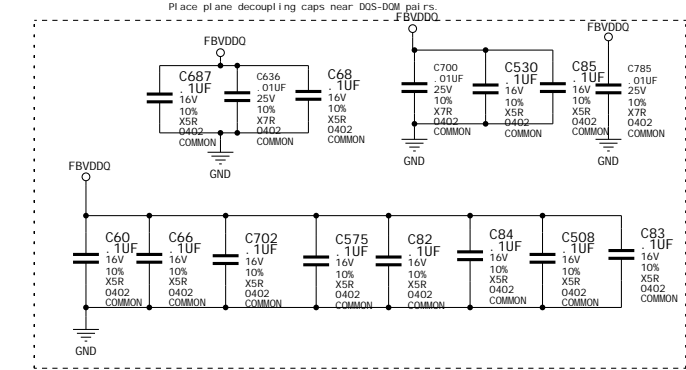
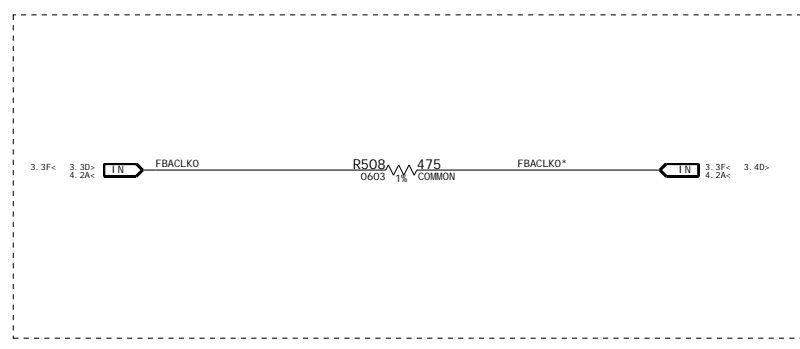
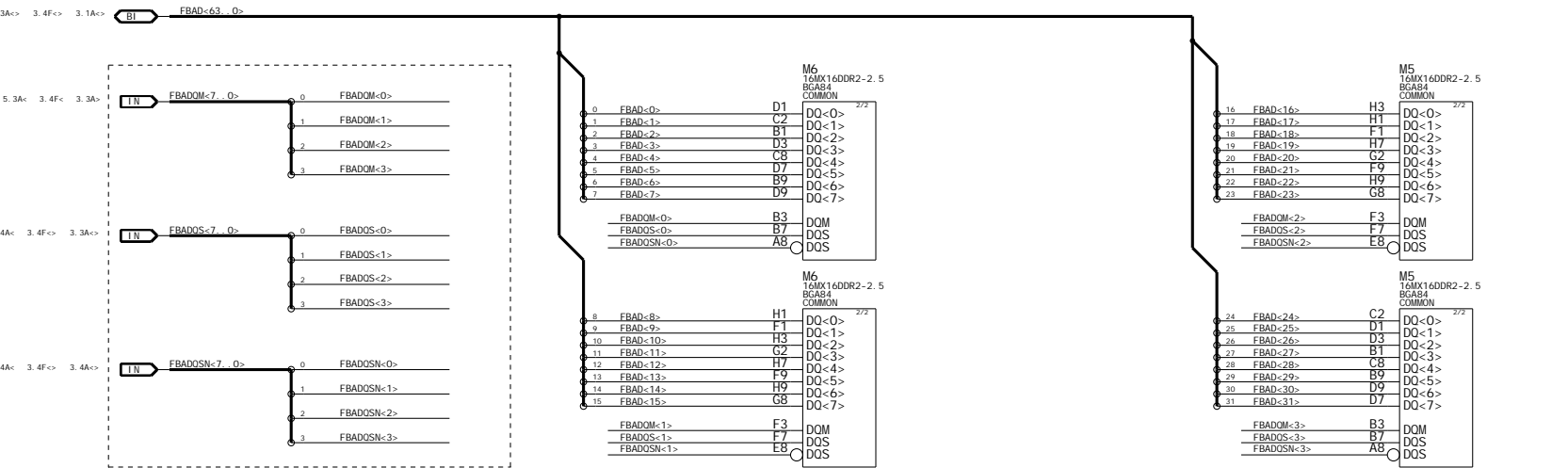
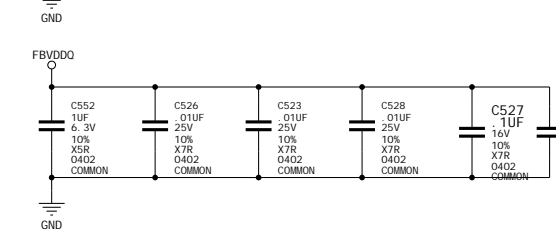
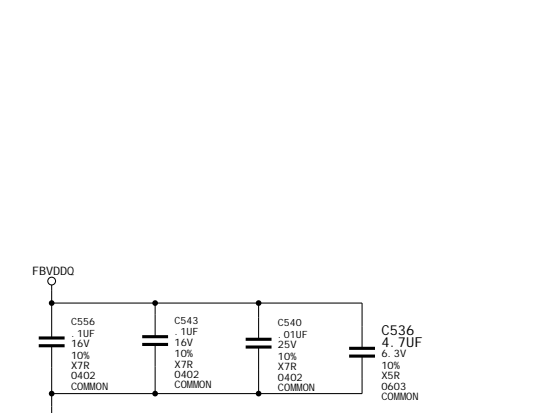
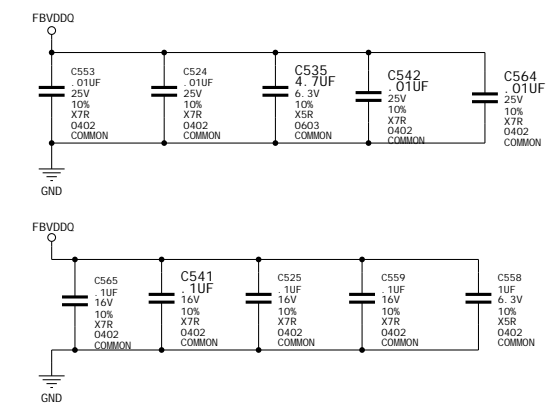
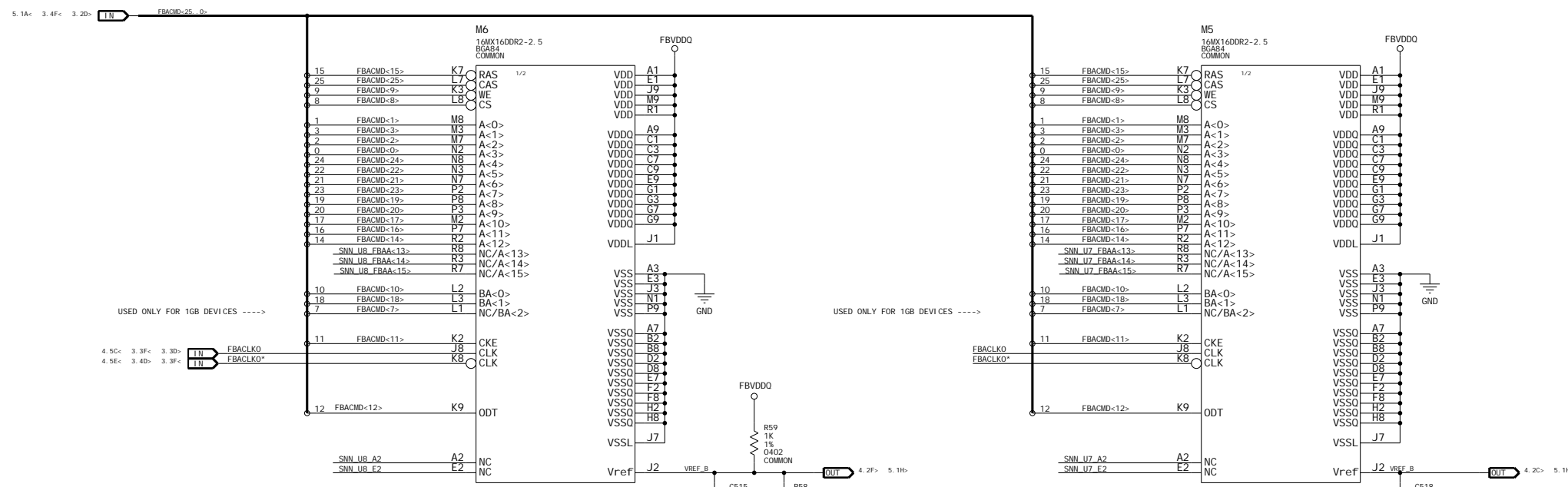
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# FBA MEMORY 1st bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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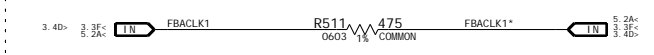
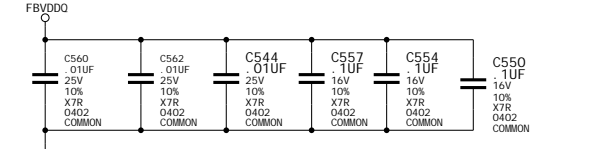
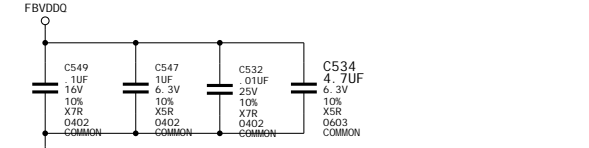
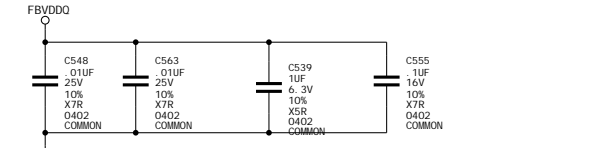
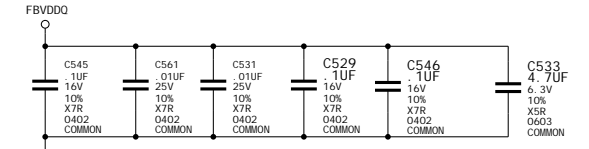
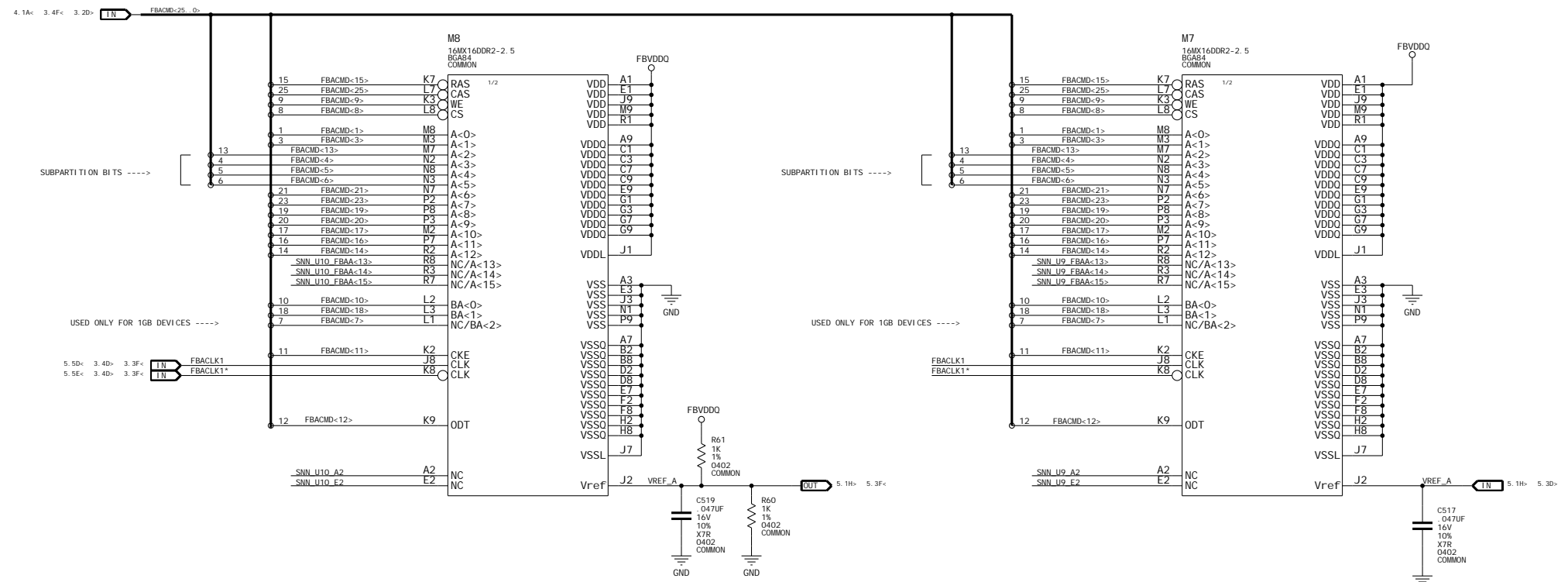
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO-STUFF ASSEMBLY NOTES AND BOM NOT FINAL		
PAGE	DETAIL	FBA 16MX16 DDR2 MEMORIES, BANK 0..31	
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# FBA MEMORY 1st bank 32..63

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY

NAME	MI_N_LI_NE_WI_DTH	
VREF_A	12.0	5.30V 5.3F
VREF_B	12.0	4.20V 4.2F

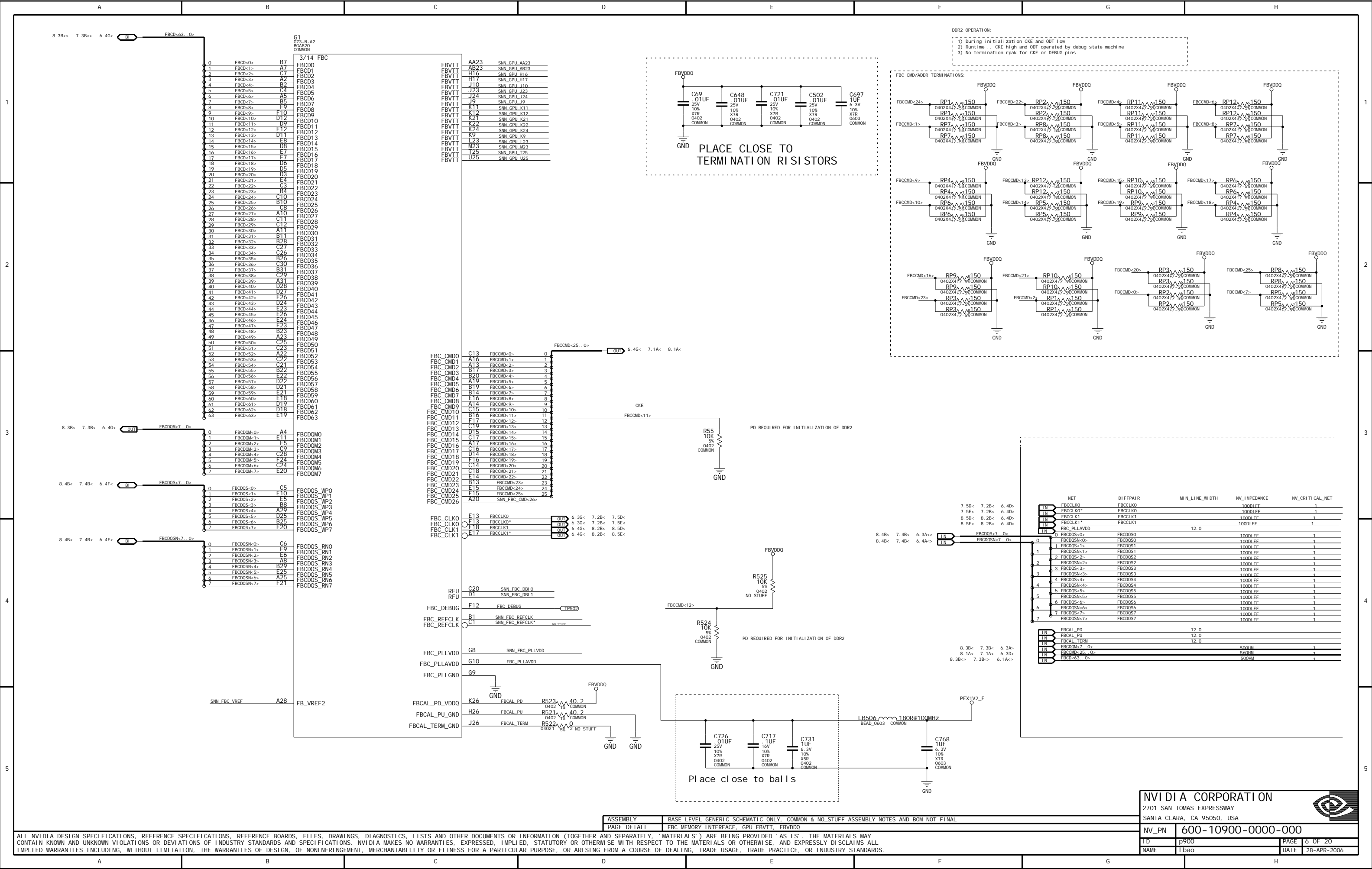


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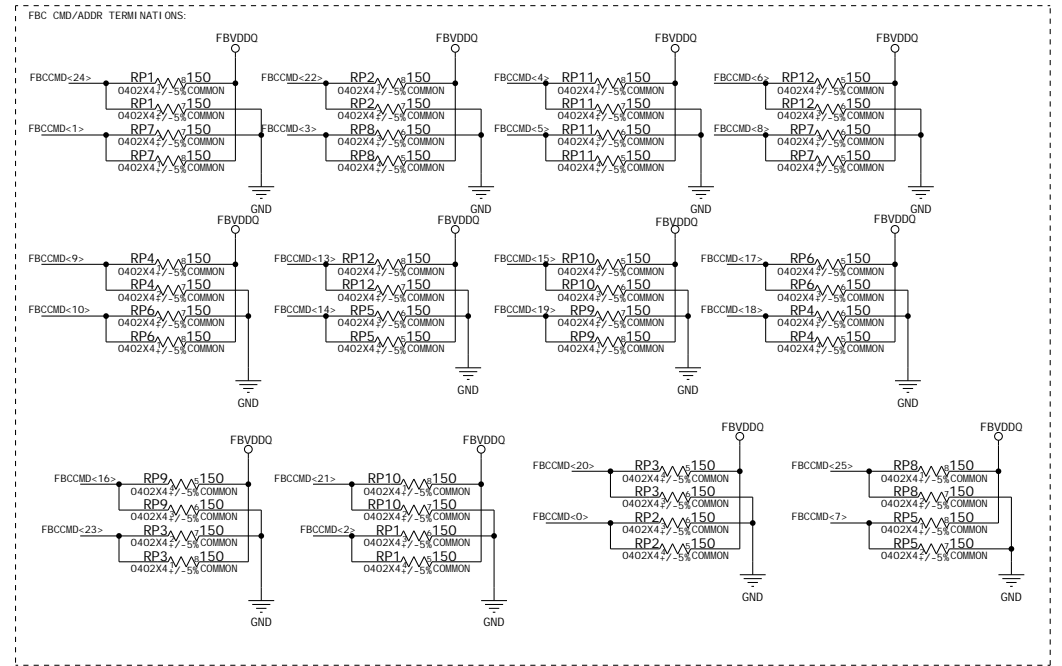
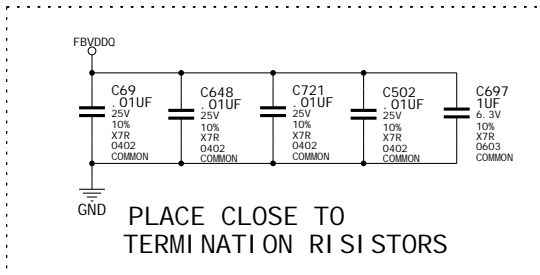
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PAGE DETAIL	FBA 16Mx16 DDR2 MEMORIES, 1ST BANK 32..63

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DDR2 OPERATION:  
 1) During initialization CKE and ODT low  
 2) Runtime ... CKE high and ODT operated by debug state machine  
 3) No termination rpak for CKE or DEBUG pins

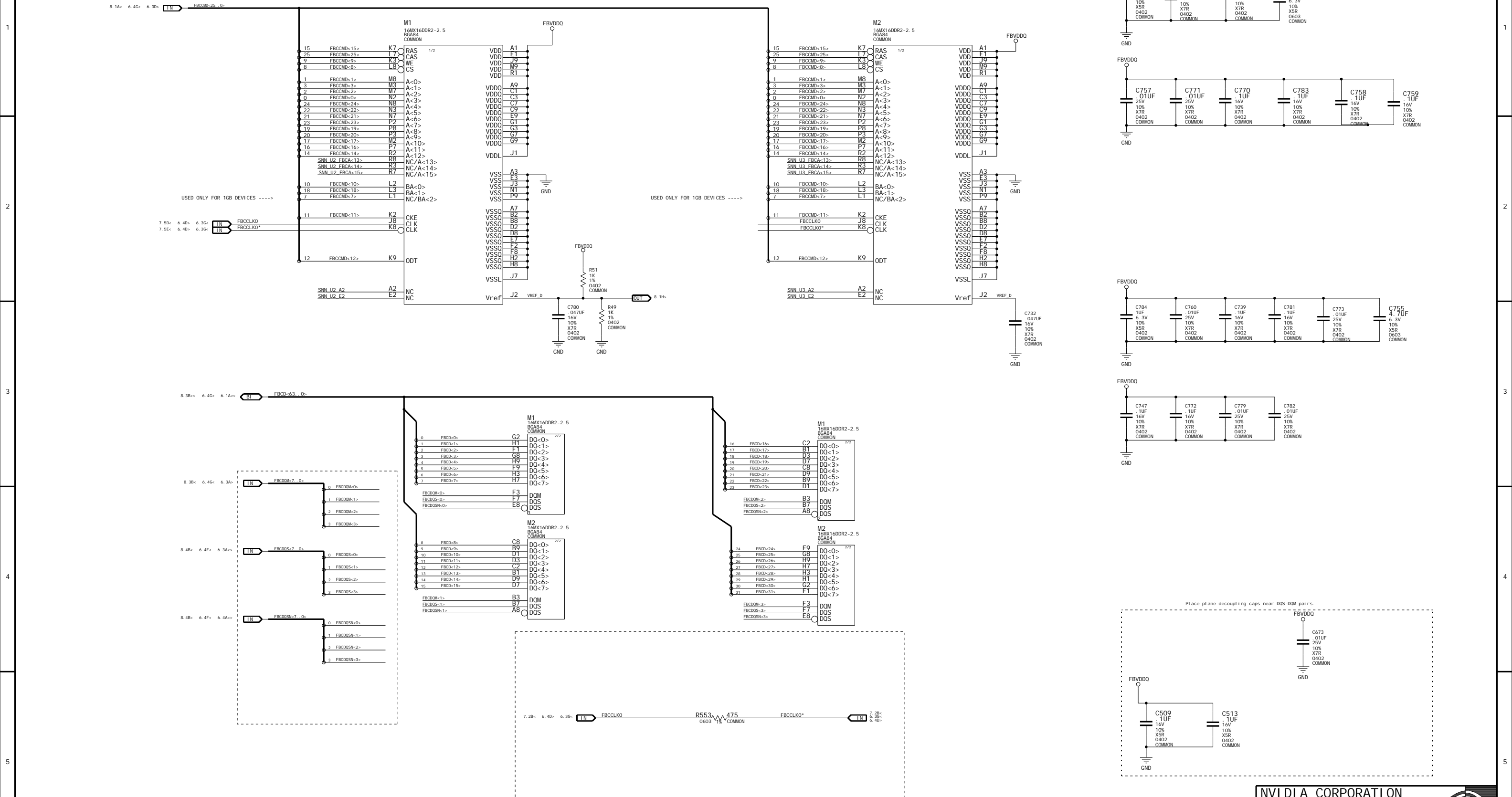


FBC_CMD0	C13	FBC_CMD<0>	0
FBC_CMD1	A16	FBC_CMD<1>	1
FBC_CMD2	A13	FBC_CMD<2>	2
FBC_CMD3	B17	FBC_CMD<3>	3
FBC_CMD4	B20	FBC_CMD<4>	4
FBC_CMD5	A19	FBC_CMD<5>	5
FBC_CMD6	B19	FBC_CMD<6>	6
FBC_CMD7	B14	FBC_CMD<7>	7
FBC_CMD8	E16	FBC_CMD<8>	8
FBC_CMD9	A14	FBC_CMD<9>	9
FBC_CMD10	C15	FBC_CMD<10>	10
FBC_CMD11	B16	FBC_CMD<11>	11
FBC_CMD12	F19	FBC_CMD<12>	12
FBC_CMD13	D15	FBC_CMD<13>	13
FBC_CMD14	C17	FBC_CMD<14>	14
FBC_CMD15	A17	FBC_CMD<15>	15
FBC_CMD16	D14	FBC_CMD<16>	16
FBC_CMD17	D14	FBC_CMD<17>	17
FBC_CMD18	F16	FBC_CMD<18>	18
FBC_CMD19	F16	FBC_CMD<19>	19
FBC_CMD20	C14	FBC_CMD<20>	20
FBC_CMD21	C18	FBC_CMD<21>	21
FBC_CMD22	B13	FBC_CMD<22>	22
FBC_CMD23	E15	FBC_CMD<23>	23
FBC_CMD24	F15	FBC_CMD<24>	24
FBC_CMD25	F15	FBC_CMD<25>	25
FBC_CMD26	A20	SNV_FBC_CMD<26>	

NET	DIFFPAIR	MIN_LI_NE_WIDTH	NV_IMPEDANCE	NV_CRTICAL_NET
FBVDDO				
FBVDDQ				
FBVDDN				
FBVDDP				
FBVDDT				
FBVDDU				
FBVDDV				
FBVDDW				
FBVDDX				
FBVDDY				
FBVDDZ				
FBVDDA				
FBVDDB				
FBVDDC				
FBVDD D				
FBVDD E				
FBVDD F				
FBVDD G				
FBVDD H				
FBVDD I				
FBVDD J				
FBVDD K				
FBVDD L				
FBVDD M				
FBVDD N				
FBVDD O				
FBVDD P				
FBVDD Q				
FBVDD R				
FBVDD S				
FBVDD T				
FBVDD U				
FBVDD V				
FBVDD W				
FBVDD X				
FBVDD Y				
FBVDD Z				
FBVDD AA				
FBVDD AB				
FBVDD AC				
FBVDD AD				
FBVDD AE				
FBVDD AF				
FBVDD AG				
FBVDD AH				
FBVDD AI				
FBVDD AJ				
FBVDD AK				
FBVDD AL				
FBVDD AM				
FBVDD AN				
FBVDD AO				
FBVDD AP				
FBVDD AQ				
FBVDD AR				
FBVDD AS				
FBVDD AT				
FBVDD AU				
FBVDD AV				
FBVDD AW				
FBVDD AX				
FBVDD AY				
FBVDD AZ				
FBVDD BA				
FBVDD BB				
FBVDD BC				
FBVDD BD				
FBVDD BE				
FBVDD BF				
FBVDD BG				
FBVDD BH				
FBVDD BI				
FBVDD BJ				
FBVDD BK				
FBVDD BL				
FBVDD BM				
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FBVDD BO				
FBVDD BP				
FBVDD BQ				
FBVDD BR				
FBVDD BS				
FBVDD BT				
FBVDD BU				
FBVDD BV				
FBVDD BW				
FBVDD BX				
FBVDD BY				
FBVDD BZ				
FBVDD CA				
FBVDD CB				
FBVDD CC				
FBVDD CD				
FBVDD CE				
FBVDD CF				
FBVDD CG				
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FBVDD DJ				
FBVDD DK				
FBVDD DL				
FBVDD DM				
FBVDD DN				
FBVDD DO				
FBVDD DP				
FBVDD DQ				
FBVDD DR				
FBVDD DS				
FBVDD DT				
FBVDD DU				
FBVDD DV				
FBVDD DW				
FBVDD DX				
FBVDD DY				
FBVDD DZ				
FBVDD EA				
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FBVDD GN				
FBVDD GO				
FBVDD GP				
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FBVDD HJ				
FBVDD HK				
FBVDD HL				
FBVDD HM				
FBVDD HN				
FBVDD HO				
FBVDD HP				
FBVDD HQ				
FBVDD HR				
FBVDD HS				
FBVDD HT				
FBVDD HU				
FBVDD HV				

# FBC MEMORY 2nd bank 0..31

PLACE ALL DISCRETE COMPONENTS AS NEAR AS POSSIBLE TO MEMORY



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Place plane decoupling caps near DQS-DQM pins.

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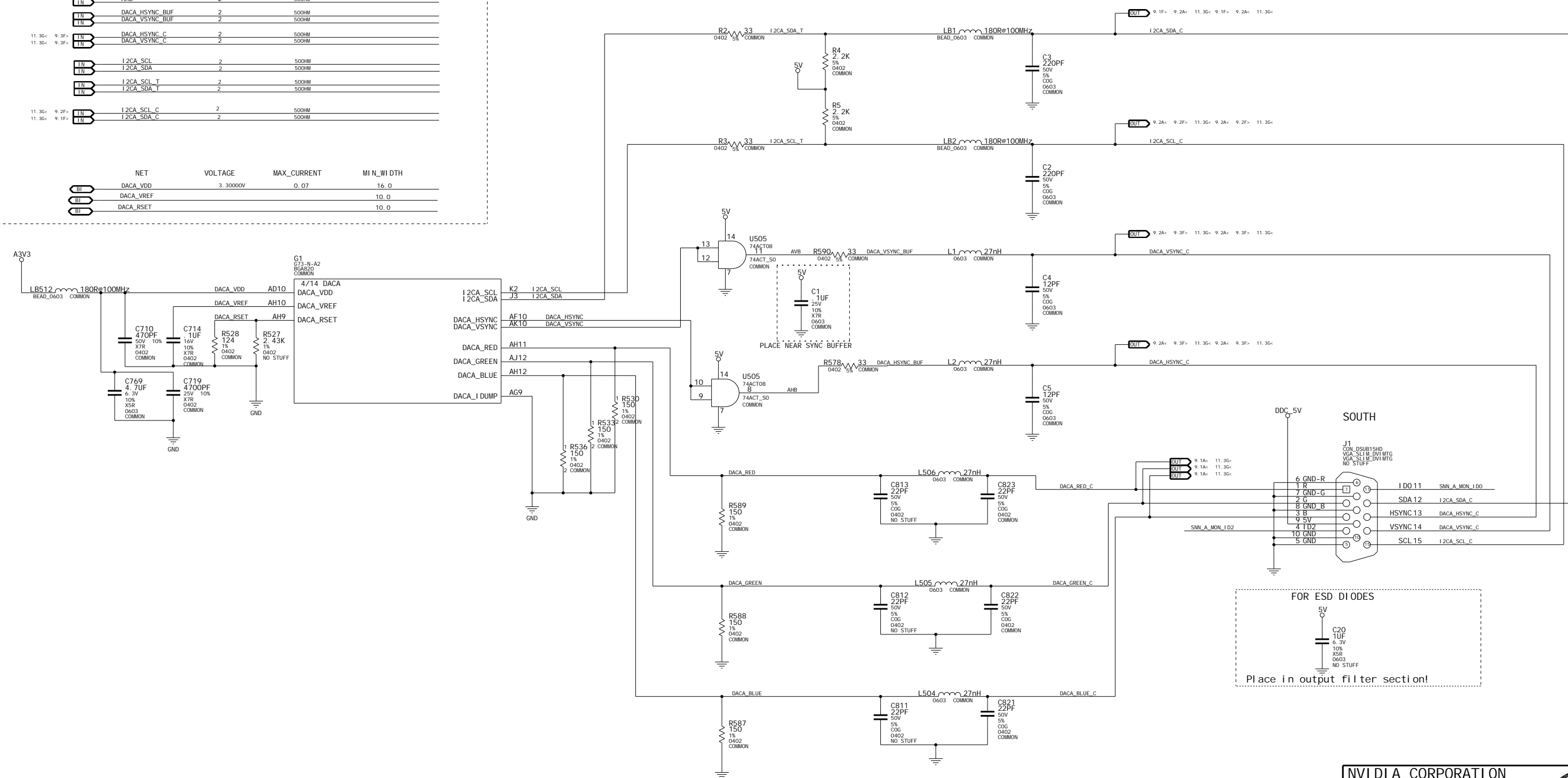


# Primary Display (DACA), SIM DB15

## DACA NET RULES

NET	INV_CRTICAL	INV_IMPEDANCE	DIFFPAIR
DACA_RED	1	560HM	
DACA_GREEN	1	560HM	
DACA_BLUE	1	560HM	
DACA_RED_C	1	560HM	
DACA_GREEN_C	1	560HM	
DACA_BLUE_C	1	560HM	
DACA_HSYNC	2	500HM	
DACA_VSYNC	2	500HM	
AVB	2	500HM	
AHB	2	500HM	
DACA_HSYNC_BUF	2	500HM	
DACA_VSYNC_BUF	2	500HM	
DACA_HSYNC_C	2	500HM	
DACA_VSYNC_C	2	500HM	
I2CA_SCL	2	500HM	
I2CA_SDA	2	500HM	
I2CA_SCL_T	2	500HM	
I2CA_SDA_T	2	500HM	
I2CA_SCL_C	2	500HM	
I2CA_SDA_C	2	500HM	
DACA_VDD		3.30000V	16.0
DACA_VREF			10.0
DACA_RSET			10.0

## DACA RGB-FILTER



FOR ESD DIODES  
 Place in output filter section!

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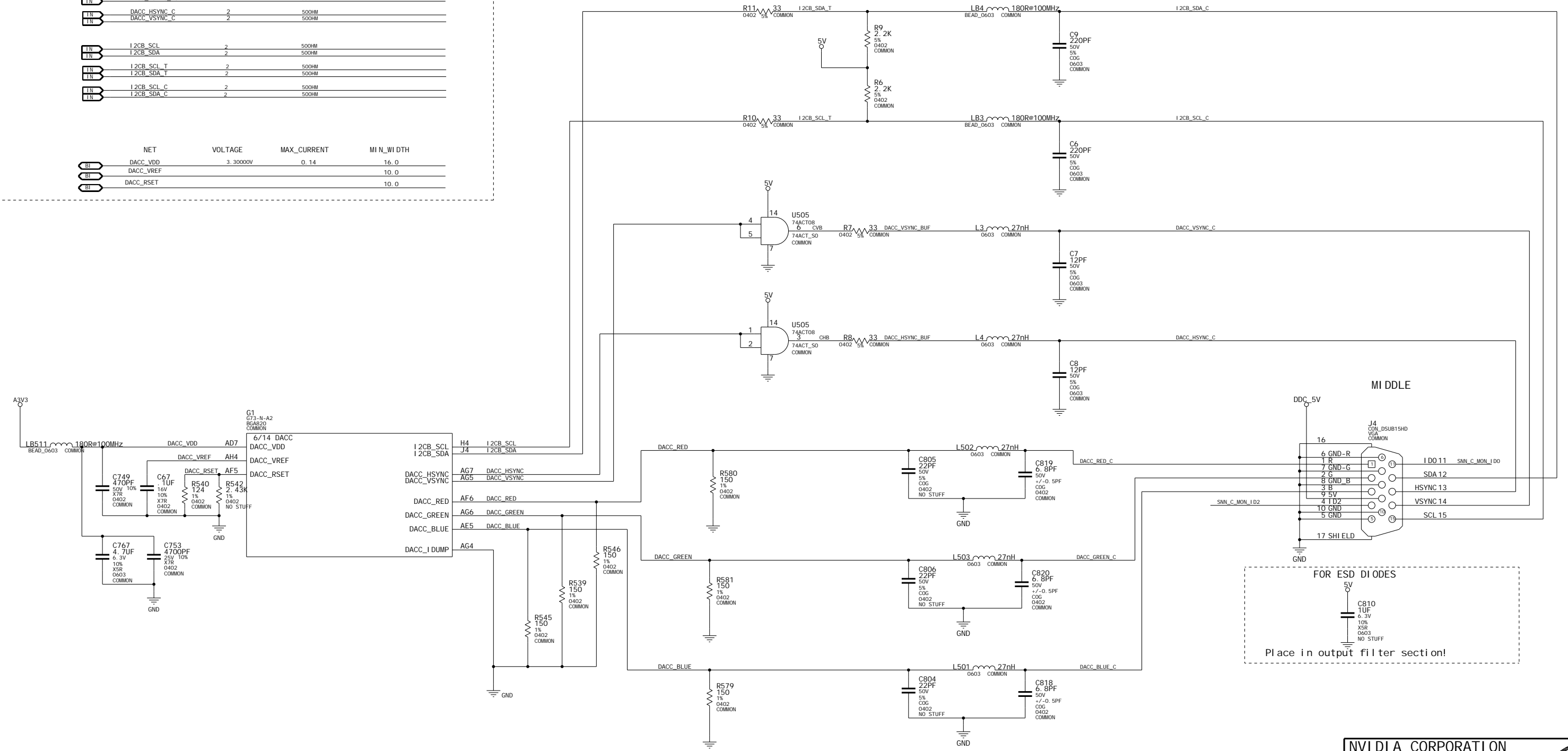
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# DACC NET RULES

NET	INV_CRITICAL	INV_IMPEDANCE	DIFFPAIR
I2C_SCL	1	50OHM	
I2C_SDA	1	50OHM	
I2C_SCL_T	1	50OHM	
I2C_SDA_T	1	50OHM	
I2C_SCL_C	1	50OHM	
I2C_SDA_C	1	50OHM	
DACC_VDD	1	50OHM	
DACC_VREF	1	50OHM	
DACC_RSET	1	50OHM	
DACC_RED	1	50OHM	
DACC_GREEN	1	50OHM	
DACC_BLUE	1	50OHM	
DACC_I_DUMP	1	50OHM	
DACC_HSYNC	2	50OHM	
DACC_VSYNC	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
DACC_HSYNC_BUF	2	50OHM	
DACC_VSYNC_BUF	2	50OHM	
DACC_HSYNC_C	2	50OHM	
DACC_VSYNC_C	2	50OHM	
DACC_VDD	3.30000V	0.14	16.0
DACC_VREF			10.0
DACC_RSET			10.0

# Secondary Display (DACC), DB15

## DACC RGB-FILTER



FOR ESD DIODES  
 Place in output filter section!

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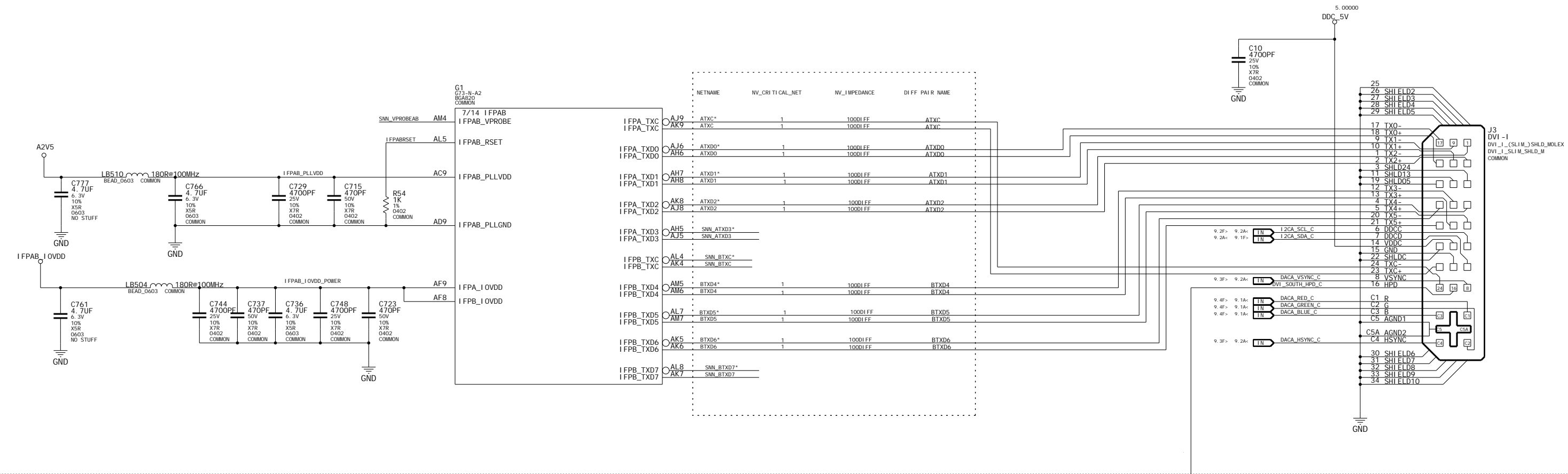
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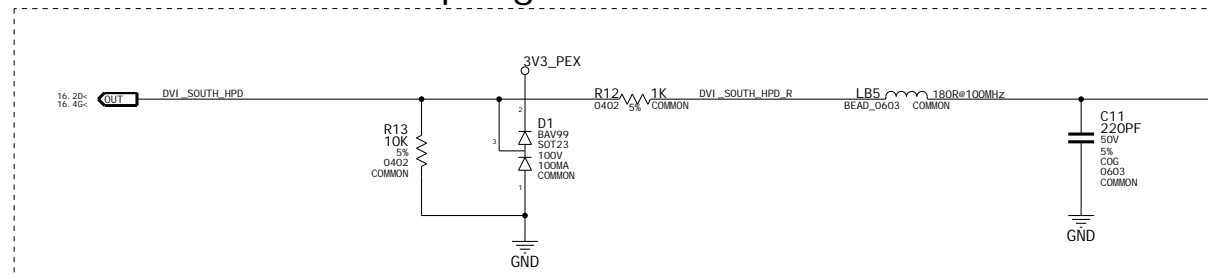
# INTERNAL TMD5 .. LINK A & B

## IFPAB NET RULES

NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FF PAI R
IFPAB_PLLVDD	2.50000V	0.04	16.0
IFPABRSET			12.0

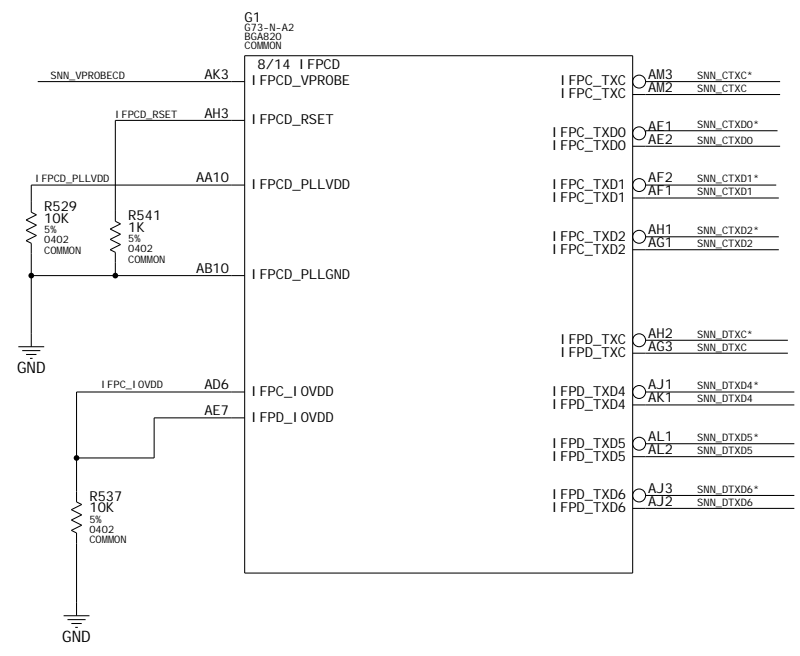


### Hotplug Detection



INTERNAL TMD5 .. LINK C

IFPAB NET RULES



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PAGE DETAIL	TMD5 LINK C

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NV_PN	600-10900-0000-000		
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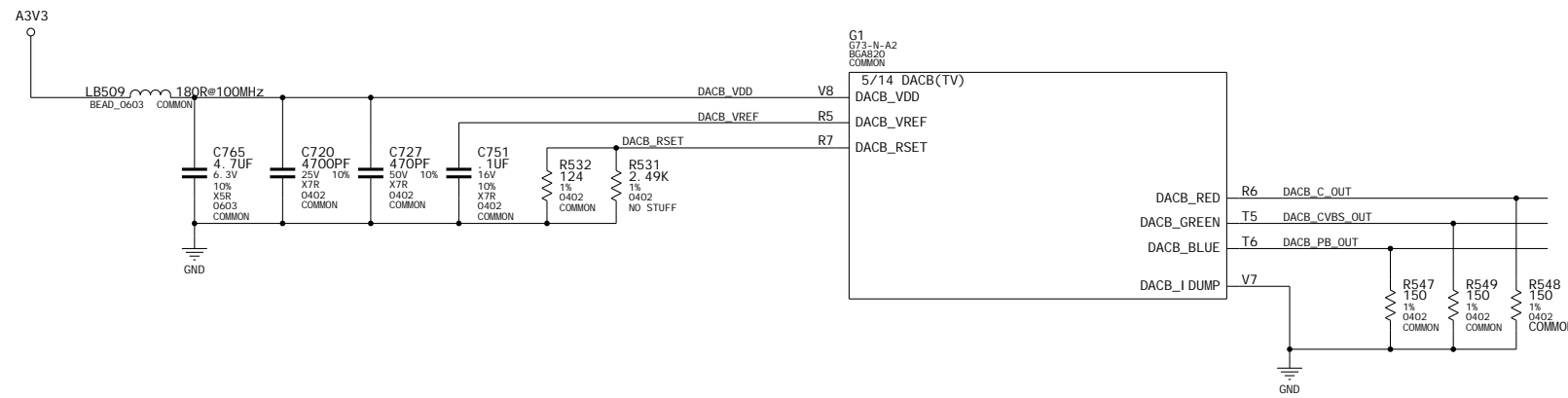
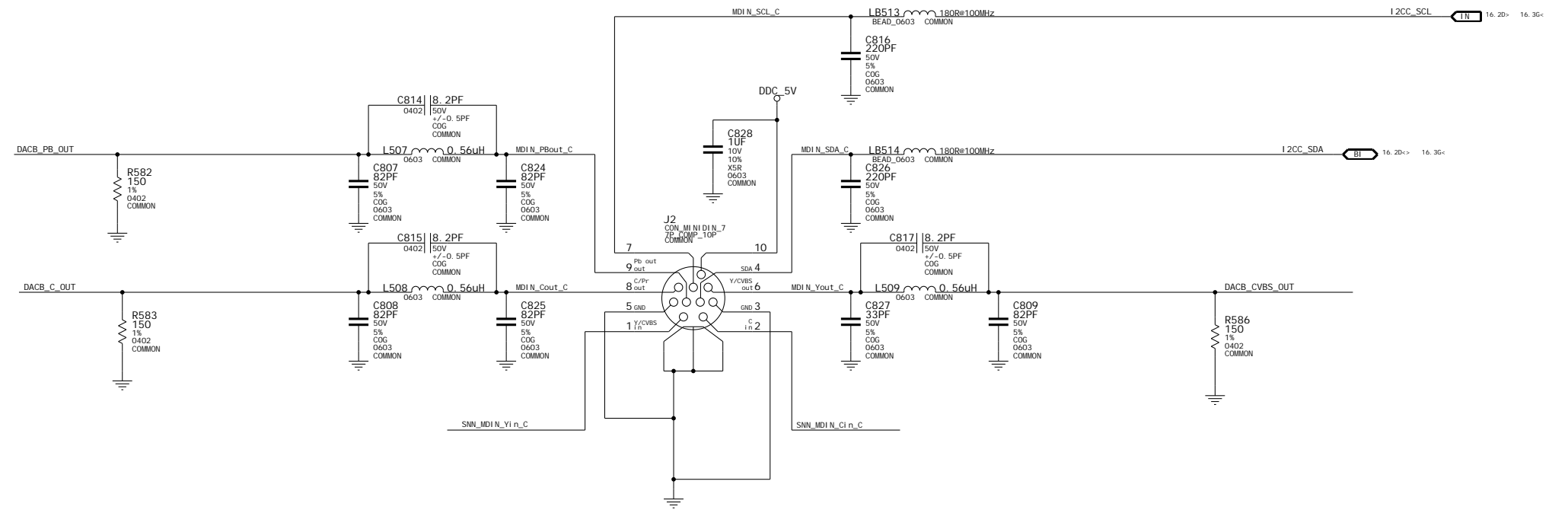


# DACB . . Mi ni DI N VI DEO OUT CONNECTOR

## DACB NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
DACB_C_OUT	1	56OHM	
MDI_N_COUT_C	1	56OHM	
DACB_CVBS_OUT	1	56OHM	
MDI_N_YOUT_C	1	56OHM	
DACB_PB_OUT	1	56OHM	
MDI_N_PBOUT_C	1	56OHM	

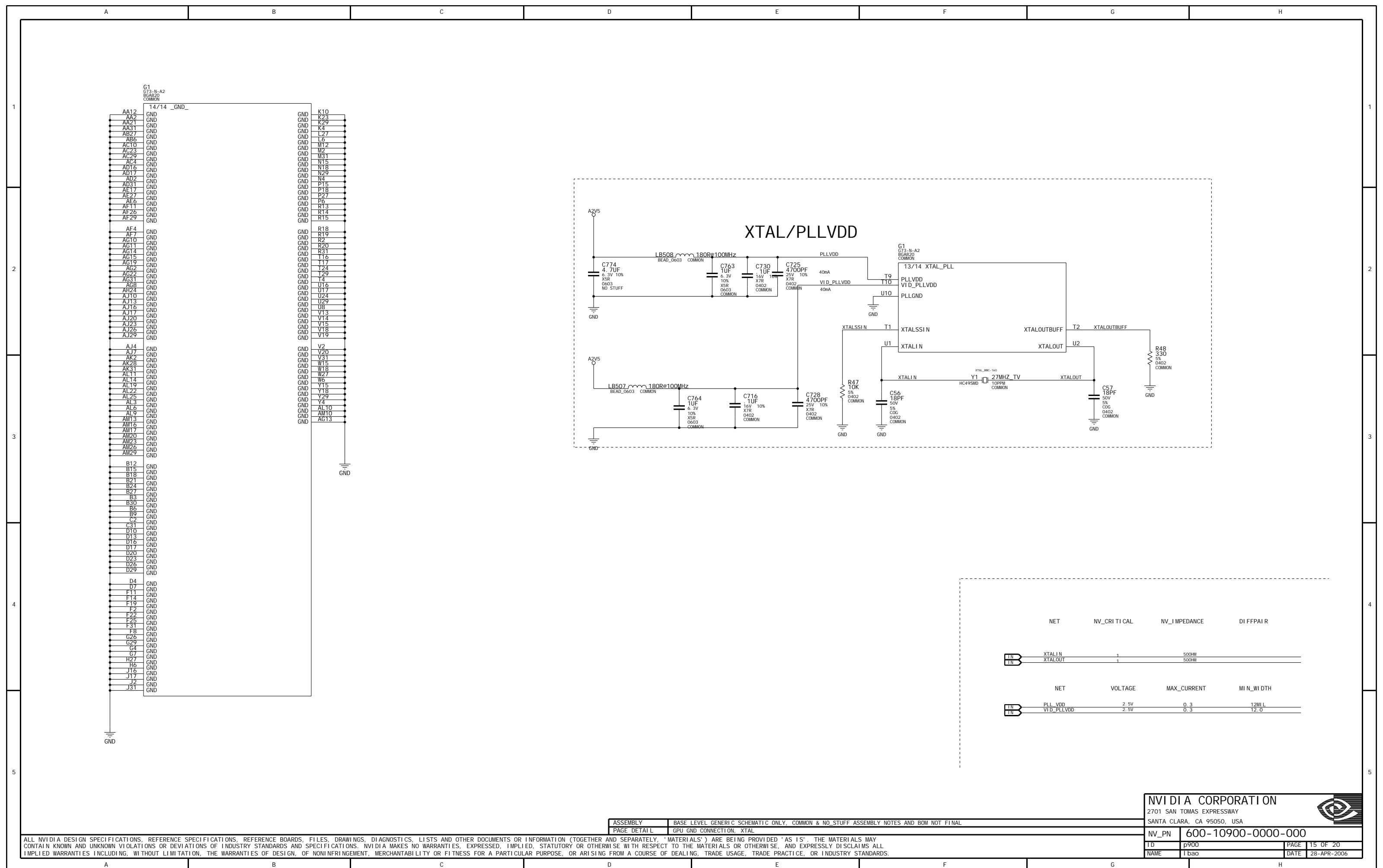
NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DACB_VDD	3.30000V	0.07	16.0
DACB_VREF			16.0
DACB_RSET			16.0



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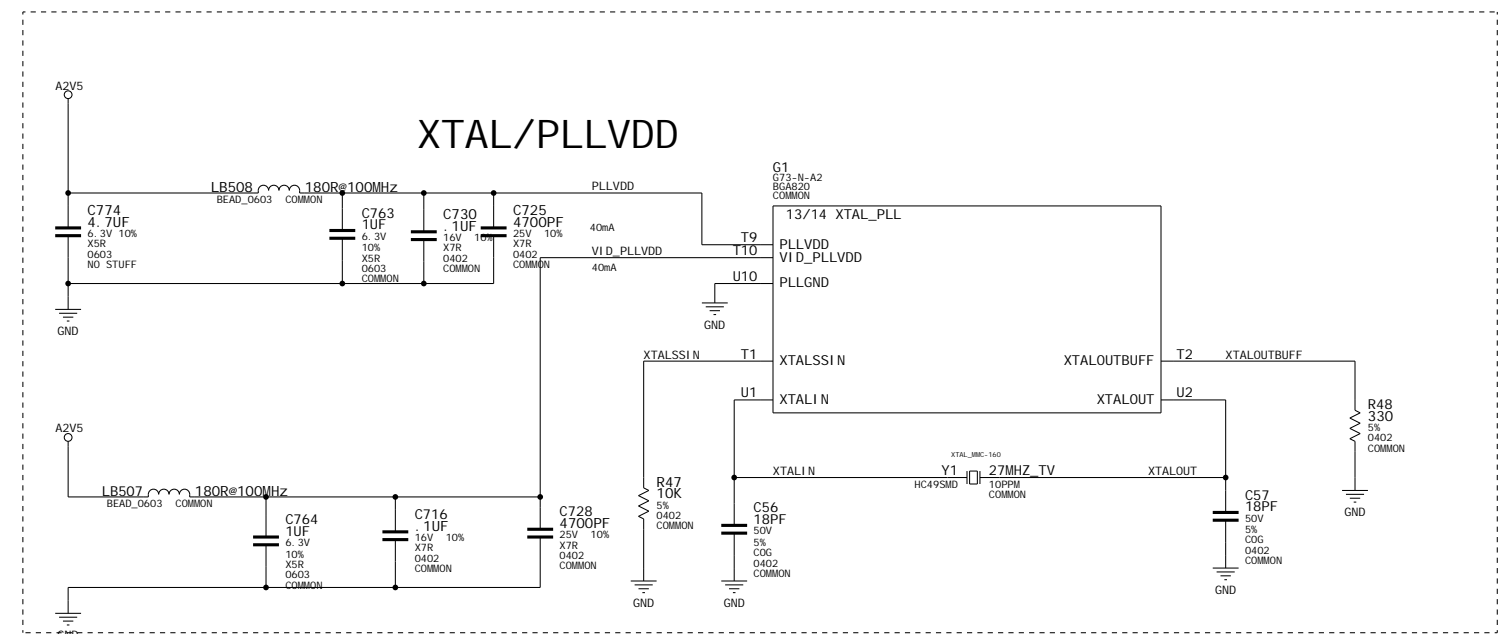
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL		
PAGE	DETAIL	DACB FILTERS, SYNC STRIPPER, MINI DIN CONNECTOR NORTH, HDTV HEADER	
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G1  
G73-N-A2  
BGA820  
COMMON

14/14 _GND_	GND	K10
AA12	GND	K23
AA2	GND	K29
AA21	GND	K4
AA31	GND	L27
AB27	GND	L6
AB6	GND	M12
AC10	GND	M2
AC23	GND	M31
AC29	GND	N15
AC4	GND	N18
AD16	GND	N29
AD17	GND	N4
AD2	GND	N15
AD3	GND	N18
AD31	GND	P15
AE17	GND	P18
AE27	GND	P27
AE6	GND	P6
AF11	GND	R13
AF26	GND	R14
AF29	GND	R15
AF4	GND	R18
AF7	GND	R19
AG10	GND	R2
AG11	GND	R20
AG14	GND	R31
AG15	GND	T16
AG19	GND	T17
AG2	GND	T24
AG22	GND	T29
AG31	GND	T4
AG8	GND	U16
AH24	GND	U17
AJ10	GND	U24
AJ13	GND	U29
AJ16	GND	U8
AJ17	GND	V13
AJ20	GND	V14
AJ23	GND	V15
AJ26	GND	V18
AJ29	GND	V19
AJ4	GND	V2
AJ7	GND	V20
AK2	GND	V31
AK28	GND	W15
AK31	GND	W18
AL11	GND	W27
AL14	GND	W5
AL19	GND	Y15
AL22	GND	Y18
AL25	GND	Y29
AL3	GND	Y4
AL6	GND	AL10
AL9	GND	AM10
AM13	GND	AG13
AM16	GND	
AM17	GND	
AM20	GND	
AM23	GND	
AM26	GND	
AM29	GND	
B12	GND	
B15	GND	
B18	GND	
B21	GND	
B24	GND	
B27	GND	
B3	GND	
B30	GND	
B6	GND	
B9	GND	
C2	GND	
C31	GND	
D10	GND	
D13	GND	
D16	GND	
D17	GND	
D20	GND	
D23	GND	
D26	GND	
D29	GND	
D4	GND	
D7	GND	
F11	GND	
F14	GND	
F19	GND	
F2	GND	
F22	GND	
F23	GND	
F31	GND	
F8	GND	
G26	GND	
G29	GND	
G4	GND	
G7	GND	
H27	GND	
H6	GND	
J16	GND	
J17	GND	
J2	GND	
J31	GND	

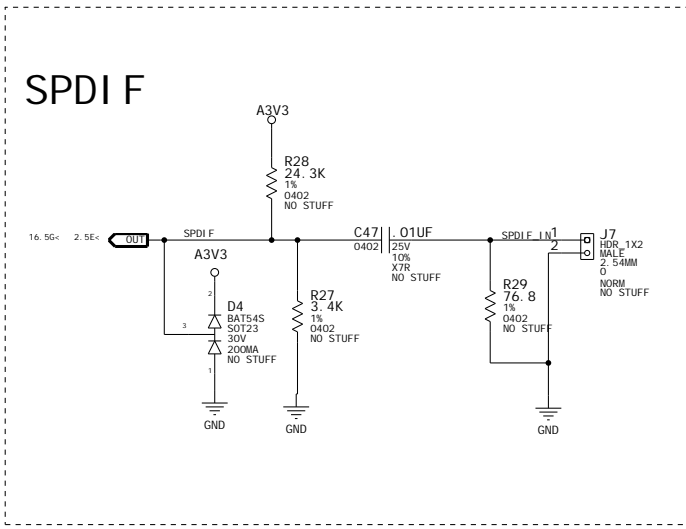
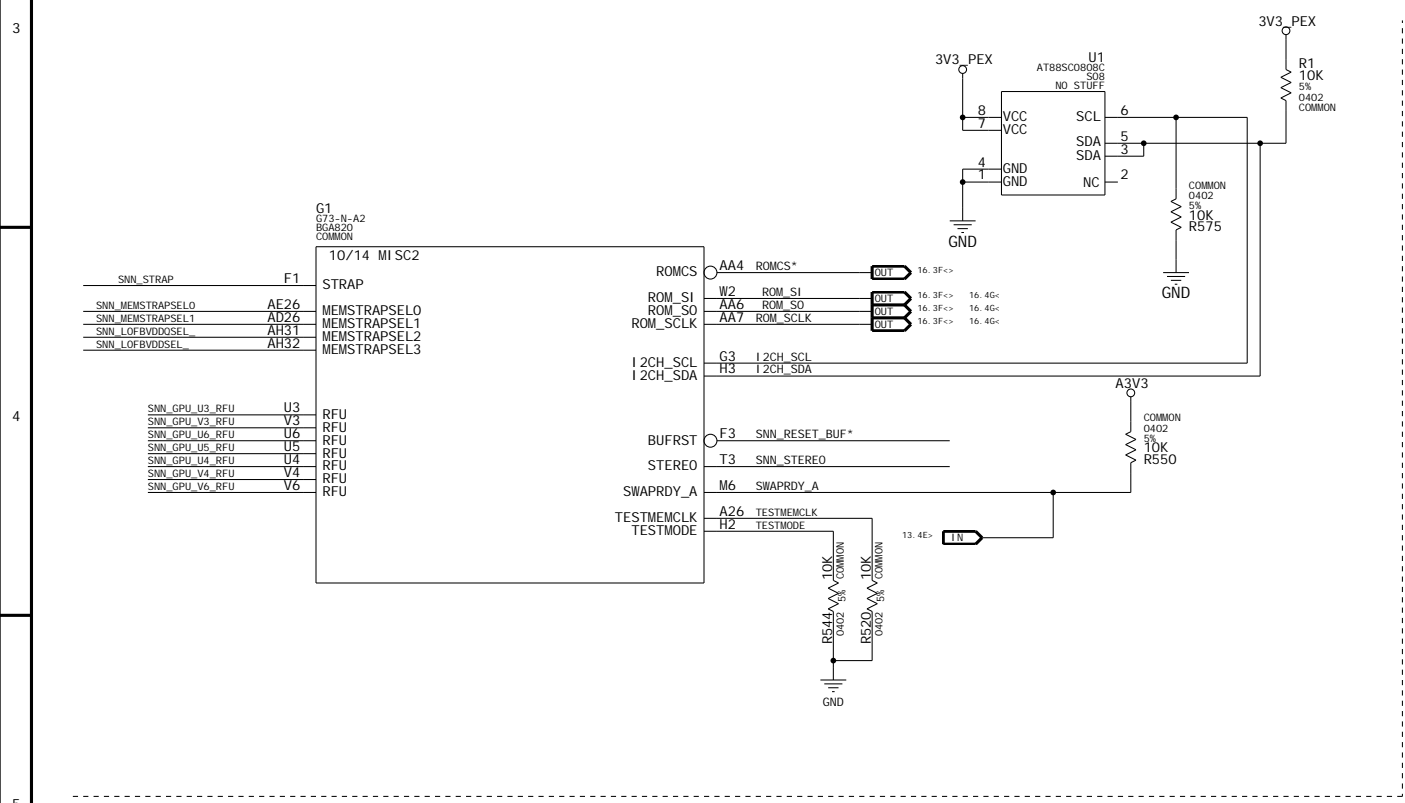
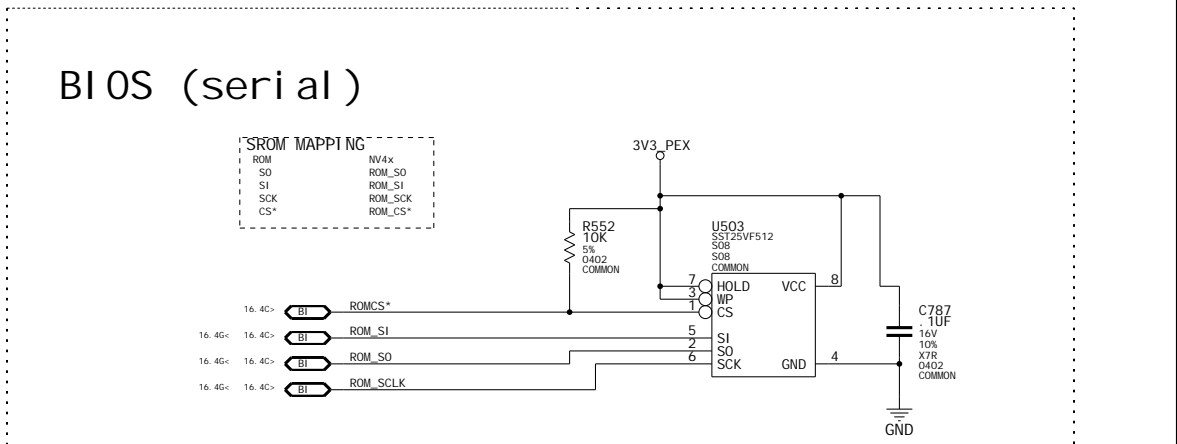
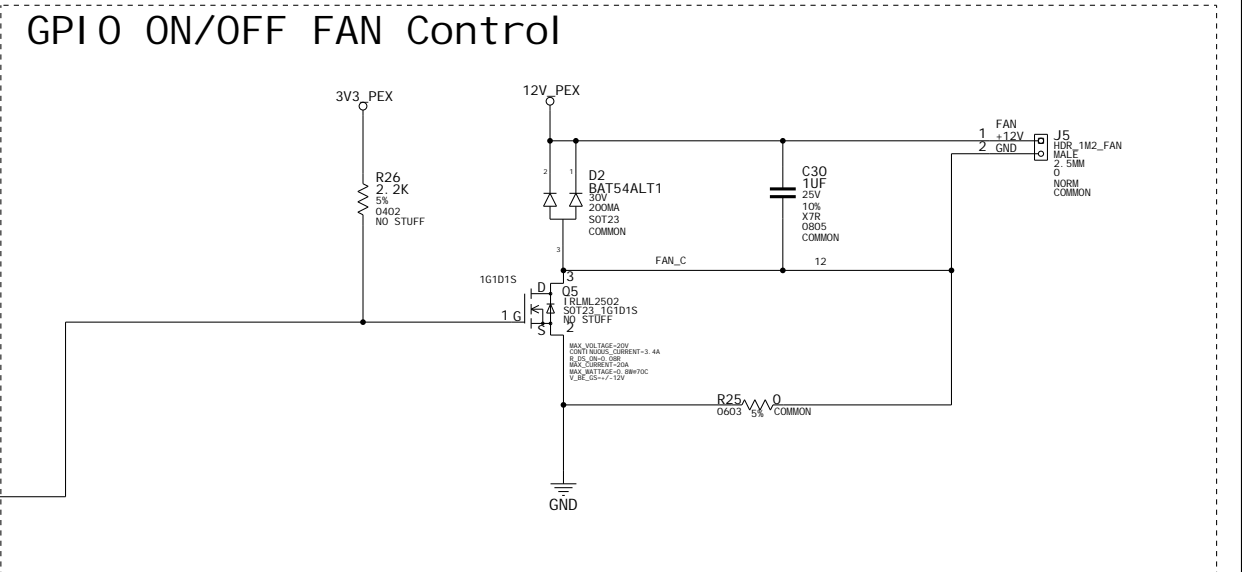
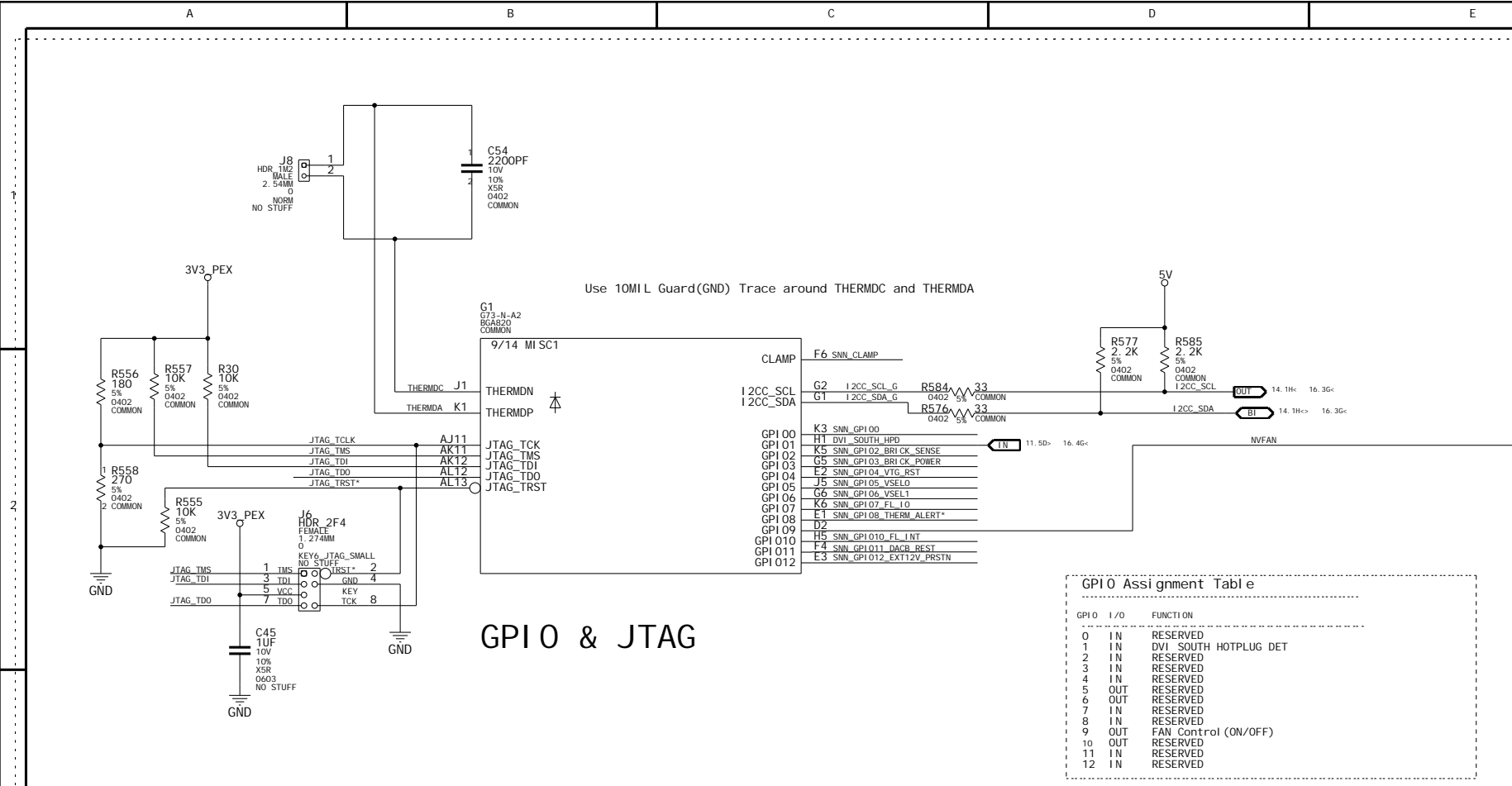


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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL GPU GND CONNECTION, XTAL

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### MISC NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DI_FPAIR
16.2D-> 14.1H<	I2CC_SCL	2	500HM
16.2D-> 14.1H<	I2CC_SDA	2	500HM
16.2D-> 14.1H<	I2CC_SCL_G	2	500HM
16.2D-> 14.1H<	I2CC_SDA_G	2	500HM
16.4C-> 16.3F<	I2CH_SCL	2	500HM
16.4C-> 16.3F<	I2CH_SDA	2	500HM
16.4C-> 16.3F<	ROM_CS*	2	500HM
16.4C-> 16.3F<	ROM_SI	2	500HM
16.4C-> 16.3F<	ROM_SO	2	500HM
16.4C-> 16.3F<	ROM_SCLK	2	500HM
16.2D-> 11.5D->	DVI_SOUTH_HPD	2	500HM
16.4D-> 2.5E<	SPDIF	1	500HM
16.4D-> 2.5E<	SPDIF_IN	1	500HM

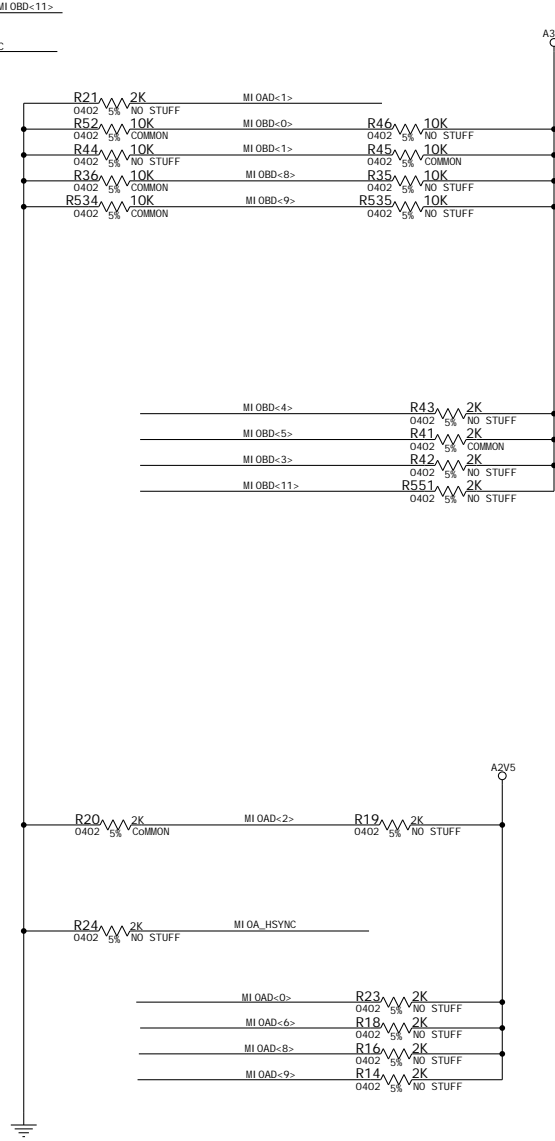
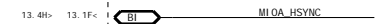
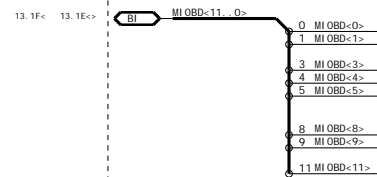
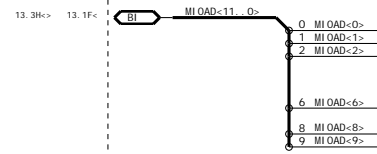


# BIOS, Straps, Misc

## Straps

Assembly: BIOS

## Mechanical parts

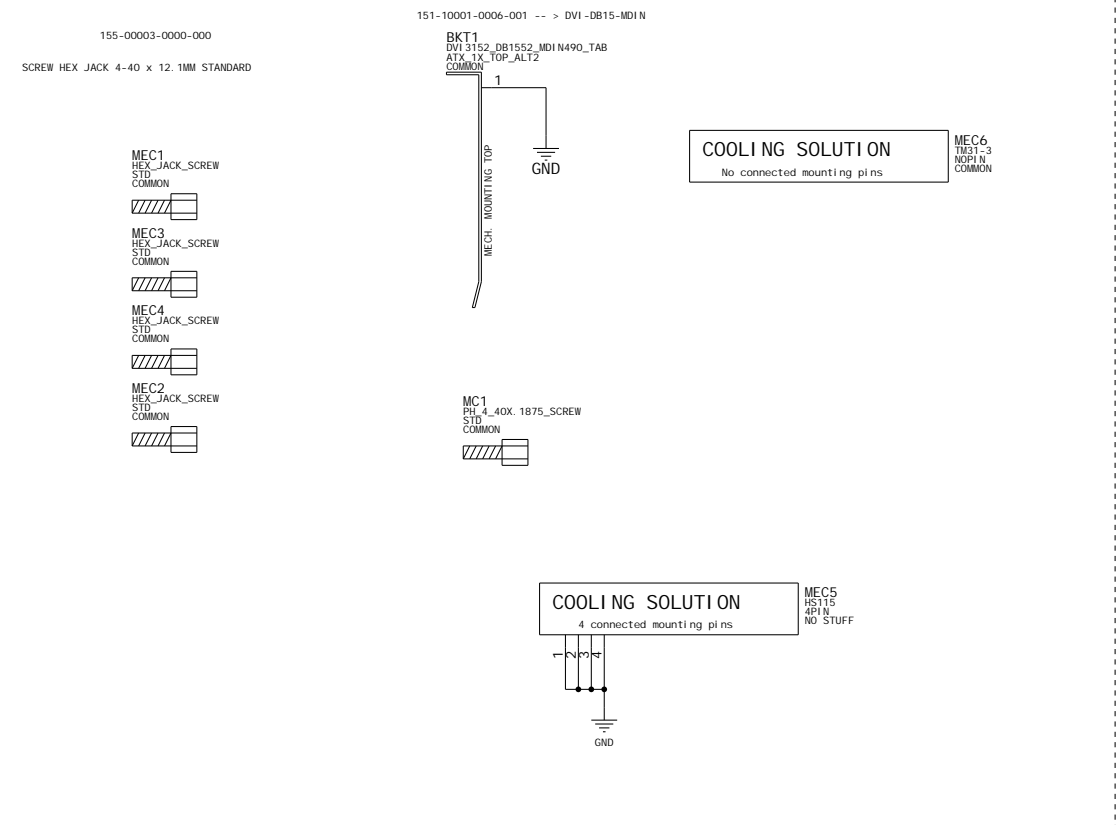


REG: NV\_PEXTDEV\_BOOT\_0

Bit Signal	VALUE_ID	VALUES
00: PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED
01: SUB_VENDOR	SUB_VENDOR	1 NORMAL 0 NO BIOS
02: RAM_CFG_0	RAM_CFG[3:0]	1 Read from BIOS 0000 8Mx16 DDR2 128BIT 0001 RFU 0010 16Mx16 DDR2 128BIT 0011 RFU 0100 RFU 0101 RFU 0110 RFU 0111 RFU
03: RAM_CFG_1		1000 8Mx16 DDR2 64BIT 1001 RFU 1010 16Mx16 DDR2 64BIT 1011 RFU
04: RAM_CFG_2		1100 RFU 1101 RFU 1110 RFU
05: RAM_CFG_3		1111 RFU
06: CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz 10 27.000 Mhz
22: CRYSTAL_1		11 UNKNOWN
07: TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC 10 PAL
08: TV_MODE_1		11 CRT
09: AGP_SBA_Enable	AGP_SBA	0 AGP_SBA enabled 1 AGP_SBA disabled
10: AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled
11: AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled
12: PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x140 ... 1111 0x014F 0000 (default 0x140) 0101 (0x145)
13: PCI_DEVID_1		
20: PCI_DEVID_2		
21: PCI_DEVID_3		
14: BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP
15: FP_FACE	FP_FACE[0]	0 24BIT 1 12BIT (DEFAULT)
23: FB_0	FB[1:0]	00 64M 01 128M 10 256M (DEFAULT) 11 512M
24: FB_1		0 BRIDGE disabled 1 BRIDGE enabled
25: BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled
26: BR_128M		BR bits are ignored if BRIDGE is disabled
27: BR_AGP		
28: BR_IO		
29: ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F 10 Serial_SST45VF 11 RFU
30: ROM_TYPE_1		
16: USER_0	STRAP_USER[3:0]	0000 (default)
17: USER_1		
18: USER_2		
19: USER_3		
31: SLOT_CLOCK_CFG		0 COMMON PCIe REF CLK enabled 1 COMMON PCIe REF CLK disabled

REG: NV\_STRAP\_1

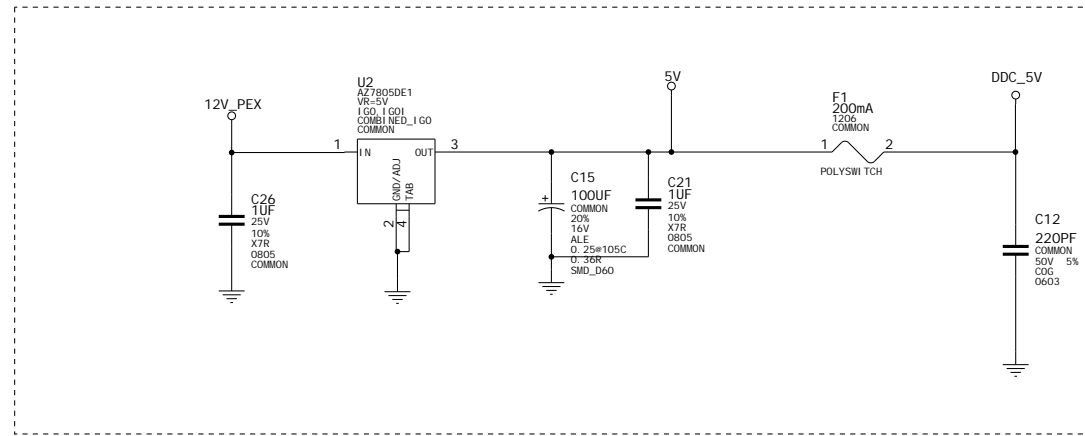
Bit Signal	VALUE_ID	VALUES
11: PEX_PLL_EN_TERM100		0 (default -- internal term on)
12: 3GI0_PADCFG_LUT_ADR[0]		
13: 3GI0_PADCFG_LUT_ADR[1]		
14: 3GI0_PADCFG_LUT_ADR[2]		



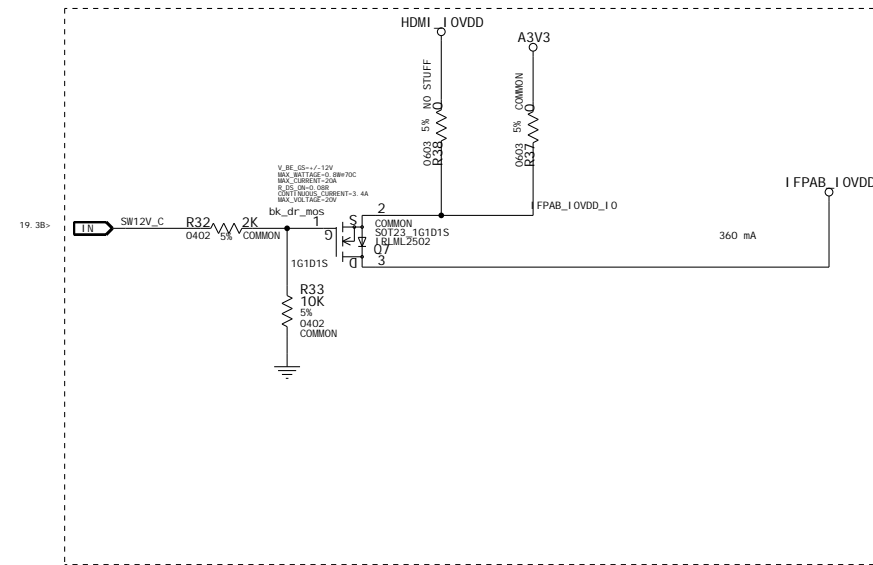
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# Power Supply: TMDS\_I0VDD A3V3 A2V5

## DDC 5V

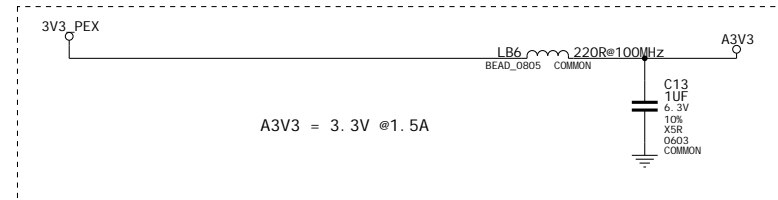


## TMDS I0 SUPPLY WITH BACKDRIVE PROTECTION



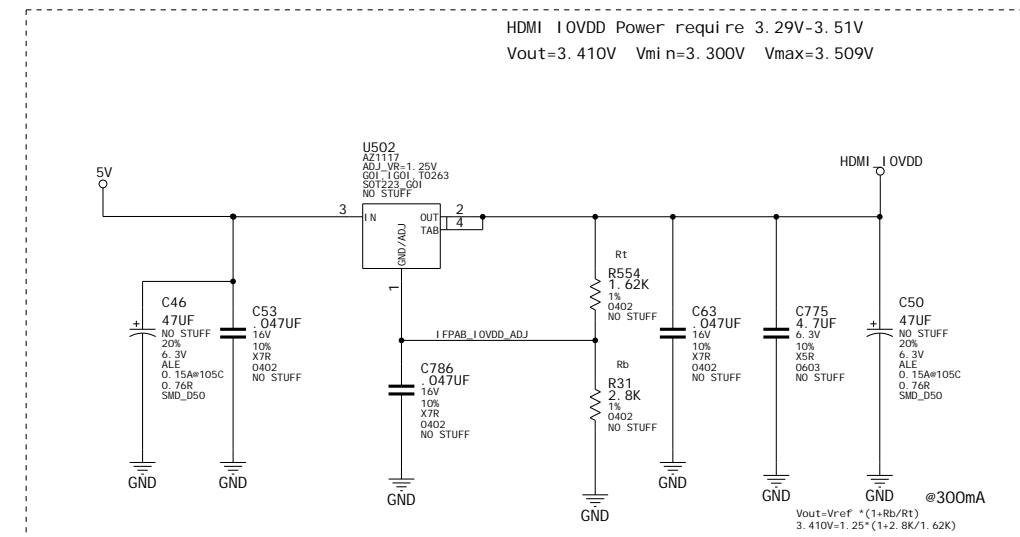
NETNAME	MAX_CURRENT	MIN_LENGTH	VOLTAGE
DDC_5V	0.1	12.0	5.00000V
A3V3	1.5	30.0	3.30000V
IFPAB_I0VDD	0.3	16	3.30000V
GND		35.0	0.000000V

## A3V3 Power Supply



## HDMI I0 SUPPLY

HDMI I0VDD Power require 3.29V-3.51V  
Vout=3.410V Vmin=3.300V Vmax=3.509V



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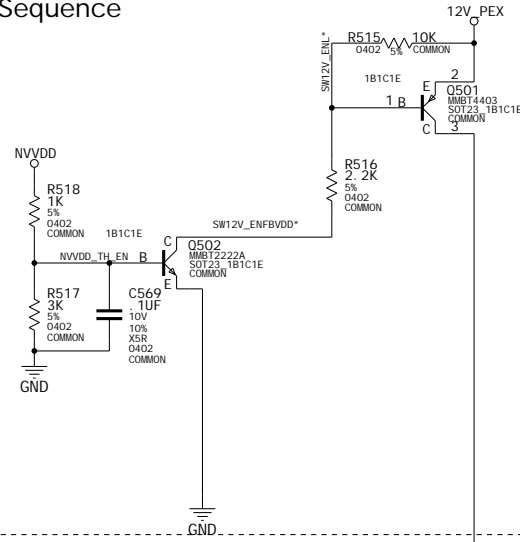
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY. COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	POWER SUPPLY: TMDS_I0VDD, 5V, A3V3



# PowerSupply111: FBVDDQ, FBVTT, PLLVDD

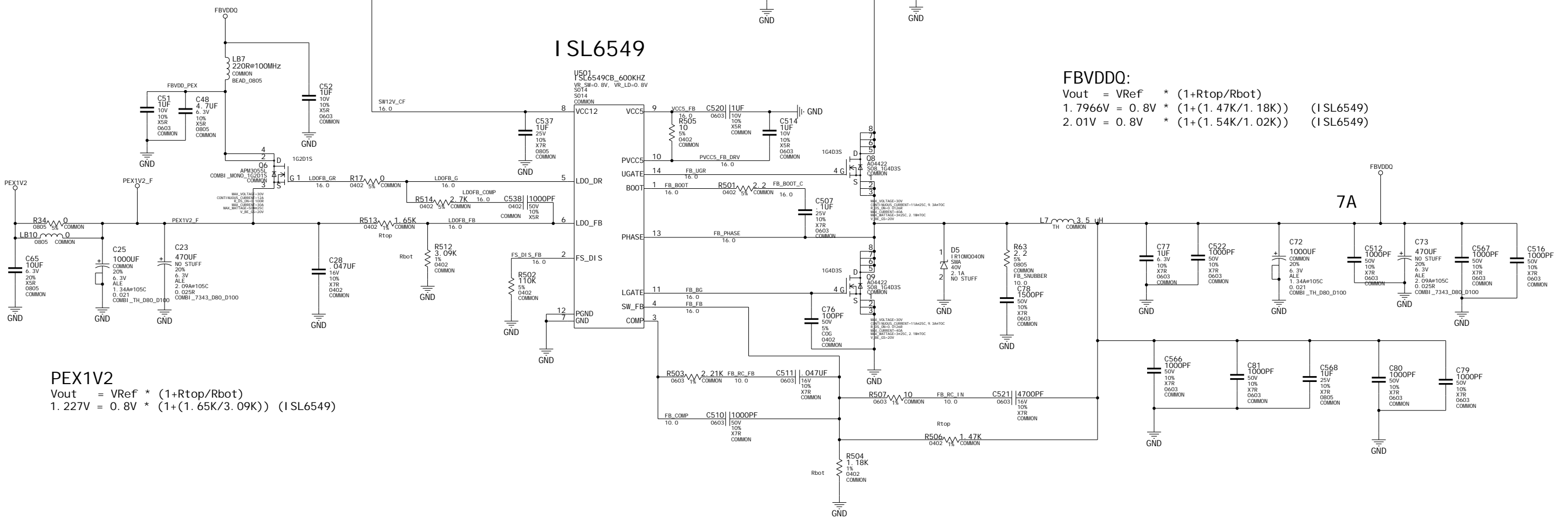
Net Name	LINE_WIDTH	CURRENT	Vol tage
FBVDDQ	12MIL		1.8V
PEX1V2_F	24MIL	1.5	1.2V

Power Sequence



## ISL6549

FBVDDQ:  
 $V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$   
 $1.7966V = 0.8V * (1 + (1.47K/1.18K))$  (ISL6549)  
 $2.01V = 0.8V * (1 + (1.54K/1.02K))$  (ISL6549)



PEX1V2  
 $V_{out} = V_{Ref} * (1 + R_{top}/R_{bot})$   
 $1.227V = 0.8V * (1 + (1.65K/3.09K))$  (ISL6549)

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ASSEMBLY PAGE DETAIL BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO\_STUFF ASSEMBLY NOTES AND BOM NOT FINAL PowerSupply111: FBVDDQ, PLLVDD

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