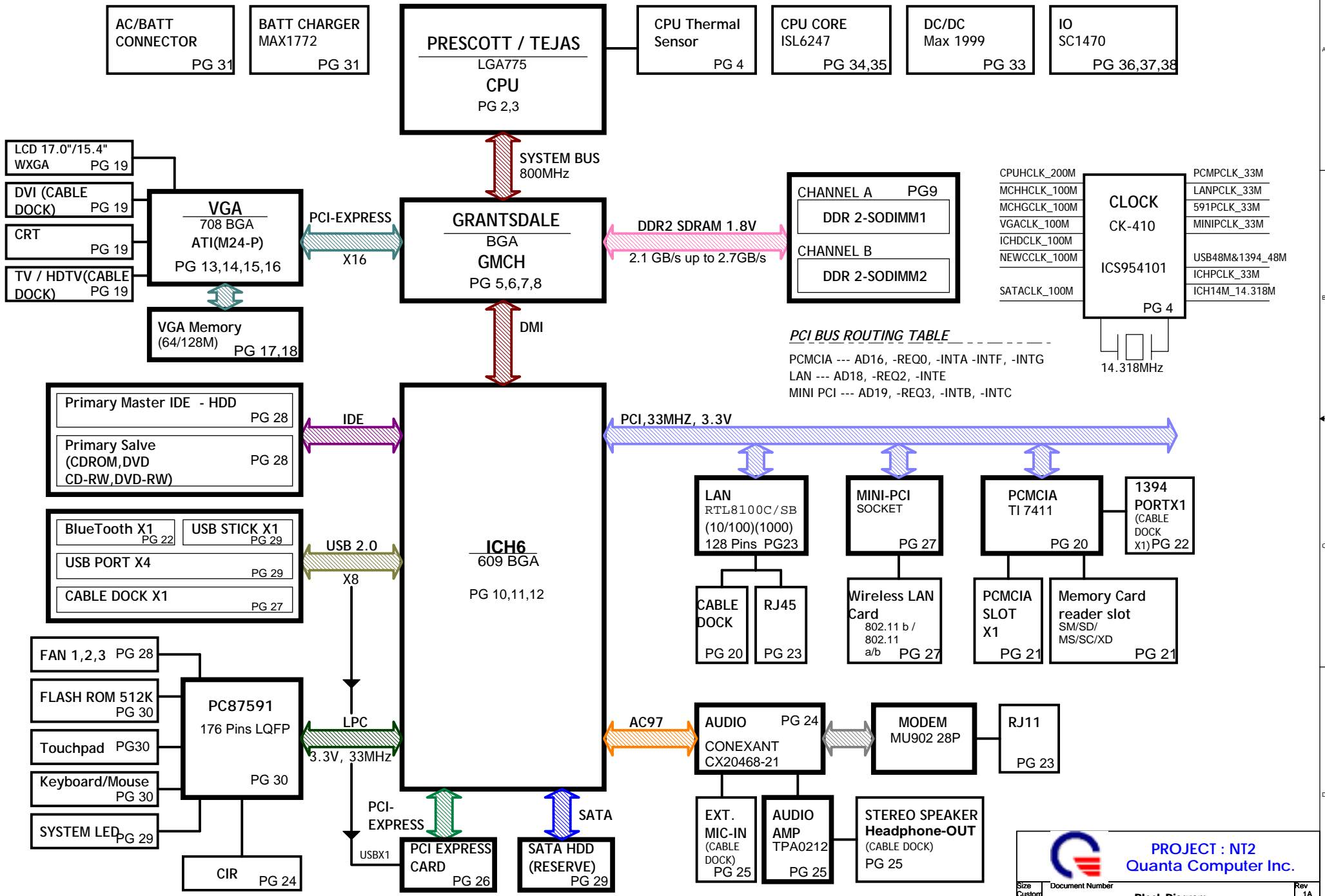


MODEL	REV	CHANGE LIST	Model	NT2 M/B BOARD	
			Page	FM	TO
NT2 M/B	1A	FIRST RELEASE	1	1A	2A
	2A	<p>PAGE1: Change COREVTT power good circuit for CORE VCC Sequence.</p> <p>PAGE4,11: Add CPU PROCHOT CIRCUT (Throttle) at battery only.</p> <p>PAGE7: Because system 2.5V will change to 1.8V for support 1.8V VRAM so reserve one LED for support GMCH 2.5V voltage.</p> <p>PAGE11: Add one system ID for NT2B, and assign GPO19 pin to support CPU PROCHOT (Throttle) function.</p> <p>PAGE13: Add M24 GPIO14 to support TV_OUT select forTampa2, and reserve strap pin for VGA Memory tyep setting.</p> <p>PAGE14: Add LDO for VGA2.5 when system 2.5V change to 1.8V for support 1.8V VRAM.</p> <p>PAGE14: Reserve LDO of VGA1.5V for tune VGA power sequence.</p> <p>PAGE15: Add VGA BIOS "-ROMCS" control pin for support VRAM 256MB and reserve Memory type strip pin.</p> <p>PAGE16: Add Flash ROM for VGA BIOS.</p> <p>PAGE19: Modify DIODE Pin Deffine for BAV99 Part.</p> <p>PAGE21: Add pull up resistor for XD "-CE" singnal.</p> <p>PAGE23: Reserve another LAN TRANSFORM FOR 10/100 and reserver one resistor for LAN1.2V source and pull up resistor for GIGA LAN transform terminal pin.</p> <p>PAGE24: Del CIR on board circuit and reserve CN37 for NT2B.</p> <p>PAGE24: Add resistor to lower Cable Dock MIC signal and add more EMI PAD reserve.</p> <p>PAGE25: Modify Headphone CIRCUIT FOR CABLE DOCK.</p> <p>PAGE26: Change PCI EXPRESS Card power circuit - use TI TPS2331; and add CAP of Power plane bridge for EMI reserve.</p> <p>PAGE27: Cable Dock pin define change for match NP2 pin define and add one pin for TV-OUT select.</p> <p>PAGE27: Reserve always turn on the cable dock power circuit and change VA power to VAD.</p> <p>PAGE29: Add two connect for LED board and reserve two LED for NT2B.</p> <p>PAGE30: Add pull-up resistor for Touch PAD power control and DIODE on "-SWI"&amp;"-RUNSCI" for leakage, and reserve schottky diode and resistor for VCC voltage undershoot issue.</p> <p>PAGE31: Add PD32 prevent power VAD with PWR_SRC leakage.</p> <p>PAGE31: Change PR146 and PR72 to 100K because PWM frequence change to 200Hz.</p> <p>PAGE32: Add 1.8V,VGACORE,VGA1.2V voltage discharge circuit.</p> <p>PAGE33: Add PR210 to fix MAX1999.</p> <p>PAGE34: Change PR180 to 0ohm and delete PC36 for COREVTTTPWG signal delay time.</p> <p>PAGE34: Add PR203 NTC 4.7K to control cpu load line.</p> <p>PAGE36: Change 1.8VSUS and 1.5V power circuit of use MAX1845 for enhance transform efficiency.</p> <p>PAGE37: Change VGACORE of use LMV321 for enhance transform efficiency.</p>	2	1A	
			3	1A	
			4	1A	2A
			5	1A	
			6	1A	
			7	1A	2A
			8	1A	
			9	1A	
			10	1A	
			11	1A	2A
			12	1A	
			13	1A	2A
			14	1A	2A
			15	1A	2A
			16	1A	2A
			17	1A	
			18	1A	
			19	1A	2A
			20	1A	
			21	1A	
			22	1A	
			23	1A	2A
			24	1A	2A
			25	1A	2A
			26	1A	2A
			27	1A	2A
			28	1A	
			29	1A	2A
			30	1A	2A
			31	1A	2A
			32	1A	2A
			33	1A	2A
			34	1A	2A
			35	1A	2A
			36	1A	2A
			37	1A	2A
			38	1A	2A



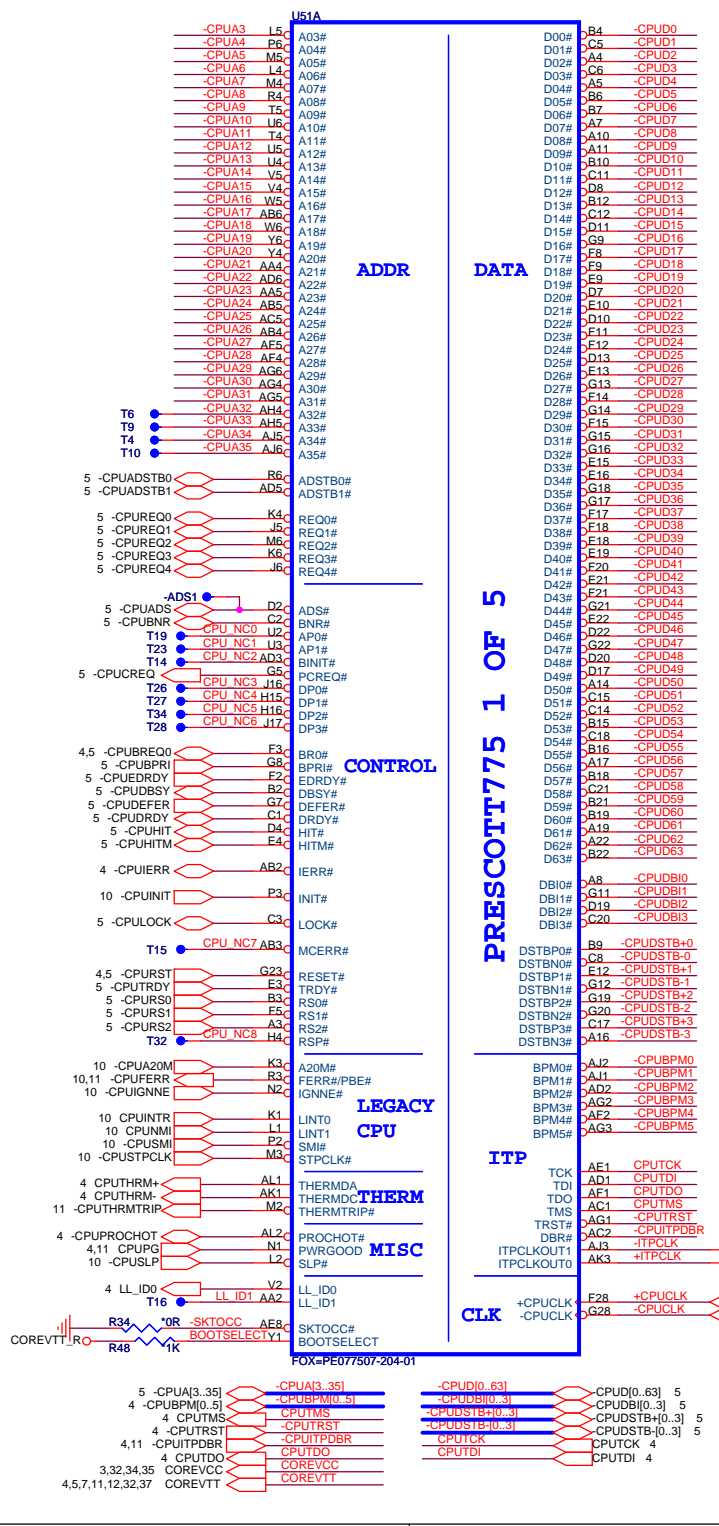
PROJECT:NT2	PCBA NO.	REV: 2A	DOC. NO: 204
APPROVED BY :Tom Wang	CHECK BY:Carey Chen	DRAWING BY:Johnny O	DATE :03/05/2004 SHEET 1

# NT2 - Block Diagram

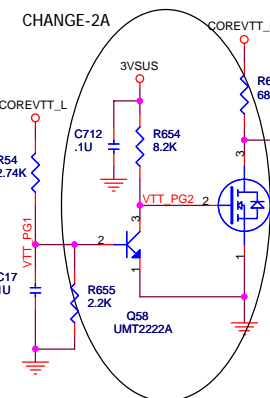
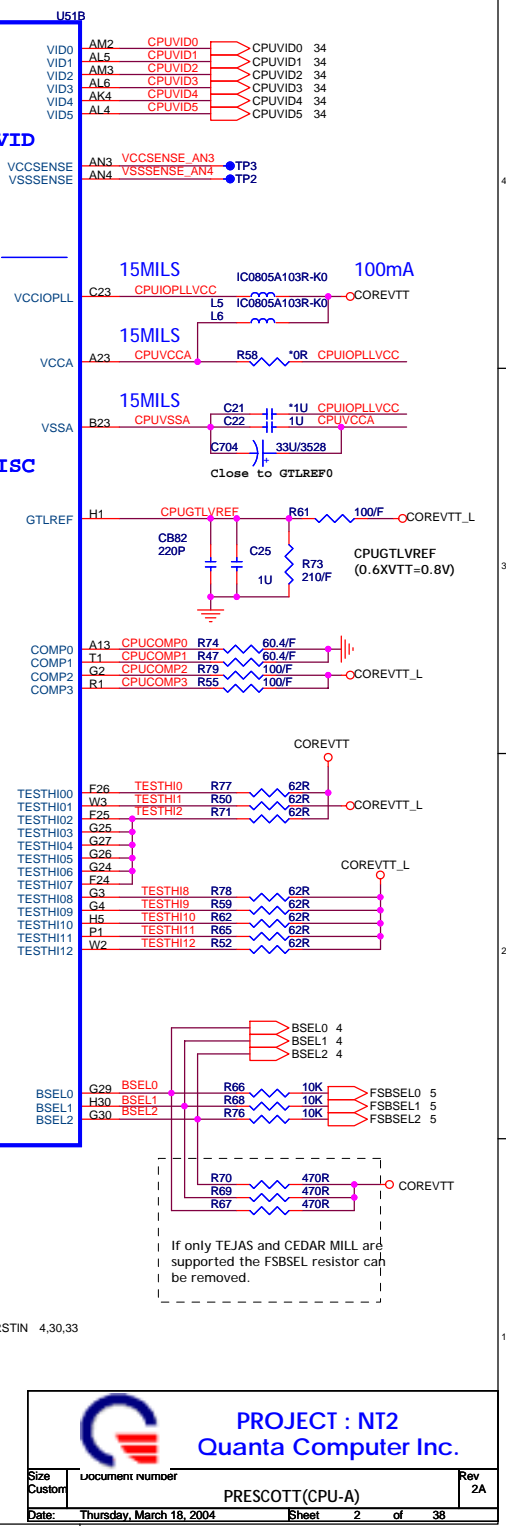
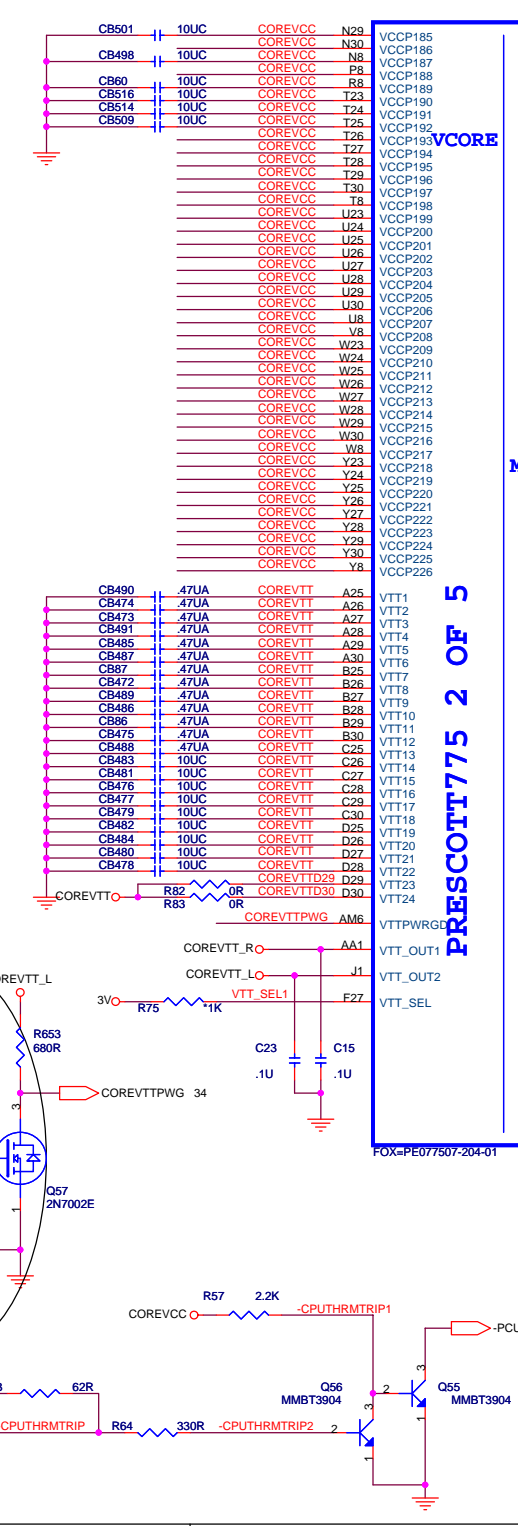


**PCI BUS ROUTING TABLE**

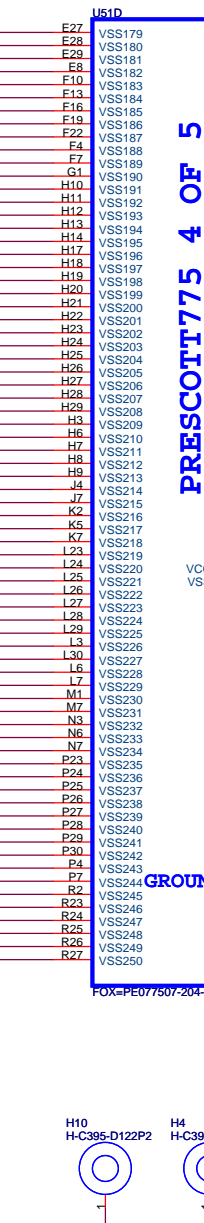
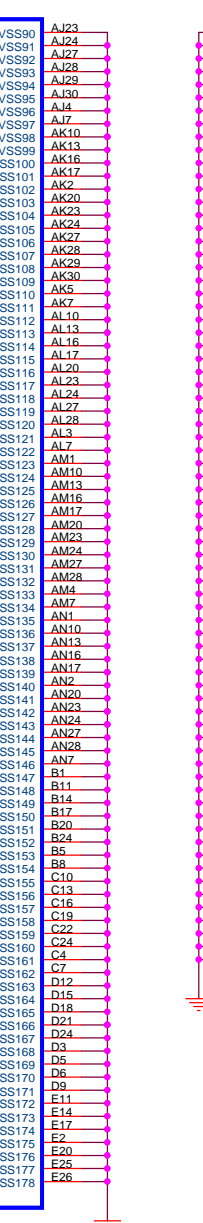
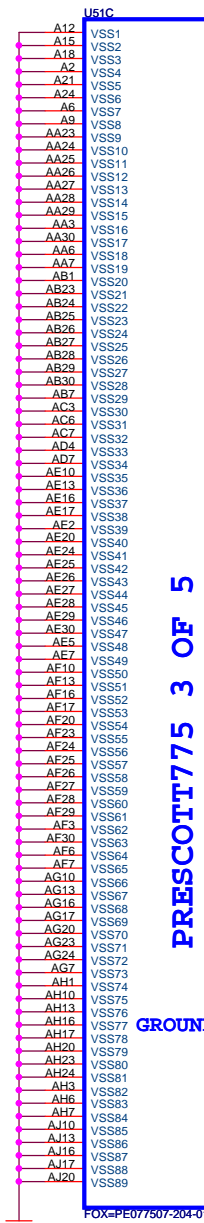
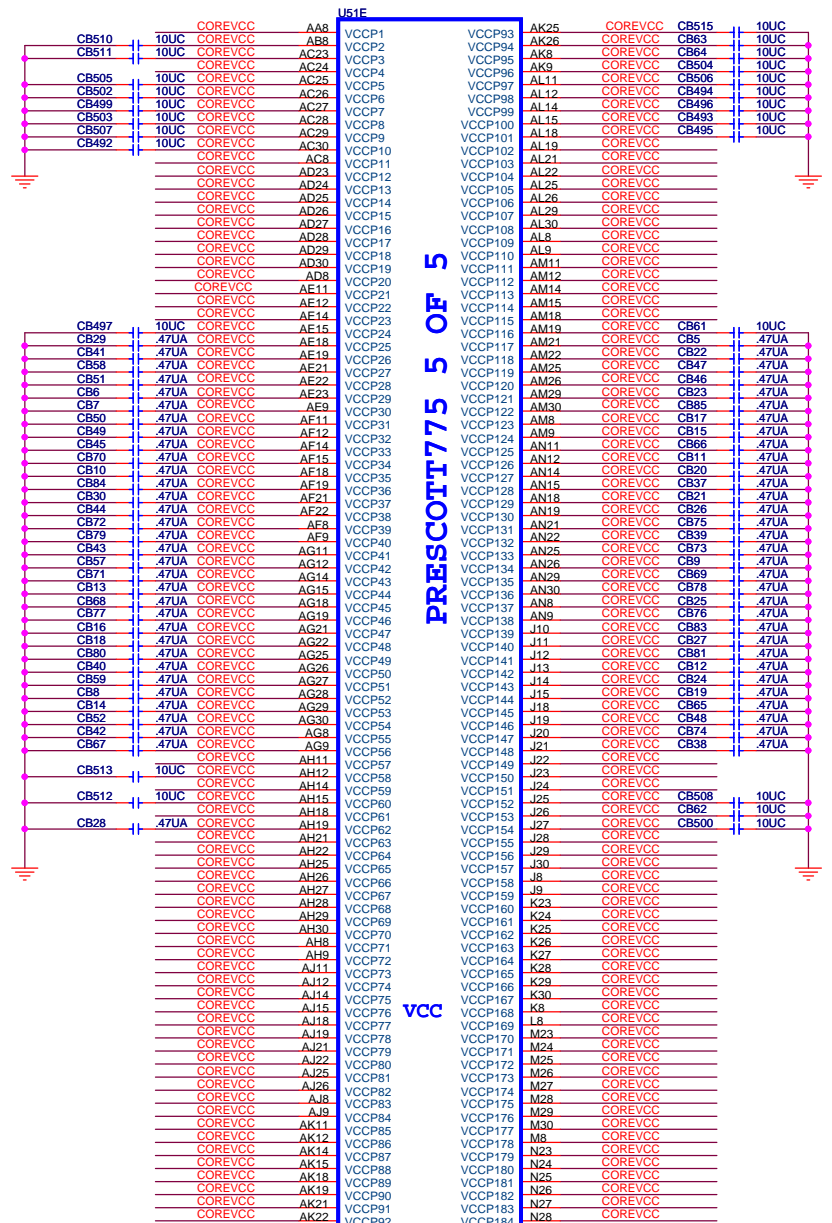
PCMCIA --- AD16, -REQ0, -INTA -INTF, -INTG  
 LAN --- AD18, -REQ2, -INTE  
 MINI PCI --- AD19, -REQ3, -INTB, -INTC



- PLACEMENT NOTICE :**
1. CPUOPLLVC, CPUVCCA AND CPUVSSA RELATIVE R/C MUST NEAR CPU PIN
  2. CPUGTLREF RELATIVE R/C MUST NEAR CPU PIN
  3. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
  4. CPUCOMPO AND CPUCOMP1 PULLDN MUST NEAR CPU PIN
  5. ALL TESTHX PULLUP MUST NEAR CPU PIN
  6. AT LEAST 4 BULK CAPACITORS ON BOTH SIDE OF CPU POWER PLANE
  7. AT LEAST 32PCS 22U CAP AND 42 .47U CAP AROUND CPU



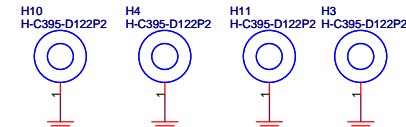
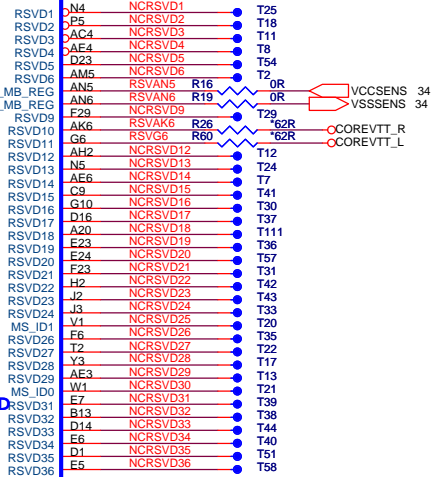
If only TEJAS and CEDAR MILL are supported the FSSEL resistor can be removed.



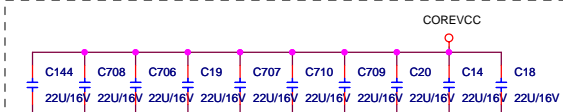
PRESCOTT775 4 OF 5

PRESCOTT775 3 OF 5

PRESCOTT775 5 OF 5



2,32,34,35 COREVCC ← COREVCC



Inside processor socket cavity

**PROJECT : NT2**  
**Quanta Computer Inc.**

Size: Custom    Document number: **PRESCOTT(Power/GND)**    Rev: 1A

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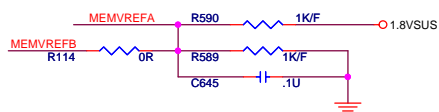


U49C		GRANTS DALE		3 OF 8		DDR CHANNEL A	
DDRM DA0	AE3	SDQS_A0	AG1	DDRDQSA0			
DDRM DA1	AE3	SDQS_A0#	AG2	-DDRDQSA0			
DDRM DA2	AH3	SDQS_A1	AL3	DDRDQSA1			
DDRM DA3	AJ2	SDQS_A1#	AL2	-DDRDQSA1			
DDRM DA4	AE2	SDQS_A2	AP7	DDRDQSA2			
DDRM DA5	AE1	SDQS_A2#	AR7	-DDRDQSA2			
DDRM DA6	AG3	SDQS_A3	AF17	DDRDQSA3			
DDRM DA7	AH2	SDQS_A3#	AG17	-DDRDQSA3			
DDRM DA8	AK2	SDQS_A4	AM30	DDRDQSA4			
DDRM DA9	AK3	SDQS_A4#	AL29	-DDRDQSA4			
DDRM DA10	AN4	SDQS_A5	AG35	DDRDQSA5			
DDRM DA11	AN4	SDQS_A5#	AG33	-DDRDQSA5			
DDRM DA12	AJ1	SDQS_A6	AA34	DDRDQSA6			
DDRM DA13	AJ3	SDQS_A6#	AA35	-DDRDQSA6			
DDRM DA14	AP2	SDQS_A7	U34	DDRDQSA7			
DDRM DA15	AP3	SDQS_A7#	U35	-DDRDQSA7			
DDRM DA16	AR5	SDM_A0	AF2	DDRS DMA0			
DDRM DA17	AP6	SDM_A1	AL1	DDRS DMA1			
DDRM DA18	AP9	SDM_A2	AN7	DDRS DMA2			
DDRM DA19	AN9	SDM_A3	AH16	DDRS DMA3			
DDRM DA20	AN5	SDM_A4	AK29	DDRS DMA4			
DDRM DA21	AN5	SDM_A5	AC34	DDRS DMA5			
DDRM DA22	ANR	SDM_A6	AA33	DDRS DMA6			
DDRM DA23	ARR	SDM_A7	U33	DDRS DMA7			
DDRM DA24	AL17	SMA_A0	AP26	DDRMAA0			
DDRM DA25	AJ17	SMA_A1	AR24	DDRMAA1			
DDRM DA26	AE19	SMA_A2	AL24	DDRMAA2			
DDRM DA27	AH16	SMA_A3	AP23	DDRMAA3			
DDRM DA28	AH16	SMA_A4	AR23	DDRMAA4			
DDRM DA29	AF16	SMA_A5	AP22	DDRMAA5			
DDRM DA30	AD17	SMA_A6	AN23	DDRMAA6			
DDRM DA31	AE19	SMA_A7	AP21	DDRMAA7			
DDRM DA32	AK27	SMA_A8	AN22	DDRMAA8			
DDRM DA33	AJ28	SMA_A9	AN21	DDRMAA9			
DDRM DA34	AL31	SMA_A10	AM27	DDRMAA10			
DDRM DA35	AK31	SMA_A11	AR20	DDRMAA11			
DDRM DA36	AH27	SMA_A12	AP31	DDRMAA12			
DDRM DA37	AL27	SMA_A13	AP31	DDRMAA13			
DDRM DA38	AN30	SWE_A#	AN28	-DDRWEA			
DDRM DA39	AL30	SCAS_A#	AN29	-DDRCASA			
DDRM DA40	AH33	SRAS_A#	AP27	-DDRRASA			
DDRM DA41	AH35	SBS_A0	AR27	DDRBAA0			
DDRM DA42	AE33	SBS_A1	AN27	DDRBAA1			
DDRM DA43	AE33	SBS_A2	AN20	DDRBAA2			
DDRM DA44	AJ33	SCS_A0#	AR29	-DDRCSA0			
DDRM DA45	AG32	SCS_A1#	AP32	-DDRCSA1			
DDRM DA46	AG32	SCS_A2#	AR28	-DDRCSA2 NC			
DDRM DA47	AE34	SCS_A3#	AN31	-DDRCSA3 NC			
DDRM DA48	AD31	SCKE_A0	AP19	DDRCKEA0			
DDRM DA49	AD35	SCKE_A1	AM18	DDRCKEA1			
DDRM DA50	Y33	SCKE_A2	AN18	DDRCKEA2 NC			
DDRM DA51	W34	SCKE_A3	AR19	DDRCKEA3 NC			
DDRM DA52	AE35	SCLK_A0	AN26	+DIMMCLKA0			
DDRM DA53	AE34	SCLK_A0#	AP25	-DIMMCLKA0			
DDRM DA54	AA32	SCLK_A1	AM2	+DIMMCLKA1			
DDRM DA55	Y35	SCLK_A1#	AM3	-DIMMCLKA1			
DDRM DA56	V34	SCLK_A2	AC34	+DIMMCLKA2			
DDRM DA57	V33	SCLK_A2#	AC35	-DIMMCLKA2			
DDRM DA58	R32	SCLK_A3	AN25	+DIMMCLKA3 NC			
DDRM DA59	R34	SCLK_A3#	AM24	-DIMMCLKA3 NC			
DDRM DA60	W35	SCLK_A4	AN3	+DIMMCLKA4 NC			
DDRM DA61	W33	SCLK_A4#	AN2	-DIMMCLKA4 NC			
DDRM DA62	T33	SCLK_A5	AC33	+DIMMCLKA5 NC			
DDRM DA63	T35	SCLK_A5#	AB34	-DIMMCLKA5 NC			
REVD DRMAA13	AB33	RSV_4	RSV_4				
DDRSODTA0	AP30	SODT_A0	SODT_A0				
DDRSODTA1	AN32	SODT_A1	SODT_A1				
DDRSODTA2	AP29	SODT_A2	SODT_A2				
DDRSODTA3	AP33	SODT_A3	SODT_A3				
MCHRSV_TP1	AH15	RSV_TP1	RSV_TP1				
MCHRSV_TP0	AE16	RSV_TP0	RSV_TP0				
MCH_SLWIN0	AJ12	SM_SLEWIN0	SM_SLEWIN0				
	AK12	SM_SLEWOUT0	SM_SLEWOUT0				
MEMVREFA	AE7	SVREF0	SVREF0				

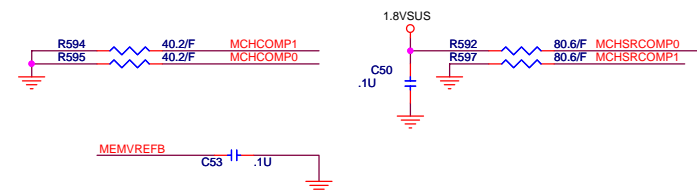
GRANTS DALE-DDR2


U49D		GRANTS DALE		4 OF 8		DDR CHANNEL B	
DDRM DB0	AH4	SDQS_B0	AK5	DDRDQSB0			
DDRM DB1	AJ6	SDQS_B0#	AL4	-DDRDQSB0			
DDRM DB2	AL6	SDQS_B1	AK10	DDRDQSB1			
DDRM DB3	AN6	SDQS_B1#	AH10	-DDRDQSB1			
DDRM DB4	AG9	SDQS_B2	AK13	DDRDQSB2			
DDRM DB5	AL5	SDQS_B2#	AL14	-DDRDQSB2			
DDRM DB6	AL5	SDQS_B3	AD20	DDRDQSB3			
DDRM DB7	AM5	SDQS_B3#	AE20	-DDRDQSB3			
DDRM DB8	AJ8	SDQS_B4	AH25	DDRDQSB4			
DDRM DB9	AL8	SDQS_B4#	AG26	-DDRDQSB4			
DDRM DB10	AE11	SDQS_B5	AH28	DDRDQSB5			
DDRM DB11	AJ7	SDQS_B5#	AB31	-DDRDQSB5			
DDRM DB12	AL7	SDQS_B6	AD24	DDRDQSB6			
DDRM DB13	AG10	SDQS_B6#	W27	DDRDQSB7			
DDRM DB14	AG11	SDQS_B7	Y28	-DDRDQSB7			
DDRM DB15	AE18	SDM_B0	AM5	DDRS DMB0			
DDRM DB16	AH12	SDM_B1	AJ9	DDRS DMB1			
DDRM DB17	AD14	SDM_B2	AH13	DDRS DMB2			
DDRM DB18	AD15	SDM_B3	AG20	DDRS DMB3			
DDRM DB19	AD12	SDM_B4	AG24	DDRS DMB4			
DDRM DB20	AD12	SDM_B5	AH31	DDRS DMB5			
DDRM DB21	AE13	SDM_B6	AD24	DDRS DMB6			
DDRM DB22	AG17	SDM_B7	W31	DDRS DMB7			
DDRM DB23	AF14	SMA_B0	AM15	DDRMAB0			
DDRM DB24	AK19	SMA_B1	AR15	DDRMAB1			
DDRM DB25	AH19	SMA_B2	AL15	DDRMAB2			
DDRM DB26	AH21	SMA_B3	AL15	DDRMAB3			
DDRM DB27	AD21	SMA_B4	AP14	DDRMAB4			
DDRM DB28	AD18	SMA_B5	AM12	DDRMAB5			
DDRM DB29	AL18	SMA_B6	AP13	DDRMAB6			
DDRM DB30	AE22	SMA_B7	AL12	DDRMAB7			
DDRM DB31	AF22	SMA_B8	AN13	DDRMAB8			
DDRM DB32	AE24	SMA_B9	AR12	DDRMAB9			
DDRM DB33	AE26	SMA_B10	AG20	DDRMAB10			
DDRM DB34	AL26	SMA_B11	AP15	DDRMAB11			
DDRM DB35	AJ26	SMA_B12	AR11	DDRMAB12			
DDRM DB36	AJ26	SMA_B13	AL33	DDRMAB13			
DDRM DB37	AD23	SWE_B#	AP17	-DDRWEB			
DDRM DB38	AJ25	SCAS_B#	AP18	-DDRCASB			
DDRM DB39	AJ25	SRAS_B#	AK24	-DDRRASB			
DDRM DB40	AK32	SBS_B0	AN17	-DDRRASB			
DDRM DB41	AJ31	SBS_B1	AR16	DDRBAB0			
DDRM DB42	AG31	SBS_B2	AN16	DDRBAB1			
DDRM DB43	AE28	SCS_B0#	AN11	DDRBAB2			
DDRM DB44	AJ26	SCS_B1#	AR30	-DDRCASB			
DDRM DB45	AK33	SCS_B2#	AN17	-DDRWEB			
DDRM DB46	AG30	SCS_B3#	AN17	-DDRWEB			
DDRM DB47	AG27	SCKE_B0	AR16	DDRCKEB0			
DDRM DB48	AE27	SCKE_B1	AN16	DDRCKEB1			
DDRM DB49	AE27	SCKE_B2	AN10	DDRCKEB2 NC			
DDRM DB50	AE26	SCKE_B3	AM9	DDRCKEB3 NC			
DDRM DB51	AE26	SCLK_B0	AH22	+DIMMCLKB0			
DDRM DB52	AE31	SCLK_B0#	AG23	-DIMMCLKB0			
DDRM DB53	AE29	SCLK_B1	AK9	+DIMMCLKB1			
DDRM DB54	AC28	SCLK_B1#	AL9	-DIMMCLKB1			
DDRM DB55	AE27	SCLK_B2	AE26	+DIMMCLKB2			
DDRM DB56	AJ28	SCLK_B2#	AE25	-DIMMCLKB2			
DDRM DB57	V29	SCLK_B3	AL23	+DIMMCLKB3 NC			
DDRM DB58	W28	SCLK_B3#	AK22	-DIMMCLKB3 NC			
DDRM DB59	V29	SCLK_B4	AJ11	+DIMMCLKB4 NC			
DDRM DB60	V26	SCLK_B4#	AL11	-DIMMCLKB4 NC			
DDRM DB61	AJ29	SCLK_B5	AD28	+DIMMCLKB5 NC			
DDRM DB62	U26	SCLK_B5#	AD29	-DIMMCLKB5 NC			
DDRM DB63	U26						
DDRSODTB0	AM33	SODT_B0	SODT_B0				
DDRSODTB1	AL34	SODT_B1	SODT_B1				
DDRSODTB2	AL35	SODT_B2	SODT_B2				
DDRSODTB3	AK34	SODT_B3	SODT_B3				
REVD DRMB13	AD32	RSV_16	RSV_16				
MCHRSV_TP3	AK15	RSV_TP3	RSV_TP3				
MCHRSV_TP2	AN14	RSV_TP2	RSV_TP2				
MCH_SLWIN1	AF9	SM_SLEWIN1	SM_SLEWIN1				
	AF10	SM_SLEWOUT1	SM_SLEWOUT1				
MEMVREFB	AE8	SVREF1	SVREF1				
MCHSRCOMP1	AG8	SRCOMP1	SRCOMP1				
MCHSRCOMP0	AG4	SRCOMP0	SRCOMP0				
MCHCOMP1	AE5	SOCOMP1	SOCOMP1				
MCHCOMP0	AE5	SOCOMP0	SOCOMP0				

GRANTS DALE-DDR2



1. MEMVREFA AND MEMVREFB RELATIVE R/C MUST NEAT GMCH PIN





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Quanta Computer Inc.

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**GMCH DDR2 CHANNEL A**

1.5V OC 1.5VEXPRESS 1.5VEXPRESS

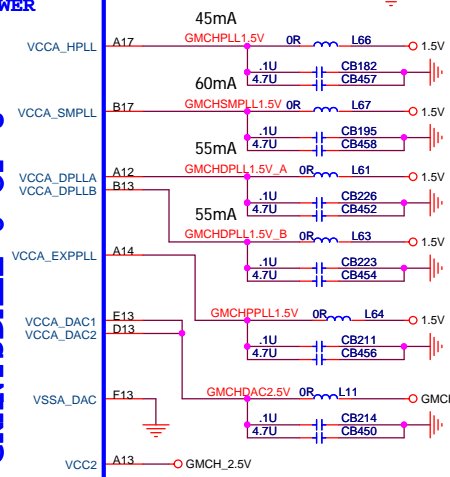
CB197	.1U	1.8VSUS	AK35	VCCSM_1
CB171	.1U	1.8VSUS	AM10	VCCSM_2
CB104	.1U	1.8VSUS	AM11	VCCSM_3
CB117	.1U	1.8VSUS	AM13	VCCSM_4
CB93	.1U	1.8VSUS	AM14	VCCSM_5
CB137	.1U	1.8VSUS	AM16	VCCSM_6
CB92	.1U	1.8VSUS	AM17	VCCSM_7
CB105	.1U	1.8VSUS	AM19	VCCSM_8
CB174	.1U	1.8VSUS	AM20	VCCSM_9
CB111	.1U	1.8VSUS	AM22	VCCSM_10
CB210	.1U	1.8VSUS	AM23	VCCSM_11
CB238	.1U	1.8VSUS	AM25	VCCSM_12
CB462	4.7U	1.8VSUS	AM26	VCCSM_13
CB453	4.7U	1.8VSUS	AM28	VCCSM_14
CB215	.1U	1.8VSUS	AM32	VCCSM_15
CB229	.1U	1.8VSUS	AM35	VCCSM_16
CB88	.1U	1.8VSUS	AP12	VCCSM_17
CB219	.1U	1.8VSUS	AP16	VCCSM_18
CB207	.1U	1.8VSUS	AP20	VCCSM_19
CB130	.1U	1.8VSUS	AP24	VCCSM_20
CB100	.1U	1.8VSUS	AP28	VCCSM_21
CB208	.1U	1.8VSUS	AR10	VCCSM_22
CB89	.1U	1.8VSUS	AR14	VCCSM_23
CB897	.1U	1.8VSUS	AR18	VCCSM_24
CB173	.1U	1.8VSUS	AR22	VCCSM_25
CB90	.1U	1.8VSUS	AR26	VCCSM_26
CB98	.1U	1.8VSUS	AR31	VCCSM_27
CB455	4.7U	1.8VSUS	AR33	VCCSM_28

**POWER**

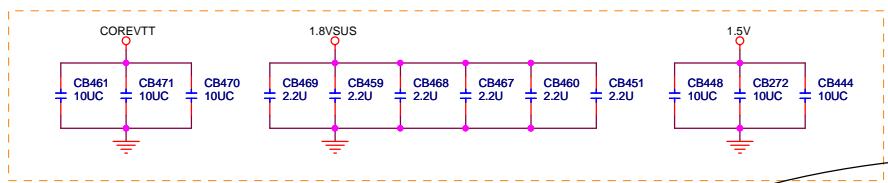
**GRANTSDALE 6 OF 8**

**1.4A**

W1	1.5VEXPRESS	.1U	CB244
W2	1.5VEXPRESS	.1U	CB252
W3	1.5VEXPRESS	.1U	CB263
W4	1.5VEXPRESS	.1U	CB258
W6	1.5VEXPRESS	.1U	CB267
W7	1.5VEXPRESS	.1U	CB273
W8	1.5VEXPRESS	.1U	CB248
W9	1.5VEXPRESS	.1U	CB255
Y1	1.5VEXPRESS	4.7U	CB449
Y2	1.5VEXPRESS	.1U	CB235
Y3	1.5VEXPRESS	.1U	CB261
Y4	1.5VEXPRESS	.1U	CB276
Y6	1.5VEXPRESS	.1U	CB270
Y7	1.5VEXPRESS	4.7U	CB447
Y8	1.5VEXPRESS	.1U	CB265
Y9	1.5VEXPRESS	.1U	CB241



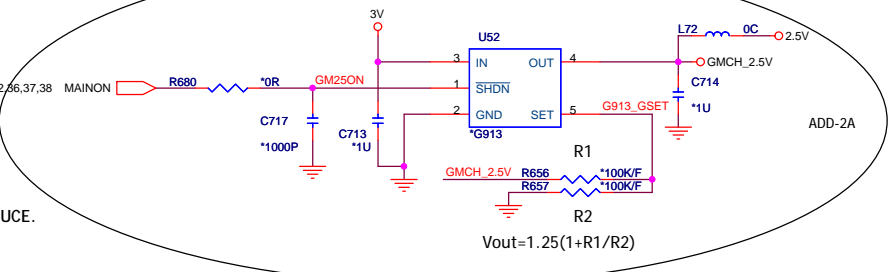
**CURRENT SPEC 1.6A**



3V	2,4,9,10,11,12,13,14,15,16,19,20,21,22,23,25,26,27,28,29,30,32,33,34,36,37,38
2.5V	14,15,17,18,26,32,38
1.8VSUS	COREVCC 2,3,32,34,35
1.8VSUS	6,9,26,32,36,37
COREVTT	2,4,5,11,12,32,37

**PLACEMENT NOTICE :**

1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. GMCHFSB1.5V RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHDACLL1.5V RELATIVE R/C MUST NEAR GMCH PIN



.1U	CB184	1.5V	AA13	VCC_1
.1U	CB121	1.5V	AA14	VCC_2
.1U	CB154	1.5V	AA16	VCC_3
.1U	CB220	1.5V	AA18	VCC_4
.1U	CB120	1.5V	AA20	VCC_5
.1U	CB128	1.5V	AA22	VCC_6
.01U/X7R	CB141	1.5V	AA23	VCC_7
.01U/X7R	CB250	1.5V	AA24	VCC_8
.01U/X7R	CB149	1.5V	AB1	VCC_9
.01U/X7R	CB230	1.5V	AB2	VCC_10
.01U/X7R	CB198	1.5V	AB3	VCC_11
.01U/X7R	CB222	1.5V	AB4	VCC_12
.01U/X7R	CB216	1.5V	AB5	VCC_13
.01U/X7R	CB180	1.5V	AB6	VCC_14
.01U/X7R	CB206	1.5V	AB7	VCC_15
.01U/X7R	CB153	1.5V	AB9	VCC_16
.01U/X7R	CB202	1.5V	AB8	VCC_17
1000P	CB278	1.5V	AB10	VCC_18
1000P	CB271	1.5V	AB11	VCC_19
4.7U	CB446	1.5V	AB13	VCC_21
4.7U	CB274	1.5V	AB14	VCC_22
		1.5V	AB15	VCC_23
		1.5V	AB16	VCC_24
		1.5V	AB17	VCC_25
		1.5V	AB18	VCC_26
		1.5V	AB19	VCC_27
		1.5V	AB20	VCC_28
		1.5V	AB21	VCC_29
		1.5V	AB22	VCC_30
		1.5V	AB23	VCC_31
		1.5V	AB24	VCC_32
		1.5V	AC1	VCC_33
		1.5V	AC2	VCC_34
		1.5V	AC3	VCC_35
		1.5V	AC4	VCC_36
		1.5V	AC5	VCC_37
		1.5V	AC6	VCC_38
		1.5V	AC7	VCC_39
		1.5V	AC8	VCC_40
		1.5V	AC9	VCC_41
		1.5V	AC10	VCC_42
		1.5V	AC11	VCC_43
		1.5V	AD1	VCC_44
		1.5V	AD2	VCC_45
		1.5V	AD3	VCC_46
		1.5V	AD4	VCC_47
		1.5V	AD5	VCC_48
.1U	CB165	1.5V	AD6	VCC_49
.1U	CB185	1.5V	AD7	VCC_50
.1U	CB189	1.5V	AD8	VCC_51
.1U	CB122	1.5V	AD9	VCC_52
.1U	CB176	1.5V	AD10	VCC_53
.1U	CB232	1.5V	L10	VCC_54
.1U	CB234	1.5V	N13	VCC_55
.01U/X7R	CB140	1.5V	N14	VCC_56
.01U/X7R	CB249	1.5V	N15	VCC_57
.01U/X7R	CB237	1.5V	N16	VCC_58
.01U/X7R	CB231	1.5V	N18	VCC_59
.01U/X7R	CB260	1.5V	N20	VCC_60
.01U/X7R	CB196	1.5V	N21	VCC_61
.01U/X7R	CB262	1.5V	P13	VCC_62
.01U/X7R	CB254	1.5V	P14	VCC_63
.01U/X7R	CB243	1.5V	P15	VCC_64
.01U/X7R	CB118	1.5V	P17	VCC_65
.01U/X7R	CB175	1.5V	P19	VCC_66
.01U/X7R	CB172	1.5V	P21	VCC_67
.01U/X7R	CB124	1.5V	P22	VCC_68
.01U/X7R	CB123	1.5V	R13	VCC_69
.01U/X7R	CB246	1.5V	R14	VCC_70
.01U/X7R	CB247	1.5V	R15	VCC_71
.01U/X7R	CB236	1.5V	R16	VCC_72
.01U/X7R	CB279	1.5V	R18	VCC_73
		1.5V	R20	VCC_74
		1.5V	R22	VCC_75
		1.5V	R23	VCC_76
		1.5V	T13	VCC_77
		1.5V	T14	VCC_78
		1.5V	T15	VCC_79
		1.5V	T16	VCC_80
		1.5V	T17	VCC_81

**POWER**

**GRANTSDALE 5 OF 8**

VCC_82	T19	1.5V	CB213	.1U
VCC_83	T20	1.5V	CB150	.1U
VCC_84	T21	1.5V	CB198	.1U
VCC_85	T23	1.5V	CB201	.1U
VCC_86	T14	1.5V	CB145	.1U
VCC_87	U14	1.5V	CB170	.1U
VCC_88	U16	1.5V	CB257	.01U/X7R
VCC_89	U18	1.5V	CB203	.01U/X7R
VCC_90	U18	1.5V	CB190	.01U/X7R
VCC_91	U22	1.5V	CB143	.01U/X7R
VCC_92	U14	1.5V	CB266	.01U/X7R
VCC_93	U13	1.5V	CB264	.01U/X7R
VCC_94	V14	1.5V	CB268	.01U/X7R
VCC_95	V15	1.5V		
VCC_97	V17	1.5V		
VCC_98	V19	1.5V		
VCC_99	V21	1.5V		
VCC_100	V23	1.5V		
VCC_101	V24	1.5V		
VCC_102	W13	1.5V		
VCC_103	W14	1.5V		
VCC_104	W18	1.5V		
VCC_105	W20	1.5V	CB259	.01U/X7R
VCC_106	W22	1.5V	CB221	.01U/X7R
VCC_107	W24	1.5V	CB253	.01U/X7R
VCC_108	Y13	1.5V	CB178	.01U/X7R
VCC_109	Y14	1.5V	CB256	.01U/X7R
VCC_110	Y15	1.5V	CB217	.01U/X7R
VCC_111	Y16	1.5V	CB242	.01U/X7R
VCC_112	Y17	1.5V	CB269	1000P
VCC_113	Y19	1.5V	CB445	1000P
VCC_114	Y20	1.5V	CB275	1000P
VCC_115	Y21	1.5V		
VCC_116	Y23	1.5V		
VCC_117	Y24	1.5V		

RSV_1	AA30
RSV_2	AB24
RSV_3	AC12
RSV_4	AC10
RSV_5	AC16
RSV_6	AC14
RSV_7	AC19
RSV_8	AC16
RSV_9	AC12
RSV_10	AC18
RSV_11	AC16
RSV_12	AC19
RSV_13	AC16
RSV_14	AC12
RSV_15	AC18
RSV_16	AC16
RSV_17	AC12
RSV_18	AC18
RSV_19	AC16
RSV_20	AC12
RSV_21	AC18
RSV_22	AC16
RSV_23	AC12
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RSV_25	AC16
RSV_26	AC12
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RSV_32	M16
RSV_33	R30

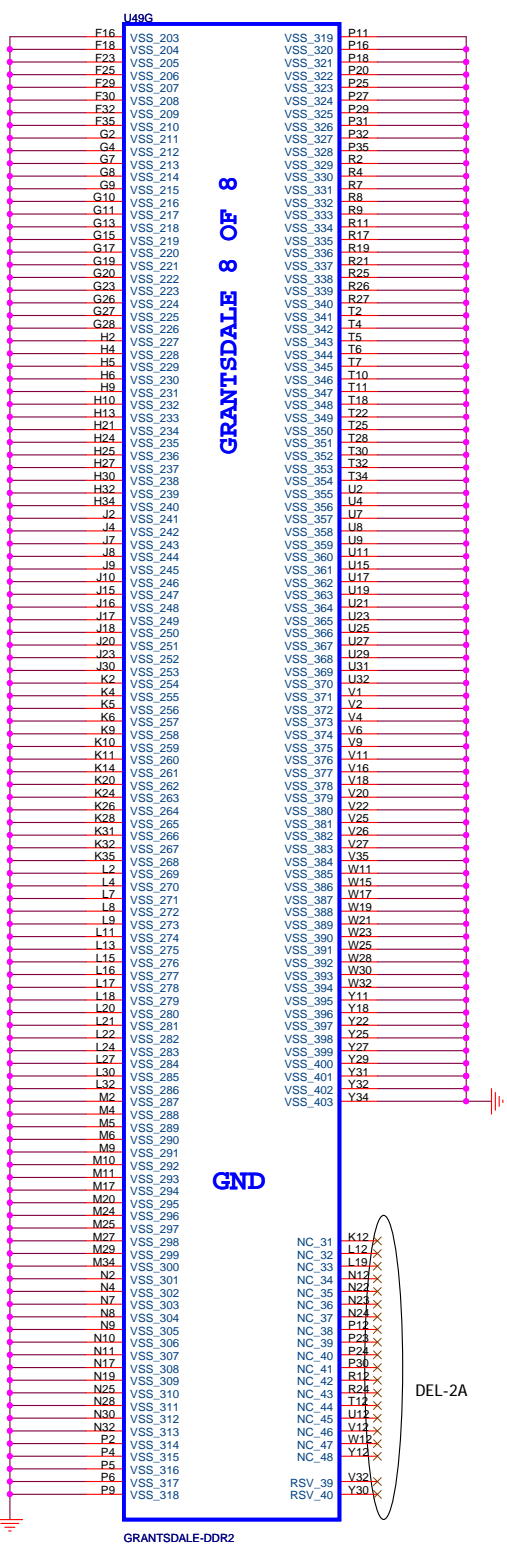
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**PROJECT : NT2**  
**Quanta Computer Inc.**

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Date: Thursday, March 18, 2004 | Sheet: 7 of 38

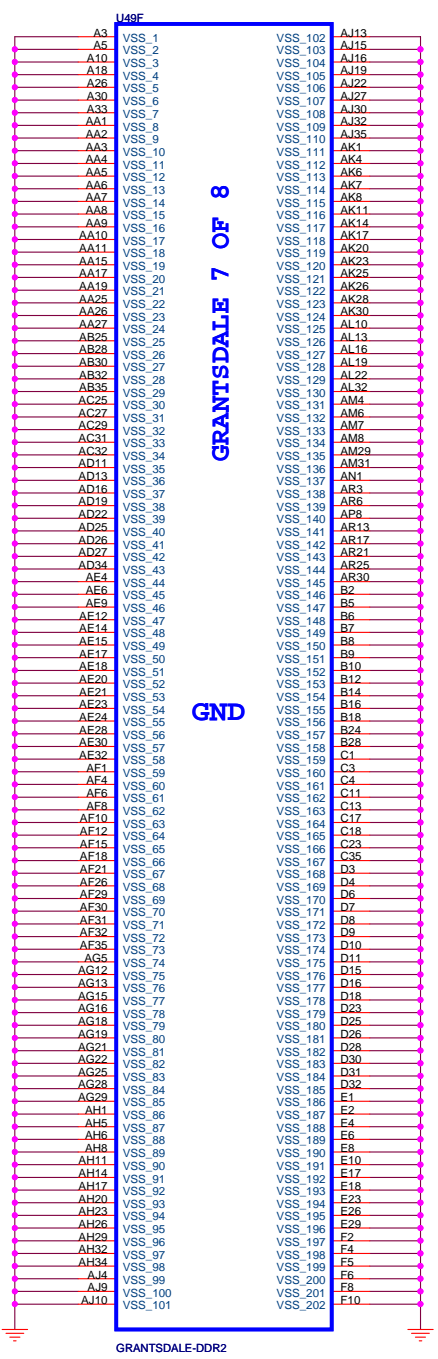




GRANTSDALE 8 OF 8

GND


DEL-2A

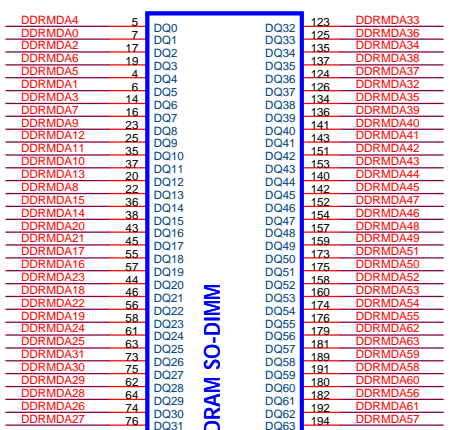


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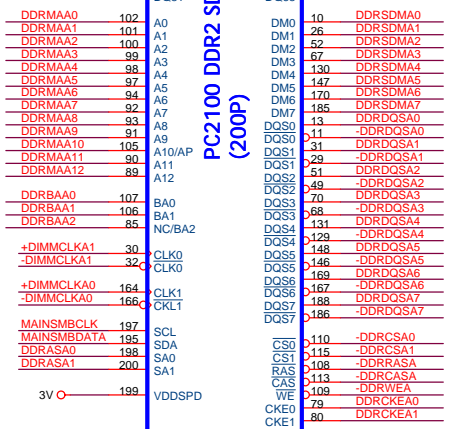
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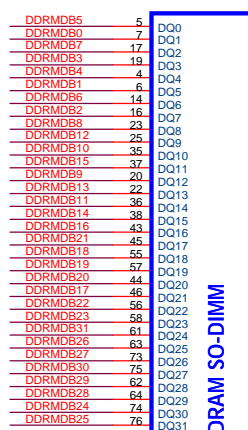
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Date: Thursday, March 16, 2004		Sheet 8 of 38	



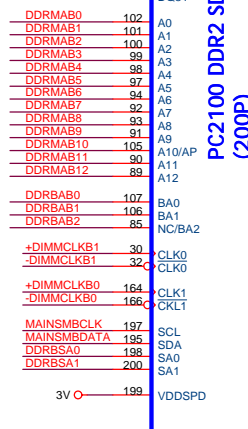
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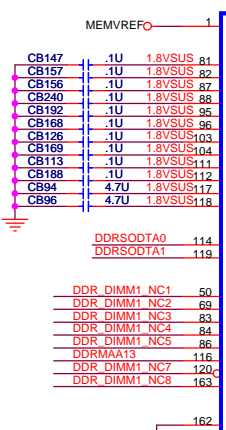
CHANNEL A SINGLE DIMM



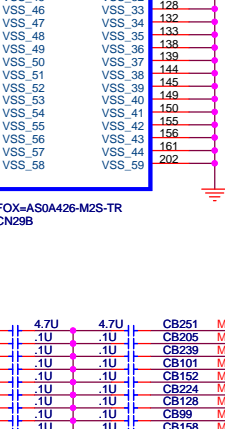
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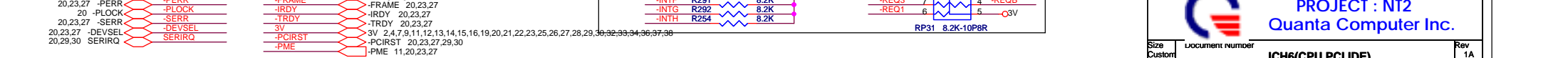
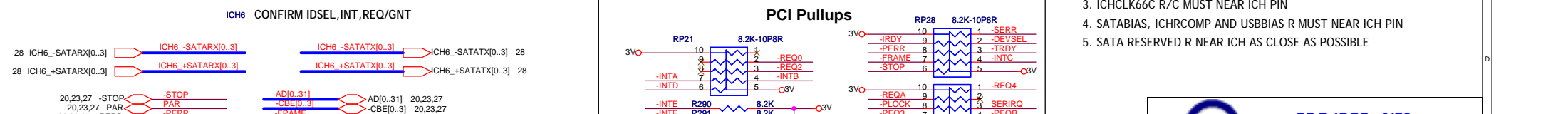
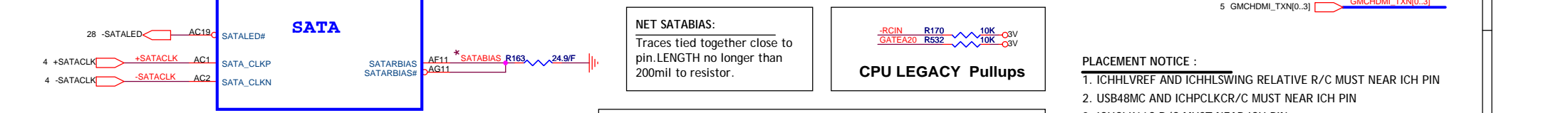
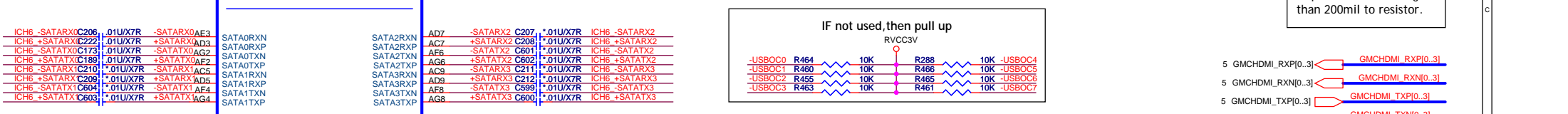
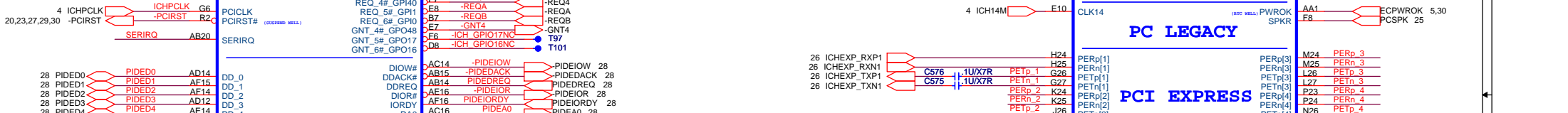
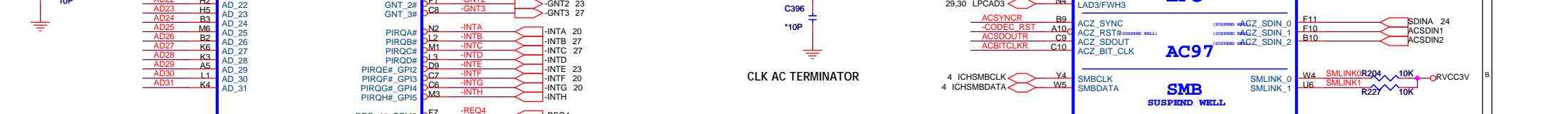
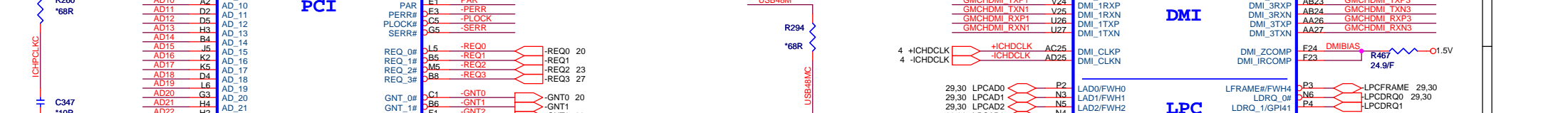
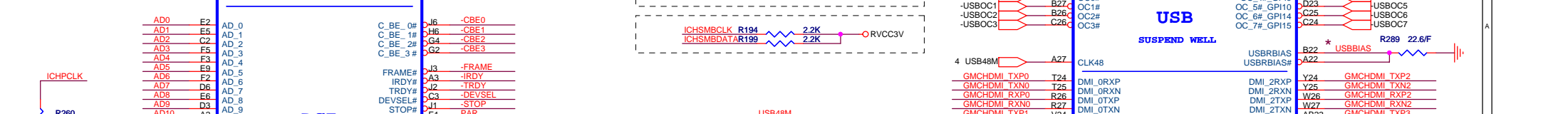
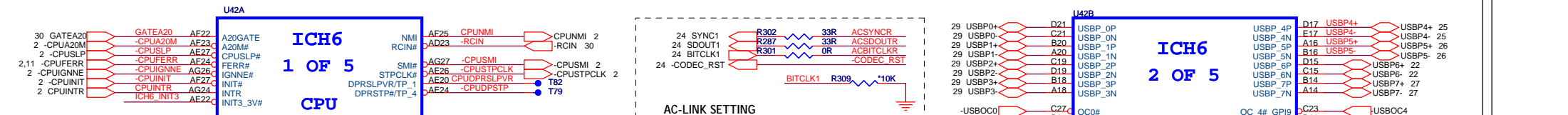


CHANNEL B SINGLE DIMM



PC2100 DDR2 SDRAM SO-DIMM (200P)





**GPIO PIN DEFINE**

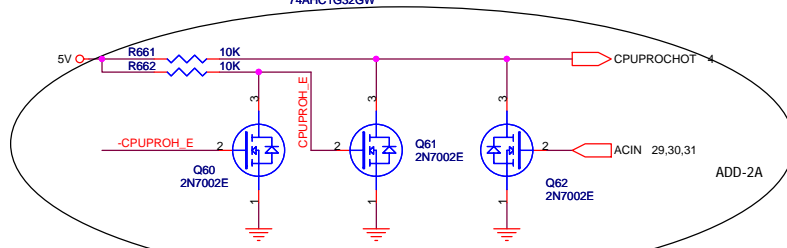
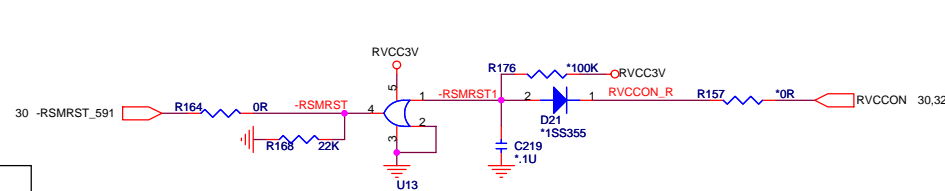
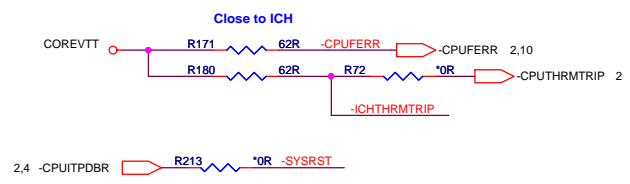
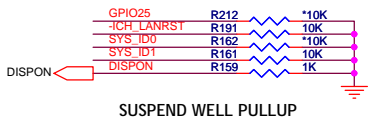
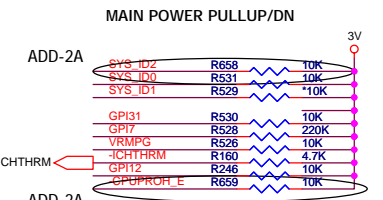
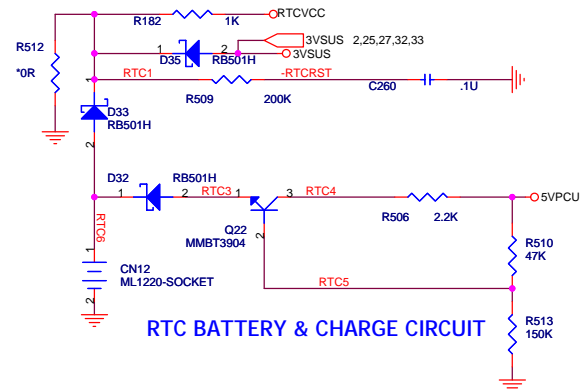
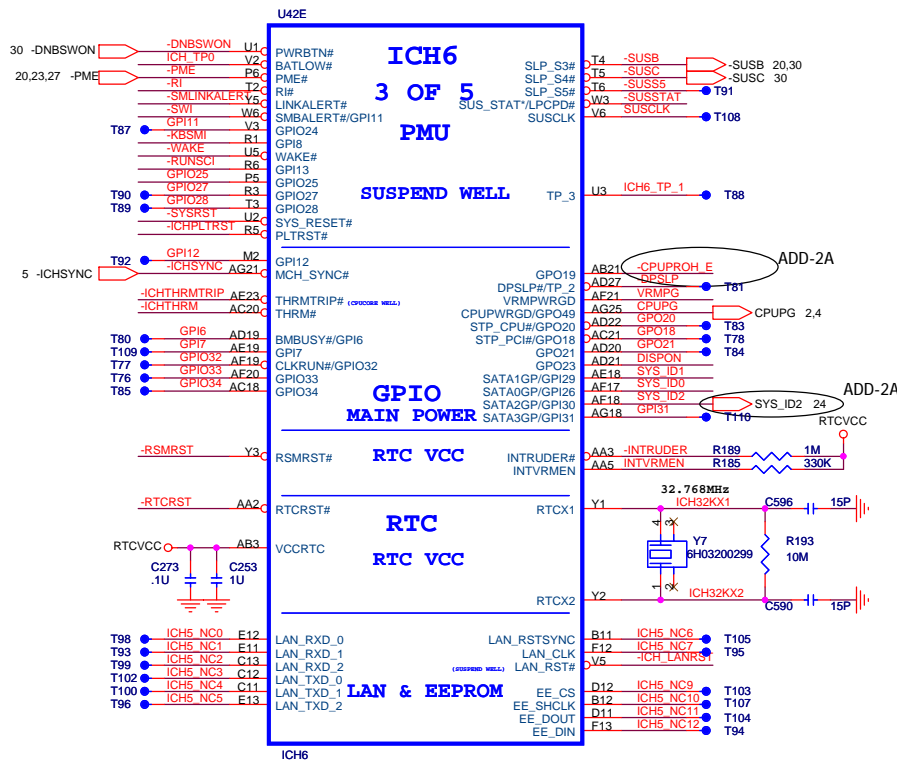
GPI6		PULL UP
GPI7	-KBSMI	PULL UP
GPI11	-SWI	PULL UP
GPI12		PULL UP
GPI13	-RUNSCI	PULL UP
GPI26	SYS_ID0	PULL UP
GPI29	SYS_ID1	PULL LO
GPI30		PULL UP
GPI31		PULL UP
GPO18		SET OUTPUT
GPO19		SET OUTPUT
GPO20		SET OUTPUT
GPO21		SET OUTPUT
GPO22	DISPON	SET OUTPUT
GPO24		SET OUTPUT
GPO49	CPUPG	SET OUTPUT
GPO25		SET OUTPUT
GPO27		SET OUTPUT
GPO28		SET OUTPUT
GPI032		SET OUTPUT
GPI033		SET OUTPUT
GPI034		SET OUTPUT

**Functional Straps**

GNT[6]#/GPO[16]	Top-Block Swap Override Pull-Low : "top-block swap" mode
LINKALERT#	Reserved Requires an external pull-up resistor.
SPKR	No Reboot Pull-up : "No Reboot" mode
INTVRMEN	Integrated VccSus1.5 VRM enable/disable Pull-up : Enable integrated VccSus1.5V VRM
GPI0[25]	Integrated Vcc2.5 VRM enable/disable Pull-Low : Enable integrated Vcc2.5 VRM
EE_CS	Reserved Internal pull-down & should not be pull-high
GNT[5]#/GPO[17]	Boot BIOS Destination Selection This functionality for debug/testing only
EE_DOUT	Reserved Internal pull-up & should not be pull-low
ACZ_SDOUT	XOR chain Entrance / PCI Express port config bit1 Pull-low : allows entrance to XOR Chain testing
ACZ_SYNC	PCI Express Port Config bit 0 This signal has a weak internal pull-down
TP[1]	Internal pull-down & should not be pull-high
STATLED#	Internal pull-up & should not be pull-low
REQ[4:1]	XOR Chain Selection / See Chapter 8
TP[3]	XOR Chain Entrance / See Chapter 8 This signal should not be Pull-low unless using XOR Chain testing

**DESIGN CHECK LIST :**

1. CLASSIFY THE POWER PLANE FOR PMU AND GPIO PIN
2. CLASSIFY GPI AND GPO PIN
3. COMMON PIN FOR PMU INPUT: -PME, BATLOW, -RI, -WAKESCI, RUNSCI, KBSMI AND -DNBSWON
4. USUALLY USED GPIO PIN : DISPON, CRTSENSE, SPKOFF
5. USUALLY USED CLK CONTRL PIN : -CPUSTP, -PCISTP, -SUSA AND -SUSSTAT
6. AGP PMU PIN : -AGPBUSY AND -STPAGP
7. CHECK -PCIRST BUFFERAND PWROK SIGNAL
8. CHECK -RSMRST CIRCUIT



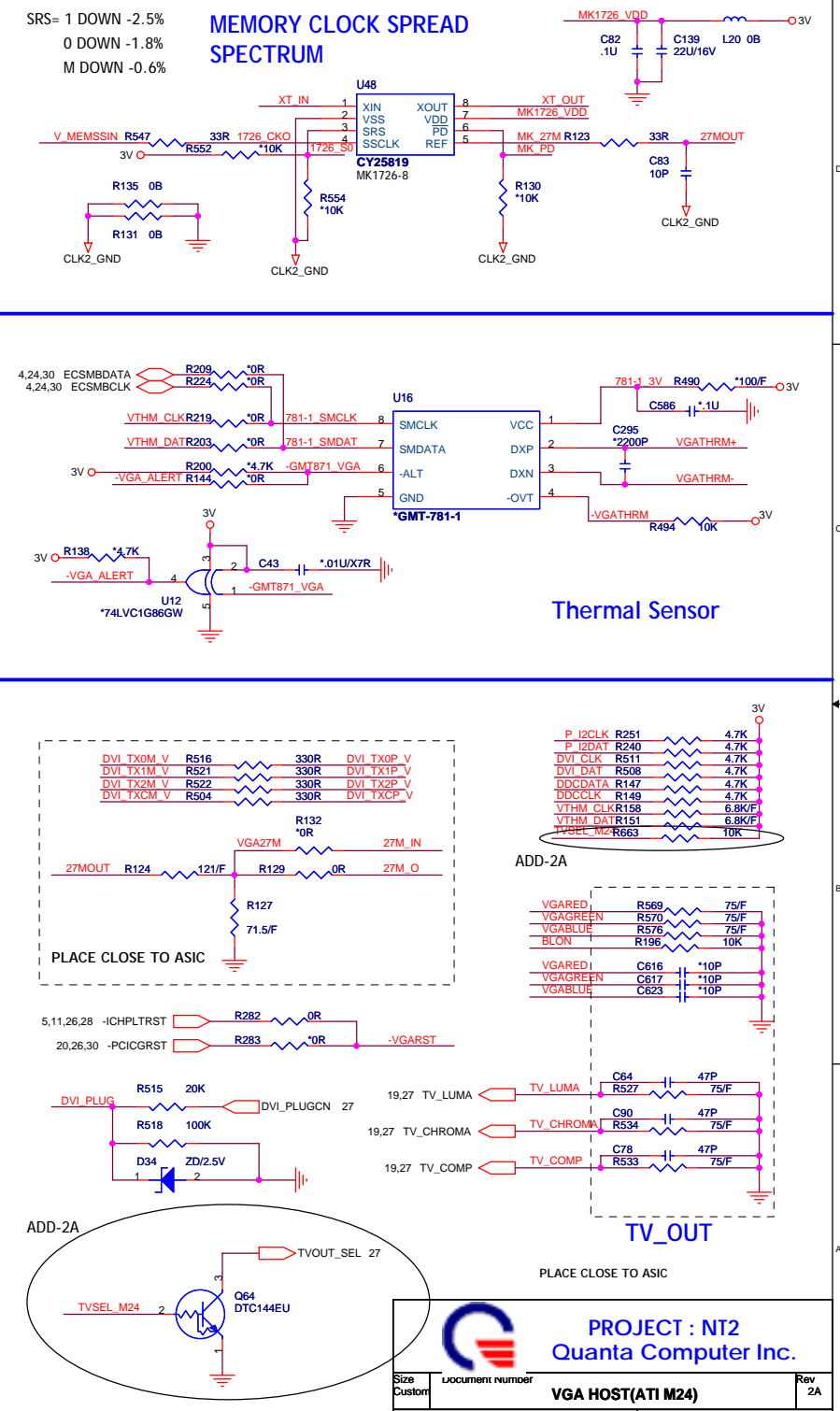
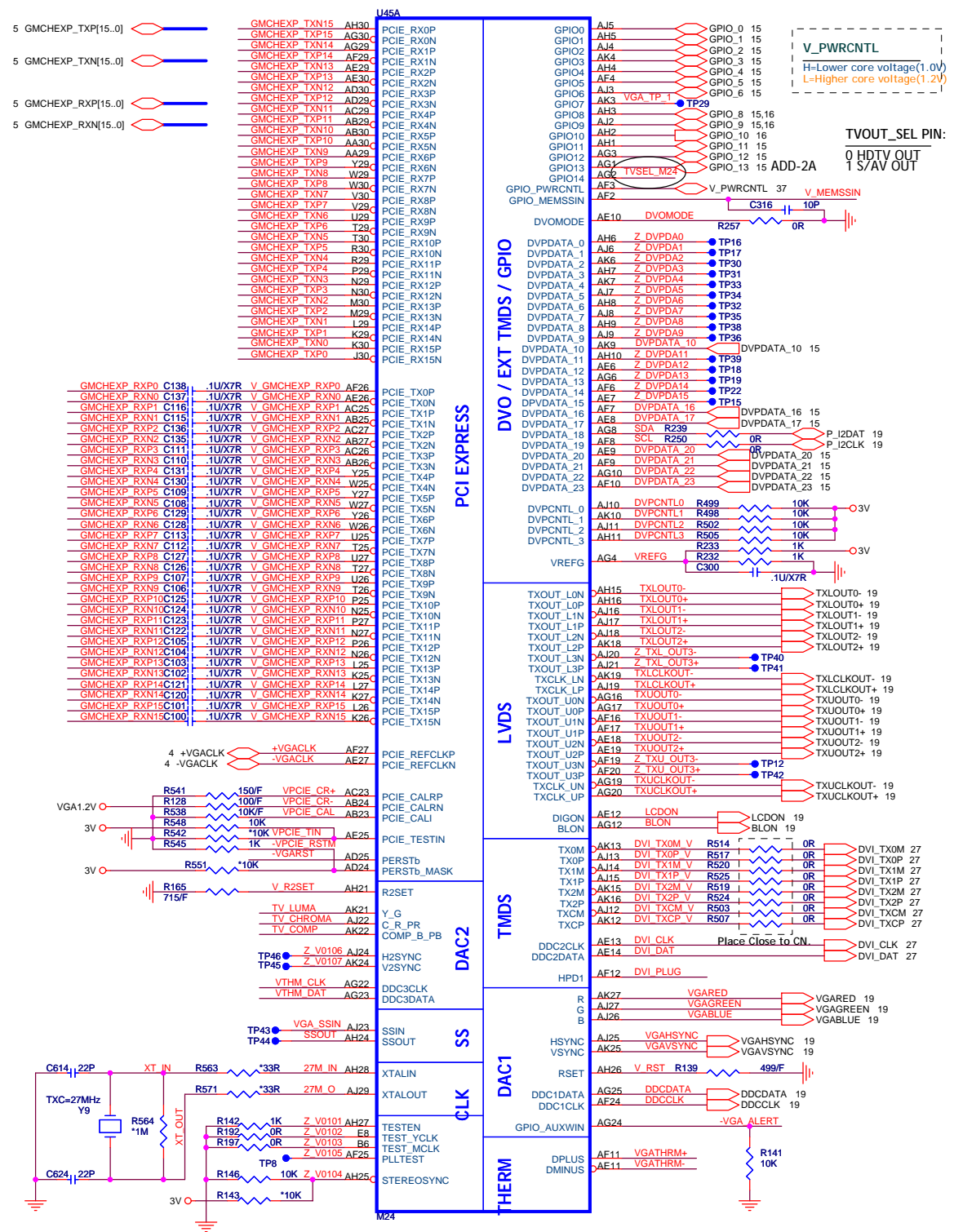
- PLACEMENT NOTICE :**
1. ONE BYPASS CAP FOR EACH ICH PIN IF POSSIBLE
  2. RTC XTAL MUST NEAR ICH
  3. PUT RTC BAT CIRCUIT AS A GROUP
  4. REF5VSUS AND REF5V R/C/D NEAR ICH PIN

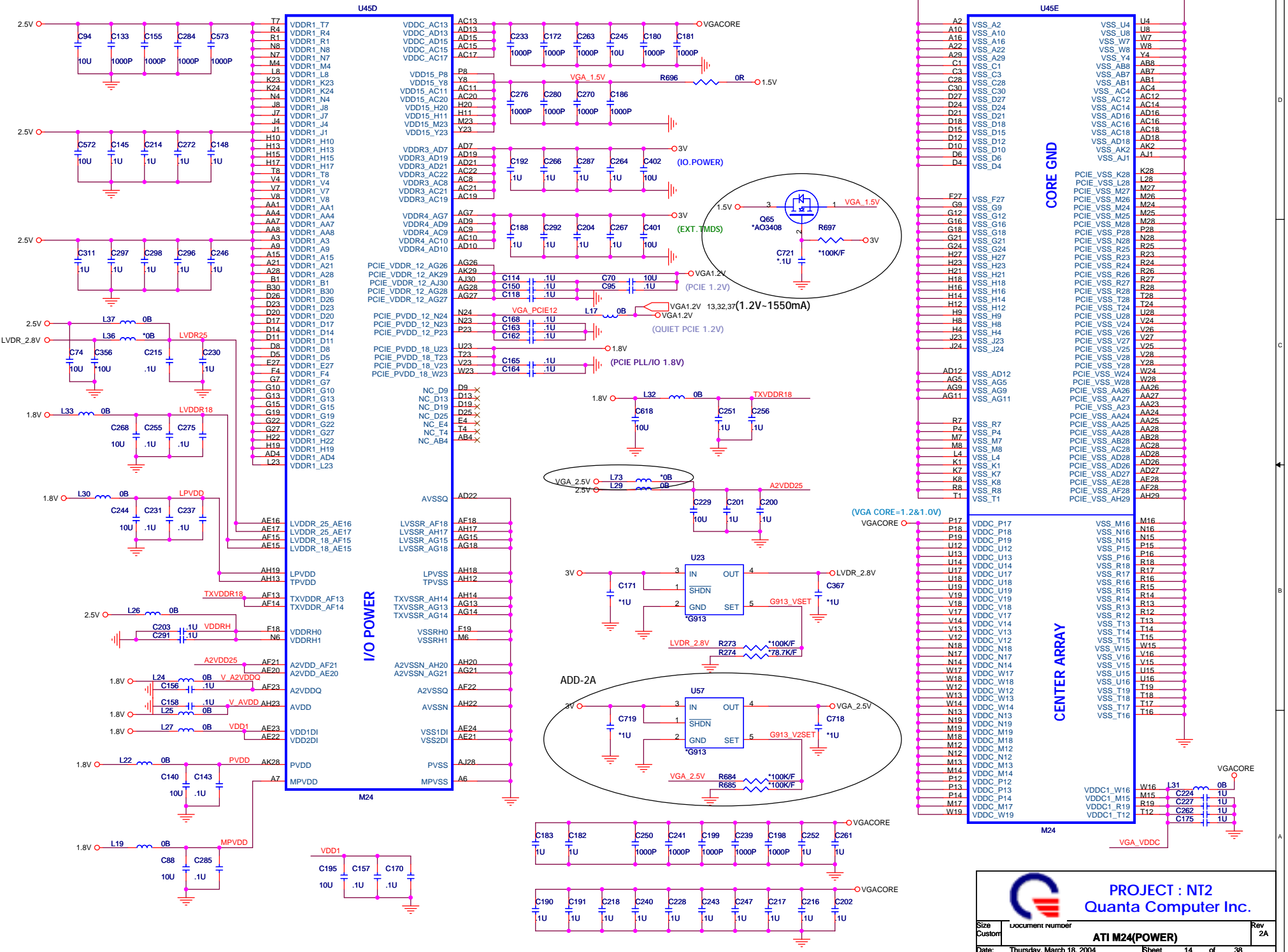
**PROJECT : NT2**  
**Quanta Computer Inc.**

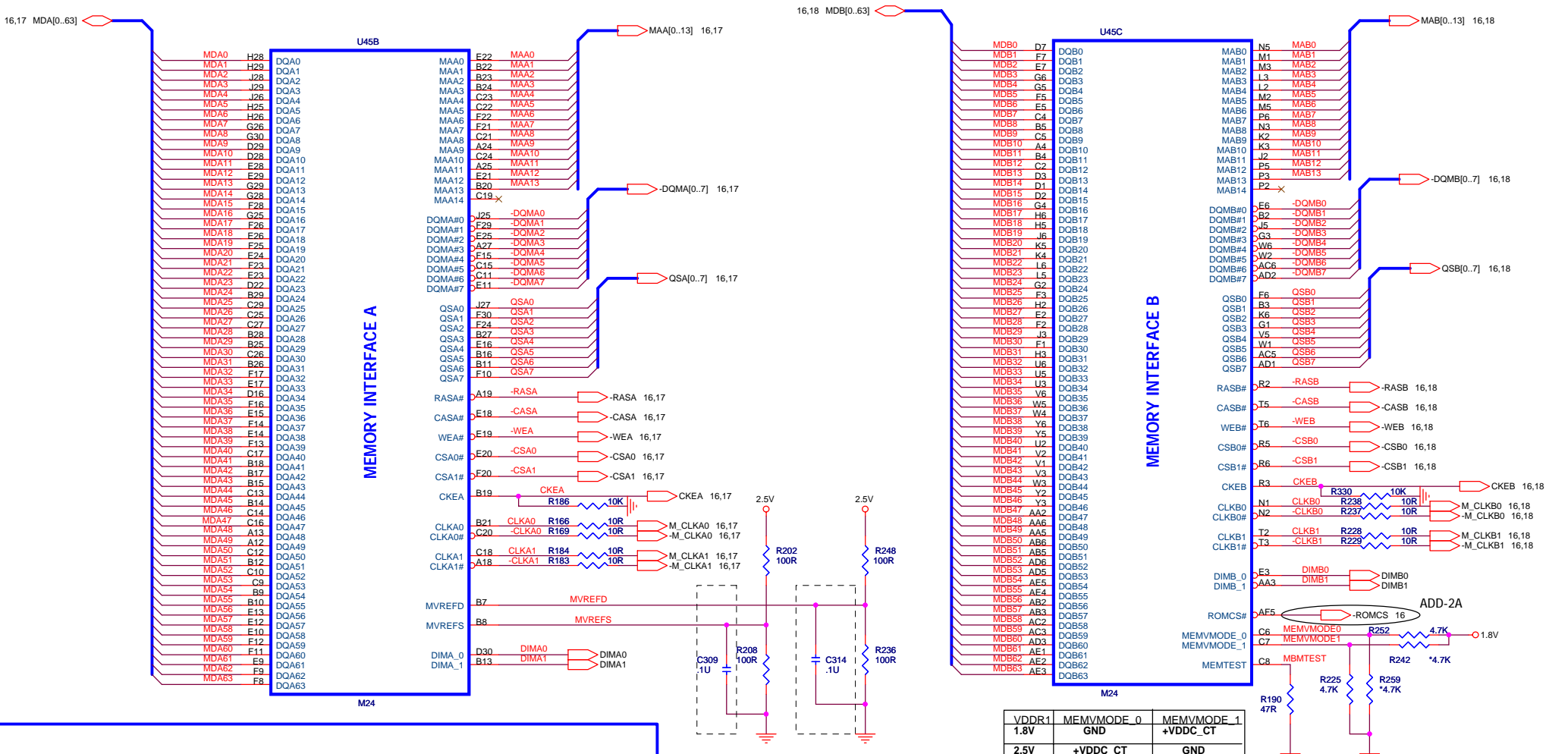
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Date: Thursday, March 18, 2004 | Sheet: 11 of 38









MEMORY INTERFACE A

MEMORY INTERFACE B

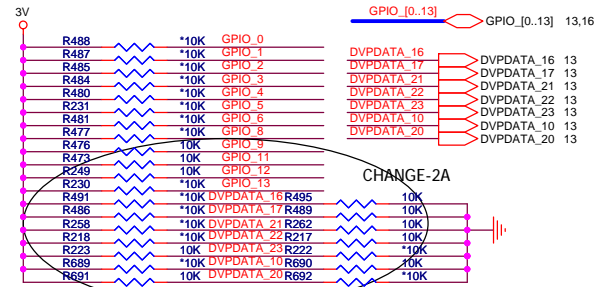
Place close to ASIC

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND

GPIO_0	PCI-Express Current Calibration Bandgap Backup
	0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable
	0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode
	01: RESERVED
	10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration
	0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL
GPIO_6	PCI-Express transmitter current compensation
	0: Normal 1: Inject extra current for output buffer switching

STRAPS PIN

GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible					
GPIO(9,13:11)	ROMIDCFG					
INT P/D	0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM					
DVPDATA_15, 20, 21	Vendor	DATA23	DATA22	DATA21	DATA20	DATA10
	Voltage	CS	MEM SIZE	MEM TYPE		
MEM TYPE	0	0	0	0	0	4MX32
	0	0	0	0	1	8MX32
	0	0	0	0	1	X 128M(M22), 256M(M24)
	0	0	0	1	X	X CS x1
	0	0	1	X	X	X 1.8V
	0	1	X	X	X	X 2.5V
	0	X	X	X	X	Hynix
	1	X	X	X	X	Samsung

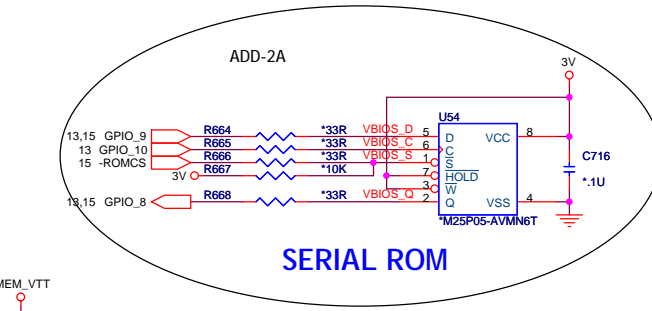
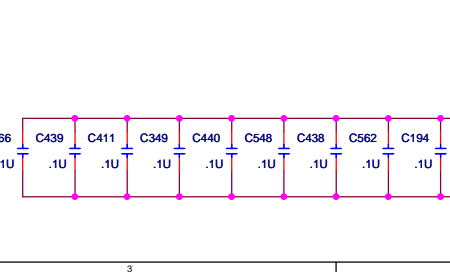
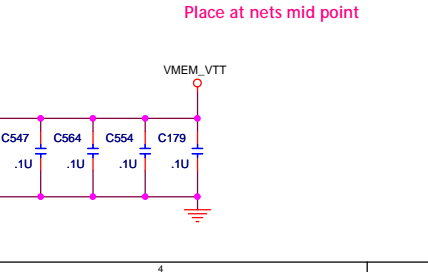
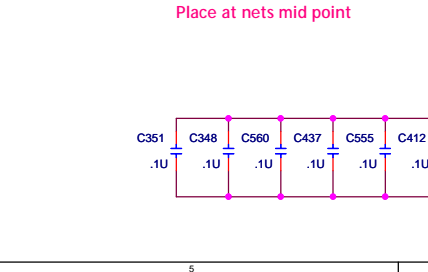
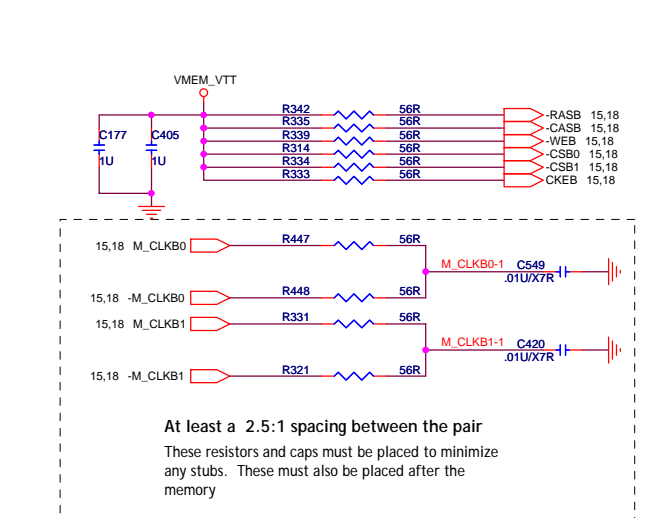
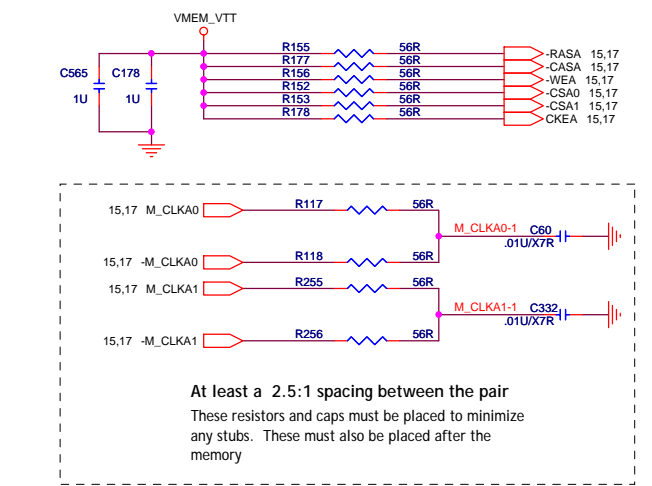
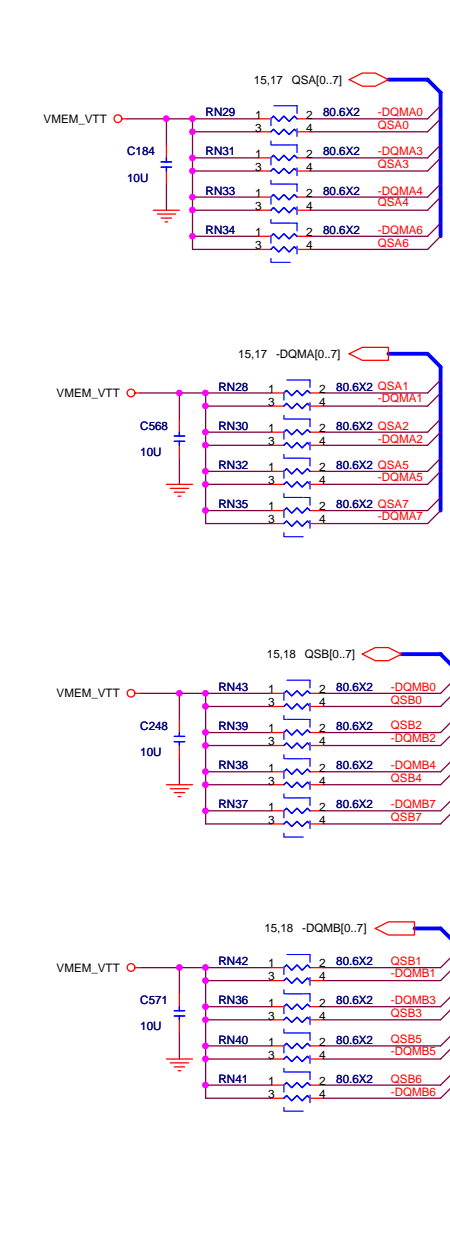
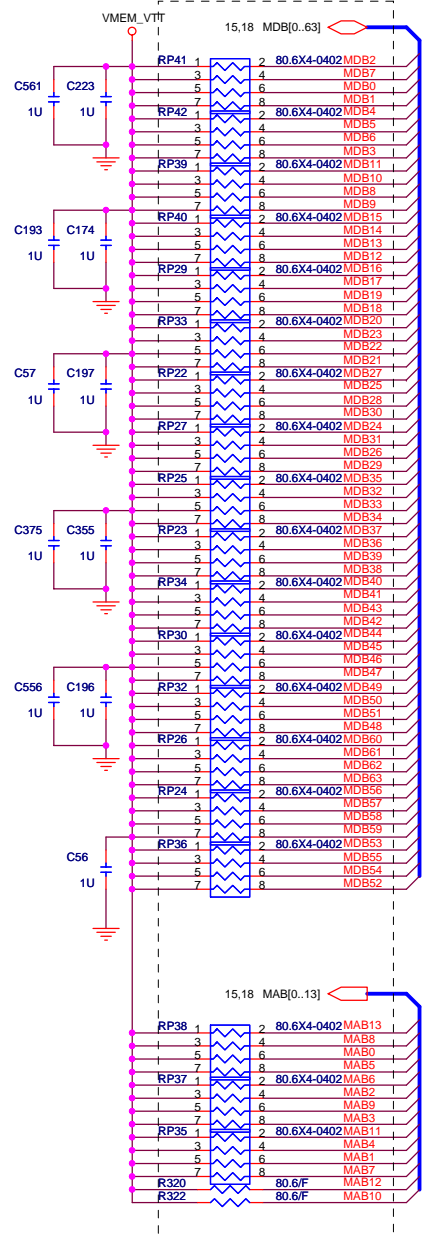
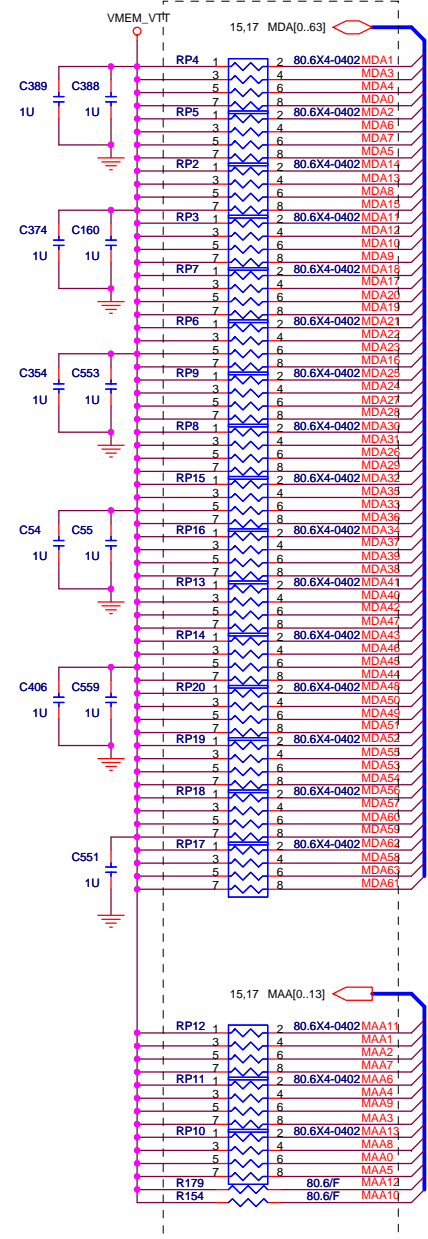


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**Quanta Computer Inc.**

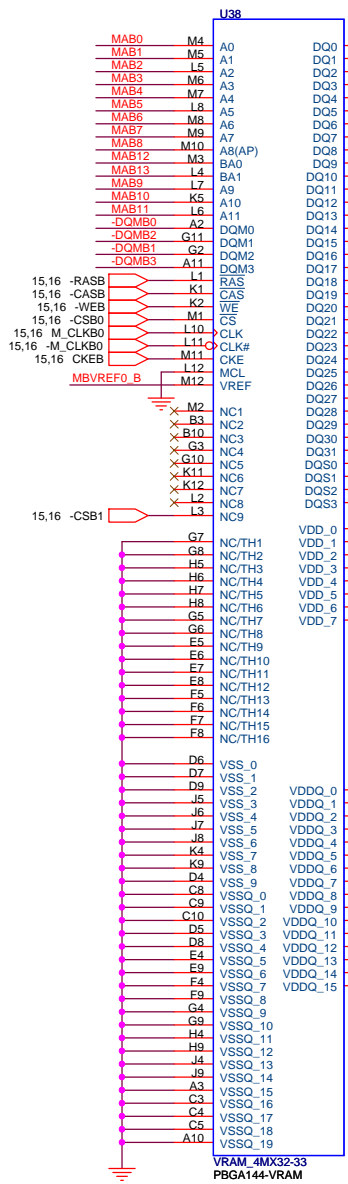
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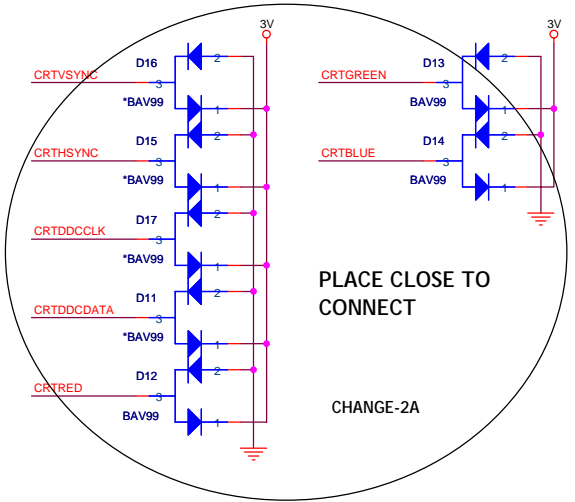
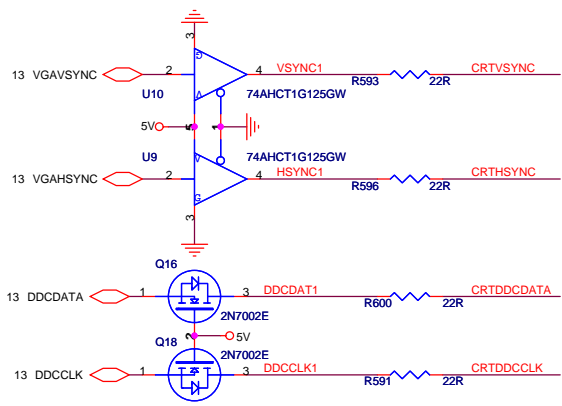
Date: Thursday, March 18, 2004    Sheet: 15 of 38



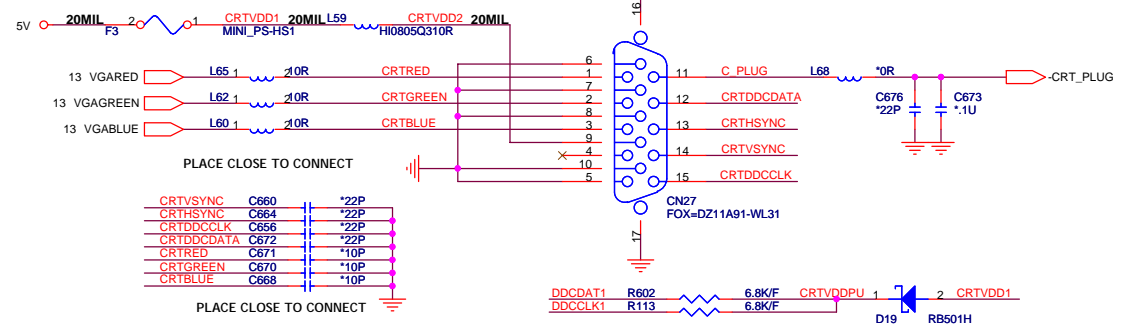




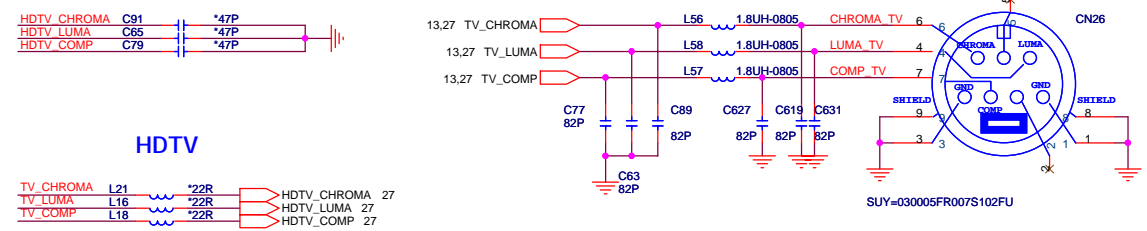




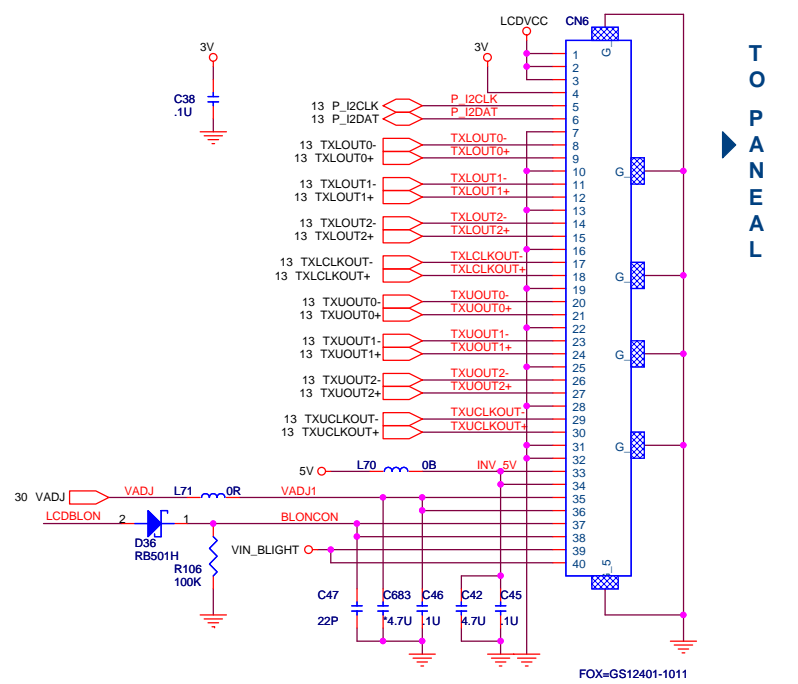
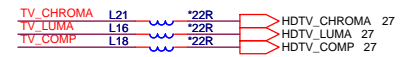
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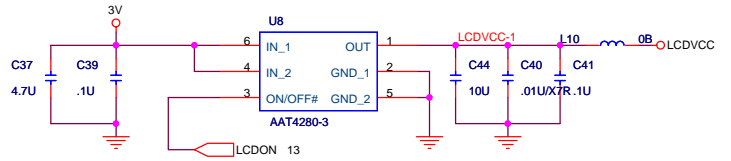
**TV\_OUT**



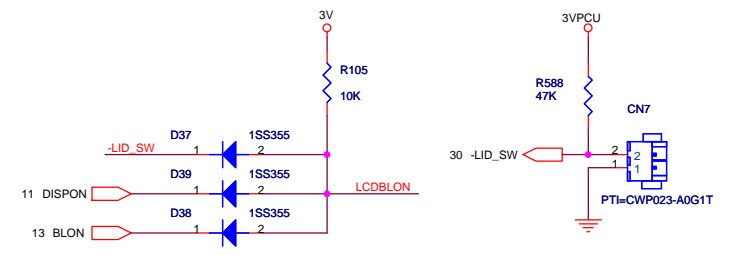
**HDTV**



TOP PANEL

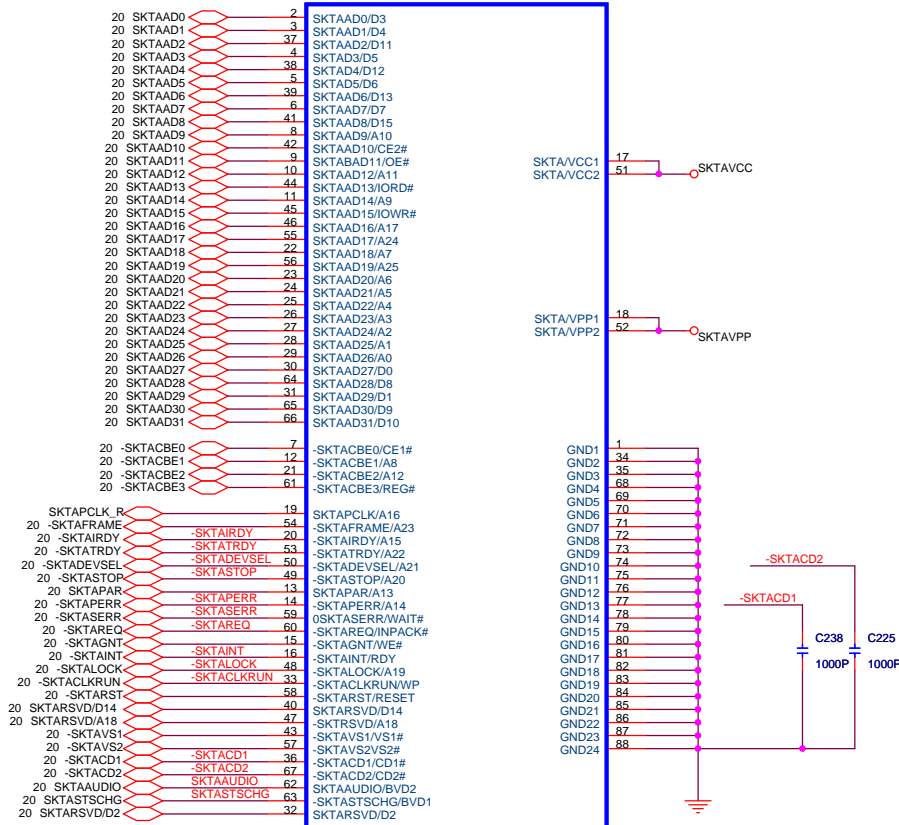


**BACKLIGHT CONTROL**



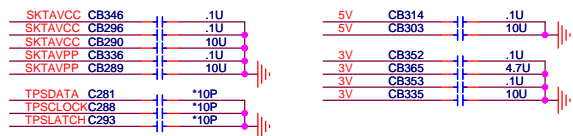
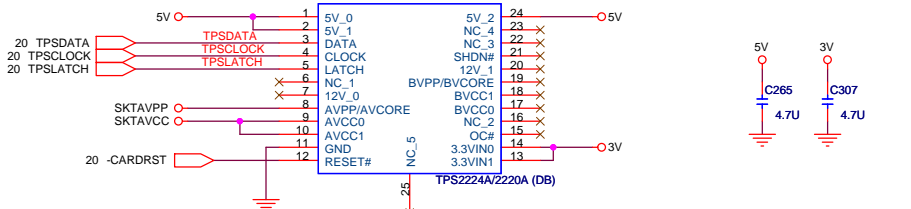


**CN24**

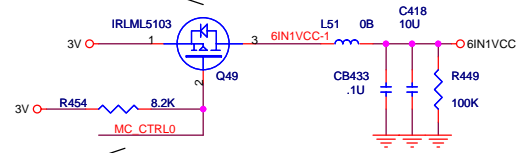


**CARBUS SLOT**  
**FOX=WZ21131-G2**  
**FOX=1CA4C5X2-TC**

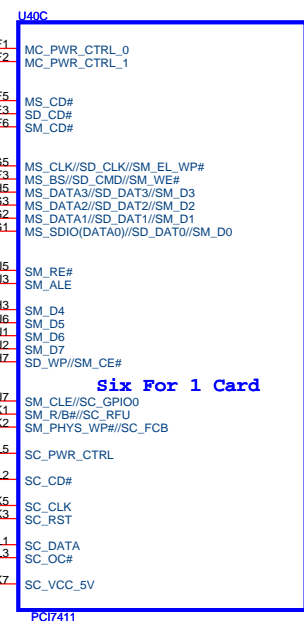
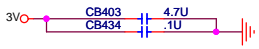
**U17**



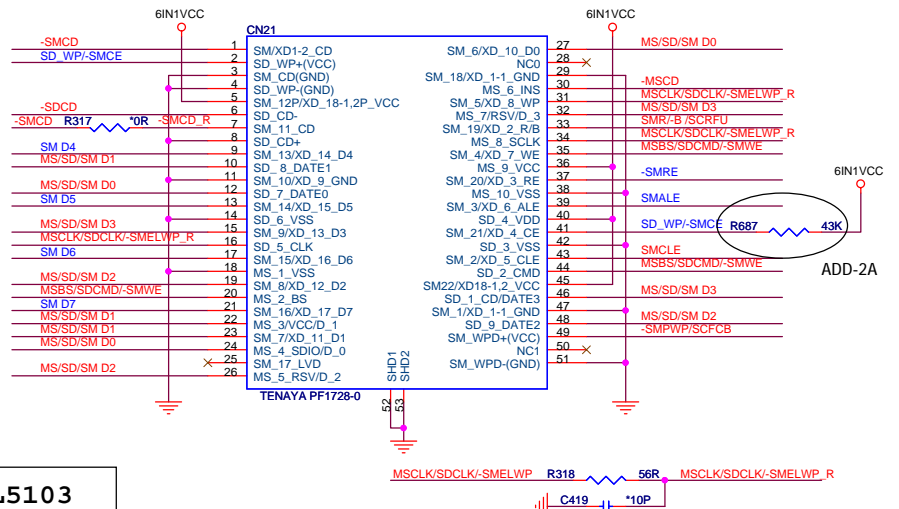
**IRLML5103**  
**Rds (on) = 0.6**



**MC\_PWR\_CTRL low active(default) , or change register to high active**



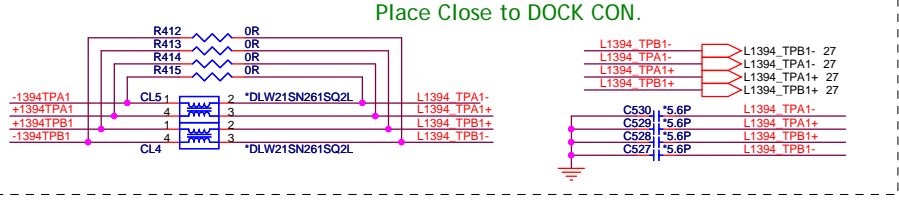
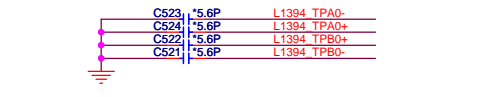
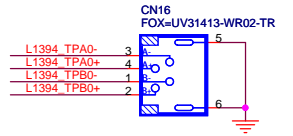
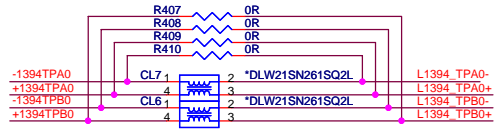
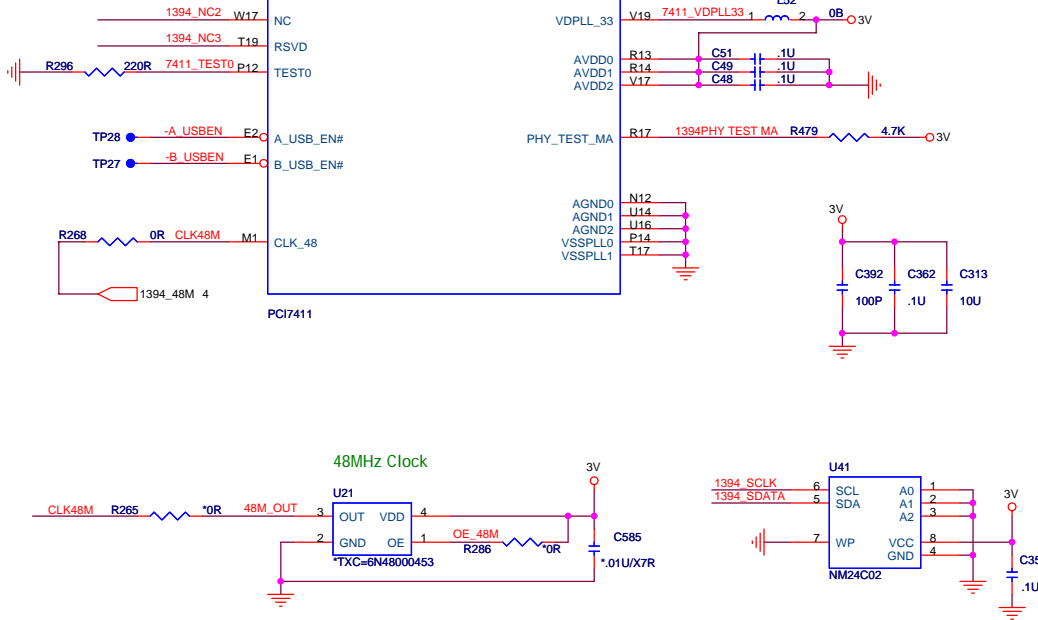
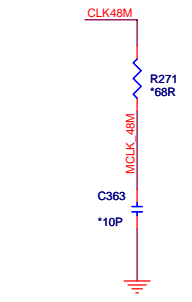
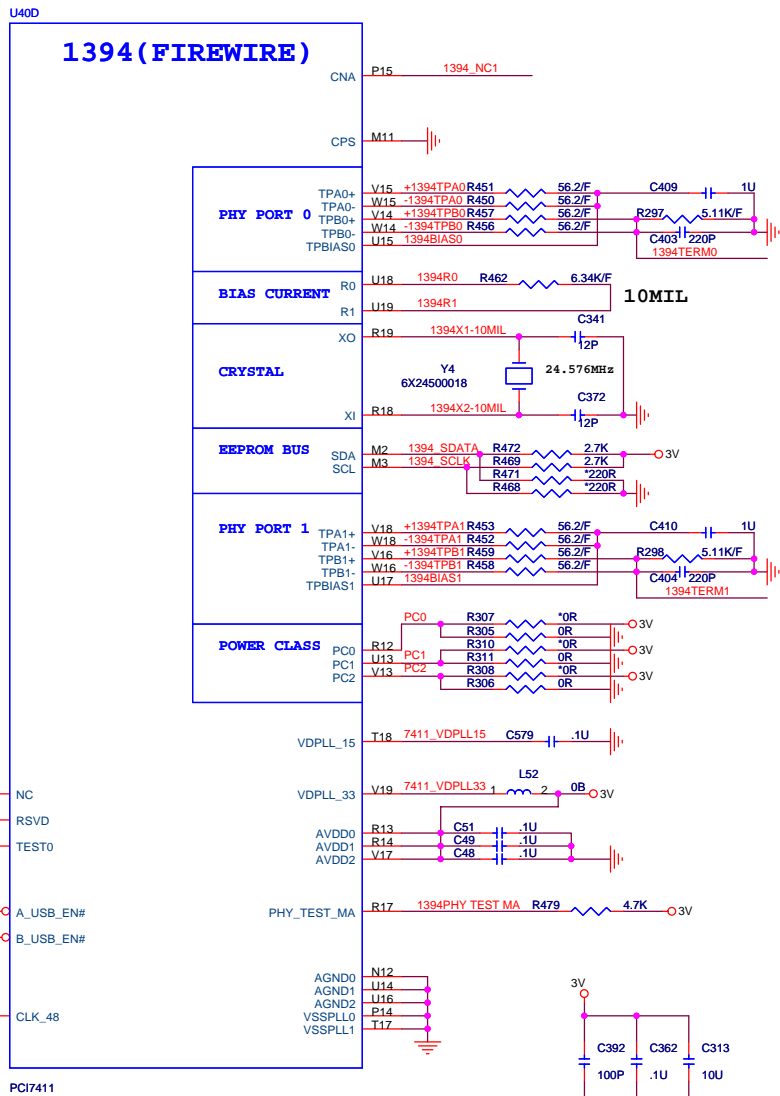
**Six For 1 Card**



- Flash Media Layout Guidelines:**
1. Signal traces should be 60 Ohm +/- 10%.
  2. All signal traces should be routed with equal propagation delay, and with trace lengths as short as practical.
  3. A 56 Ohm damping resistor for MS\_CLK and SD\_CLK should be placed near the PCI7411 source.

**PROJECT : NT2**  
**Quanta Computer Inc.**

Size	Document number	<b>PCMCIA SOCKET/6-IN-1</b>	Rev
Custom			2A
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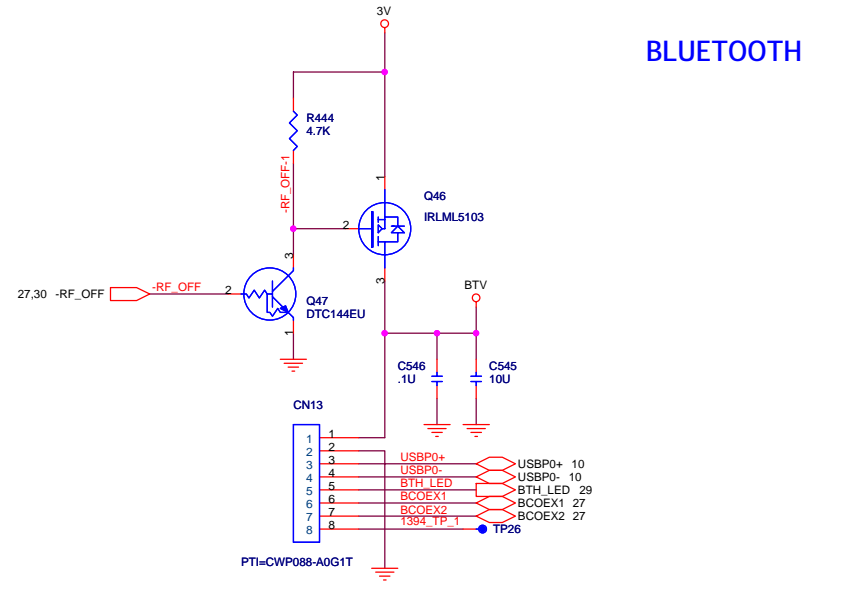


**NOTE:**

- All 1394 signals must be routed on top side only
- 110 ohm +/- 5% differential pairs must be used
- Differential pairs must be 5 mills wide and 10 mills apart
- Parallelism must be maintained throughout differential pairs
- Minimum rise time @ 500 ps

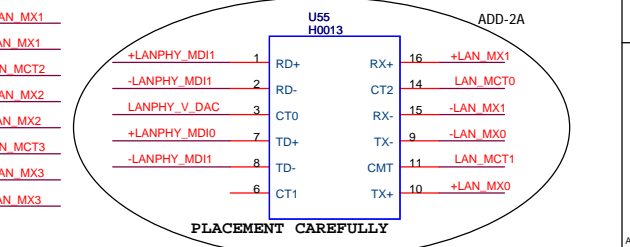
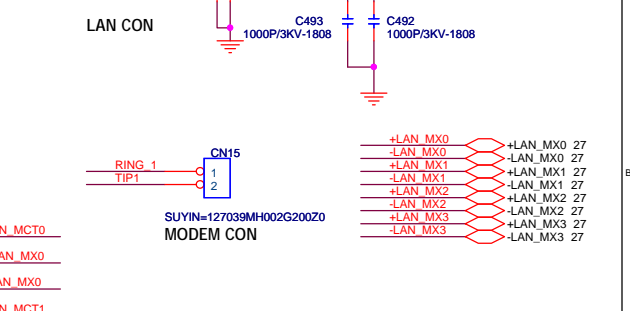
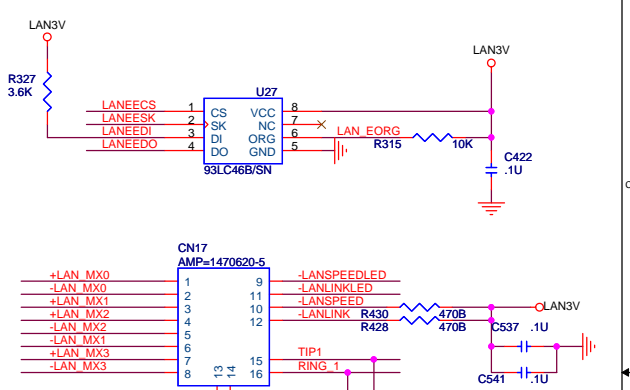
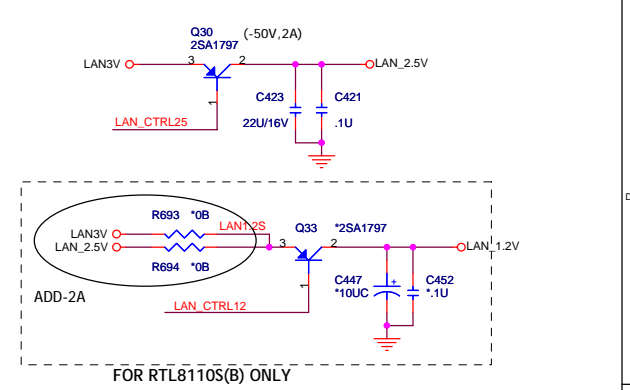
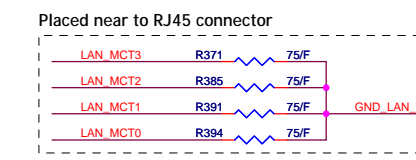
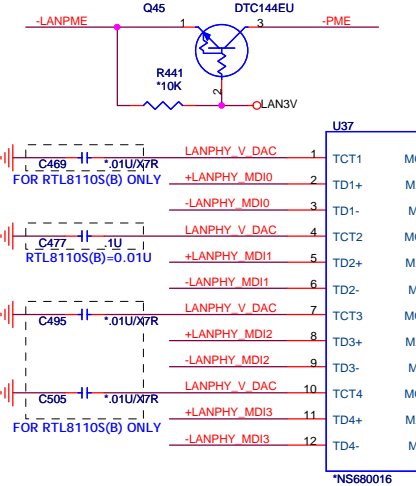
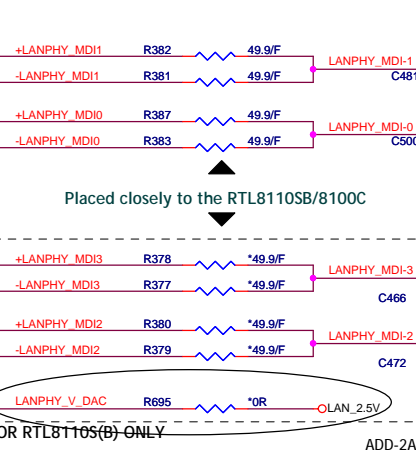
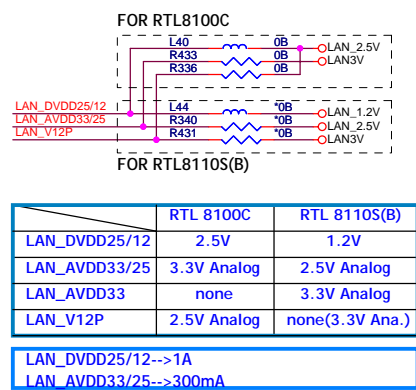
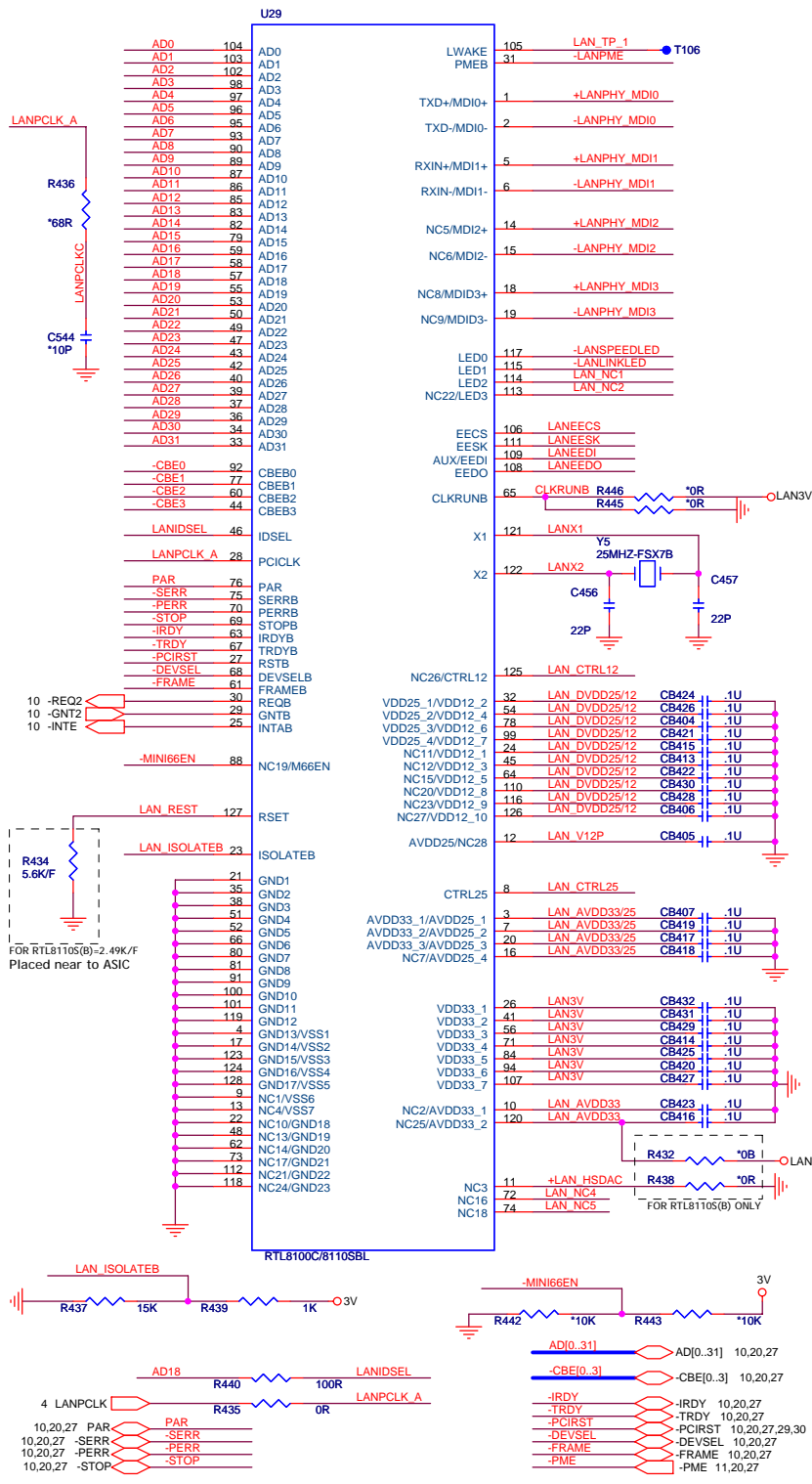
**Place Close to DOCK CON.**

- Fbw @ 700 MHz
- Lambda/2 = 3 inches
- Differential pair must be routed with equal lengths no longer than 3 inches
- Stubs must be kept as short as possible
- All components must be place as close to device as possible



**PROJECT : NT2**  
**Quanta Computer Inc.**

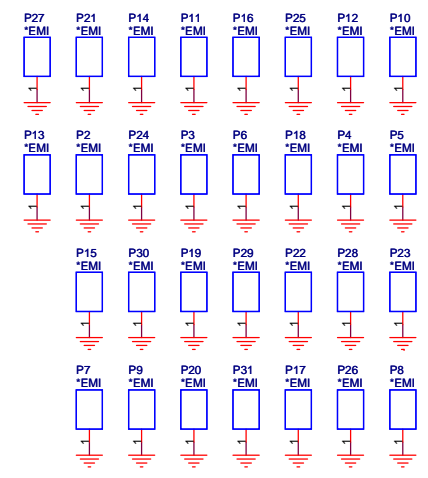
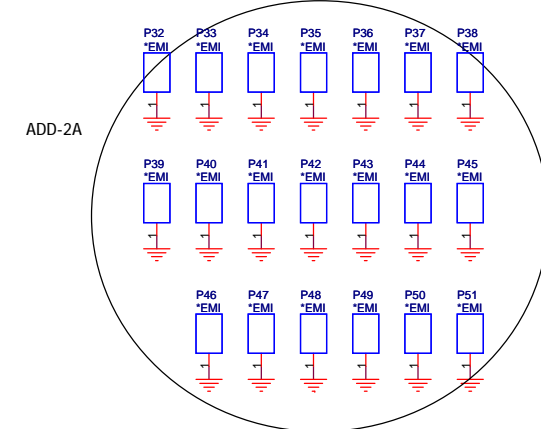
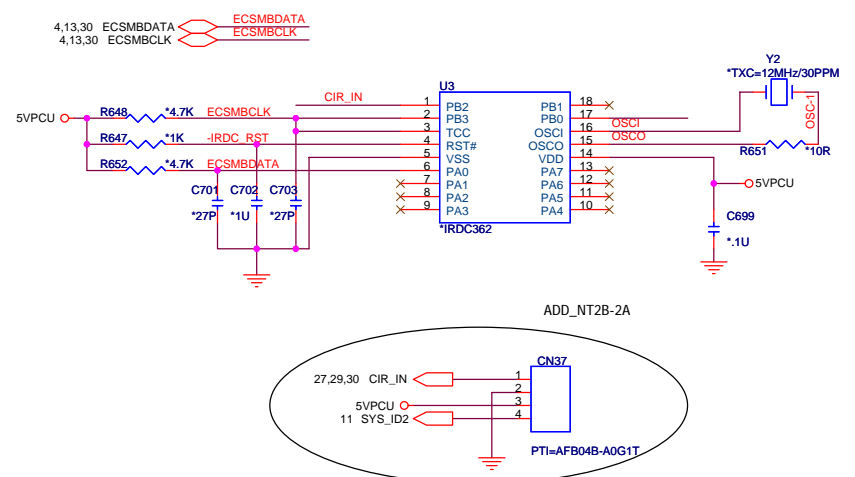
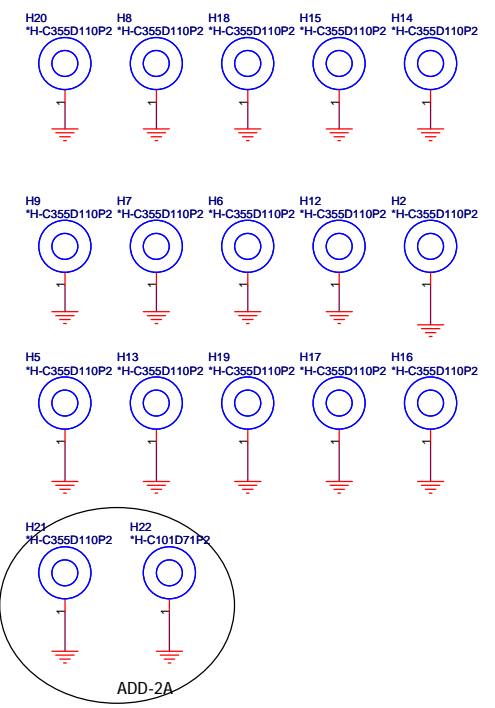
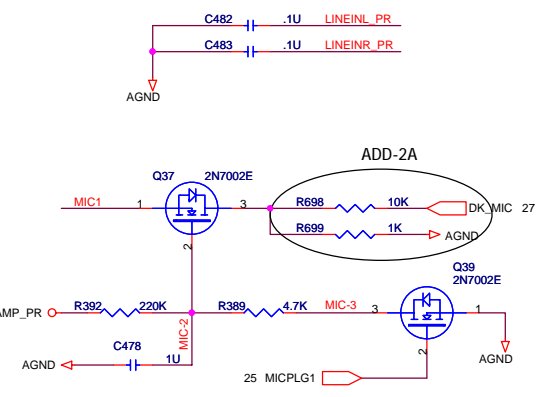
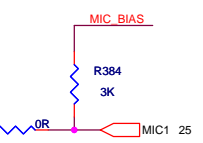
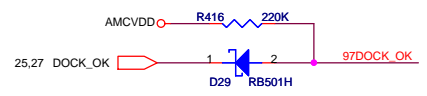
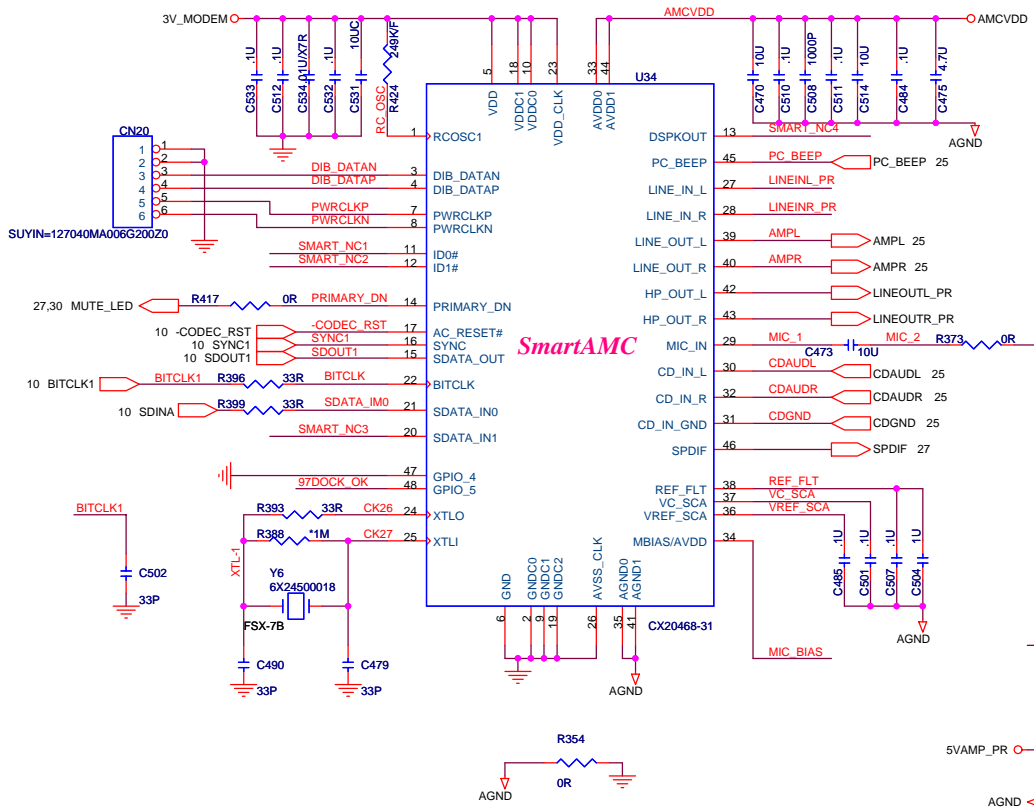
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 Date: Thursday, March 18, 2004 Sheet 22 of 38



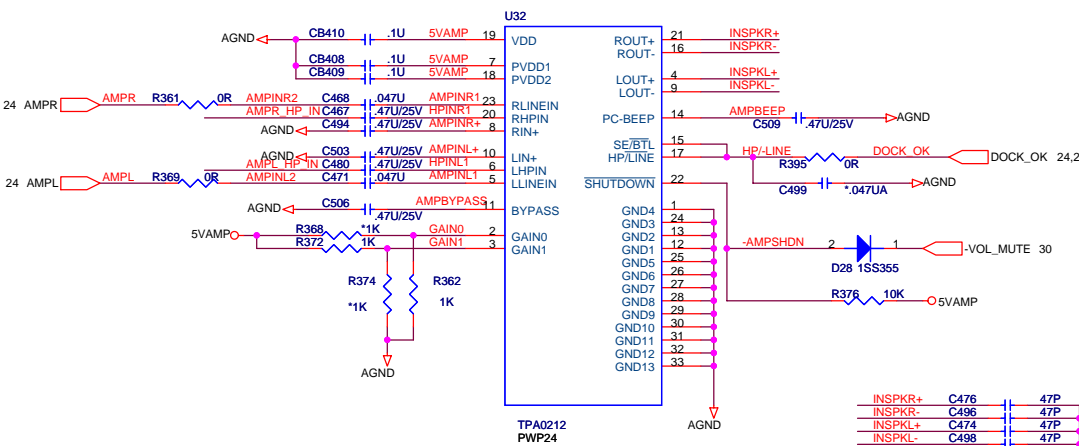
**PROJECT : NT2**  
**Quanta Computer Inc.**

Size: Custom  
Document number: LAN interface RTL8100C/8110SB  
Date: Thursday, March 18, 2004  
Sheet 23 of 38  
Rev 2A

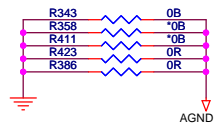
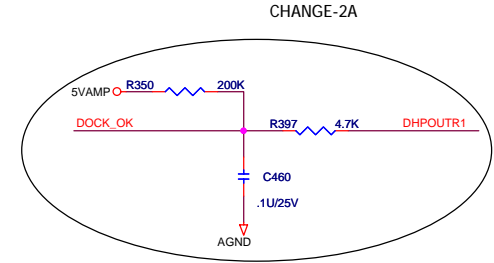
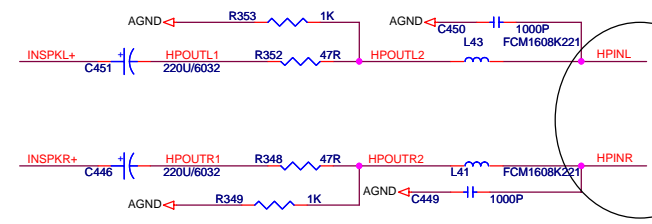
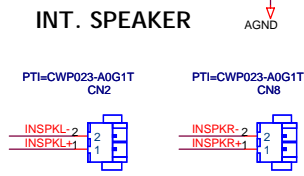
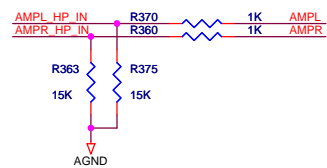




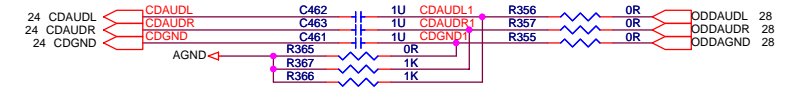
# AUDIO AMPLIFIER



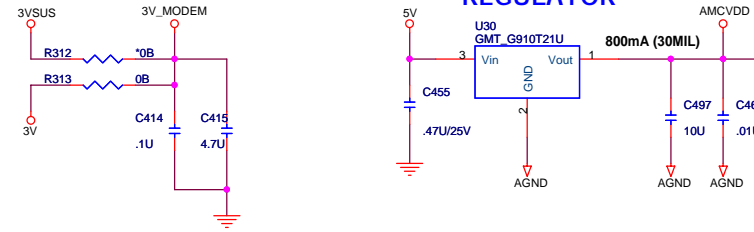
GAIN0	GAIN1	Av
0	0	6dB
0	1	15.6dB
1	0	21.6dB
1	1	27.6dB



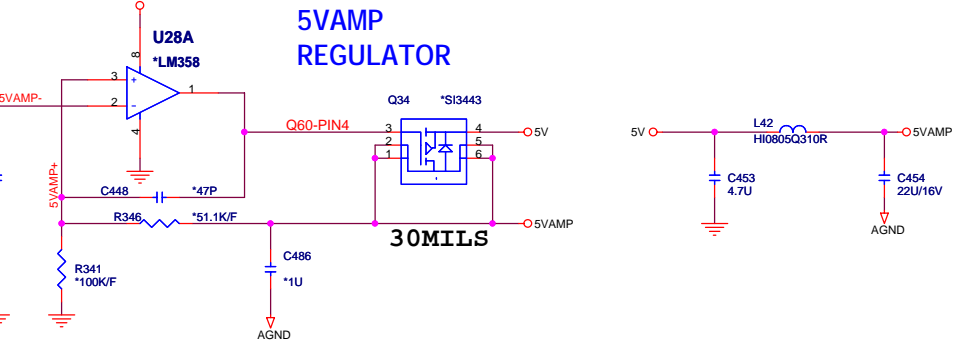
## CD/PHONE INPUT & MONOOUT



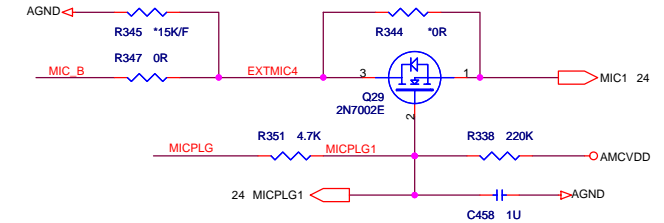
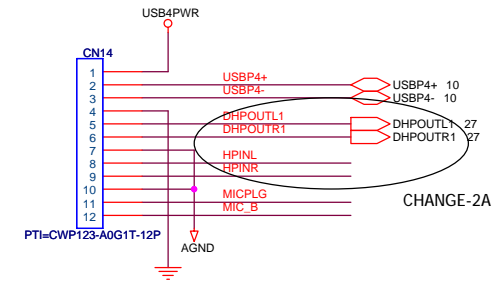
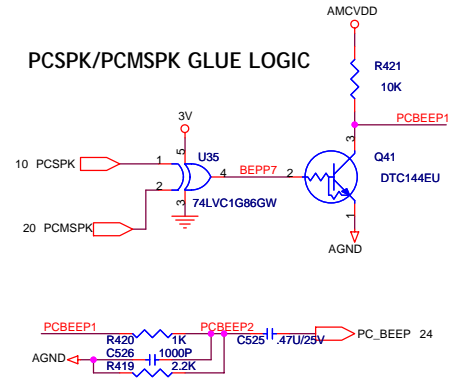
## 3VAUD REGULATOR

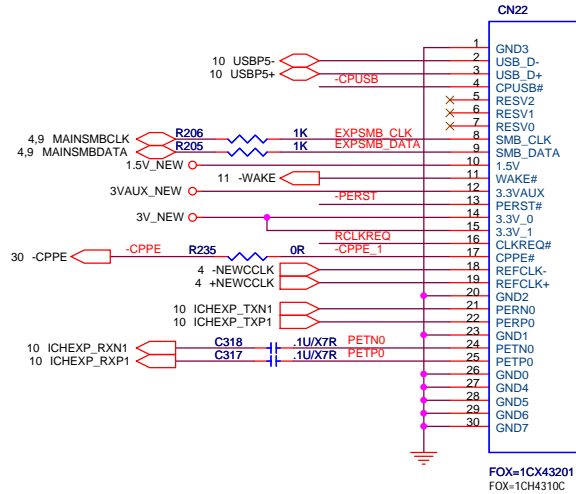
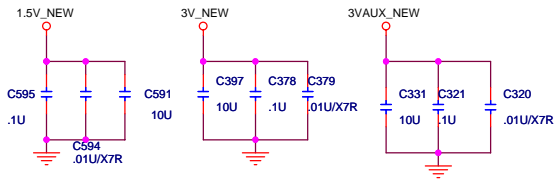
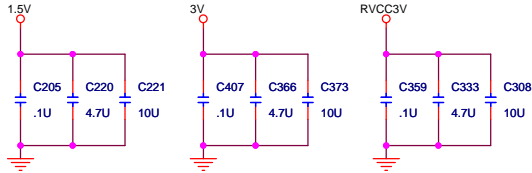
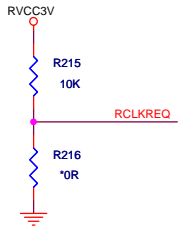


## 5VAMP REGULATOR

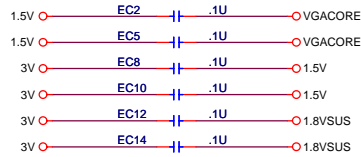
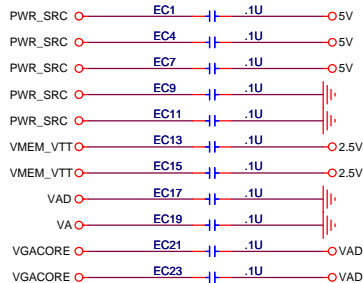
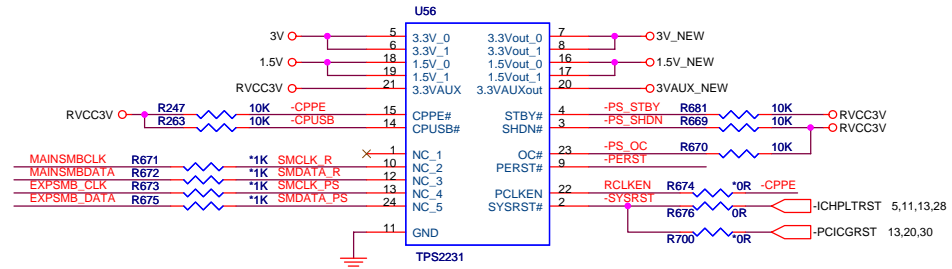


## PCSPK/PCMSPK GLUE LOGIC





CHANGE-2A



EMI

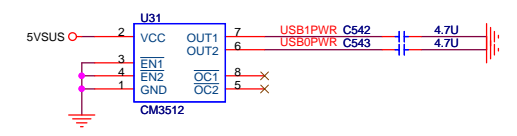
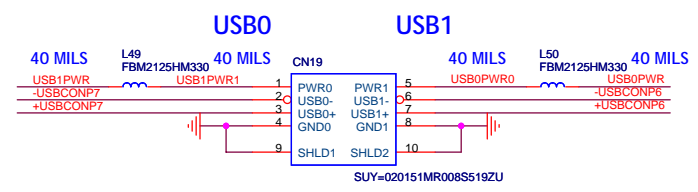
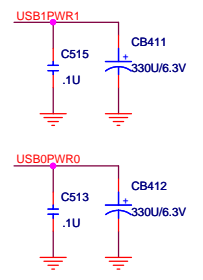
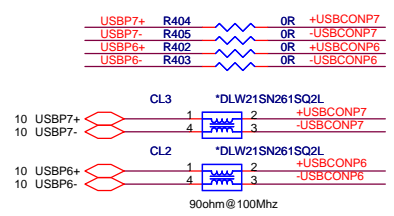
ADD-2A

**PROJECT : NT2**  
**Quanta Computer Inc.**

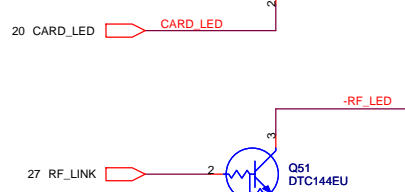
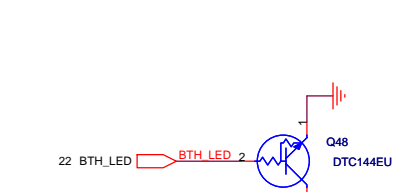
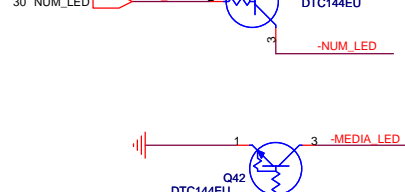
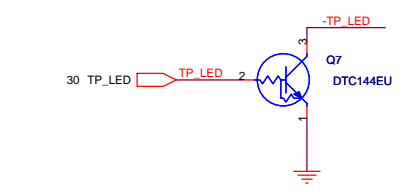
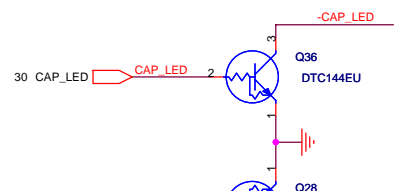
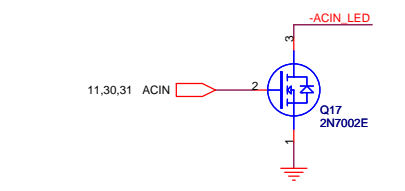
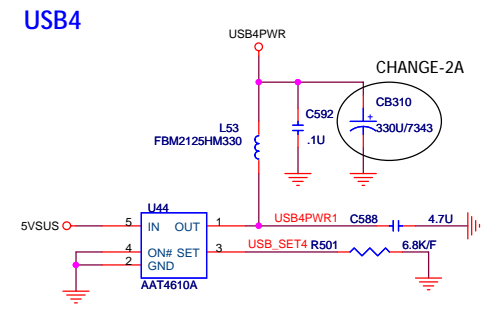
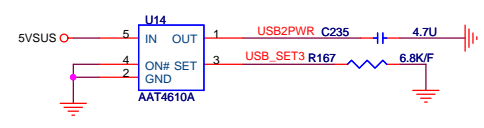
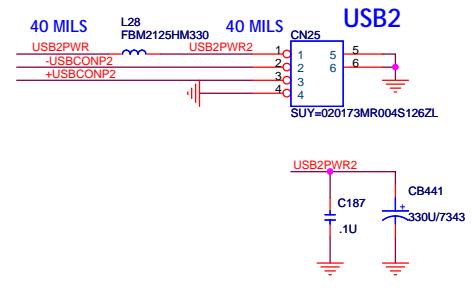
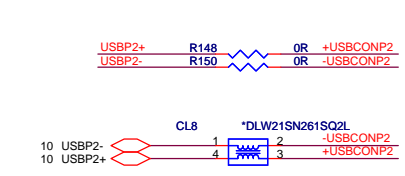
Size Custom	Document number <b>PCI EXPRESS CARD</b>	Rev 2A
Date: Thursday, March 18, 2004      Sheet 26 of 38		



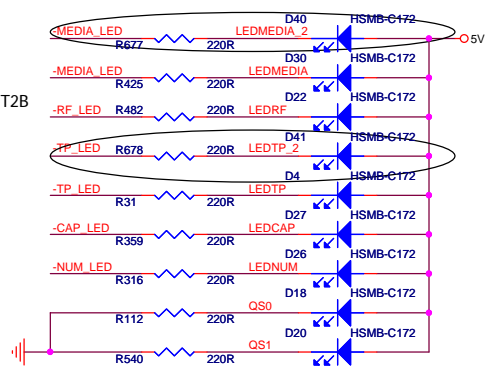




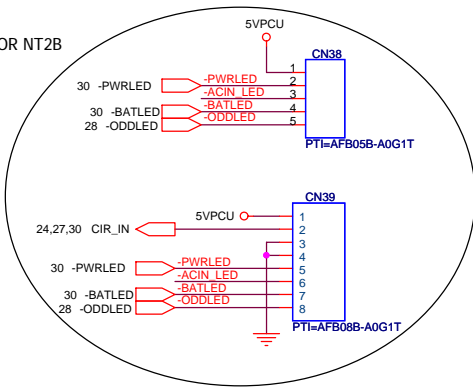
- PLACEMENT NOTICE :**
1. ALL USB PORT RELATIVE R/C/L MUST NEAR USB CONNECTOR
  2. place the common-mode choke as close as possible to the connector pins
  3. max trace length mismatch between usb 2.0 signal pair should be no greater than 150 mils



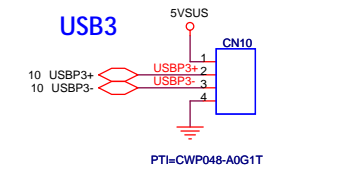
ADD-2A FOR NT2B



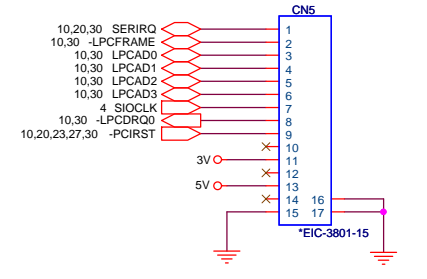
ADD-2A FOR NT2B



**USB3**



**LPC CONN**



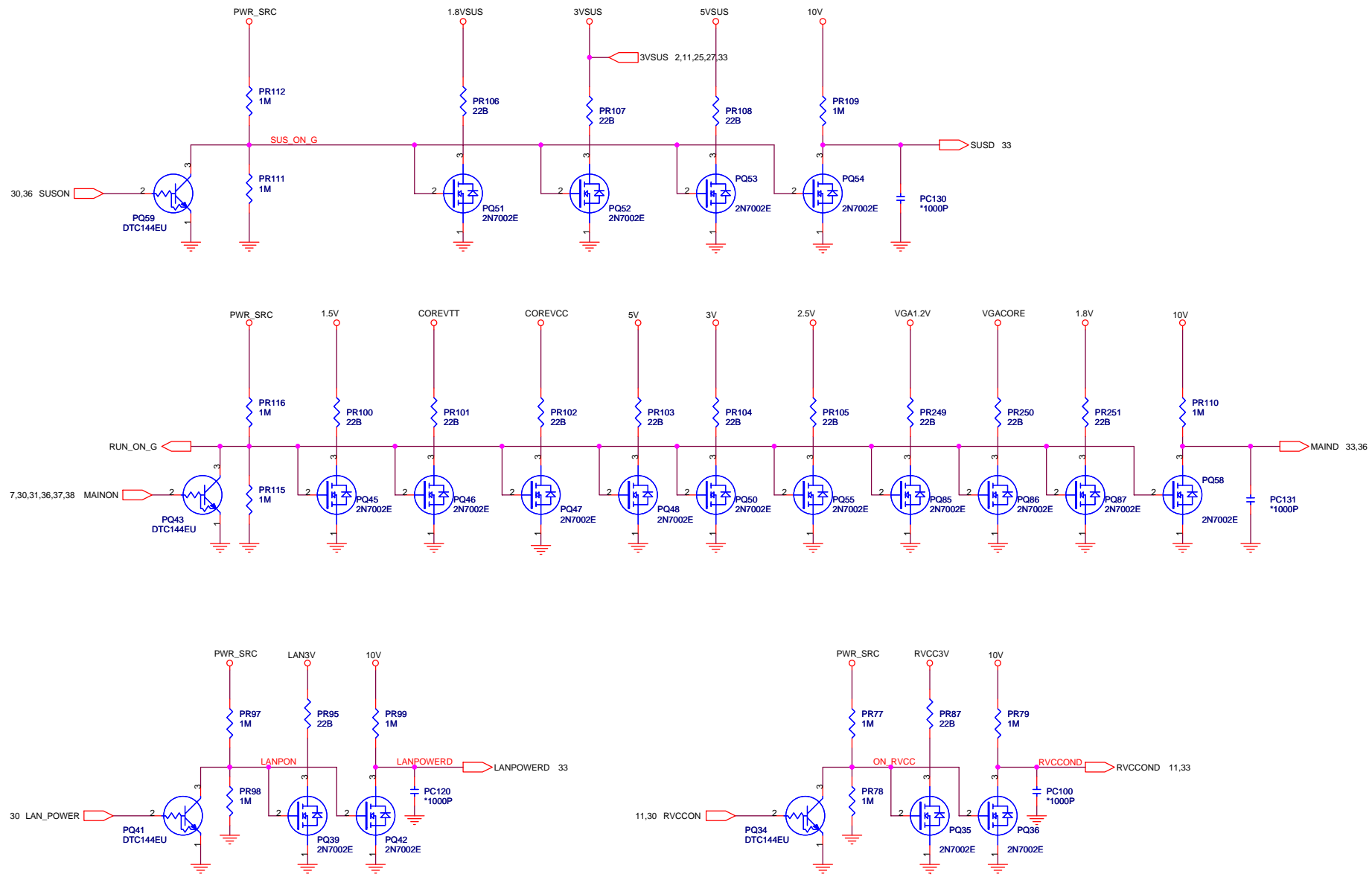
**PROJECT : NT2**  
**Quanta Computer Inc.**


Size	Document number	<b>USB PORT/LED</b>	Rev
Custom			2A
Date:	Thursday, March 18, 2004	Sheet	29 of 38



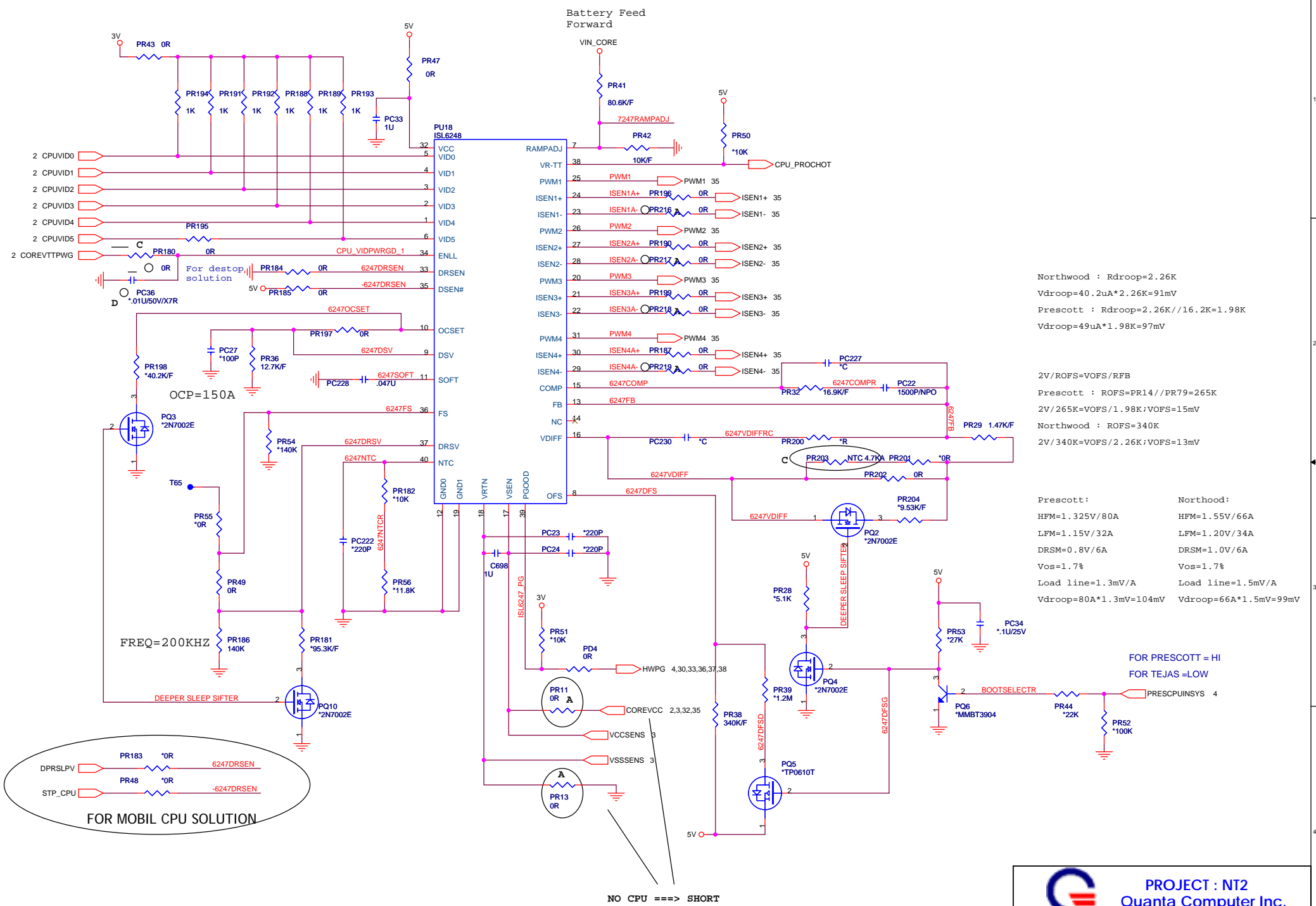






 <b>PROJECT : NT2</b> <b>Quanta Computer Inc.</b>		Rev
		2A
Size	Document number	<b>DISCHARGE CIRCUIT</b>
Custom		
Date:	Thursday, March 18, 2004	Sheet 32 of 38





Northwood : Rdroop=2.26K  
Vdroop=40.2uA\*2.26K=91mV  
Prescott : Rdroop=2.26K//16.2K=1.98K  
Vdroop=49uA\*1.98K=97mV

2V/ROFS=VOFS/RFB  
Prescott : ROFS=PR14//PR79=265K  
2V/265K=VOFS/1.98K;VOFS=15mV  
Northwood : ROFS=340K  
2V/340K=VOFS/2.26K;VOFS=13mV

Prescott :                      Northwood:  
HFM=1.325V/80A                      HFM=1.55V/66A  
LFM=1.15V/32A                      LFM=1.20V/34A  
DRSM=0.8V/6A                      DRSM=1.0V/6A  
Vos=1.7%                      Vos=1.7%  
Load line=1.3mV/A                      Load line=1.5mV/A  
Vdroop=80A\*1.3mV=104mV                      Vdroop=66A\*1.5mV=99mV

FOR MOBIL CPU SOLUTION

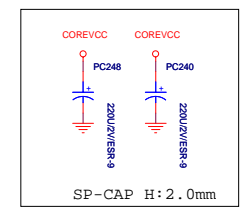
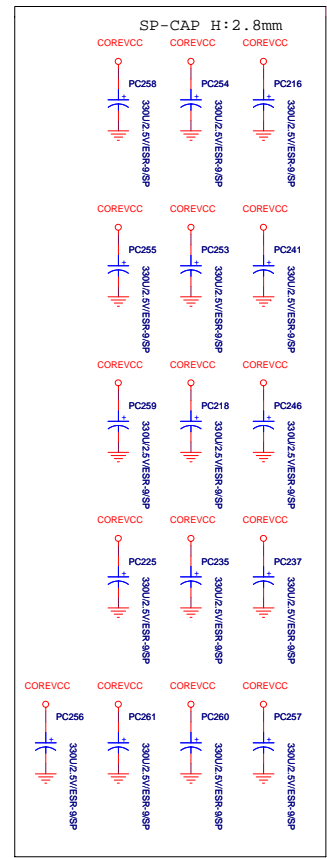
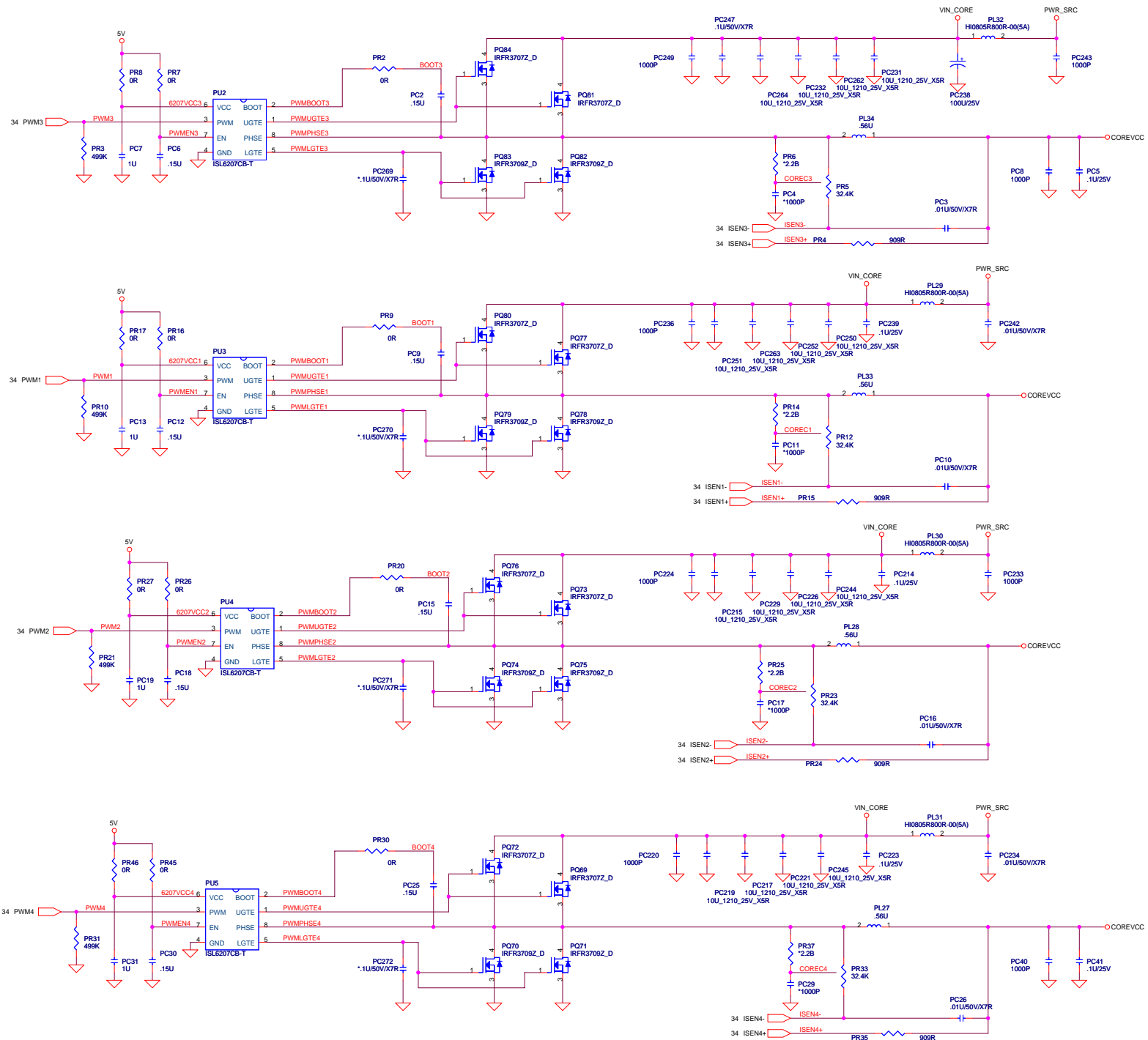
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STP\_CPU    PR48    0R    -6247DRSEN

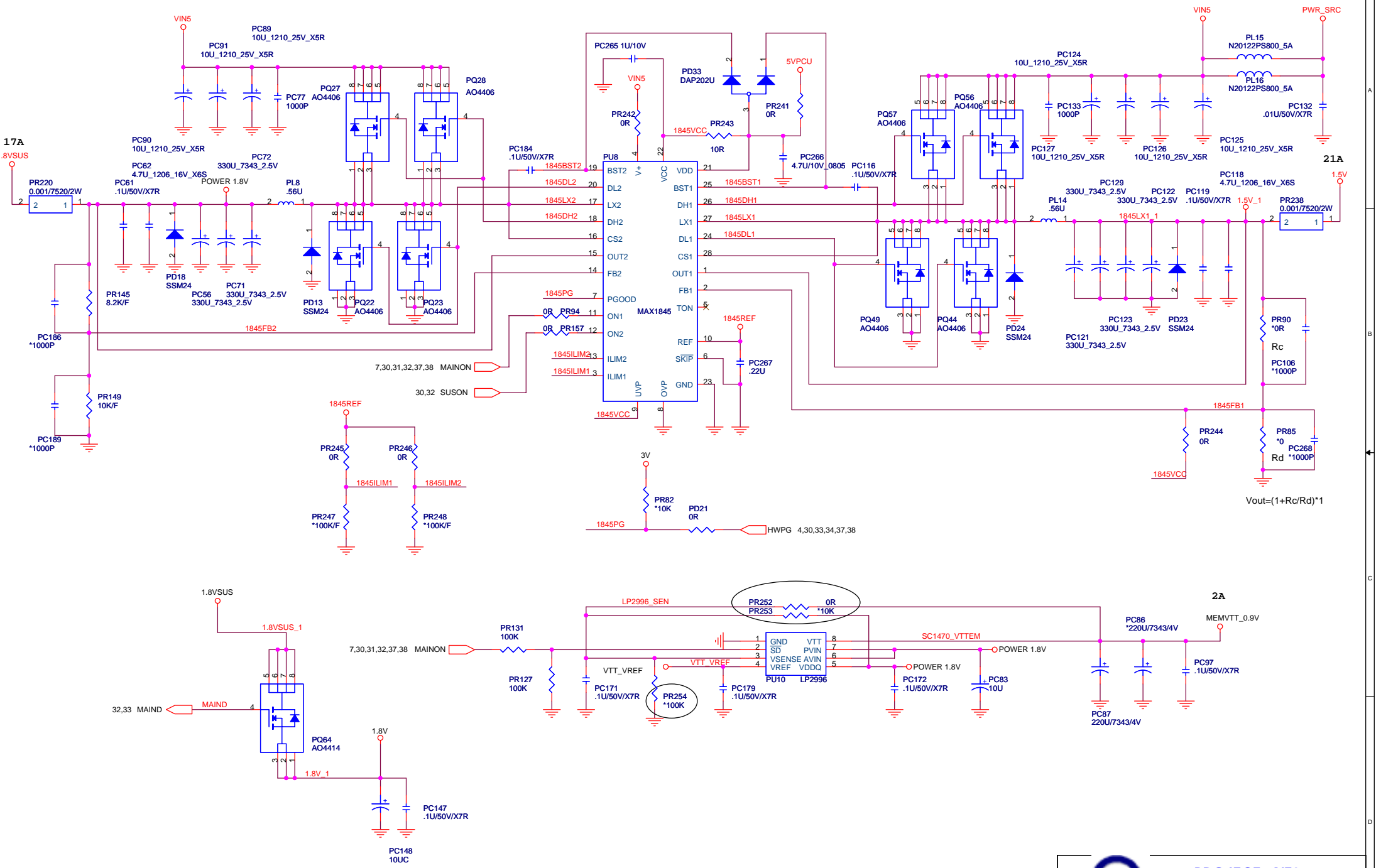
NO CPU ==> SHORT

**PROJECT : NT2**  
Quanta Computer Inc.

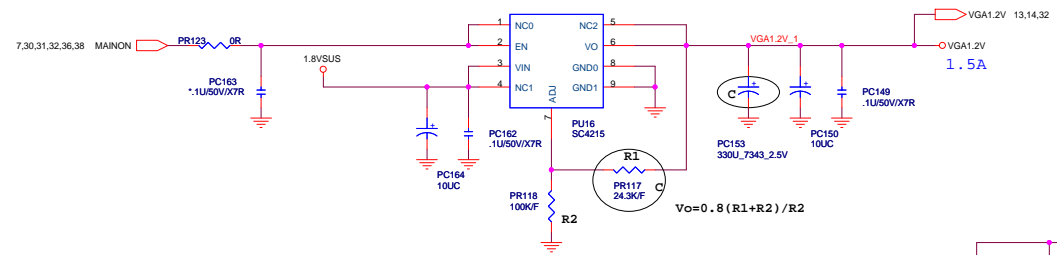
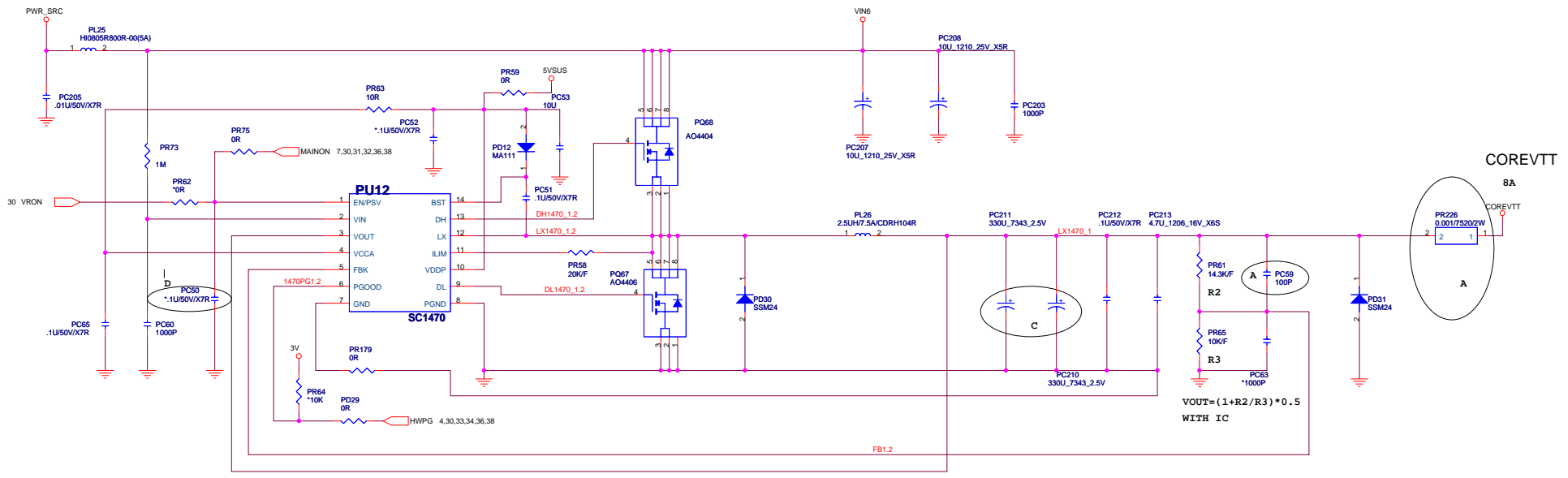
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$V_{out} = (1 + R_c/R_d) * 1$



VGACORECTL

LO	1.2V
HI	1.0V

