R22 SYSTEM DIAGRAM

AMD Smarter Choice

01

DDR3-SODIMM1 PAGE 6

DDR3-SODIMM2 PAGE 7

DDR3 channel A

DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)35W/25W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

HT3

PCI-E

PCI-Express 8X

NORTH BRIDGE
RS880M A12
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

HDMI PAGE 25

CRT PAGE 24

LVDS PAGE 23

VRAM PAGE 22

DDR3

ATI SEYMOUR-XT
23mm X 23mm
PAGE 17,18,19
20,21

Side port

DDR3 RAM for UMA only PAGE 8

X1 Flash Media RTS5219-GR PAGE 26

X1 LAN Realtek PCIE-LAN RTS8165EH-CG (10/100) PAGE 30

X1 Mini PCI-E Card (Wireless LAN) PAGE 33

RJ45 PAGE 30

ALINK X4

SATA - HDD PAGE 29

SATA0 150MB

SATA - CD-ROM PAGE 29

SATA4 150MB

SOUTH BRIDGE
SB820 A13
21mm X 21mm, 605pin FCBGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13,14,15,16

USB2.0

0,5,8 USB2.0 Ports X3 PAGE 29

15 BT softbreeze PAGE 29

2 Webcam X1 PAGE 23

10 PCI-E WLAN Card x1 PAGE 33

Azalia

IDT 92HD80 PAGE 27

DIG MIC PAGE 27

AUDIO CONN (Phone/ MIC) PAGE 28

LPC

ENE KBC
KB3930 Qx
PAGE 32

Keyboard PAGE 31
Touch Pad PAGE 31

FAN PAGE 28

SPI PAGE 31

SYSTEM CHARGER(ISL6251) PAGE 40

SYSTEM POWER ISL6237 PAGE 34

DDR II SMDDR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37

VCCP +1.1V AND +1.2V(RT8204) PAGE 35

VGACORE(1.1V~1.2V)Oz8118 PAGE 38

CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Wednesday, September 15, 2010 Sheet 1 of 43

Use internal CLK GEN

VLDT use 1.5A Max current

+1.1V — R174 *0_6/S — +1.1V_VLDT

+1.1V — R54 *0_6/S — +1.1V_VLDT_R

+2.5V — PBY201209T-221Y-N L31 — +CPUVDDA W/S= 15 mil/20mil

C414 4.7U/6.3V_6 LS0805-100M-N C386 4.7U/6.3V_6 C319 0.22U/25V_6 C322 3300P/50V_4

CPU CLK

12 CPUCLKP — CPUCLKP

12 CPUCLKN — CPUCLKN

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

CPUCLKIN — R150 169/F_4 — CPUCLKIN#

CPUCLKP — C395 3900P/25V_4 — CPUCLKIN

CPUCLKN — C394 3900P/25V_4 — CPUCLKIN#

H_THRMDC — H_THRMDC 5

H_THRMDA — H_THRMDA 5

CPU_PWRGD — 300_4 — R148

CPU_LDT_RST# — 300_4 — R149

CPU_LDT_STOP# — 300_4 — R177

CPU_LDT_REQ#_CPU — *300/F_4 — R147 — +1.5V

+CPUVDDA 250mA

W/S= 15 mil/20mil

C389 10U/6.3V_8 C385 0.22U/6.3V_4 C383 180P/50V_4

+1.1V_VLDT D1 D2 D3 D4

U19A

HT LINK

SOCKET_638_PIN

VLDT_A0 VLDT_A1 VLDT_A2 VLDT_A3

VLDT_B0 VLDT_B1 VLDT_B2 VLDT_B3

+1.1V_VLDT_R AE2 AE3 AE4 AE5 — 10U/6.3V_8 0.22U/6.3V_4 180P/50V_4 10U/6.3V_8 — C111 C126 C133 C548

HT_NB_CPU_CAD_H0 E3 … HT_NB_CPU_CAD_H15 P5

HT_NB_CPU_CLK_H0 J3 … HT_NB_CPU_CLK_L1 K5

HT_NB_CPU_CTL_H0 N1 … HT_NB_CPU_CTL_L1 P4

L0_CADIN_H0 … L0_CADIN_L15

L0_CADOUT_H0 … L0_CADOUT_L15

L0_CLKIN_H0 L0_CLKIN_L0 L0_CLKIN_H1 L0_CLKIN_L1

L0_CLKOUT_H0 L0_CLKOUT_L0 L0_CLKOUT_H1 L0_CLKOUT_L1

L0_CTLIN_H0 L0_CTLIN_L0 L0_CTLIN_H1 L0_CTLIN_L1

L0_CTLOUT_H0 L0_CTLOUT_L0 L0_CTLOUT_H1 L0_CTLOUT_L1

HT_CPU_NB_CAD_H0 AD1 … HT_CPU_NB_CAD_H15 AD5

HT_CPU_NB_CLK_H0 Y1 … HT_CPU_NB_CLK_L1 Y3

HT_CPU_NB_CTL_H0 R2 … HT_CPU_NB_CTL_L1 R5

8 HT_NB_CPU_CAD_H[15..0] — HT_NB_CPU_CAD_H[15..0]

8 HT_NB_CPU_CAD_L[15..0] — HT_NB_CPU_CAD_L[15..0]

8 HT_NB_CPU_CLK_H[1..0] — HT_NB_CPU_CLK_H[1..0]

8 HT_NB_CPU_CLK_L[1..0] — HT_NB_CPU_CLK_L[1..0]

8 HT_NB_CPU_CTL_H[1..0] — HT_NB_CPU_CTL_H[1..0]

8 HT_NB_CPU_CTL_L[1..0] — HT_NB_CPU_CTL_L[1..0]

8 HT_CPU_NB_CAD_H[15..0] — HT_CPU_NB_CAD_H[15..0]

8 HT_CPU_NB_CAD_L[15..0] — HT_CPU_NB_CAD_L[15..0]

8 HT_CPU_NB_CLK_H[1..0] — HT_CPU_NB_CLK_H[1..0]

8 HT_CPU_NB_CLK_L[1..0] — HT_CPU_NB_CLK_L[1..0]

8 HT_CPU_NB_CTL_H[1..0] — HT_CPU_NB_CTL_H[1..0]

8 HT_CPU_NB_CTL_L[1..0] — HT_CPU_NB_CTL_L[1..0]

FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

SideBand Temp sense I2C

5 CPU_SIC — CPU_SIC AF4

5 CPU_SID — CPU_SID AF5

5 CPU_ALERT — CPU_ALERT AE6

12 CPU_LDT_RST# — CPU_LDT_RST# B7

12 CPU_PWRGD — CPU_PWRGD A7

10,12 CPU_LDT_STOP# — CPU_LDT_STOP# F10

CPU_LDT_REQ#_CPU C6

+1.5VSUS — R169 510/F_4 — CPUTEST25H — R168 510/F_4 — CPUTEST25L

+1.1V_VLDT — R81 44.2/F_4 — CPU_HTREF0 R6

R83 44.2/F_4 — CPU_HTREF1 P6

place them to CPU within 1.5"

36 CPU_VDD0_RUN_FB_H — F6

36 CPU_VDD0_RUN_FB_L — E6

36 CPU_VDD1_RUN_FB_H — Y6

36 CPU_VDD1_RUN_FB_L — AB6

CPU_DBRDY G10

CPU_TMS AA9

CPU_TCK AC9

CPU_TRST# AD9

CPU_TDI AF9

T4 — CPUTEST23 AD7

T24 — CPUTEST18 H10

T27 — CPUTEST19 G9

CPUTEST25H E9

CPUTEST25L E8

place them to CPU within 1.5"

T108 — CPUTEST21 AB8

CPUTEST20 AF7

CPUTEST24 AF7

CPUTEST22 AE8

T5 — CPUTEST12 AC8

T3 — CPUTEST27 AF8

R160 *0_4/S C2 AA6

+1.5VSUS — R375 300/F_4 CPU_DBREQ# — R310 1K/F_4 CPUTEST27 — R309 *300/F_4

U19D

SOCKET_638_PIN

VDDA1 VDDA2 — +CPUVDDA F8 F9

CLKIN_H CLKIN_L — CPUCLKIN A9 A8

RESET_L — CPU_LDT_RST# B7

PWROK — CPU_PWRGD A7

LDTSTOP_L — CPU_LDT_STOP# F10

LDTREQ_L — CPU_LDT_REQ#_CPU C6

SIC — CPU_SIC AF4

SID — CPU_SID AF5

ALERT_L — CPU_ALERT AE6

HT_REF0 — CPU_HTREF0 R6

HT_REF1 — CPU_HTREF1 P6

VDD0_FB_H VDD0_FB_L — F6 E6

VDD1_FB_H VDD1_FB_L — Y6 AB6

DBRDY — CPU_DBRDY G10

TMS — CPU_TMS AA9

TCK — CPU_TCK AC9

TRST_L — CPU_TRST# AD9

TDI — CPU_TDI AF9

TEST23 — T4 CPUTEST23 AD7

TEST18 — T24 CPUTEST18 H10

TEST19 — T27 CPUTEST19 G9

TEST25_H — CPUTEST25H E9

TEST25_L — CPUTEST25L E8

TEST21 — T108 CPUTEST21 AB8

TEST20 — CPUTEST20 AF7

TEST24 — CPUTEST24 AF7

TEST22 — T5 CPUTEST22 AE8

TEST12 — T3 CPUTEST12 AC8

TEST27 — CPUTEST27 AF8

TEST9 — R160 *0_4/S C2

TEST6 — AA6

RSVD1 A3 RSVD2 A5 RSVD3 B3 RSVD4 B5 RSVD5 C1

VSS M11 RSVD11 W18

CLKIN_H A6 CLKIN_L A4 — CPU_SVC_R CPU_SVD_R

RESET_L — CPU_LDT_RST#

PWROK — CPU_PWRGD

LDTSTOP_L — CPU_LDT_STOP#

LDTREQ_L — CPU_LDT_REQ#_CPU

THERMTRIP_L AF6 — CPU_THERMTRIP_L#

PROCHOT_L AC7 — CPU_PROCHOT_L#

MEMHOT_L AA8 — CPU_MEMHOT_L# — T10

SIC — CPU_SIC

SID — CPU_SID

ALERT_L — CPU_ALERT

THERMDC W7 — H_THRMDC

THERMDA W8 — H_THRMDA

HT_REF0 — CPU_HTREF0

HT_REF1 — CPU_HTREF1

VDD0_FB_H W9 VDD0_FB_L Y9 — VDDIO_FB_H VDDIO_FB_L — VDDIO_FB_H 37 VDDIO_FB_L 37

VDD1_FB_H H6 VDD1_FB_L G6 — CPU_VDDNB_RUN_FB_H CPU_VDDNB_RUN_FB_L — 36 36

DBRDY — CPU_DBREQ# F10

TMS — DBREQ_L

TCK — CPU_TDO AE9

TRST_L — TDO

TDI

TEST23 — TEST28_H J7 TEST28_L H8

TEST18 — TEST17 D7 — CPUTEST17 — T45

TEST19 — TEST16 E7 — CPUTEST16 — T40

TEST25_H — TEST15 F7 — CPUTEST15 — T26

TEST25_L — TEST14 C7 — CPUTEST14 — T49

TEST21 — TEST7 C3

TEST20 — TEST10 K8 — R163 *300/F_4 — +1.1V_VLDT

TEST24

TEST22 — TEST8 C4 — CPUTEST29H — T46

TEST12

TEST27

TEST29_H C9 — R116

TEST29_L C8 — 80.6/F_4

CPUTEST29L — T50

RSVD1 H18 RSVD2 H19 RSVD3 AA7 RSVD4 D5 RSVD5 C5

RSVD10 RSVD9 RSVD8 RSVD7 RSVD6

Route as 80ohm, diff

HDT Connector

CN4

+1.5VSUS

CPU_LDT_RST_HTPA#
CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO

HDT CONN
88511-2001-20p-l

SI Change HDT connector fo FFC type

Can remove on MP

+3V — C718 0.1U/10V_4

U30 TC7SH08FU

CPU_LDT_RST_HTPA# — CPU_LDT_RST#

Serial VID

+1.5VSUS — R181 *1K/F_4 — CPU_SVC_R — R188 *0_4/S — CPU_SVC

+1.5V — R182 *1K/F_4 — CPU_SVD_R — R189 *0_4/S — CPU_SVD

CPU_PWRGD — R191 *0_4/S — CPU_PWRGD_SVID_REG

R203 1K/F_4 — +1.5VSUS

R204 1K/F_4 — +1.5V

CPU_SVC 36

CPU_SVD 36

CPU_PWRGD_SVID_REG 36

R198 *220_4

R197 *220_4

R199 *220_4

VFIX MODE — VID Override table (VDD)

SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

CPUTEST12 R47 1K/F_4

CPUTEST19 R104 1K/F_4

CPUTEST18 R106 1K/F_4

CPUTEST20 R311 1K/F_4

CPUTEST21 R53 1K/F_4

CPUTEST22 R52 1K/F_4

CPUTEST24 R49 1K/F_4

+1.5VSUS — R224 10K/F_4

+1.5VSUS — R225 300_4

CPU_PROCHOT_L# — R209 *0_4/S

32 CPU_PROCHOT# — R219 *0_4/S — Q26 MMBT3904 — CPU_PROCHOT_R# — CPU_PROCHOT_R# 12

EC new option

+1.5VSUS — R187 10K/F_4

+1.5VSUS — R373 1K/F_4 — Q23 MMBT3904

5 CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — CPU_THERMTRIP# 13

NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G4 HT,CTL I/F 1/3	1A

Date: Wednesday, September 15, 2010 Sheet 3 of 43

Processor Memory Interface

04

VDDR = 0.9V for 25W & 35W CPU

VDDR = 1.05V for 35W & 45W CPU

PLACE THEM CLOSE TO CPU WITHIN 1"

U19B MEM:CMD/CTRL/CLK

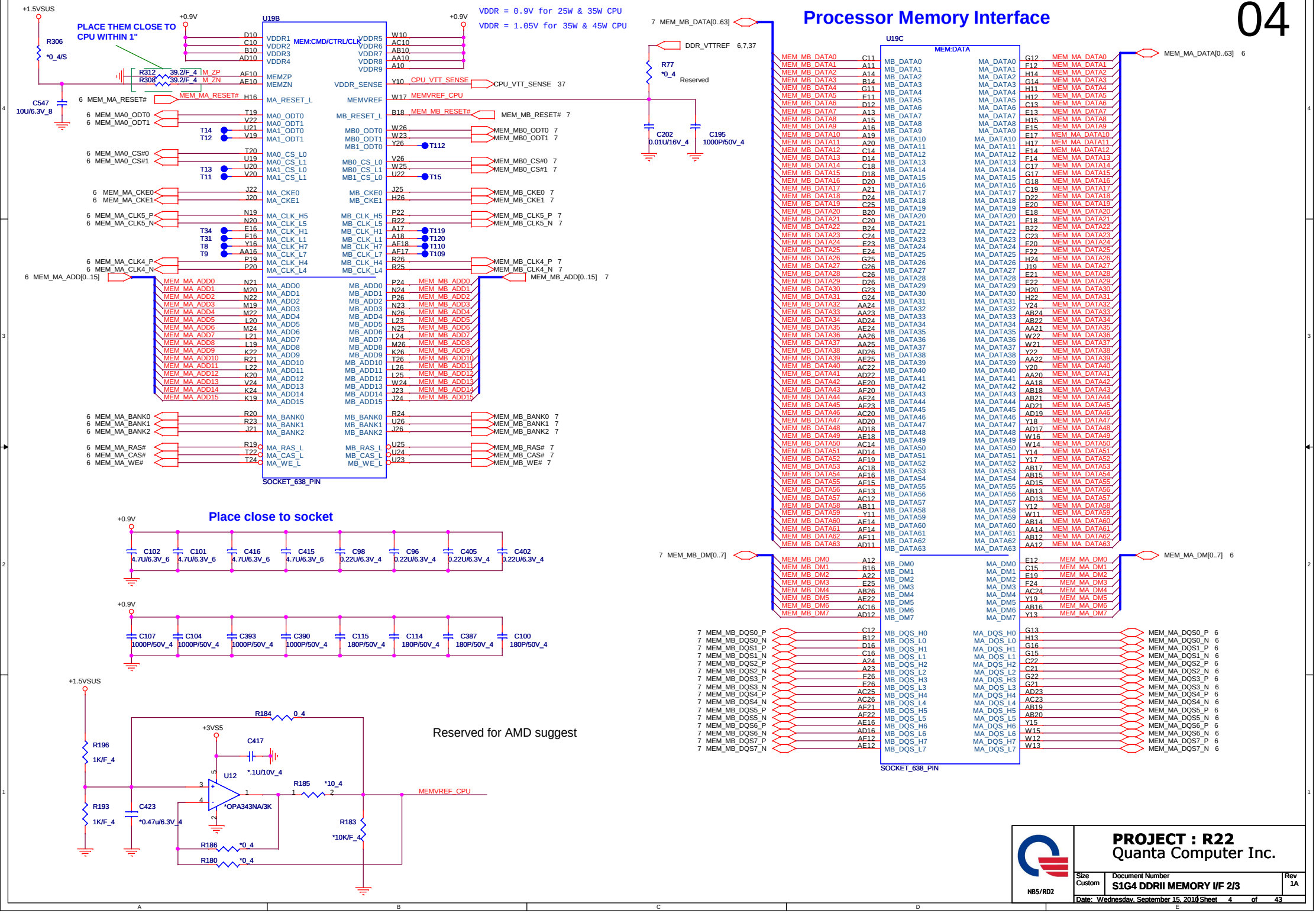
SOCKET_638_PIN

Place close to socket

Reserved for AMD suggest

U19C MEM:DATA

SOCKET_638_PIN



PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G4 DDRII MEMORY I/F 2/3	1A

Date: Wednesday, September 15, 2010 Sheet 4 of 43

NB5/RD2

PROCESSOR POWER AND GROUND

BOTTOM SIDE DECOUPLING

+VCORE: C201 22U/6.3V_8, C235 22U/6.3V_8, C249 22U/6.3V_8, C266 22U/6.3V_8, C275 0.22U/6.3V_4, C274 0.01U/16V_4, C273 180P/50V_4

+VCORE: C261 22U/6.3V_8, C270 22U/6.3V_8, C247 22U/6.3V_8, C234 22U/6.3V_8, C198 0.22U/6.3V_4, C199 0.01U/16V_4, C197 180P/50V_4

+CPUVDDNB: C243 22U/6.3V_8, C229 22U/6.3V_8, C256 22U/6.3V_8

+1.5VSUS: C231 22U/6.3V_8, C246 22U/6.3V_8, C257 0.22U/6.3V_4, C276 0.22U/6.3V_4, C277 180P/50V_4

DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE

+1.5VSUS: C128 4.7U/6.3V_6, C137 4.7U/6.3V_6, C309 4.7U/6.3V_6, C307 4.7U/6.3V_6, C130 0.22U/6.3V_4, C134 0.22U/6.3V_4

+1.5VSUS: C144 0.22U/6.3V_4, C141 0.22U/6.3V_4, C208 0.01U/16V_4, C193 0.1U/10V_4, C305 180P/50V_4, C303 180P/50V_4, C209 0.1U/10V_4

U19E — SOCKET_638_PIN

+VCORE, +CPUVDDNB 4A, +1.5VSUS 2A, +1.5VSUS

U19F — SOCKET_638_PIN

+1.5VSUS: R226 2K/F_4, R206 2K/F_4, R216 1K/F_4, R201 1K/F_4, R176 1K/F_4

Q27 MMBT3904, Q25 MMBT3904, RB501V-40 D20, RB501V-40 D19

32,40 MBCLK — MBCLK — CPU_SIC — CPU_SIC 3

32,40 MBDATA — MBDATA — CPU_SID — CPU_SID 3

CPU_ALERT — CPU_ALERT 3

+3V: R367 10K/F_4, R368 10K/F_4, R360 10K/F_4

+3V: R356 200/F_6, C619 0.1U/10V_4

U22 MSOP — G786P8

32 MBCLK2 — SCLK, VCC

32 MBDATA2 — SDA, DXP

13 PM_THERM# — ALERT#, DXN

OVERT#, GND

C621 1000P/50V_4

H_THRMDA 3, H_THRMDC 3

SMBALERT#

Q24 MMBT3904: R190 *0_4/S, 3920_RST# — 3920_RST# 32

D18 CH501H-40PT: ECPWROK — ECPWROK 16,20,32

R194 10K/F_4 — +3V

+1.5V: R374 10K/F_4

Q36 MMBT3904: 3 CPU_THERMTRIP_L# — CPU_THERMTRIP_L# — SMBALERT#

PQ30 *2N7002E-G: R200 10K/F_4 — TEMP_FAIL 18

ADD VGA TEMP_ FAIL function
M92 is active Hi

+1.5V_VGA: EC10 *0.01U/16V_4 — +3V

+1.8V_VGA: EC14 *0.01U/16V_4 — +3V

+VGA_CORE: EC8 *0.01U/16V_4 — +3V

+VGA_CORE: EC5 *0.1U/10V_4, +3V: EC12 *0.1U/10V_4

+1.5V_VGA: EC11 *0.01U/16V_4 — +3V

+5V: EC6 *0.01U/16V_4 — +3V

+1.5VSUS: EC9 *0.01U/16V_4 — +1.1V

+VGA_CORE: EC13 *0.01U/16V_4 — +1.8V_VGA

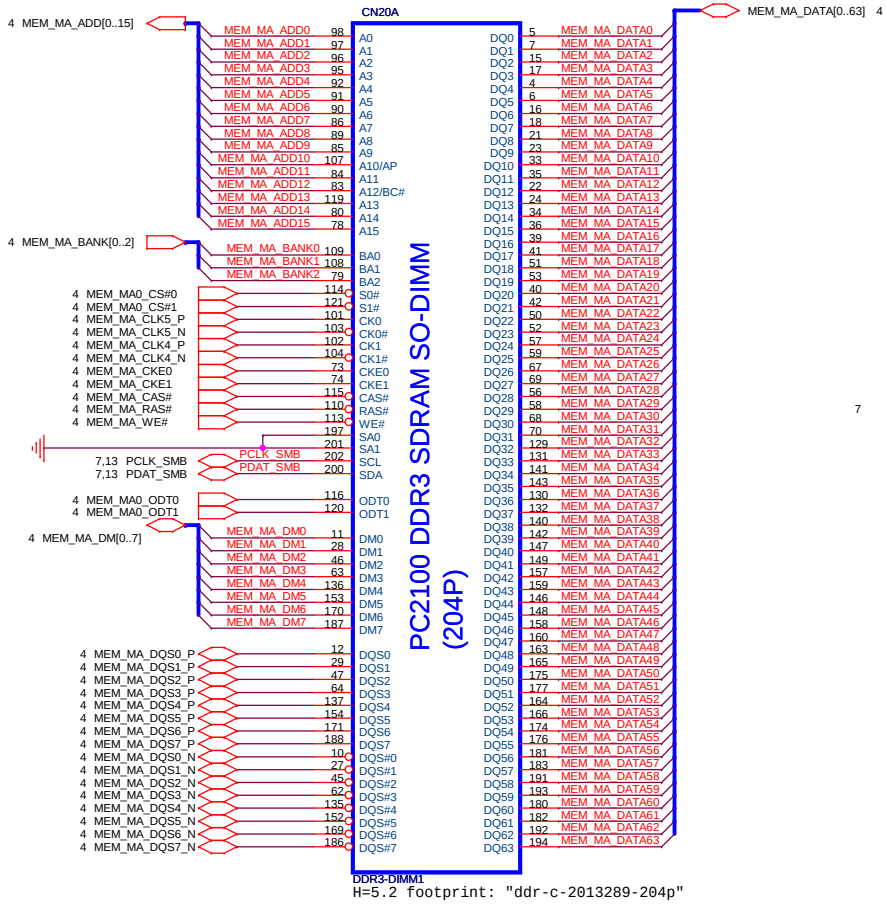
For fix HyperTransport nets across plane splits

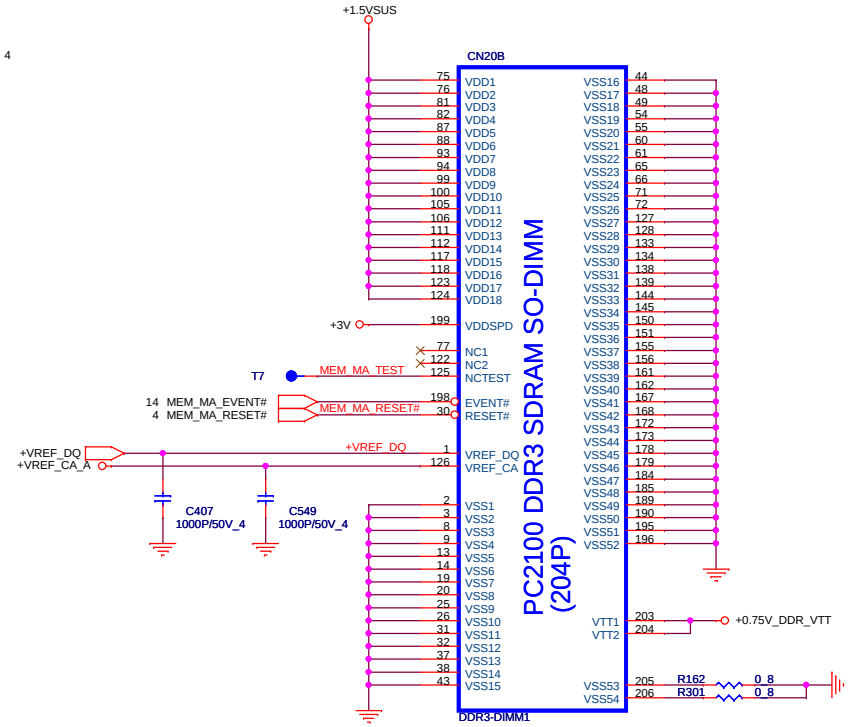
NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G4 PWR & GND 3/3	1A

Date: Wednesday, September 15, 2010 Sheet 5 of 43



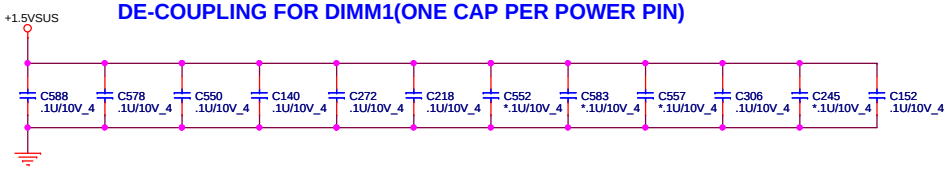


SO-DIMM BYPASS PLACEMENT :

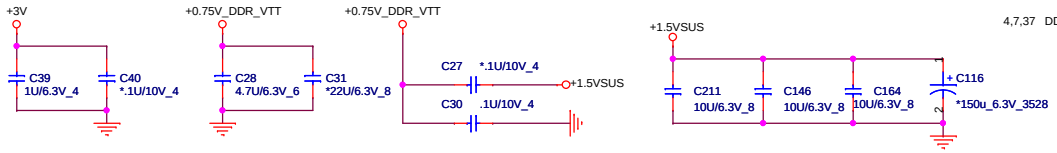
Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

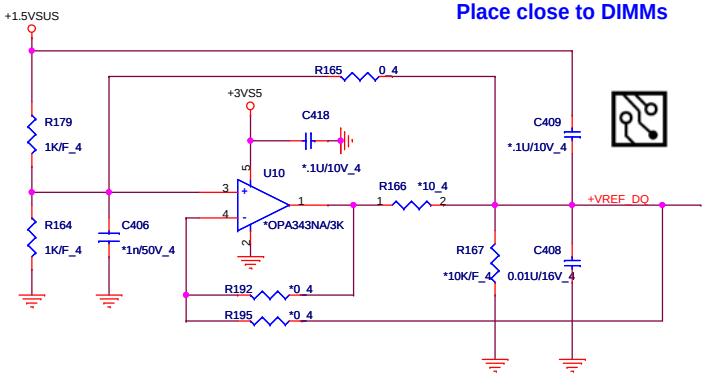
DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)

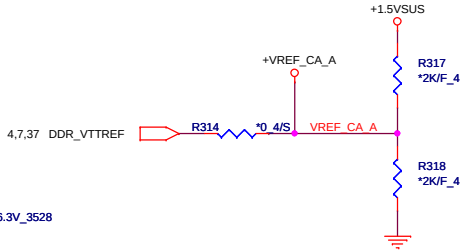


DE-COUPLING FOR DIMM1



Place close to DIMMs



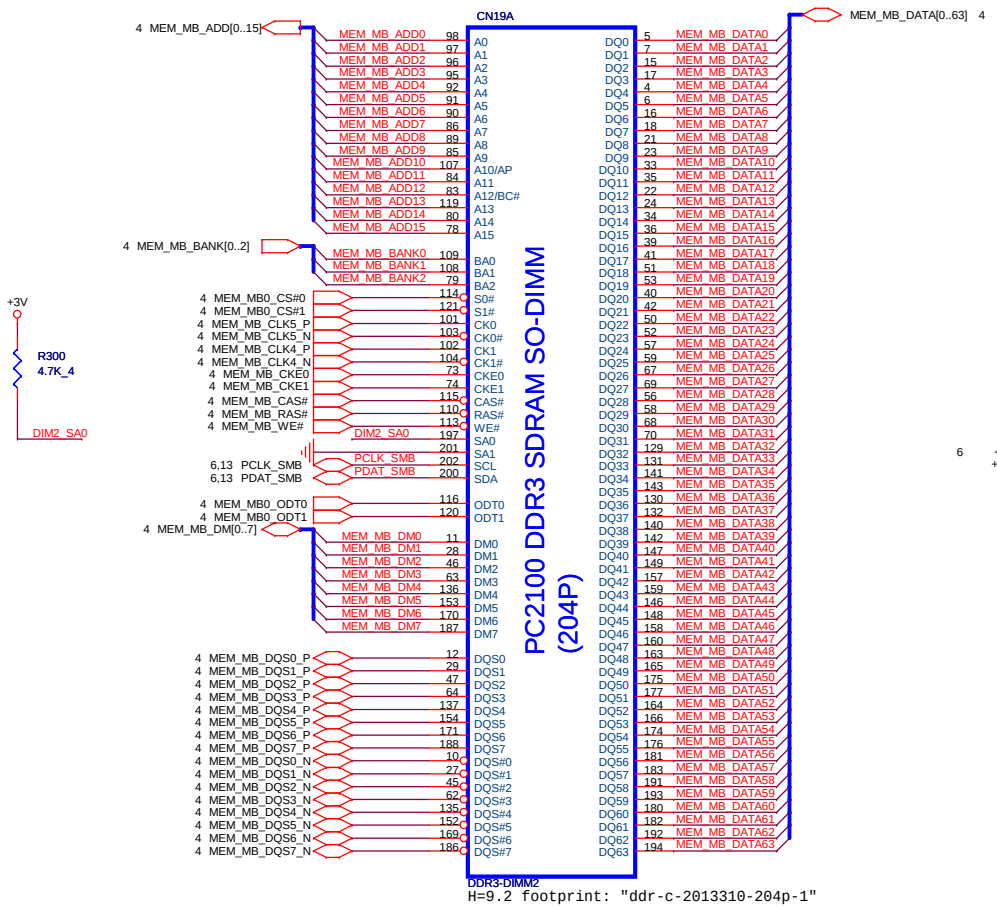


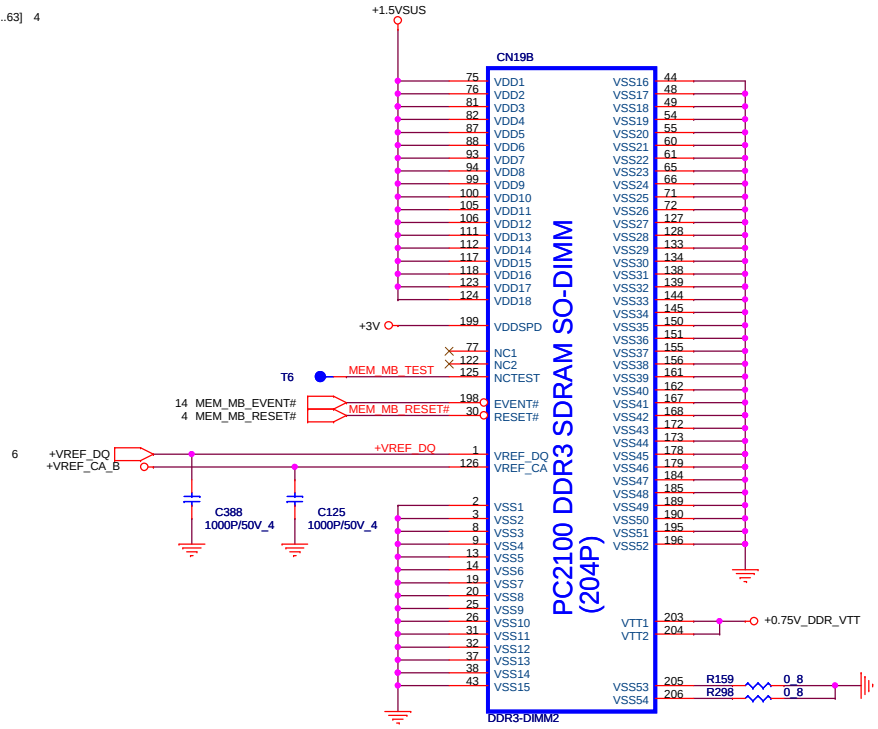
PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SODIMMS: A/B CHANNEL	1A

NB5/RD2

Date: Wednesday, September 15, 2010 Sheet 6 of 43



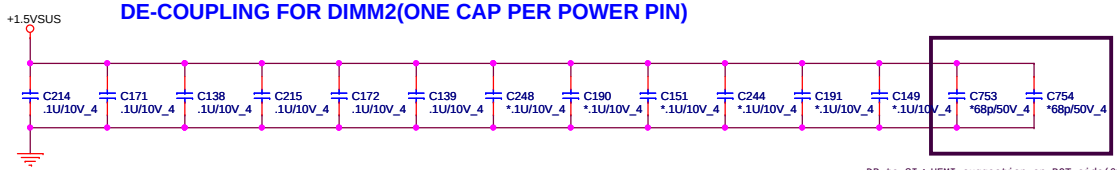


SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

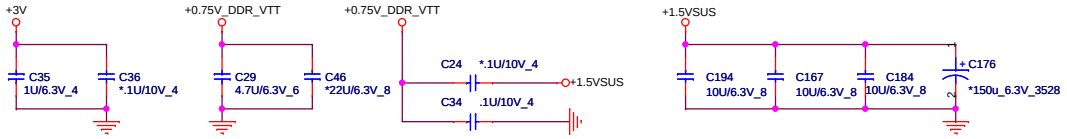
No Vias Between the Trace of PIN to CAP.

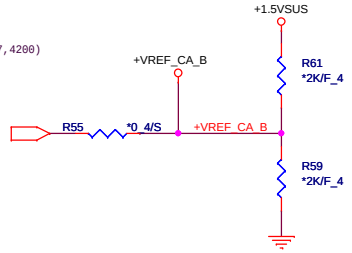
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)



DB to SI : UEMI suggestion on BOT side(6847,5047)(6847,4200)

DE-COUPLING FOR DIMM2





PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 SODIMMS TERMINATIONS	1A

NB5/RD2

Date: Wednesday, September 15, 2010 Sheet 7 of 43

HT_CPU_NB_CAD_H[15..0] — HT_CPU_NB_CAD_H[15..0] 3
HT_CPU_NB_CAD_L[15..0] — HT_CPU_NB_CAD_L[15..0] 3
HT_CPU_NB_CLK_H[1..0] — HT_CPU_NB_CLK_H[1..0] 3
HT_CPU_NB_CLK_L[1..0] — HT_CPU_NB_CLK_L[1..0] 3
HT_CPU_NB_CTL_H[1..0] — HT_CPU_NB_CTL_H[1..0] 3
HT_CPU_NB_CTL_L[1..0] — HT_CPU_NB_CTL_L[1..0] 3
HT_NB_CPU_CAD_H[15..0] — HT_NB_CPU_CAD_H[15..0] 3
HT_NB_CPU_CAD_L[15..0] — HT_NB_CPU_CAD_L[15..0] 3
HT_NB_CPU_CLK_H[1..0] — HT_NB_CPU_CLK_H[1..0] 3
HT_NB_CPU_CLK_L[1..0] — HT_NB_CPU_CLK_L[1..0] 3
HT_NB_CPU_CTL_H[1..0] — HT_NB_CPU_CTL_H[1..0] 3
HT_NB_CPU_CTL_L[1..0] — HT_NB_CPU_CTL_L[1..0] 3

U20A

HYPER TRANSPORT CPU I/F — PART 1 OF 6

HT_CPU_NB_CAD_H0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_NB_CPU_CAD_H0
HT_CPU_NB_CAD_L0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_NB_CPU_CAD_L0
HT_CPU_NB_CAD_H1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_NB_CPU_CAD_H1
HT_CPU_NB_CAD_L1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_NB_CPU_CAD_L1
HT_CPU_NB_CAD_H2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_NB_CPU_CAD_H2
HT_CPU_NB_CAD_L2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_NB_CPU_CAD_L2
HT_CPU_NB_CAD_H3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_NB_CPU_CAD_H3
HT_CPU_NB_CAD_L3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_NB_CPU_CAD_L3
HT_CPU_NB_CAD_H4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_NB_CPU_CAD_H4
HT_CPU_NB_CAD_L4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_NB_CPU_CAD_L4
HT_CPU_NB_CAD_H5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_NB_CPU_CAD_H5
HT_CPU_NB_CAD_L5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_NB_CPU_CAD_L5
HT_CPU_NB_CAD_H6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_NB_CPU_CAD_H6
HT_CPU_NB_CAD_L6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_NB_CPU_CAD_L6
HT_CPU_NB_CAD_H7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_NB_CPU_CAD_H7
HT_CPU_NB_CAD_L7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_NB_CPU_CAD_L7
HT_CPU_NB_CAD_H8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_NB_CPU_CAD_H8
HT_CPU_NB_CAD_L8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_NB_CPU_CAD_L8
HT_CPU_NB_CAD_H9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_NB_CPU_CAD_H9
HT_CPU_NB_CAD_L9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_NB_CPU_CAD_L9
HT_CPU_NB_CAD_H10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_NB_CPU_CAD_H10
HT_CPU_NB_CAD_L10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_NB_CPU_CAD_L10
HT_CPU_NB_CAD_H11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_NB_CPU_CAD_H11
HT_CPU_NB_CAD_L11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_NB_CPU_CAD_L11
HT_CPU_NB_CAD_H12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_NB_CPU_CAD_H12
HT_CPU_NB_CAD_L12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_NB_CPU_CAD_L12
HT_CPU_NB_CAD_H13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_NB_CPU_CAD_H13
HT_CPU_NB_CAD_L13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_NB_CPU_CAD_L13
HT_CPU_NB_CAD_H14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_NB_CPU_CAD_H14
HT_CPU_NB_CAD_L14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_NB_CPU_CAD_L14
HT_CPU_NB_CAD_H15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_NB_CPU_CAD_H15
HT_CPU_NB_CAD_L15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_NB_CPU_CAD_L15
HT_CPU_NB_CLK_H0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_NB_CPU_CLK_H0
HT_CPU_NB_CLK_L0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_NB_CPU_CLK_L0
HT_CPU_NB_CLK_H1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_NB_CPU_CLK_H1
HT_CPU_NB_CLK_L1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_NB_CPU_CLK_L1
HT_CPU_NB_CTL_H0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_NB_CPU_CTL_H0
HT_CPU_NB_CTL_L0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_NB_CPU_CTL_L0
HT_CPU_NB_CTL_H1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_NB_CPU_CTL_H1
HT_CPU_NB_CTL_L1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_NB_CPU_CTL_L1
	C23	HT_RXCALP	HT_TXCALP	B24	HT_TXCALP R359 301/F_4
R358 301/F_4 HT_RXCALN	A24	HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

RS880

signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

U17

SPM_VREF1	M9	VREFCA	DQL0	E4	SPM_DQ2
SPM_VREF2	H2	VREFDQ	DQL1	F8	SPM_DQ1
			DQL2	F3	SPM_DQ5
SPM_A0	N4	A0	DQL3	F9	SPM_DQ3
SPM_A1	P8	A1	DQL4	H4	SPM_DQ7
SPM_A2	P4	A2	DQL5	H9	SPM_DQ0
SPM_A3	N3	A3	DQL6	G3	SPM_DQ4
SPM_A4	P9	A4	DQL7	H8	SPM_DQ6
SPM_A5	P3	A5			
SPM_A6	R9	A6			
SPM_A7	R3	A7	DQU0	D8	SPM_DQ13
SPM_A8	T9	A8	DQU1	C4	SPM_DQ8
SPM_A9	R4	A9	DQU2	C9	SPM_DQ10
SPM_A10	L8	A10/AP	DQU3	C3	SPM_DQ12
SPM_A11	R8	A11	DQU4	A8	SPM_DQ15
SPM_A12	N8	A12/BC	DQU5	A3	SPM_DQ11
SPM_A13	T4	A13	DQU6	B9	SPM_DQ14
	T8	A14	DQU7	A4	SPM_DQ9
	M8	A15			
SPM_BA0	M3	BA0	VDD#B3	B3	+1.5V_MEM_VDDQ
SPM_BA1	N9	BA1	VDD#D10	D10	
SPM_BA2	M4	BA2	VDD#G8	G8	
			VDD#K3	K3	
			VDD#K9	K9	
			VDD#N2	N2	
SPM_CLKP	J8	CK	VDD#N10	N10	
R58 *100_4 SPM_CLKN	K8	CK	VDD#R2	R2	
SPM_CKE	K10	CKE	VDD#R10	R10	+1.5V_MEM_VDDQ
SPM_ODT	K2	ODT	VDDQ#A2	A2	
SPM_CS#	L3	CS	VDDQ#A9	A9	
SPM_RAS#	J4	RAS	VDDQ#C2	C2	
SPM_CAS#	K4	CAS	VDDQ#C10	C10	
SPM_WE#	L4	WE	VDDQ#D3	D3	
			VDDQ#E10	E10	
SPM_DQS0P	F4	DQSL	VDDQ#F2	F2	
SPM_DQS1P	C8	DQSU	VDDQ#H3	H3	
			VDDQ#H10	H10	
SPM_DM0	E8	DML	VSS#A10	A10	
SPM_DM1	D4	DMU	VSS#B4	B4	
			VSS#E2	E2	
			VSS#G9	G9	
SPM_DQS0N	G4	DQSL	VSS#J3	J3	
SPM_DQS1N	B8	DQSU	VSS#J9	J9	
			VSS#M2	M2	
+1.5V_MEM_VDDQ			VSS#M10	M10	
R305 *10K/F_4			VSS#P2	P2	
13 SP_DDR3_RST#	T3	RESET	VSS#P10	P10	
VMA_ZQ2	L9	ZQ	VSS#T2	T2	
			VSS#T10	T10	
			VSSQ#B2	B2	
			VSSQ#B10	B10	
			VSSQ#D2	D2	
			VSSQ#D9	D9	
			VSSQ#E3	E3	
			VSSQ#E9	E9	
			VSSQ#F10	F10	
			VSSQ#G2	G2	
			VSSQ#G10	G10	
R56 *243/F_4					
	J2	NC#J2			
	L2	NC#L2			
	J10	NC#J10			
	L10	NC#L10			

100-BALL SDRAM DDR3
*H5TQ1G63AFR-14C

This block is for UMA only , DIS can remove all component

U20D

SBD_MEM/DVO_I/F — PAR 4 OF 6

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22	SPM_DQ10
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18	SPM_DQ11
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22	SPM_DQ13
T16			MEM_DQ14/DVO_D10(NC)	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)			
SPM_BA2	AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17	SPM_DQS0P
			MEM_DQS0N/DVO_IDCKN(NC)	W18	SPM_DQS0N
SPM_RAS#	W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20	SPM_DQS1P
SPM_CAS#	Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21	SPM_DQS1N
SPM_WE#	AD18	MEM_WEb(NC)			
SPM_CS#	AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17	SPM_DM0
SPM_CKE	AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19	SPM_DM1
SPM_ODT	V14	MEM_ODT(NC)			
			IOPLLVDD18(NC)	AE23	+1.8V_IOPLLVDD18
SPM_CLKP	V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24	+1.1V_IOPLLVDD
SPM_CLKN	W14	MEM_CKN(NC)			
			IOPLLVSS(NC)	AD23	
R324 *40.2/F_4 SPM_COMPP	AE12	MEM_COMPP(NC)		AE18	SPM_VREF
R320 *40.2/F_4 SPM_COMPN	AD12	MEM_COMPN(NC)	MEM_VREF(NC)		

+1.5V_MEM_VDDQ
RS880

40mils wdith or more

+1.5V_MEM_VDDQ
C93 *0.1U/10V_4
C85 *10U/6.3V_8
C78 *10U/6.3V_8
R307 *0_6
C91 *0.1U/10V_4
C99 *0.1U/10V_4
C94 *0.1U/10V_4
+1.5V

*PBY160808T-221Y-N L52 +1.8V
*PBY160808T-221Y-N L14 +1.1V
C574 *2.2U/6.3V_6
C154 *2.2U/6.3V_6

R322 *1K/F_4
R323 *1K/F_4
C564 *0.1U/10V_4
C563 *0.1U/10V_4
+1.5V_MEM_VDDQ

SPM_VREF1
R46 *1K/F_4
R48 *1K/F_4
C92 *0.1U/10V_4
C87 *0.1U/10V_4
+1.5V_MEM_VDDQ

SPM_VREF2
R62 *1K/F_4
R63 *1K/F_4
C132 *0.1U/10V_4
C147 *0.1U/10V_4
+1.5V_MEM_VDDQ

PROJECT : R22
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	RS880-HT LINK I/F 1/5	1A

Date: Wednesday, September 15, 2010 Sheet 8 of 43

GFX_RX can remove
at next stage for MUXLESS

UMA can remove all GFX_TX CAP

To HDMI CONN

U20B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS880

TO WLAN

TO PCIE-LAN

TO PCIE CARD READER

RS880 Display Port Support (muxed on GFX)

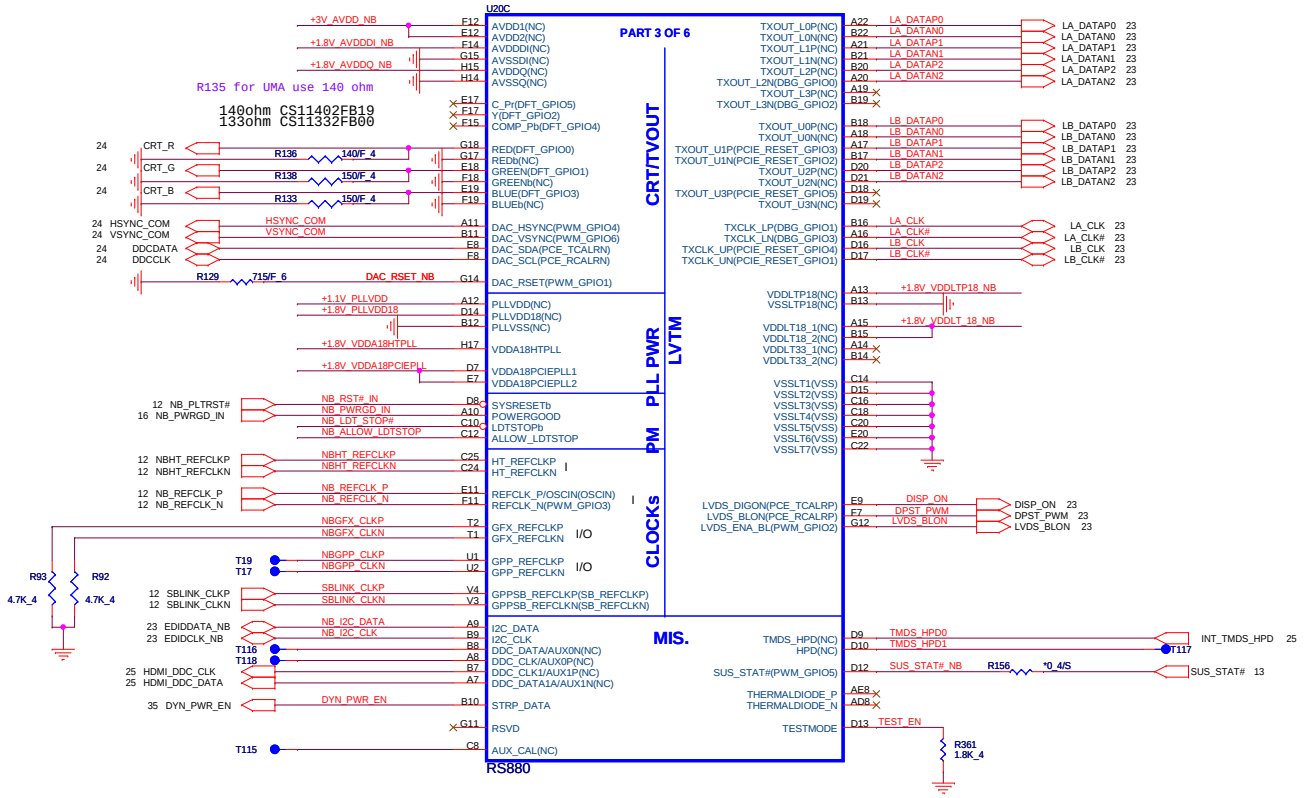
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NB5/RD2

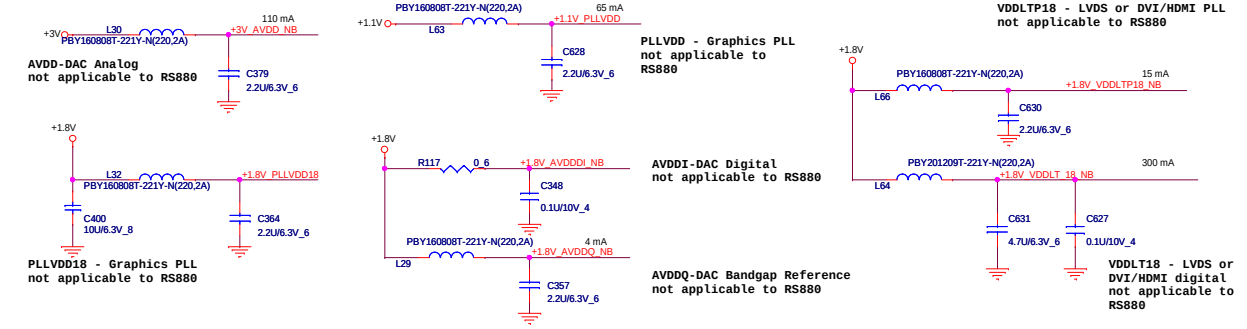
PROJECT : R22
Quanta Computer Inc.

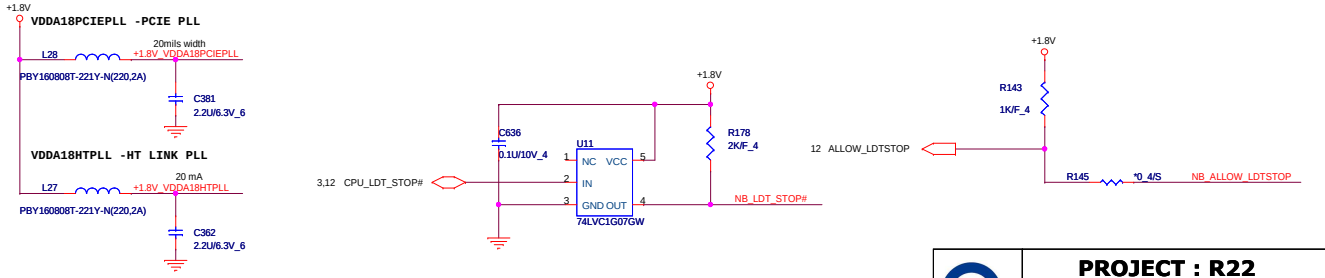
Size	Document Number	Rev
Custom	RS880-PCIE I/F 2/5	1A

Date: Wednesday, September 15, 2010 Sheet 9 of 43



MUXLESS need add PLL power for LVDS





STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M
1 Disable
0 Enable

RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

For external EEPROM Debug only

RS780/RX780

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS880-SYSTEM I/F 3/5	1A

N85/RD2

Date: Wednesday, September 15, 2010 | Sheet 10 of 43

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

U20F — PART 6/6 — GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

VDDHT - HT LINK digital I/O for RX780/RS780

+1.1V — 0.6A — L49 *0_8/S — +1.1V_VDDHT

C551 4.7U/6.3V_6 | C278 0.1U/10V_4 | C329 0.1U/10V_4 | C293 0.1U/10V_4

+1.1V 2A for RS880M

VDDHTRX - HT LINK RX I/O for RX780/RS780

0.7A — L65 *0_8/S — +1.1V_VDDHTRX

C632 4.7U/6.3V_8 | C350 0.1U/10V_4 | C345 0.1U/10V_4 | C629 0.1U/10V_4

VDDHTTX - HT LINK TX I/O for RS880

RS880 — +1.1V — L9 *0_8/S — 0.5A — +1.1V_VDDHTTX

C196 4.7U/6.3V_6 | C228 0.1U/10V_4 | C241 0.1U/10V_4 | C260 0.1U/10V_4 | C219 0.1U/10V_4

+1.1V 2A for RS880M

+1.8V 1A for RS780M+SB700

+1.8V — 700mA — L16 PBY201209T-221Y-N(220,2A) — +1.8V_VDDA18PCIE

C213 4.7U/6.3V_6 | C204 4.7U/6.3V_6 | C267 0.1U/10V_4 | C238 0.1U/10V_4 | C281 0.1U/10V_4 | C255 0.1U/10V_4

VDDA18PCIE - PCIE TX stage I/O for RX780/RS780

VDD18 - RS780 I/O transform

+1.8V — R141 *0_6/S — 25mA — C328 1U/10V_4 — +1.8V_VDDG18_NB

+1.8V — R321 *0_6/S — 25mA — C558 1U/10V_4 — +1.8V_VDD18_MEM

VDD18_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

U20E — PART 5/6 — POWER — RS880

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15

VDDG18_1(VDDH18_1) VDDG18_2(VDDH18_2) VDD18_MEM1(NC) VDD18_MEM2(NC)

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC)

VDDG33_1(NC) VDDG33_2(NC)

VDDPCIE - PCIE-E Main power

+1.1V_VDD_PCIE — 2.5A — R146 *0_8/S — +1.1V

C315 0.1U/10V_4 | C370 0.1U/10V_4 | C336 1U/10V_4 | C359 1U/10V_4 | C378 4.7U/6.3V_6

VDDC - Core Logic power

7A — +1.1V_DYN

C264 560P/50V | C304 0.1U/10V_4 | C314 0.1U/10V_4 | C317 0.1U/10V_4 | C545 10U/6.3V_8 | C544 0.1U/10V_4 | C542 0.1U/10V_4

C296 0.1U/10V_4 | C290 0.1U/10V_4 | C265 560P/50V | C546 10U/6.3V_8 | C543 560P/50V

VDD_MEM For UMA RS780 only Not applicable to RX780 memory I/O transform

+1.5V_VDD_MEM — L53 *0_8 — +1.5V

C225 *0.1U/10V_4 | C206 *0.1U/10V_4 | C205 *0.1U/10V_4 | C222 0_4 | C220 *4.7U/6.3V_6

+3V_VDDG33 — RS780 — R142 *0_6/S — 3.3V(0.06A) — +3V

C366 0.1U/10V_4 | C360 0.1U/10V_4

VDD33 - 3.3V I/O Not applicable to RX780

This is side port power DIS remove L55 , change C205 to 0 ohm and short to GND

NB5/RD2	PROJECT : R22 Quanta Computer Inc.	
Size: Custom	Document Number: RS880-POWER5/5	Rev: 1A
Date: Wednesday, September 15, 2010	Sheet 11 of 43	

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB

SB800 Part 1 of 5

All the PCI bus has build-in Pull-UP/Down resistors

All RP resistor need within 0.5"of SB

DB to SI Change C673,C675 to 33P

DB to SI CN27 Change PN
PN : DFWF02MS022
Footprint : 50273-0027N-001-2P-L

EMI suggestion

Support BACO, remove R465 and U6508 , add R6601

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB820M A12

PROJECT : R22
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	SB820-PCIE/PCI/CPU/LPC 1/4	1A

Date: Wednesday, September 15, 2010 Sheet 12 of 43

NC,no install by default

+3VS5 R245 *2.2K_4 SB_TEST0
R417 *2.2K_4 SB_TEST1
R239 *2.2K_4 SB_TEST2

remove pull hi
(chip internal
have pull hi)

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R412 2.2K_4 SB_SMBCLK1
R411 2.2K_4 SB_SMBDATA1

30,33 PCIE_WAKE#

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R282 2.2K_4 PCLK_SMB
R281 2.2K_4 PDAT_SMB

Clock gen/Robson/TV
tuner
/DDR2/DDR2
thermal/Accelerometer

C477 100P/50V_4

Pure UMA can
remove D25

+3V R430 10K/F_4
RB501V-40 D25
37 VGA_REQ

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R286 2.2K_4 SB_SCLK2
R284 2.2K_4 SB_SDATA2
R408 *10K_4 SYS_RST#

+3VS5 R413 2.2K_4 DNBSWON#

+3V R414 4.7K_4 SUS_STAT#
R431 8.2K_4 WLAN_CLKREQ#
R272 8.2K_4 LAN_CLKREQ#

To Azalia

ACZ_SDOUT R240 33_4 ACZ_SDOUT_AUDIO 27
C461 *10P/50V_4
ACZ_SYNC R244 33_4 ACZ_SYNC_AUDIO 27
C467 *10P/50V_4
BIT_CLK_AUDIO 27
ACZ_BCLK R247 33_4 C463 27P/50V_4
ACZ_RST# R241 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27

EMI suggestion

U28D

14 MEM_GEVEN#
T122 RI#
T68 SPI_CS3#
32 SUSB# SUSB#
32 SUSC# SUSC#
32 DNBSWON# SB_PWRGD_IN
16 SB_PWRGD_IN SUS_STAT#
10 SUS_STAT# SB_TEST0
T71 SB_TEST1
SB_TEST2
32 GATEA20 GATEA20
32 RCIN# RCIN#
32 KBSMI#
32 SCI# SCI#
SYS_RST#
3 CPU_THERMTRIP#
16 WD_PWRGD WD_PWRGD
32 RSMRST# RSMRST#
26 CARD_CLKREQ#
30 LAN_CLKREQ#
30,32 LAN_DISABLE# R404 *0_4 LAN_DISABLE#_SB
T104
T101
27 ACZ_SPKR ACZ_SPKR
6,7 PCLK_SMB PCLK_SMB
6,7 PDAT_SMB PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
33 WLAN_CLKREQ# VGA_REQ_R
T121
T129
8 SP_DDR3_RST#
T65
T73
T74
T70
T105 EXT_SB_OSC

For Zero ODD

5 PM_THERM# R238 *0_4 SMBALERT#_1
31 ODD_DA#_FCH
31 ODD_PLUGIN#
T81 SB_JTAG_TCK
T76 SB_JTAG_TDI
T80 SB_JTAG_RST#

HD audio
interface is
3.3S5 voltage

R248 *10K/F_4
16 ACZ_SDOUT
R392 *10K/F_4 ACZ_SDIN0
R394 *10K/F_4 ACZ_SDIN1
R393 *10K/F_4 ACZ_SDIN2_R
R395 *10K/F_4 ACZ_SDIN3_R
ACZ_SYNC
ACZ_RST#

R398 10K/F_4
R390 10K/F_4
+3VS5
R235 10K/F_4
R246 10K/F_4
R257 10K/F_4

T103
T131
T133

SB800
Part 4 of 5

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN

GPIO
USB 2.0

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#

USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#

HD AUDIO

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR

GBE LAN

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

EMBEDDED CTRL

SB820M A12

USBCLK/14M_25M_48M_OSC A10 CLK_48M_USB
USB_RCOMP G19 USB_RCOMP_SB R270 11.8K/F_6

USB_FSD1P/GPIO186 J10 USBP15+ 29
USB_FSD1N H11 USBP15- 29 BLUETOOTH
USB_FSD0P/GPIO185 H9 T79
USB_FSD0N J8 T84

USB_HSD13P B12 T85
USB_HSD13N A12 T78
USB_HSD12P F11 T88
USB_HSD12N E11 T89
USB_HSD11P E14 T95
USB_HSD11N E12 T92
USB_HSD10P J12 USBP10+ 33
USB_HSD10N J14 USBP10- 33 WLAN Min-Card
USB_HSD9P A13 T87
USB_HSD9N B13 T77
USB_HSD8P D13 T97
USB_HSD8N C13 T91
USB_HSD7P G12 T94
USB_HSD7N G14 T96
USB_HSD6P G16 USBP6+ 29
USB_HSD6N G18 USBP6- 29 USB Connector
USB_HSD5P D16 USBP5+ 29
USB_HSD5N C16 USBP5- 29 USB Connector
USB_HSD4P B14 T126
USB_HSD4N A14 T128
USB_HSD3P E18 T102
USB_HSD3N E16 T99
USB_HSD2P J16 USBP2+ 23
USB_HSD2N J18 USBP2- 23 Carama USB
USB_HSD1P B17 T98
USB_HSD1N A17 T127
USB_HSD0P A16 USBP0+ 29
USB_HSD0N B16 USBP0- 29 USB Connector

CLK_48M_USB
C485 *2.2P/50V_4
for EMI

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_SCLK3 T130
SDA3_LV/GPIO196 E26 T132
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 SB_GPIO199 SB_GPIO199 16
EC_PWM3/EC_TIMER3/GPIO200 F21 SB_GPIO200 SB_GPIO200 16 SPI/LPC define

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

EMBEDDED CTRL

NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	1A

Date: Wednesday, September 15, 2010 Sheet 13 of 43

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SATA1

SATA ODD

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

NOTE :
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

U28B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB820M A12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

Side port ID H/W setting

For Zero ODD

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

Item	Board ID Hardware setting
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

U26 TC7SH08FU

Q22 *MMBT3904

Q21 *MMBT3904

PROJECT : R22
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	1A

Date: Wednesday, September 15, 2010 Sheet 14 of 43

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power

SB800 Part 3 of 5

U28C

+3.3V_SB_R

VDDQ--3.3V I/O power 131mA

+3V R236 *0_8/S

C460 22U/6.3V_8 C472 0.1U/10V_4 C474 0.1U/10V_4 C497 0.1U/10V_4

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power 71mA

R288 *0_8/S VDDIO_18_FC

Delete Cap and change +1.8V to pull low from AMD command , due to no IDE & flash mode

POWER

+3V L71 0_6

C713 2.2U/6.3V_4 C708 *0.1U/10V_4 VDDPL_3.3V_PCIE 43mA

+1.1V_PCIE_VDDR

PCIE_VDDR--PCIE I/O power 600mA

+1.1V L72 0_6

C715 10U/6.3V_8 C717 1U/10V_4 C710 10U/6.3V_8 C516 0.1U/10V_4 C510 0.1U/10V_4

+3V L41 VDDPL_3.3V_SATA 93mA

PBY160808T-221Y-N(220,2A)

C489 2.2U/6.3V_4 C488 *0.1U/10V_4

+1.1V_AVDD_SATA

AVDD_SATA--SATA phy power 567mA

+1.1V L45

BLM18PG181SN1D(180,1.5A)_6

C514 22U/6.3V_8 C502 0.1U/10V_4 C504 0.1U/10V_4 C495 1U/10V_4 C494 1U/10V_4

For support USB wakeup-->3V_S5

+3V_AVDD_USB

AVDDTX--USB Phy Analog I/O power 658mA

+3VS5 L69

PBY160808T-221Y-N(220,2A)

C687 10U/6.3V_8 C690 10U/6.3V_8 C688 1U/10V_4 C686 1U/10V_4

+1.1VS5 L40 VDDAN_1.1V_USB TBDmA

PBY160808T-221Y-N(220,2A)

C482 2.2U/6.3V_4 C483 0.1U/10V_4

SB820M A12

CORE S0: VDDCR_11_1 N13, VDDCR_11_2 R15, VDDCR_11_3 N17, VDDCR_11_4 U13, VDDCR_11_5 U17, VDDCR_11_6 V12, VDDCR_11_7 V18, VDDCR_11_8 W12, VDDCR_11_9 W18 — 510mA

+1.1V_VCC_SB_R R265 *0_8/S +1.1V

C491 0.1U/10V_4 C490 0.1U/10V_4 C487 1U/10V_4 C484 1U/10V_4 C486 10U/6.3V_8

CKVDD_1.1V--Internal clock Generator I/O power

+1.1V_CKVDD

CLKGEN I/O: VDDAN_11_CLK_1 K28, VDDAN_11_CLK_2 K29, VDDAN_11_CLK_3 J28, VDDAN_11_CLK_4 K26, VDDAN_11_CLK_5 J21, VDDAN_11_CLK_6 J20, VDDAN_11_CLK_7 K21, VDDAN_11_CLK_8 J22 — TBDmA

BLM18PG181SN1D(180,1.5A)_6 L48 +1.1V

C505 1U/10V_4 C507 1U/10V_4 C512 0.1U/10V_4 C498 0.1U/10V_4 C530 22U/6.3V_8

GBE LAN: VDDRF_GBE_S V1, VDDIO_33_GBE_S M10, VDDCR_11_GBE_S_1 L7, VDDCR_11_GBE_S_2 L9, VDDIO_GBE_S_1 M6, VDDIO_GBE_S_2 P8

PCI EXPRESS: VDDPL_33_PCIE, VDDAN_11_PCIE_1 U26, VDDAN_11_PCIE_2 V22, VDDAN_11_PCIE_3 V26, VDDAN_11_PCIE_4 V27, VDDAN_11_PCIE_5 V28, VDDAN_11_PCIE_6 V29, VDDAN_11_PCIE_7 W22, VDDAN_11_PCIE_8 W26

SERIAL ATA: VDDPL_33_SATA, VDDAN_11_SATA_1 AJ20, VDDAN_11_SATA_4 AF18, VDDAN_11_SATA_2 AH20, VDDAN_11_SATA_3 AG19, VDDAN_11_SATA_5 AE18, VDDAN_11_SATA_6 AD18, VDDAN_11_SATA_7 AE16

3.3V_S5 I/O: VDDIO_33_S_1 A21, VDDIO_33_S_2 D21, VDDIO_33_S_3 B21, VDDIO_33_S_4 K10, VDDIO_33_S_5 L10, VDDIO_33_S_6 J9, VDDIO_33_S_7 T6, VDDIO_33_S_8 T8 — 32mA

+3VALW_R C692 *0.1U/10V_4 C696 2.2U/6.3V_6 C695 2.2U/6.3V_6 R433 *0_6/S +3VS5

S5_3.3--3.3v standby power

CORE S5: VDDCR_11_S_1 F26, VDDCR_11_S_2 G26 — 113mA

VDDCR_1.1V R280 *0_6/S +1.1VS5

C506 1U/10V_4 C515 1U/10V_4

VDDIO_AZ_S M8 +3VS5 TBDmA

VDDCR_1.1V_USB VDDCR_11_USB_S_1 A11, VDDCR_11_USB_S_2 B11

S5_1.1V--1.1V standby power

USB I/O: VDDAN_33_USB_S_1 A18, VDDAN_33_USB_S_2 A19, VDDAN_33_USB_S_3 A20, VDDAN_33_USB_S_4 B18, VDDAN_33_USB_S_5 B19, VDDAN_33_USB_S_6 B20, VDDAN_33_USB_S_7 C18, VDDAN_33_USB_S_8 C20, VDDAN_33_USB_S_9 D18, VDDAN_33_USB_S_10 D19, VDDAN_33_USB_S_11 D20, VDDAN_33_USB_S_12 E19

PLL: VDDPL_33_SYS M21 +VDDPL_3.3V 47mA, VDDPL_11_SYS_S L22 +VDDPL_1.1V 62mA, VDDPL_33_USB_S F19 +3VS5 17mA, VDDAN_33_HWM_S D6 +VDDAN_3.3VHWM 5mA

197mA

PBY160808T-221Y-N(220,2A) L68 +1.1VS5

C684 10U/6.3V_8 C682 0.1U/10V_4 C683 0.1U/10V_4

VDDXL_33_S L20 VDDXL_3.3V 32mA

PBY160808T-221Y-N(220,2A) L43 +3V

C500 *0.1U/10V_4 C496 2.2U/6.3V_6

VDDAN_11_USB_S_1 C11, VDDAN_11_USB_S_2 D11

U28E

SB800

GROUND

VSSIO_SATA_1 Y14, VSSIO_SATA_2 Y16, VSSIO_SATA_3 AB16, VSSIO_SATA_4 AC14, VSSIO_SATA_5 AE12, VSSIO_SATA_6 AE14, VSSIO_SATA_7 AF9, VSSIO_SATA_8 AF11, VSSIO_SATA_9 AF13, VSSIO_SATA_10 AF16, VSSIO_SATA_11 AG8, VSSIO_SATA_12 AH7, VSSIO_SATA_13 AH11, VSSIO_SATA_14 AH13, VSSIO_SATA_15 AH16, VSSIO_SATA_16 AJ7, VSSIO_SATA_17 AJ11, VSSIO_SATA_18 AJ13, VSSIO_SATA_19 AJ16

VSSIO_USB_1 A9, VSSIO_USB_2 B10, VSSIO_USB_3 K11, VSSIO_USB_4 B9, VSSIO_USB_5 D10, VSSIO_USB_6 D12, VSSIO_USB_7 D14, VSSIO_USB_8 D17, VSSIO_USB_9 E9, VSSIO_USB_10 F9, VSSIO_USB_11 F12, VSSIO_USB_12 F14, VSSIO_USB_13 F16, VSSIO_USB_14 C9, VSSIO_USB_15 G11, VSSIO_USB_16 F18, VSSIO_USB_17 D9, VSSIO_USB_18 H12, VSSIO_USB_19 H14, VSSIO_USB_20 H16, VSSIO_USB_21 H18, VSSIO_USB_22 J11, VSSIO_USB_23 J19, VSSIO_USB_24 K12, VSSIO_USB_25 K14, VSSIO_USB_26 K16, VSSIO_USB_27 K18, VSSIO_USB_28 H19

EFUSE Y4

VSSAN_HWM D8

VSSXL M19

VSSPL_SYS M20

VSSIO_PCIECLK_1 P21, VSSIO_PCIECLK_2 P20, VSSIO_PCIECLK_3 M22, VSSIO_PCIECLK_4 M24, VSSIO_PCIECLK_5 M26, VSSIO_PCIECLK_6 P22, VSSIO_PCIECLK_7 P24, VSSIO_PCIECLK_8 P26, VSSIO_PCIECLK_9 T20, VSSIO_PCIECLK_10 T22, VSSIO_PCIECLK_11 T24, VSSIO_PCIECLK_12 V20, VSSIO_PCIECLK_13 J23, VSSIO_PCIECLK_14 H23, VSSIO_PCIECLK_15 H26, VSSIO_PCIECLK_16 AA21, VSSIO_PCIECLK_17 AA23, VSSIO_PCIECLK_18 AB23, VSSIO_PCIECLK_19 AD23, VSSIO_PCIECLK_20 AA26, VSSIO_PCIECLK_21 AC26, VSSIO_PCIECLK_22 Y20, VSSIO_PCIECLK_23 W21, VSSIO_PCIECLK_24 W20, VSSIO_PCIECLK_25 AE26, VSSIO_PCIECLK_26 L21, VSSIO_PCIECLK_27 K20

VSS_1 AJ2, VSS_2 A28, VSS_3 A2, VSS_4 E5, VSS_5 D23, VSS_6 E25, VSS_7 E6, VSS_8 F24, VSS_9 N15, VSS_10 R13, VSS_11 R17, VSS_12 T10, VSS_13 P10, VSS_14 V11, VSS_15 U15, VSS_16 M18, VSS_17 V19, VSS_18 M11, VSS_19 L12, VSS_20 L18, VSS_21 J7, VSS_22 P3, VSS_23 V4, VSS_24 AD6, VSS_25 AD4, VSS_26 AB7, VSS_27 AC9, VSS_28 V8, VSS_29 W9, VSS_30 W10, VSS_31 AJ28, VSS_32 B29, VSS_33 U4, VSS_34 Y18, VSS_35 Y10, VSS_36 Y12, VSS_37 Y11, VSS_38 AA11, VSS_39 AA12, VSS_40 G4, VSS_41 J4, VSS_42 G8, VSS_43 G9, VSS_44 M12, VSS_45 AF25, VSS_46 H7, VSS_47 AH29, VSS_48 V10, VSS_49 P6, VSS_50 N4, VSS_51 L4, VSS_52 L8

Part 5 of 5

SB820M A12

+3VS5 C475 2.2U/6.3V_6

Close to pin M8

+3V +VDDPL_3.3V L47 PBY160808T-221Y-N(220,2A) C517 2.2U/6.3V_6 C503 *0.1U/10V_4

+3VS5 +VDDAN_3.3VHWM L39 *0_6/S C478 0.1U/10V_4

+1.1V +VDDPL_1.1V L46 PBY160808T-221Y-N(220,2A) C519 2.2U/6.3V_6 C511 *0.1U/10V_4

+3VS5 C679 2.2U/6.3V_6 C513 0.1U/10V_4

Close to pin F19

NB5/RD2

PROJECT : R22
Quanta Computer Inc.

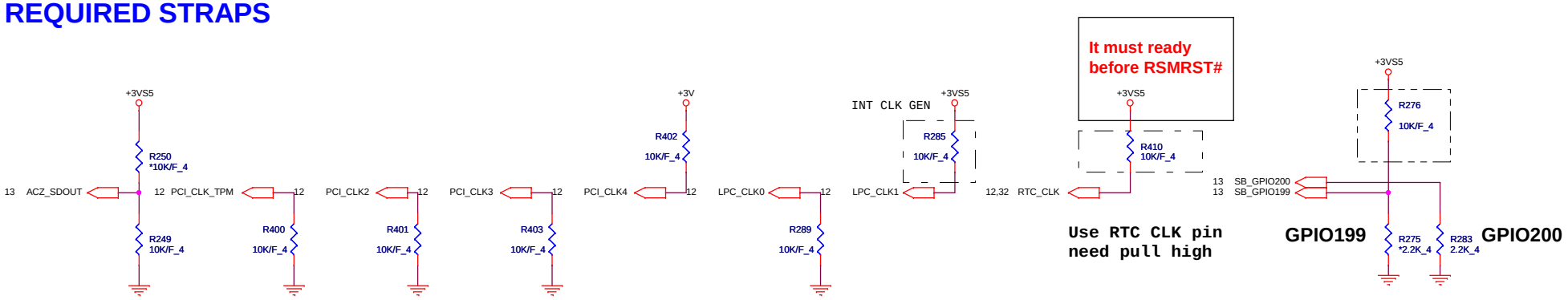
Size	Document Number	Rev
Custom	SB820-PWR/DECOUPLING 4/4	1A

Date: Wednesday, September 15, 2010 Sheet 15 of 43

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull Hi 10K , confirm AMD ward this pull Hi not need

REQUIRED STRAPS



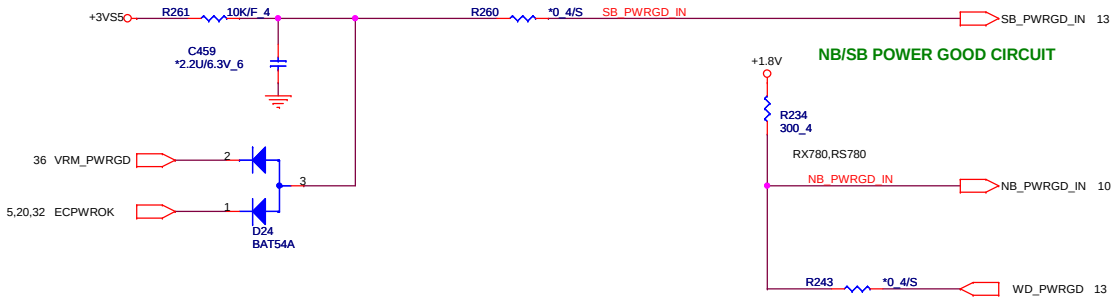
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

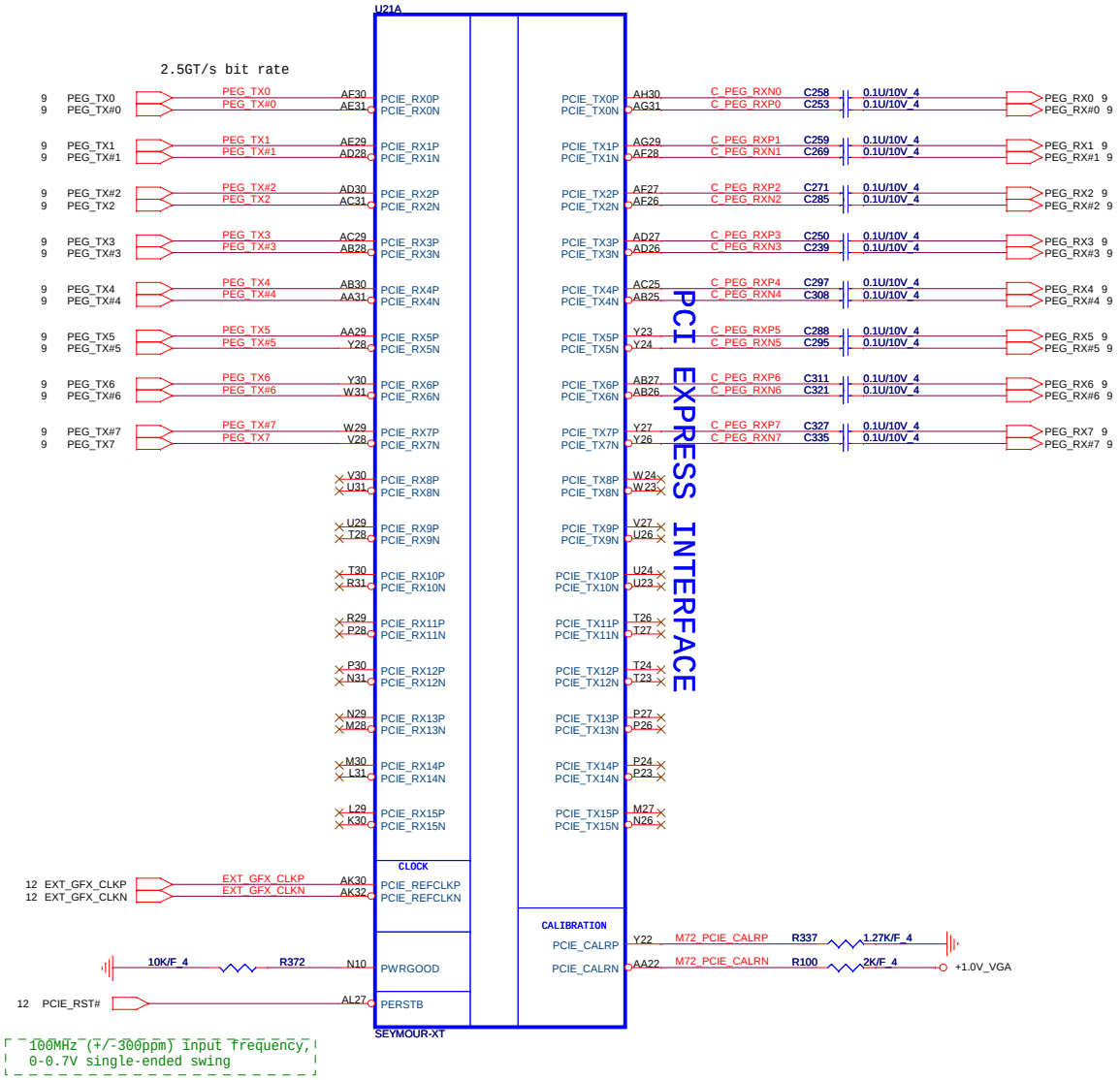
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

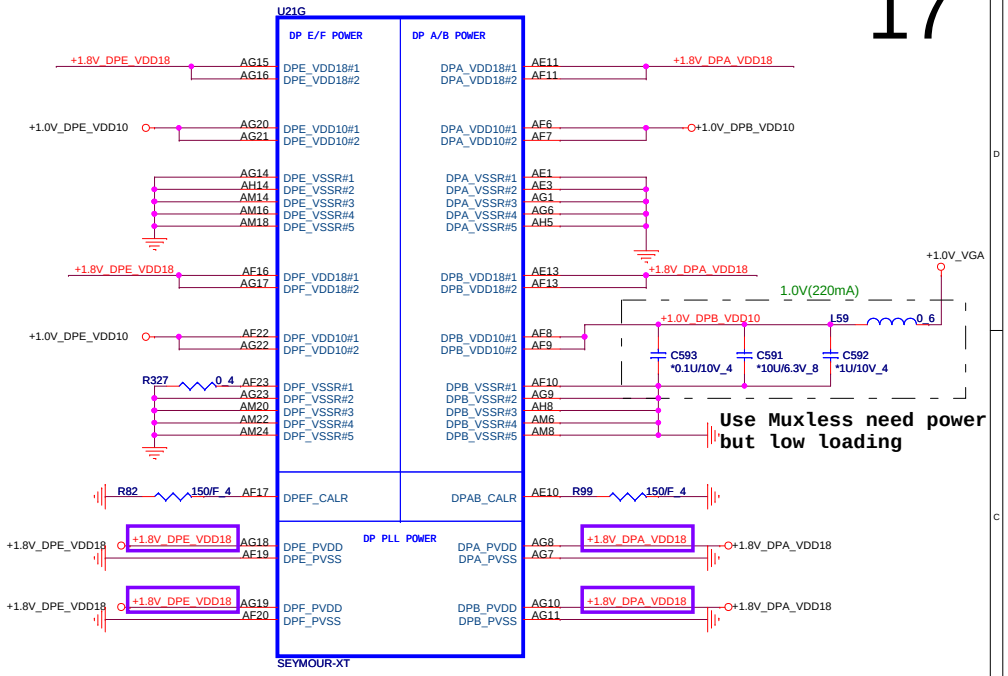
NB5/RD2

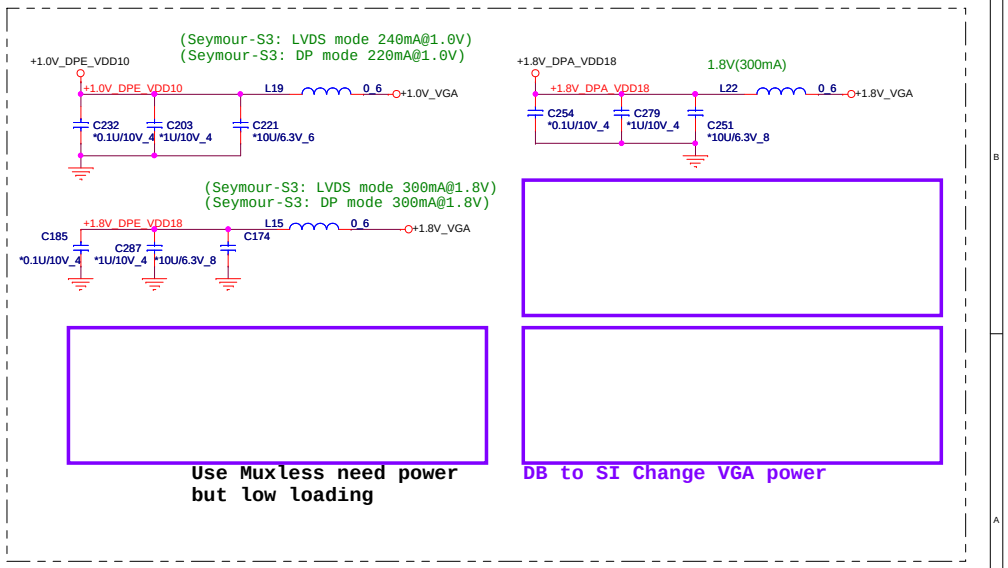
PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-STRAPS	1A

Date: Wednesday, September 15, 2010 Sheet 16 of 43







PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SEYMOUR-XT PCIE_Interface	1A

NB5/RD2

Date: Wednesday, September 15, 2010 Sheet 17 of 43

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D
0101	Reserved		
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C
0111	Samsung- E die	64*16-900MHZ	K4W1G1646E-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1001	Reserved		
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

MEM_ID[3:0]	31 Level BOM	H/W setting
0000	TBD	TBD
0001	TBD	TBD
0010	TBD	TBD
0011	TBD	TBD
0100	TBD	TBD

Memory ID

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

Add a 3K ohm pull-down resistor to set the correct VDDC during power up.

Seymour uninstall to meet AF24 N/C

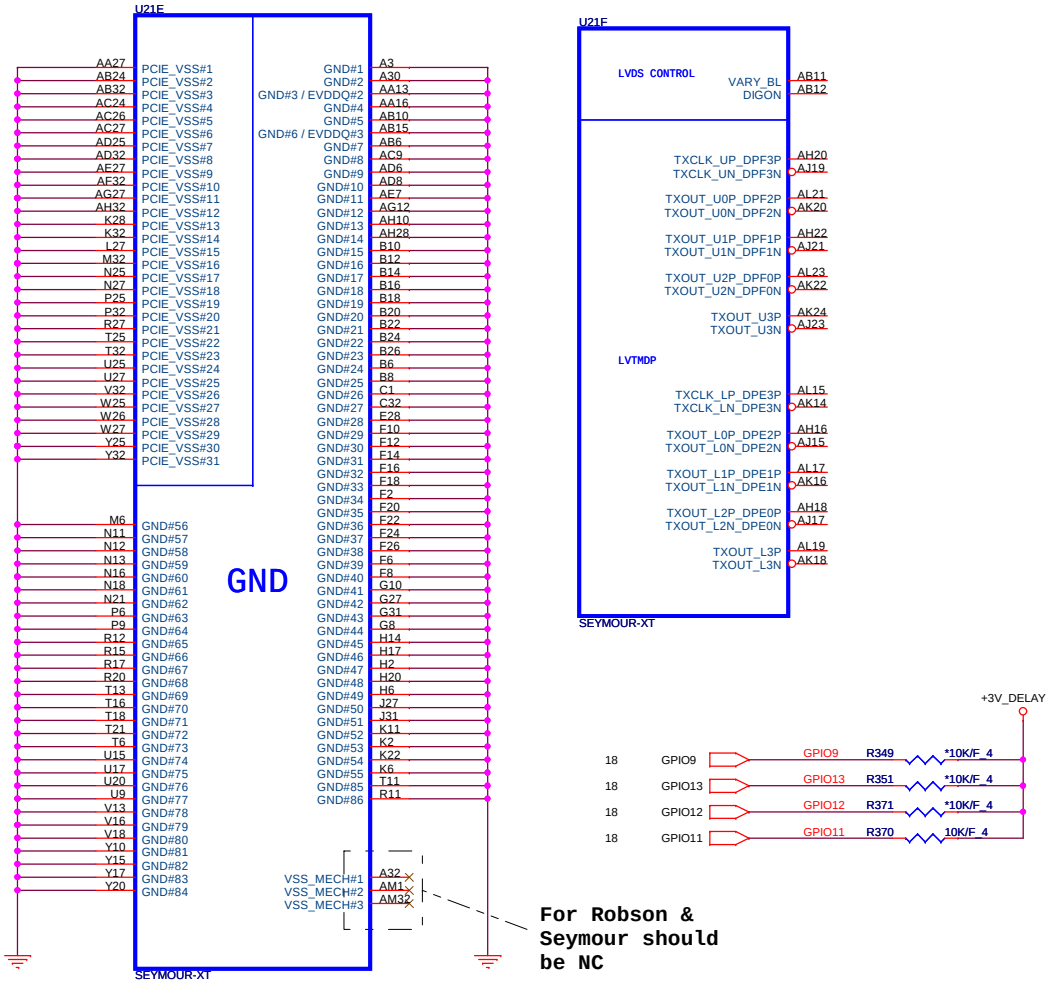
If no contact this pin to LVDS need pull low

Robson-- Install
Seymour-- NC
BACO mode -- install

BACO MODE:AD19 & AE17 & AE20 need with power

Robson-- Install
Seymour-- NC

For Int Clk 27Mhz



For Robson & Seymour should be NC

CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

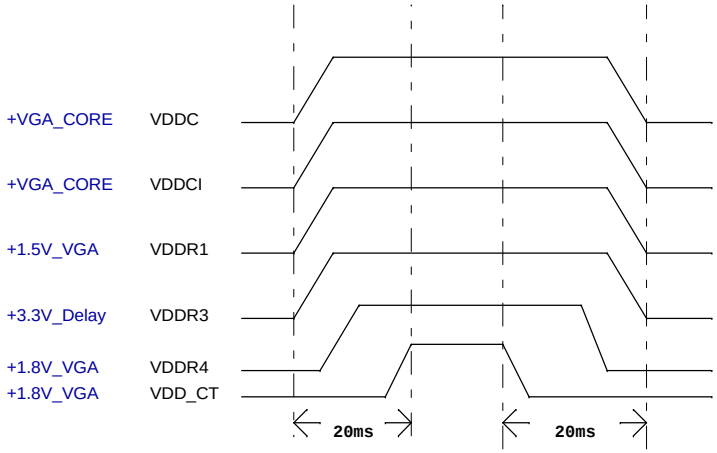
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0 X
RSVD RSVD	GPIO2 GPIO8	RESERVED RESERVED	0 0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

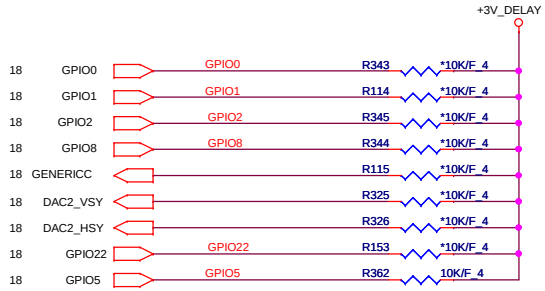
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



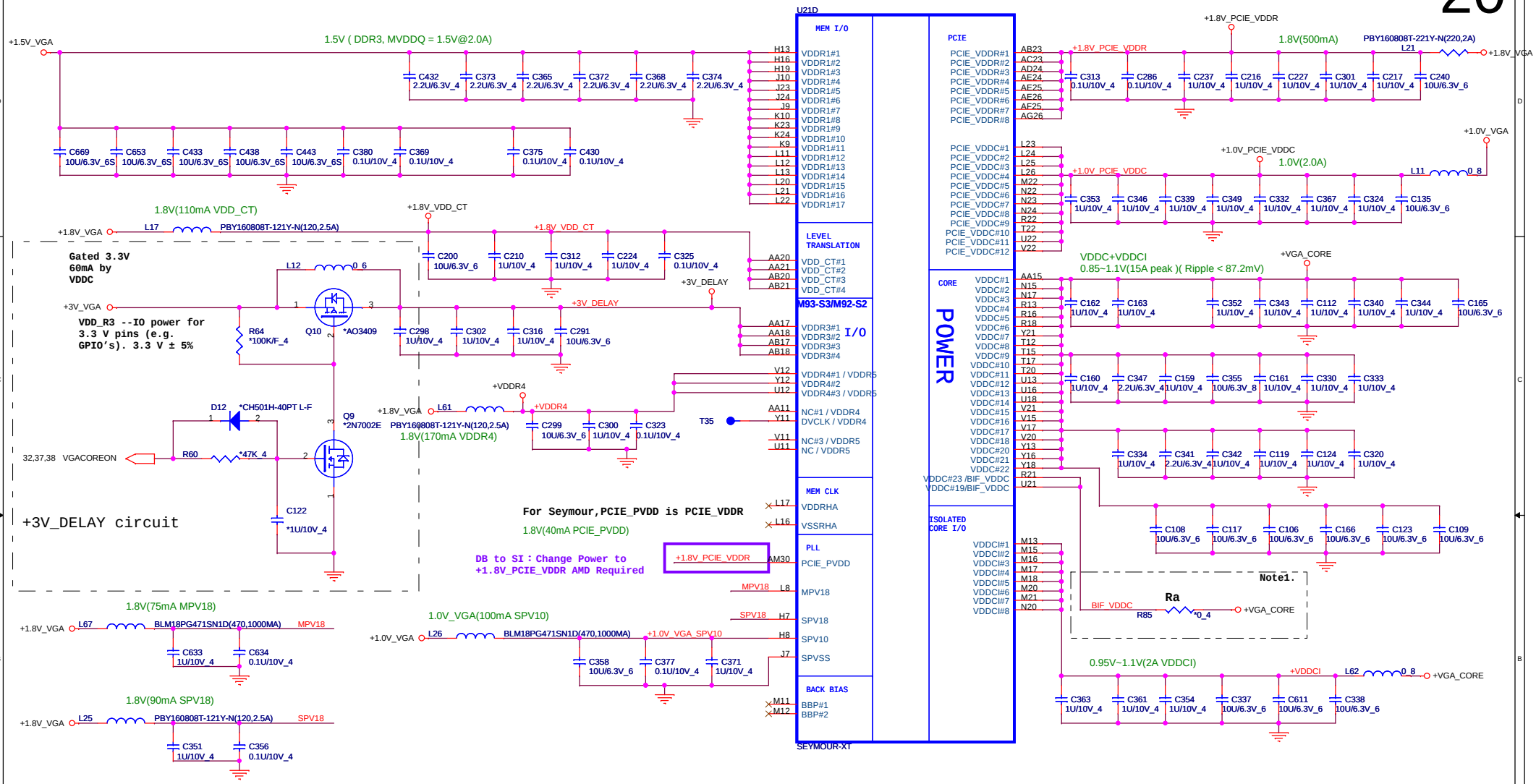
NB5/RD2

PROJECT : R22
Quanta Computer Inc.

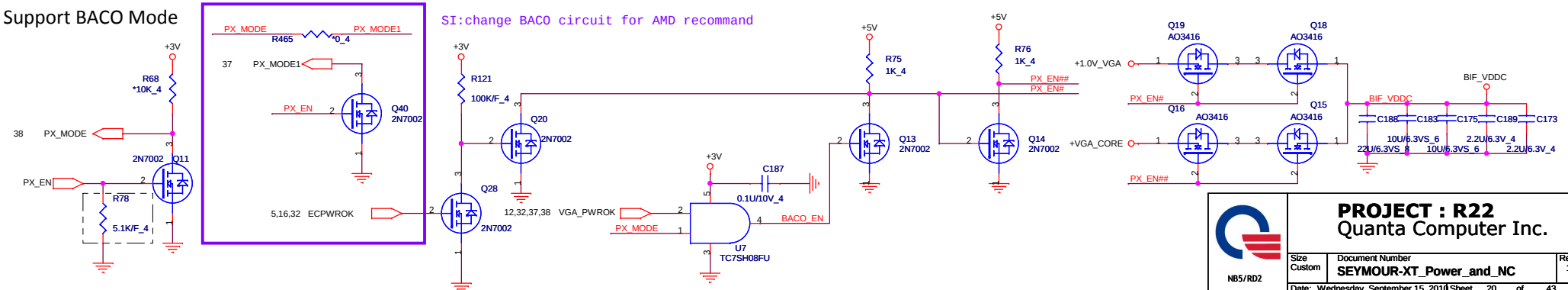
Size	Document Number	Rev
Custom	SEYMOUR-XT GND / LVDS/ Straps	1A

Date: Wednesday, September 15, 2010 Sheet 19 of 43

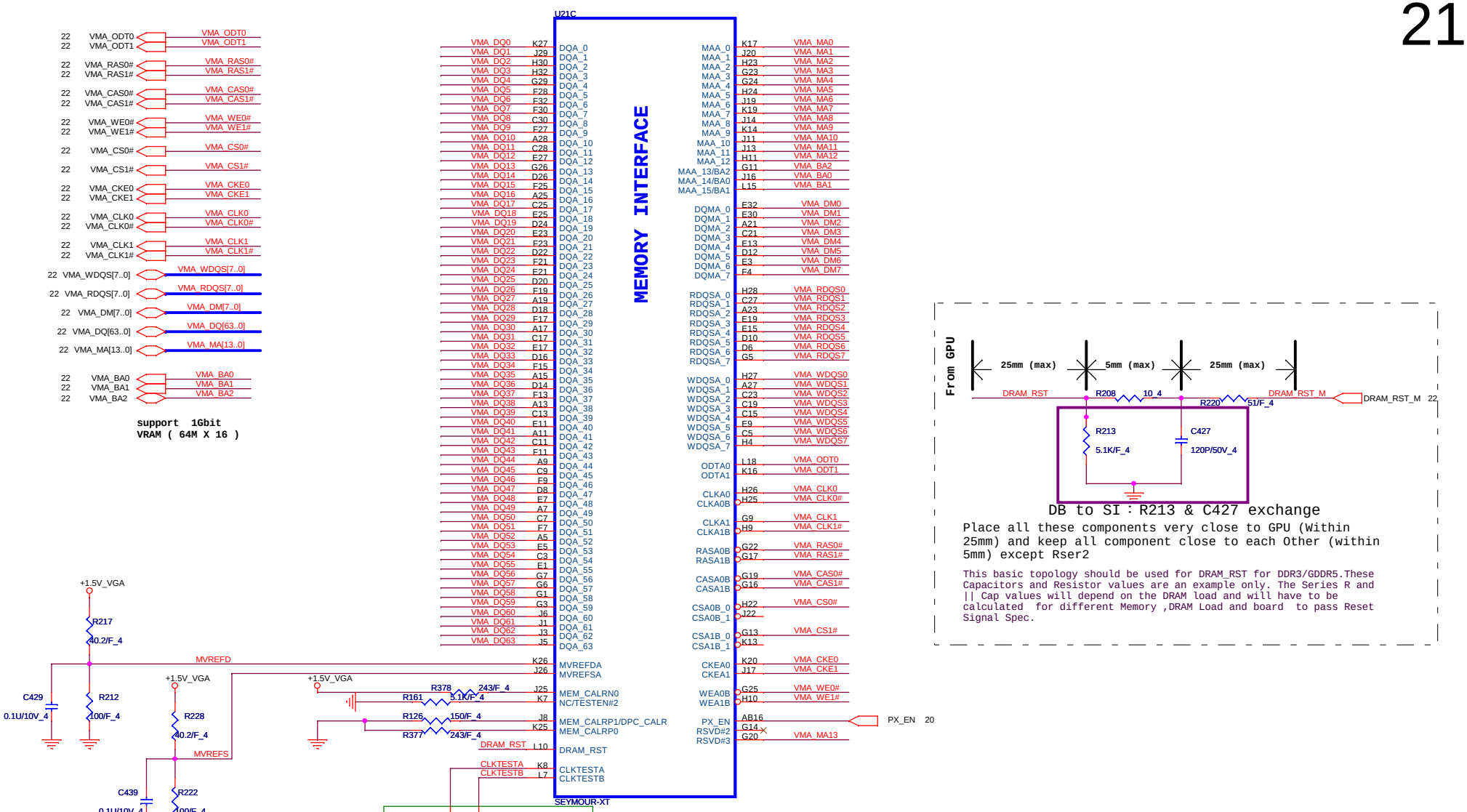
PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



Support BACO Mode



NB5/RD2	**PROJECT : R22** Quanta Computer Inc.		
	Size: Custom	Document Number: SEYMOUR-XT_Power_and_NC	Rev: 1A
	Date: Wednesday, September 15, 2010	Sheet 20 of 43	



NB5/RD2	PROJECT : R22 Quanta Computer Inc.	
	Size: Custom Document Number: SEYMOUR-XT MEM_Interface	Rev: 1A
	Date: Wednesday, September 15, 2010 Sheet 21 of 43	

512MB DDR3

21 VMA_MA[13..0]
21 VMA_DM[7..0]
VMA_MA[13..0]
21 VMA_DQ[63..0]
21 VMA_WDQS[7..0]
21 VMA_RDQS[7..0]

U14 / U24 / U13 / U23 — K4W1G1646E-HC12 (100-BALL SDRAM DDR3)

Should be 240 Ohms +-1%

R227 243/F_4 (U14) · R382 243/F_4 (U24) · R218 243/F_4 (U13) · R379 243/F_4 (U23)

+1.5V_VGA

R386 4.99K/F_4 · R385 4.99K/F_4 · C655 .1U/10V_4 · VREFC_VMA1
R202 4.99K/F_4 · R207 4.99K/F_4 · C431 .1U/10V_4 · VREFD_VMA1
R384 4.99K/F_4 · R387 4.99K/F_4 · C663 .1U/10V_4 · VREFC_VMA2
R205 4.99K/F_4 · R210 4.99K/F_4 · C646 .1U/10V_4 · VREFD_VMA2
R231 4.99K/F_4 · R230 4.99K/F_4 · C445 .1U/10V_4 · VREFC_VMA3
R223 4.99K/F_4 · R229 4.99K/F_4 · C440 .1U/10V_4 · VREFD_VMA3
R381 4.99K/F_4 · R383 4.99K/F_4 · C651 .1U/10V_4 · VREFC_VMA4
R376 4.99K/F_4 · R380 4.99K/F_4 · C645 .1U/10V_4 · VREFD_VMA4

VMA_CLK0 · R214 56.2/F_4 · C436 .01U/16V_4 · VMA_CLK0_COMM · R221 56.2/F_4 · VMA_CLK0#
VMA_CLK1 · R211 56.2/F_4 · C428 .01U/16V_4 · VMA_CLK1_COMM · R215 56.2/F_4 · VMA_CLK1#

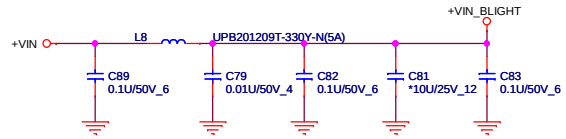
+1.5V_VGA
C425 1U/6.3V_4 · C426 1U/6.3V_4 · C452 1U/6.3V_4 · C441 1U/6.3V_4 · C434 1U/6.3V_4 · C424 1U/6.3V_4 · C422 1U/6.3V_4 · C666 1U/6.3V_4
C640 1U/6.3V_4 · C638 1U/6.3V_4 · C664 1U/6.3V_4 · C421 1U/6.3V_4 · C667 1U/6.3V_4 · C656 1U/6.3V_4 · C637 1U/6.3V_4 · C635 1U/6.3V_4
C670 1U/6.3V_4 · C668 1U/6.3V_4 · C658 1U/6.3V_4 · C446 1U/6.3V_4 · C449 1U/6.3V_4 · C451 1U/6.3V_4 · C661 1U/6.3V_4 · C665 1U/6.3V_4
C642 1U/6.3V_4 · C641 1U/6.3V_4 · C639 1U/6.3V_4 · C649 1U/6.3V_4 · C650 1U/6.3V_4 · C652 1U/6.3V_4 · C442 1U/6.3V_4 · C448 1U/6.3V_4
C662 10U/6.3V_6S · C643 10U/6.3V_6S · C455 10U/6.3V_6S · C457 10U/6.3V_6S · C454 10U/6.3V_6S
C644 10U/6.3V_6S · C654 10U/6.3V_6S · C657 10U/6.3V_6S · C648 10U/6.3V_6S · C453 10U/6.3V_6S · C456 10U/6.3V_6S · C450 10U/6.3V_6S

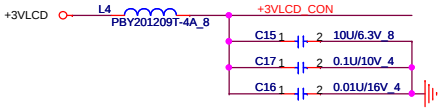
	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

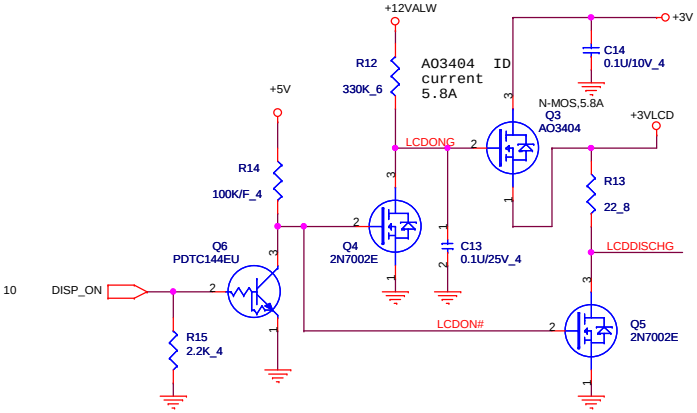
NB5/RD2

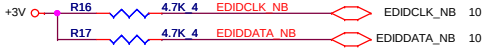
PROJECT : R22
Quanta Computer Inc.

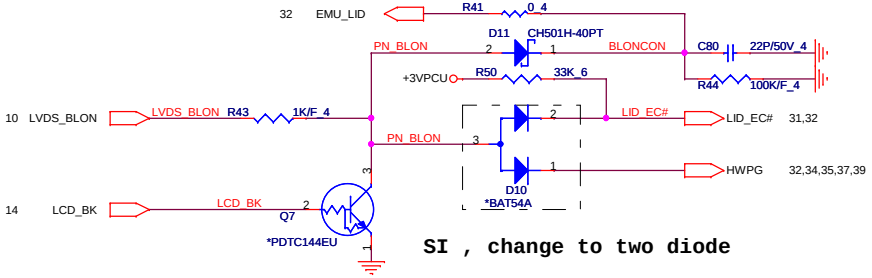
Size: Custom | Document Number: SEYMOUR-XT VRAM(DDR3 BGA96) | Rev: 3A
Date: Wednesday, September 15, 2010 | Sheet 22 of 43



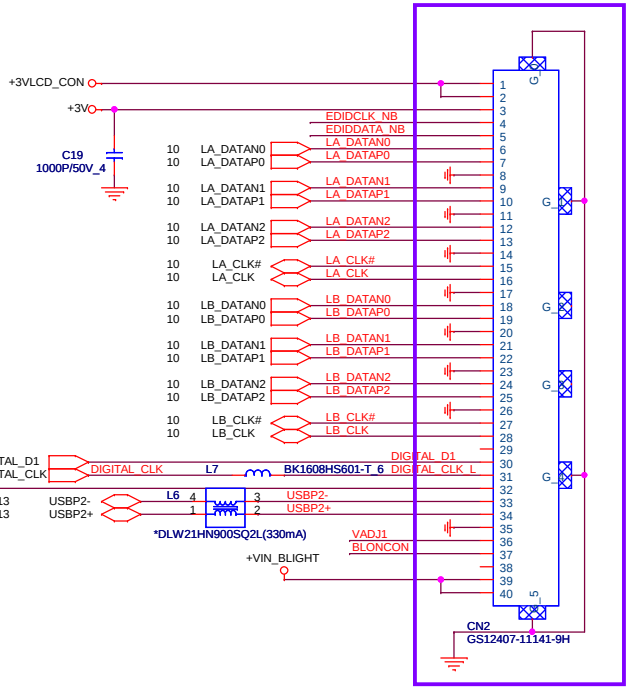




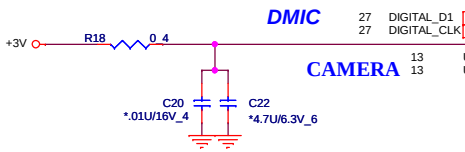


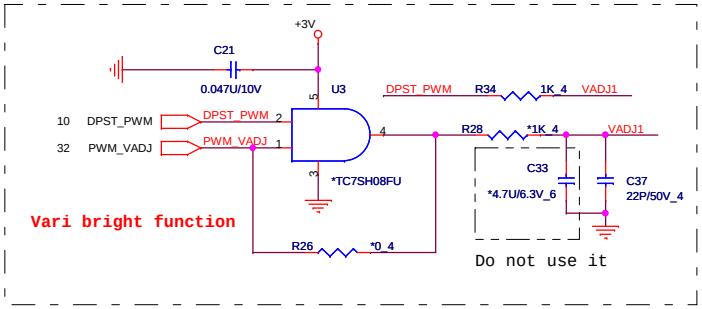


SI , change to two diode

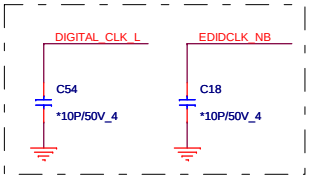


CN2 Change PN DFHS40FS036



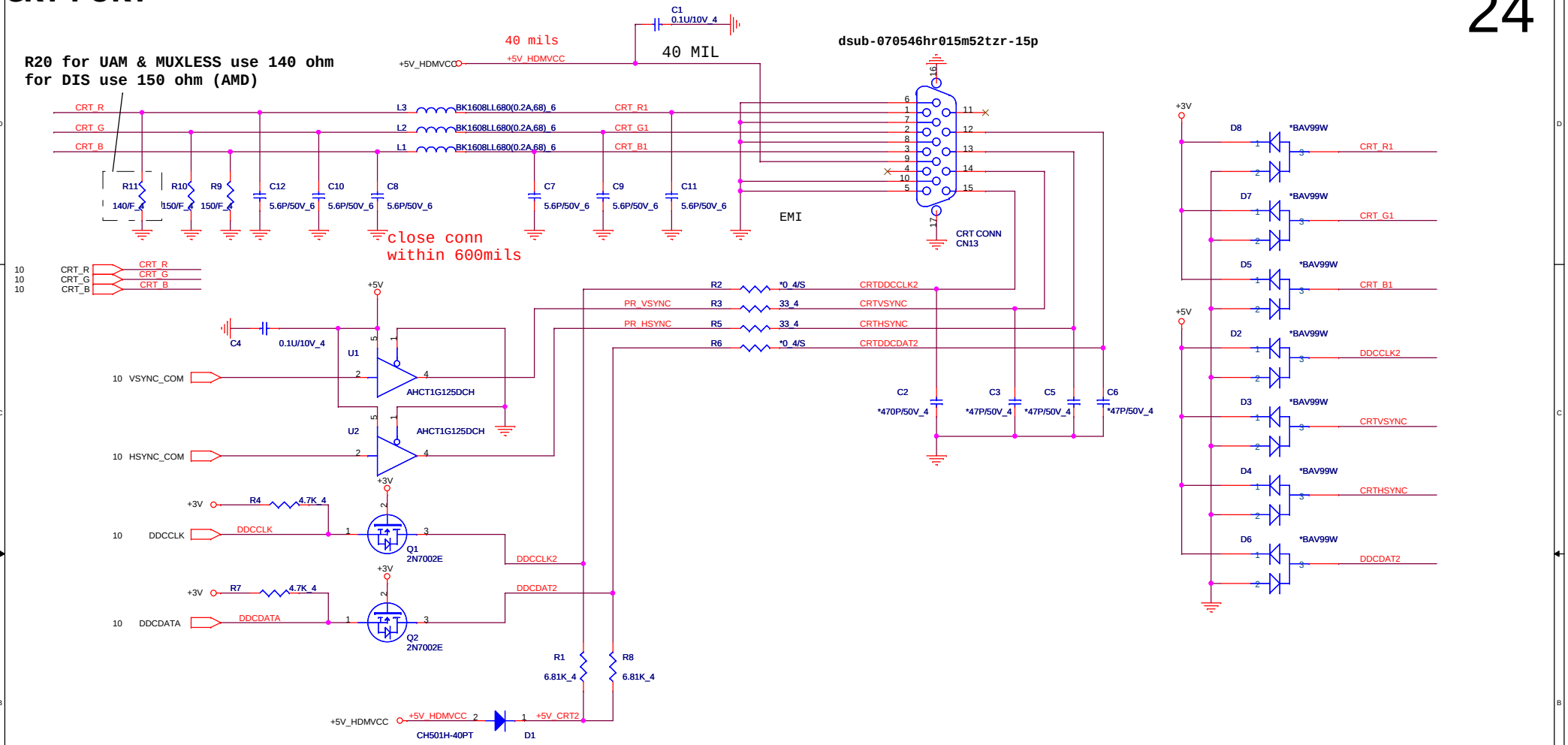


Reserve for EMI



NB5/RD2	**PROJECT : R22** Quanta Computer Inc.	
	Size: Custom — Document Number: **LCD CONN**	Rev: 1A
	Date: Wednesday, September 15, 2010 — Sheet 23 of 43	

CRT PORT



NB5/RD2	**PROJECT : R22** Quanta Computer Inc.
Size: Custom	Document Number: CRT
Rev: 1A	
Date: Wednesday, September 15, 2010	Sheet 24 of 43

UMA/DISCRETE select for HDMI

From RS880M

for Layout concern ,placement close north bridge

9 C_PEG_TX15 — C_PEG_TX15 C625 0.1U/10V_4 TX2_HDMI-L
9 C_PEG_TX#15 — C_PEG_TX#15 C626 0.1U/10V_4 TX2_HDMI+L
9 C_PEG_TX14 — C_PEG_TX14 C623 0.1U/10V_4 TX1_HDMI-L
9 C_PEG_TX#14 — C_PEG_TX#14 C624 0.1U/10V_4 TX1_HDMI+L
9 C_PEG_TX#13 — C_PEG_TX#13 C620 0.1U/10V_4 TX0_HDMI-L
9 C_PEG_TX13 — C_PEG_TX13 C622 0.1U/10V_4 TX0_HDMI+L
9 C_PEG_TX#12 — C_PEG_TX#12 C615 0.1U/10V_4 TXC_HDMI-L
9 C_PEG_TX12 — C_PEG_TX12 C617 0.1U/10V_4 TXC_HDMI+L

+5V
Q35 2N7002E
R335 100K/F_4

R118 715/F_4 TX2_HDMI+L
R113 715/F_4 TX2_HDMI-L
R111 715/F_4 TX1_HDMI+L
R107 715/F_4 TX1_HDMI-L
R127 715/F_4 TX0_HDMI+L
R124 715/F_4 TX0_HDMI-L
R102 715/F_4 TXC_HDMI+L
R101 715/F_4 TXC_HDMI-L

Close to HDMI Connector

HDMI HPD SENSE

10 INT_TMDS_HPD — R331 *0_4/S
+3V
R330 10K/F_4
Q33 2N7002E
+3V
R334 10K/F_4
Q34 2N7002E
HDMI_DET_R
R338 200K/F_4
HDMI_DET
R339 200K/F_4

HDMI Connector

+5V_HDMVCC
D14 CH501H-40PT
R88 2K_4
HDMI_SCLK

+5V_HDMVCC
D13 CH501H-40PT
R87 2K_4
HDMI_SDATA

Add for EMI debug

RP6 0_4P2R_4
TX2_HDMI-L — TX2_HDMI-
TX2_HDMI+L — TX2_HDMI+
RP5 0_4P2R_4
TX1_HDMI-L — TX1_HDMI-
TX1_HDMI+L — TX1_HDMI+
RP7 0_4P2R_4
TX0_HDMI-L — TX0_HDMI-
TX0_HDMI+L — TX0_HDMI+
RP4 0_4P2R_4
TXC_HDMI-L — TXC_HDMI-
TXC_HDMI+L — TXC_HDMI+

Need add nearby HDMI CONN

+5V — FUSE1A6V_POLY F1 — +5V_HDMVCC
C230 *0.1U/10V_4
1A

CN21 CON_HDMI_A SMT_R
TYPE A
TX2_HDMI+ 1
TX2_HDMI- 3
TX1_HDMI+ 4
TX1_HDMI- 6
TX0_HDMI+ 7
TX0_HDMI- 9
TXC_HDMI+ 10
TXC_HDMI- 12
HDMI_SCLK 15
HDMI_SDATA 16
+5V_HDMVCC 18
HDMI_DET 19
GND 20 21
I71

hdmi-100042mr019s172zl-19p-v

UMA HDMI I2C SELECT

Close to HDMI Connector

10 HDMI_DDC_DATA
10 HDMI_DDC_CLK
RP3 0_4P2R_4
HDMI_SDATA
HDMI_SCLK

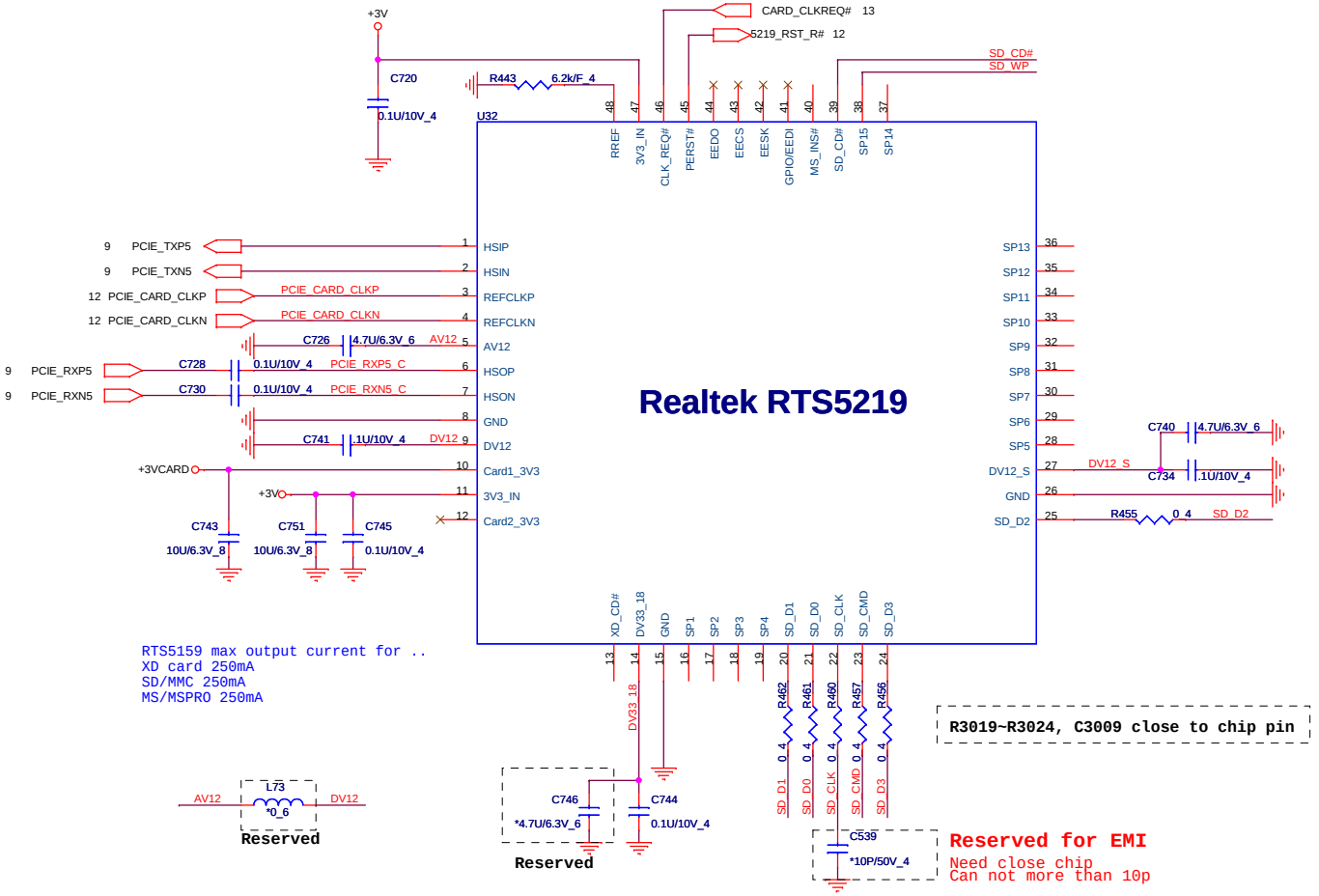
UMA

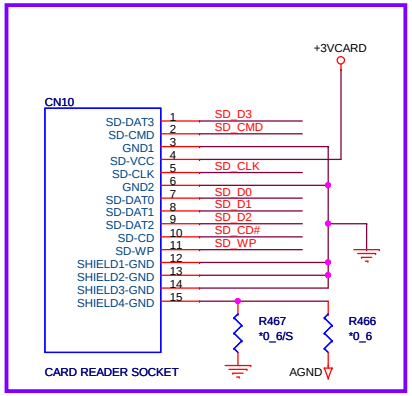
PROJECT : R22
Quanta Computer Inc.

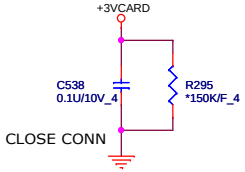
Size	Document Number	Rev
Custom	HDMI	1A

NB5/RD2

Date: Wednesday, September 15, 2010 Sheet 25 of 43







DB to SI Change Footprint to SDCARD-CS1S-038-11P-SMT For SMT issue

NB5/RD2	PROJECT : R22 Quanta Computer Inc.	
	Size: Custom Document Number: RTS5219 & CR SOCKET	Rev: 1A
	Date: Wednesday, September 15, 2010 Sheet 26 of 43	

3,5,6,7,10,11,12,13,14,15,16,20,23,24,25,26,28,29,30,31,32,33,38,39 +3V
+4.75VAVDD
5,20,23,24,25,28,29,31,33,39 +5V

Close to CODEC

Close to CODEC

>40mils trace

+5V_AVDD L70 +4.75VAVDD
HCB1608KF-181T15/1.5A_6
C703 10U/6.3VS_6 C700 1U/6.3V_4 C725 0.1U/10V_4
AGND

+4.75VAVDD
U29
C704 2.2U/10V_6 C698 0.1U/10V_4 C691 1U/6.3V_4
TPS793475
C697 0.1U/10V_4 C694 0.047U/10V_4 C693 1U/6.3V_4
R432 10K_4 +5V
Vset=1.242V

+3V_DVDD_CORE
C707 10U/6.3VS_6

+3V
C727 1U/6.3V_4 C724 0.1U/10V_4
C712 0.1U/10V_4

U31

HDA Bus

13 BIT_CLK_AUDIO R444 0_4 HD_BCLK
13 ACZ_SDIN0 R445 33_4 HD_SDIN0
13 ACZ_SDOUT_AUDIO R442 0_4 HD_SDOUT
13 ACZ_SYNC_AUDIO C719 *10P/50V_4 R447 0_4 HD_SYNC
13 ACZ_RST#_AUDIO C729 *10P/50V_4

DVDD_CORE 1
DVDD 9
DVDD_IO 3
HDA_BITCLK 6
HDA_SDI 8
HDA_SDO 5
HDA_SYNC 10
HDA_RST# 11

Digital

AVDD 27 AVDD 38
PVDD 39 PVDD 45
SENSE_A 13 SENSE_A SENSE_A 28
SENSE_B 14 SENSE_B

Close to CODEC

>40mils trace

+5V
C702 1U/6.3V_4 C701 0.1U/10V_4 C699 10U/6.3VS_6
AGND

Close to CODEC

SENSE_A R451 2.49K/F_4 +5V_AVDD
C735 1000P/50V_4 AGND
SENSE_B R450 100K/F_4 +5V_AVDD

TO Digital MIC

23 DIGITAL_CLK C706 10P/50V_4 R439 100/F_4 DMIC_CLK_R
23 DIGITAL_D1 R441 0_4 DMIC0 C716 10P/50V_4

DMIC_CLK/GPIO1 2
DMIC0/GPIO2 4
DMIC1/GPIO0/SPDIF_OUT_1 46
SPDIF_OUT_0 48
EAPD 47
DVSS 7

HP0_PORT_A_L 28
HP0_PORT_A_R 29
VREFOUT_A_or_F 23

HP1_PORT_B_L 31 HPOUT_L HPOUT_L 28 AGND SHIELD
HP1_PORT_B_R 32 HPOUT_R HPOUT_R 28 AGND SHIELD
AGND SHIELD

TO Headphone jack

PORT_C_L 19 MIC_L MIC_L 28
PORT_C_R 20 MIC_R MIC_R 28
VREFOUT_C 24 VREFOUT_C VREFOUT_C 28

TO Audio Jack MIC

SPKR_PORT_D_L+ 40 L_SPK+
SPKR_PORT_D_L- 41 L_SPK-
SPKR_PORT_D_R- 43 R_SPK-
SPKR_PORT_D_R+ 44 R_SPK+

TO Internal Speakers

PORT_E_L 15
PORT_E_R 16
PORT_F_L 17
PORT_F_R 18
PC_BEEP 12 AMP_BEEP

+3V
R435 10K_4
32 VOLMUTE# ADC_EAPD#
D26 RB500V-40

Close to CODEC

CAP- C711 4.7U/6.3V_6 CAP+

CAP- 35
CAP+ 36
AVSS 33
AVSS 30
AVSS 26
PVSS 42
DAP 49

Analog

92HD80B1X5NLGXA4B

VREG 21 V- 20 VREFFILT 22 CAP2 24 MONO_OUT 25

C10625 close C10629, and C10625 close Chip

C736 0.1U/10V_4 AMP_BEEP_L R453 100K_4 AMP_BEEP_R2 C738 0.1U/10V_4
C737 0.01U/16V_4 R452 10K_4
R10453 close R10454
AGND

+5V_AVDD
R458 10K_4
2N7002 Q39 6/17
ACZ_SPKR 13

Check layout mount location

+3V
R449 *4.7K_4
ACZ_RST#_AUDIO
C731 *.01U/16V_4

ADC_VREG ADC_V- ADC_VREFFILT ADC_CAP2

C705 4.7U/6.3V_6 C721 4.7U/6.3V_6 C733 10U/6.3VS_6 C732 0.1U/10V_4
AGND AGND AGND AGND

Close to CODEC

R388 *0_4
R459 *0_4
R448 *0_4
R434 *0_4
R297 *0_8/S
AGND

DB to SI：Reverse For EMI & ESD

EMI Request

INT. SPEAKER

INT SPEAKER CONN

L_SPK+ L74 SBK160808T-221Y-N/0.2A_6 L_SPK+_R
L_SPK- L75 SBK160808T-221Y-N/0.2A_6 L_SPK-_R
R_SPK- L76 SBK160808T-221Y-N/0.2A_6 R_SPK-_R
R_SPK+ L77 SBK160808T-221Y-N/0.2A_6 R_SPK+_R
CN12

C750 220P/50V_4
C749 220P/50V_4
C748 220P/50V_4
C747 220P/50V_4

DB to SI：9/14 for IDT recommend

BIT_CLK_AUDIO ACZ_SDIN0
C722 *33P/50V_4 C723 33P/50V_4
FOR EMI

SI , check BIT_CLK_AUDIO double pull low

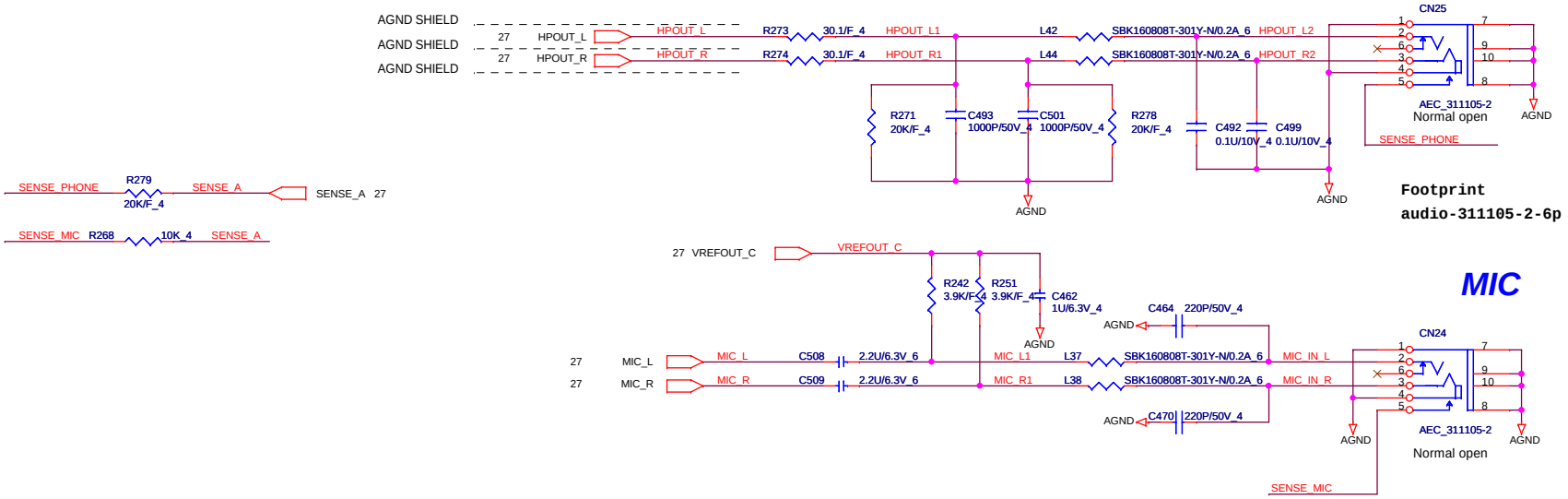
PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia 92HD80	1A

Date: Wednesday, September 15, 2010 Sheet 27 of 43

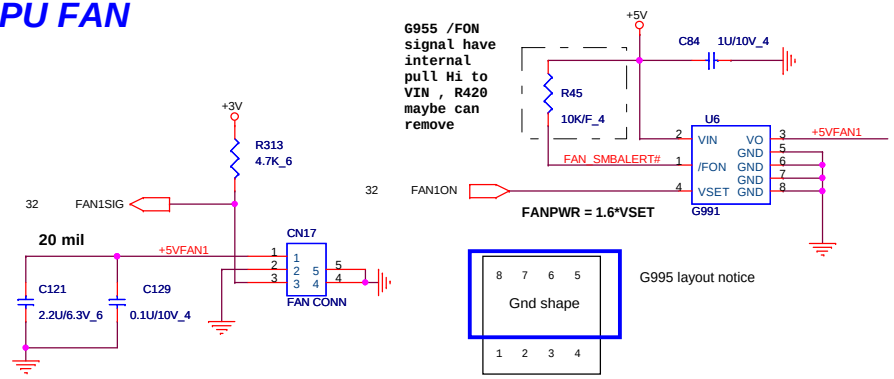
N85/RD2

Line out

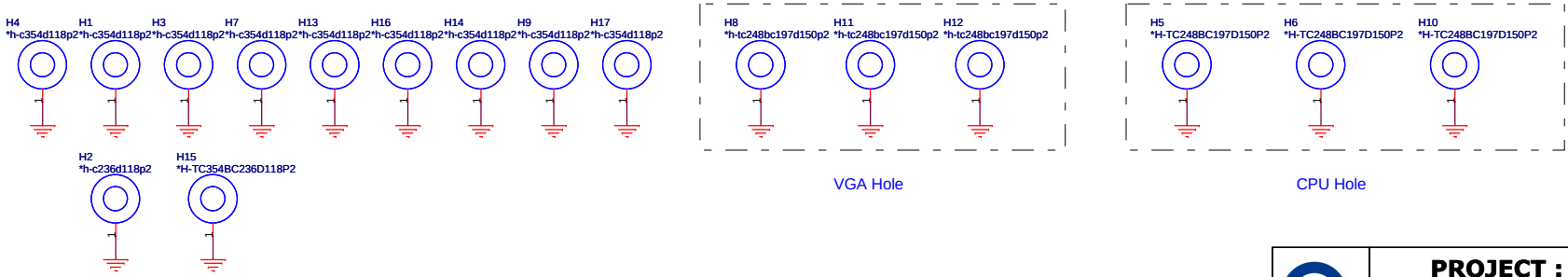


MIC

CPU FAN



HOLE



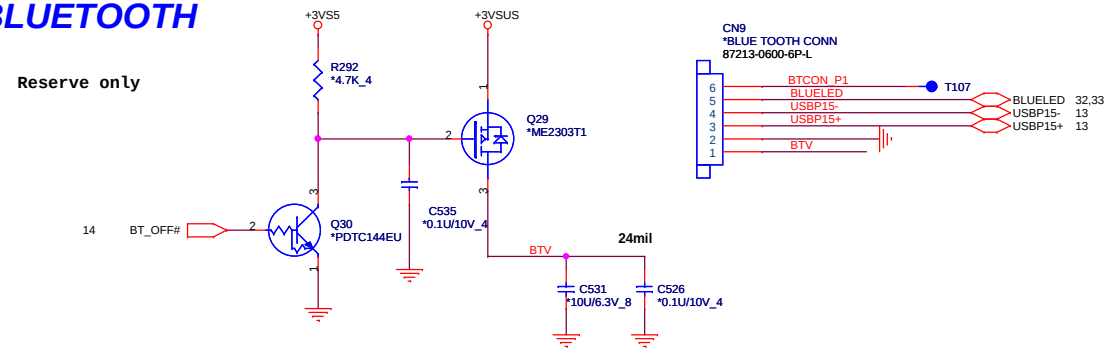
NB5/RD2

PROJECT : R22
Quanta Computer Inc.

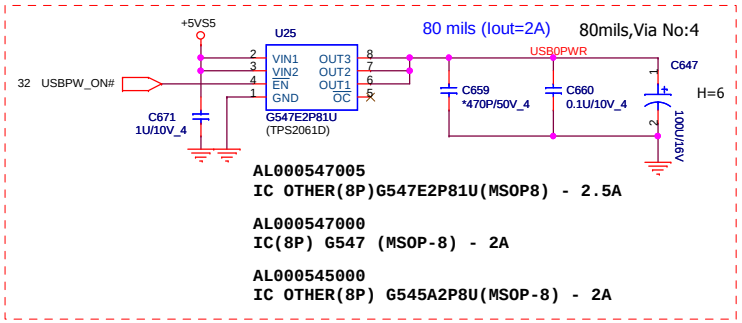
Size	Document Number	Rev
Custom	AMP_TPA6017/CPU FAN/HOLE	1A

Date: Wednesday, September 15, 2010 Sheet 28 of 43

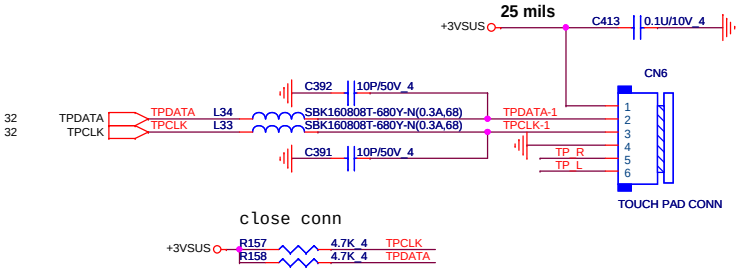
BLUETOOTH



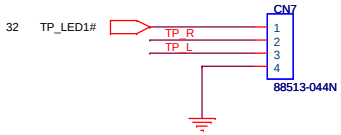
LEFT SIDE USBX2

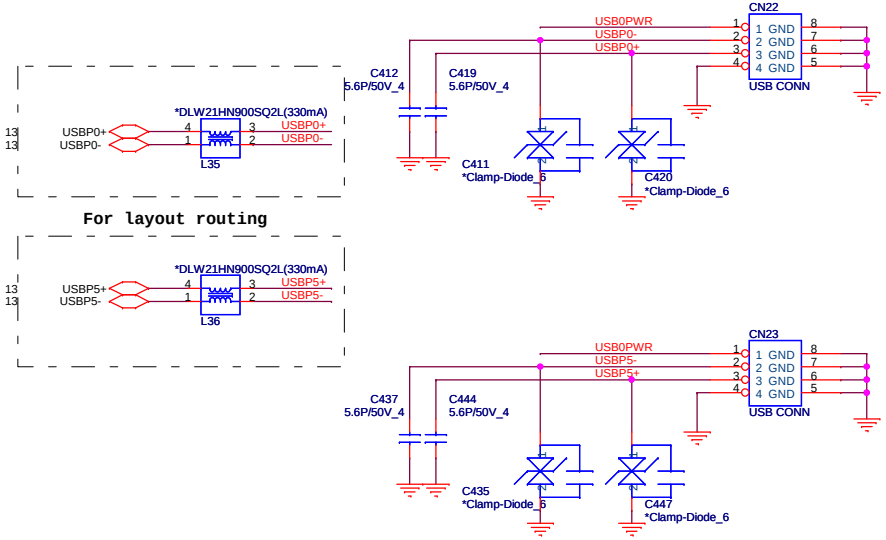


TOUCH PAD CONN

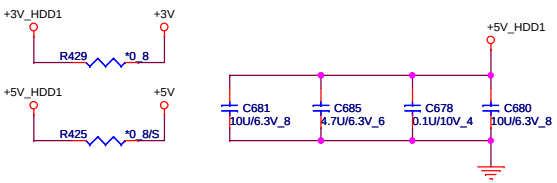


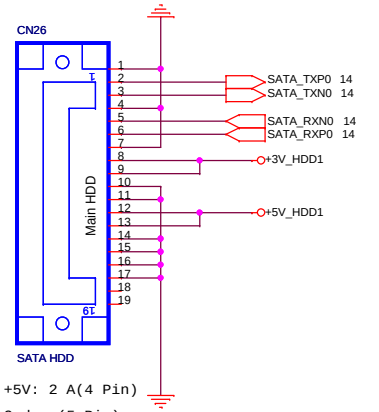
To TOUCH PAD SW board





SATA HDD CONNECTOR

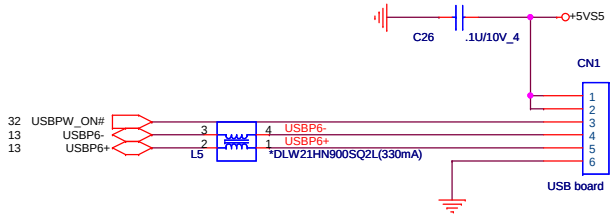




+5V: 2 A(4 Pin)
Gnd : (5 Pin)

ANT CONN

Right SIDE USBX1



NB5/RD2	**PROJECT : R22** Quanta Computer Inc.	
	Size: Custom Document Number: BT/USBX3/TP/HDD	Rev: 1A
	Date: Wednesday, September 15, 2010 Sheet 29 of 43	

IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

GND VIA x 9 Pcs

Power trace Layout 寬度> 60mil

C55,C56 near pins 21.

VDD10 near pins 13, 29, 45.

DB to SI：For Realtek

DB to SI：U5-Pin21 Change to +1.05V_LAN

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

Check schematic control by EC ?

VDD33 nesr pins 27, 39, 47, 48.

Transformer for 10/100

FOR EMI

Footprint : rj45-130452-u4-12p

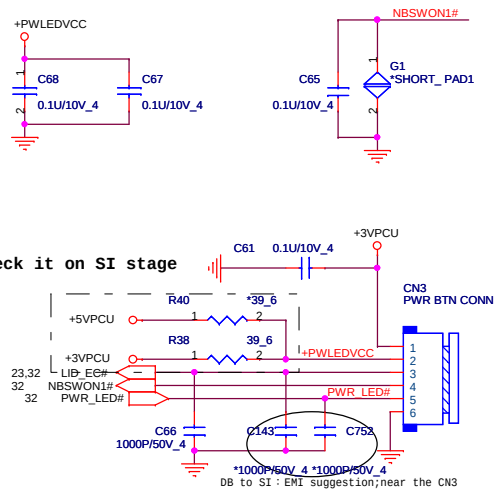
PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8102EL/RJ45	1A

Date: Wednesday, September 15, 2010 Sheet 30 of 43

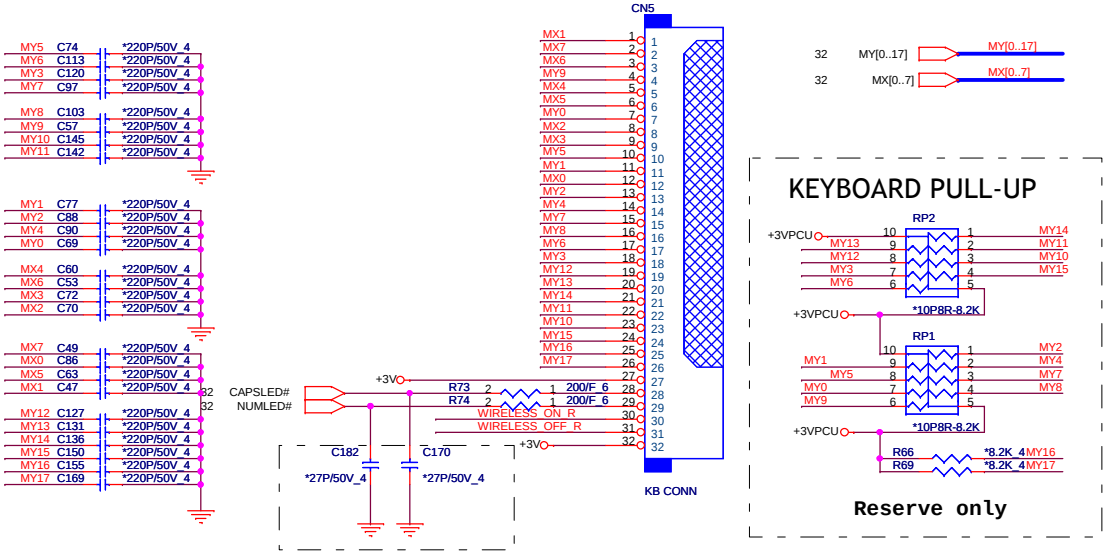
NB5/RD2

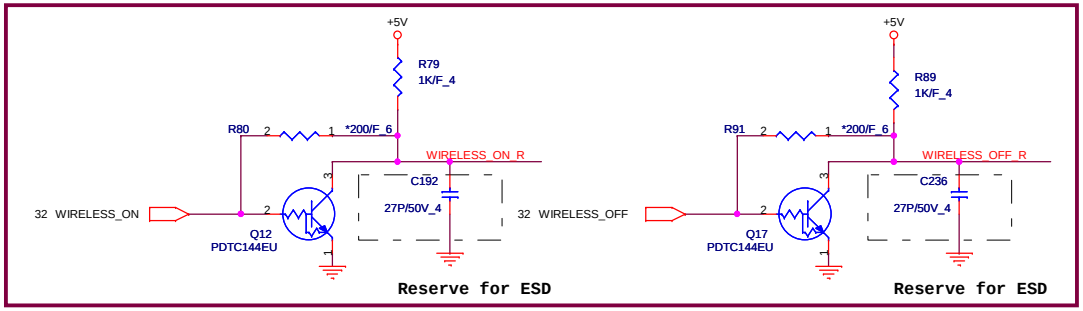
POWER BUTTON CONNECTOR



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

KEYBOARD CONN

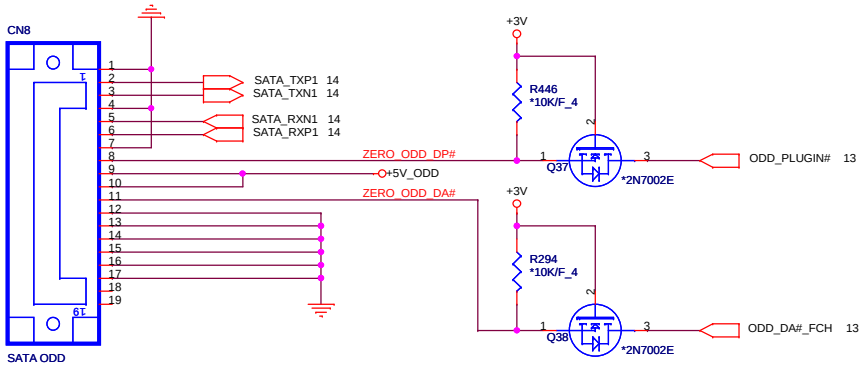




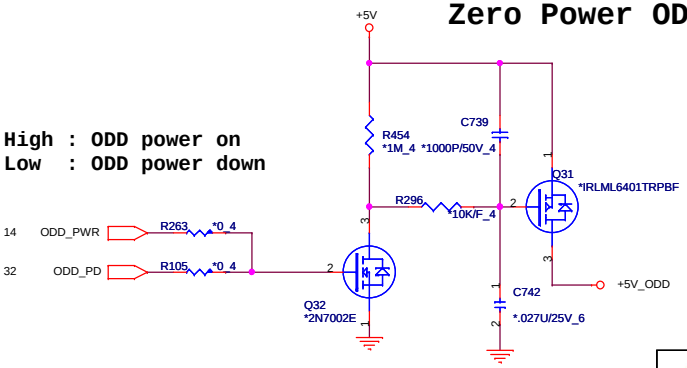
DB to SI : K/B RF LED Change

SATA CD-ROM

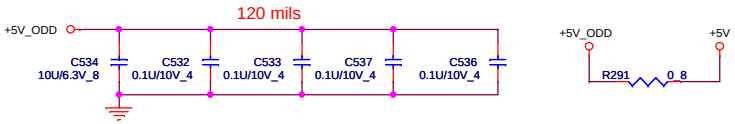
ANT CONN



Zero Power ODD circuit



High : ODD power on
Low : ODD power down



NB5/RD2	**PROJECT : R22** Quanta Computer Inc.	
Size: Custom	Document Number: KEYBOARD/SW_BOARD/ODD	Rev: 1A
Date: Wednesday, September 15, 2010	Sheet 31 of 43	

U9

KB3930QF A1

VGA thermal

Battery charge/discharge Cap button

system thermal

Enable Vari-bright need pull low

MAX	AKE38FP0Z00 2M byte
WINBOND	AKE38FP0N01 SPI
EON	AKE38ZA0Q00 BIOS
SOCKET	DFHS08FS023

Platform model	GPIO42
SG/DIS	High
UMA	Low
TBD	Middle (1.5V)

Hi ==> 90W

Low ==> 65W

If use SB RTC CLK should change to 20P

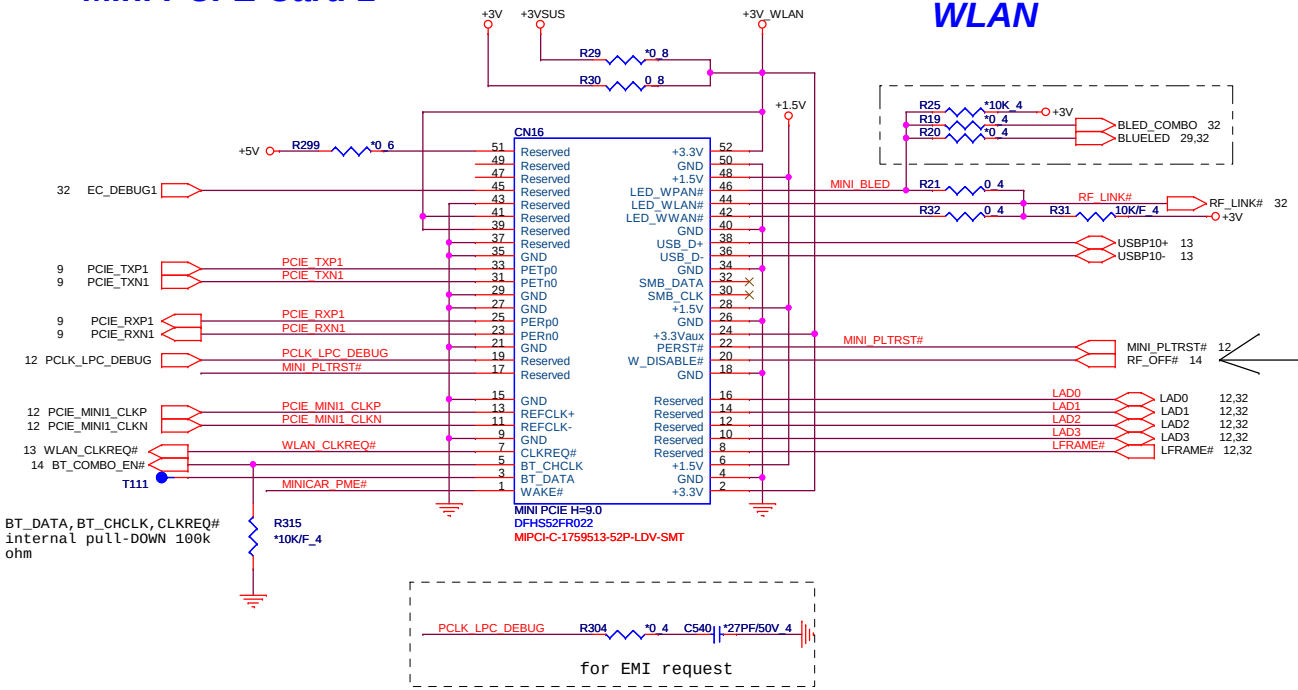
For KB3926 C version

Put close to EC side

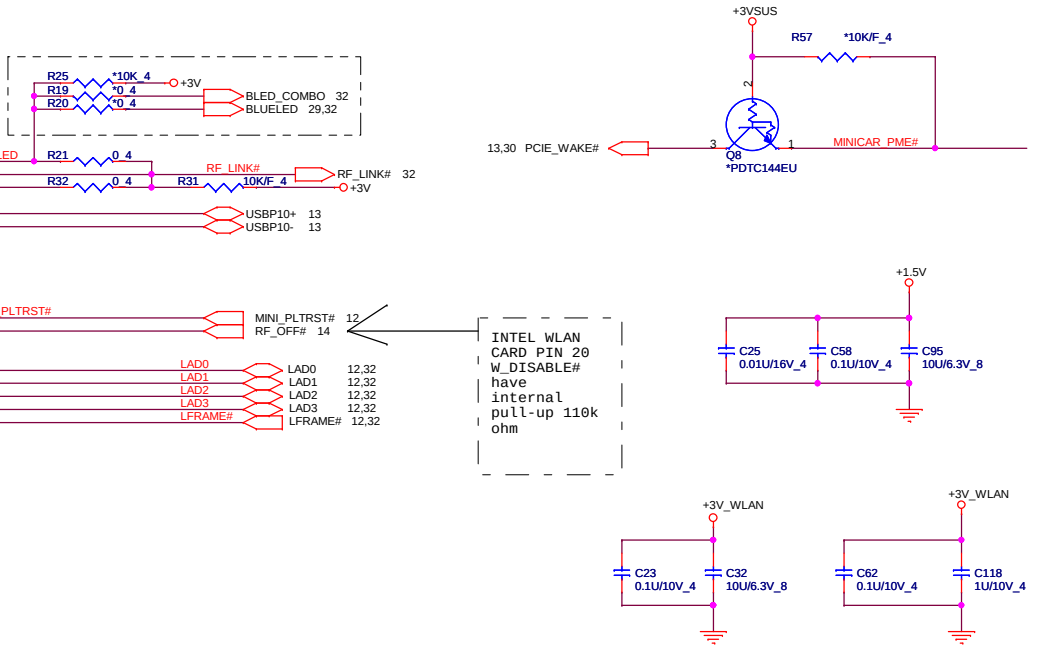
Change D12, D16 to RB500 for current loss

adapter Type check

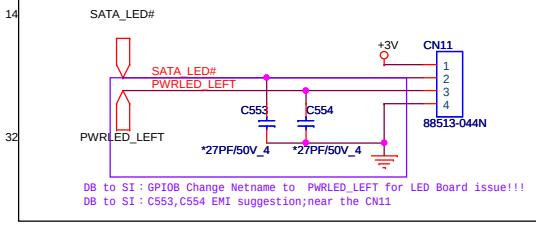
Mini PCI-E Card 1



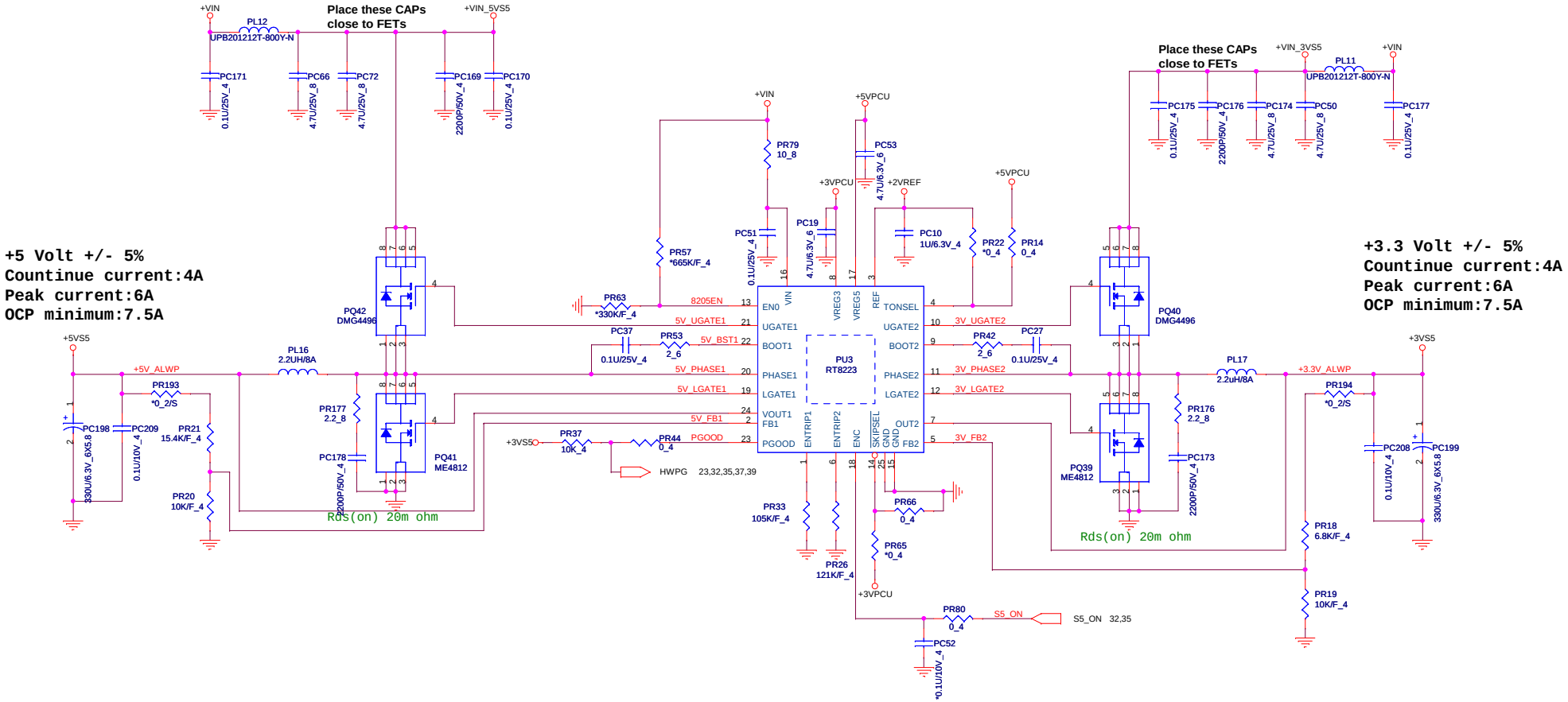
WLAN



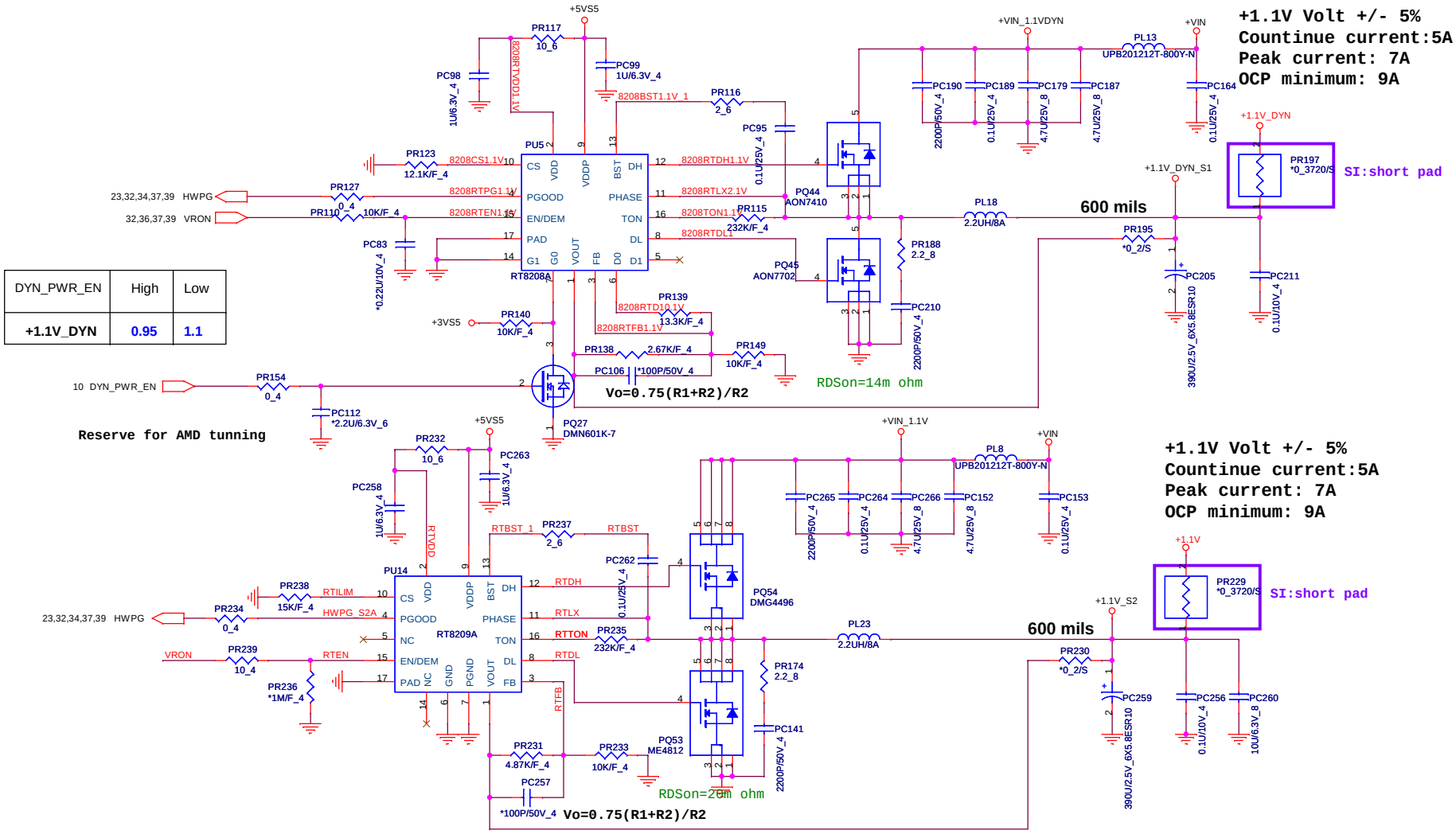
LED board CONN



NB5/RD2	PROJECT : R22 Quanta Computer Inc.	
Size: Custom	Document Number: Mini CARD/LED CONN	Rev: 1A
Date: Wednesday, September 15, 2010	Sheet 33 of 43	



Quanta Computer Inc.	PROJECT : R22		
N85/RD2	Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
	Date: Wednesday, September 15, 2010	Sheet 34 of 43	



DYN_PWR_EN	High	Low
+1.1V_DYN	0.95	1.1

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	1A

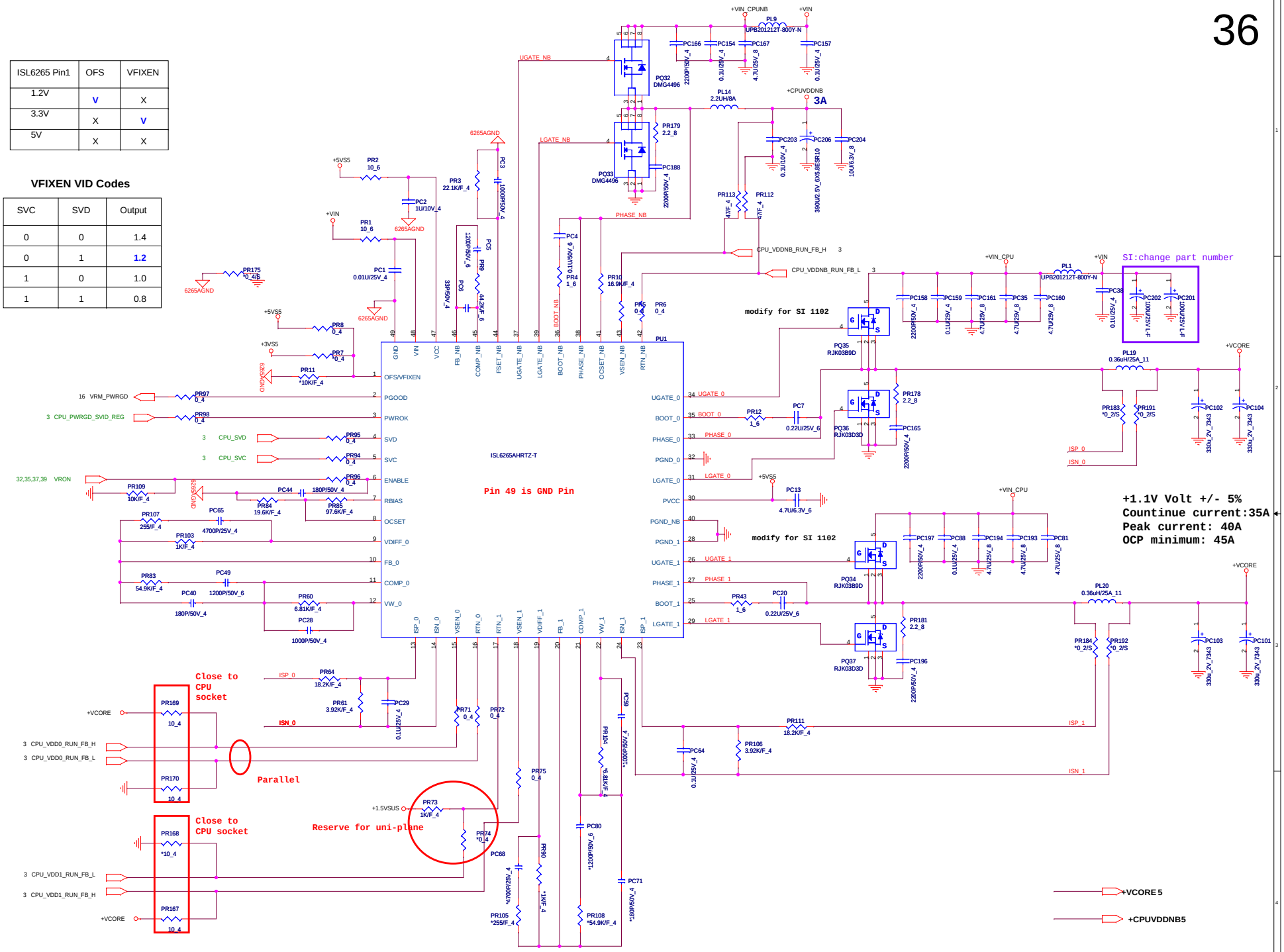
NB5/RD2

Date: Wednesday, September 15, 2010 Sheet 35 of 43

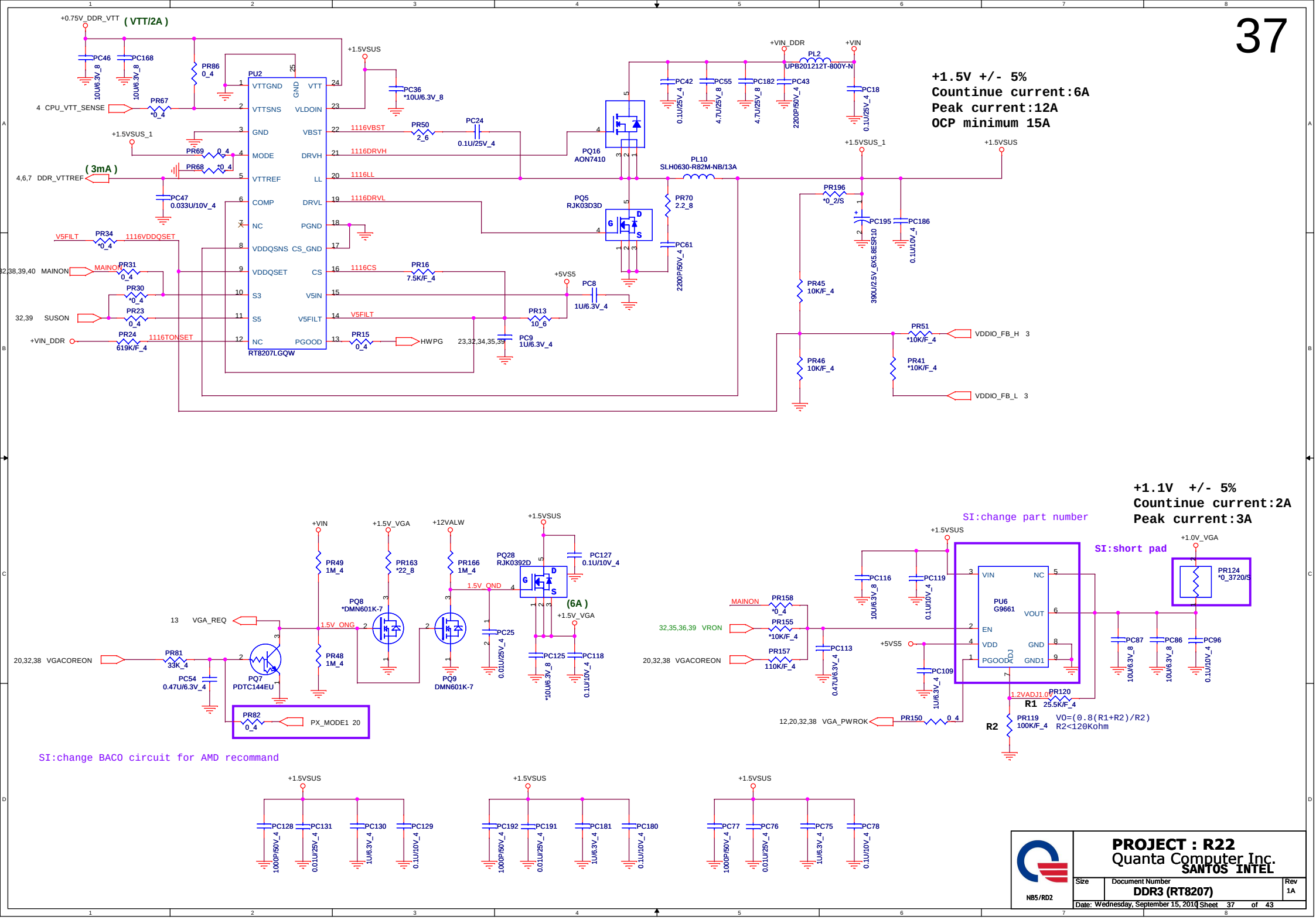
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



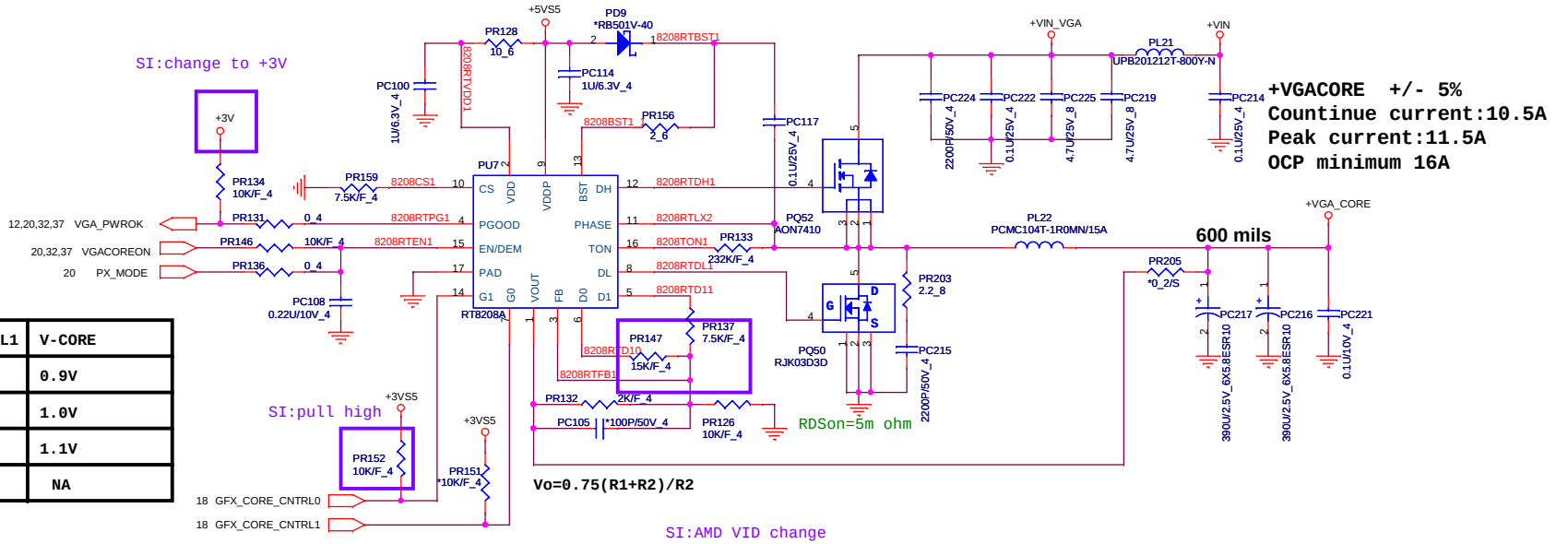
NB5/RD2	PROJECT : R22 Quanta Computer Inc.		
	Size: C	Document Number: CPU_CORE(ISL6265)	Rev: 1A
	Date: Wednesday, September 15, 2010	Sheet 36 of 43	

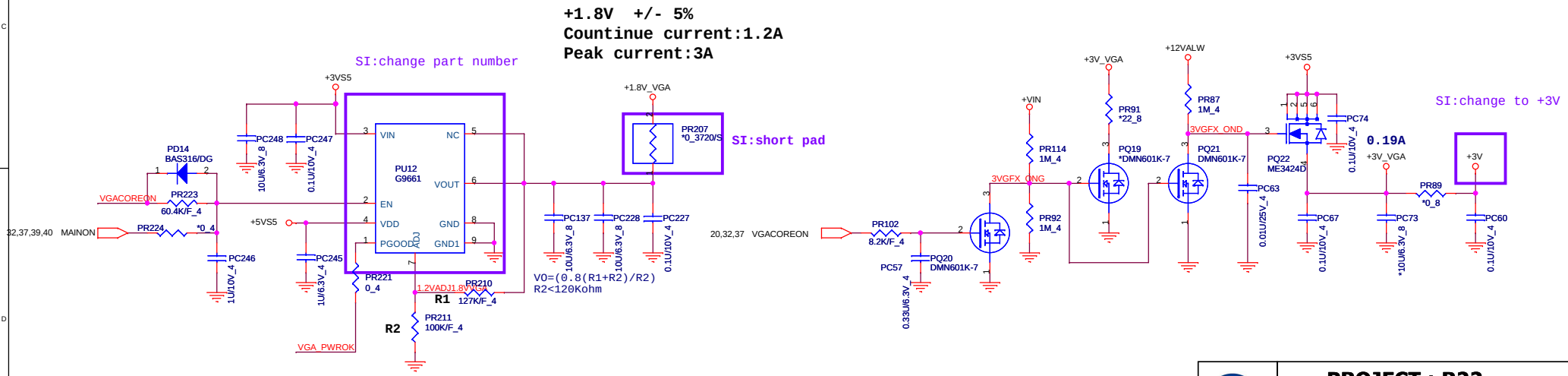


NB5/RD2	PROJECT : R22 Quanta Computer Inc. SANTOS INTEL	
Size	Document Number DDR3 (RT8207)	Rev 1A
Date: Wednesday, September 15, 2010	Sheet 37 of 43	

VGA Core

Park-LP	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1.0V
H	1	0	1.1V
TBD	1	1	NA





NB5/RD2	PROJECT : R22 Quanta Computer Inc.	
	Size: Custom Document Number: +VGACORE (RT8208/1.8V)	Rev: 1A
	Date: Wednesday, September 15, 2010 Sheet 38 of 43	

+0.9V +/- 5%
Countinue current:1.5A
Peak current:2A

SI:change part number

+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA

+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

SI:change part number

SI:change part number

SI:short pad

SI:short pad

R1 VO=(0.8(R1+R2)/R2)
R2 R2<120Kohm

R1 VO=(0.8(R1+R2)/R2)
R2 R2<120Kohm

R1
R2 Vout=1.2(1+R1/R2)

VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

5.2A
0.4A
0.7A
5.1A
2.35A

PU4 P2806
PU10 G9661
PU9 G9661
PU11 G917
PQ51 AON7410
PQ31 AON7410
PQ6 AON7410
PQ3 ME3424D
PQ15 ME3424D
PQ29 DMN601K-7
PQ4 *DMN601K-7
PQ10 *DMN601K-7

N85/RD2
PROJECT : R22
Quanta Computer Inc.
Size Custom
Document Number Dis-charge IC (G5934)
Rev 1A
Date: Wednesday, September 15, 2010 Sheet 39 of 43

SI:change part number & footprint

DC_JACK
90W

Place this ZVS close to Idea Diode

Do Not add test pad on BATDIS_G signal

To PWR LED

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

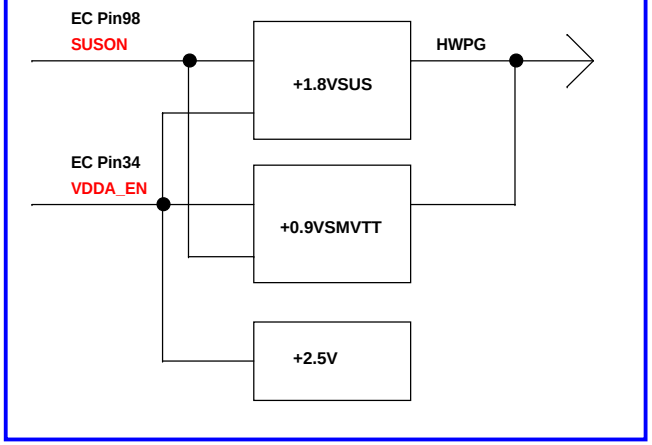
Place this cap close to EC

Place this cap close to EC

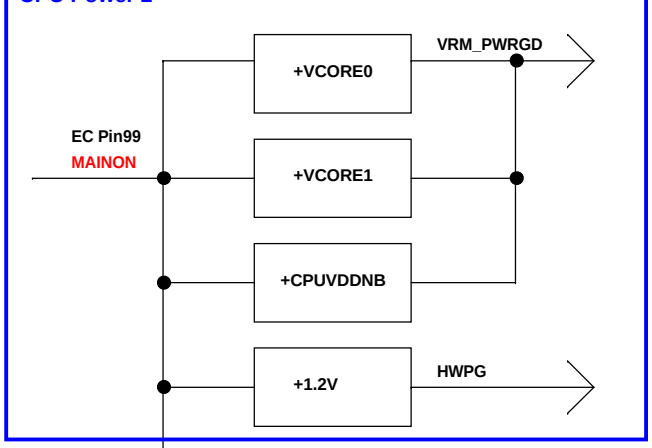
PU8
OZ8681

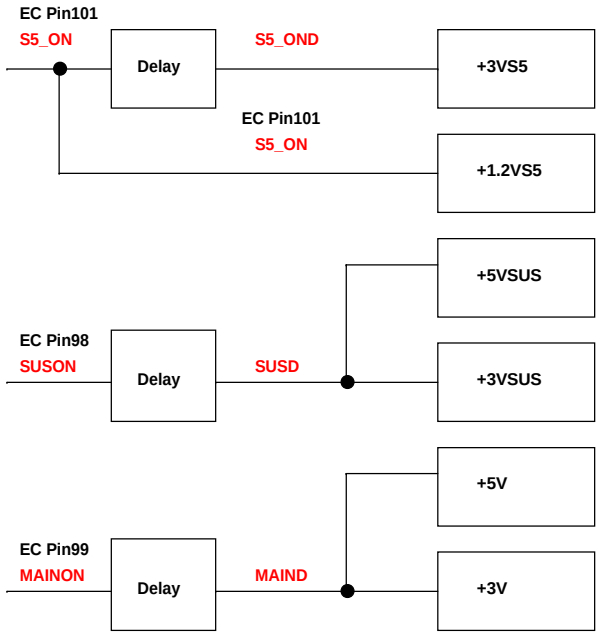
PROJECT : R22	
Quanta Computer Inc.	
Size: Custom	Document Number: CHARGER (ISL6251)
Rev: 1A	
Date: Wednesday, September 15, 2010	Sheet 40 of 43
N85/RD2	

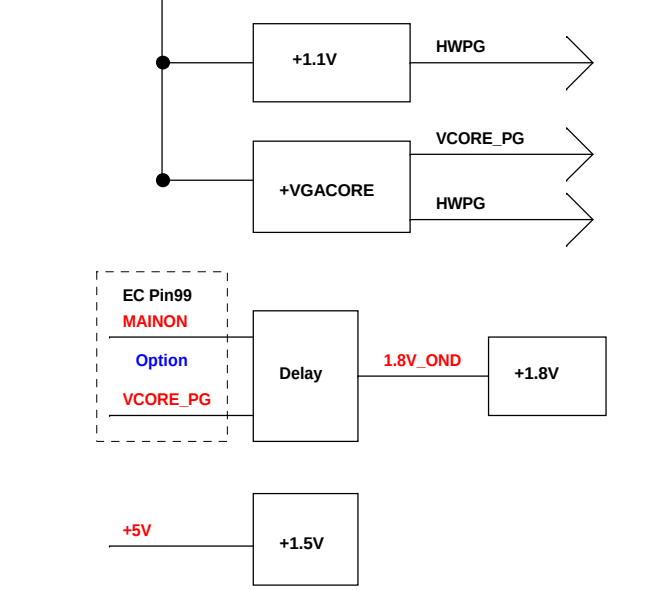
CPU Power 1



CPU Power 2







1 S5_ON, S5_OND, RSMRST# → 2 SUSON, SUSD → 3 MAINON, MAIND → 4 HWPG, VCORE_PG, VRM_PWRGD → EC Pin76 ECPWROK, Delay 600ms → SB_PWRGD_IN, 3.3V → NB_PWRGD_IN, 1.8V

NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power control	3A

Date: Wednesday, September 15, 2010 Sheet 41 of 43

Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER（3_3V）	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

Custom<Doc>
NB5/RD2

PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev
		1A

Date: Wednesday, September 15, 2010 Sheet 42 of 43