Compal Confidential

G400/G500 UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

2013-02-27

LA-9632P

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-9632P	Rev: 1.0
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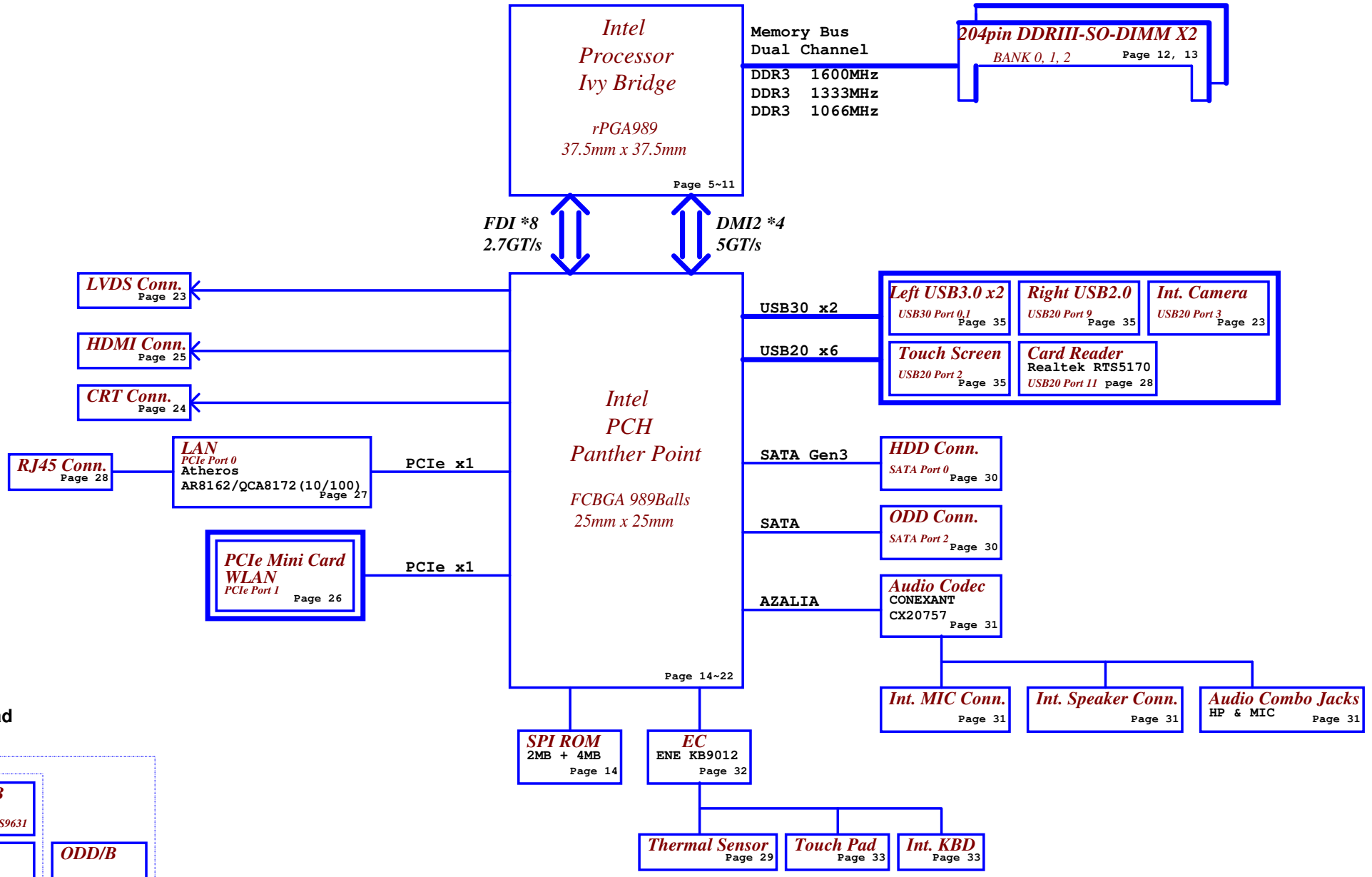
Chief River



Sub-borad

15"
14"

- Power/B (LID) LS9631
- USB/B LS9632
- ODD/B LS9634
- IO/B (Card Reader) LS9633
- Switch/B (LED, LID) LS9635

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: MB Block Diagram			
Size: Custom	Document Number: LA-9632P		Rev: 1.0
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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V
R694	100K +/- 1%

Board ID / SKU ID Table for AD channel

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0 V	0x00 ~ 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C ~ 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D ~ 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 ~ 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h
DDR_JDIMM2	1010 010x	A4h

AMD-GPU SM Bus address

Device	Address	
Internal thermal sensor	0100 0001	41h

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76,HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VGS	X	X	X	X	V +3VS	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X	V +3VS	X

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Issued Date	2011/06/15	Deciphered Date 2012/07/11	Title: Notes List

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Title: VGA Notes List

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ZZZ1 14@

14" UMA_PCB_LA9632P
DA6000WP000
PCB 0Y0 LA-9632P REV0 M/B UMA 3

ZZZ2 15@

15" UMA_PCB_LA9632P
DA6000WPT00
PCB 0Y0 LA-9632P REV0 M/B UMA 5

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

+V1.05S_VCCP

R1 24.9_0402_1%

PEG_COMP

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

JCPU1A

DMI

<16> DMI_CRX_PTX_N0 B27 DMI_RX#[0]
<16> DMI_CRX_PTX_N1 B25 DMI_RX#[1]
<16> DMI_CRX_PTX_N2 A25 DMI_RX#[2]
<16> DMI_CRX_PTX_N3 B24 DMI_RX#[3]

<16> DMI_CRX_PTX_P0 B28 DMI_RX[0]
<16> DMI_CRX_PTX_P1 B26 DMI_RX[1]
<16> DMI_CRX_PTX_P2 A24 DMI_RX[2]
<16> DMI_CRX_PTX_P3 B23 DMI_RX[3]

<16> DMI_CTX_PRX_N0 G21 DMI_TX#[0]
<16> DMI_CTX_PRX_N1 E22 DMI_TX#[1]
<16> DMI_CTX_PRX_N2 F21 DMI_TX#[2]
<16> DMI_CTX_PRX_N3 D21 DMI_TX#[3]

<16> DMI_CTX_PRX_P0 G22 DMI_TX[0]
<16> DMI_CTX_PRX_P1 D22 DMI_TX[1]
<16> DMI_CTX_PRX_P2 F20 DMI_TX[2]
<16> DMI_CTX_PRX_P3 C21 DMI_TX[3]

Intel(R) FDI

<16> FDI_CTX_PRX_N0 A21 FDI0_TX#[0]
<16> FDI_CTX_PRX_N1 H19 FDI0_TX#[1]
<16> FDI_CTX_PRX_N2 E19 FDI0_TX#[2]
<16> FDI_CTX_PRX_N3 F18 FDI0_TX#[3]
<16> FDI_CTX_PRX_N4 B21 FDI1_TX#[0]
<16> FDI_CTX_PRX_N5 C20 FDI1_TX#[1]
<16> FDI_CTX_PRX_N6 D18 FDI1_TX#[2]
<16> FDI_CTX_PRX_N7 E17 FDI1_TX#[3]

<16> FDI_CTX_PRX_P0 A22 FDI0_TX[0]
<16> FDI_CTX_PRX_P1 G19 FDI0_TX[1]
<16> FDI_CTX_PRX_P2 E20 FDI0_TX[2]
<16> FDI_CTX_PRX_P3 G18 FDI0_TX[3]
<16> FDI_CTX_PRX_P4 B20 FDI1_TX[0]
<16> FDI_CTX_PRX_P5 C19 FDI1_TX[1]
<16> FDI_CTX_PRX_P6 D19 FDI1_TX[2]
<16> FDI_CTX_PRX_P7 F17 FDI1_TX[3]

<16> FDI_FSYNC0 J18 FDI0_FSYNC
<16> FDI_FSYNC1 J17 FDI1_FSYNC

<16> FDI_INT H20 FDI_INT

<16> FDI_LSYNC0 J19 FDI0_LSYNC
<16> FDI_LSYNC1 H17 FDI1_LSYNC

+V1.05S_VCCP

R7 24.9_0402_1%

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

EDP_COMP A18 eDP_COMPIO
A17 eDP_ICOMPO
eDP_HPD B16 eDP_HPD#

eDP

C15 D15 eDP_AUX eDP_AUX#

C17 F16 C16 G15 eDP_TX[0] eDP_TX[1] eDP_TX[2] eDP_TX[3]

C18 E16 D16 F15 eDP_TX#[0] eDP_TX#[1] eDP_TX#[2] eDP_TX#[3]

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_RX#[0] K33
PEG_RX#[1] M35
PEG_RX#[2] L34
PEG_RX#[3] J35
PEG_RX#[4] J32
PEG_RX#[5] H34
PEG_RX#[6] H31
PEG_RX#[7] G33
PEG_RX#[8] G30
PEG_RX#[9] F35
PEG_RX#[10] E34
PEG_RX#[11] E32
PEG_RX#[12] D33
PEG_RX#[13] D31
PEG_RX#[14] B33
PEG_RX#[15] C32

PEG_RX[0] J33
PEG_RX[1] L35
PEG_RX[2] K34
PEG_RX[3] H35
PEG_RX[4] H32
PEG_RX[5] G34
PEG_RX[6] G31
PEG_RX[7] F33
PEG_RX[8] F30
PEG_RX[9] E35
PEG_RX[10] E33
PEG_RX[11] F32
PEG_RX[12] D34
PEG_RX[13] E31
PEG_RX[14] C33
PEG_RX[15] B32

PEG_TX#[0] M29
PEG_TX#[1] M32
PEG_TX#[2] M31
PEG_TX#[3] L32
PEG_TX#[4] L29
PEG_TX#[5] K31
PEG_TX#[6] K28
PEG_TX#[7] J30
PEG_TX#[8] J28
PEG_TX#[9] H29
PEG_TX#[10] G27
PEG_TX#[11] E29
PEG_TX#[12] F27
PEG_TX#[13] D28
PEG_TX#[14] F26
PEG_TX#[15] E25

PEG_TX[0] M28
PEG_TX[1] M33
PEG_TX[2] M30
PEG_TX[3] L31
PEG_TX[4] L28
PEG_TX[5] K30
PEG_TX[6] K27
PEG_TX[7] J29
PEG_TX[8] J27
PEG_TX[9] H28
PEG_TX[10] G28
PEG_TX[11] E28
PEG_TX[12] F28
PEG_TX[13] D27
PEG_TX[14] E26
PEG_TX[15] D25

TYCO_2013620-2_IVY BRIDGE

ME@

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: Custom | Document Number: LA-9632P | Rev: 1.0

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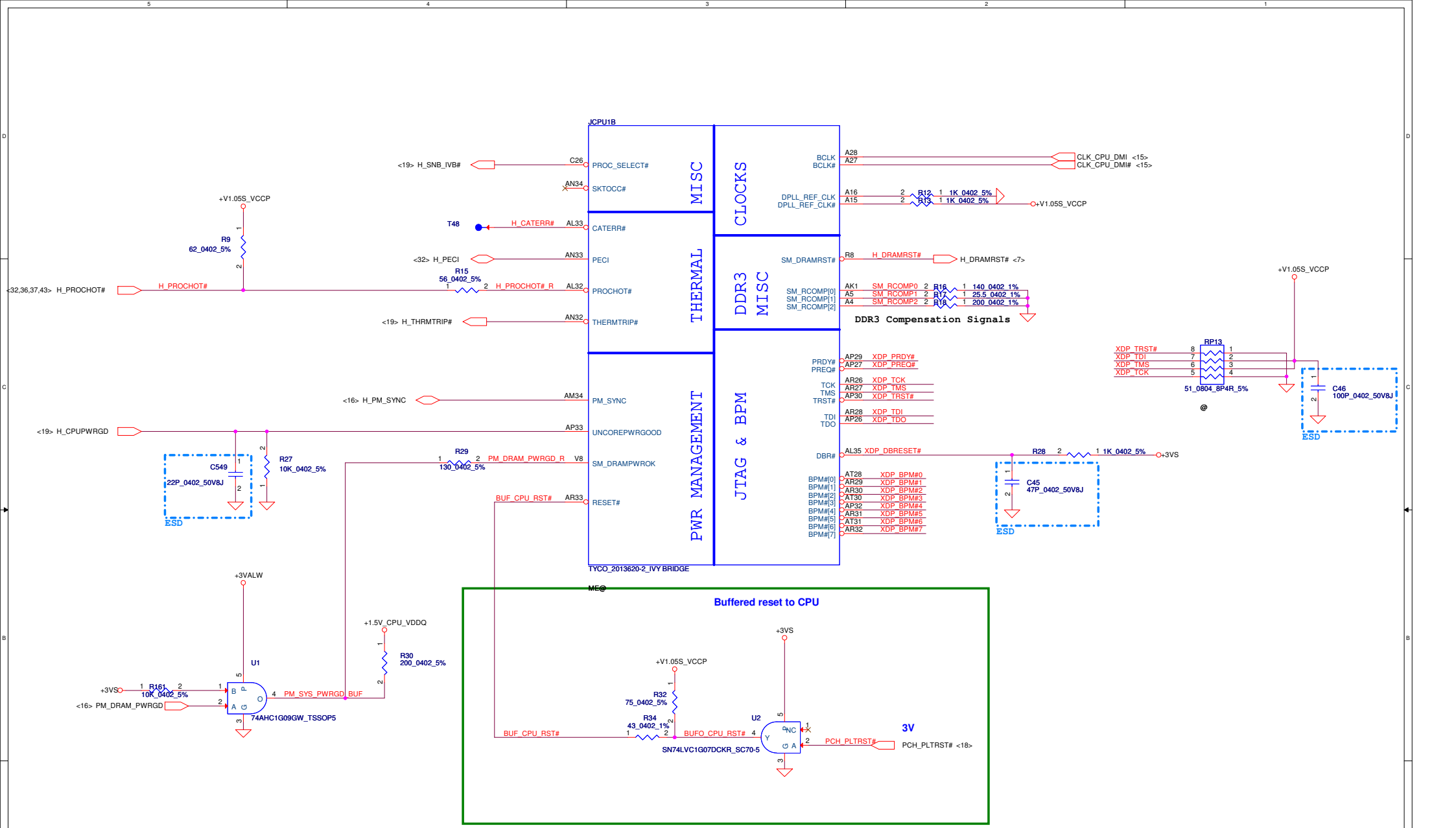
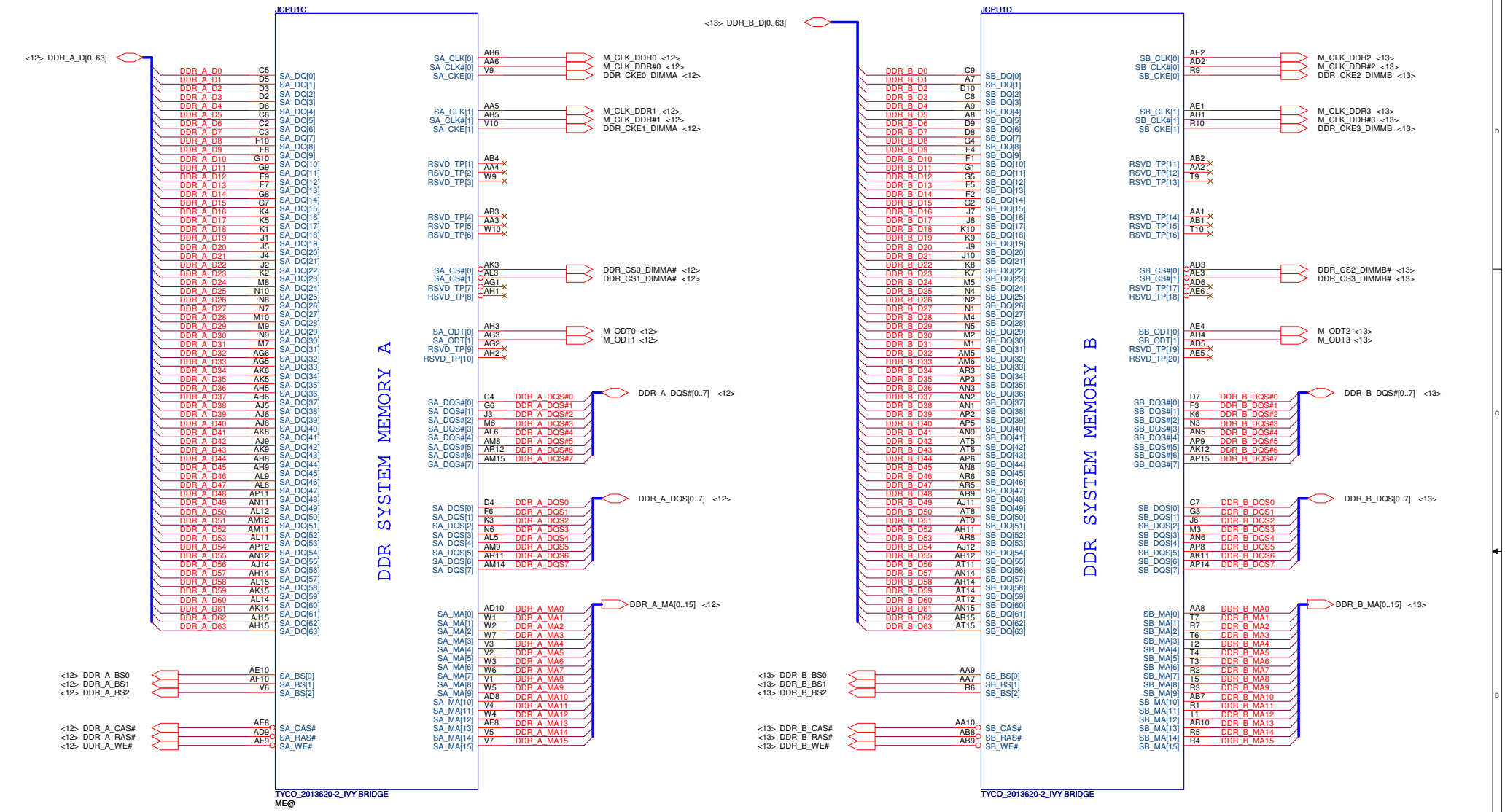


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: PROCESSOR(2/7) PM,XDP,CLK			
Size: Custom	Document Number: LA-9632P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 6 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: LA-9632P | Rev: 1.0

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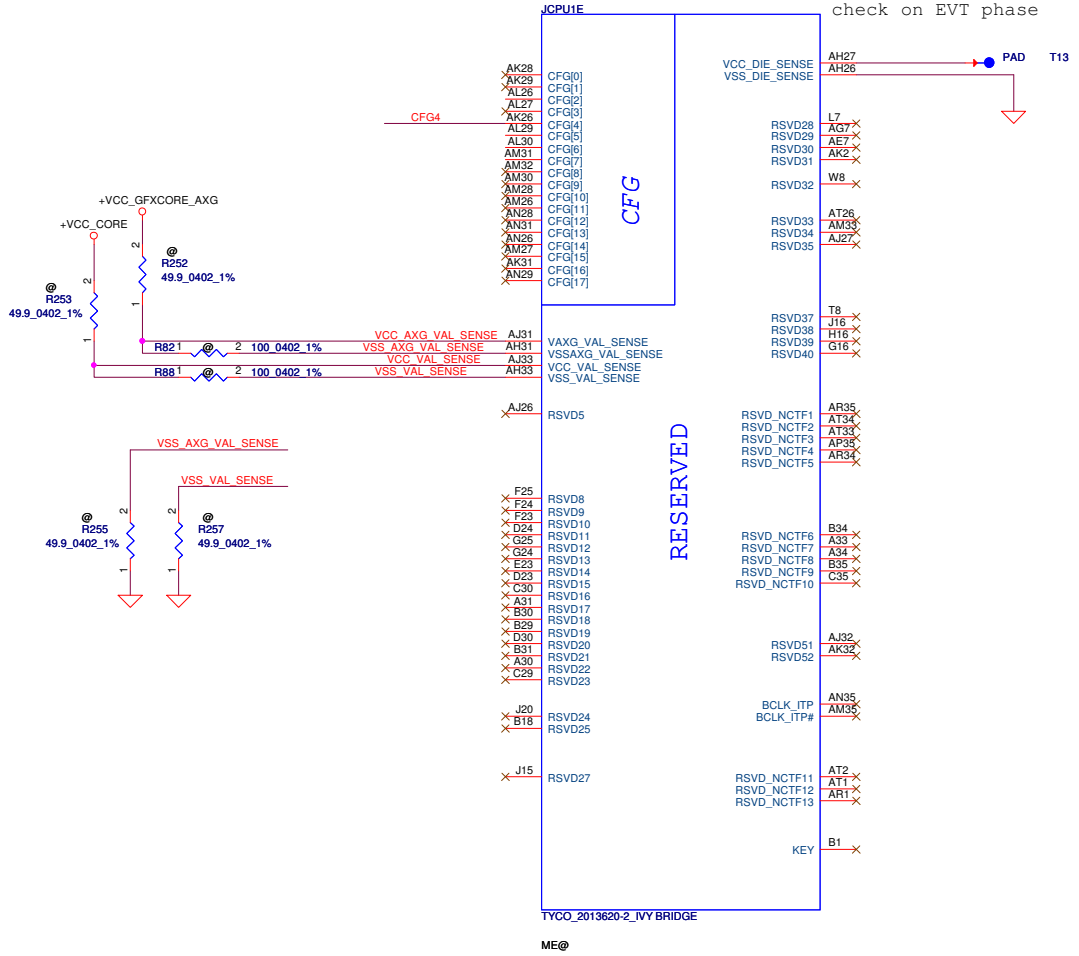
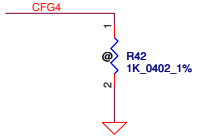
CFG Straps for Processor

Interl request AH26 short GND
check on EVT phase



PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-9632P | Rev: 1.0

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

AG35	VCC1	VCCIO1	AH13
AG34	VCC2	VCCIO2	AH10
AG33	VCC3	VCCIO3	AG10
AG32	VCC4	VCCIO4	AC10
AG31	VCC5	VCCIO5	Y10
AG30	VCC6	VCCIO6	U10
AG29	VCC7	VCCIO7	P10
AG28	VCC8	VCCIO8	L10
AG27	VCC9	VCCIO9	J14
AG26	VCC10	VCCIO10	J13
AF35	VCC11	VCCIO11	J12
AF34	VCC12	VCCIO12	J11
AF33	VCC13	VCCIO13	H14
AF32	VCC14	VCCIO14	H12
AF31	VCC15	VCCIO15	H11
AF30	VCC16	VCCIO16	G14
AF29	VCC17	VCCIO17	G13
AF28	VCC18	VCCIO18	G12
AF27	VCC19	VCCIO19	F14
AF26	VCC20	VCCIO20	F13
AD35	VCC21	VCCIO21	F12
AD34	VCC22	VCCIO22	F11
AD33	VCC23	VCCIO23	E14
AD32	VCC24	VCCIO24	E12
AD31	VCC25		
AD30	VCC26	VCCIO25	E11
AD29	VCC27	VCCIO26	D14
AD28	VCC28	VCCIO27	D13
AD27	VCC29	VCCIO28	D12
AD26	VCC30	VCCIO29	D11
AC35	VCC31	VCCIO30	C14
AC34	VCC32	VCCIO31	C13
AC33	VCC33	VCCIO32	C12
AC32	VCC34	VCCIO33	C11
AC31	VCC35	VCCIO34	B14
AC30	VCC36	VCCIO35	B12
AC29	VCC37	VCCIO36	A14
AC28	VCC38	VCCIO37	A13
AC27	VCC39	VCCIO38	A12
AC26	VCC40	VCCIO39	A11
AA35	VCC41		
AA34	VCC42	VCCIO40	J23
AA33	VCC43		
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
V28	VCC68		
V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

TYCO_2013620-2_IVY BRIDGE

ME@

+V1.05S_VCCP

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# 1 R47 2 43_0402_5% VR_SVID_ALRT# <43>
VIDSCLK AJ30 VR_SVID_CLK <43>
VIDSOUT AJ28 VR_SVID_DAT <43>

R50 2 1 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51
100_0402_1%

VCC_SENSE AJ35 VCCSENSE <43>
VSS_SENSE AJ34 VSSSENSE <43>

R54
100_0402_1%

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10 VSSIO_SENSE_L 1 R74 2 VSSIO_SENSE 10_0402_1% VCCIO_SENSE <42>

R74 & R79 put together

+V1.05S_VCCP

R79
2 1
10_0402_1%

VSSIO_SENSE_L <42>

VSS_SENCE 100ohm +-1% pull-down to GND near processor

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PROCESSOR(5/7) PWR,BYPASS

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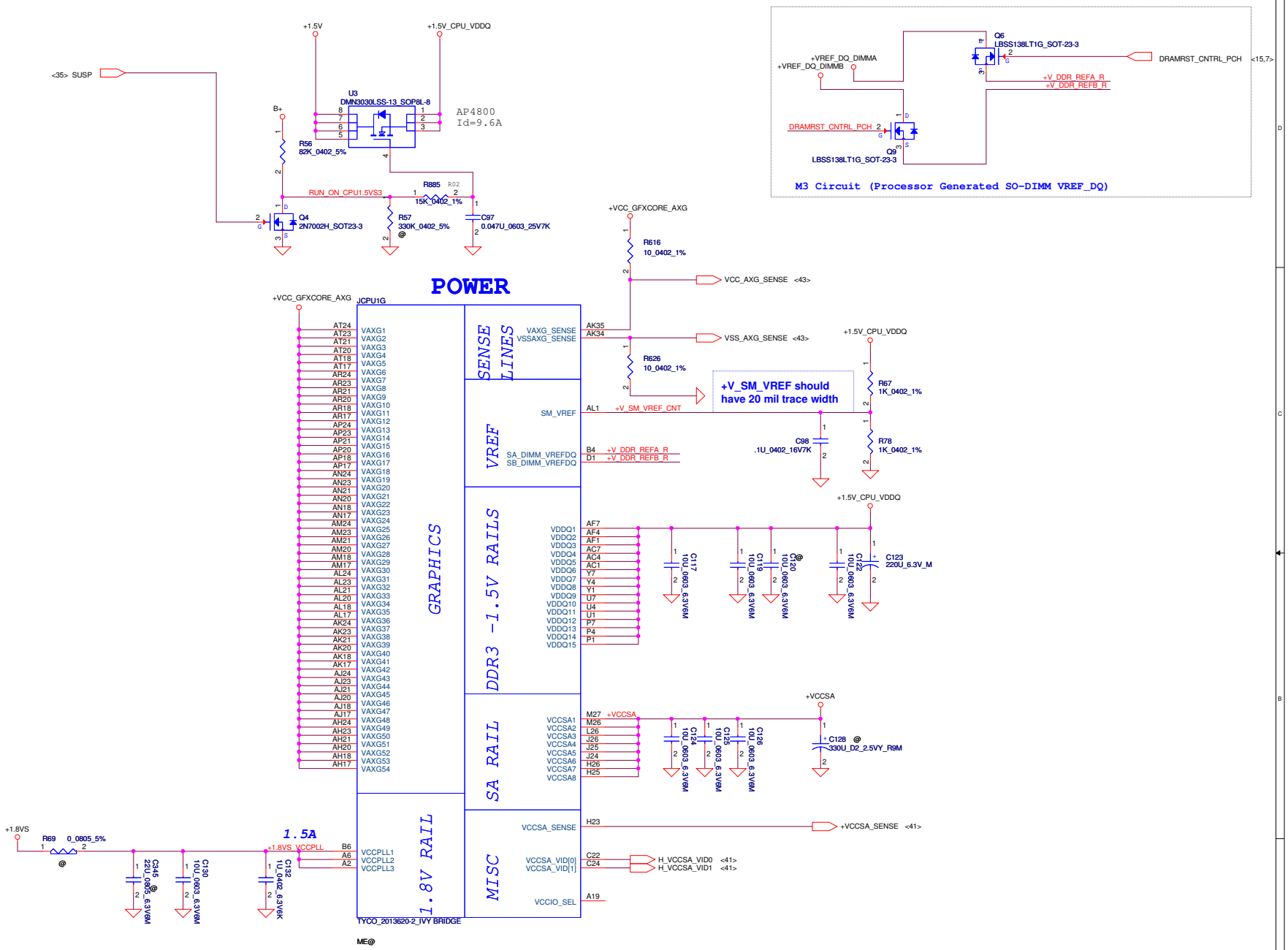
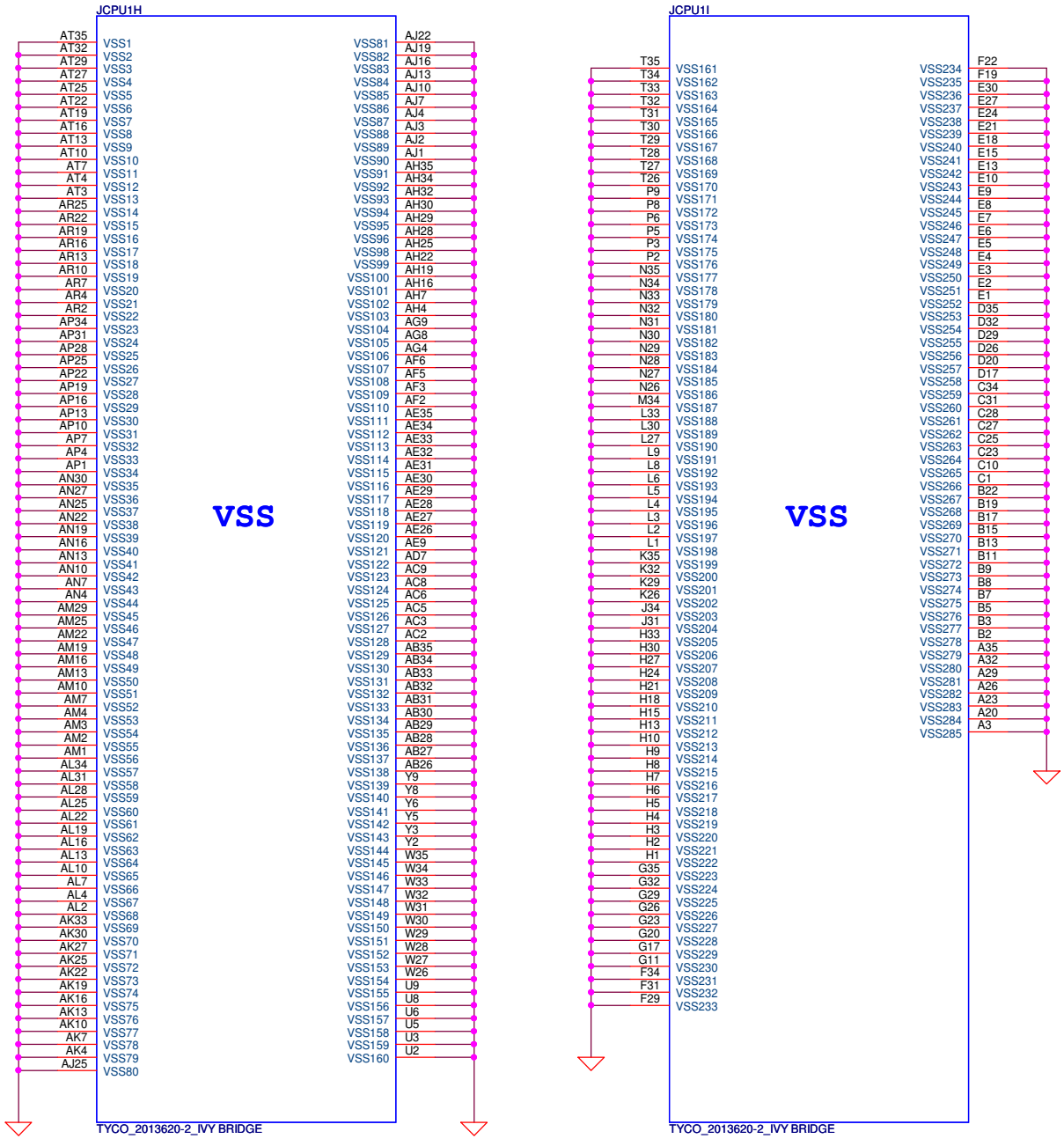


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: LA-9632P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 10 of 60		



ME@

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-9632P	1.0

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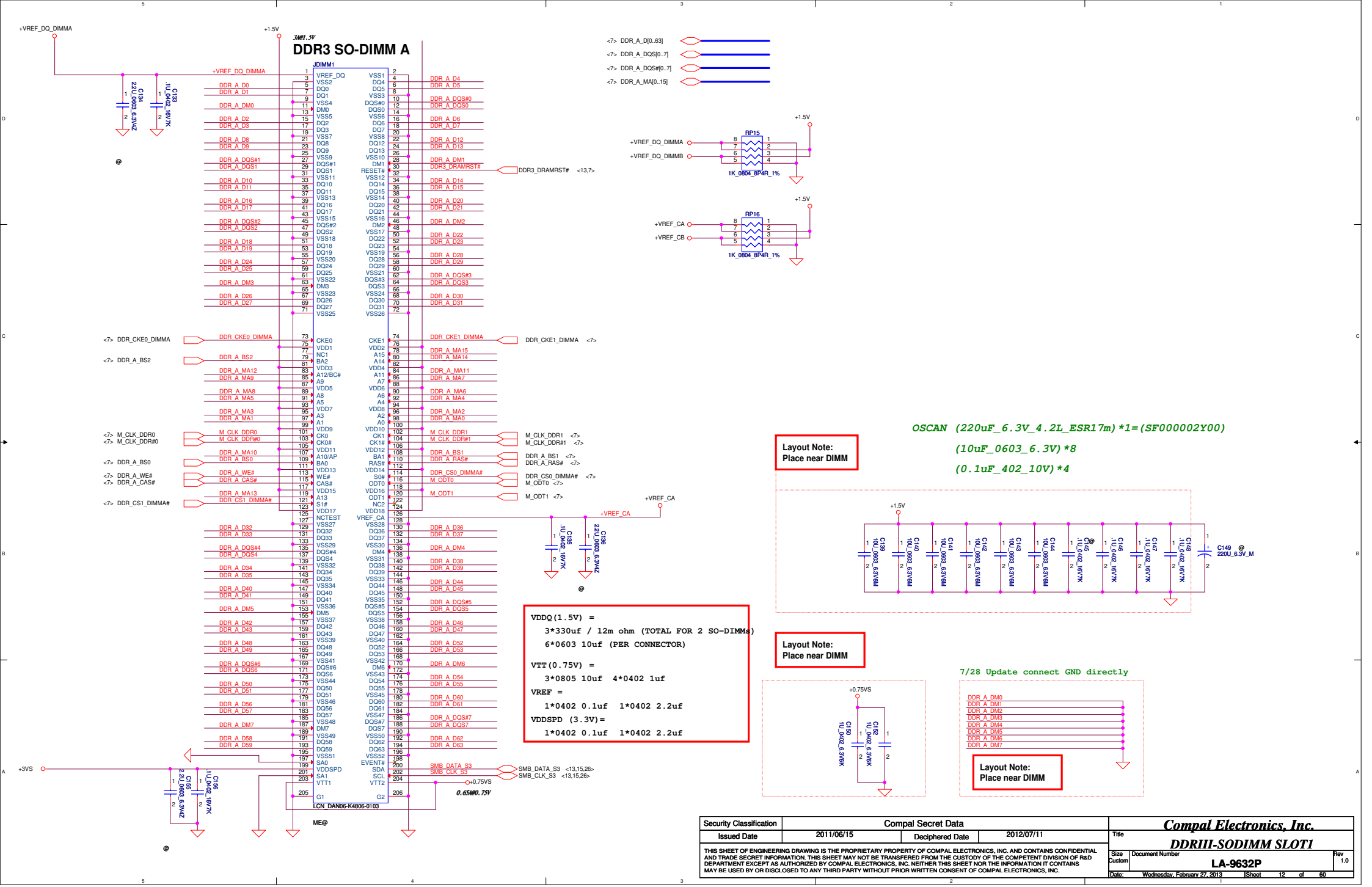


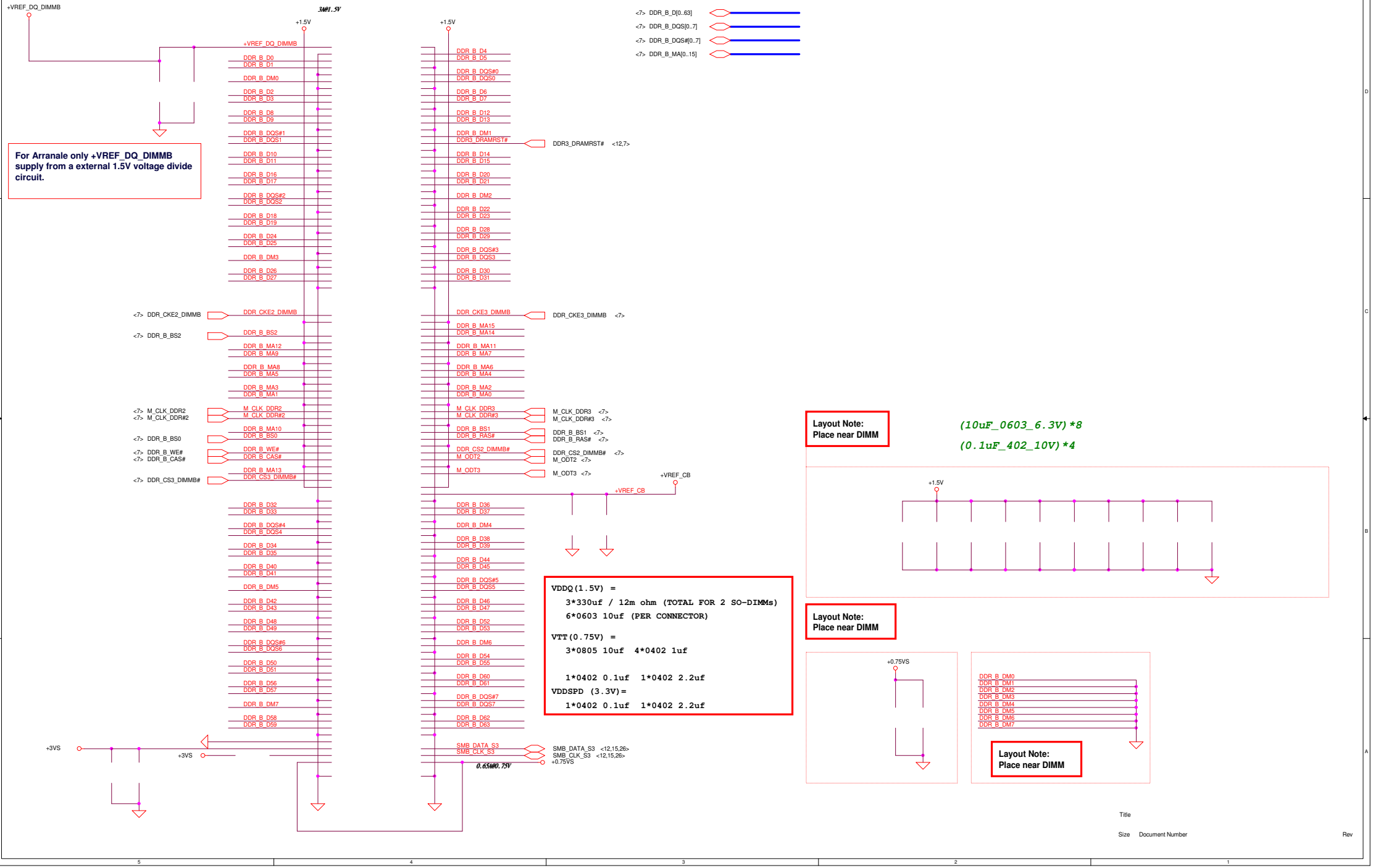
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 Sheet 12 of 60


+VREF_DQ_DIMMB
+1.5V
+VREF_DQ_DIMMB
For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
DDR_B_D0
DDR_B_D1
DDR_B_DM0
DDR_B_D2
DDR_B_D3
DDR_B_D8
DDR_B_D9
DDR_B_DQS#1
DDR_B_DQS1
DDR_B_D10
DDR_B_D11
DDR_B_D16
DDR_B_D17
DDR_B_DQS#2
DDR_B_DQS2
DDR_B_D18
DDR_B_D19
DDR_B_D24
DDR_B_D25
DDR_B_DM3
DDR_B_D26
DDR_B_D27
<7> DDR_CKE2_DIMMB
DDR_CKE2_DIMMB
<7> DDR_B_BS2
DDR_B_BS2
DDR_B_MA12
DDR_B_MA9
DDR_B_MA8
DDR_B_MA5
DDR_B_MA3
DDR_B_MA1
<7> M_CLK_DDR2
<7> M_CLK_DDR#2
M_CLK_DDR2
M_CLK_DDR#2
DDR_B_MA10
DDR_B_BS0
<7> DDR_B_BS0
<7> DDR_B_WE#
<7> DDR_B_CAS#
DDR_B_WE#
DDR_B_CAS#
DDR_B_MA13
DDR_CS3_DIMMB#
<7> DDR_CS3_DIMMB#
DDR_B_D32
DDR_B_D33
DDR_B_DQS#4
DDR_B_DQS4
DDR_B_D34
DDR_B_D35
DDR_B_D40
DDR_B_D41
DDR_B_DM5
DDR_B_D42
DDR_B_D43
DDR_B_D48
DDR_B_D49
DDR_B_DQS#6
DDR_B_DQS6
DDR_B_D50
DDR_B_D51
DDR_B_D56
DDR_B_D57
DDR_B_DM7
DDR_B_D58
DDR_B_D59
+3VS
+3VS
+1.5V
DDR_B_D4
DDR_B_D5
DDR_B_DQS#0
DDR_B_DQS0
DDR_B_D6
DDR_B_D7
DDR_B_D12
DDR_B_D13
DDR_B_DM1
DDR3_DRAMRST#
DDR3_DRAMRST# <12,7>
DDR_B_D14
DDR_B_D15
DDR_B_D20
DDR_B_D21
DDR_B_DM2
DDR_B_D22
DDR_B_D23
DDR_B_D28
DDR_B_D29
DDR_B_DQS#3
DDR_B_DQS3
DDR_B_D30
DDR_B_D31
DDR_CKE3_DIMMB
DDR_CKE3_DIMMB <7>
DDR_B_MA15
DDR_B_MA14
DDR_B_MA11
DDR_B_MA7
DDR_B_MA6
DDR_B_MA4
DDR_B_MA2
DDR_B_MA0
M_CLK_DDR3 <7>
M_CLK_DDR#3 <7>
M_CLK_DDR3
M_CLK_DDR#3
DDR_B_BS1 <7>
DDR_B_RAS# <7>
DDR_B_BS1
DDR_B_RAS#
DDR_CS2_DIMMB#
DDR_CS2_DIMMB# <7>
M_ODT2 <7>
M_ODT2
M_ODT3 <7>
M_ODT3
+VREF_CB
+VREF_CB
DDR_B_D36
DDR_B_D37
DDR_B_DM4
DDR_B_D38
DDR_B_D39
DDR_B_D44
DDR_B_D45
DDR_B_DQS#5
DDR_B_DQS5
DDR_B_D46
DDR_B_D47
DDR_B_D52
DDR_B_D53
DDR_B_DM6
DDR_B_D54
DDR_B_D55
DDR_B_D60
DDR_B_D61
DDR_B_DQS#7
DDR_B_DQS7
DDR_B_D62
DDR_B_D63
SMB_DATA_S3
SMB_CLK_S3
SMB_DATA_S3 <12,15,26>
SMB_CLK_S3 <12,15,26>
+0.75VS
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_MA[0..15]
VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)
VTT(0.75V) =
3*0805 10uf 4*0402 1uf
1*0402 0.1uf 1*0402 2.2uf
VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf
Layout Note:
Place near DIMM
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4
+1.5V
Layout Note:
Place near DIMM
+0.75VS
DDR_B_DM0
DDR_B_DM1
DDR_B_DM2
DDR_B_DM3
DDR_B_DM4
DDR_B_DM5
DDR_B_DM6
DDR_B_DM7
Layout Note:
Place near DIMM
Title
Size
Document Number
Rev

CLRP2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CLRP3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

W=20mils +RTCVCC — R99 1K_0402_5% — W=20mils +RTCBATT — C179 1U_0603_10V4Z

PCH_RTCX1 — R98 10M_0402_5% — PCH_RTCX2 — R104 0_0402_5% — Y1 32.768KHZ_12.5PF_CM31532768DZFT — C180 18P_0402_50V8J — C181 18P_0402_50V8J

+RTCVCC — R101 1M_0402_5% SM_INTRUDER# — R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN

★ H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS — R105 @ 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
★ LOW= Disable (Default)

+3V_PCH — R106 @ 1K_0402_5% ME_FLASH

★ Low = Disable (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH — R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
★ 1.8V when sampled low
Needs to be pulled High for Chief River platfrom

DPDG1.1

CMOS

+RTCVCC — C183 1U_0603_10V4Z — R103 20K_0402_5% — R100 20K_0402_5% — C182 1U_0603_10V4Z

RP2 @ SHORT PADS — RP3 @ SHORT PADS

PCH_RTCX1 — PCH_RTCX2 — PCH_RTCRST# — PCH_SRTCRST# — SM_INTRUDER# — PCH_INTVRMEN

U4A

RTCX1	A20	RTC	
RTCX2	C20		
RTCRST#	D20		
SRTCRST#	G22		
INTRUDER#	K22		
INTVRMEN	C17		
HDA_BCLK	N34	IHDA	
HDA_SYNC	L34		
SPKR	T10		
HDA_RST#	K34		
HDA_SDIN0	E34		
HDA_SDIN1	G34		
HDA_SDIN2	C34		
HDA_SDIN3	A34		
HDA_SDO	A36		
HDA_DOCK_EN# / GPIO33	C36		
HDA_DOCK_RST# / GPIO13	N32		
JTAG_TCK	J3	JTAG	
JTAG_TMS	H7		
JTAG_TDI	K5		
JTAG_TDO	H1		
SPI_CLK	T3	SPI	
SPI_CS0#	Y14		
SPI_CS1#	T1		
SPI_MOSI	V4		
SPI_MISO	U3		

HDA_BIT_CLK — HDA_SYNC — HDA_RST# — HDA_SDO — HDA_JTAG_TCK — HDA_JTAG_TMS — HDA_JTAG_TDI — HDA_JTAG_TDO — SPI_CLK_PCH_R — SPI_SB_CS0# — SPI_SI — SPI_SO_R

<31> HDA_SPKR — <31> HDA_SDIN0 — <32> ME_FLASH

LPC	FWH0 / LAD0	C38	LPC_AD0
	FWH1 / LAD1	A38	LPC_AD1
	FWH2 / LAD2	B37	LPC_AD2
	FWH3 / LAD3	C37	LPC_AD3
	FWH4 / LFRAME#	D36	LPC_FRAME#
	LDRQ0#	E36	
	LDRQ1# / GPIO23	K36	
	SERIRQ	V5	SERIRQ
SATA 6G	SATA0RXN	AM3	SATA_DTX_C_IRX_N0
	SATA0RXP	AM1	SATA_DTX_C_IRX_P0
	SATA0TXN	AP7	SATA_ITX_C_DRX_N0
	SATA0TXP	AP5	SATA_ITX_C_DRX_P0
	SATA1RXN	AM10	
	SATA1RXP	AM8	
	SATA1TXN	AP11	
	SATA1TXP	AP10	
	SATA2RXN	AD7	SATA_DTX_C_IRX_N2
	SATA2RXP	AD5	SATA_DTX_C_IRX_P2
	SATA2TXN	AH5	SATA_ITX_C_DRX_N2
	SATA2TXP	AH4	SATA_ITX_C_DRX_P2
	SATA3RXN	AB8	
	SATA3RXP	AB10	
	SATA3TXN	AF3	
	SATA3TXP	AF1	
	SATA4RXN	Y7	
	SATA4RXP	Y5	
	SATA4TXN	AD3	
	SATA4TXP	AD1	
	SATA5RXN	Y3	
	SATA5RXP	Y1	
	SATA5TXN	AB3	
	SATA5TXP	AB1	
	SATAICOMPO	Y11	
	SATAICOMPI	Y10	SATA_COMP
	SATA3RCOMPO	AB12	
	SATA3COMPI	AB13	SATA3_COMP
	SATA3RBIAS	AH1	RBIAS_SATA3
	SATALED#	P3	SATALED#
	SATA0GP / GPIO21	V14	PCH_GPIO21
	SATA1GP / GPIO19	P1	BBS_BIT0_R

EC and Mini card debug port

LPC_AD0 <32> — LPC_AD1 <32> — LPC_AD2 <32> — LPC_AD3 <32> — LPC_FRAME# <32> — SERIRQ <32>

HDD: SATA_DTX_C_IRX_N0 <30> — SATA_DTX_C_IRX_P0 <30> — SATA_ITX_C_DRX_N0 <30> — SATA_ITX_C_DRX_P0 <30>

ODD: SATA_DTX_C_IRX_N2 <30> — SATA_DTX_C_IRX_P2 <30> — SATA_ITX_C_DRX_N2 <30> — SATA_ITX_C_DRX_P2 <30>

R111 37.4_0402_1% — +V1.05S_VCCP
R113 49.9_0402_1% — +V1.05S_VCCP
R115 750_0402_1%

PANTHER-POINT_FCBGA989
HM76@
SA00005FH70
S IC BD82HM76 SLJ8E C1 BGA 989P PCH C38!

<31> HDA_BITCLK_AUDIO — <31> HDA_SYNC_AUDIO — <31> HDA_RST_AUDIO# — <31> HDA_SDOUT_AUDIO

For EMI — RP12 33_0804_8P4R_5% — HDA_BIT_CLK — HDA_SYNC_R — HDA_RST# — ME_FLASH

+5VS — Q10 LBSS138LT1G_SOT-23-3 — HDA_SYNC — R878 1M_0402_5%

check with vender
Del Q10 check with codec
VDDIO using 3VALW

SPI_CLK_PCH_R — R124 33_0402_5% — C190 22P_0402_50V8J For EMI

R124;c190 close to U4.T3 pin

U4 HM70@
SA00005MQ80
IC BD82HM70 SJTNV C1 BGA 989P PCH C38!

U4 NM70@
SA00005WU60
S IC BD82NM70 SLJTA C1 BGA 989P PCH C38!

+3V_ROM — R127 3.3K_0402_5% SPI_WP# — R129 3.3K_0402_5% SPI_HOLD#

+3VS — RP17 10K_0804_8P4R_5% — BBS_BIT0_R — SATALED# — PCH_GPIO16 — SERIRQ — <19> PCH_GPIO16

Share ROM — RP2 0_0804_8P4R_5% — SPI_SO_R — SPI_SI — SPI_CLK_PCH_R — SPI_SB_CS0# — EC_SPI_SO — EC_SPI_SI — EC_SPI_CLK — EC_SPI_CS#

EC_SPI_SO <32> — EC_SPI_SI <32> — EC_SPI_CLK <32> — EC_SPI_CS# <32>

Share ROM — +3V_ROM

SPI_SB_CS0# — SPI_SO_R — R131 0_0402_5% — For EMI

U5 W25Q64FVSSIQ_SO8
SA000039A30
S IC FL 64M W25Q64FVSSIQ SOIC 8P SPI ROM

CS# — SO — WP# — GND — VCC — HOLD# — SCLK — SI

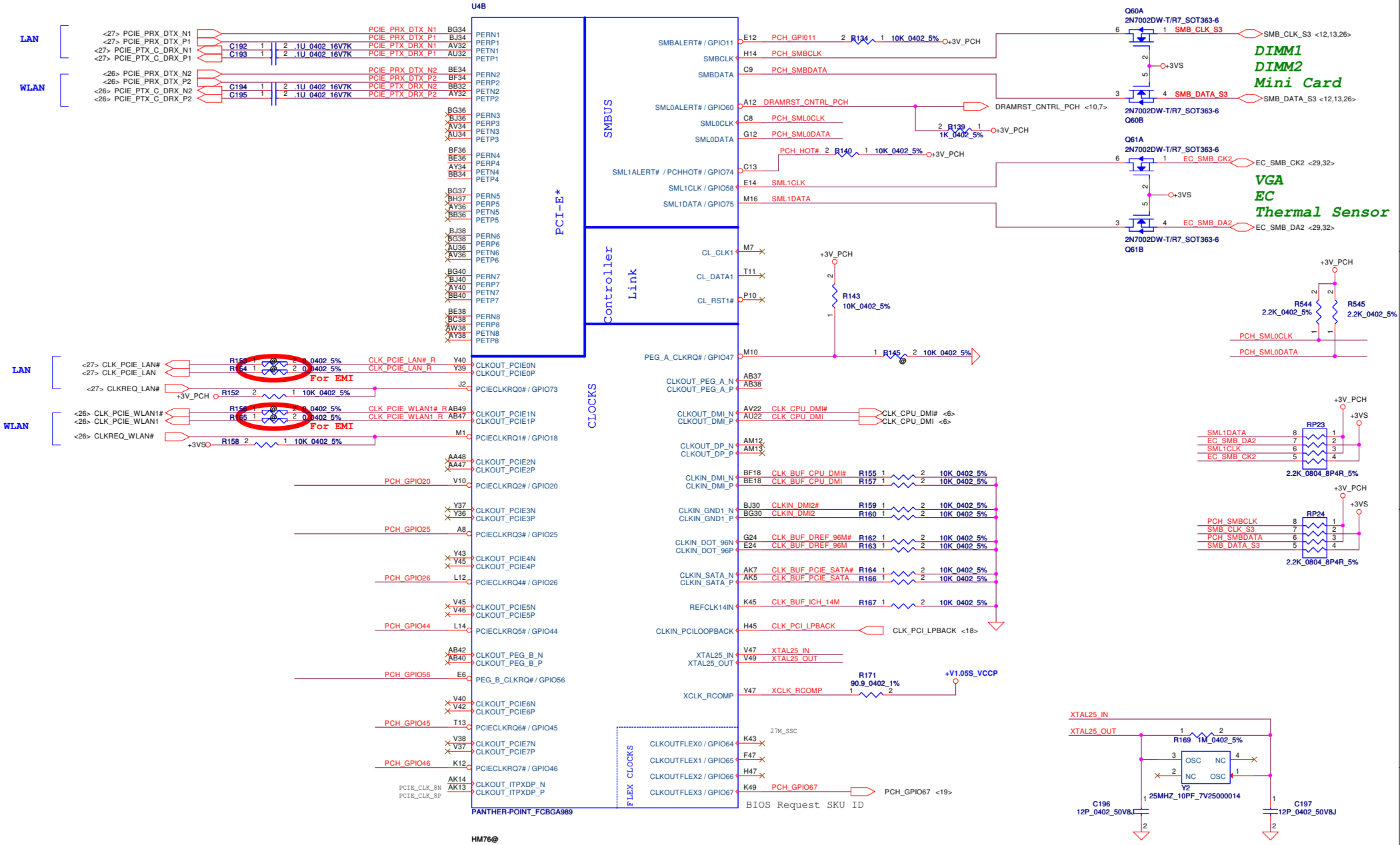
SPI_SO_L — SPI_WP# — SPI_HOLD# — SPI_CLK_1 — R132 0_0402_5% — SPI_CLK_PCH_R — SPI_SI — For EMI

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size: Custom — Document Number: LA-9632P — Rev: 1.0

Date: Wednesday, March 06, 2013 — Sheet 14 of 60



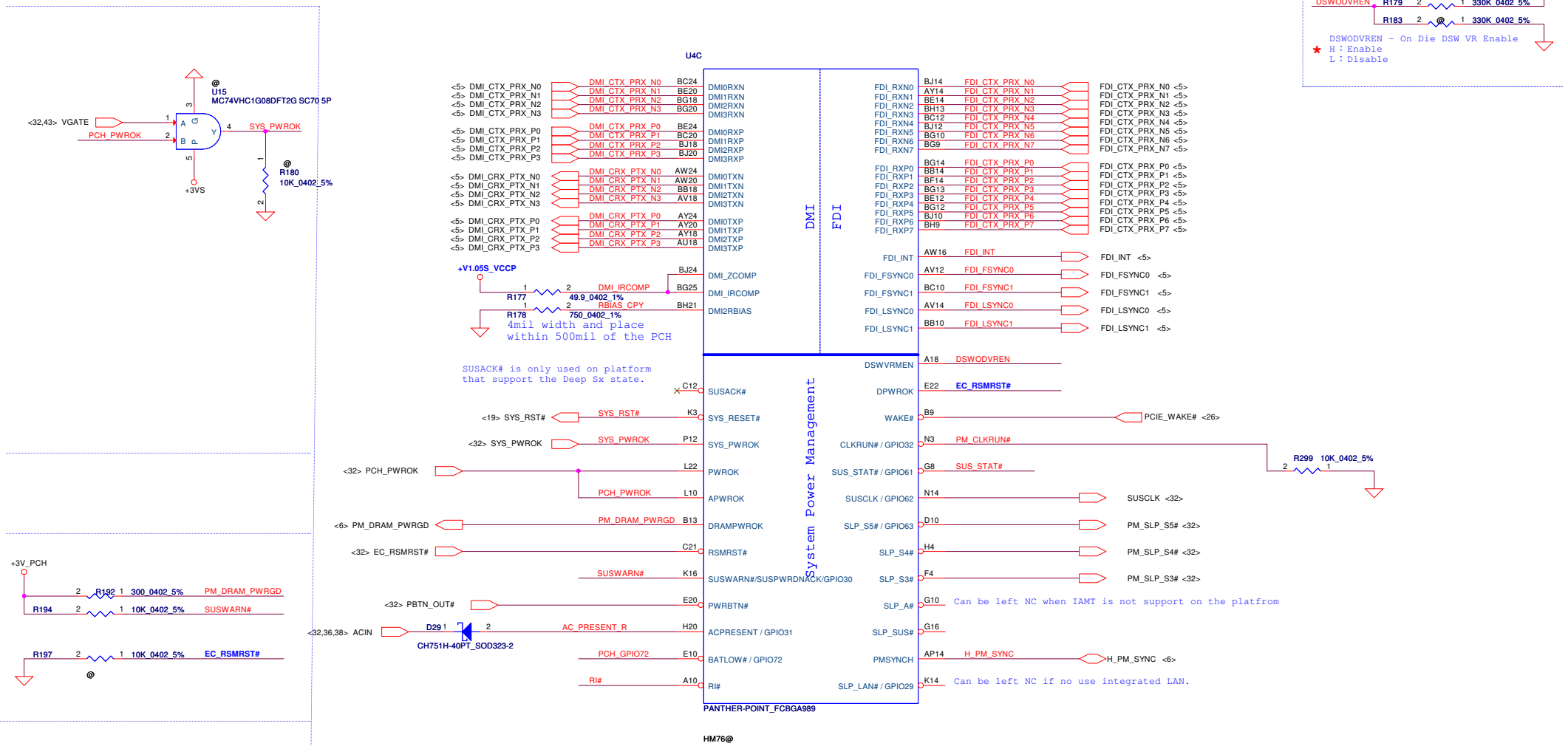
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 Sheet 15 of 60



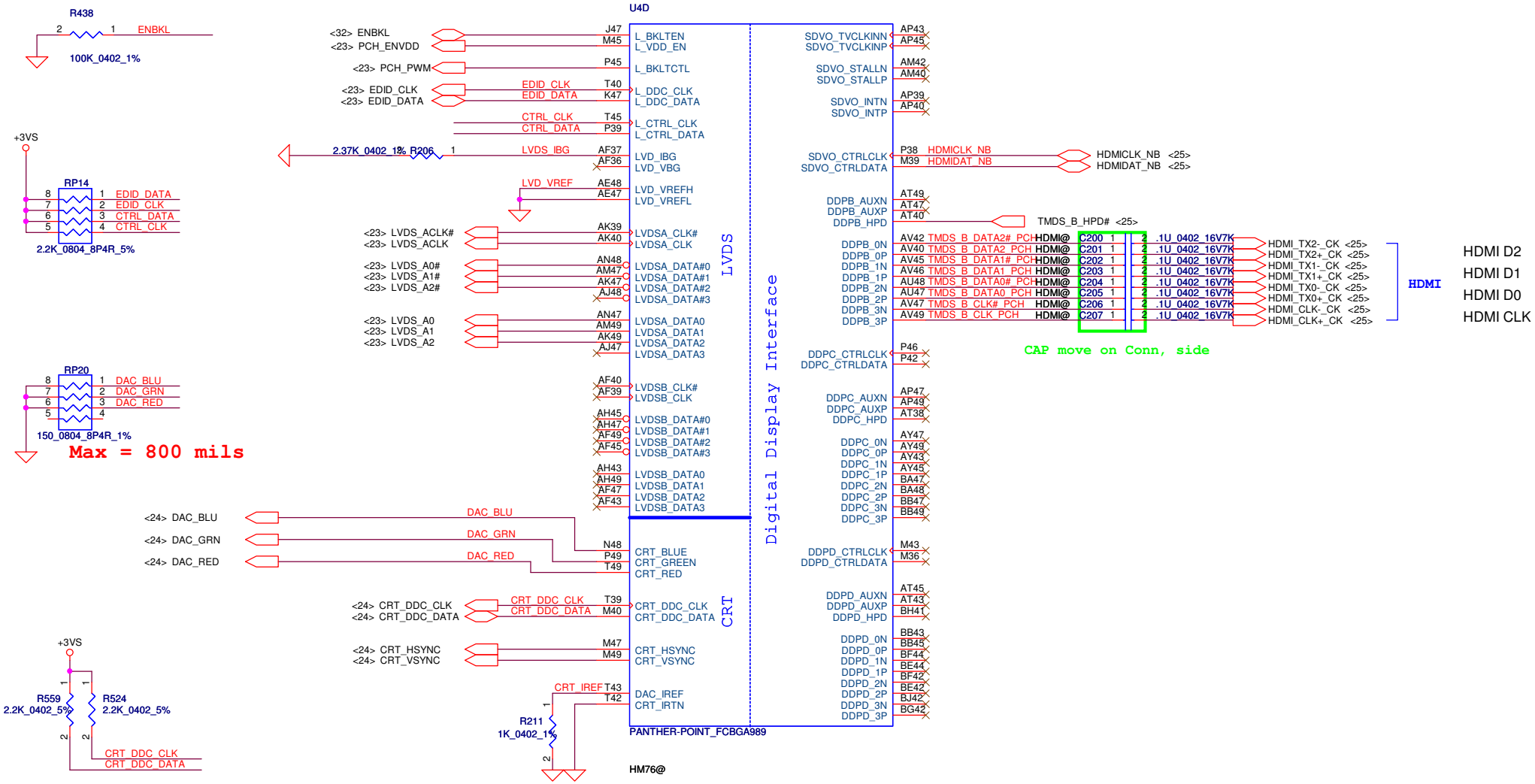
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 Sheet 16 of 60

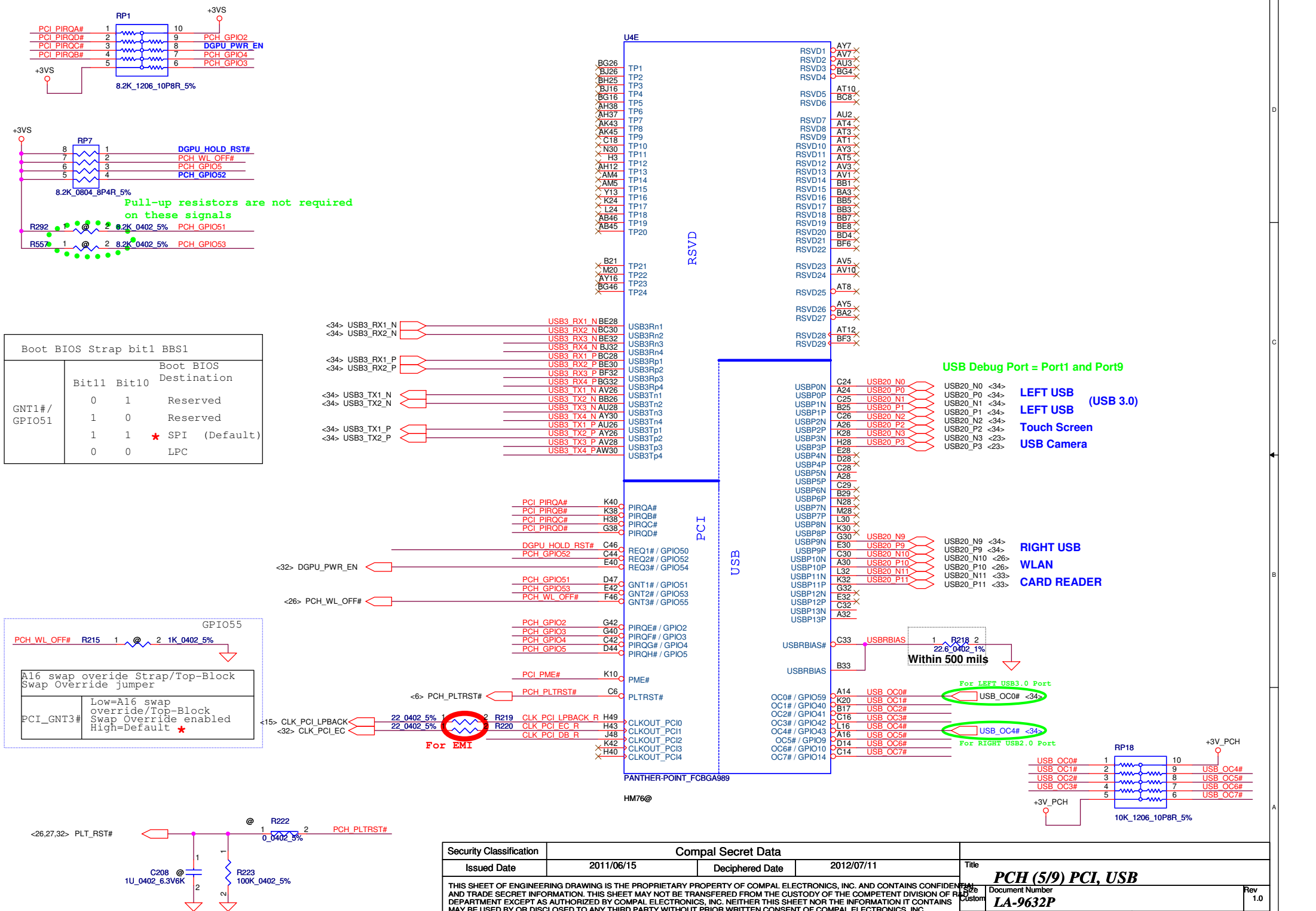


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: B | Document Number: LA-9632P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 17 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: **PCH (5/9) PCI, USB**

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 Sheet 18 of 60

PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76

PCH_GPIO71	Function
1	Mars XT
0	Sun Pro

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 10K_0402_5% PCH_GPIO27

GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.

R244 10K_0402_5% PCH_GPIO37
R881 10K_0402_5%
R250 10K_0402_5% PCH_GPIO36
R547 10K_0402_5%

BIOS Request SKU ID

R711 UMA@ 10K_0402_5%
R246 UMA@ 10K_0402_5%
PCH_GPIO38
PCH_GPIO67 PCH_GPIO67 <15>
R708 PX@ 10K_0402_5%
R295 PX@ 10K_0402_5%

RP10 10K_0804_8P4R_5%
PCH_GPIO39
SYS_RST# SYS_RST# <16>
PCH_BT_ON#
PCH_GPIO35

PCH_GPIO38	PCH_GPIO67	Function
0	0	SG(Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA

U4F

GPIO:
PCH_GPIO0 T7 BMBUSY# / GPIO0
PCH_GPIO1 A42 TACH1 / GPIO1
PCH_GPIO6 H36 TACH2 / GPIO6
<32> EC_SCI# EC_SCI# E38 TACH3 / GPIO7
<16,32> EC_SMI# EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
+3V_PCH R230 1K_0402_5% EC_LID_OUT# G2 GPIO15
<32> EC_LID_OUT#
<14> PCH_GPIO16 PCH_GPIO16 U2 SATA4GP / GPIO16
DGPU_PWROK D40 TACH0 / GPIO17
<26> PCH_BT_ON# PCH_BT_ON# T5 SCLOCK / GPIO22
+3V_PCH <30> ODD_EN ODD_EN E8 GPIO24
R241 10K_0402_5% PCH_GPIO27 E16 GPIO27
+3VS R242 10K_0402_5% PCH_GPIO28 P8 GPIO28
<26> INTEL_BT_OFF# INTEL_BT_OFF# K1 STP_PCI# / GPIO34
PCH_GPIO35 K4 GPIO35
PCH_GPIO36 V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
PCH_GPIO38 N2 SLOAD / GPIO38
PCH_GPIO39 M3 SDATAOUT0 / GPIO39
PCH_GPIO48 V13 SDATAOUT1 / GPIO48
PCH_GPIO49 V3 SATA5GP / GPIO49 / TEMP_ALERT#
PCH_GPIO57 D6 GPIO57

CPU/MISC:
TACH4 / GPIO68 C40 PCH_GPIO68
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71
A20GATE P4 GATEA20 <32>
PECI AU16
RCIN# P5 KBRST# KBRST# <32>
PROCPWRGD AY11 H_CPUPWRGD <6>
THRMTRIP# AY10 PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
INIT3_3V# T14
DF_TVS AY1
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

NCTF:
VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

PANTHER-POINT_FCBGA989

HM76@

R236 10K_0402_5%
KBRST# R226 10K_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
Weak internal PU,Do not pull low
CLOSE TO THE BRANCHING POINT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom | Document Number: LA-9632P | Rev: 1.0
Date: Wednesday, February 27, 2013 | Sheet 19 of 60

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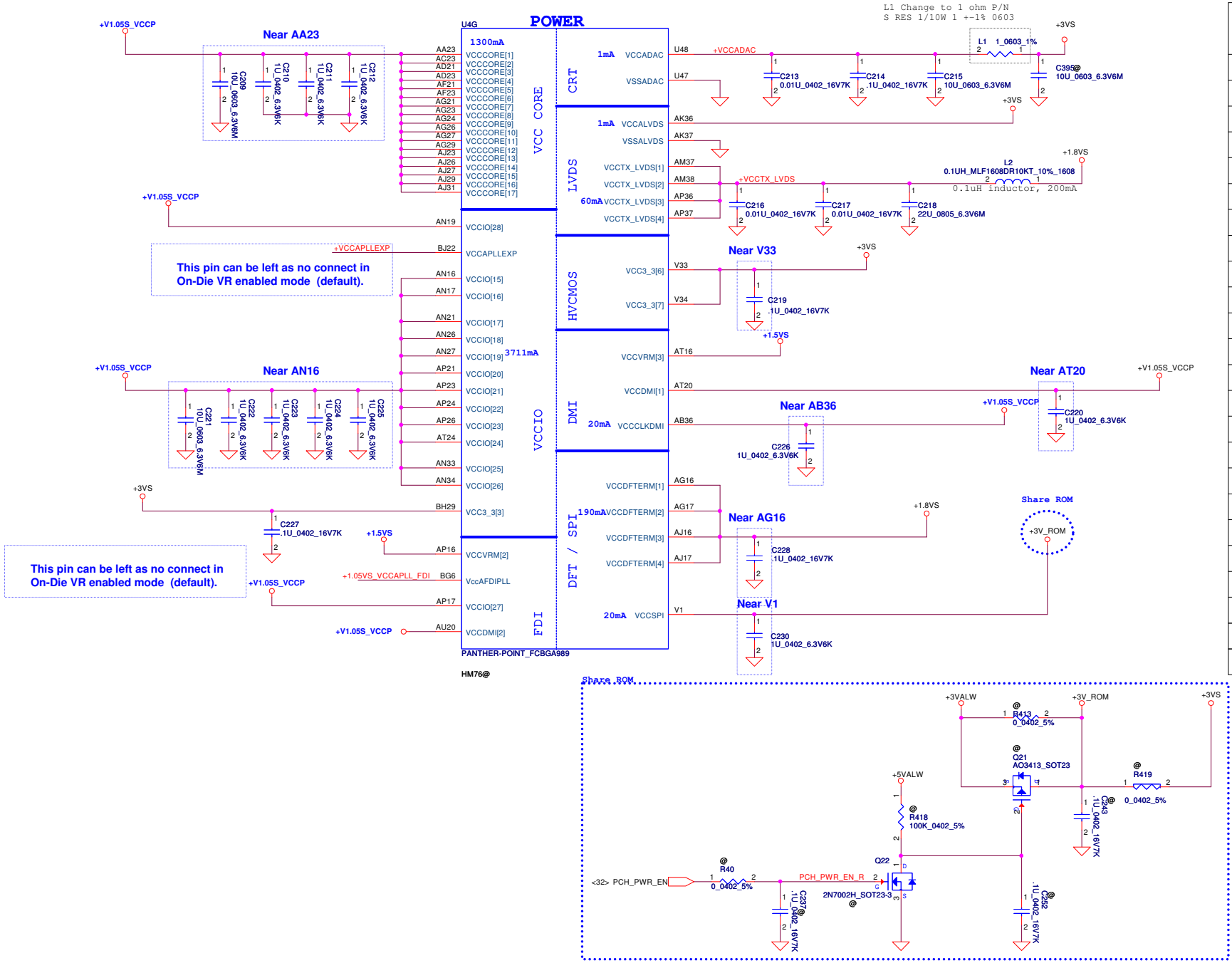

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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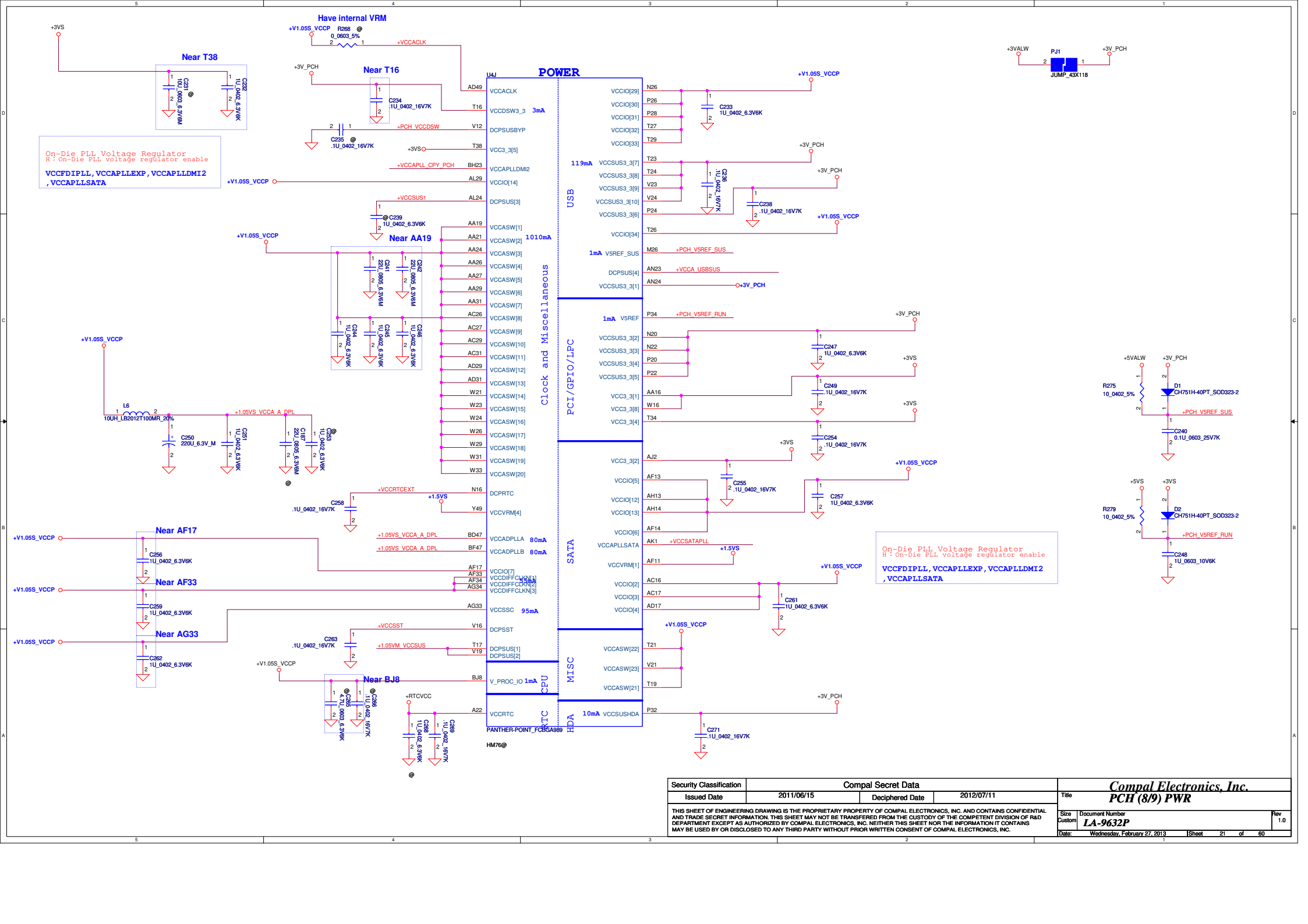
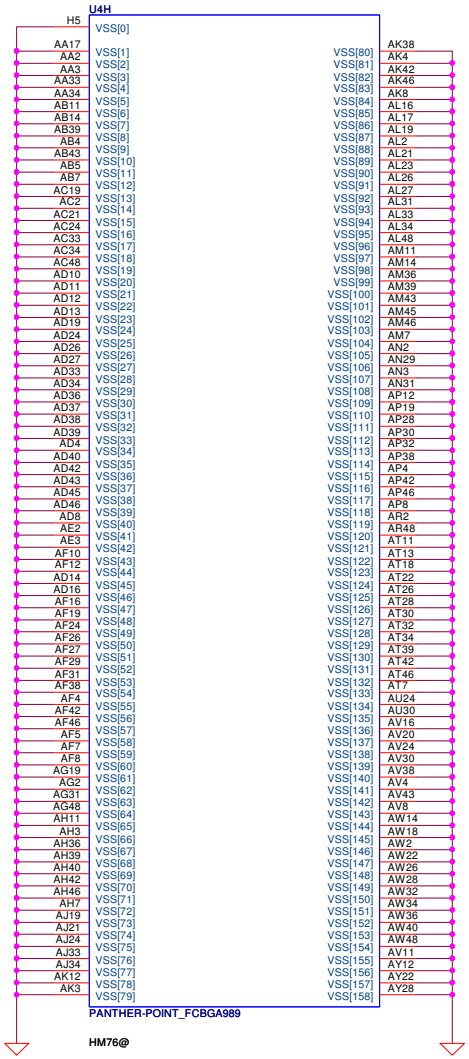
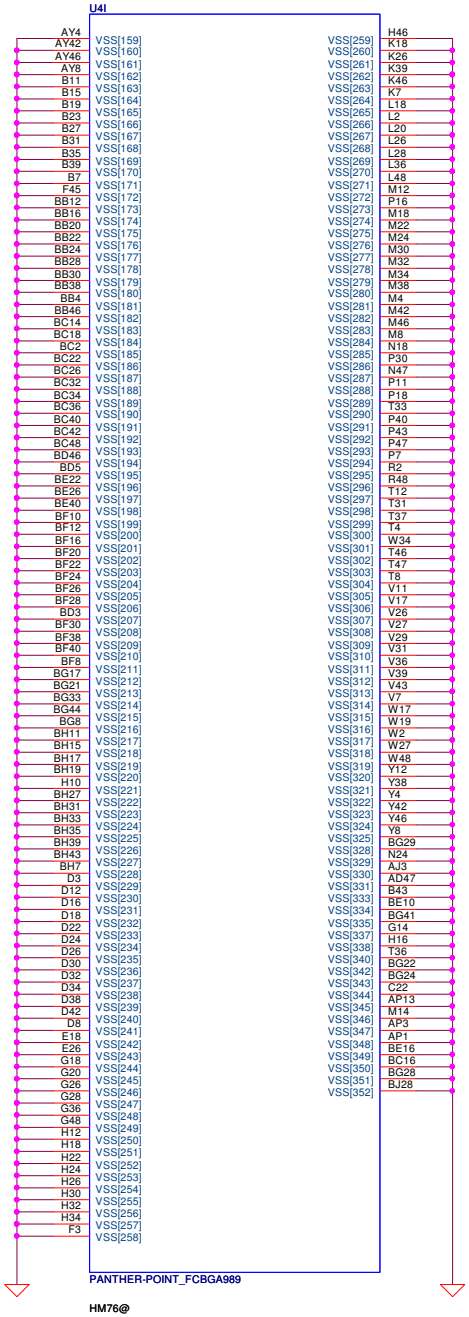
Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-9632P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 20 of 60


Have internal VRM
POWER
Near T38
Near T16
Near AA19
Near AF17
Near AF33
Near AG33
Near BJ8
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA
U4J
PANTHER-POINT_FCBGA989
HM76@
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
JUMP_43X118
Compal Secret Data
2011/06/15
2012/07/11
Compal Electronics, Inc.
PCH (8/9) PWR
LA-9632P
1.0
Wednesday, February 27, 2013
21
60





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

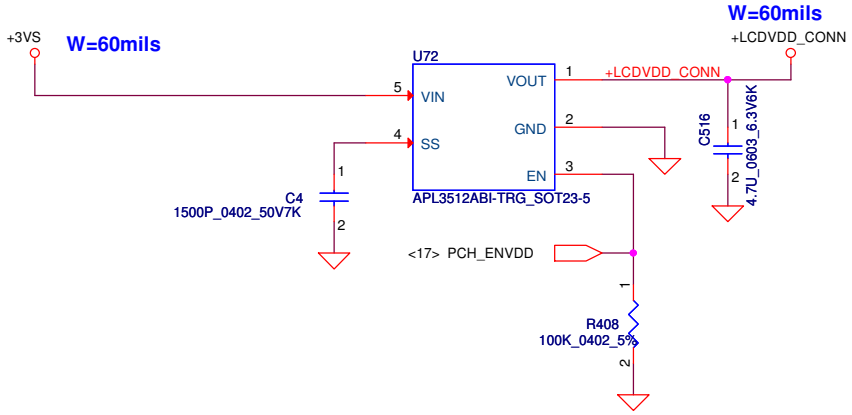
Compal Electronics, Inc.

Title: PCH (9/9) VSS

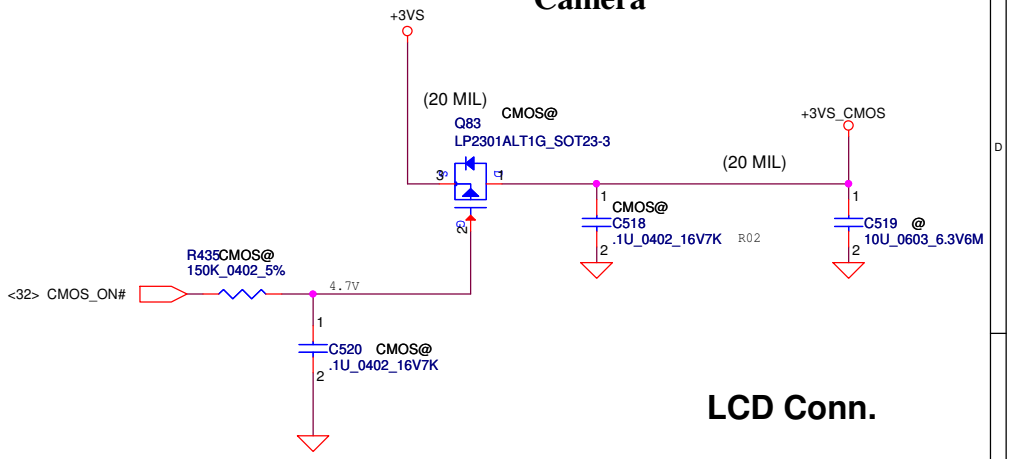
Size: Custom | Document Number: LA-9632P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 22 of 60

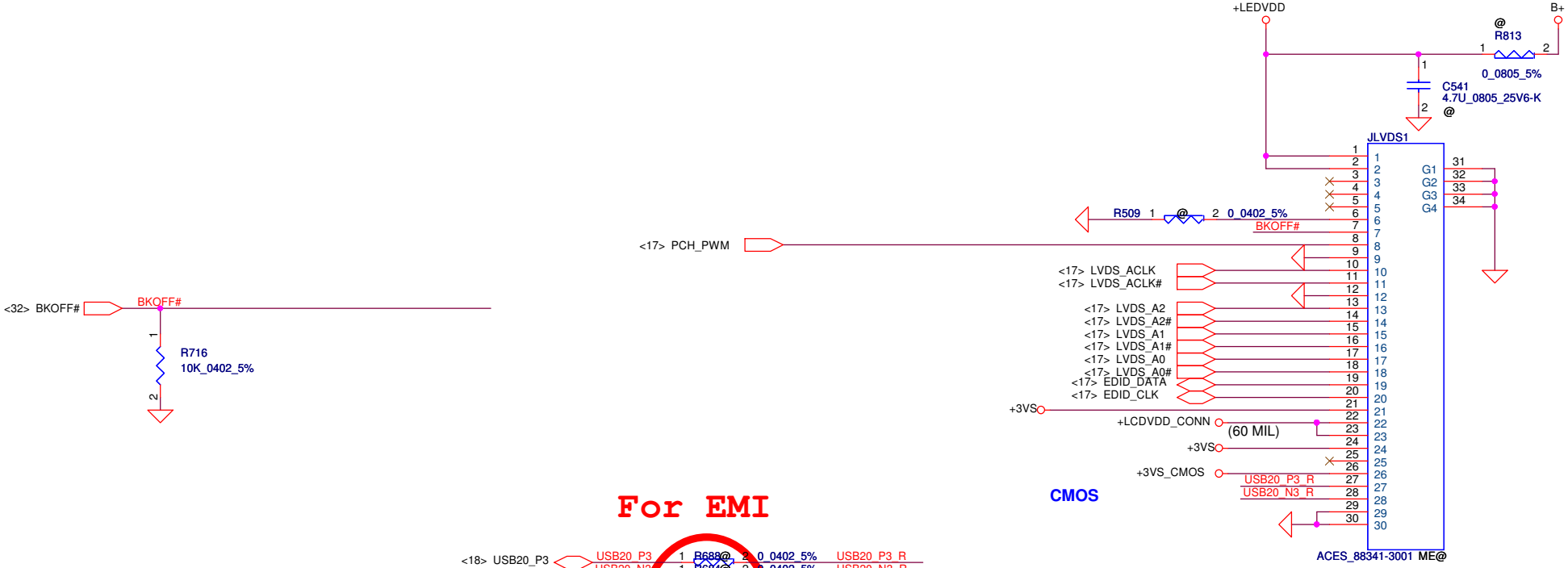
LCD POWER CIRCUIT



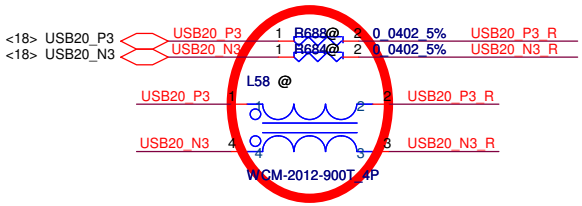
Camera



LCD Conn.



For EMI



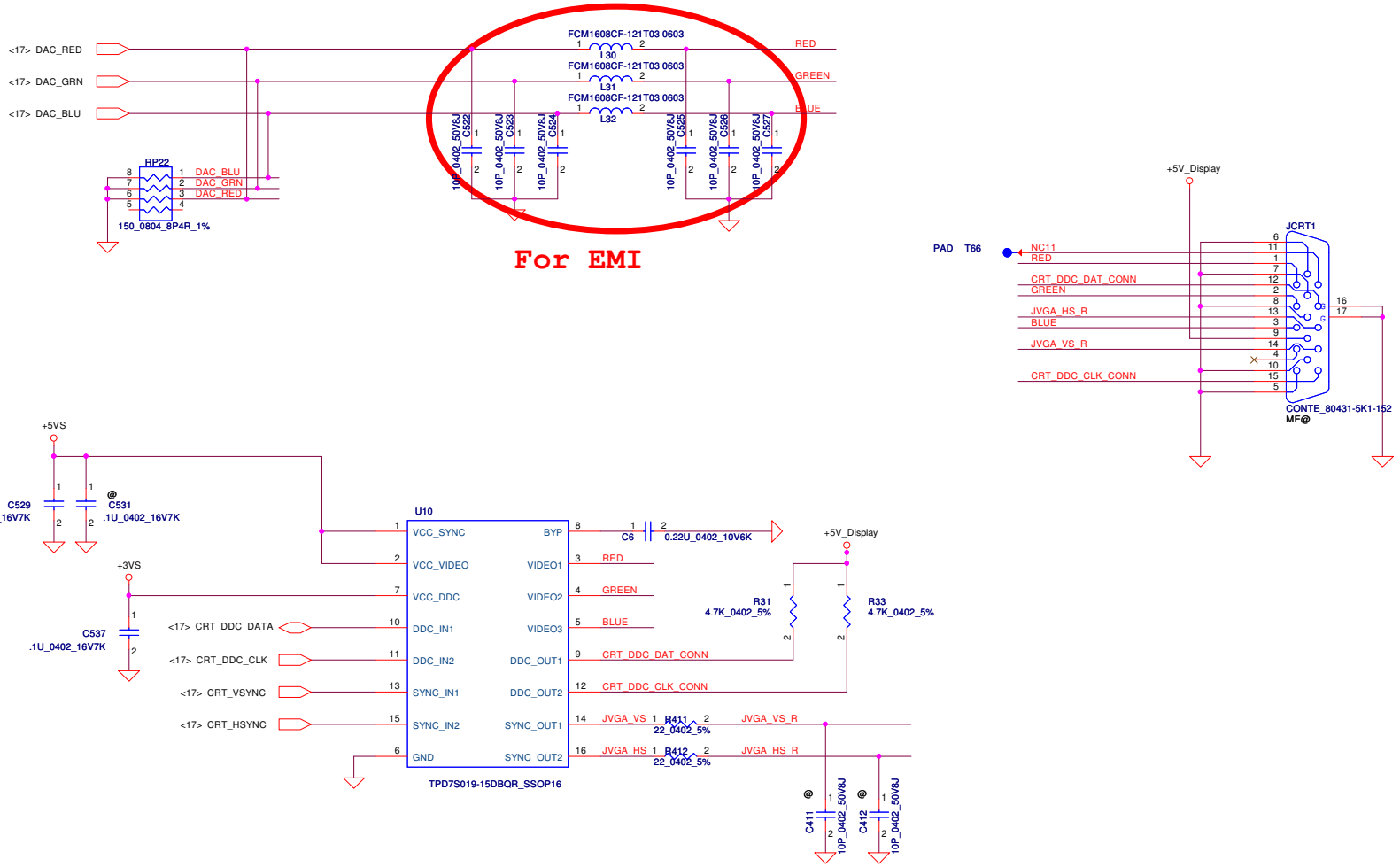
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 | Sheet 23 of 60



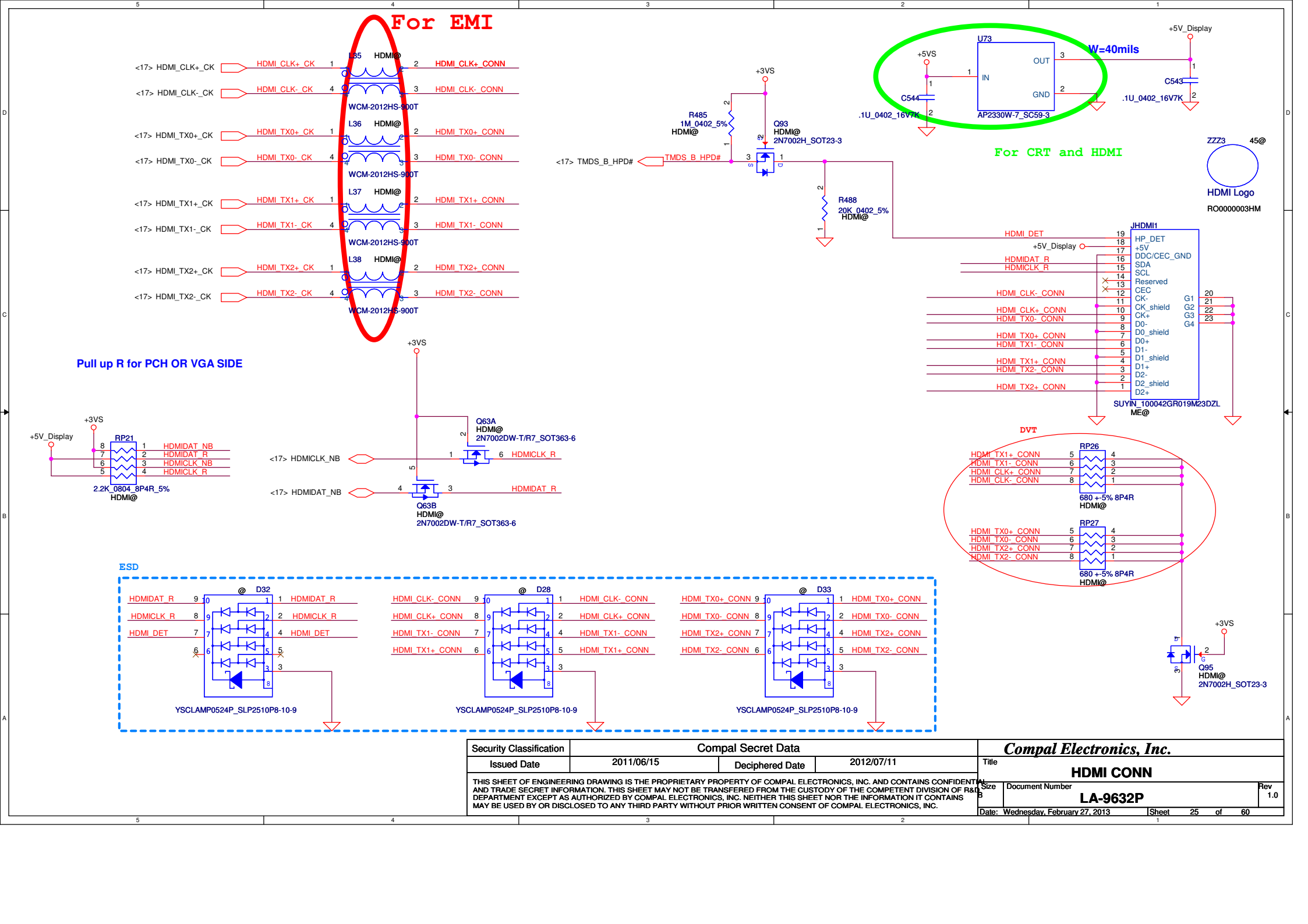
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 | Sheet 24 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

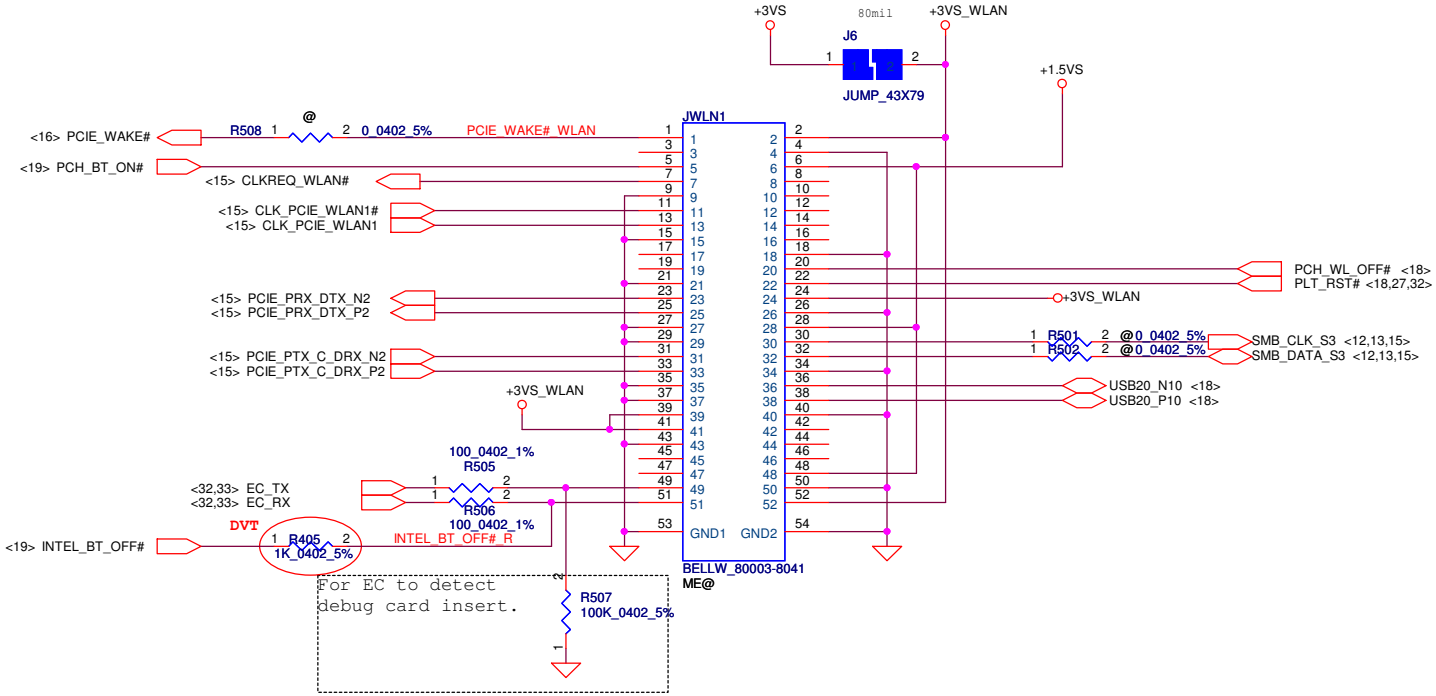
Compal Electronics, Inc.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-9632P	1.0

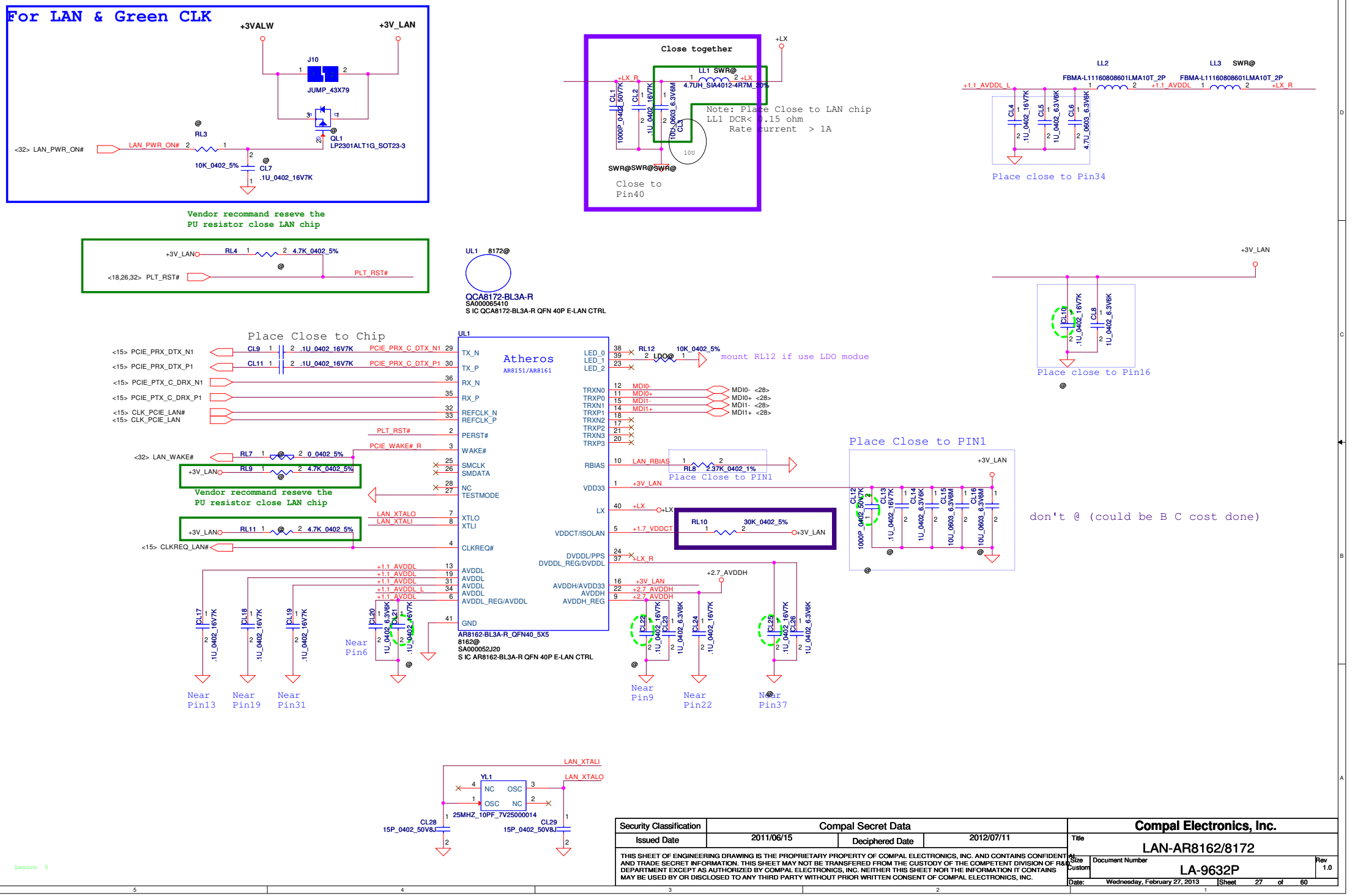
Date: Wednesday, February 27, 2013 Sheet 25 of 60

Mini Card for WLAN/WiMAX(Half)



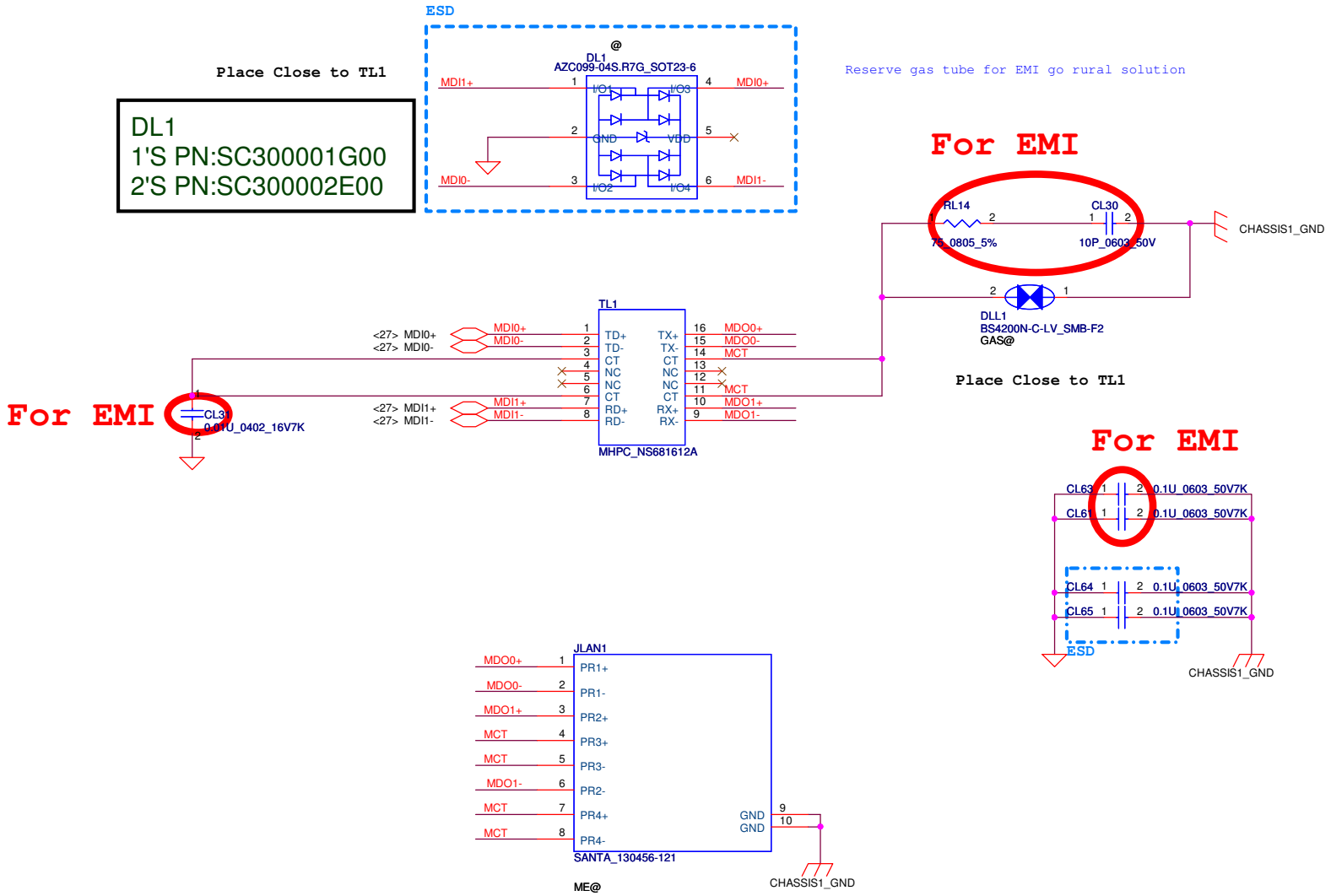
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: Mini-Card/NEW Card/SIM			
Size	Document Number: LA-9632P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 26 of 60		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	LAN-AR8162/8172		
Size Custom	Document Number LA-9632P		Rev 1.0
Date: Wednesday, February 27, 2013	Sheet 27 of 60		

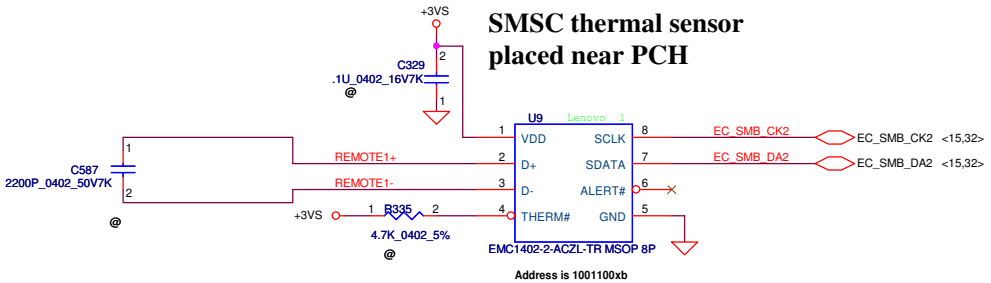


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	LAN_Transformer		
Size: B	Document Number: LA-9632P		Rev: 1.0
Date: Wednesday, February 27, 2013	Sheet 28 of 60		

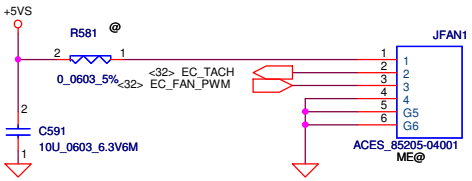
2 Channel

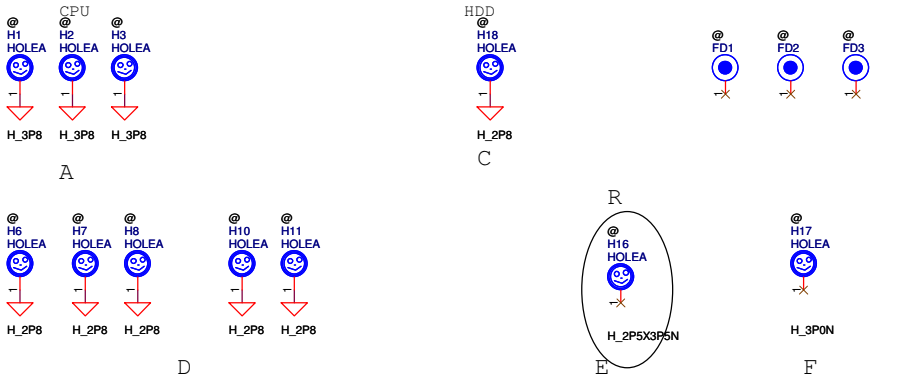
SMSC thermal sensor placed near PCH



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn





2P8 * 9 pcd

M/B 橢圓孔

M/B 圓孔

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

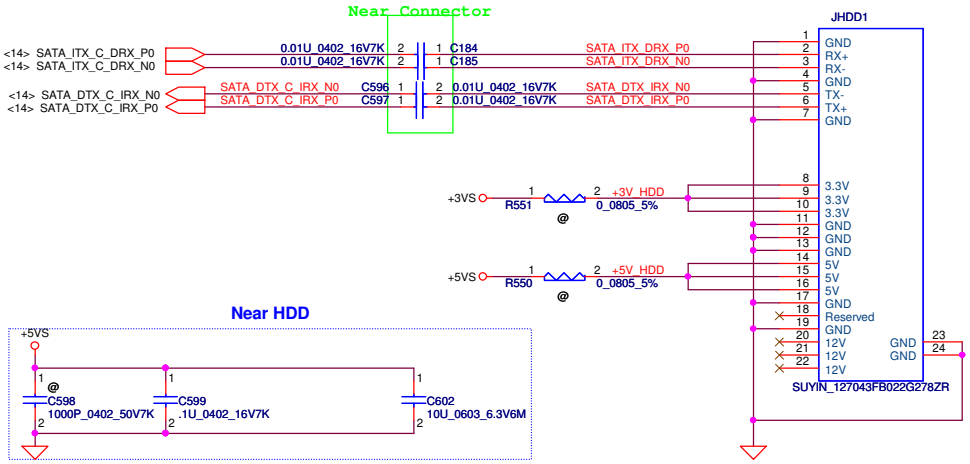
Compal Electronics, Inc.

Title: **Fintek-Thermal IC/FAN/screw**

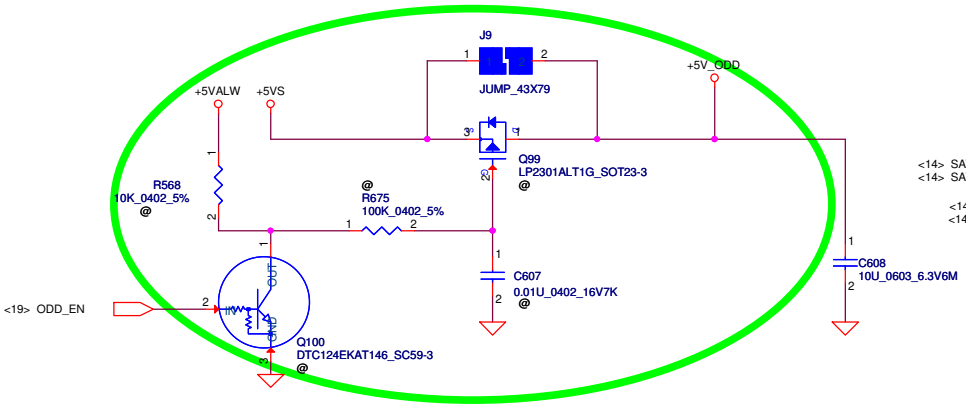
Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 29 of 60

SATA HDD Conn.

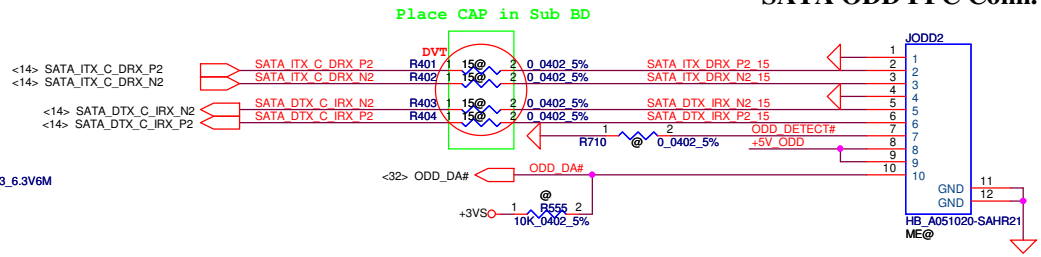


ODD Power Control



FOR 15"

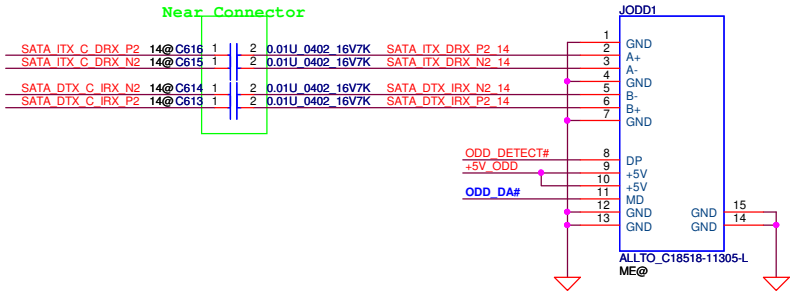
SATA ODD FFC Conn.



Co-lay

FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

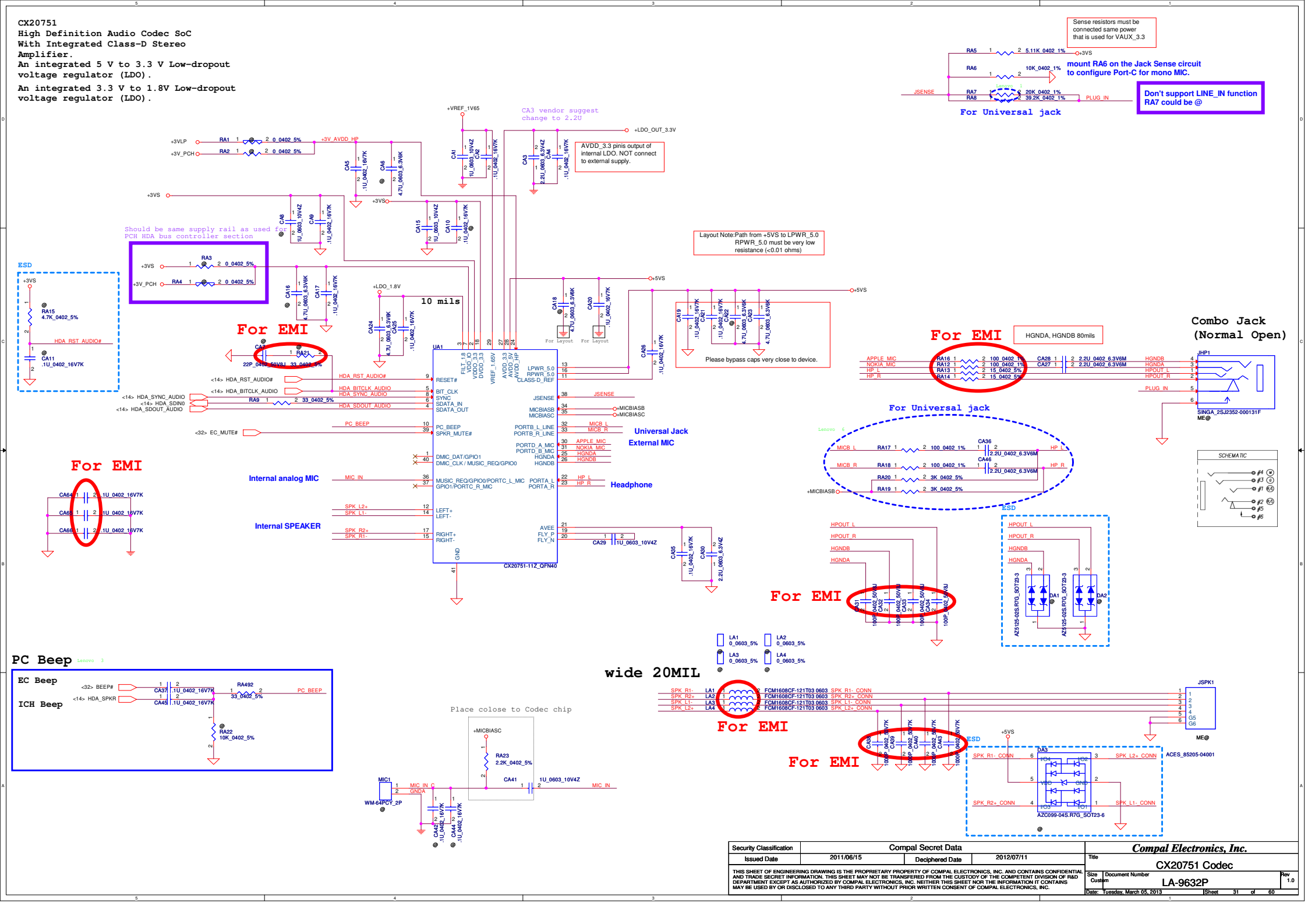
Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 | Sheet 30 of 60

CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: CX20751 Codec

Size: Custom | Document Number: LA-9632P | Rev: 1.0

Date: Tuesday, March 05, 2013 | Sheet 31 of 60

Vcc	3.3V
R694	100K +/- 1%

Board ID / SKU ID Table for AD channel

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0 V	0x00 – 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C – 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D – 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 – 0x30	EVT

SA00004OB30
S IC KB9012QF A4 LQFP 128P KB CONTROLLER

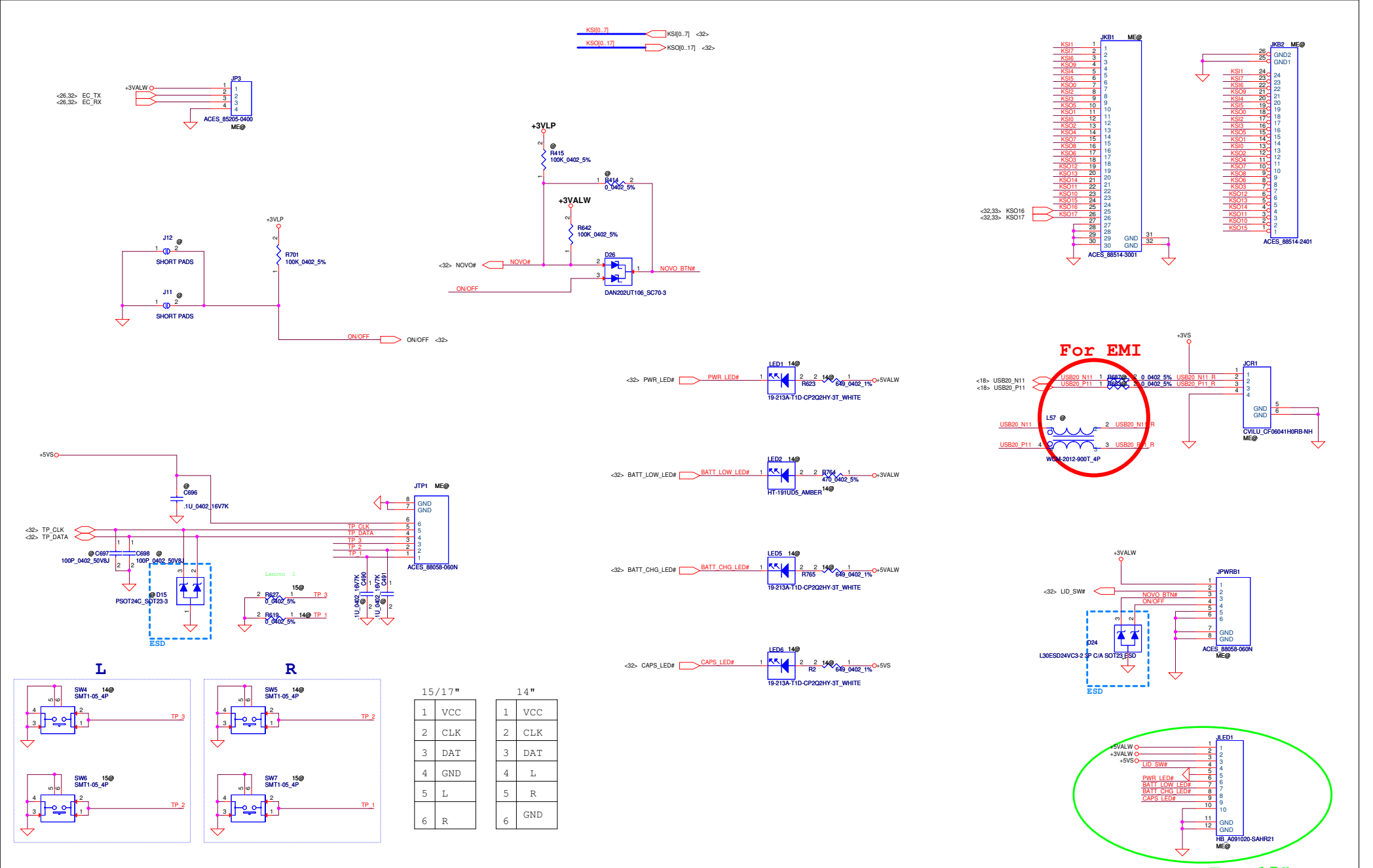
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 32 of 60



15/17"

1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"

1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ROM/KBD/PWR/CR/LED/TP Conn.

Size	Document Number	Rev
C	LA-9632P	1.0

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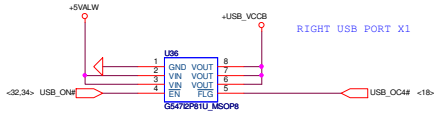
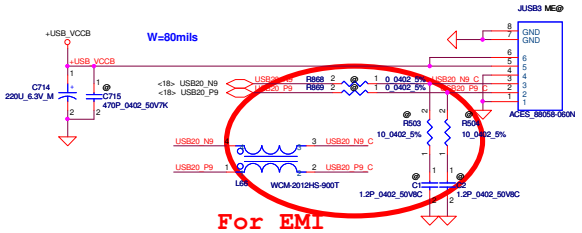
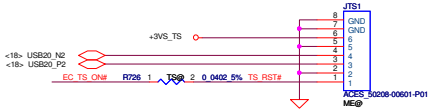
Ext. USB2.0

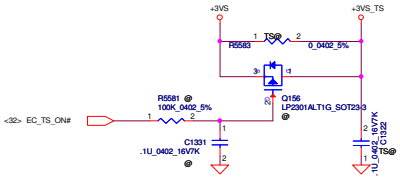


Right Ext.USB Conn.

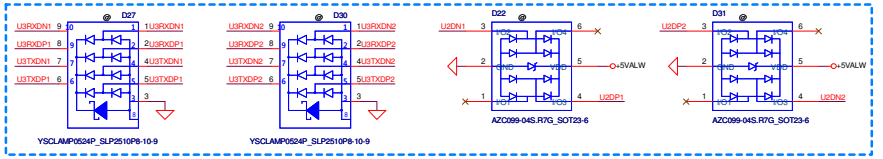


Touch Screen

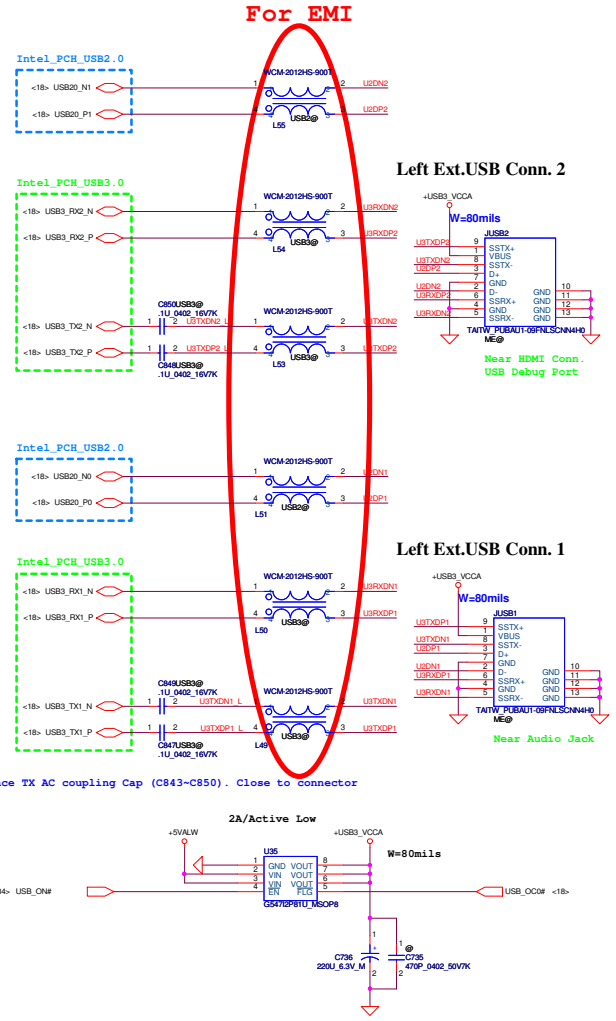




ESD



USB3.0



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Issued Date	2011/06/15	Deciphered Date	2012/07/11
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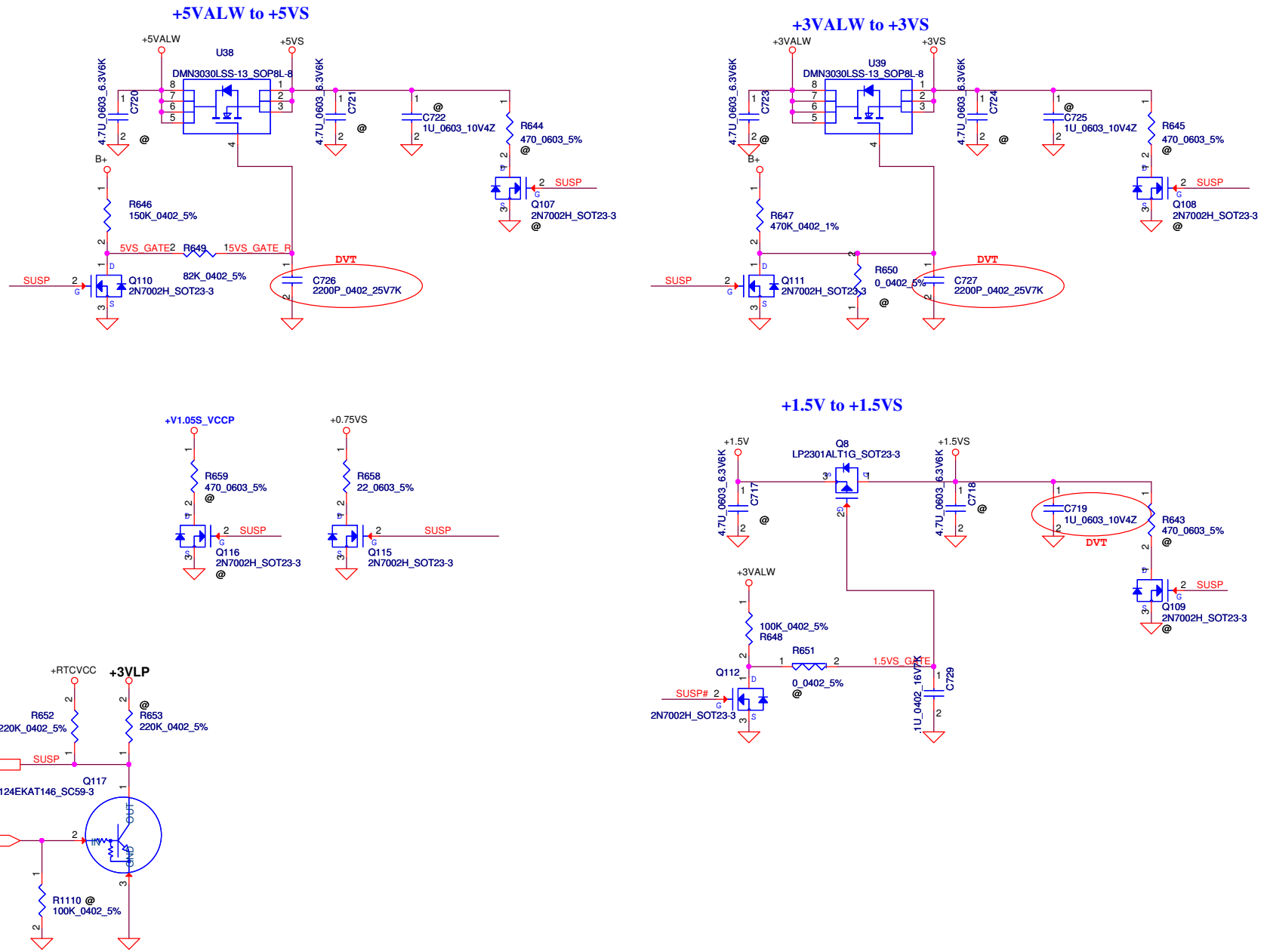
			Document Number: Rev 1.0
			Date: Wednesday, February 27, 2013 Sheet 34 of 60



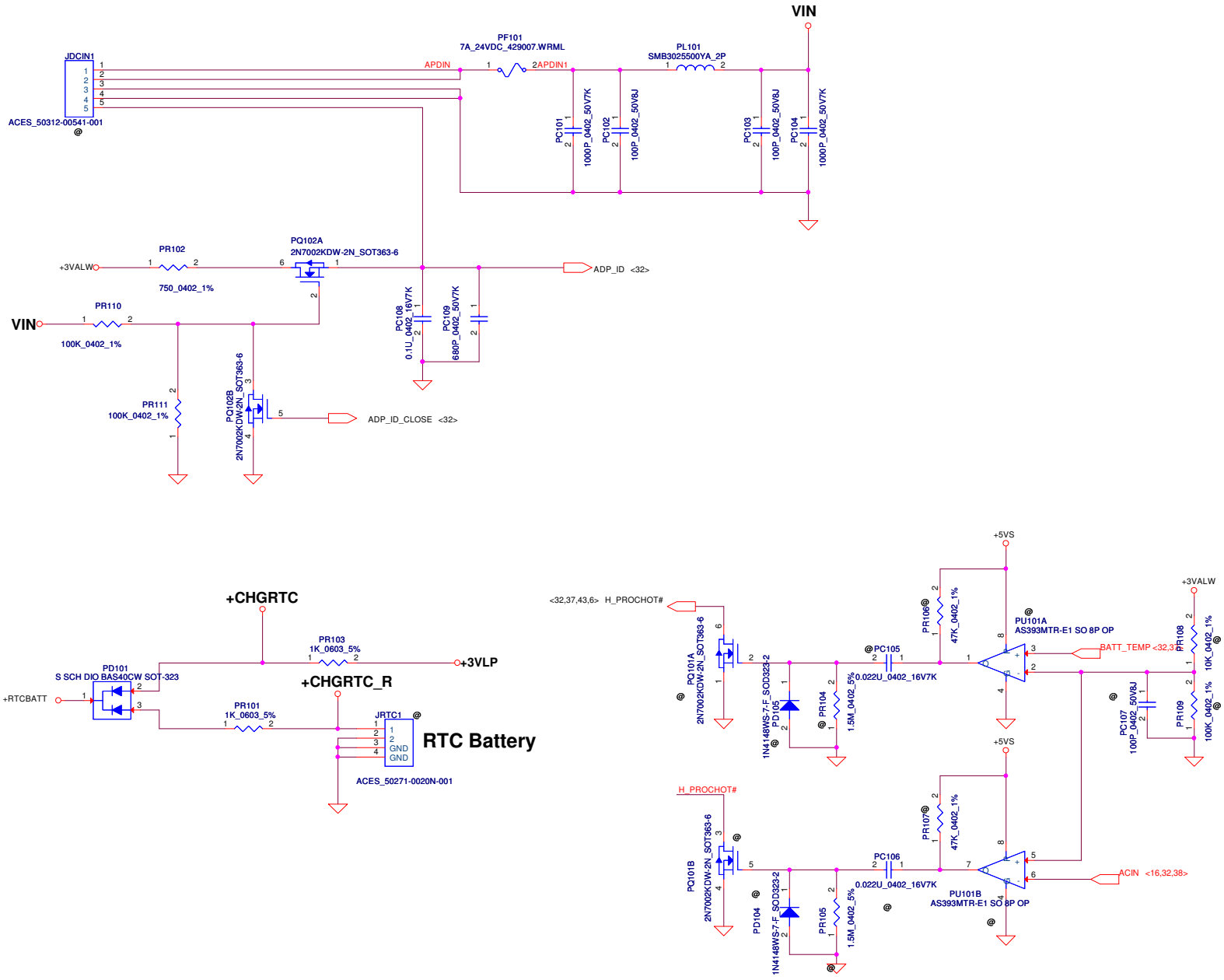
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-9632P	1.0

Date: Wednesday, February 27, 2013 Sheet 35 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: Gx00 | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 36 of 60

JBATT1 ---> 15"

JBATT2 ---> 14"

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

90W(DIS) : 6.65K 100W active 90W recovery
65W(UMA): 1.65K 70W active 65W recovery

20120314
Change to +EC_VCCA from +3VLP

VMB2
JBATT1
SUYIN_200082GR007M229ZR
PF201 12A_65V_451012MRL
VMB
PL201 SMB3025500YA_2P
BATT+
EC_SMCA
EC_SMDA
PR201 100_0402_1%
PR204 100_0402_1%
PC201 1000P_0402_50V7K
PC203 0.01U_0402_25V7K
EC_SMB_CK1 <32,38>
EC_SMB_DA1 <32,38>
JBATT2
SUYIN_200082GR007M229ZR
PR209 6.49K_0402_1%
+3VLP
PR206 6.49K_0402_1%
+3VALW
PR207 10K_0402_5%
BATT_TEMP <32,36,37>
A/D

+3VS
<32,36,43,6> H_PROCHOT#
PR215 100K_0402_1%
PQ201
2N7002KW_SOT323-3
ADP_OCP_1
PR216 0_0402_5%
<32,37> PROCHOT

<32,38> ADP_I
+EC_VCCA
PR221 8.45K_0402_1%
PR226 12.7K_0402_1%
<32> Turbo_V
PR229 100K_0402_1%
PR225 25.5K_0402_1%
PR227 9.31K_0402_1%
PR228 5.9K_0402_1%
PR222 100K_0402_1%
<32> NTC_V
PH201 PH-I201 100K_0402_1%_TSM0B104F4251RZ
<32,37> PROCHOT
<32> ADP_65
<32> ADP_90
<32> ADP_135
PQ206 2N7002KW_SOT323-3
PQ208 2N7002KW_SOT323-3
PQ207 2N7002KW_SOT323-3
ECAGND

VL
PC202 0.01U_0402_25V7K
PR202 75K_0402_1%
PR210 47K_0402_1%
<32,36,37> BATT_TEMP
PC208 0.068U_0402_16V7K~N
PU201A AS393MTR-E1 SO 8P OP
PR213 100K_0402_1%
PC207 100P_0402_50V8J
PR205 1.5M_0402_5%
PD201 1N4148WS-7-F_SOD323-2
+3VALW
PR211 100K_0402_1%
PR214 100K_0402_1%
BATT_OUT <38>
PQ202A 2N7002KDW-2N_SOT363-6
PQ202B 2N7002KDW-2N_SOT363-6

VMB
+3V_LDO
VL
@PR208 75K_0402_1%
@PR218 47K_0402_1%
@PC210 0.068U_0402_16V7K~N
PU201B AS393MTR-E1 SO 8P OP
@PR217 100K_0402_1%
@PC213 100P_0402_50V8J
@PR223 1.5M_0402_5%
@PD203 1N4148WS-7-F_SOD323-2
+3VLP
PR220 100K_0402_1%
<32> BATT_LEN#
PQ205 2N7002KW_SOT323-3
@PQ209 2N7002KW_SOT323-3

+5VALW
@PC212 22U_0603_6.3V6M
@PU202
IN OUT GND SHDN# BYP
G9191-330T1U_SOT23-5
+3V_LDO
@PC209 4.7U_0402_6.3V6M
@PC211 1U_0402_16V6K

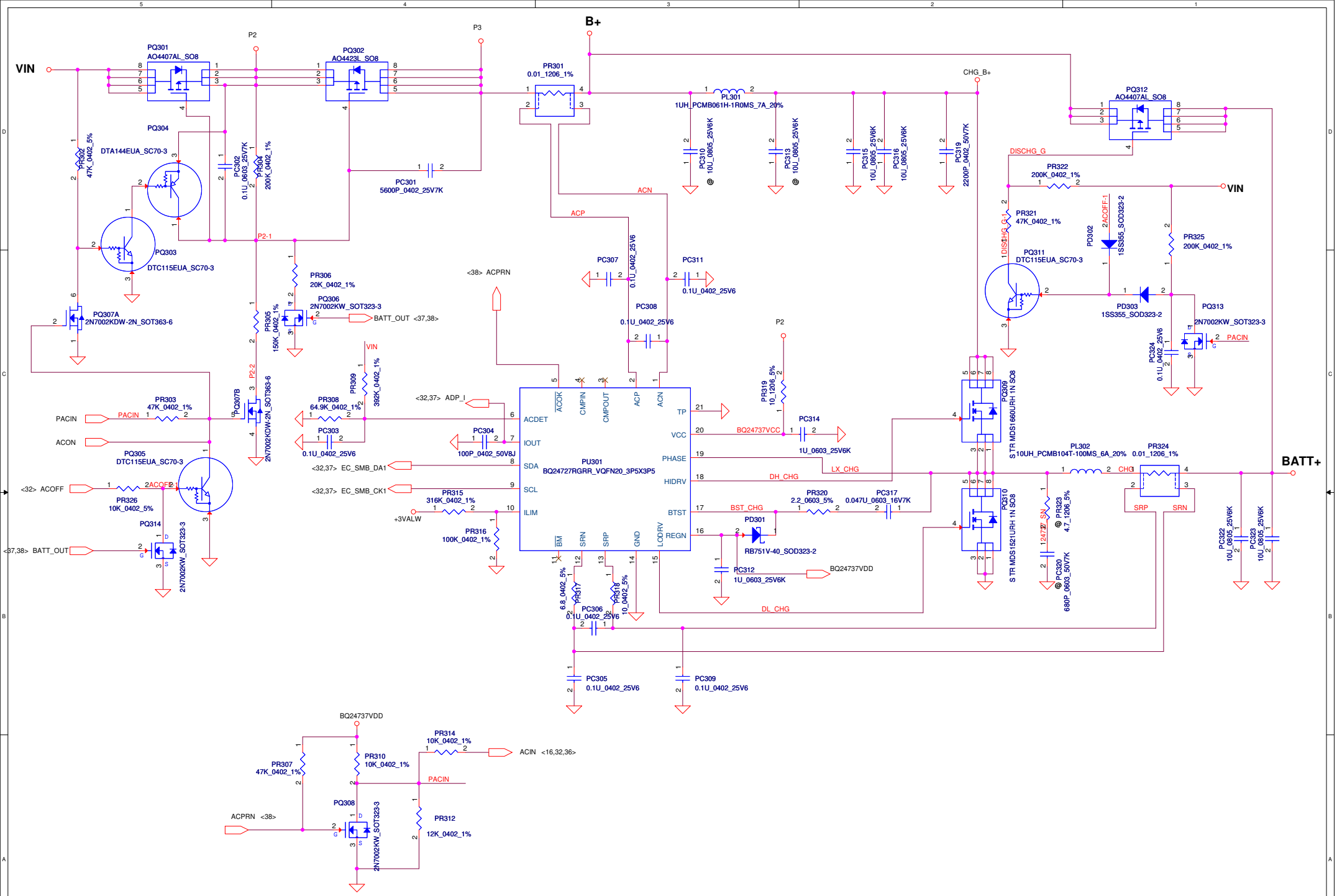
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 37 of 60



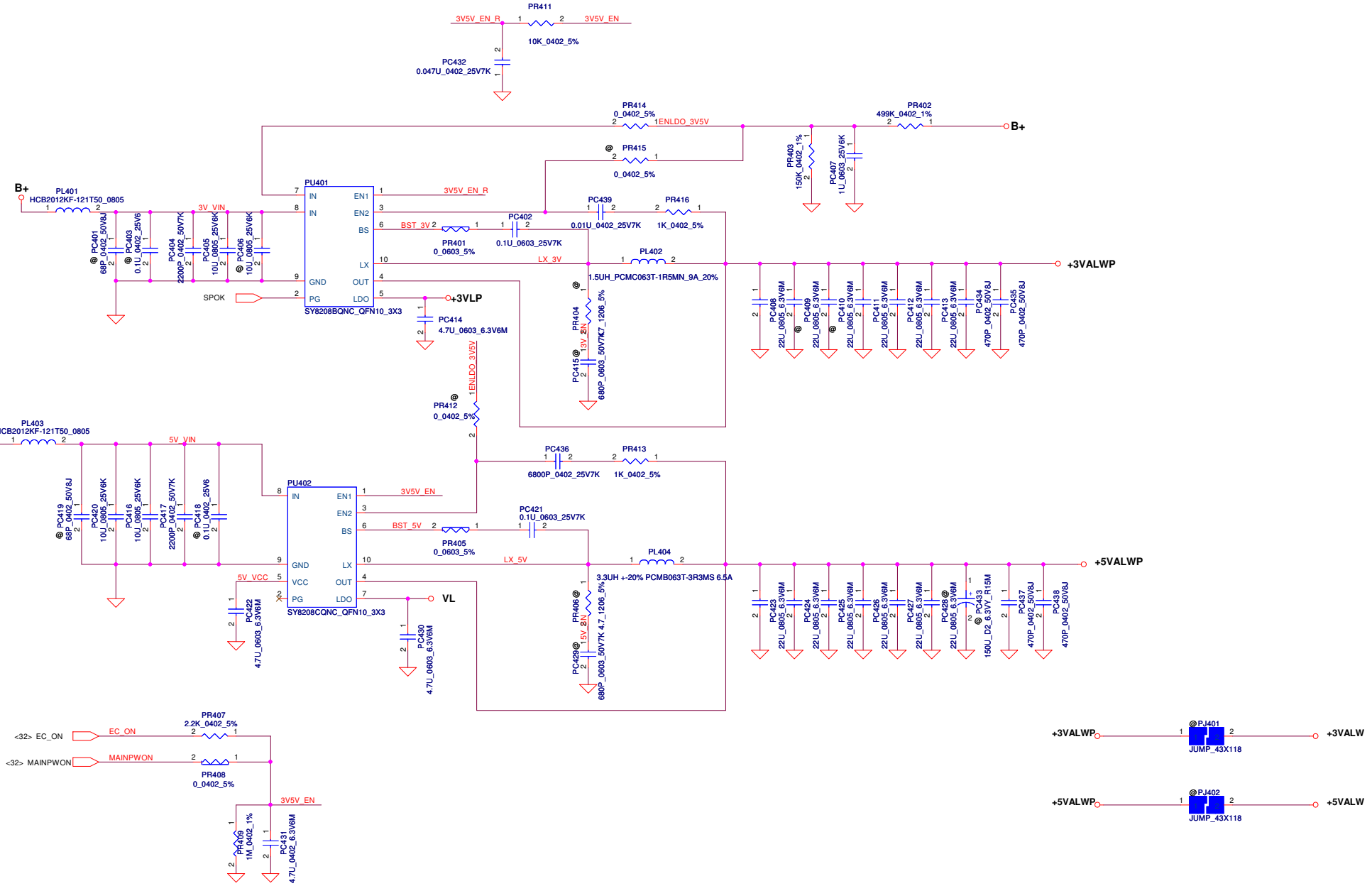
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	Gx00-CR	1.0

Date: Wednesday, February 27, 2013 | Sheet 38 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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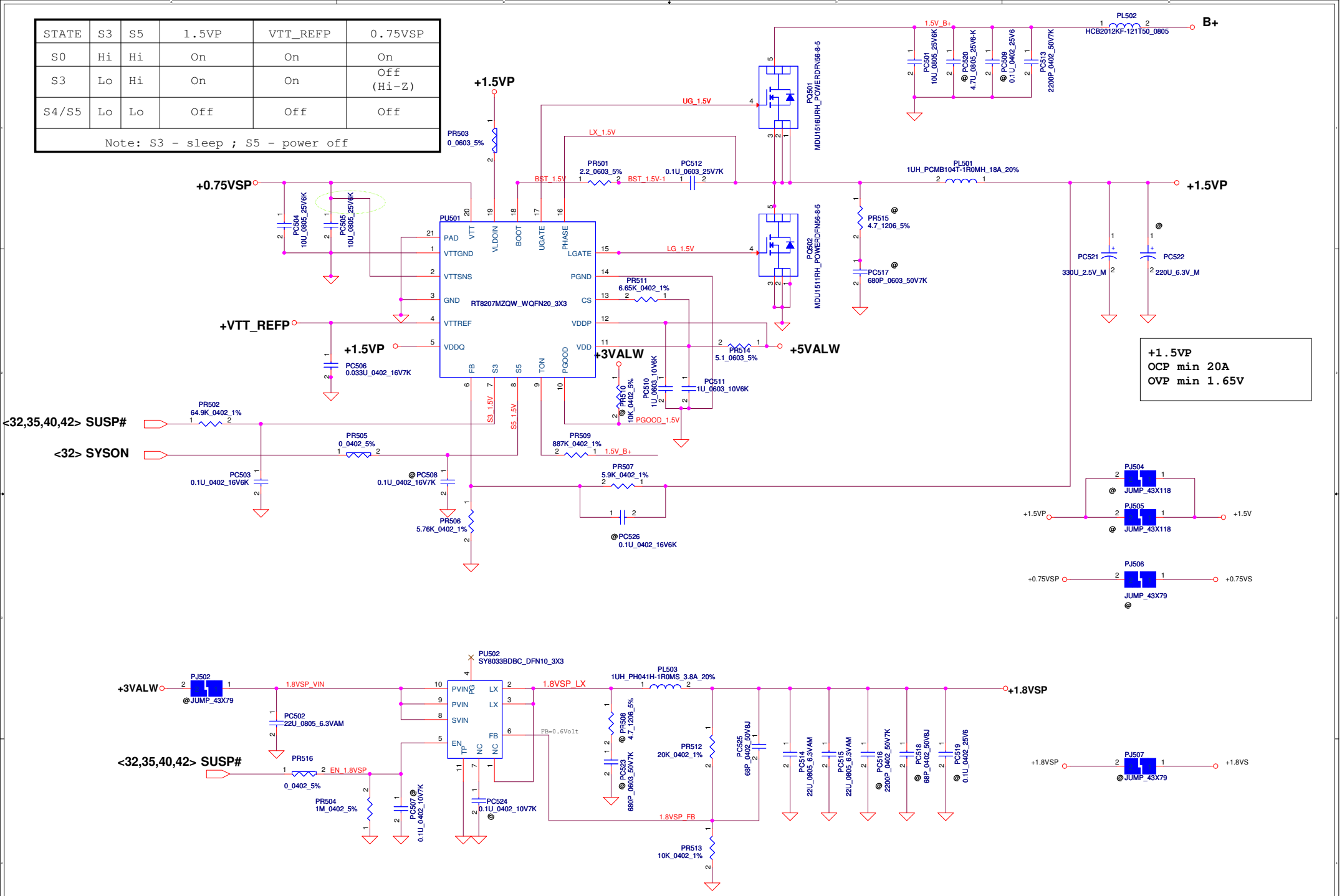
Compal Electronics, Inc.

Title: +1.05VS_VCCP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 39 of 60

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **+1.5VP/+1.8VSP**

Size	Document Number	Rev
Custom	Gx00-CR	1.0

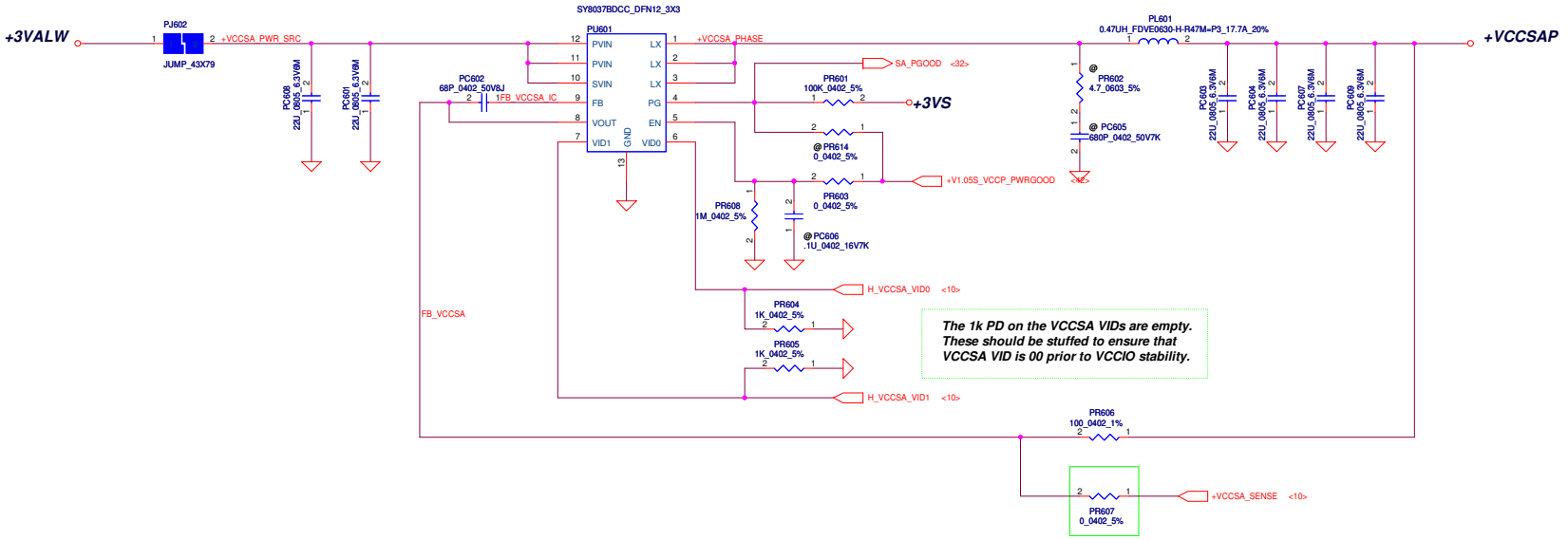
Date: Wednesday, February 27, 2013 | Sheet 40 of 60

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCCSAP — PJ601 JUMP_43X118 — +VCCSA

+V1.05S_VCCP — PR613 0.005_1206_1% — +VCCSA



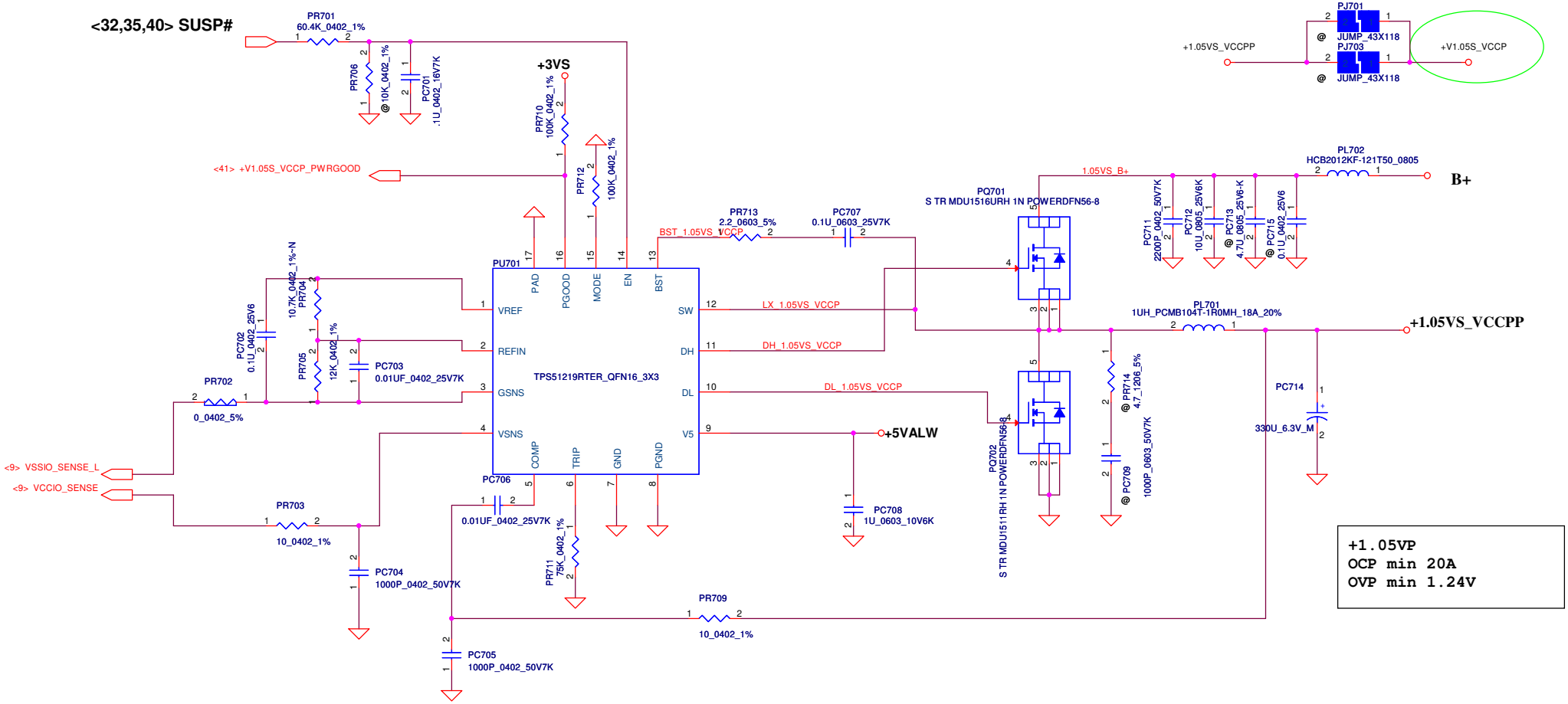
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +VCCSAP

Size	Document Number	Rev
C	Gx00-CR	1.0

Date: Wednesday, February 27, 2013 Sheet 41 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.05VS_VCCP

Size	Document Number	Rev
Custom	Gx00-CR	1.0

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PR915,PR946=200K(setting 113 degreeC)
PR915,PR946=8.25K(setting 93 degreeC)

Switching Frequency = 450KHz

NCP6132AMNR2G_QFN60_7X7

PUT COLSE TO GT Inductor

PUT COLSE TO V_GT HOT SPOT

PUT COLSE TO VCORE Phase 1 Inductor

PUT COLSE TO VCORE HOT SPOT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: PWR-CPU_CORE

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

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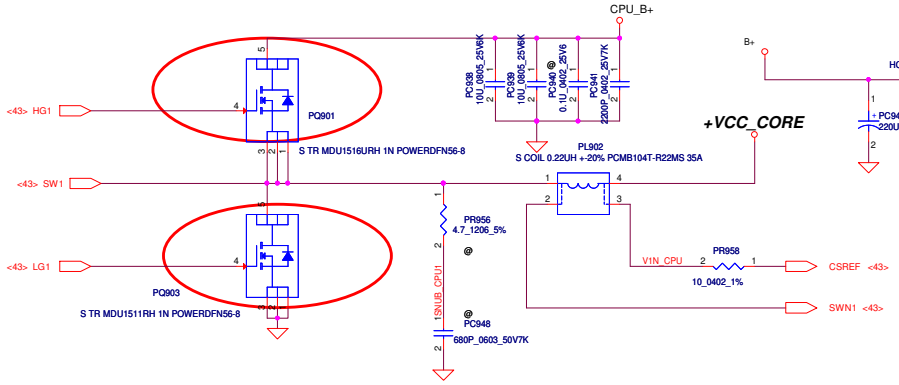
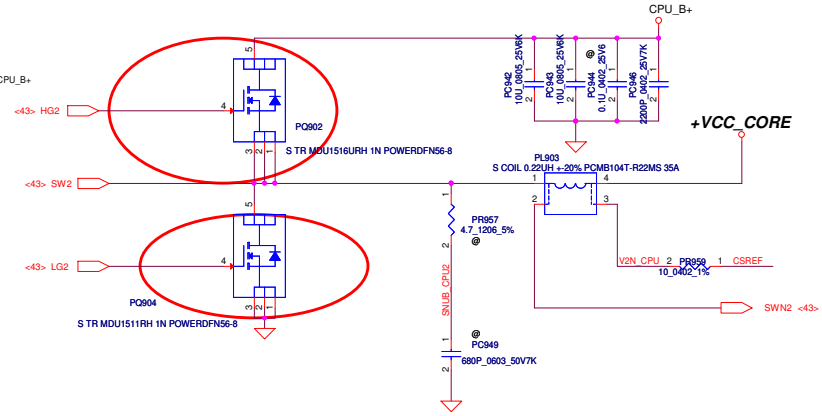
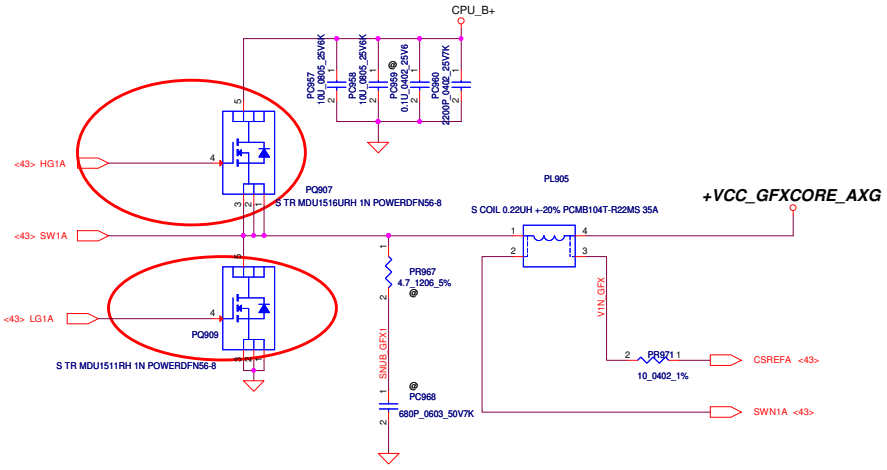




QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size	Document Number	Rev
C	Gx00-CR	1.0

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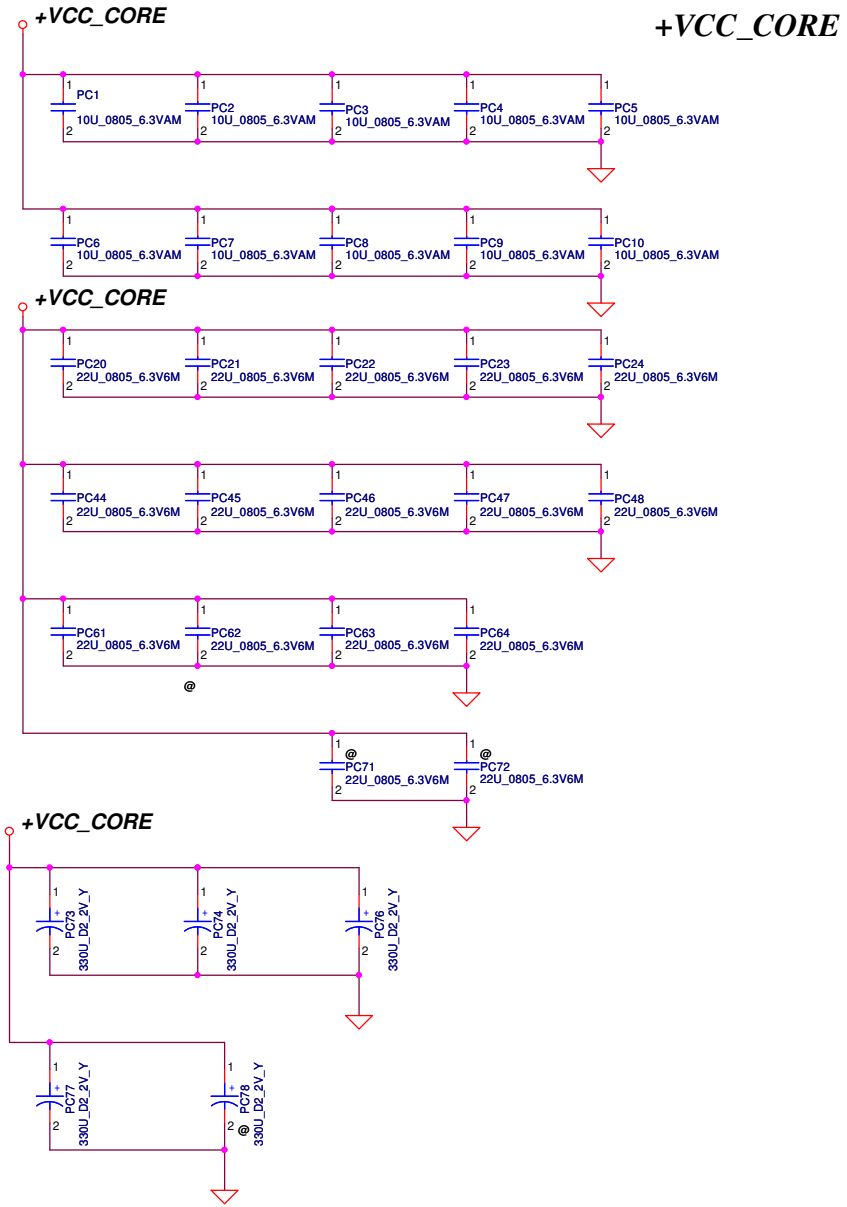
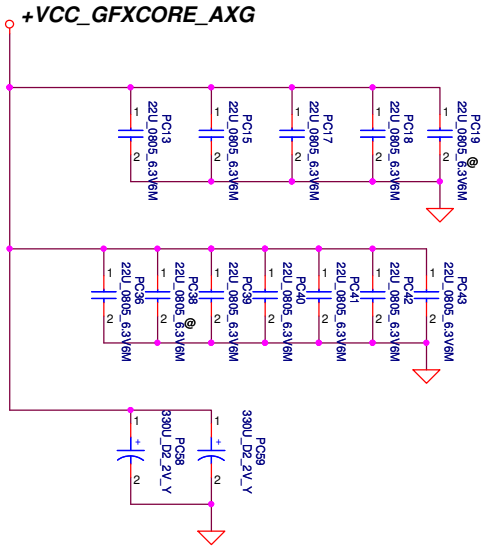
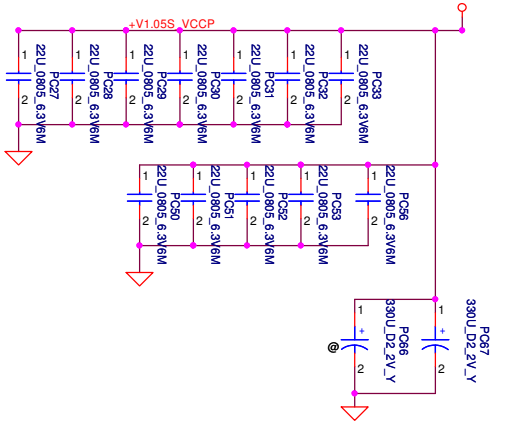




+VCC_GFXCORE_AXG

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



+V1.05S_VCCP

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA-9632P	1.0

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VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.46	Add PR102,PC108,PC109	For ADP_ID pin detect
2	P.47	Add PR225,PR227,PR228,PQ206,PQ207,PQ208	For protect adapter function
3	P.49	Add PR410,PC433	For 3VALWP/5VALWP sequence
4	P.49	Add PC434,PC435,PC436,PC437	For EMI solution
5	P.49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple
6	P.50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence
7	P.51	Add PC637	For +0.95VGSP sequence
8	P.54	Change PC907,PR912,PR927,PC928	For CPU Transient Compensation
9			
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Title: PIR (PWR)

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 1.0

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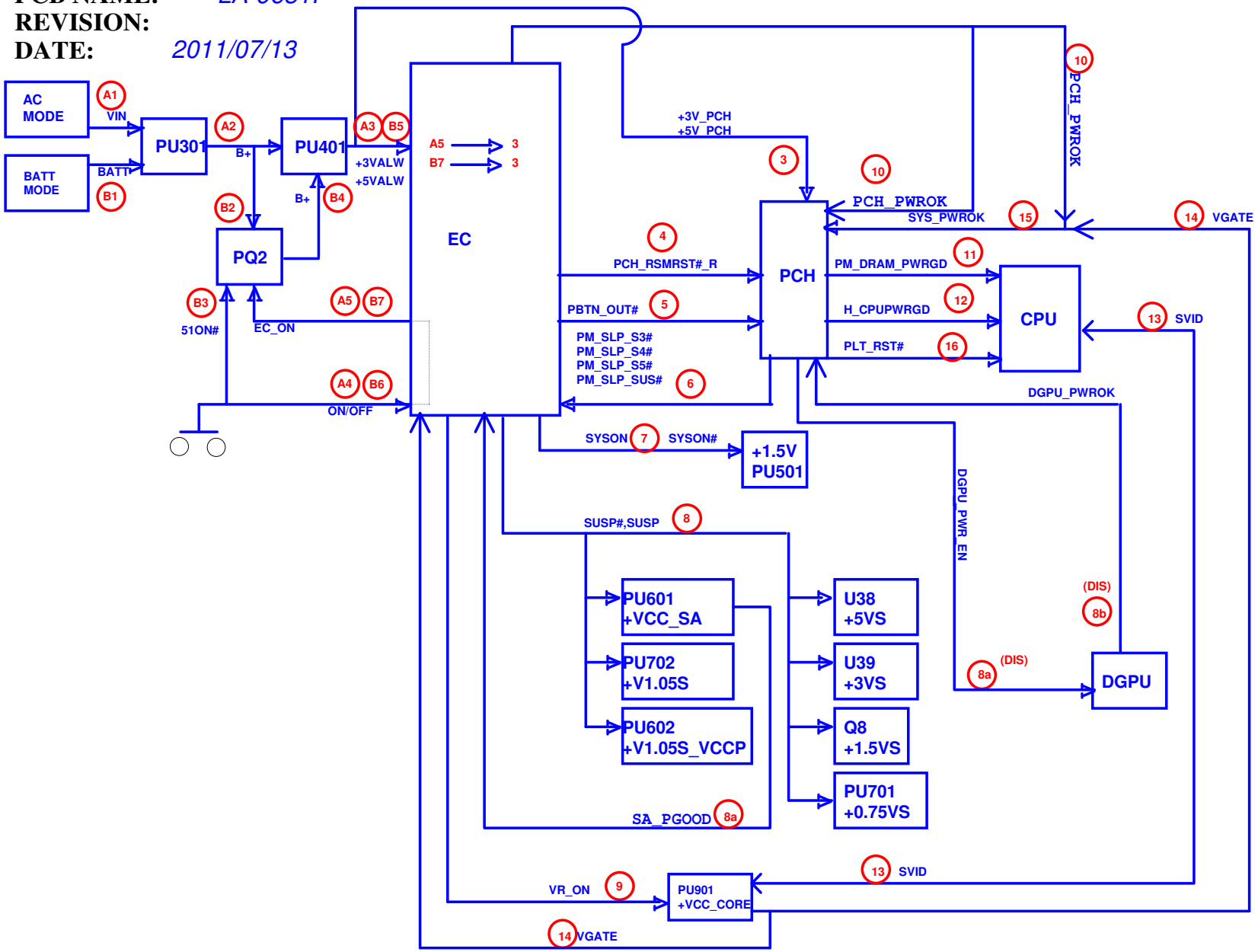
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9631P*
REVISION:
DATE: *2011/07/13*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: ***Power sequence***

Size: Custom | Document Number: ***LA-9632P*** | Rev: 1.0

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VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.36	Change C726, C727 to 2.2nF	For Sequence
2	P.26	Add R405	For Intel Combo Card
3	P.25	Delete RP19. Add RP26, RP27	Because ME modify MIC location
4	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
5	P.32	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
6	P.32	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
7	P.32	Reserve R410	Reserve Pull-high for GPIO
8	P.5~22	Change footprint of JCPU1, U4	For Lenovo rule
9	P.21	Add Q21, R40, C237, R225, C243	Reserve for power consumption
10	P.24	Add R411, R412, C411, C412	Reserve for EMI
11	P.32	Add ADP_65 to EC Pin.21	For adapter protection
12	P.32	Add ADP_90 to EC Pin.68	For adapter protection
13	P.32	Add ADP_135 to EC Pin.85	For adapter protection
14	P.32	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
15	P.32	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
16	P.32	Add ADP_ID to EC Pin.66	For adapter
17	P.32	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design
18	P.32	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
19	P.32	Add VGATE to EC Pin.74	Reserve for sequence
20	P.32	Add SYS_PWROK to EC Pin.86	Reserve for sequence
21	P.32	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design
22	P.32	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
23	P.32	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design

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Title: HW-PIR1

Size: Custom | Document Number: LA-9632P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 48 of 60

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.30	Delete R416, Add J9	No need Zero ODD Function
2	P.26	Reserve R508	For leakage current issue of Atheros WLAN
3	P.23	Add R509	protect BKOFF# damage
4	P.32	Reserve R416	Reserve +3VLP power rail to EC
5	P.32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P.32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC.
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P.14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P.31	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P.32	Reserve resistance in EC for share ROM.	Follow common design
3	P.41	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU

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Title: HW-PIR2		
Size: Custom	Document Number: LA-9632P	Rev: 1.0
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