

# Multi-Phase PWM Controller for CPU Core Power Supply with Serial Programming Interface

## General Description

The MS-10 is a multi-phase synchronous buck controller which is implemented with full control functions for Intel® VR10.0/10.1-compliant CPU. The MS-10 could be operated with 2, 3 or 4 buck switching stages operating in interleaved phase set automatically. The multiphase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors.

MS-10 is the 1<sup>st</sup> of RichTek CPU core power solutions which integrates a specific series programming interface for the controller peration configuration. There are several registers implemented for the specific parameters configuration including switching operation frequency, VID for core power, and signal for load current indication. For the consideration of performance, load regulation and thermal dissipation, User can program the configuration of the parameters easily via the specific programming interface. With the implementation of MS-10, the part provides more flexibility and feature for customers advanced segment product design.

The MS-10 applies the DCR sensing technology newly as well; with such a topology, the MS-10 extracts the DCR of output inductor as sense component to deliver a more precise load line regulation and better thermal balance for next generation processor application. For current sense setting, droop tuning,  $V_{CORE}$  initial offset and over current protection are independent to compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning. The DAC output of MS-10 supports VRD10.x with 6-bit VID input, precise initial value & smooth  $V_{CORE}$  transient at VID jump. The IC monitors the  $V_{CORE}$  voltage for over-voltage protection. Soft-start, over-current protection and programmable under-voltage lockout are also provided to assure the safety of microprocessor and power system. The MS-10 comes to the package of VQFN-32L 5x5.

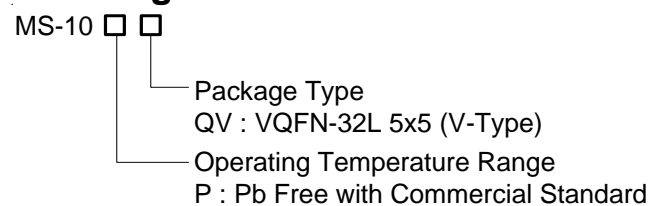
## Features

- Multi-Phase Power Conversion with Automatic Phase Selection
- 6-bits VRD10.x DAC Output with Active Droop Compensation for Fast Load Transient
- Smooth  $V_{CORE}$  Transition at VID Jump
- Power Stage Thermal Balance by DCR Current Sense
- Hiccup Mode Over-Current Protection
- Adjustable Switching Frequency (50kHz to 400kHz per Phase)
- Under-Voltage Lockout and Soft-Start
- High Ripple Frequency Times Channel Number
- Signal for  $V_{CORE}$  Load Current Indication
- 2-Wires Programming Interface
- Software Programmable Switching Frequency
- Software Programmable VID
- Software Programmable High-Current Indication
- 32-Lead VQFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

## Applications

- Intel® VR10.x-compliant Processors Voltage Regulator
- Low Output Voltage, High power density DC-DC Converters
- Voltage Regulator Modules

## Ordering Information



Note :

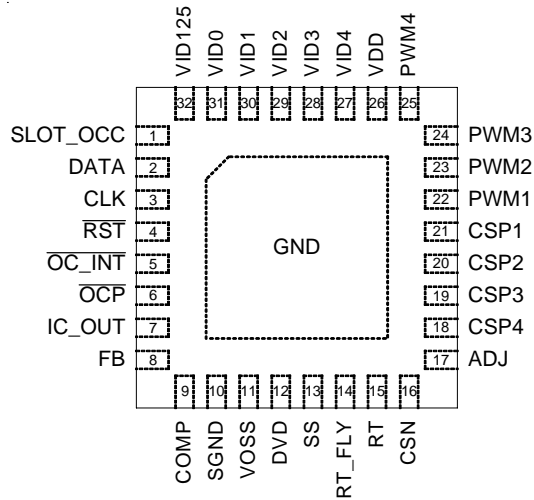
RichTek Pb-free products are :

- ▶RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶Suitable for use in SnPb or Pb-free soldering processes.
- ▶100% matte tin (Sn) plating.

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Pin Configurations

(TOP VIEW)



VQFN-32L 5x5

Registers

0x00 Hi-I setting registers; Default 0x00

Bit4-0 :

Bit4	Bit3	Bit2	Bit1	Bit0	VID Offset (mV)
0	0	0	0	0	0
0	0	0	0	1	12.5
0	0	0	1	0	25
0	0	0	1	1	37.5
0	0	1	0	0	50
0	0	1	0	1	62.5
0	0	1	1	0	75
0	0	1	1	1	87.5
0	1	0	0	0	100
0	1	0	0	1	112.5
0	1	0	1	0	125
0	1	0	1	1	137.5
0	1	1	0	0	150
0	1	1	0	1	162.5
0	1	1	1	0	175
0	1	1	1	1	187.5

Bit4	Bit3	Bit2	Bit1	Bit0	VID Offset (mV)
1	0	0	0	0	200
1	0	0	0	1	212.5
1	0	0	1	0	225
1	0	0	1	1	237.5
1	0	1	0	0	250
1	0	1	0	1	262.5
1	0	1	1	0	275
1	0	1	1	1	287.5
1	1	0	0	0	300
1	1	0	0	1	312.5
1	1	0	1	0	325
1	1	0	1	1	337.5
1	1	1	0	0	350
1	1	1	0	1	362.5
1	1	1	1	0	375
1	1	1	1	1	400

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**0x01 Core Current. Default 0x00 (read only). The core current full scale is over current trigger point.**

Bit6-0 : Show core voltage current.

**0x02 OC\_int Threshold. Default 0x00. The core current Hi-I threshold register.**

Bit7 : Disable/Enable.

0 : Disable 1 : Enable

Bit6-0 : Setting core voltage Hi-I current.

**0x03 MISC. Default 0x04.**

Bit6-5 : OC\_int threshold hysteresis

00 : 60% of OC\_int Threshold 01 : 70% of OC\_int Threshold

10 : 80% of OC\_int Threshold 11 : 90% of OC\_int Threshold

Bit4 : OC\_int mode

0 : OC\_int level mode 1 : OC\_int pluse mode

Bit3 : OC\_int delay

0 : Disable 1 : Enable

Bit2 : Slot\_OCC Detection. This bit be written clear and only can be written 0.

0 : Normal 1 : Slot\_OCC ever be pulled high

Bit1 : The reset pin ever be pull low when bit0 = 1 and only can be written 0.

0 : Never issue reset 1 : Ever issue reset

Bit0 : Reset control. Reset pin be pull low, if this bit = 1 will reset all registers to default exception MISC(Index 0x03).

0 : Disable 1 : Enable

Note : If SLOT\_OCC pin = 1 reset all registers value to default.

**0x04 Frequency Taxiing Configure. Default 0x00.**

Bit5-4 : Adjust frequency current source (RT pin).

00 : Default current value 01 : Default value \* 2/3 10 : Default value \* 1/3

Bit3-2 : Frequency taxi threshold.

00 : Core current threshold \* 1.1 01 : Core current threshold \* 1.2

10 : Core current threshold \* 1.3 11 : Core current threshold \* 1.4

Bit1-0 : Frequency taxi threshold hysteresis.

00 : Frequency taxi threshold \* 0.6 01 : Frequency taxi threshold \* 0.7

10 : Frequency taxi threshold \* 0.8 11 : Frequency taxi threshold \* 0.9

**Product information registers (Read Only)**

**0x14 Vendor\_LID                      0x62**

**0x15 Vendor\_HID                      0x14**

**0x16 Chip\_ID                            0x05**

**0x17 Revision\_ID                      0x00**

**Serial Bus address 0x5C**

The Slot\_OCC power consumption must less 1 $\mu$ A, when V<sub>DD</sub> disappear.

**DAC response time maximum 380 $\mu$ s.**

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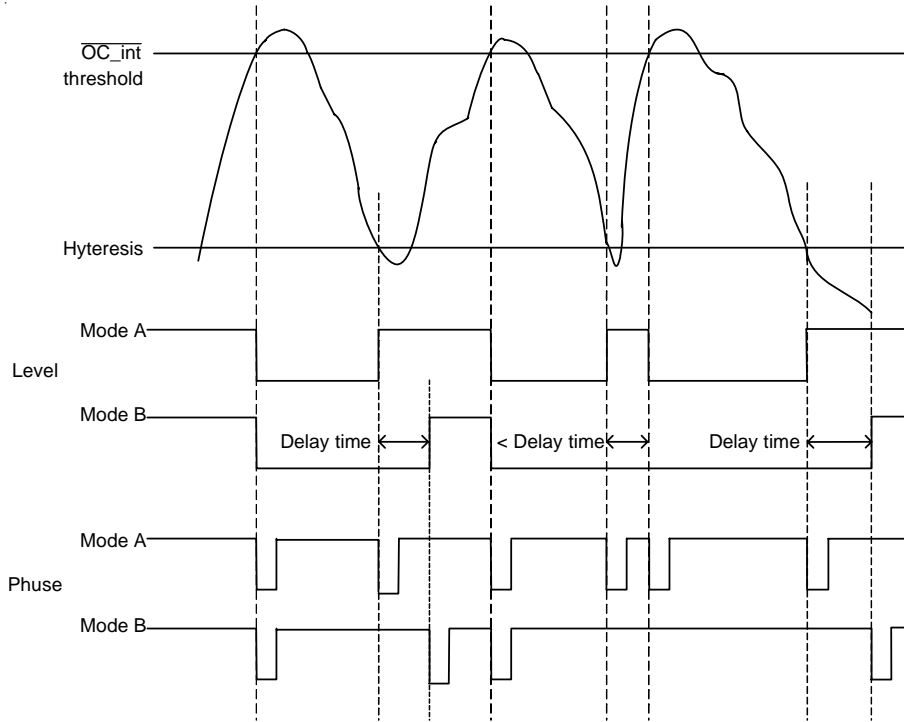


Figure 1. Hi-I Indicate

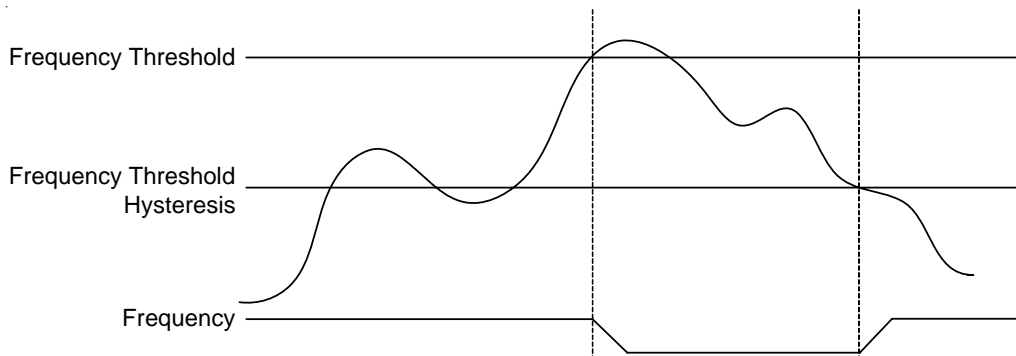


Figure 2. Switching Frequency

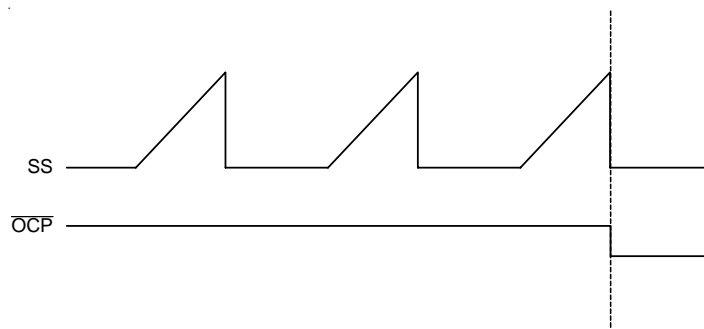


Figure 3. Over Current Protection



## Functional Pin Description

### SLOT\_OCC (Pin 1)

CPU socket occupied; the signal is defined to indicate if the CPU has been changed/ removed and it will reset all chip. There is one register implemented for the status indication. The register will be reset when the VDD power removed or CPU changed/removed. The pin is implemented as an input, TTL level, and active-low signal.

### DATA (Pin 2), CLK (Pin 3)

2-wires programming interface.

### $\overline{\text{RST}}$ (Pin 4)

This pin be pull low, it will reset some register, when 0x03 bit 0 be setting.

### $\overline{\text{OC\_INT}}$ (Pin 5)

The pin is signal low when the load current of CPU is higher than the threshold registers set after it complete VID and frequency Taxiing.

### $\overline{\text{OCP}}$ (Pin 6)

(OD) sink capacitor = 12mA. This pin is signal low when core current over OCP trigger point.

When DVD = Low & FB > 2V then OCP = Low.

When DVD = High & FB > 1.4(VID + Offset + Droop) then OCP = Low.

Till VDD disappear.

### IC\_OUT (Pin 7)

The pin is defined as a reference current output. A capacitor is attached to set the default threshold delay timer for Hi-I indication and frequency taxiing slope rate.

### FB (Pin 8)

The pin is defined as an inverting input of internal error amplifier.

### COMP (Pin 9)

The pin is defined as an output of the error amplifier and an input of the PWM comparator.

### SGND (Pin 10)

Difference ground sense of  $V_{\text{CORE}}$ .

### VOSS (Pin 11)

$V_{\text{CORE}}$  initial value offset. Connect this pin to GND with a resistor to set the offset value.

### DVD (Pin 12)

Hardware adjustable system power UVLO detection; input pin; the internal trip threshold = 0.9V at  $V_{\text{DVD}}$  rising.

### SS (Pin 13)

The pin is defined to set soft-start ramp rate; a capacitor is attached to set the start time interval. Pull this pin lower than 1.0V (ramp valley of saw-tooth wave in pulse width modulator) will shut the converter down.

### RT\_FLY (Pin 14)

The pin is defined to set the taxiing slope rate during operation frequency transfer. A capacitor is attached on the pin for the frequency taxiing slope rate setting.

### RT (Pin 15)

Default operation switching frequency setting. A resistor is attached to set the default operation frequency.

### CSN (Pin 16)

The pin is defined to sense load current of CPU. The pin should be connected to the output node of choke.

### ADJ (Pin 17)

Pin for active droop adjustment. An external resistor is attached to GND for load droop setting.

### CSP1 (Pin 21), CSP2 (Pin 20), CSP3 (Pin 19), CSP4 (Pin 18)

Current sense inputs from the individual converter channels.

### PWM1 (Pin 22), PWM2 (Pin 23), PWM3 (Pin 24), PWM4 (Pin 25)

PWM outputs for each phase switching drive.

### VDD (Pin 26)

Chip powers supply. Connect this pin to a 5VSB supply.

**VID4 (Pin 27), VID3 (Pin 28), VID2 (Pin 29),  
VID1 (Pin 30), VID0 (Pin 31), VID125 (Pin 32)**

DAC voltage identification; Input; The VID0~4 is implemented for VRM9.0 (5-bits) DAC identification; The VID0~4, VID125 is implemented for VRM10.X (6-bits) DAC identification. The pins are internally pulled to 1.2V (pull high 50μA) if left open.

**GND (Exposed Pad)**

Exposed pad should be soldered to PCB board and connected to GND.

**Function Block Diagram**

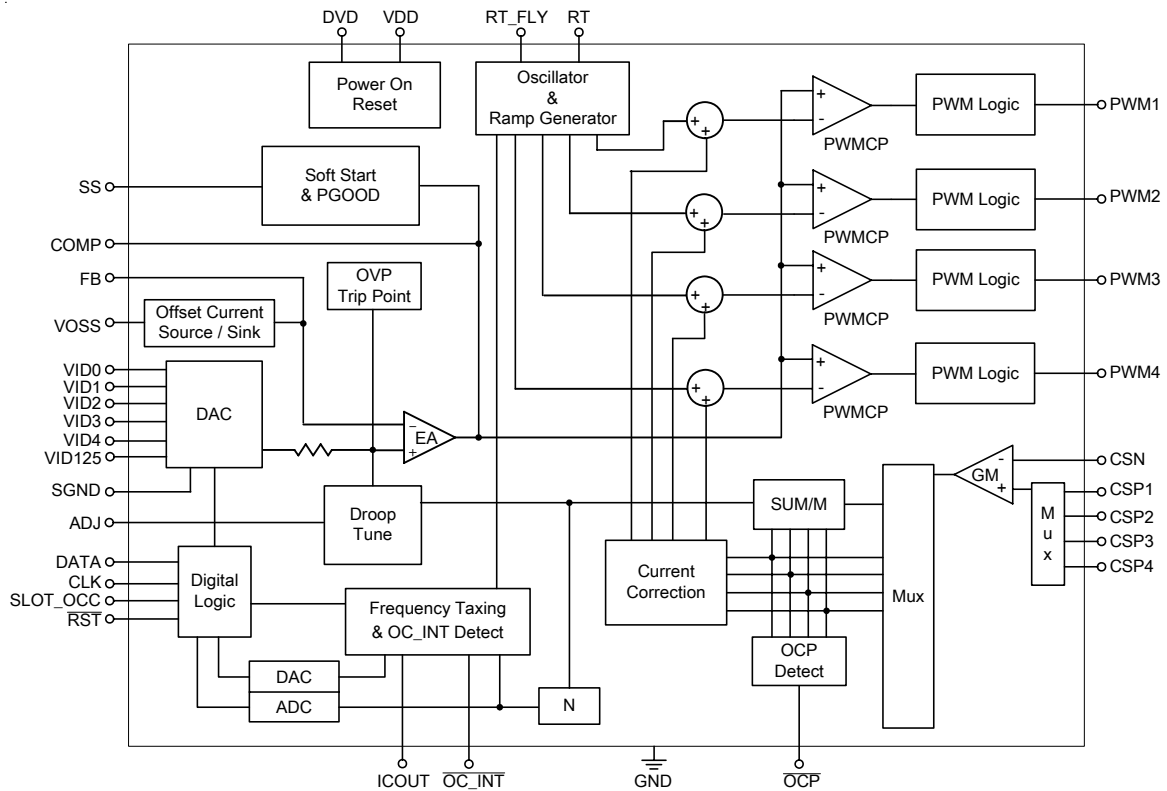


Table 1. Output Voltage Program

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	1	1	1	X	No CPU
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.850V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.875V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.900V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.925V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.950V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.025V
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.050V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.075V
0	0	0	0	0	0	1.0875V
1	1	1	1	0	1	1.100V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.125V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.150V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.175V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.200V
1	1	0	1	0	0	1.2125V

*To be continued*

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**Table 1. Output Voltage Program**

Pin Name						Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	VID125	
1	1	0	0	1	1	1.225V
1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.250V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.275V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.300V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.325V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.350V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.375V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.400V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.425V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.450V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.475V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.500V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.525V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.550V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.575V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Note: (1) 0 : Connected to GND  
 (2) 1 : Open  
 (3) X : Don't Care

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**Absolute Maximum Ratings** (Note 1)

- Supply Voltage,  $V_{DD}$  ..... 7V
- Input, Output or I/O Voltage ..... GND-0.3V to  $V_{DD}+0.3V$
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ C$   
 VQFN-32L 5x5 ..... 2.78W
- Package Thermal Resistance (Note 4)  
 VQFN-32L 5x5,  $\theta_{JA}$  ..... 36°C/W
- Junction Temperature ..... 150°C
- Lead Temperature (Soldering, 10 sec.) ..... 260°C
- Storage Temperature Range ..... -65°C to 150°C
- ESD Susceptibility (Note 2)  
 HBM (Human Body Mode) ..... 2kV  
 MM (Machine Mode) ..... 200V

**Recommended Operating Conditions** (Note 3)

- Supply Voltage,  $V_{DD}$  ..... 5V ± 10%
- Ambient Temperature Range ..... 0°C to 70°C
- Junction Temperature Range ..... 0°C to 125°C

**Electrical Characteristics**

( $V_{DD} = 5V$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
<b><math>V_{DD}</math> Supply Current</b>							
Nominal Supply Current		$I_{DD}$	PWM 1,2,3,4 Open	--	12	16	mA
<b>Power-On Reset</b>							
POR Threshold		$V_{DDRTH}$	$V_{CC}$ Rising	4.0	4.2	4.5	V
Hysteresis		$V_{DDHYS}$		0.2	0.5	--	V
$V_{DVID}$ Threshold	Trip (Low to High)	$V_{DVIDTP}$	Enable	0.8	0.9	1.0	V
	Hysteresis	$V_{DVIDHYS}$		--	70	--	mV
<b>Oscillator</b>							
Free Running Frequency		$f_{OSC}$	$R_{RT} = 22.5k\Omega$	250	300	350	kHz
Frequency Adjustable Range		$f_{OSC\_ADJ}$		50	--	400	kHz
Ramp Amplitude		$\Delta V_{OSC}$	$R_{RT} = 22.5k\Omega$	--	1.9	--	V
Ramp Valley		$V_{RV}$		0.7	1.0	--	V
Maximum On-Time of Each Channel				62	66	75	%
RT Pin Voltage		$V_{RT}$	$R_{RT} = 22.5k\Omega$	1.7	1.8	1.9	V
<b>Reference and DAC</b>							
DACOUT Voltage Accuracy		$\Delta V_{DAC}$	$V_{DAC} \geq 1V$	-1	--	+1	%
			$V_{DAC} < 1V$	-10	--	+10	mV

To be continued

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DAC (VID0-VID125) Input Low	VILDAC		--	--	0.3	V
DAC (VID0-VID125) Input High	VIHDAC		0.8	--	--	V
Offset Voltage			-3	--	3	%
VOSS Pin Voltage	VVOSS	RVOSS = 100kΩ	1.6	1.7	1.8	V
<b>Error Amplifier</b>						
DC Gain			--	85	--	dB
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR	C <sub>COMP</sub> = 10pF	--	3	--	V/μs
<b>Current Sense GM Amplifier</b>						
CSN Full Scale Source Current	IISPFSS		150	--	--	μA
CSN Current for OCP			--	150	--	μA
<b>Protection</b>						
SS Current	I <sub>SS</sub>	V <sub>SS</sub> = 1V	8	13	18	μA
Over-Voltage Trip	$\frac{V_{SEN}}{V_{DACOUT} + V_{OFFSET}}$	ΔOVT	130	140	150	%

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

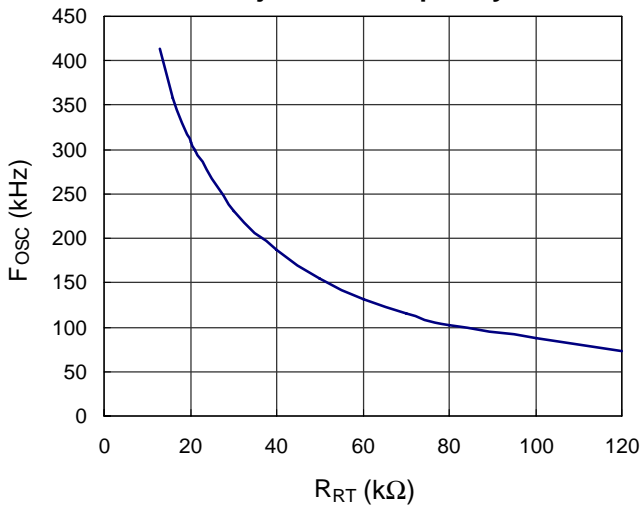
**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.** The device is not guaranteed to function outside its operating conditions.

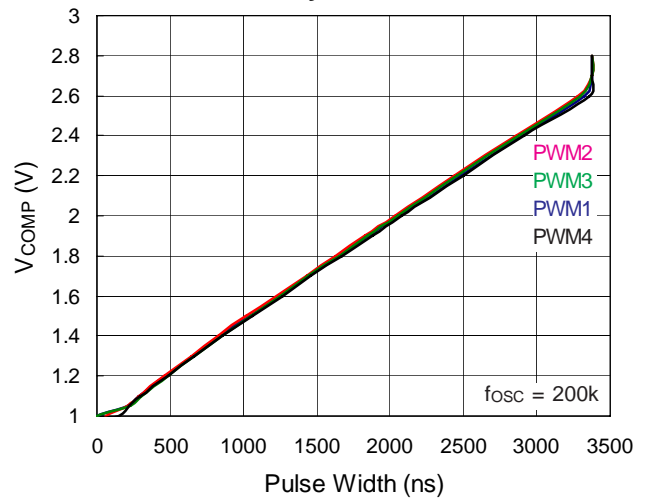
**Note 4.** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

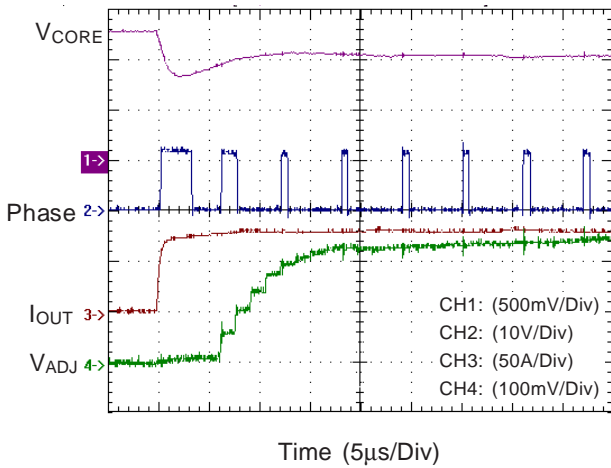
Adjustable Frequency



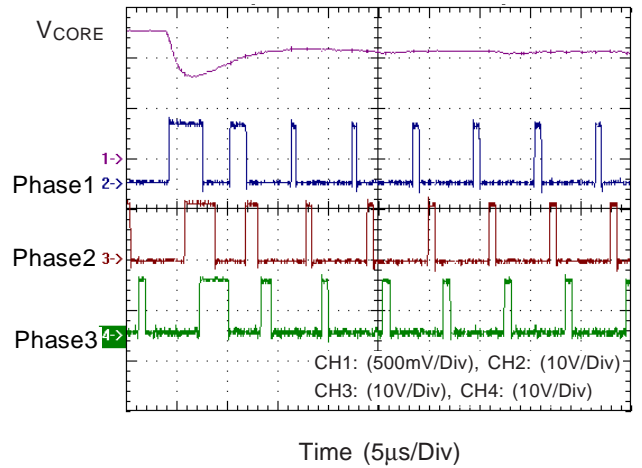
Linearity of each PWM



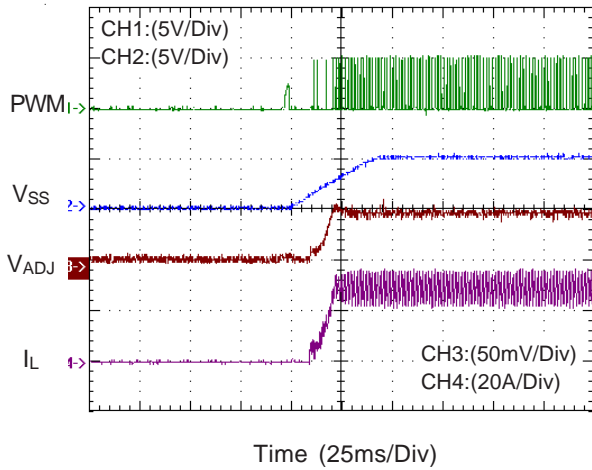
Load Transient Response



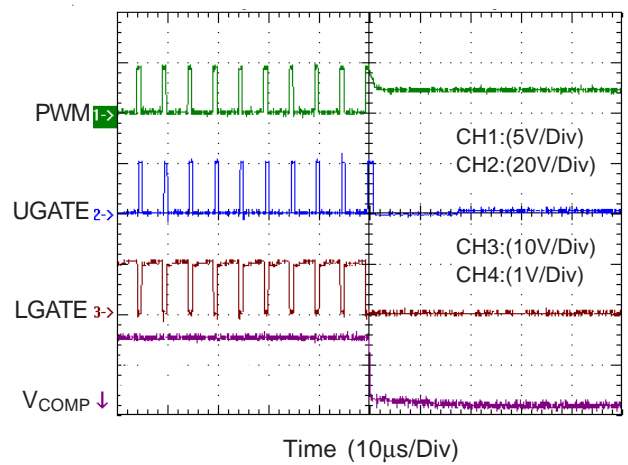
Load Transient Response



Relationship Between Inductor Current and Vadj

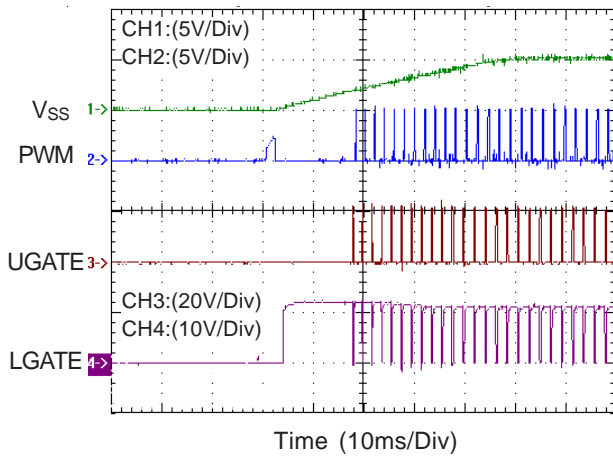


Power-Off @ Iout = 60A



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**Power-On @ I<sub>OUT</sub> = 60A**



## Application Information

MS-10 is a multi-phase DC/DC controller that precisely regulates CPU core voltage and balances the current of different power channels. The converter consisting of MS-10 and its companion MOSFET driver RT9607/RT9607A provides high quality CPU power and all protection functions to meet the requirement of modern VRM.

### Voltage Control

MS-10 senses the CPU  $V_{CORE}$  by SGND pin to sense the return of CPU to minimize the voltage drop on PCB trace at heavy load. OVP is sensed at FB pin. The internal high accuracy VID DAC provides the reference voltage for VRD10.X compliance. Control loop consists of error amplifier, multi-phase pulse width modulator, driver and power components. As conventional voltage mode PWM controller, the output voltage is locked at the  $V_{REF}$  of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals of different channels are generated by comparison of EA output and split-phase sawtooth wave. Power stage transforms  $V_{IN}$  to output by PWM signal on-time ratio.

### Current Balance

MS-10 senses the inductor current via inductor's DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal balance circuit.

The current balance circuit sums and averages the current signals and then produces the balancing signals injected to pulse width modulator. If the current of some power channel is larger than average, the balancing signal reduces that channels pulse width to keep current balance. The use of single GM amplifier via time sharing technique to sense all inductor currents can reduce the offset errors and linearity variation between GMs. Thus it can greatly improve signal processing especially when dealing with such small signal as voltage drop across DCR.

### Load Droop

The sensed power channel current signals regulate the reference of DAC to form an output voltage droop proportional to the load current. The droop or so call "active voltage positioning" can reduce the output voltage ripple at load transient and the LC filter size.

### Fault Detection

The chip detects FB for over voltage. The "hiccup mode" operation of over current protection is adopted to reduce the short circuit current. The inrush current at the start up is suppressed by the soft start circuit through clamping the pulse width and output voltage.

### Phase Setting and Converter Start Up

MS-10 interfaces with companion MOSFET drivers (like RT9619, RT9607 series) for correct converter initialization. The tri-state PWM output (high, low and high impedance) senses its interface voltage when IC POR acts (both  $V_{DD}$  and DVD trip). The channel is enabled if the pin voltage is 1.2V less than  $V_{DD}$ . Tie the PWM to  $V_{DD}$  and the corresponding current sense pins to GND or left float if the channel is unused. For example, for 3-Channel application, connect PWM4 high.

### Current Sensing Setting

MS-10 senses the current flowing through inductor via its DCR for channel current balance and droop tuning. The differential sensing GM amplifier converts the voltage on the sense component (can be a sense resistor or the DCR of the inductor) to current signal into internal circuit (see Figure 1).

$$\frac{L}{DCR} = R \times C \quad V_C = DCR \times I_L \quad I_X = \frac{V_C}{R_{CSN}}$$

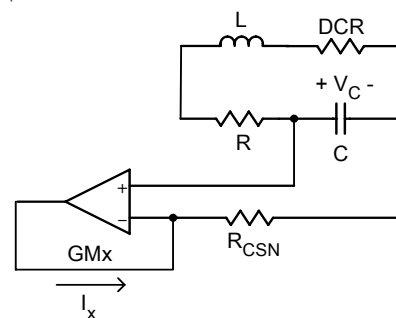


Figure 1. Current Sense Circuit

Figure 2 is the test circuit for GM. We apply test signal at GM inputs and observe its signal process output at ADJ pin. Figure 3 shows the variation of signal processing of all channels. We observe zero offsets and good linearity between phases.

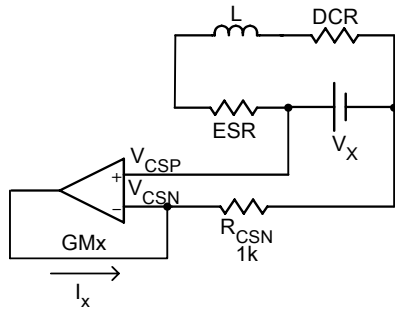


Figure 2. The Test Circuit of GM

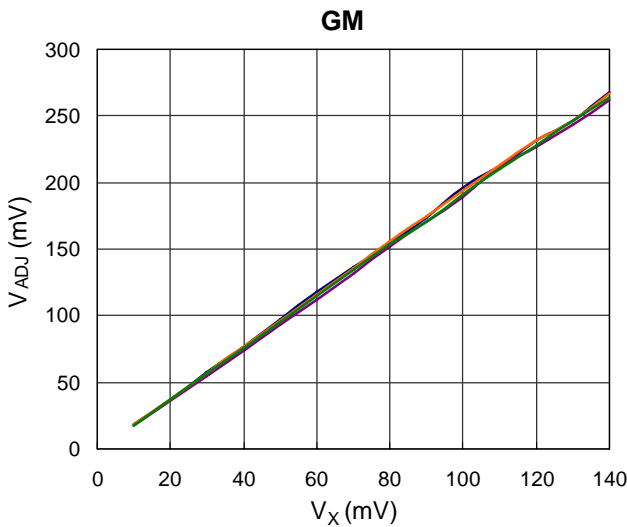


Figure 3. The Linearity of GMx

Figure 4 shows the time sharing technique of GM amplifier. We apply test signal at phase 4 and observe the waveforms at both pins of GM amplifier. The waveforms show time sharing mechanism and the performance of GM to hold both input pins equal when the shared time is on.

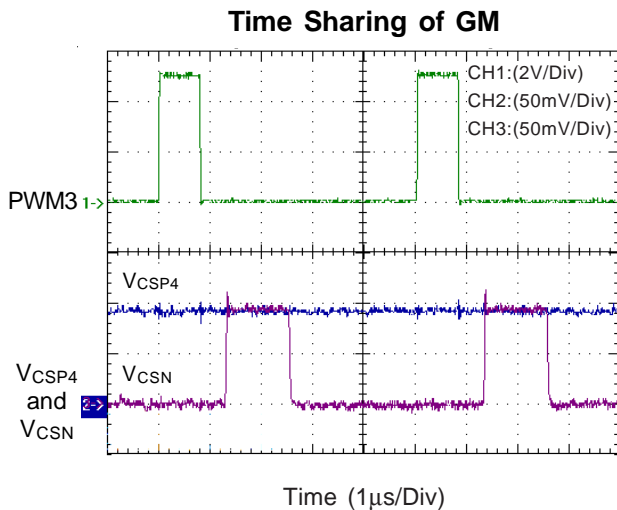


Figure 4

**Over Current Protection**

MS-10 uses an external resistor  $R_{CSN}$  to set a programmable over current trip point. OCP comparator compares each inductor current with this reference current. MS-10 uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground.

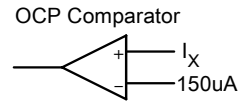


Figure 5. Over Current Comparator

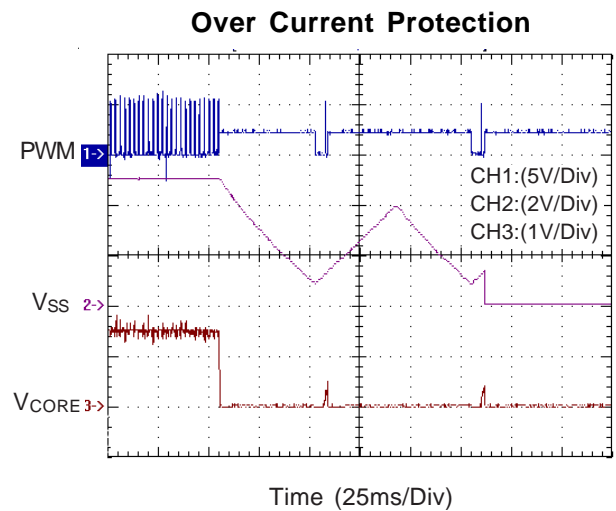


Figure 6. Over Current Protection at steady state

**Current Ratio Setting**

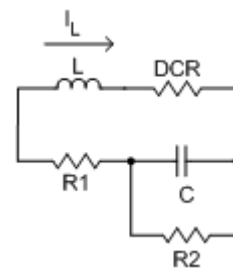


Figure 7. Application circuit for current ratio setting

For some case with preferable current ratio instead of current balance, the corresponding technique is provided. Due to different physical environment of each channel, it is necessary to slightly adjust current loading between channels. Figure 7 shows the application circuit of GM for current ratio requirement. Applying KVL along  $L+DCR$  branch and  $R1+C//R2$  branch:

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$$L \frac{dI_L}{dt} + DCR \times I_L = R_1 \left( \frac{V_C}{R_2} + C \frac{dV_C}{dt} \right) + V_C$$

$$= R_1 C \frac{dV_C}{dt} + \frac{R_1 + R_2}{R_2} V_C$$

$$\text{For } V_C = \frac{R_2}{R_1 + R_2} DCR \times I_L$$

Look for its corresponding conditions:

$$L \frac{dI_L}{dt} + DCR \times I_L = (R_1 // R_2) \times C \times DCR \times \frac{dI_L}{dt} + DCR \times I_L$$

$$\text{Let } \frac{L}{DCR} = (R_1 // R_2) \times C$$

$$\text{Thus if } \frac{L}{DCR} = (R_1 // R_2) \times C$$

$$\text{Then } V_C = \frac{R_2}{R_1 + R_2} \times DCR \times I_L$$

With internal current balance function, this phase would share  $(R_1 + R_2) / R_2$  times current than other phases. Figure 8 & 9 show different settings for the power stages. Figure 10 shows the performance of current ratio compared with conventional current balance function in Figure 11.

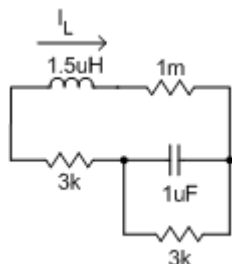


Figure 8. GM4 Setting for current ratio function

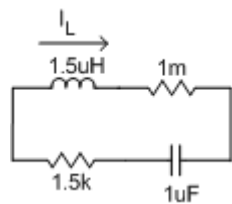


Figure 9. GM1~3 Setting for current ratio function

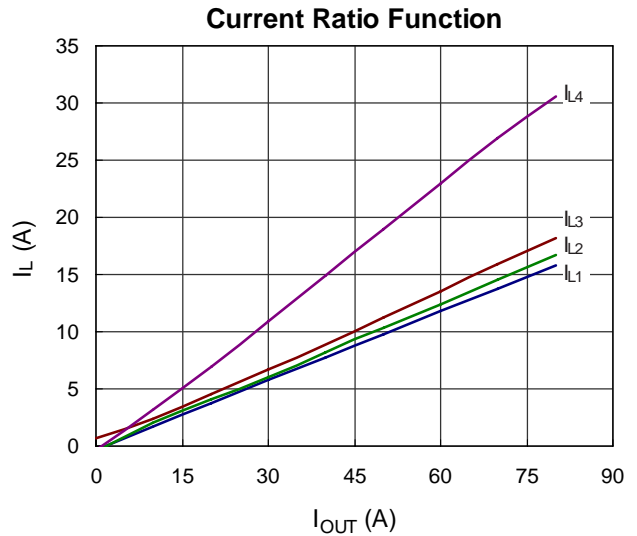


Figure 10

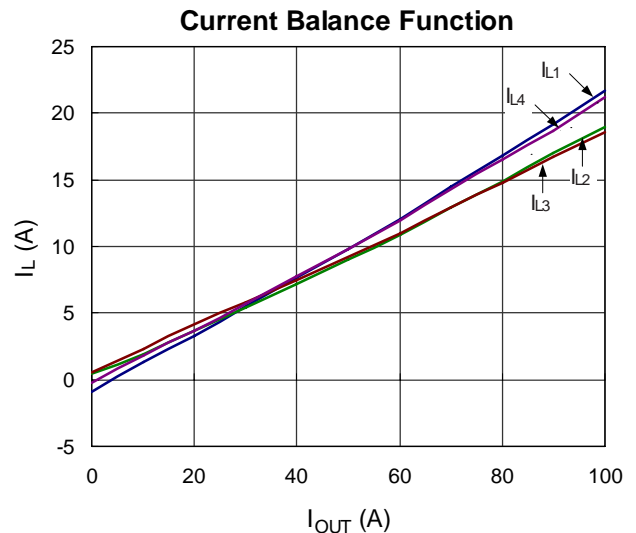


Figure 11

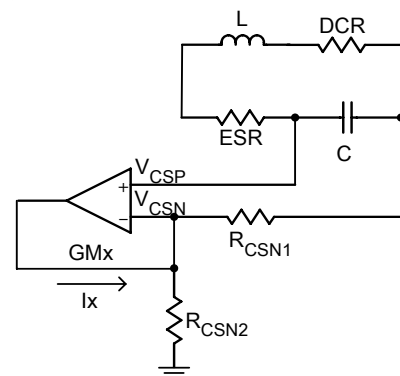


Figure 12. Application circuit of GM



For load line design, with application circuit in Figure 12, it can eliminate the dead zone of load line at light loads.

$$V_{CSP} = V_{OUT} + I_L \times DCR$$

if GM holds input voltages equal, then

$$V_{CSP} = V_{CSN}$$

$$I_X = \frac{V_{CSN}}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN1}}$$

$$= \frac{V_{OUT} + I_L \times DCR}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN1}}$$

$$= \frac{V_{OUT}}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN1}}$$

For the lack of sinking capability of GM,  $R_{CSN2}$  should be small enough to compensate the negative inductor valley current especially at light loads.

$$\frac{V_{CSN}}{R_{CSN2}} \geq \left| \frac{I_L \times DCR}{R_{CSN1}} \right|$$

Assume the negative inductor valley current is  $-5A$  at no load, then for

$$R_{CSN1} = 330\Omega, R_{ADJ} = 160\Omega, V_{OUT} = 1.300V$$

$$\frac{1.3V}{R_{CSN2}} \geq \left| \frac{-5A \times 1m\Omega}{330\Omega} \right|$$

$$R_{CSN2} \leq 85.8k\Omega$$

Choose  $R_{CSN2} = 82k\Omega$

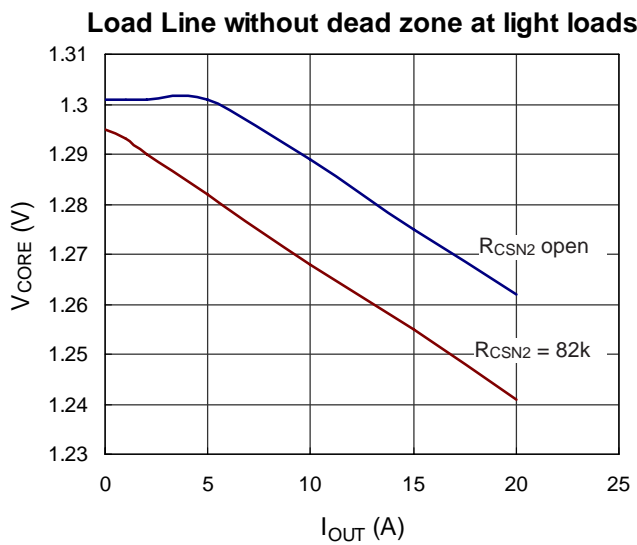


Figure 13

**VID on the Fly**

With external pull up resistors tied to VID pins, MS-10 converters different VID codes from CPU into output voltage. Figure 14 and Figure 15 show the waveforms of VID on the fly function.

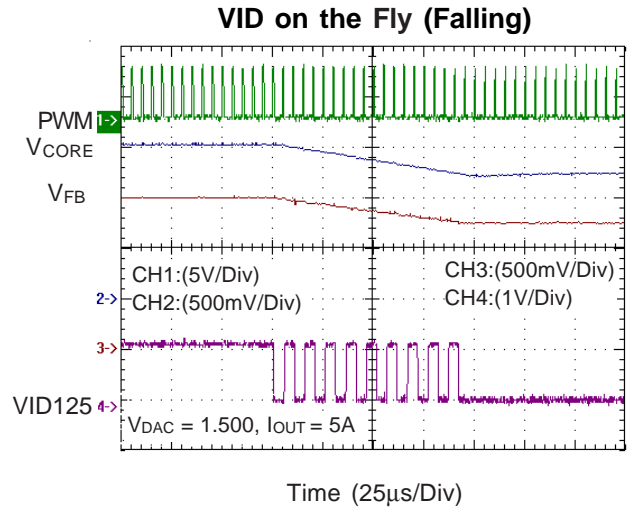


Figure 14

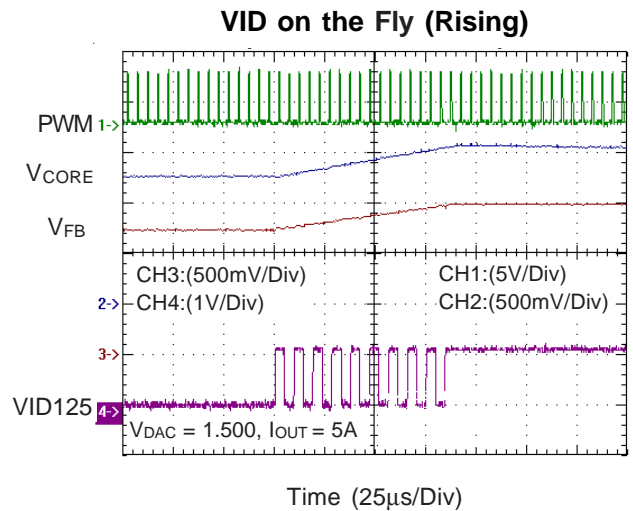


Figure 15

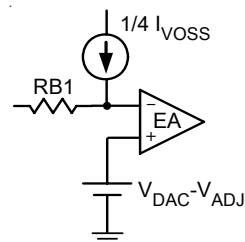


Figure 16

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**Output Voltage Offset Function**

To meet Intel® requirement of initial offset of load line, MS-10 provides programmable initial offset function. External resistor  $R_{VOSS}$  and voltage source at VOSS pin generate offset current  $I_{VOSS} = \frac{V_{VOSS}}{R_{VOSS}}$ . One quarter of  $I_{VOSS}$  flows through  $R_{B1}$  as shown in Figure 16. Error amplifier would hold the inverting pin equal to  $V_{DAC} - V_{ADJ}$ . Thus output voltage is subtracted from  $V_{DAC} - V_{ADJ}$  for a constant offset voltage.

$$V_{CORE} = V_{DAC} - V_{ADJ} - \frac{R_{FB1}}{4 \times R_{VOSS}}$$

A positive output voltage offset is possible by connecting  $R_{VOSS}$  to VDD instead of to GND. Please note that when  $R_{VOSS}$  is connected to VDD,  $V_{VOSS}$  is  $V_{DD} - 2V$  typically and half of  $I_{VOSS}$  flows through  $R_{FB1}$ .  $V_{CORE}$  is rewritten as:

$$V_{CORE} = V_{DAC} - V_{ADJ} + \frac{R_{FB1}}{R_{VOSS}}$$

**Error Amplifier Characteristic**

For fast response of converter to meet stringent output current transient response, MS-10 provides large slew rate capability and high gain-bandwidth performance.

**EA Falling Slew Rate**

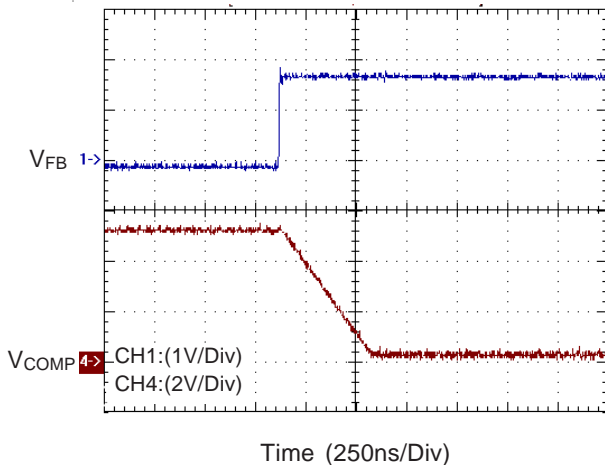


Figure 18. EA Rising Transient with 10pF Loading; Slew Rate = 10V/us

**EA Rising Slew Rate**

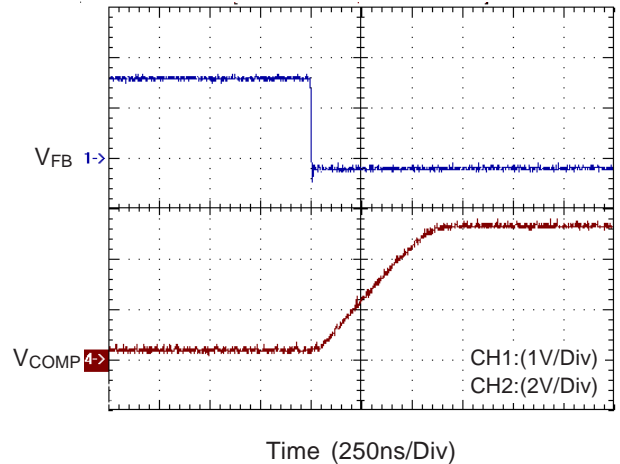


Figure 19. EA Falling Transient with 10pF Loading; Slew Rate = 8V/us

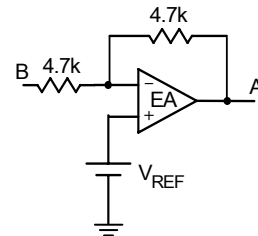


Figure 20. Gain-Bandwidth Measurement by signal A divided by signal B

**Design Procedure Suggestion**

- a. Output filter pole and zero (Inductor, output capacitor value & ESR).
- b. Error amplifier compensation & sawtooth wave amplitude (compensation network).
- c. Kelvin sense for  $V_{CORE}$ .

**Current Loop Setting**

- a. GM amplifier S/H current (current sense component DCR, CSN pin external resistor value).
- b. Over-current protection trip point ( $R_{IMAX}$  resistor).

**VRM Load Line Setting**

- a. Droop amplitude (ADJ pin resistor).
- b. No load offset ( $R_{CSN2}$ )
- c. DAC offset voltage setting (VOSS pin & compensation network resistor  $R_{B1}$ ).

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**Power Sequence & SS**

DVD pin external resistor and SS pin capacitor.

**PCB Layout**

- a. Kelvin sense for current sense GM amplifier input.
- b. Refer to layout guide for other items.

**Voltage Loop Setting**

**Design Example**

**Given:**

Apply for four phase converter

$V_{IN} = 12V$

$V_{CORE} = 1.5V$

$I_{LOAD (MAX)} = 100A$

$V_{DROOP} = 100mV$  at full load (1mΩ Load Line)

OCP trip point set at 40A for each channel (S/H)

DCR = 1mΩ of inductor at 25°C

$L = 1.5\mu H$

$C_{OUT} = 8000\mu F$  with 5mΩ equivalent ESR.

**1. Compensation Setting**

a. Modulator Gain, Pole and Zero :

From the following formula :

Modulator Gain =  $V_{IN}/V_{RAMP} = 12/1.9 = 6.3$  (i.e 16dB)

where  $V_{RAMP}$  : ramp amplitude of saw-tooth wave

LC Filter Pole = = 1.45kHz and

ESR Zero = 3.98kHz

b. EA Compensation Network :

Select  $R1 = 4.7k$ ,  $R2 = 15k$ ,  $C1 = 12nF$ ,  $C2 = 68pF$  and use the Type 2 compensation scheme shown in Figure 21. By calculation, the  $FZ = 0.88kHz$ ,  $FP = 322kHz$  and Middle Band Gain is 3.19 (i.e 10.07dB).

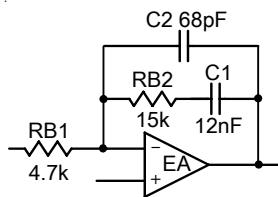


Figure 21. Type 2 compensation network of EA

The bode plot of EA compensation is shown as Figure 23.

The bode plot of power stage is shown as Figure 24. The total loop gain is in Figure 25.

**2. Over-Current Protection Setting**

Consider the temperature coefficient of copper 3900ppm/°C,

$$\frac{I_L \times DCR}{R_{CSN}} = 150\mu A$$

$$R_{CSN} = \frac{40A \times 1.39m\Omega}{150\mu A}$$

$$R_{CSN} = 370\Omega$$

**3. Soft-Start Capacitor Selection**

For most application cases, 0.1μF is a good engineering value.

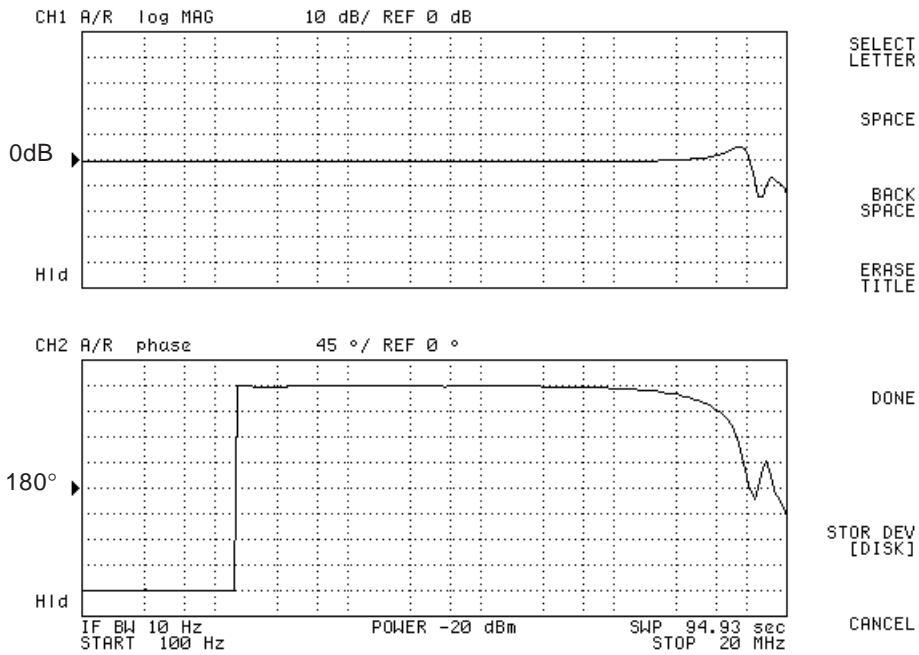


Figure 22. EA Frequency Response with closed loop gain set at 0db to observe gain-bandwidth product; -3dB at 10.86MHz

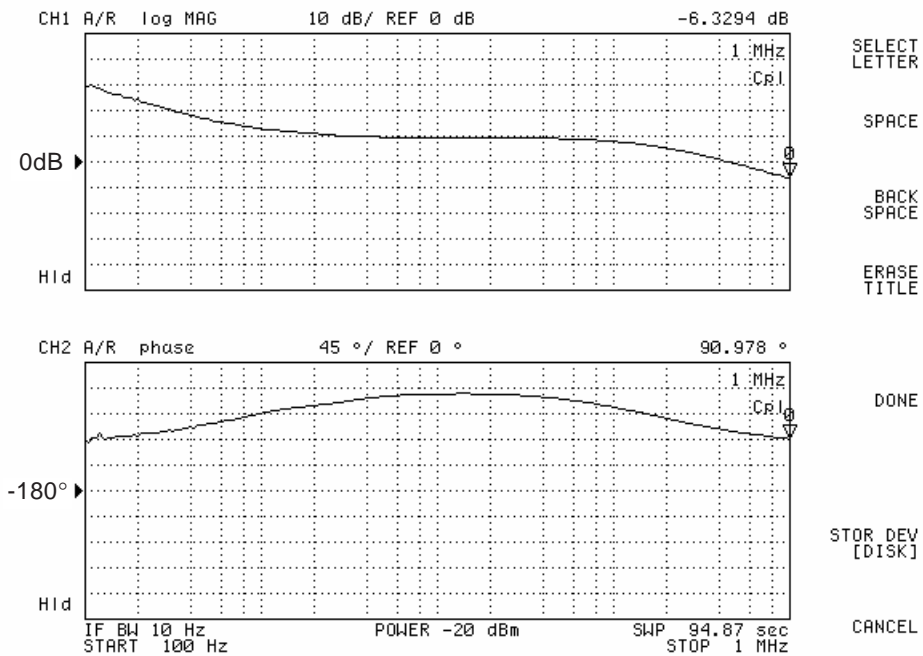


Figure 23. The Frequency Response of the Compensator Network

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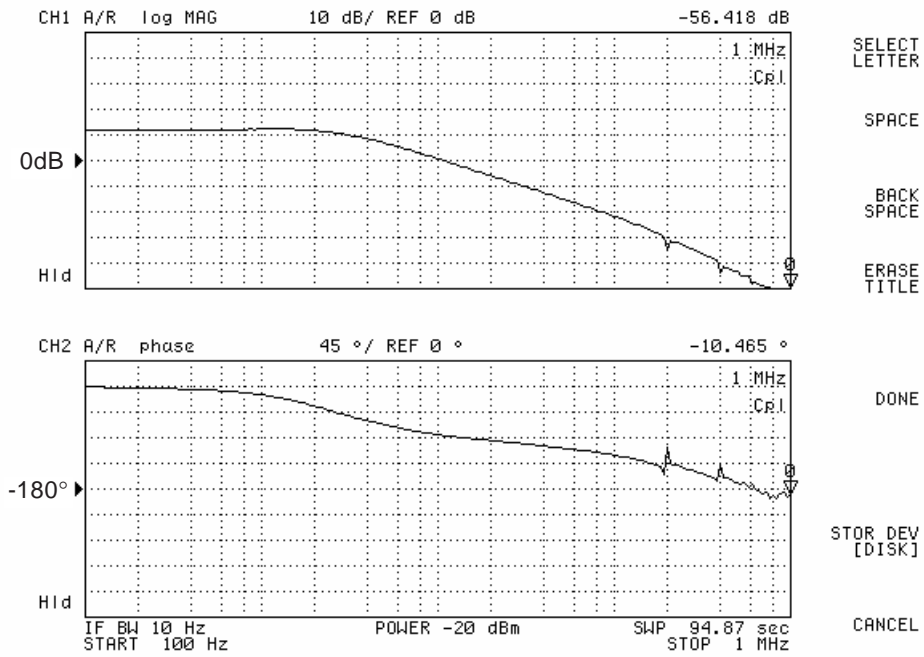


Figure 24. The Frequency Response of Power Stage

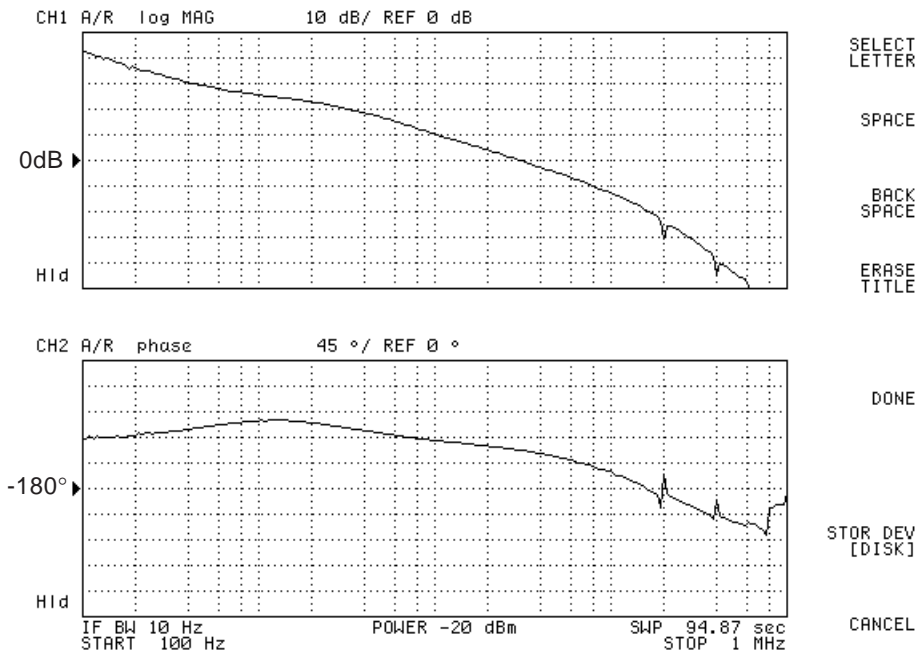


Figure 25. The Loop Gain of Converter

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## Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. **Most critical path: the current sense circuit is the most sensitive part of the converter. The current sense resistors tied to CSP1,2,3,4 and CSN should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. Kelvin connection of the sense component (additional sense resistor or Inductor DCR) ensures the accurate stable current sensing.**

### **Keep well Kelvin sense to ensure the stable operation!**

2. Switching ripple current path:
  - a. Input capacitor to high side MOSFET.
  - b. Low side MOSFET to output capacitor.
  - c. The return path of input and output capacitor.
  - d. Separate the power and signal GND.
  - e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.
  - f. Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.
3. MOSFET driver should be closed to MOSFET.
4. The compensation, bypass and other function setting components should be near the IC and away from the noisy power path.

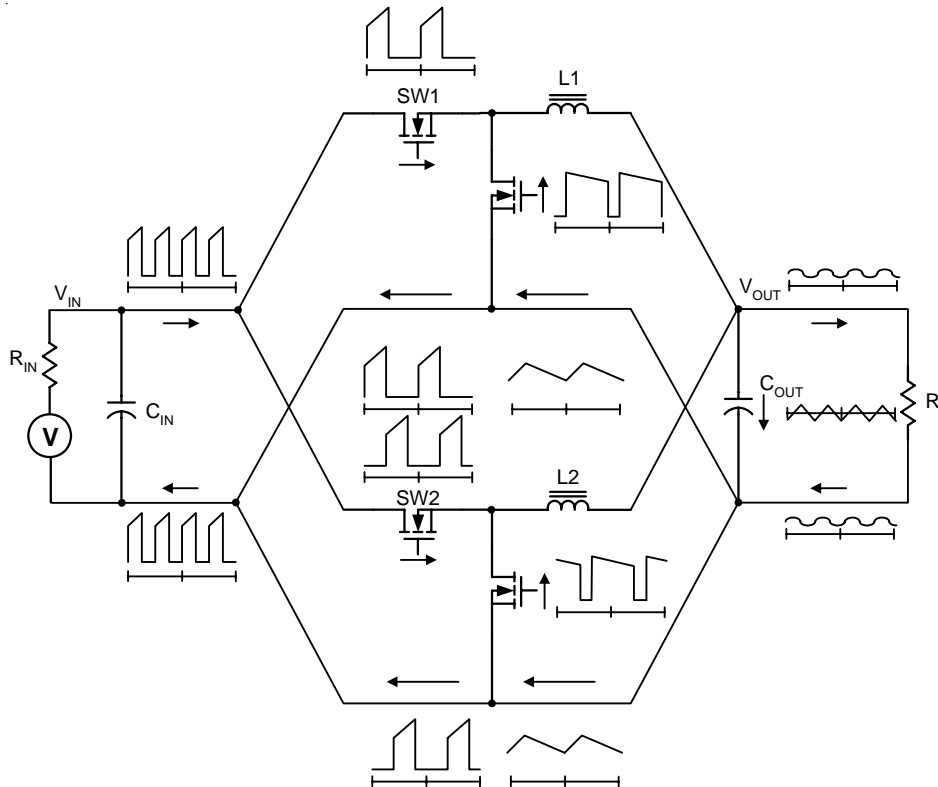


Figure 26. Power Stage Ripple Current Path

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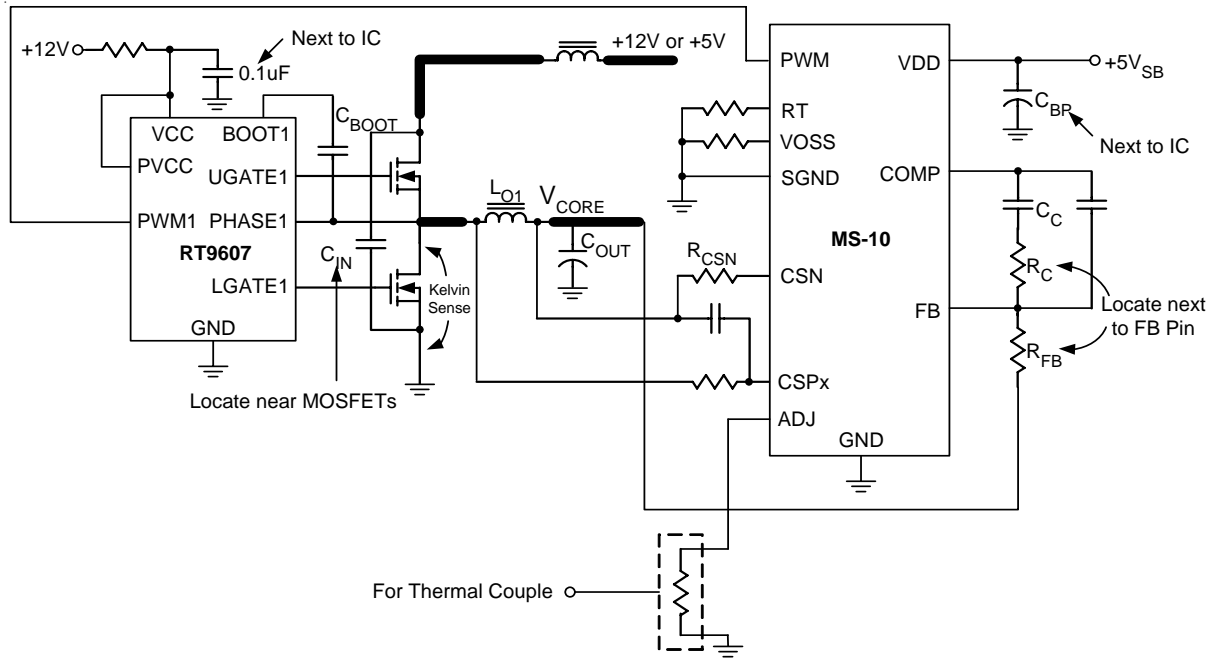


Figure 27. Layout Consideration

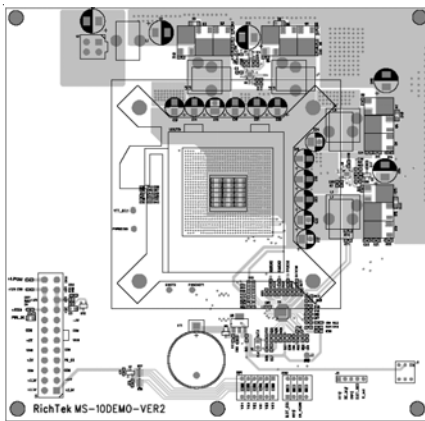


Figure 28

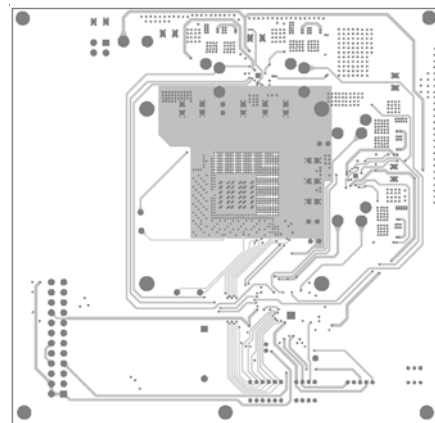


Figure 30

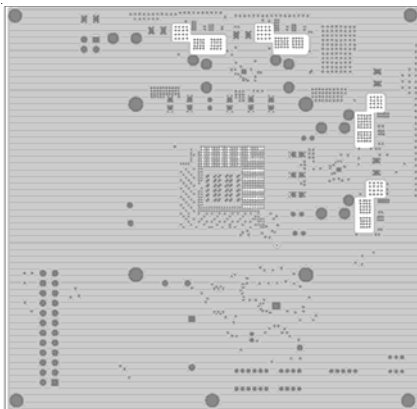


Figure 29

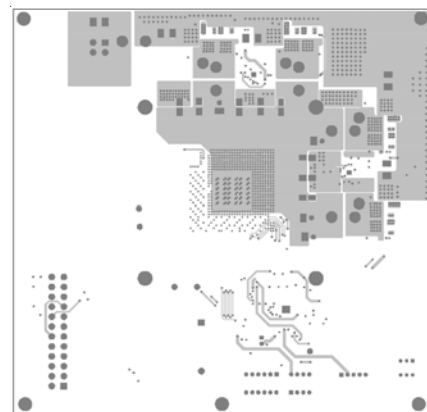
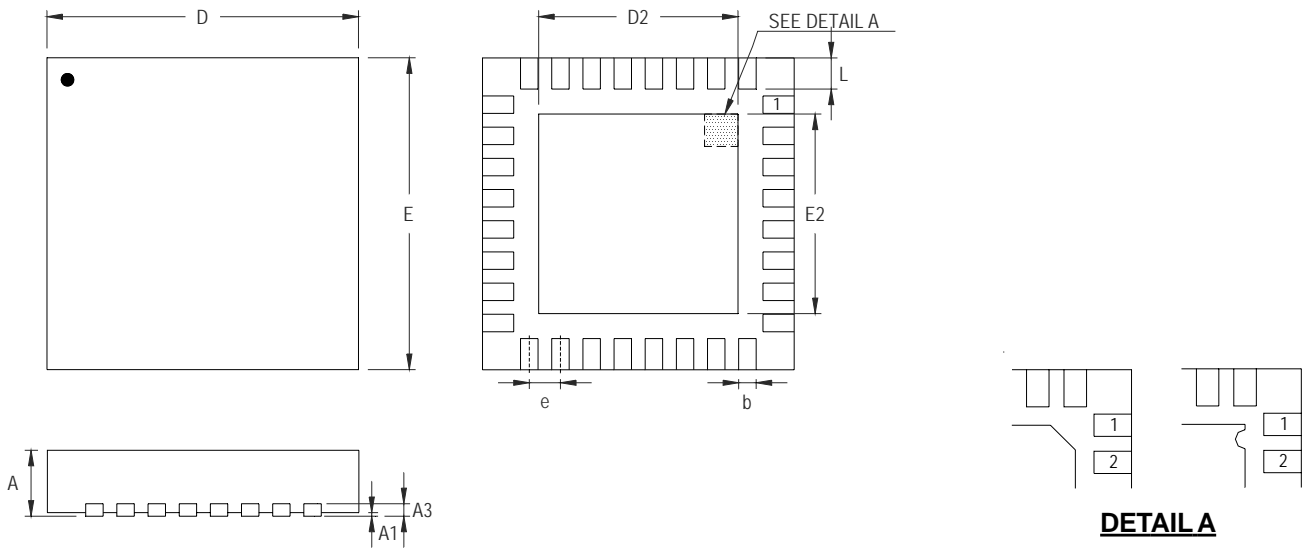


Figure 31

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**Outline Dimension**



**DETAIL A**  
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.500	3.750	0.138	0.148
E	4.950	5.050	0.195	0.199
E2	3.500	3.750	0.138	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

**V-Type 32L QFN 5x5 Package**

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