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# MS-7360

ATX Version: 0A

**CPU:** Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

**System Chipset:**

Intel Bearlake - Q/G/P (G33, P35, Q35/33North Bridge)  
Intel ICH9 (South Bridge)

**On Board Device:**

CLOCK Gen -- ICS 9LPRS900  
LPC Super I/O -- Fintek F71882F  
LAN -- Realtek 8111 (PCIE)  
HD Audio Codec -- ALC888  
1394 Controller -- VT6307 / VT6308 (2-port)  
PCIE to PATA/SATA Bridge -- Marvel 88SE6111

**Main Memory:**

Dual-channel DDR-II \* 4


**Expansion Slots:**

PCI EXPRESS X16 SLOT \*3  
PCI SLOT \* 2

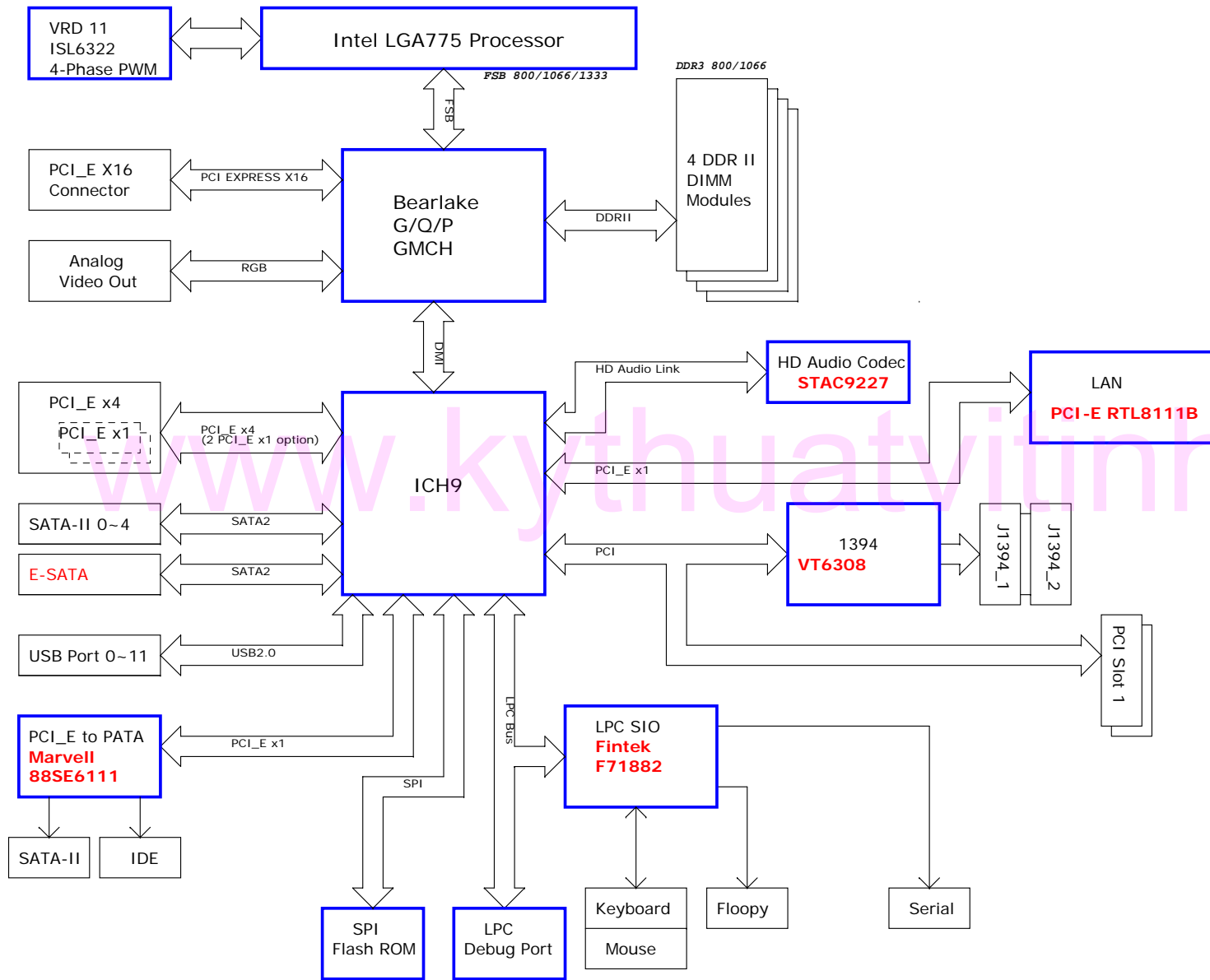
**PWM:** Intersil ISL6322 (3 Phases) w/ ISL6612 driver

Configuration and BOM match up

Option	Function	Orcad Configure	BOM
STD	Bearlake-G/ICH9/ICH-Fan/Non-PCIEx4	cfg-STD	601-72345-A10

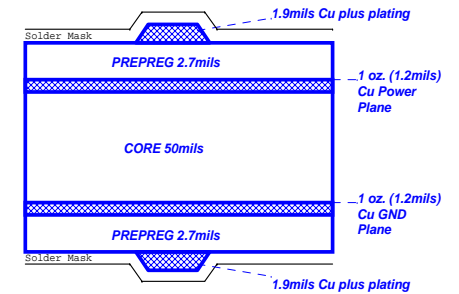
	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7360</b>		
Size Custom	Document Description <b>COVER SHEET</b>	Rev 1.0	
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# Block Diagram



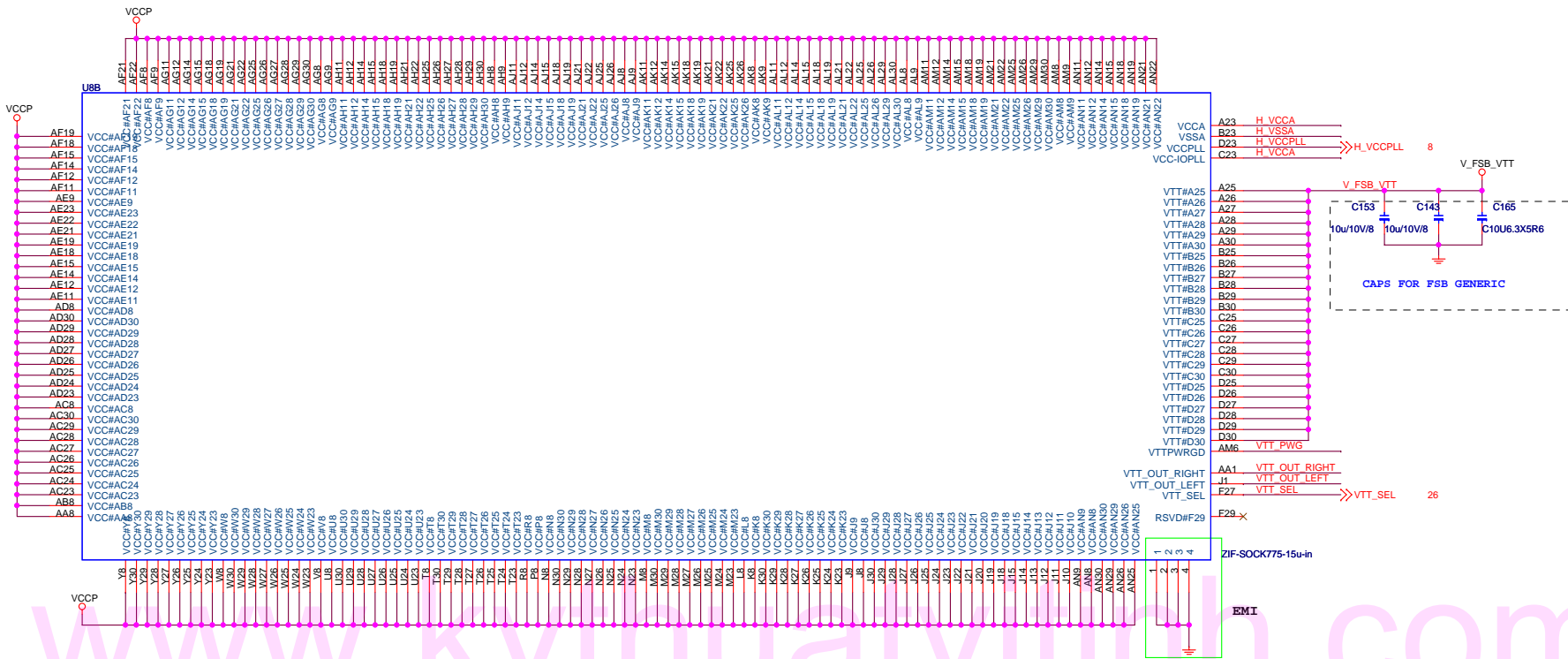
## Board Stack-up

(1080 Prepreg Considerations)

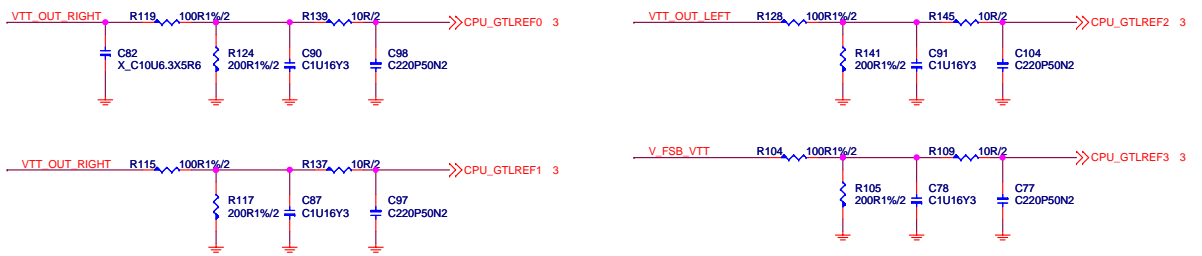


Single End 50ohm Top/Bottom : 4mils  
 USB2.0 - 90ohm : 15/4.5/7.5/4.5/15  
 SATA - 95ohm : 15/4/8/4/15  
 LAN - 100ohm : 15/4/8/4/15  
 PCIE - 95ohm : 15/4/8/4/15  
 IEEE1394 - 110ohm : 15/4/9/4/15  
 IDE : 15/4/8/4/15

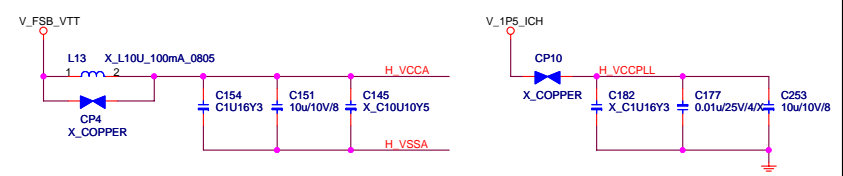




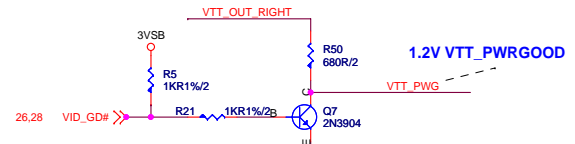
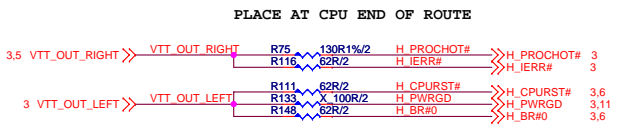
\*GTLREF VOLTAGE SHOULD BE  
0.67 \* VTT = 0.8V (At VTT=1.2V)



\*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET  
\*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS

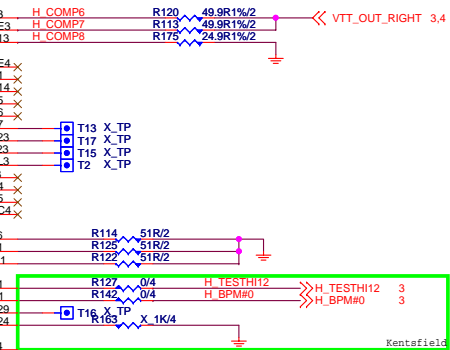
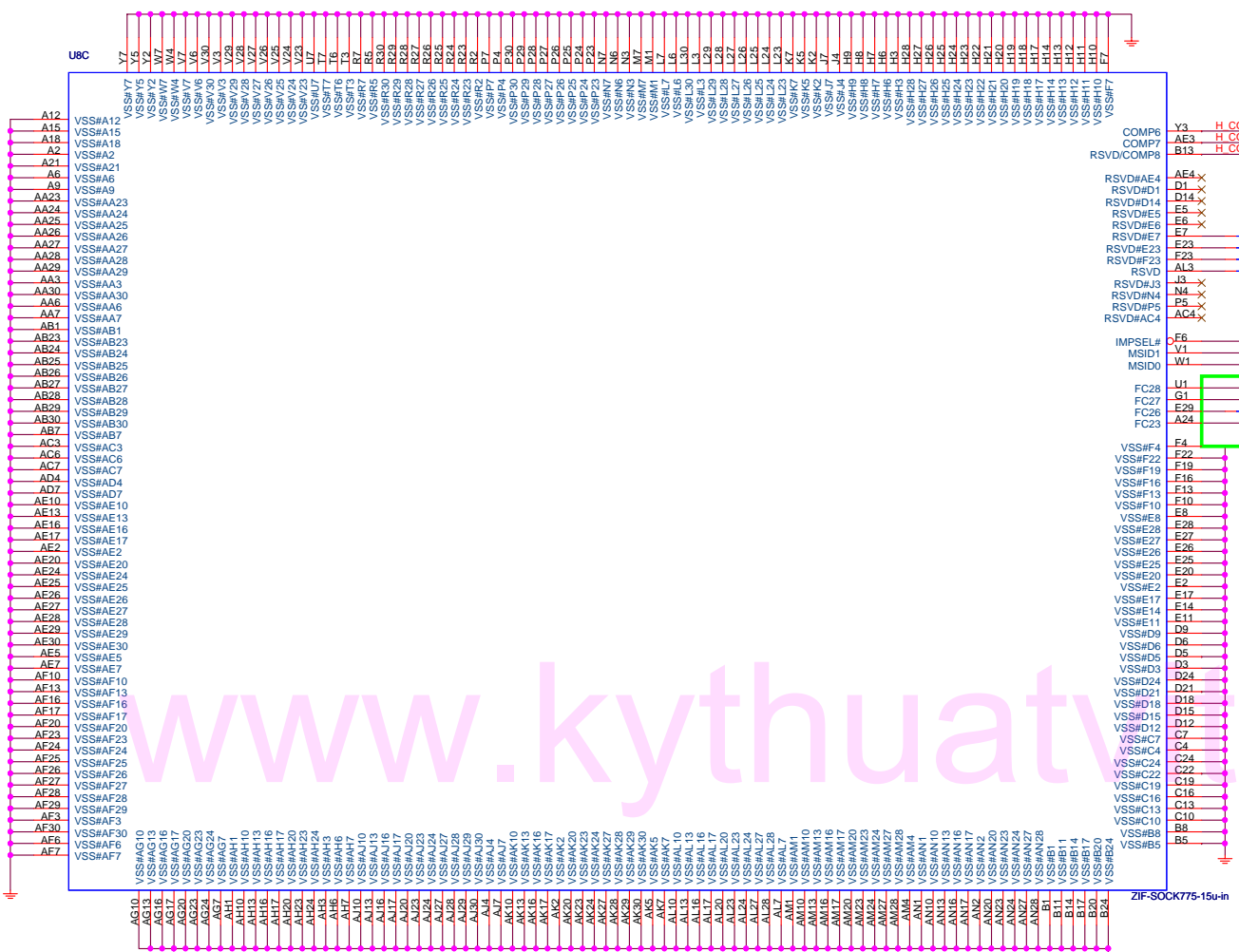


### VTT PWRGOOD



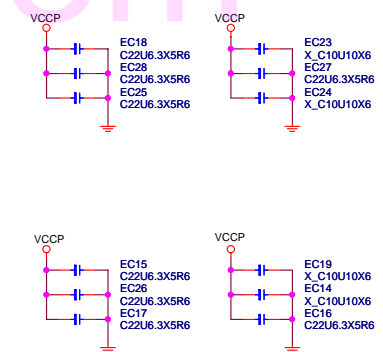
VTT\_PWG SPEC :  
High > 0.9V  
Low < 0.3V  
Trise < 150ns

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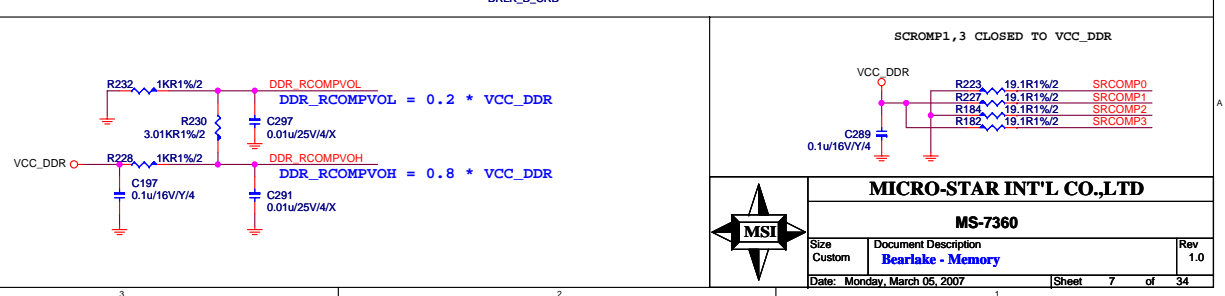
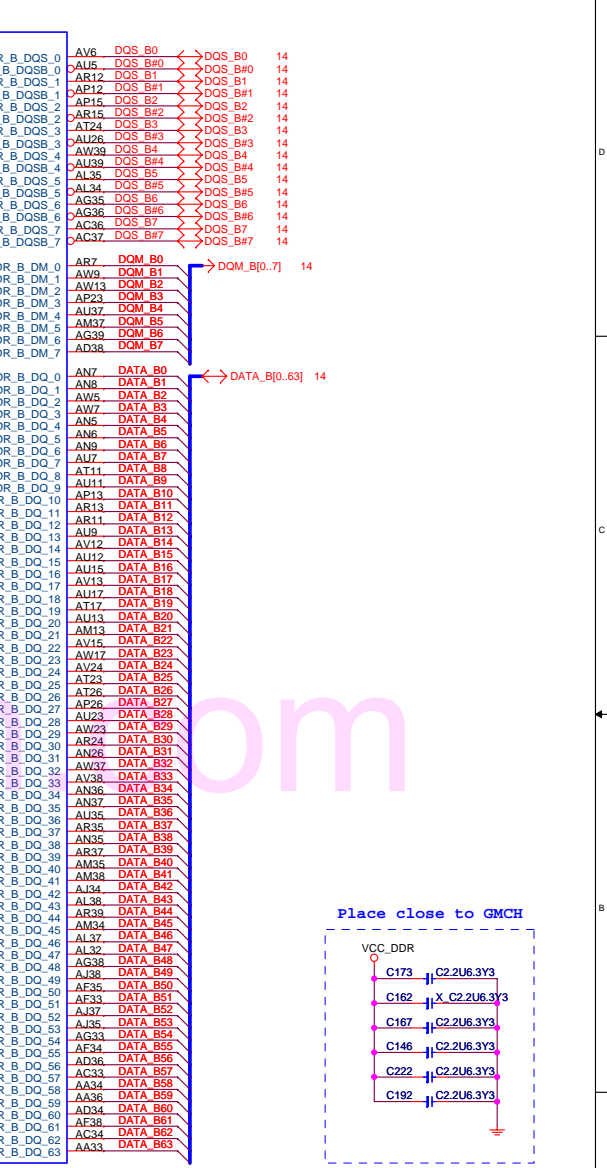
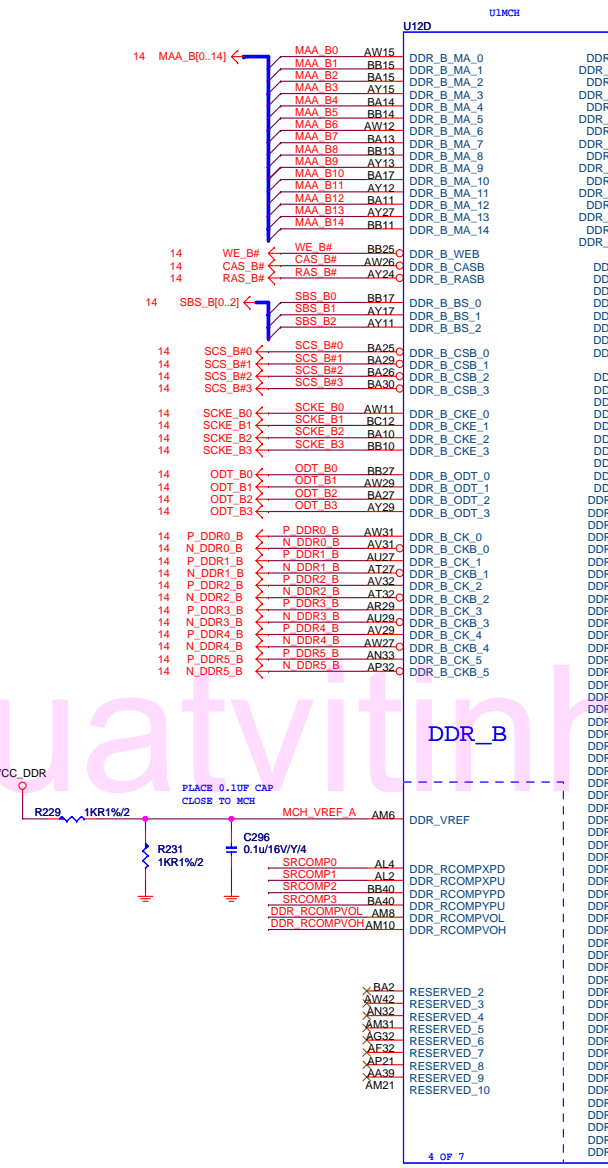
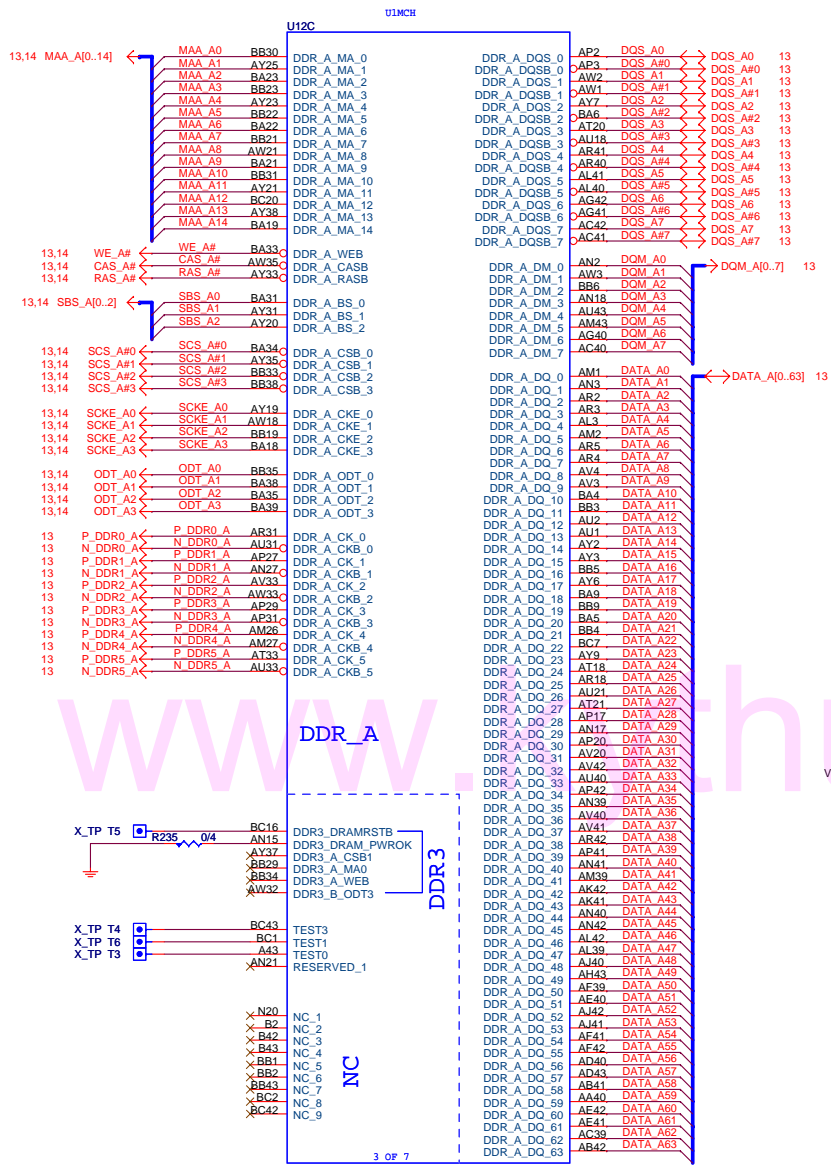
**CPU DECOUPLING CAPACITORS**

Place these caps within socket cavity



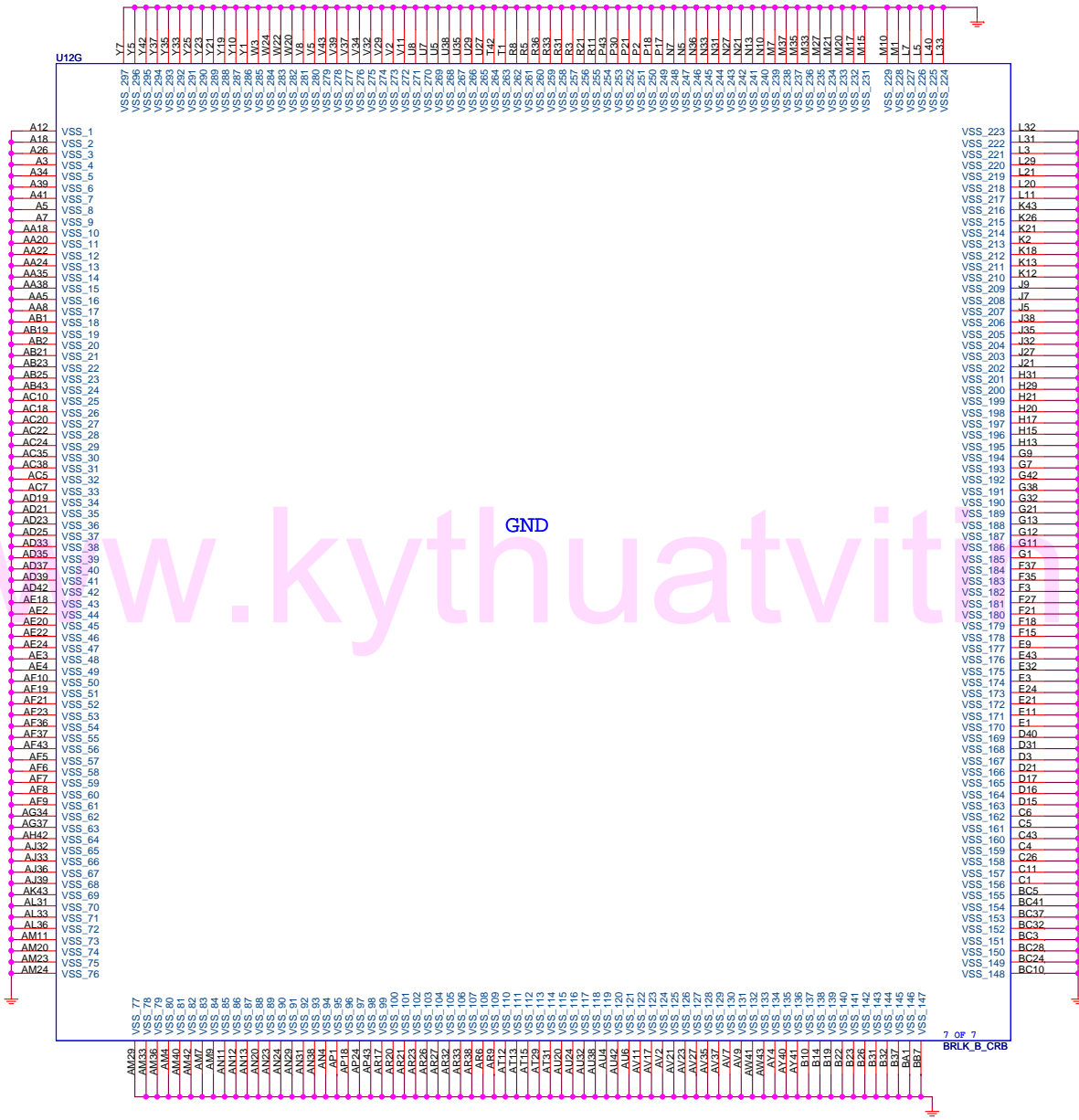
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7360</b>		
Size Custom	Document Description <b>LGA775 - GND</b>	Rev 1.0
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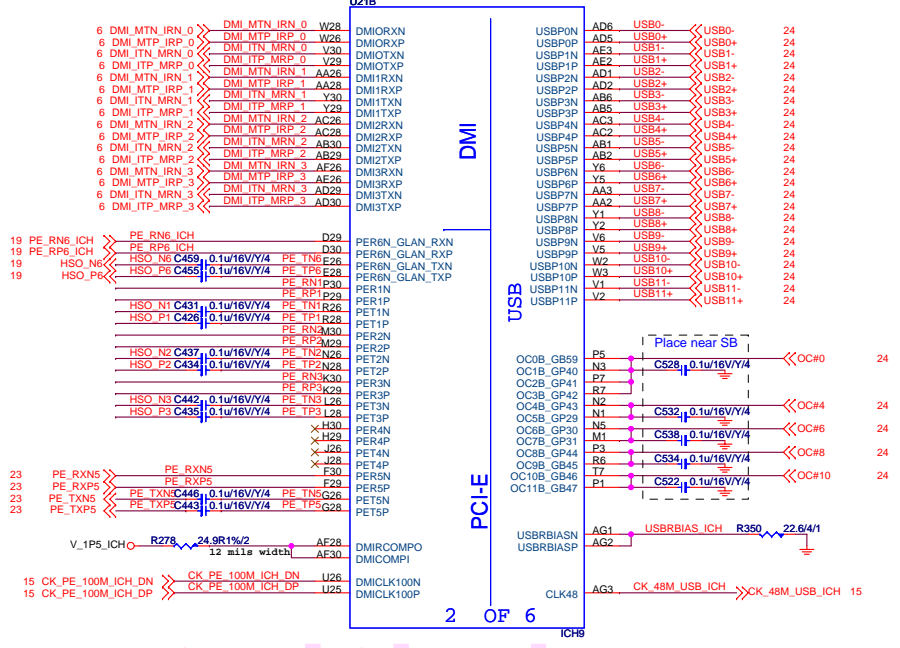
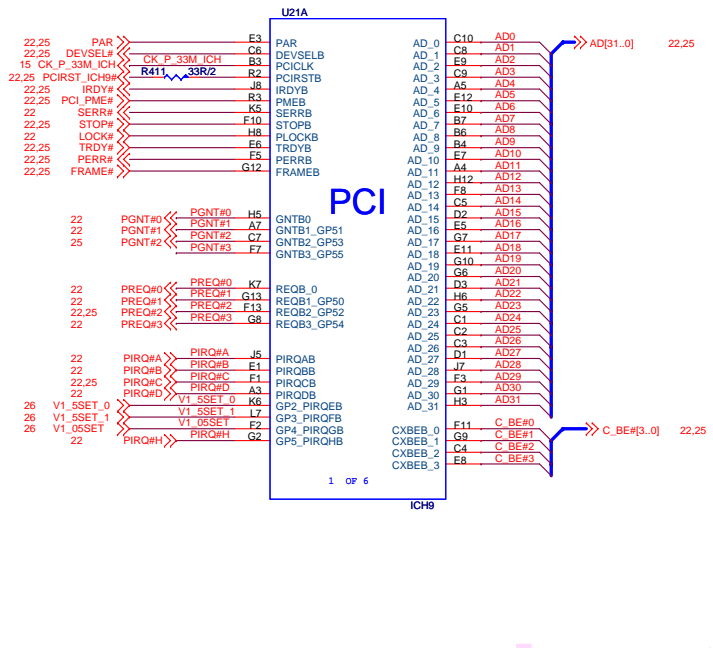




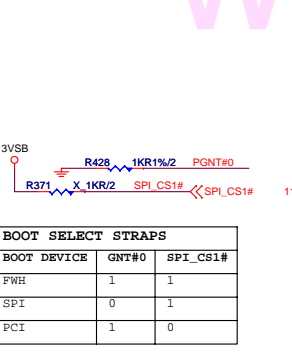




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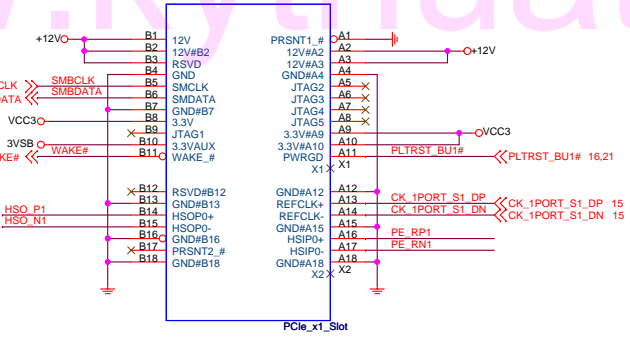


**SB STRAPPING RESISTOR**

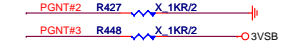
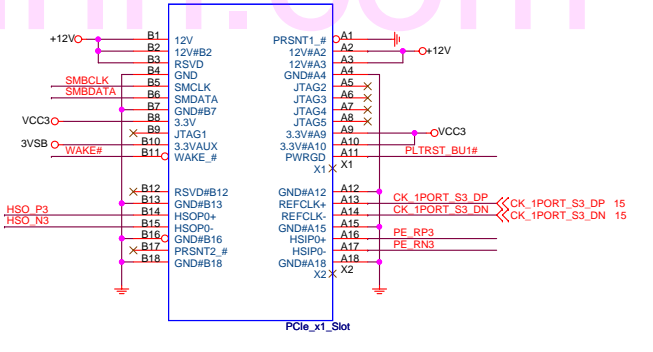


BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	1	
PCI	1	0	

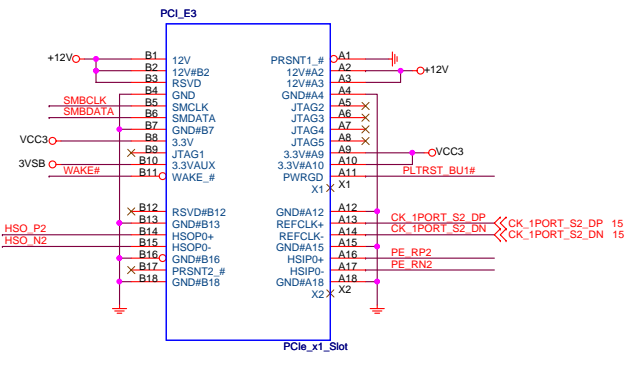
**PCIEX 1 SLOT 1,2,3**



**PCIEX 4**



SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERRIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)



**MICRO-STAR INT'L CO.,LTD**

**MSI**

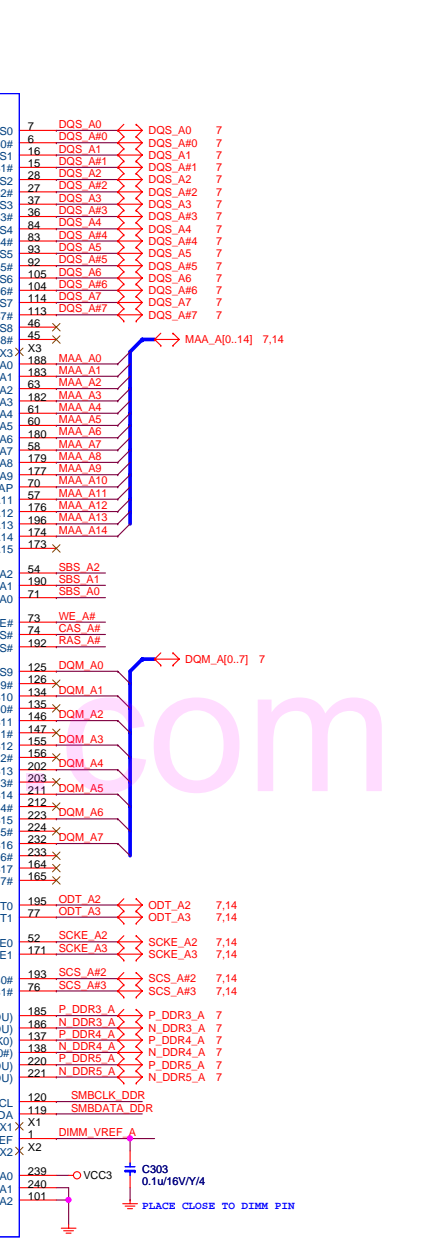
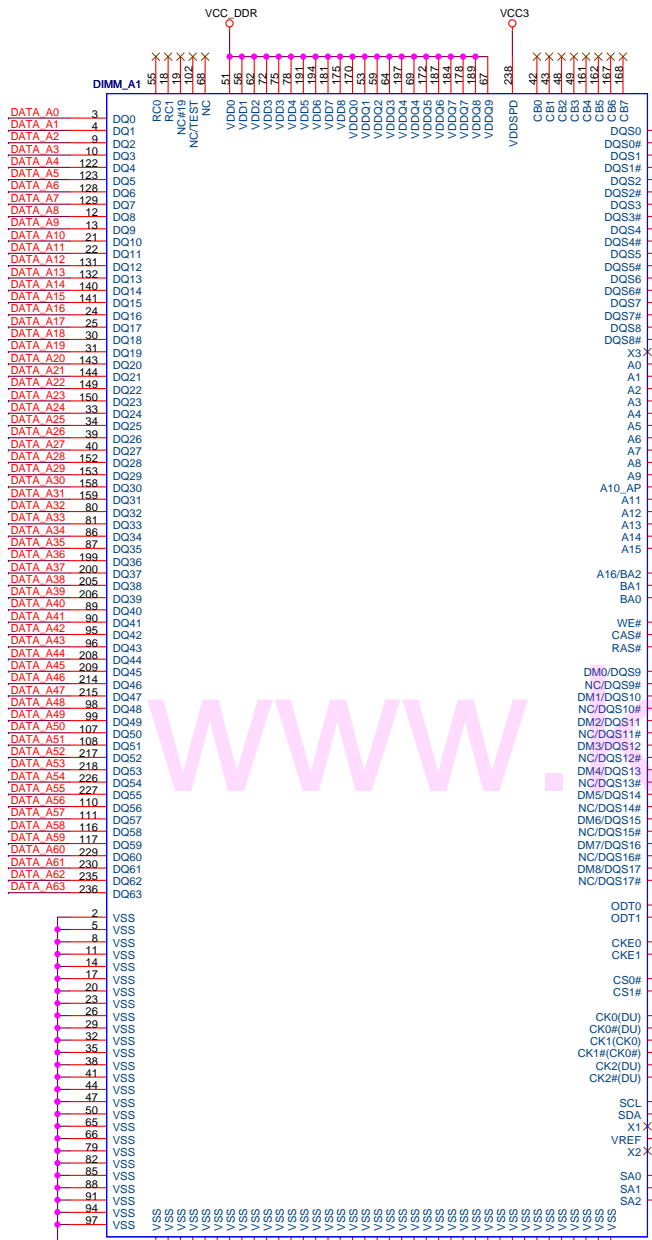
**MS-7360**

Size Custom Document Description ICH9 - PCI, DMI, USB, PCIE & Slots Rev 1.0

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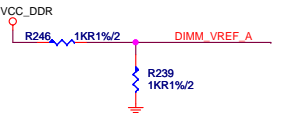


**DDRII DIMM\_A1**

**DDRII DIMM\_A2**

ADDRESS: 000  
0xA0

ADDRESS: 001  
0xA2



SMBCLK\_DDR R121 33R/2 SMBCLKA 10.11.15.21.26.28  
SMBDATA\_DDR R129 33R/2 SMBDATA 10.11.15.21.26.28



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MS-7360

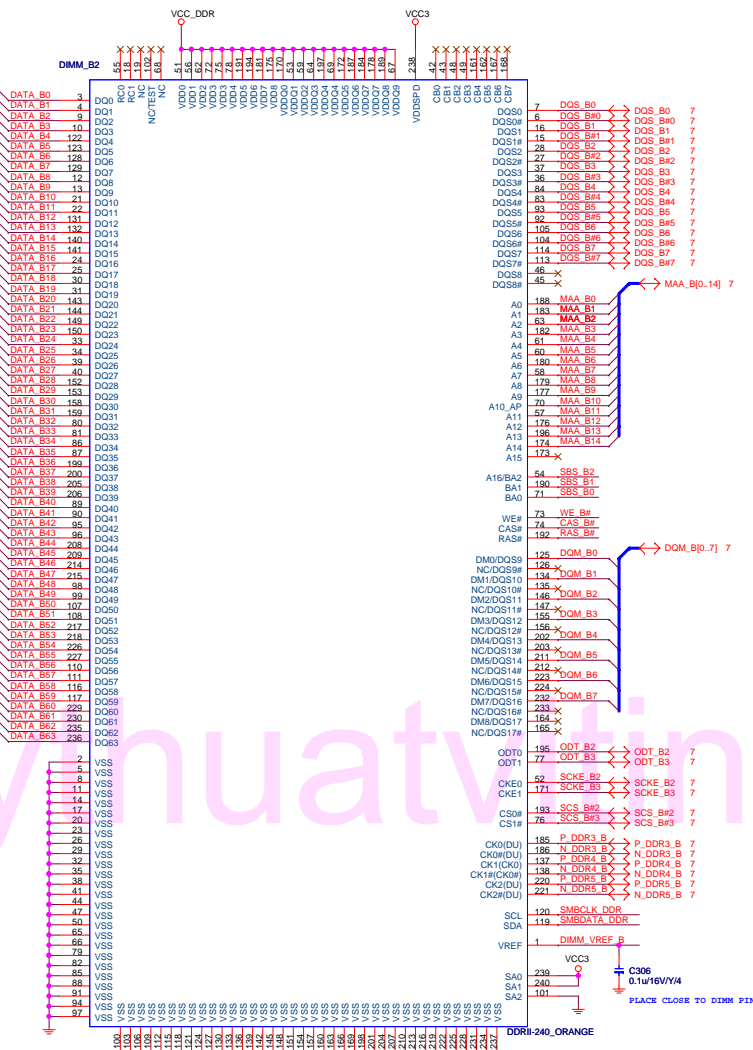
Size	Document Description	Rev
Custom	DDR2 CHANNEL-A	1.0

# DDR II Termination



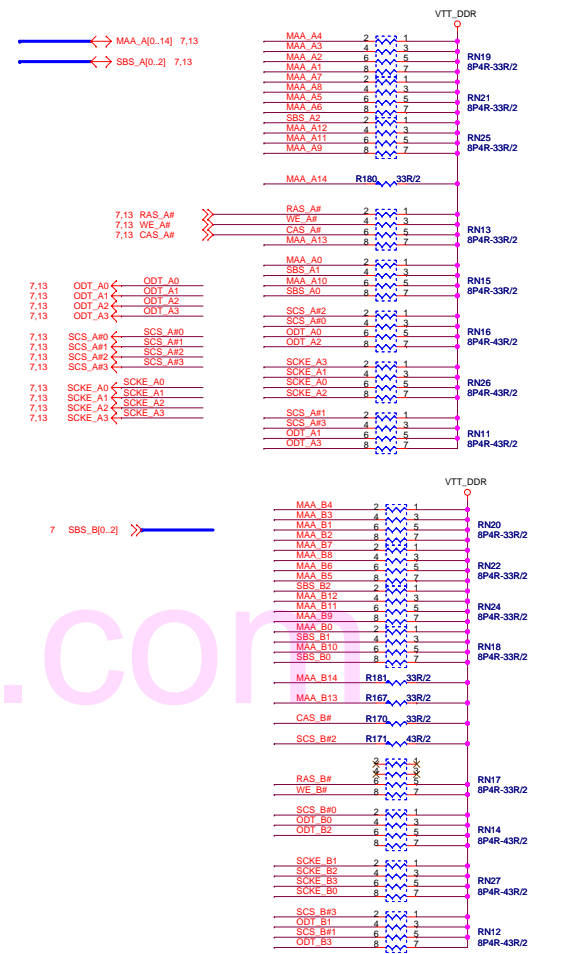
ADDRESS: 010  
0xA4

## DDR II DIMM\_B1



ADDRESS: 011  
0xA6

## DDR II DIMM\_B2



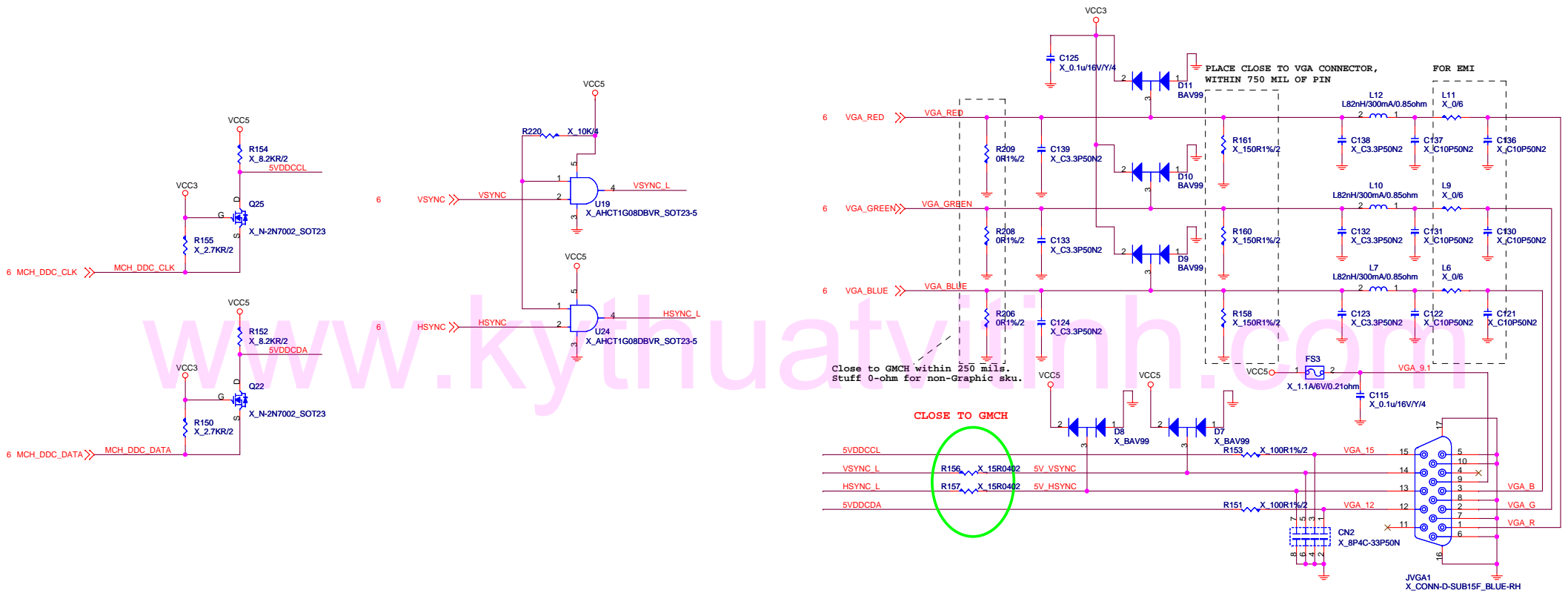
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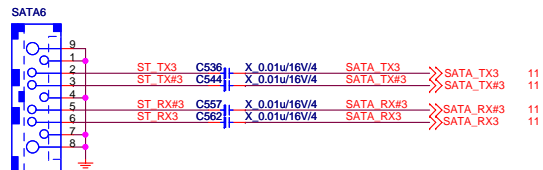




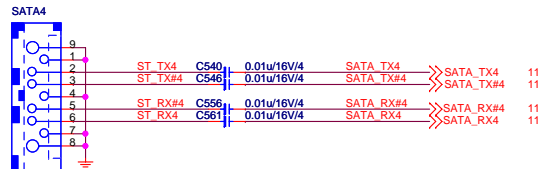


# Video Connector

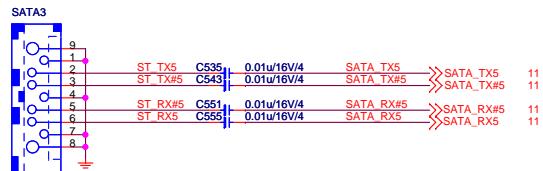




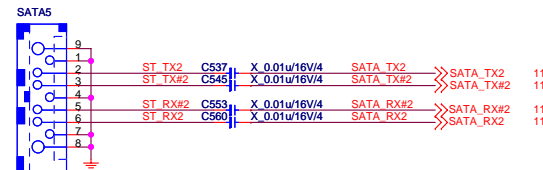
X\_CONN-SATA10P\_PURPLE



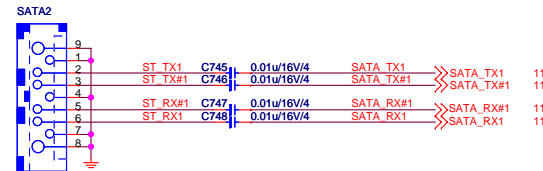
CONN-SATA10P\_PURPLE



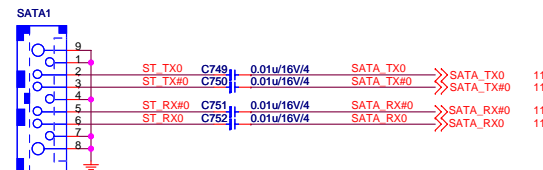
CONN-SATA10P\_PURPLE



X\_CONN-SATA10P\_PURPLE



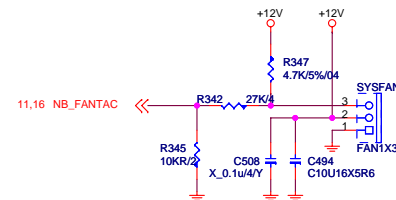
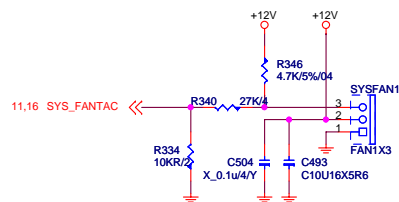
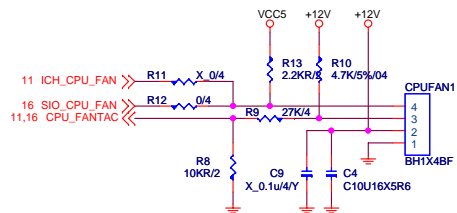
CONN-SATA10P\_PURPLE

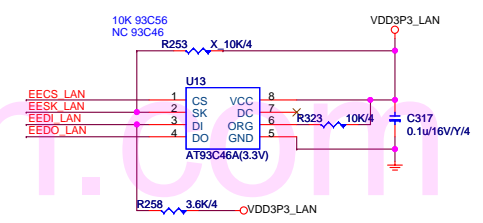
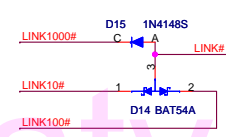
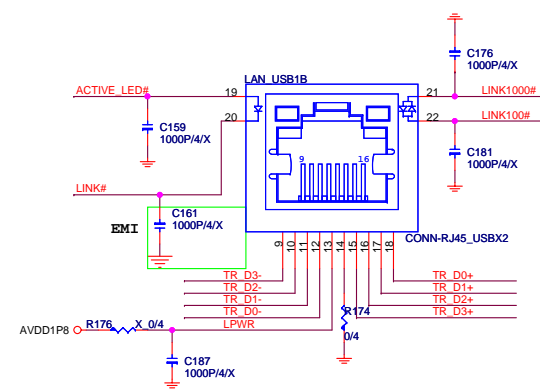
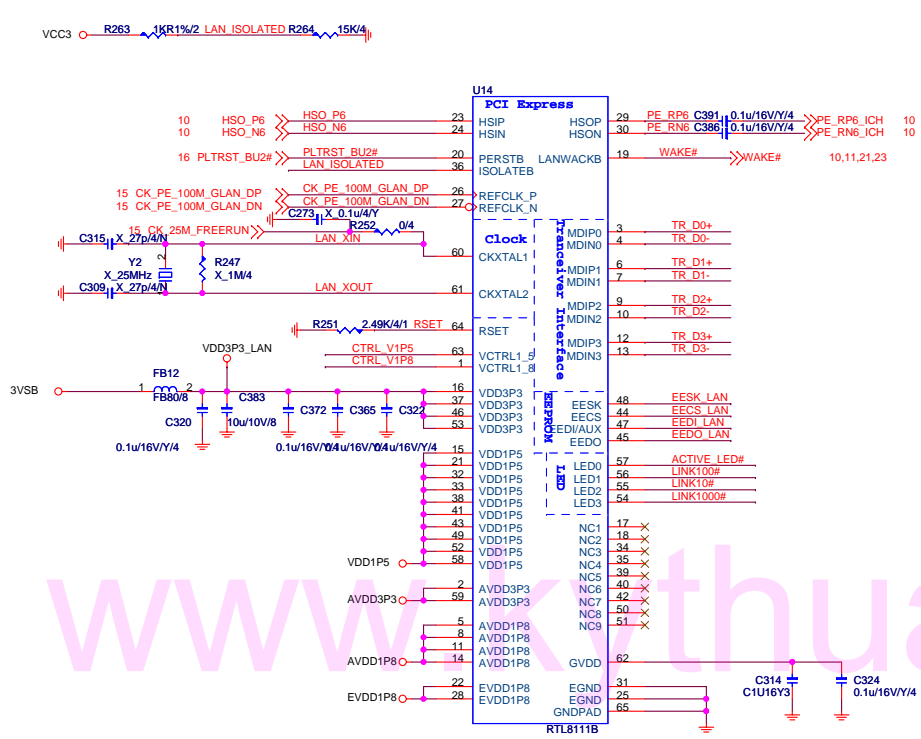


CONN-SATA10P\_PURPLE

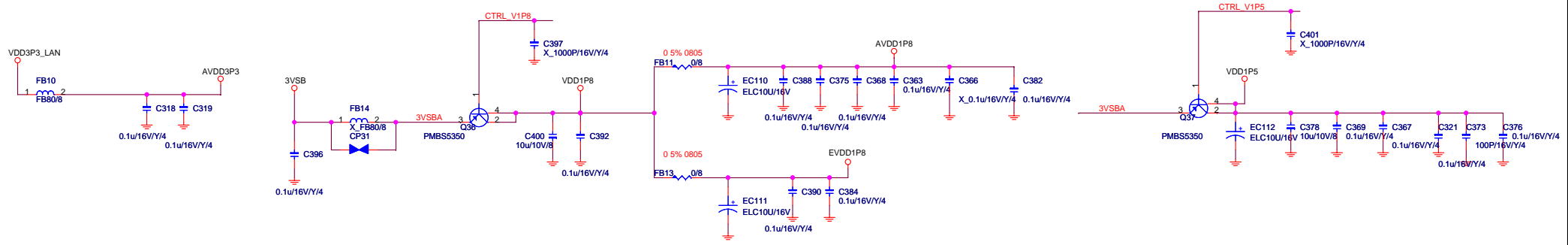
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**FAN-COUNTROL CIRCUIT**



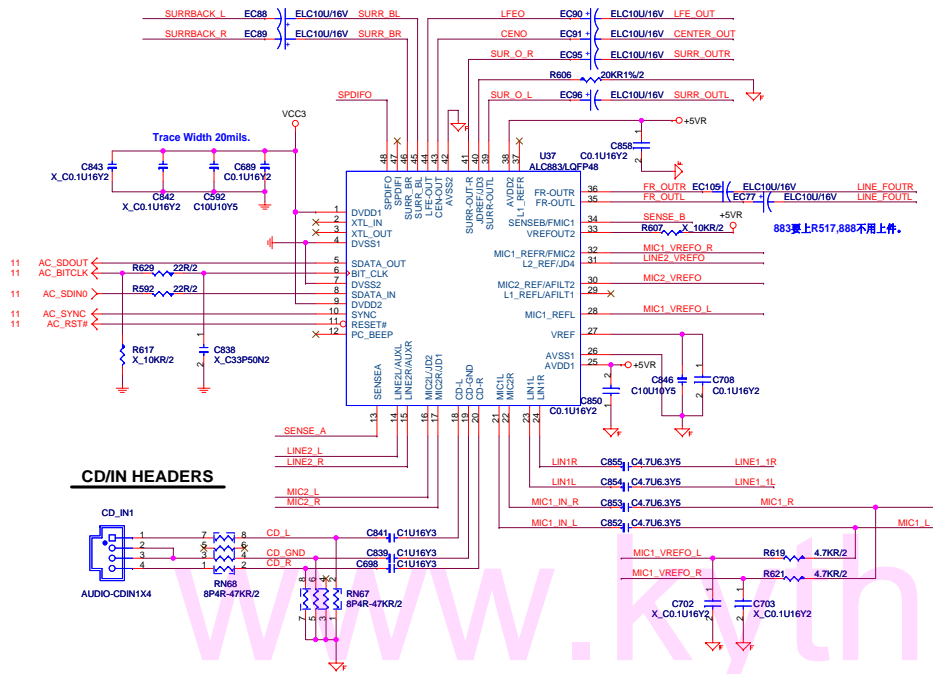


**PCIE LAN(RTL8111B) POWER**

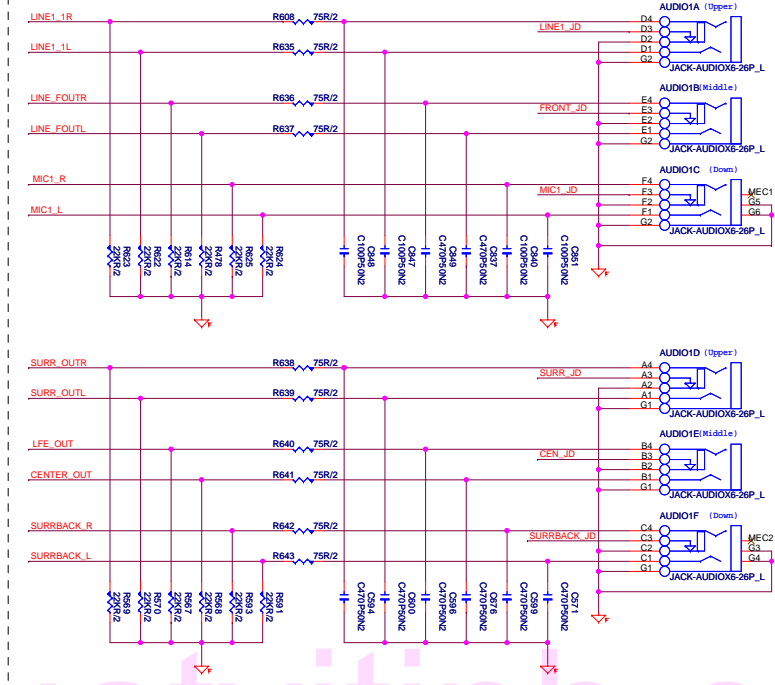


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Custom	<b>PCIE_LAN_RTL8111B</b>	1.0
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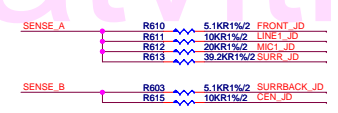
# ALC888 CODEC



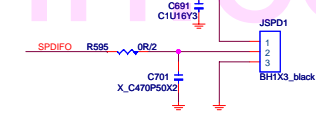
# ALC883 JACK



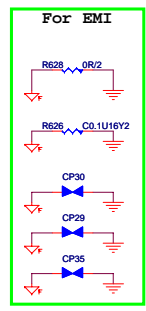
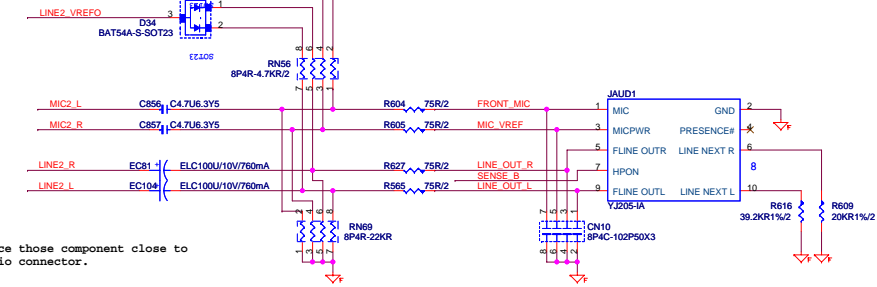
# ALC883 JACK DETECT



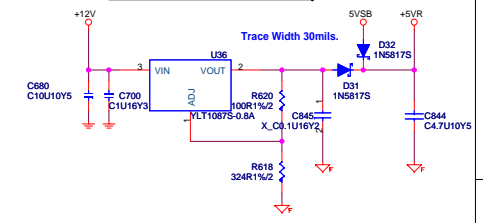
# SPDIF\_OUT



# Azalia Front Audio Connector

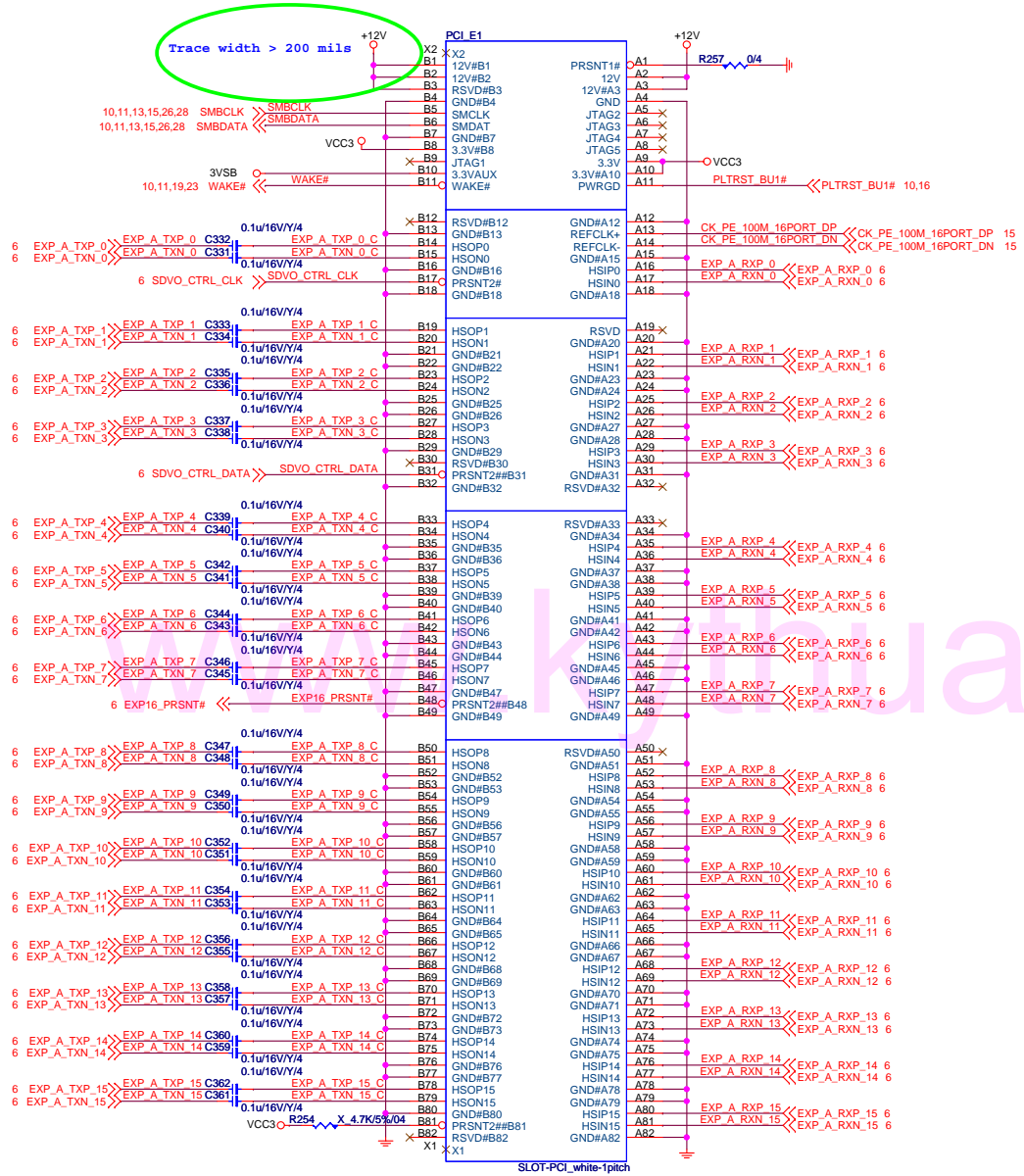



# AUDIO CODE REGULATORS



Place those component close to audio connector.

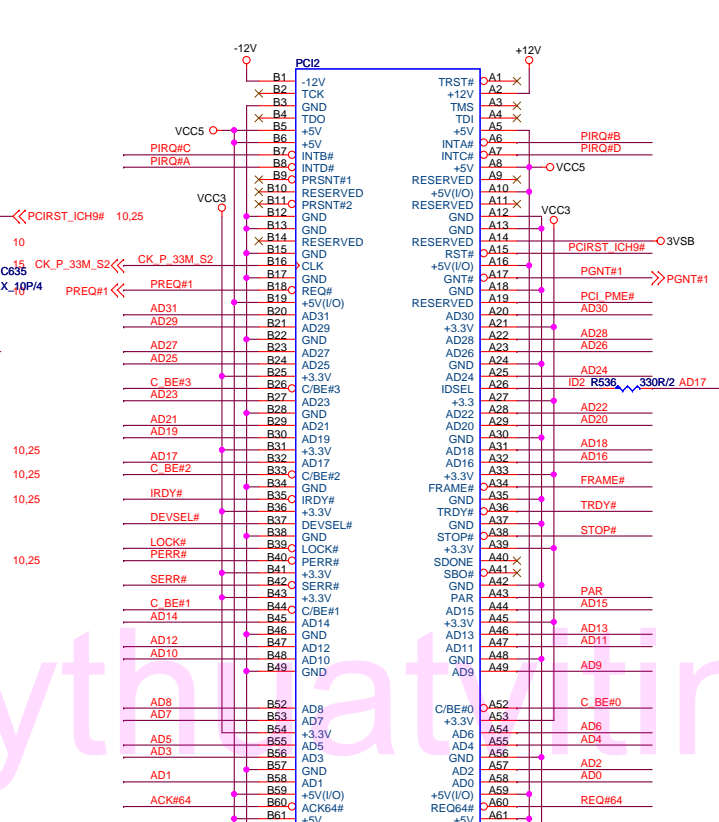
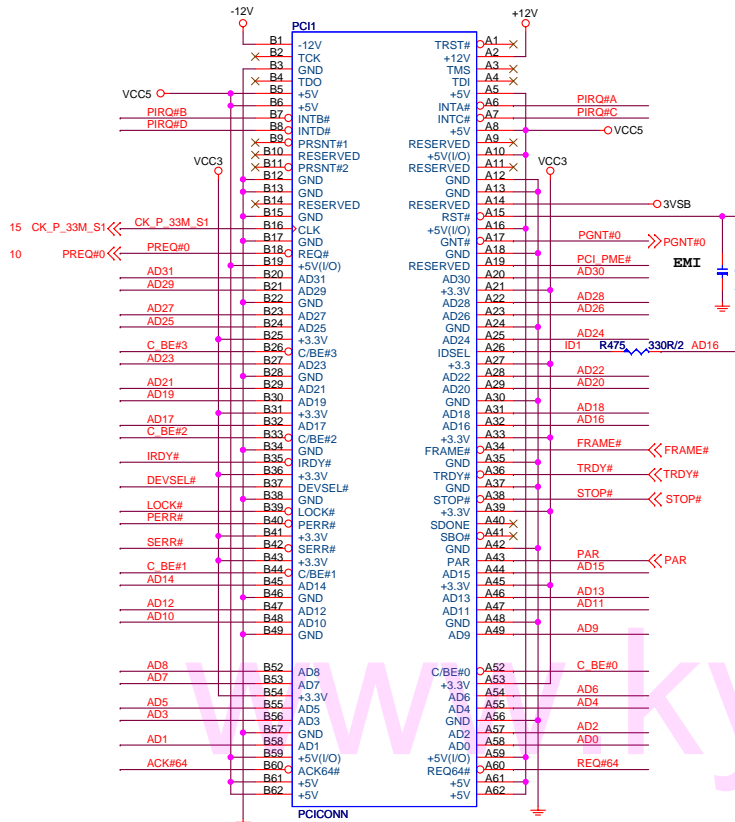
# PCI\_Express X16 Slot



			<b>MICRO-STAR INT'L CO.,LTD</b>		
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Size	Document Description				Rev
Custom	PCIe x16, x4, x1 & Bus Switch				1.0
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**PCI SLOT 1 (PCI VER: 2.2 COMPLY)**

**PCI SLOT 2 (PCI VER: 2.2 COMPLY)**



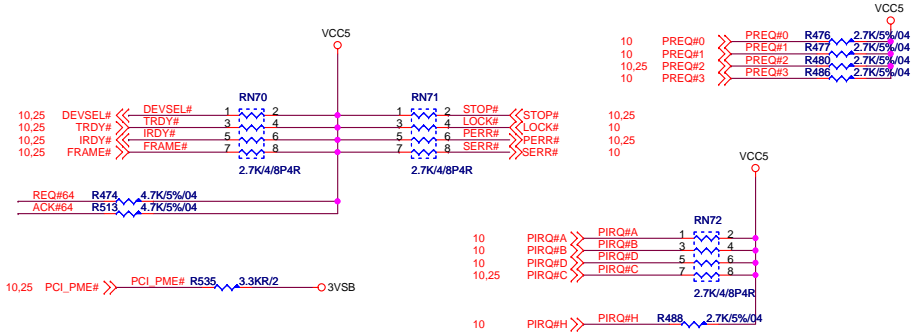
**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**

10.25 AD[31..0] <<< AD[31..0]

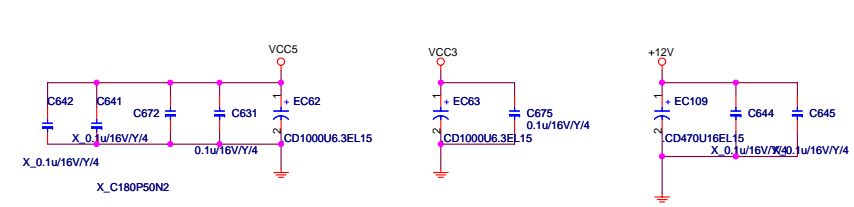
10.25 C\_BE#[3..0] <<< C\_BE#[3..0]

**IDSEL = AD17**  
**MASTER = PREQ#1**  
**PIRQ#B**

**PCI PULL-UP / DOWN RESISTORS**

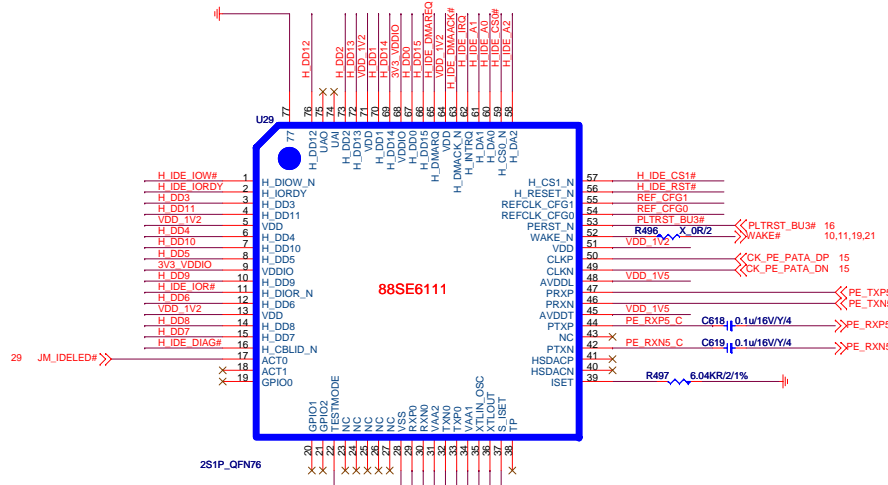


**PCI SLOT DECOUPLING CAPACITORS**

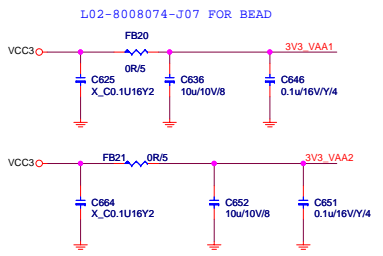
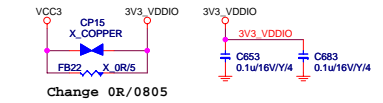


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Size Custom	Document Description <b>PCI Slot 1 &amp; 2</b>	Rev 1.0
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# Hi-Speed PCIE to SATA/PATA Bridge



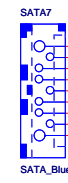
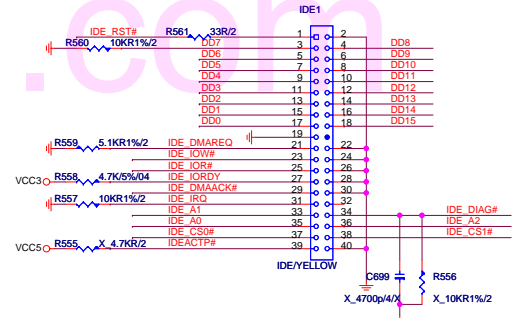
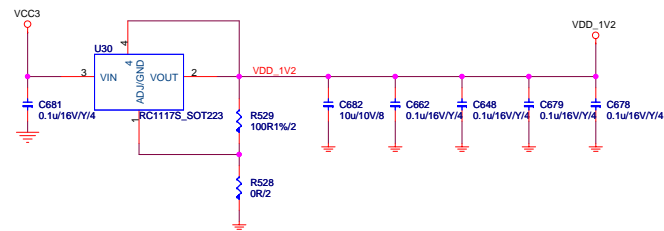
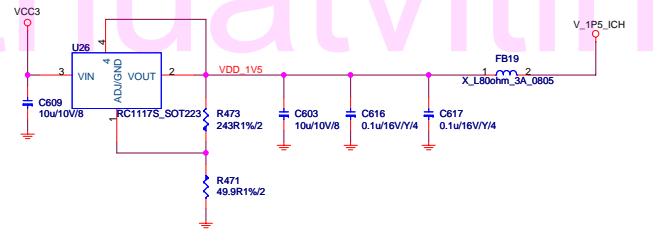
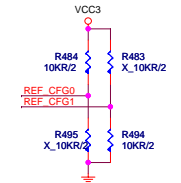
H_DD15	2	1	DD15
H_DD0	4	3	DD0
H_DD14	6	5	DD14
H_DD1	8	7	DD1
H_DD11	2	1	DD11
H_DD4	4	3	DD4
H_DD10	6	5	DD10
H_DD5	8	7	DD5
H_DD9	2	1	DD9
H_DD6	4	3	DD6
H_DD8	6	5	DD8
H_DD7	8	7	DD7
H_DD13	2	1	DD13
H_DD2	4	3	DD2
H_DD12	6	5	DD12
H_DD3	8	7	DD3



H_IDE_IOW#	R543	22R/2	IDE_IOW#
H_IDE_IOR#	R542	22R/2	IDE_IOR#
H_IDE_A2	R502	22R/2	IDE_A2
H_IDE_A1	R503	22R/2	IDE_A1
H_IDE_A0	R509	22R/2	IDE_A0
H_IDE_DMAACK#	R511	22R/2	IDE_DMAACK#
H_IDE_CS#	R493	22R/2	IDE_CS#
H_IDE_RST#	R488	22R/2	IDE_RST#
H_IDE_DMAREQ	R522	82.5R/2/1%	IDE_DMAREQ
H_IDE_IORDY	R547	82.5R/2/1%	IDE_IORDY
H_IDE_IRQ	R506	22R/2	IDE_IRQ
H_IDE_DIAG#	R537	82.5R/2/1%	IDE_DIAG#

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REF\_CFG[1:0] =  
00: 20MHz  
01: 25MHz



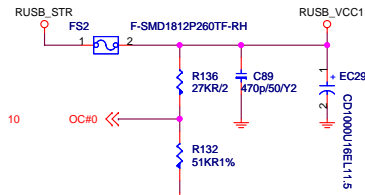
1	ST_TX7	C638	0.01u25V/4X	SATA_TX7
2	ST_TX#7	C649	0.01u25V/4X	SATA_TX#7
3				
4	ST_RX#7	C655	0.01u25V/4X	SATA_RX#7
5	ST_RX7	C663	0.01u25V/4X	SATA_RX7
6				
7				
8				

		<b>MICRO-STAR INT'L CO.,LTD</b>			
		<b>MS-7360</b>			
Size	Custom	Document Description	Marvell 88SE6111 PCIE to PATA/SATA	Rev	1.0
Date:		Thursday, March 08, 2007		Sheet	23 of 34

# Rear USB Connector

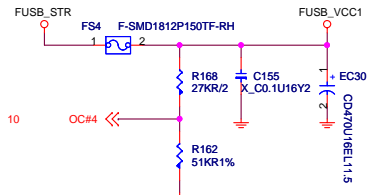
## USB POWER FOR PORT 0,1

NEAR CONNECTOR

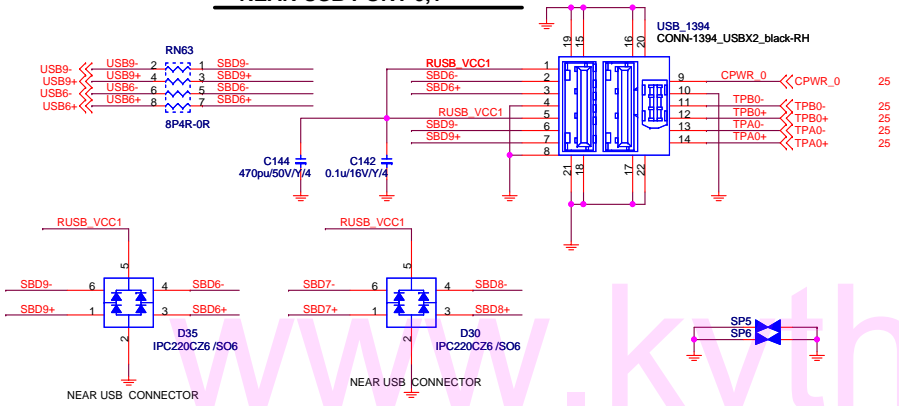


## USB POWER FOR PORT 6,7,8,9

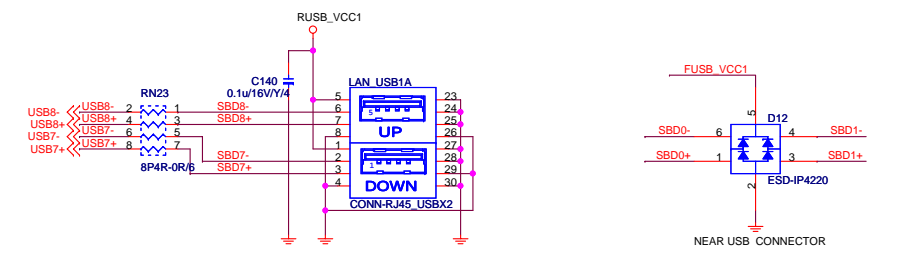
NEAR CONNECTOR



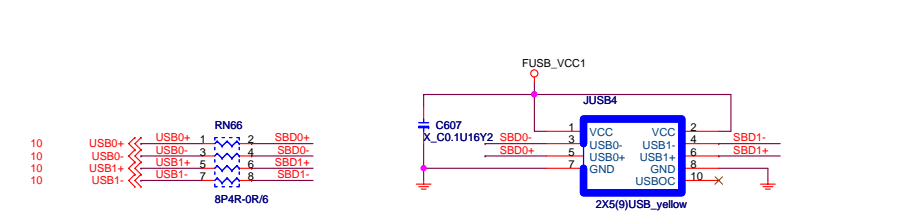
## REAR USB PORT 0,1



## REAR USB PORT 2,3 (With LAN)



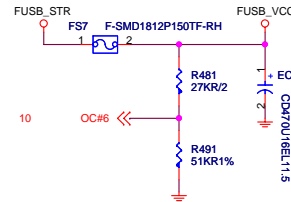
## FRONT USB PORT 0,1



# Front USB Connector

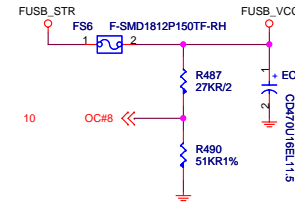
## USB POWER FOR PORT 6,7

NEAR CONNECTOR



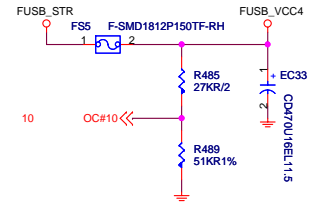
## USB POWER FOR PORT 6,7

NEAR CONNECTOR

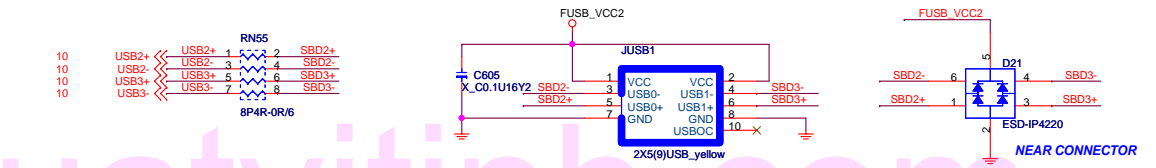


## USB POWER FOR PORT 6,7

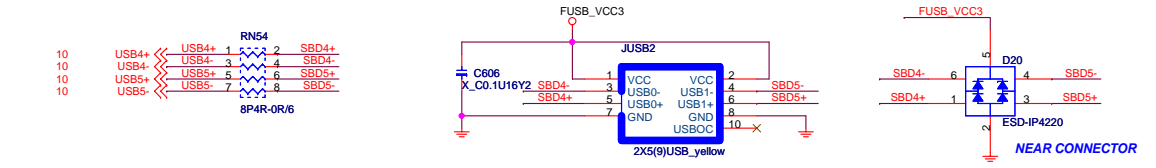
NEAR CONNECTOR



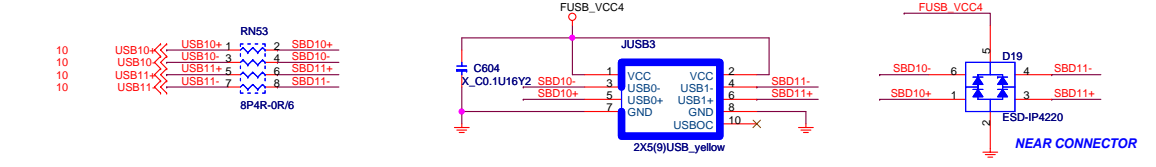
## FRONT USB PORT 2,3




## FRONT USB PORT 4,5



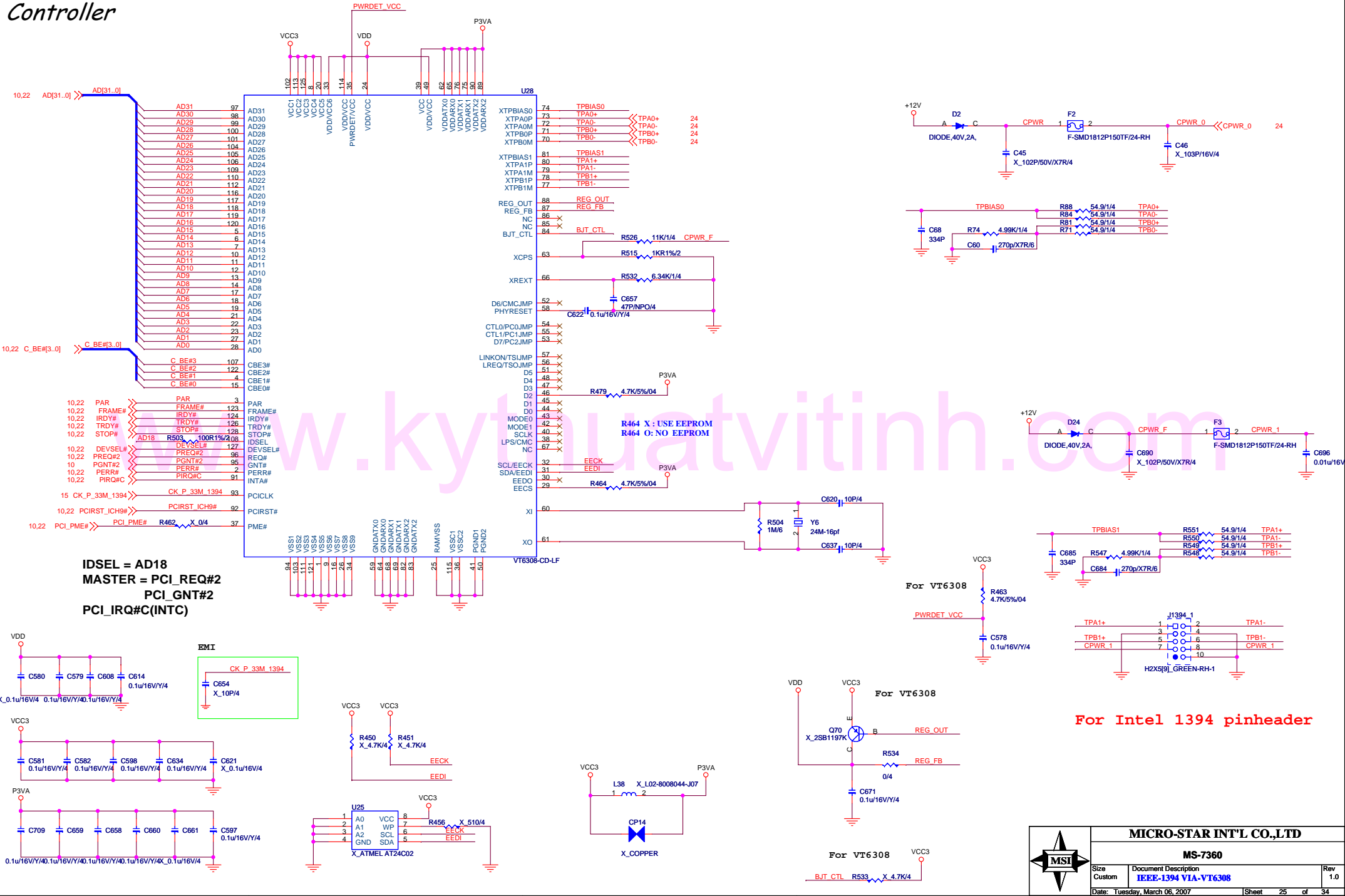
## FRONT USB PORT 10,11



			<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7360</b>			<b>MS-7360</b>		
Size	Document Description	Rev			
Custom	<b>USB Connector</b>	1.0			
Date:	Monday, March 05, 2007	Sheet	24	of	34

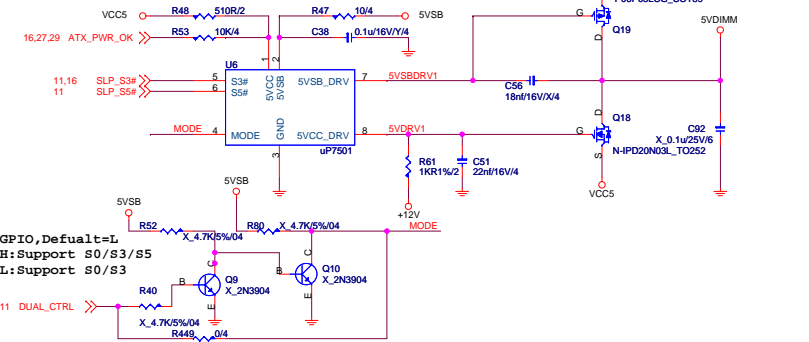


# 1394a OHCI Link Layer Controller



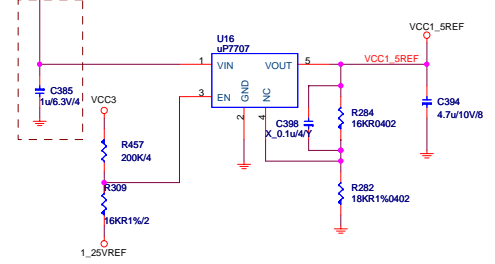
<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7360</b>		
Size Custom	Document Description <b>IEEE-1394 VIA-VT6308</b>	Rev 1.0
Date: Tuesday, March 06, 2007	Sheet 25 of 34	

**5VDIMM FOR DDR**

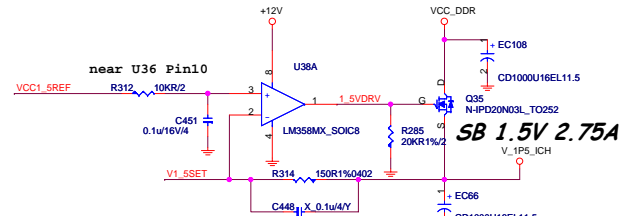
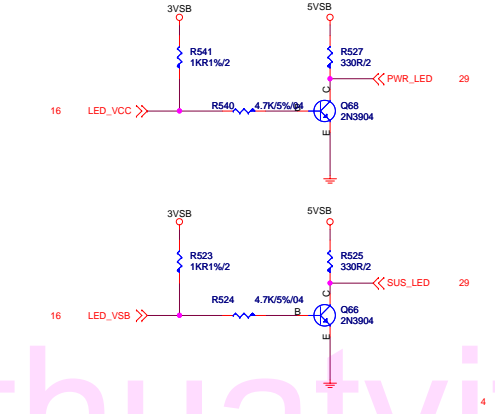


GPIO, Default=L  
H: Support S0/S3/S5  
L: Support S0/S3

**VCC1\_5REF**



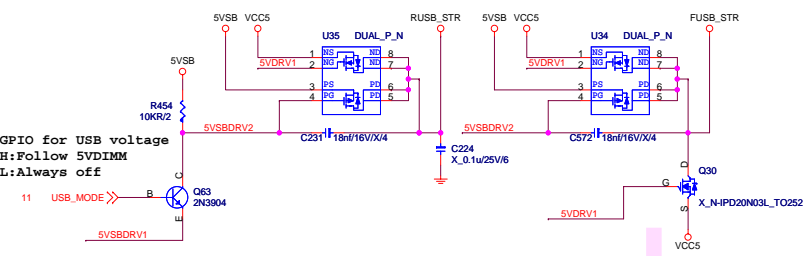
**LED ( for Fintek 71882)**



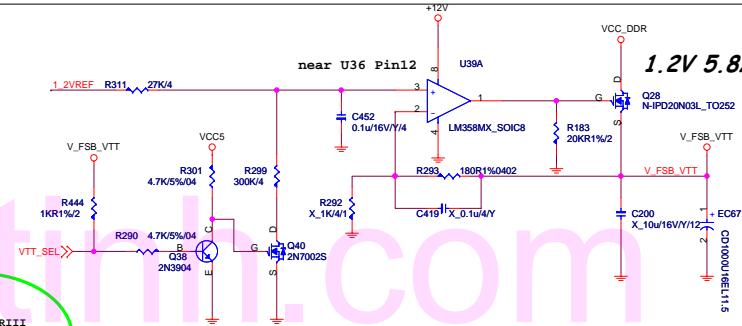
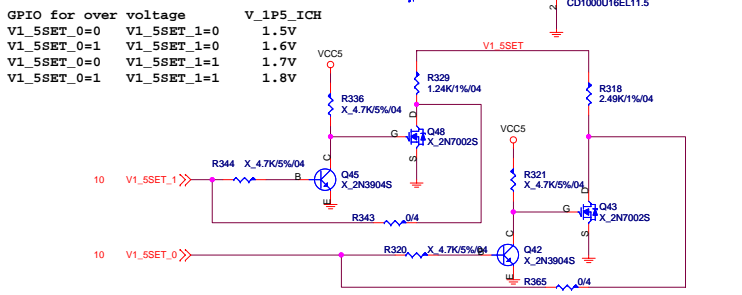
GPIO for over voltage  
V1\_5SET\_0=0 V1\_5SET\_1=0 1.5V  
V1\_5SET\_0=1 V1\_5SET\_1=0 1.6V  
V1\_5SET\_0=0 V1\_5SET\_1=1 1.7V  
V1\_5SET\_0=1 V1\_5SET\_1=1 1.8V

**5VSB FOR Rear USB**

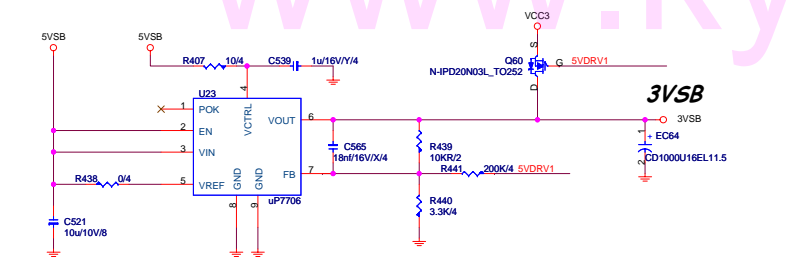
**5VSB FOR Front USB**



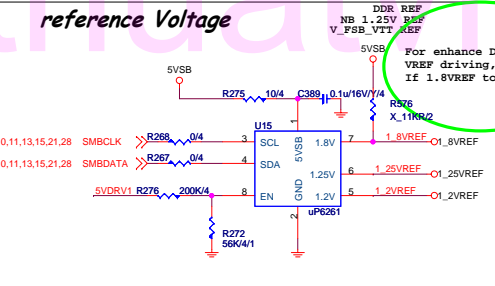
GPIO for USB voltage  
H: Follow 5VDIMM  
L: Always off



**1.2V 5.8A**



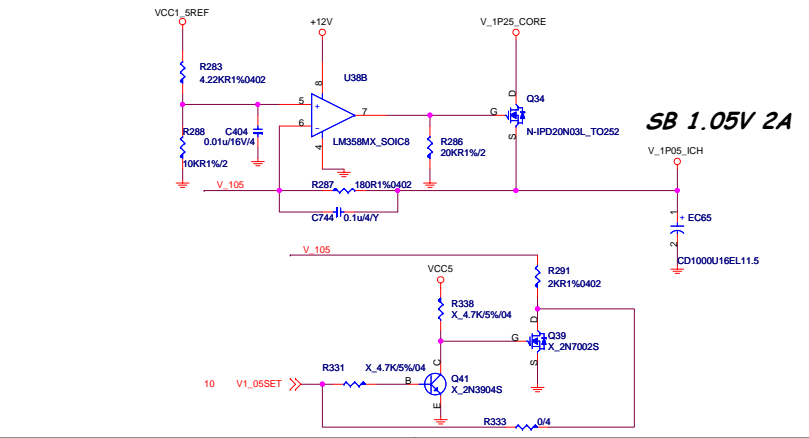
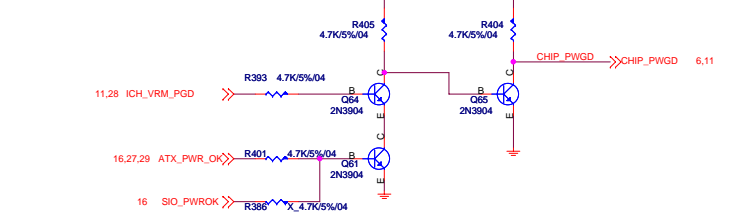
**3VSB**



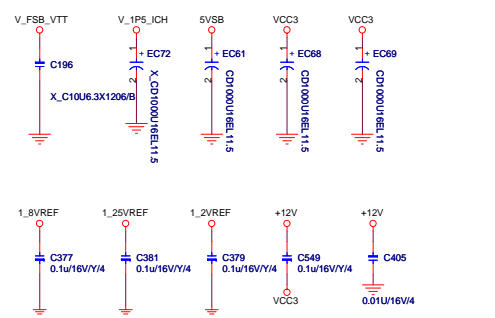
**reference Voltage**

For enhance DDRIII VREF driving, If 1.8VREF to 1.5VREF

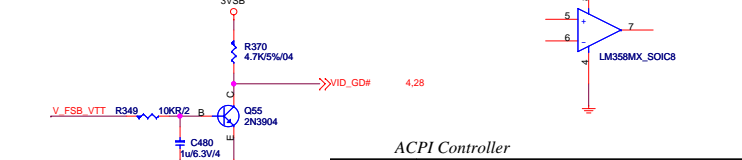
**PWROK DELAY 100ms**



**SB 1.05V 2A**



**VID before PWROK >3ms**



ACPI Controller

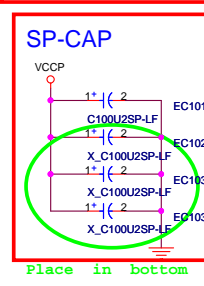
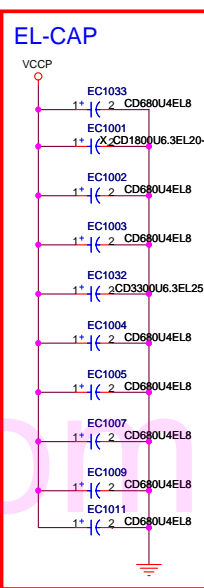
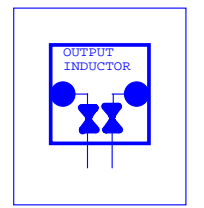
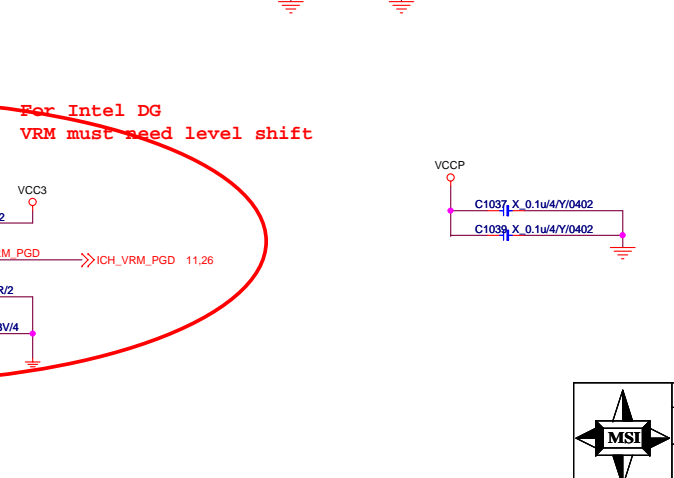
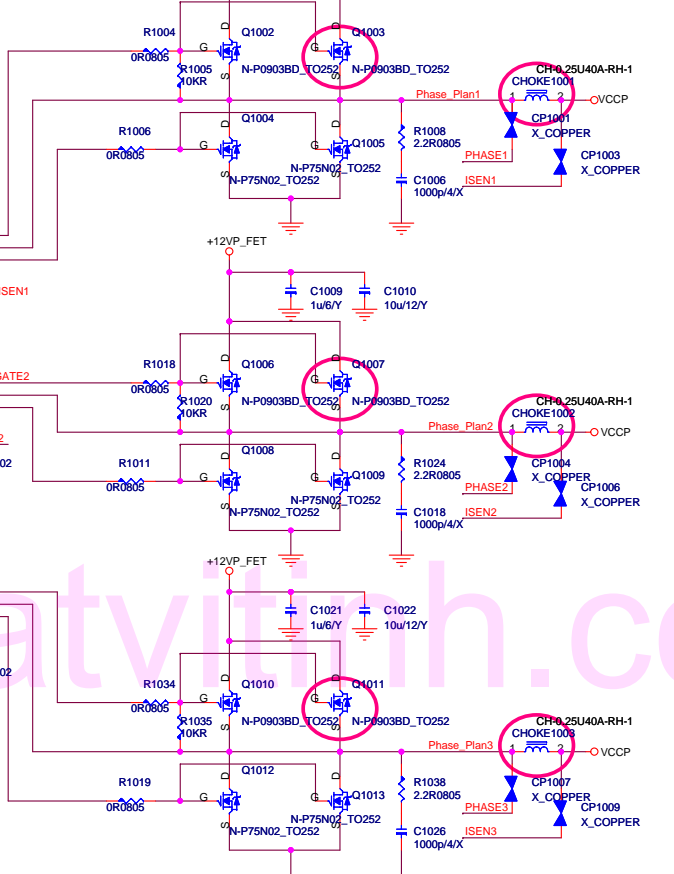
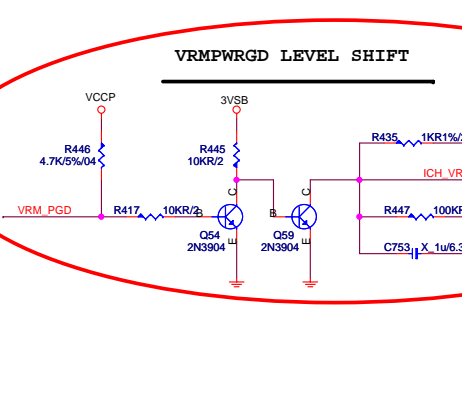
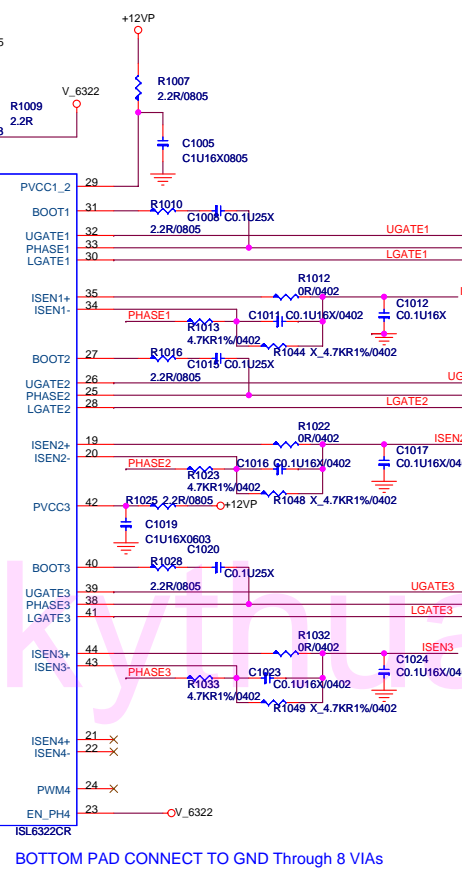
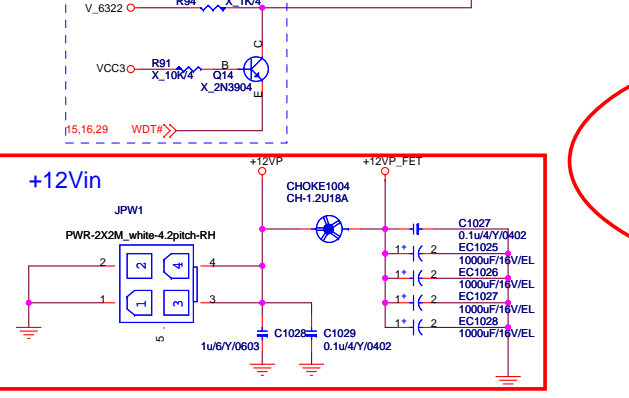
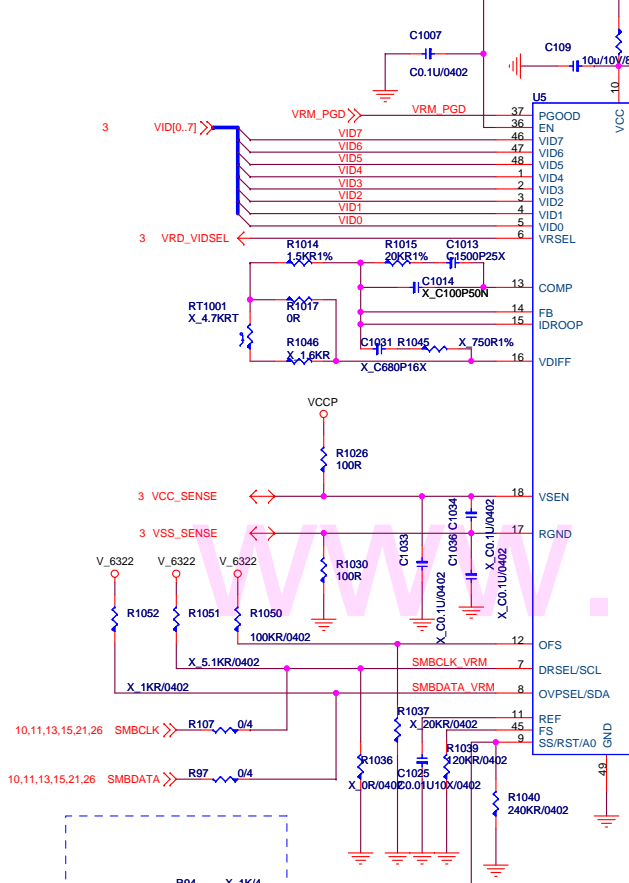
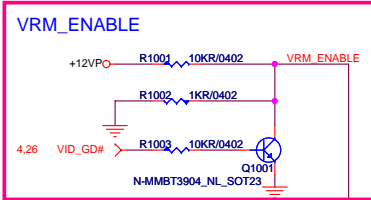
**MICRO-STAR INT'L CO.,LTD**

**MS-7360**

Size	Document Description	Rev
Custom	ACPI controller UPI	1.0

Date: Monday, March 05, 2007 Sheet 26 of 34

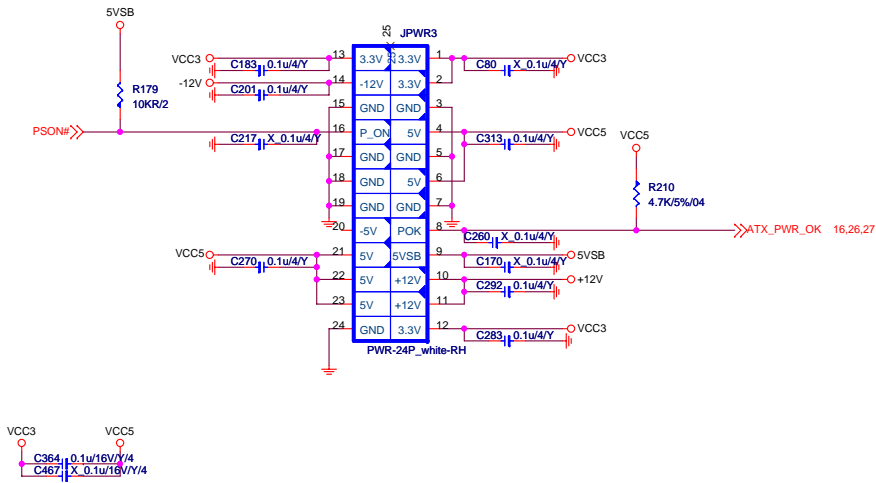




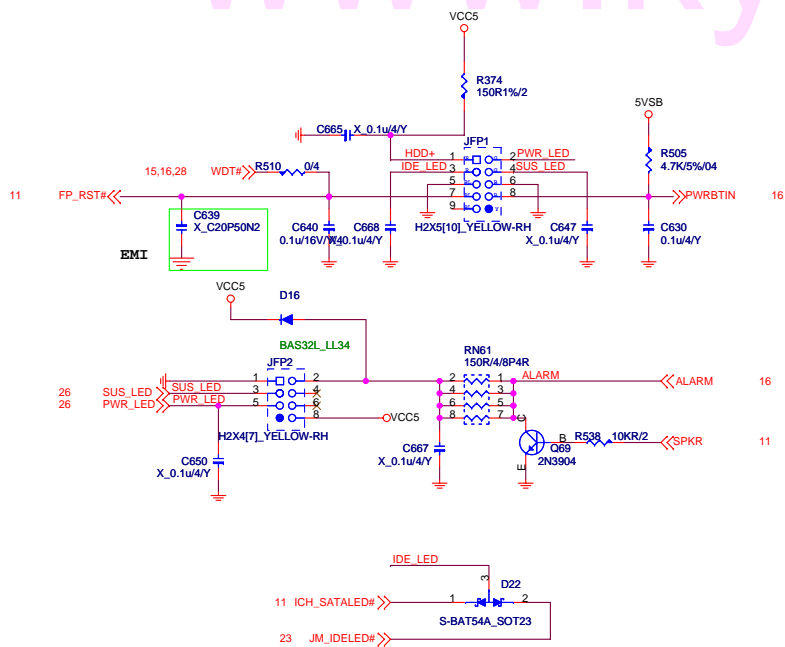
For Intel DG VRM must need level shift

Place in bottom

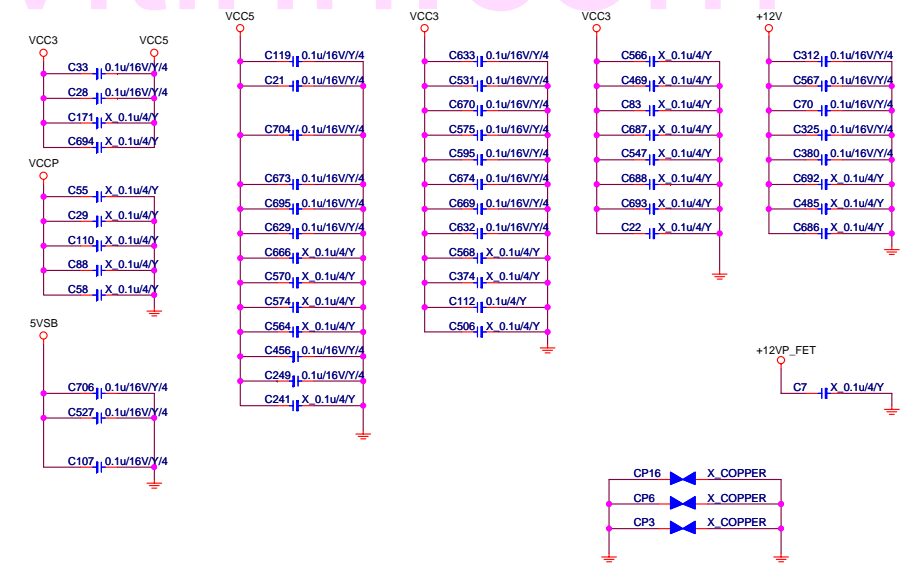
# ATX POWER CONNECTOR




# FRONT PANNEL



# Cap. for EMI & Power



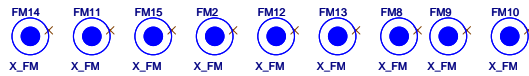


**MICRO-STAR INT'L CO.,LTD**

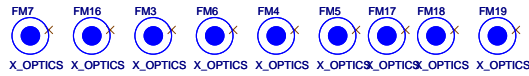
**MS-7360**

Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel	1.0
Date: Monday, March 05, 2007		Sheet 29 of 34

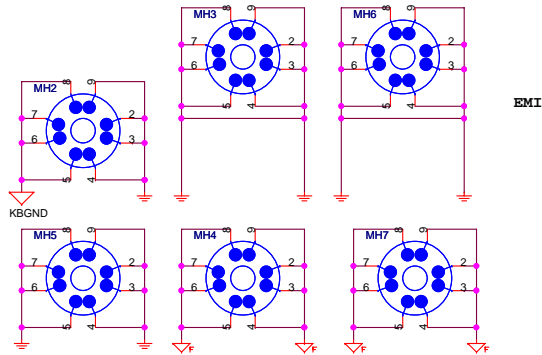
**Optical Fiducial Marks-120**



**Optical Fiducial Marks-100**

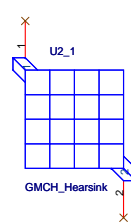


**Mounting Holes**



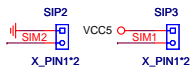
7360

P80-073600A-D05, 緋( )緋 嘲),23, 盤 稷幅紅  
 P80-0736050A-Y34, じ環,23, 盤 稷幅紅



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**Simulation**



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7360</b>		
Size Custom	Document Description <b>Manual Parts &amp; Option Parts</b>	Rev 1.0
Date: Tuesday, March 06, 2007	Sheet 30 of 34	

LGA775-CPU	
0.8375V - 1.6000V Core	- 125A
1.2V FSB Vtt	- 4.6A

Bearlake-G (G33)	
1.2V FSB_VTT	- 1.2 A
1.25V Core	- 13.8A
1.25V DMI/PCI Exp.	- 2.47 A
1.5V VCC_DDR	- 3.3A
1.5V VCC_SMCLK	- 350mA
3.3V VCCA_DAC	- 66 mA
3.3V VCC33	- 15.8mA
1.25V Vcc CL	- 4.9A

ICH9	
1.05V Core	- 1.16A
1.25V DMI	- 41 mA
1.2V FSB_VTT	- 2 mA
1.5V_A USB/SATA/PLL	- 1.65A
1.5V_B PCI Exp.	- 0.65A
VCCRTC	- 6 uA
3.3V CL	- 19 mA
1.5V GbE LAN	- 87 mA
3.3V VccSus3_3	- 200mA
3.3V Vcc3_3	- 308mA
3.3V 10/100 LAN	- 19 mA
3.3V GbE LAN	- 1 mA
3.3V HDA	- 32 mA
3.3V SusHDA	- 33 mA

1394 Controller VT6308	
3.3V	- 156mA

HD Audio STAC9227	
3.3V AUDIO	- 32mA
5V AUDIO	- 200mA

CK505	
3.3V VDD_48/PCI/REF	- 250mA
0.3V - 1V CPU/SRC/DOT/PLL	- 80mA

RTL8111B	
3.3V_SB I/O & LED	- 668mA
1.8V EVDD/AVDD	- 198mA
1.5V VDD	- 367mA

ISL6306	
VCCP VRD11/10.x	0.8375V-1.6000V
4-Phase Switch	

W83310DS	
VTT_DDR	0.75V Linear 0.83A

uP6103 SW-Power	
VCC_DDR	1.5V PWM 18.64A

uP6103 SW-Power	
V_1P25_CORE	1.25V PWM 21.21A

MS12 Controller	
V_1P05_ICH	1.05V Linear 1.16A
V_FSB_VTT	1.2V Linear 5.8A
V_1P5_ICH (TO263)	1.5V Linear 2.31A
VCC3_SB	3.3V Linear 2.5A
5VDUAL1	5V Switch 6.35A
5VDIMM	5V Switch 6.99A

DDRIII x4 & TERMINATOR	
0.9V VTT_DDR	- 0.83A
1.5V VCC_DDR (S0,S1)	- 7.2A

PCI Express x16 slot	
+12V	- 5.5 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A

PCI Express x 1 slot	
+12V	- 0.5 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A

PCI Express x 4 slot	
+12V	- 5.5A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A

PCI slot x2	
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 7.6A
+5V	- 5.0A
+12V	- 0.5A

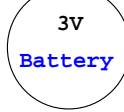
USB x12	
+5V (S0,S1)	- 6.0A
+5V (S3)	- 20mA

PS2	
+5V (S0,S1)	- 345mA
+5V (S3)	- 2.0mA

5VAudio	+5VR	500mA
---------	------	-------

+12V
ATX 2x2

+5V	+3.3V	+5VSB	+12V
ATX POWER			

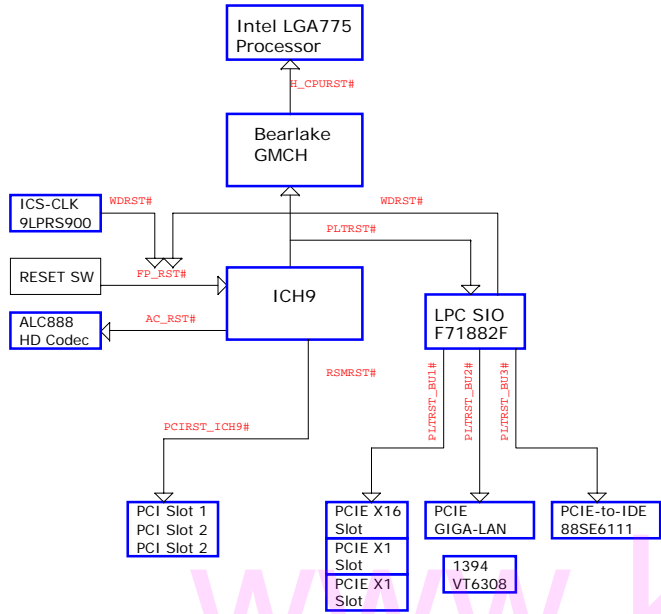


■ Bead or Inductor  
 X-Copper

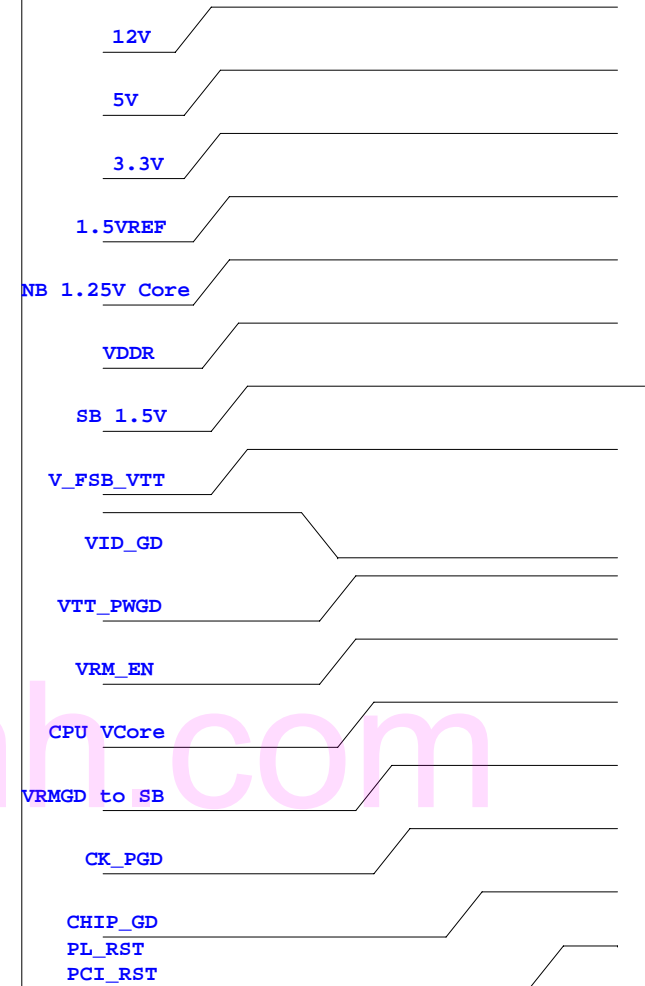
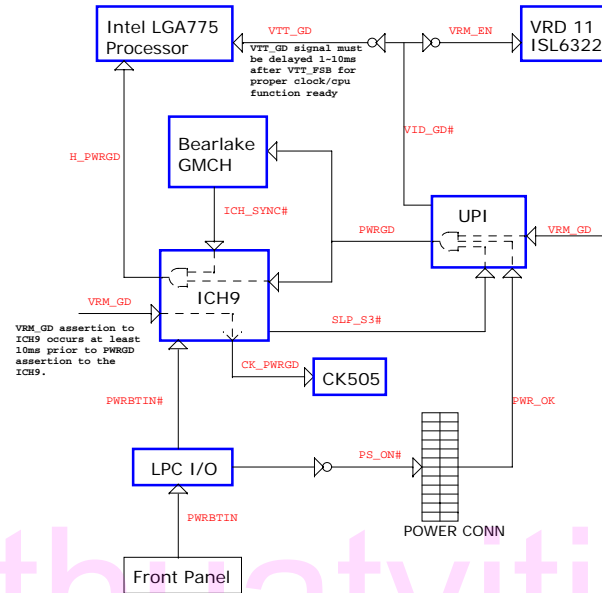


MICRO-STAR INT'L CO.,LTD		
MS-7360		
Size Custom	Document Description Power Delivery	Rev 1.0
Date: Monday, March 05, 2007		Sheet 31 of 34

# RESET MAP



# PWROK MAP



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## ICH8

GPIO	Alt Func	I/O/NC	Power	ToI	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	SYS2/3_FANTAC
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#8;OC#10
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

## JUMPER SETTING

JBAT1	(1-2) NORMAL	(2-3) CLEAR
-------	--------------	-------------

## SIO(F71882)

PIN NAME	USAGE	Input/Output	NOTES
GPIO[2:0]	MCH_BSEL[2:0]	OUTPUT	PROGRAMED BSEL[2:0] OUTPUT
GPIO3	PCIEX1#	OUTPUT	PROGRAMED X1/X4 OPTION OUTPUT
GPIO4	UNUSED		
GPIO5	UNUSED		
GPIO6	UNUSED		
GPIO7	WDT#	OUTPUT	WATCH DOG TIMER RESET OUTPUT
GPIO10	DLED1	OUTPUT	DEBUG LED OUTPUT 1
GPIO11	UNUSED		
GPIO12	UNUSED		
GPIO13	BEEP	OUTPUT	
GPIO14	UNUSED		
GPIO15	DLED2	OUTPUT	DEBUG LED OUTPUT 2
GPIO16	DLED3	OUTPUT	DEBUG LED OUTPUT 3
GPIO17	UNUSED		
GPIO20	PLTRST_BU#1	OUTPUT	PCI RESTE BUFFER1
GPIO21	PLTRST_BU#2	OUTPUT	PCI RESTE BUFFER2
GPIO22	PLTRST_BU#3	OUTPUT	PCI RESTE BUFFER3
GPIO23	UNUSED		
GPIO24	PWR_OK	INPUT	ATX POWER OK INPUT
GPIO26	PWRBTIN	INPUT	FRONT PANNEL POWER BUTTON
GPIO27	PWRBTN#	OUTPUT	POWER BUTTON BUFFER OUT
GPIO30	SLP_S3#	INPUT	FRONT SOUTBRIDGE S3#
GPIO31	PSON#	OUTPUT	OUTPUT FOR ATX POWER ON
GPIO32	DLED4	OUTPUT	DEBUG LED OUTPUT 4
GPIO33	UNUSED		
GPIO40	SYS2_FANTAC	INPUT	
GPIO41	UNUSED		
GPIO42	IRTX	OUTPUT	
GPIO43	IRRX	INPUT	
VIDIN[2:0]	CPU_BSEL[2:0]	INPUT	CPU BSEL[2:0] INPUT
VIDIN3	UNUSED	INPUT	RESERVED FOR PCIE X4 INDICATION

## DDR-III DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	00	P/N_DDR0_A P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B P/N_DDR4_B

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	CK_P_33M_S2
1394	PIRQ#D	PREQ#2 PGNT#2	AD18	CK_P_33M_1394



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HW Ver.0A Change to Ver.0B List:

- 1.Remove Q54 and R374and short Q54 B,C pin for power sequence.(page26)
- 2.U24 power change from VCC3 to 3VSB for power sequence.(page26)
- 3.Change EC42 from 470u to 820u for V\_FSB\_VTT power noise.(page26)
- 4.Change EC52 from 470u to 820u for SB1\_05 power noise.(page26)
- 5.Change EC53 from 470u to 820u for SB1\_5 power noise.(page26)
- 6.CPU\_GTLREF resistor value R119 , R115, R128, R104 change from 50ohm to 100ohm for pull-up(intel suggestion)(page4)
- 7.CPU\_GTLREF resistor value R124 , R117 , R141 , R105 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page4)
- 8.MCH\_GTLREF resistor value R190 change from 50ohm to 100ohm for pull-pu.(intel suggestion)(page6)
- 9.MCH\_GTLREF resistor value R195 change from 100ohm to 200ohm for pull-down.(intel suggestion)(page6)
- 10.SRCOMP[3:0] R223 , R227 , R184 , R182 change from 20ohm to 19.1ohm.(intel suggestion)(page7)
- 11.DDR2 termination RN16 , RN26 , RN11 , RN14 , RN27 , RN12 , R171 change from 39ohm to 43ohm.(intel suggestion)(page14)
- 12.Add CK\_DOT96\_MCH\_DP pull-high 1.25V and CK\_DOT96\_MCH\_DN pull-down for non-graphic SKU.(intel suggestion)(page6)
- 13.RIRQ[H:A] pull-up 2.7Kohm to VCC5.(intel suggestion)(page22)
- 14.USB have two group [5:0] EHCI#1,[6:11EHCI#2 , please one group to real and one group to front.(intel suggestion)(page24)
- 15.Audio VREFOUT\_E and VREFOUT\_F swap.(for schematic error)(page20)
- 16.Audio BASS and CEN\_OUT swap.(for schematic error)(page20)

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