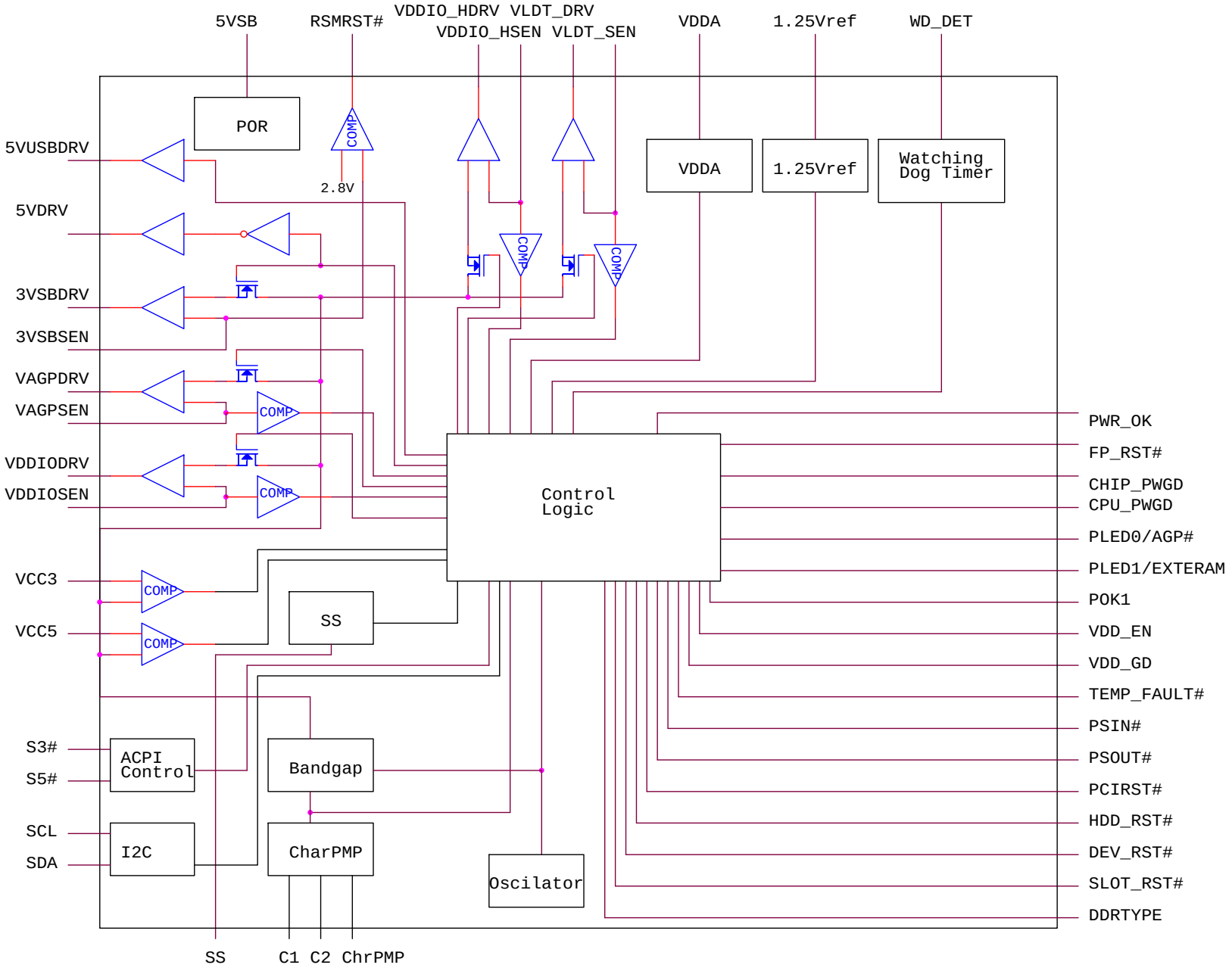
AMD K8 ACPI Controller

Internal Block Diagram



Power Function

- Support voltage regulator:
- DDR 1 or DDR 2 voltage regulator
  - DDR 1 or DDR 2 voltage select by DDRTYPE (Pin 18) select pin
  - External DDR standby voltage MOS is request when S3 state
  - Support 2 set Linear mode or PWM mode select by PLED1/EXTRAM(Pin 48)
  - The both mode support Adjust voltage through I2C bus
  - DDR 1 voltage range : 2.5V,2.55V,2.6V,2.65V,2.7V,2.75V,2.8V,2.85V,2.9V,3.0V,3.1V and default setting is 2.55V
  - DDR 2 voltage range : 1.7V,1.75V, 1.8V, 1.85V,1.9V,1.95V,2.0V,2.05V,2.1V,2.2V,2.3V and default setting is 1.8V
  - Power Good Watching Dog timer register (CR0x05) can setting keep or not when power off
- AGP voltage regulator
  - Support Linear mode or PWM mode
  - The both mode support Adjust voltage through I2C bus
  - AGP voltage range : 1.5V,1.55V,1.6V,1.65V,1.7V,1.75V,1.8V,1.85V and default setting is 1.5V
  - Power Good Watching Dog timer register (CR0x05) can setting keep or not when power off

Power Function (Cont.)

- 3VSB regulator
  - Support Single or Dual mode select by PLED0 (RAC version)
  - Support Dual mode select only (RBF version)
  - Single mode : Used one MOS regulate from 5VSB to 3VSB
  - Dual mode : Used two MOS when S3 or S5 state standby MOS regulate from 5VSB to 3VSB,When S0 state turn on VCC3 MOS to 3VSB
- 1.2VLDT regulator
  - Support Hyper Transport™ I/O ring power supply
- VDD regulator
  - Support core power supply

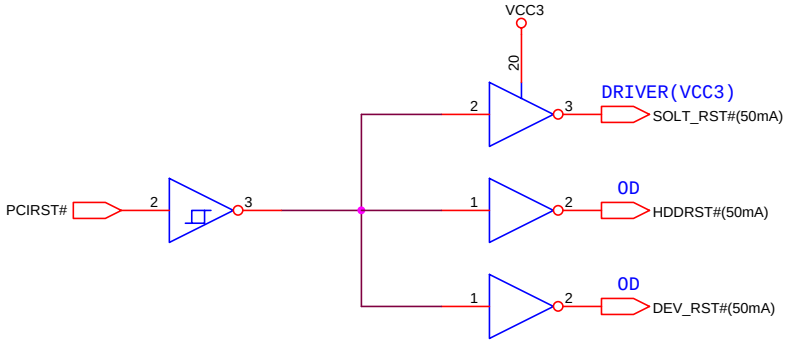
Power Function (Cont.)

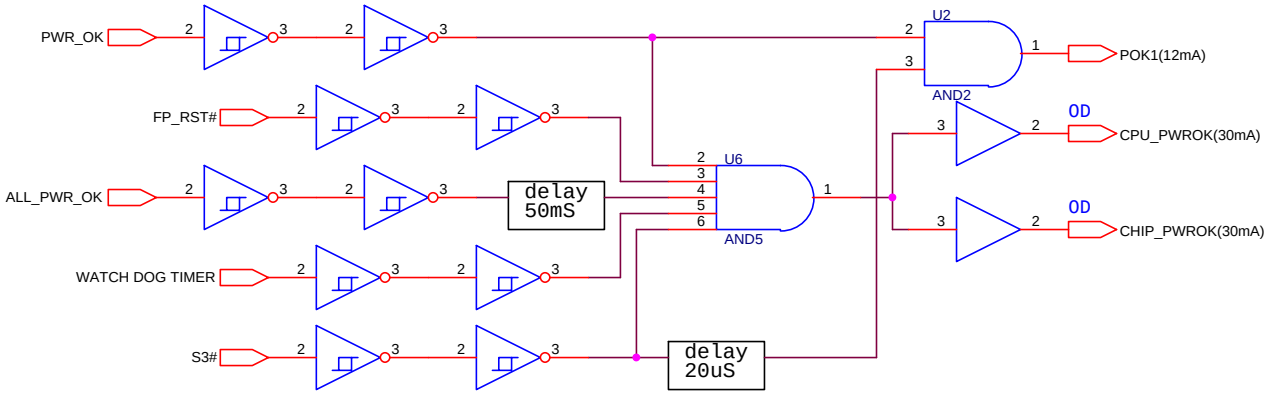
- Support 5VDUAL for USB and KB/MS voltage
- Support 9VSB for use OP-Amp extend extra voltage
- Support 1.25V reference voltage
- Support 2.5VDDA for Filtered PLL Supply Voltage
- DDR1(<1.9V), DDR2 (<1.25V), AGP(<1.1V), 1.2VLDT(<0.85V) and 3VSB(<2.45V) support power supply shutdown when under voltage protection

Digital Function

- Provide ATX PWR_OK and RST_ BTN input for 2 open drain output buffer (CPU_PWROK and CHIP_PWROK)
- Provide PWR_OK1 for power sequence or standby voltage isolate (This pin is ATX PWR_OK buffer output it can't be RST_BTN effect)
- Provide 1 to 3 PCIRST# output buffer,The SLOT_RST# is 3.3V TTL output else are open drain (HDDRST#, DEV_RST#)
- RSMRST# is delay 88ms from 3VSB ready
- Provide PLED0, PLED1 support S0,S1,S3,S5,under voltage, over temperature indicator:
  - Under voltage issue PLED0 and PLED1 flash by turn about 1/4Hz (If this condition occur system can't power on unless plug AC power core)
  - Over temperature issue PLED0 and PLED1 flash by turns about 1 Hz (If this condition occur, MS6 instantly into internal S5 state and disable ALL LUV Function. It can press power button 4 sec to release)

Digital Function (Cont.)



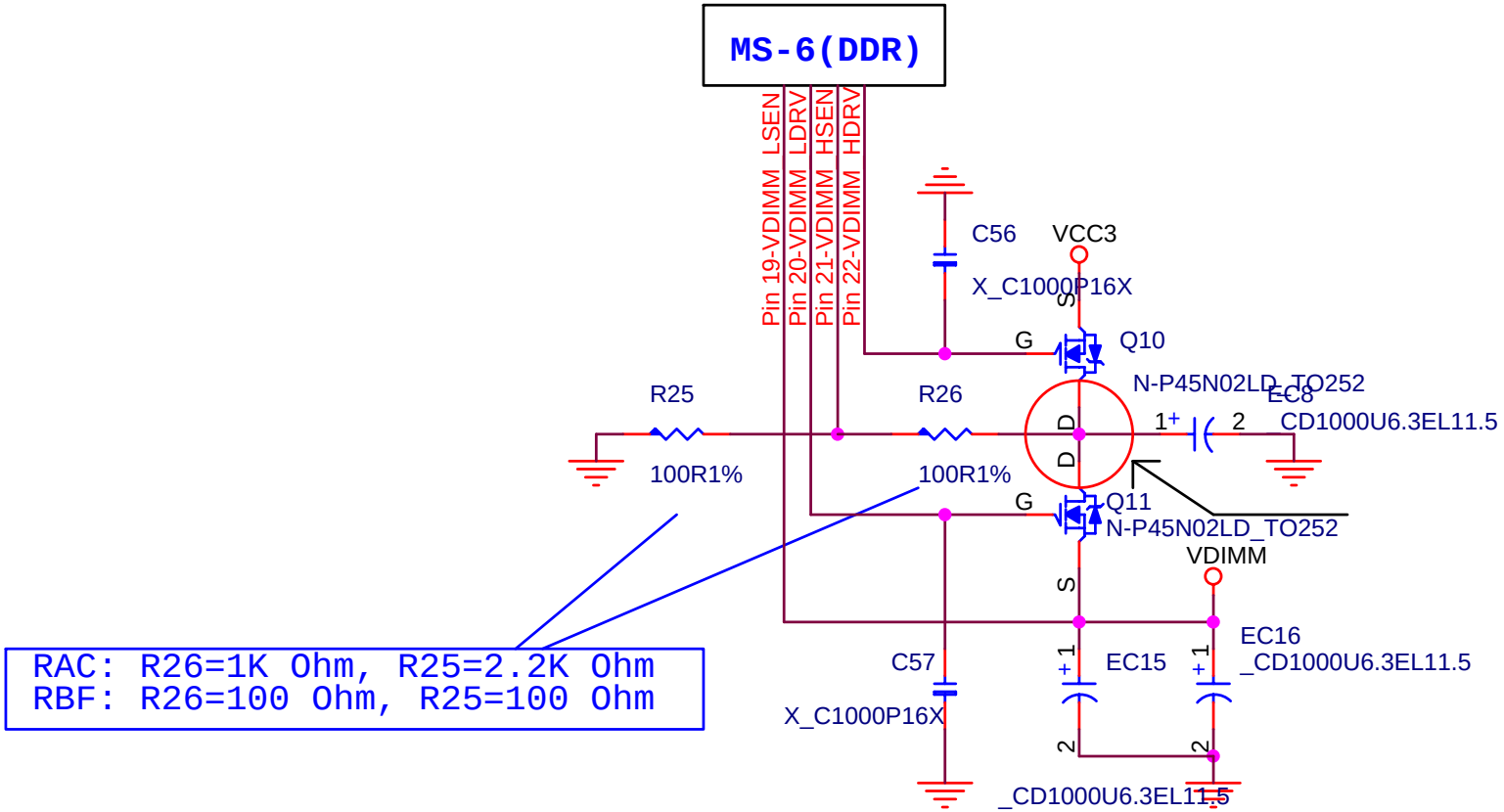


Circuit Design

DDR regulator:

(Linear mode for 754)

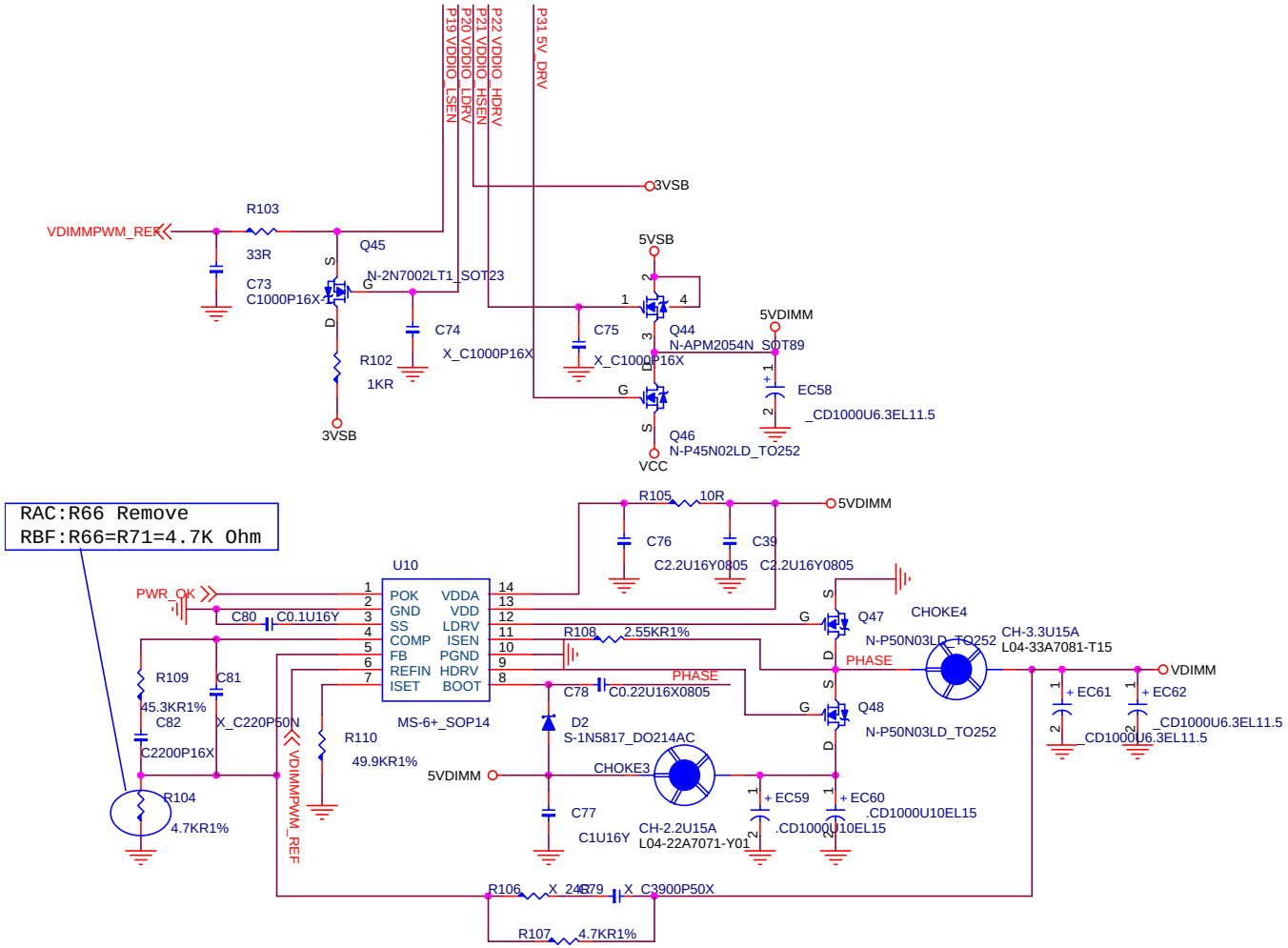
VDIMM LINEAR OR PWM SELECT	
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
EXTERNAL PWM OR LINEAR REGULATOR	PULL HIGH



Circuit Design

VDIMM LINEAR OR PWM SELECT	
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
EXTERNAL PWM OR LINEAR REGULATOR	PULL HIGH

DDR regulator: (PWM mode)

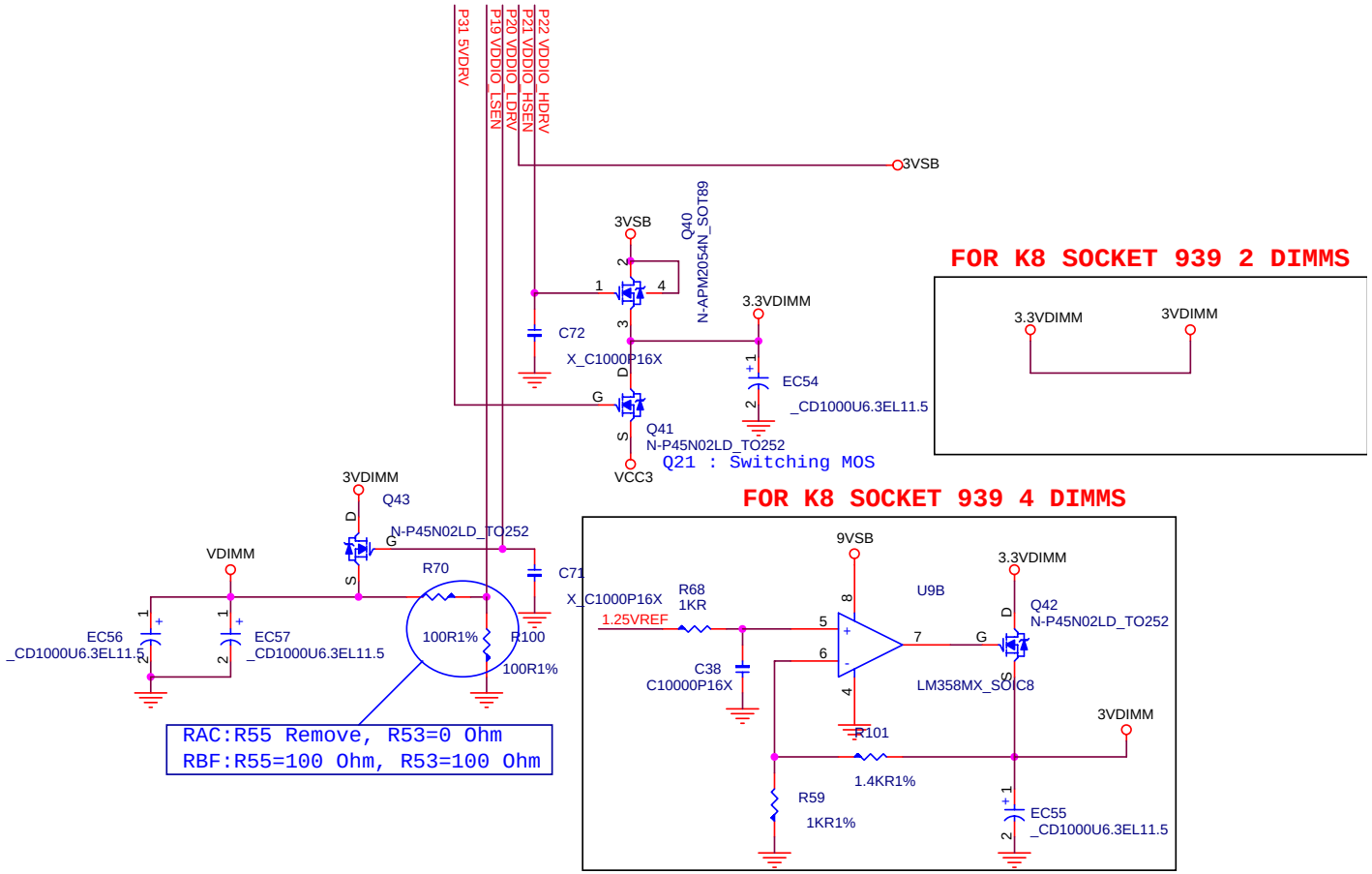


Circuit Design

DDR regulator:

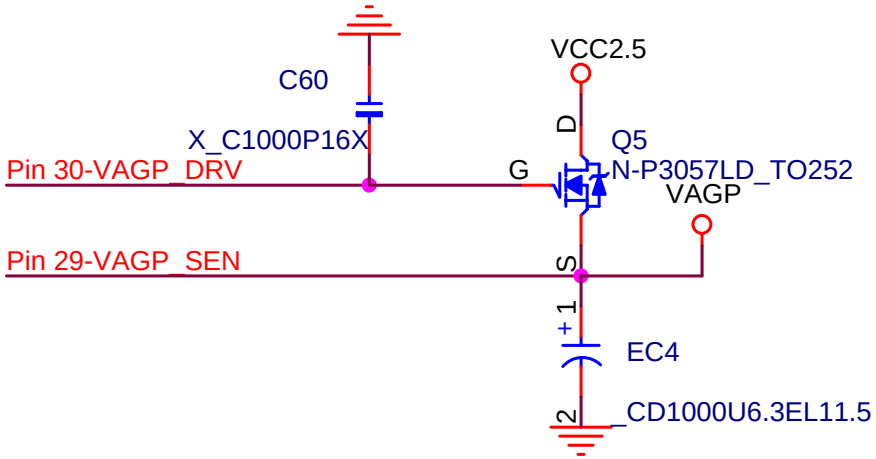
(Linear mode for 939)

VDIMM LINEAR OR PWM SELECT	
VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
EXTERNAL PWM OR LINEAR REGULATOR	PULL HIGH



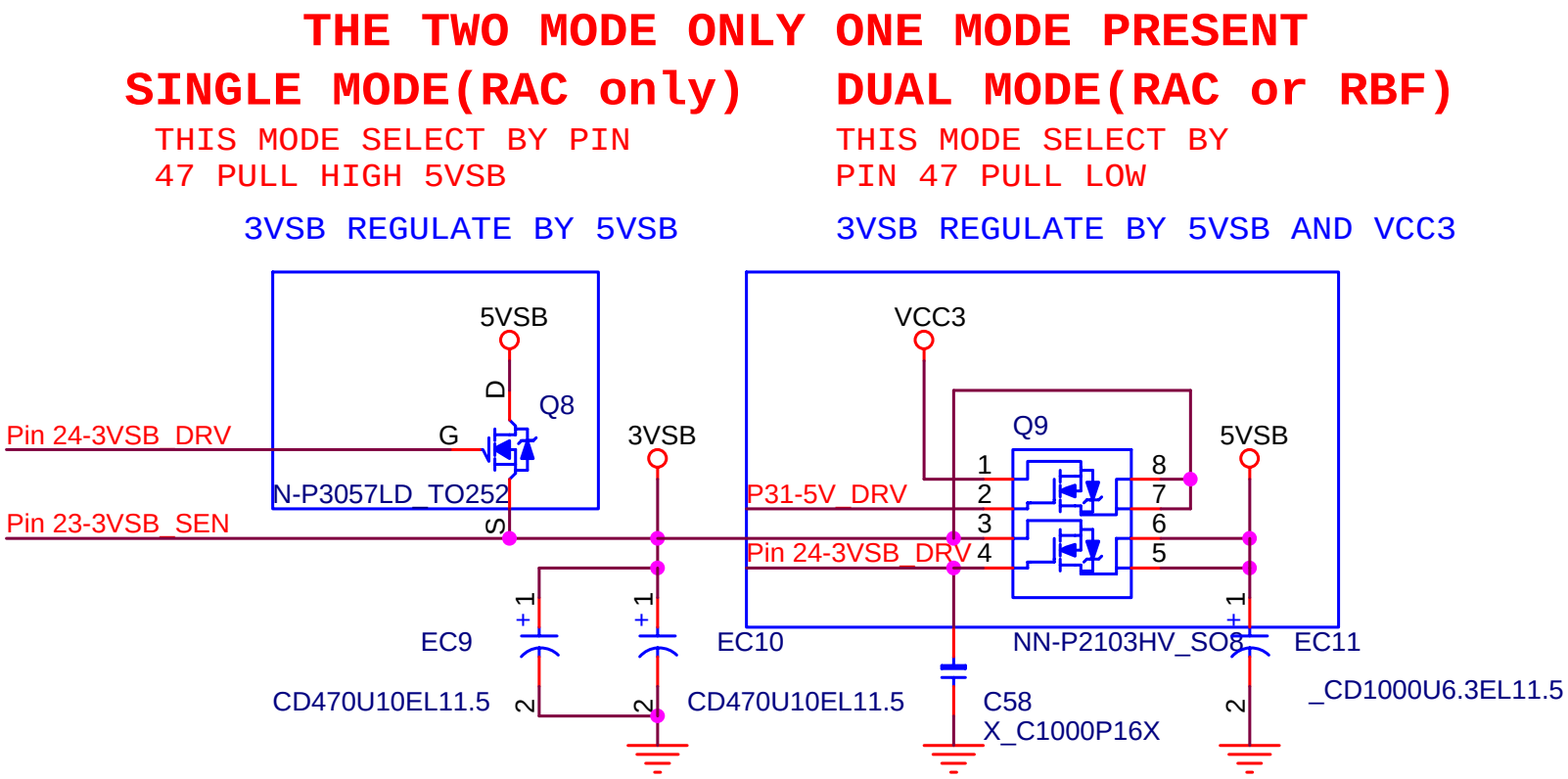
Circuit Design (Cont.)

AGP regulator:



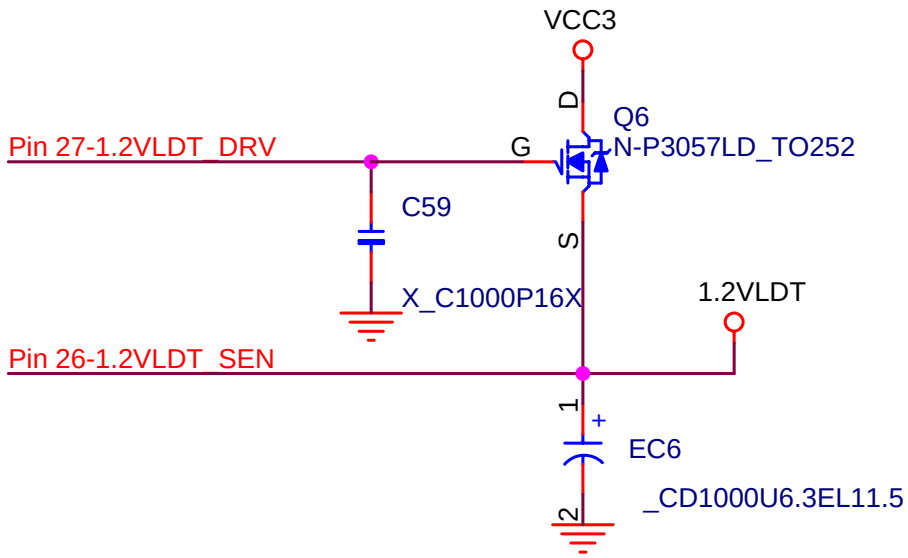
Circuit Design (Cont.)

3VSB regulator:



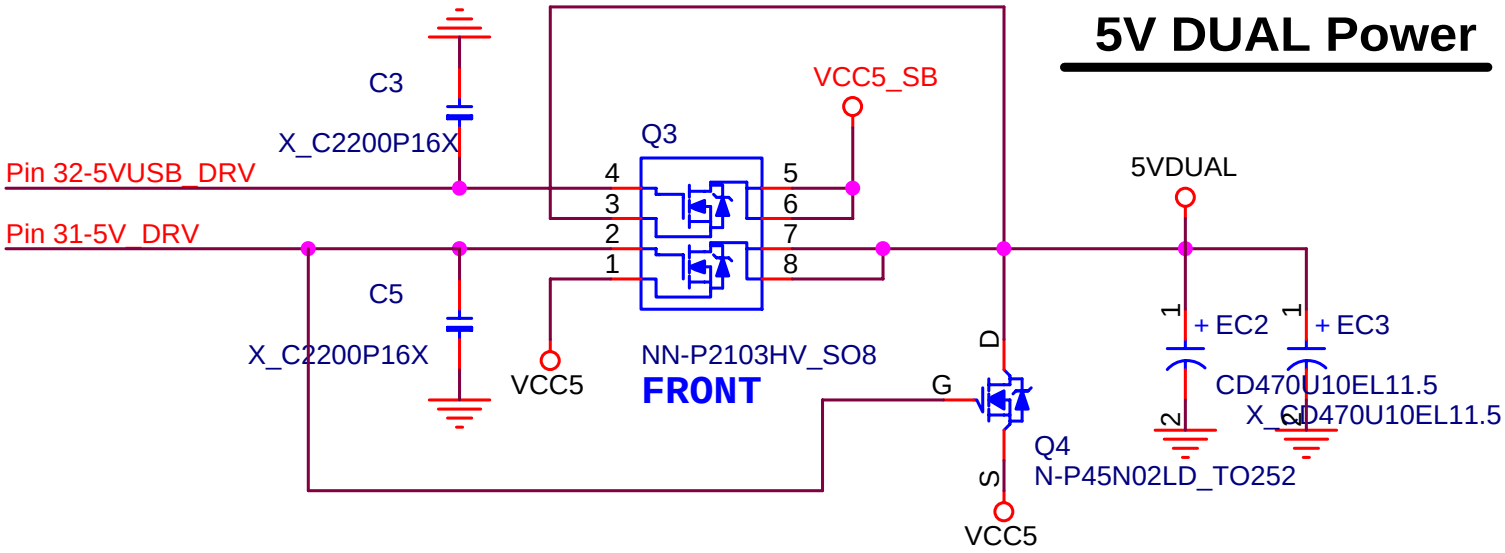
Circuit Design (Cont.)

1.2VLDT regulator:



Circuit Design (Cont.)

5VDUAL regulator:



Power sequence for AMD K8 (Signal Sequencing)

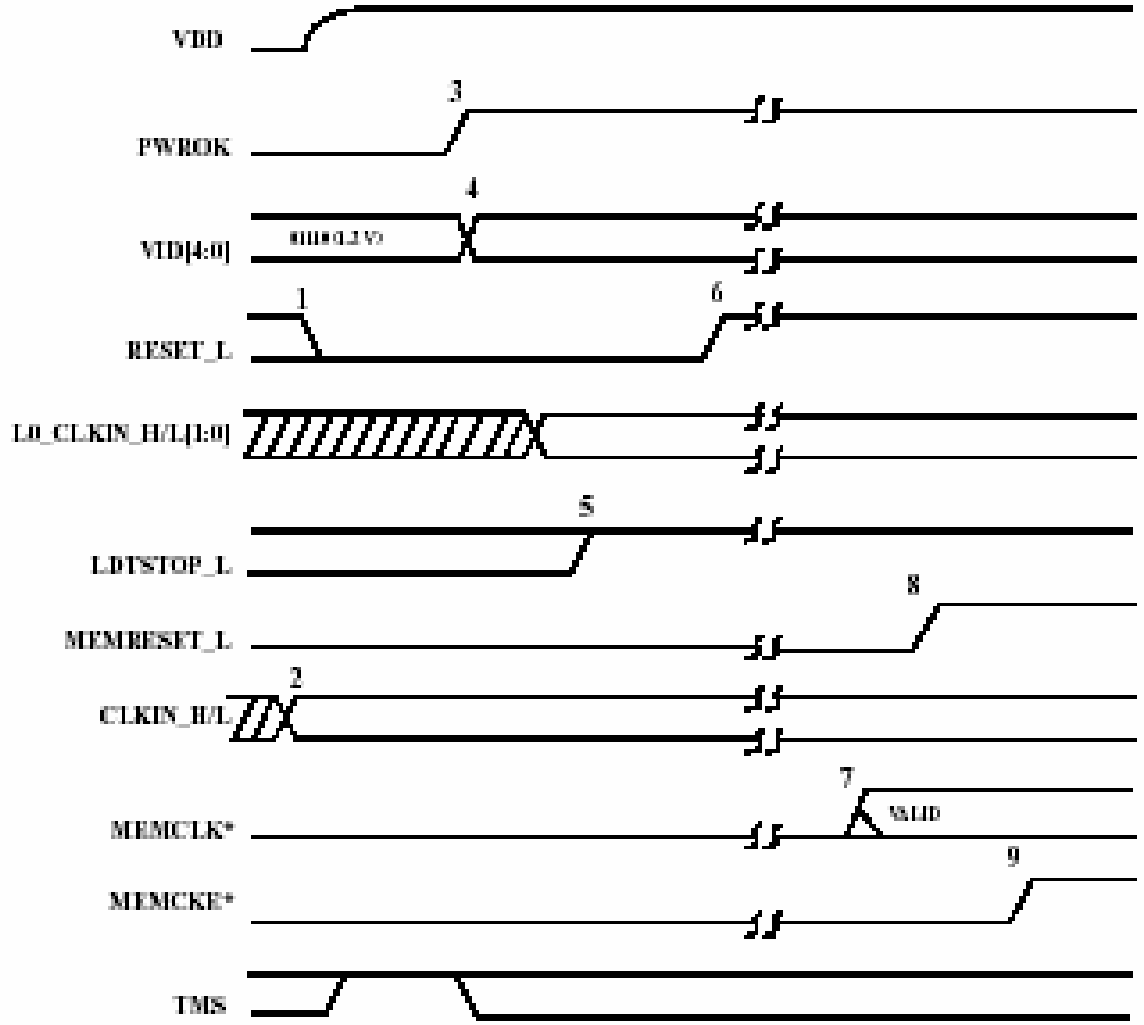


Figure 13. Power-Up Signal Sequencing

Power sequence for AMD K8
(Power supply Sequencing)