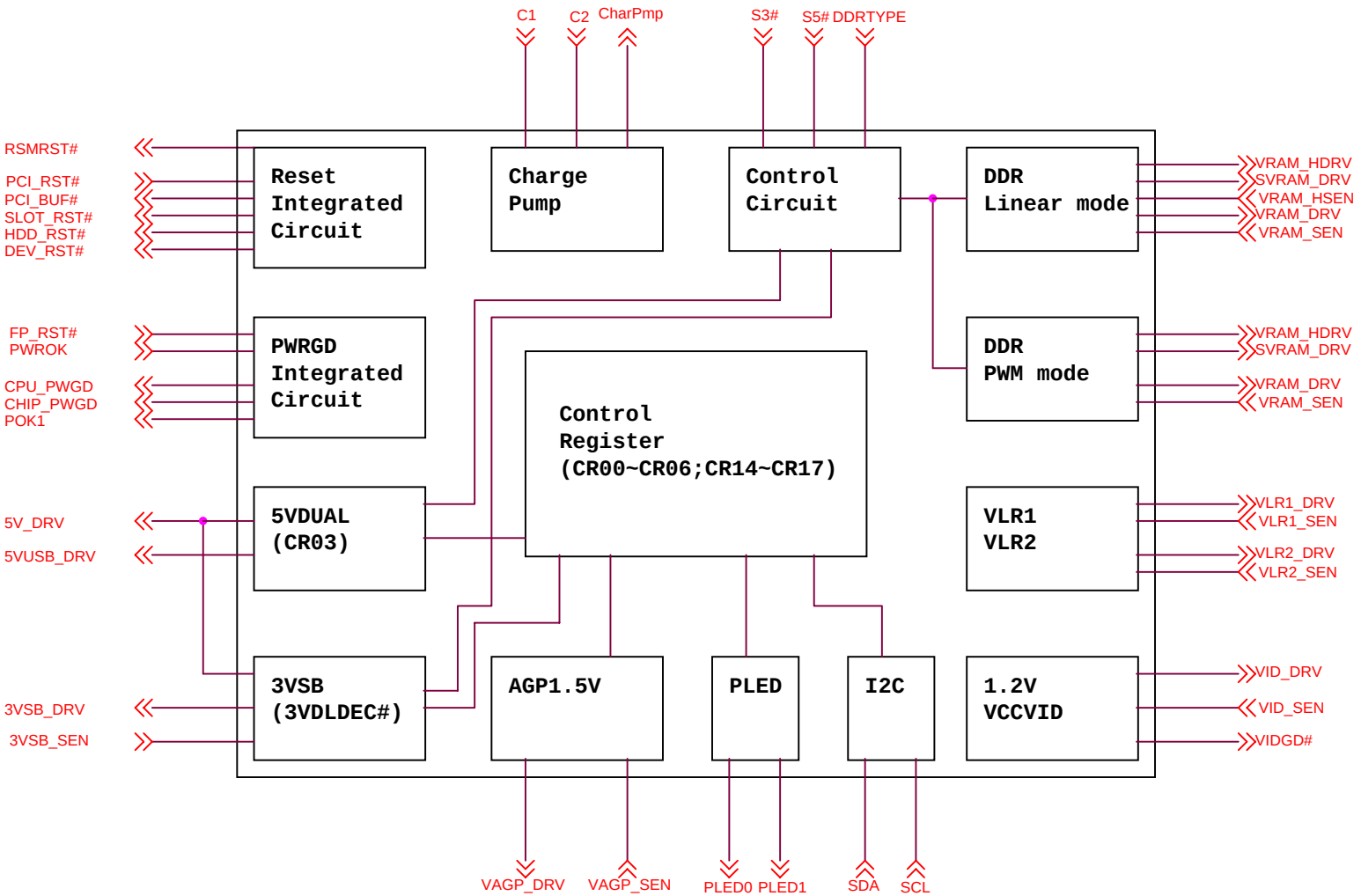

# Intel P4 & AMD K7 ACPI Controller

# Block Diagram



# Power Function

- Support voltage regulator:
- DDR 1 or DDR 2 voltage regulator
  - DDR 1 or DDR 2 voltage select by DDRTYPE (Pin 9) select pin
  - External DDR standby voltage MOS is request when S3 state
  - Support 2 set Linear mode or PWM mode select by PLED1/EXTRAM (Pin 48)
  - The both mode support Adjustment voltage through I2C bus
  - DDR 1 voltage range : 2.5V,2.55V,2.6V,2.65V,2.7V,2.75V,2.8V,2.85V,2.9V,3.0V,3.1V,3.2V,3.3V and default setting is 2.6V
  - DDR 2 voltage range : 1.8V,1.85V,1.9V,1.95V,2.0V,2.05V,2.1V,2.15V,2.2V,2.25V,2.3V,2.35V,2.4V and default setting is 1.8V
  - Watching Dog Timer register (CR0x06) can setting keep or not when power off
- AGP voltage regulator
  - Support Linear mode or PWM mode
  - The both mode support Adjust voltage through I2C bus
  - AGP voltage range : 1.5V,1.55V,1.6V,1.65V,1.7V,1.75V,1.8V,1.9V,2.0V,2.1V,2.2V and default setting is 1.55V
  - Watching Dog Timer register (CR0x06) can setting keep or not when power off

# Power Function (Cont.)

- 3VSB regulator
  - Support Single or Dual mode select by PLED0/3VDLDEC#(Pin47)
  - Single mode : Used one MOS regulate from 5VSB to 3VSB
  - Dual mode : Used two MOS when S3 or S5 state standby MOS regulate from 5VSB to 3VSB,When S0 state turn on VCC3 MOS to 3VSB
- P4 VCC_VID or K7 VCCA2_5 regulator
  - The default VREF is 1.2V
  - For K7 VCCA and left pin 13
- VLR1 and VLR2 regulator
  - Support standby or main VCC  regulator for on board chip or device
  - Both VREF is 1.2V and up 2,4,6,8,12,16 and 20% VREF by I2C adjust

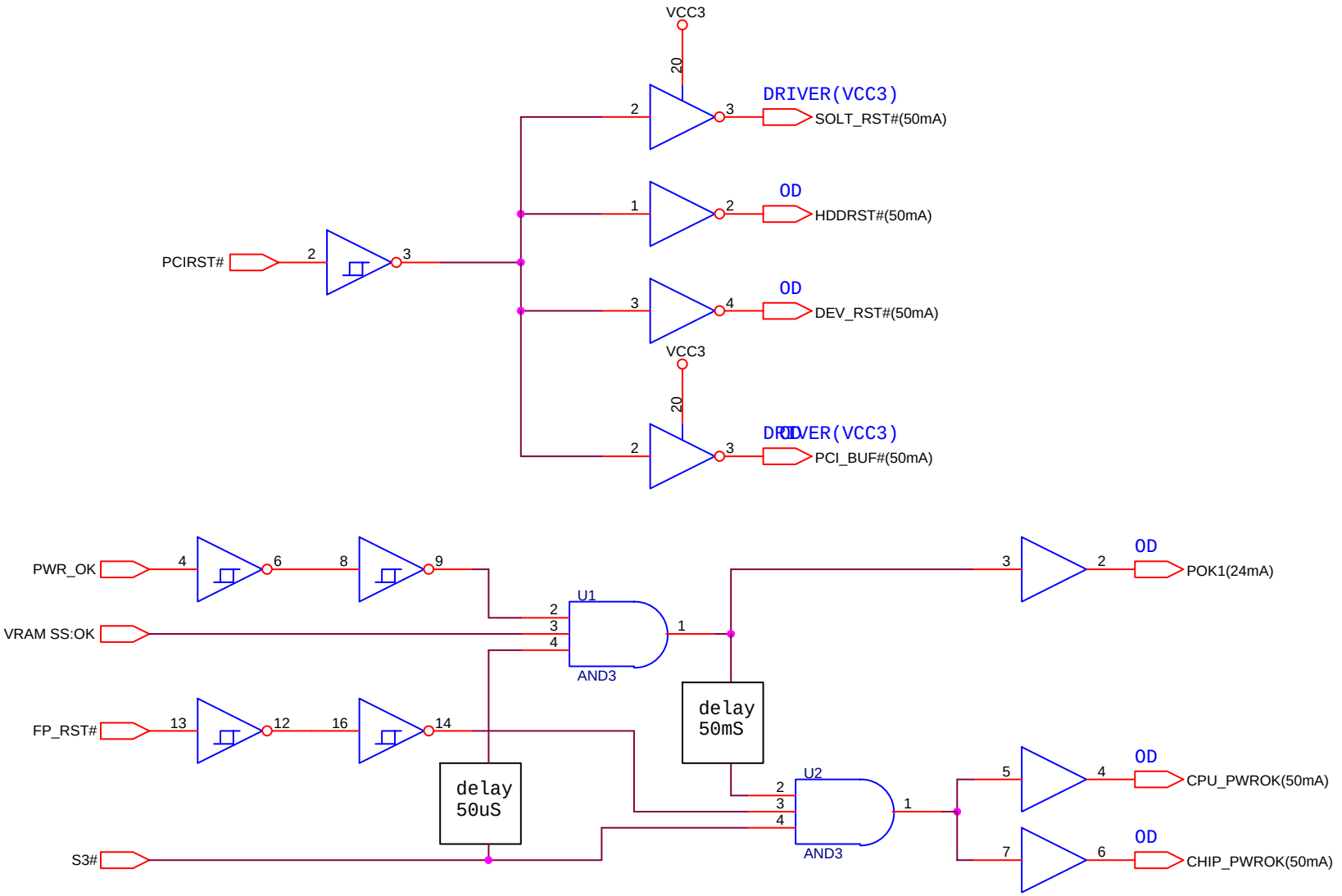
# Power Function (Cont.)

- Support 5VDUAL for USB and KB/MS voltage
- Support 9VSB for use OP-Amp extend extra voltage
- DDR1(<1.9V), DDR2(<1.25V),AGP(<1.1V) and 3VSB(<2.45V) support power supply shutdown when under voltage protection

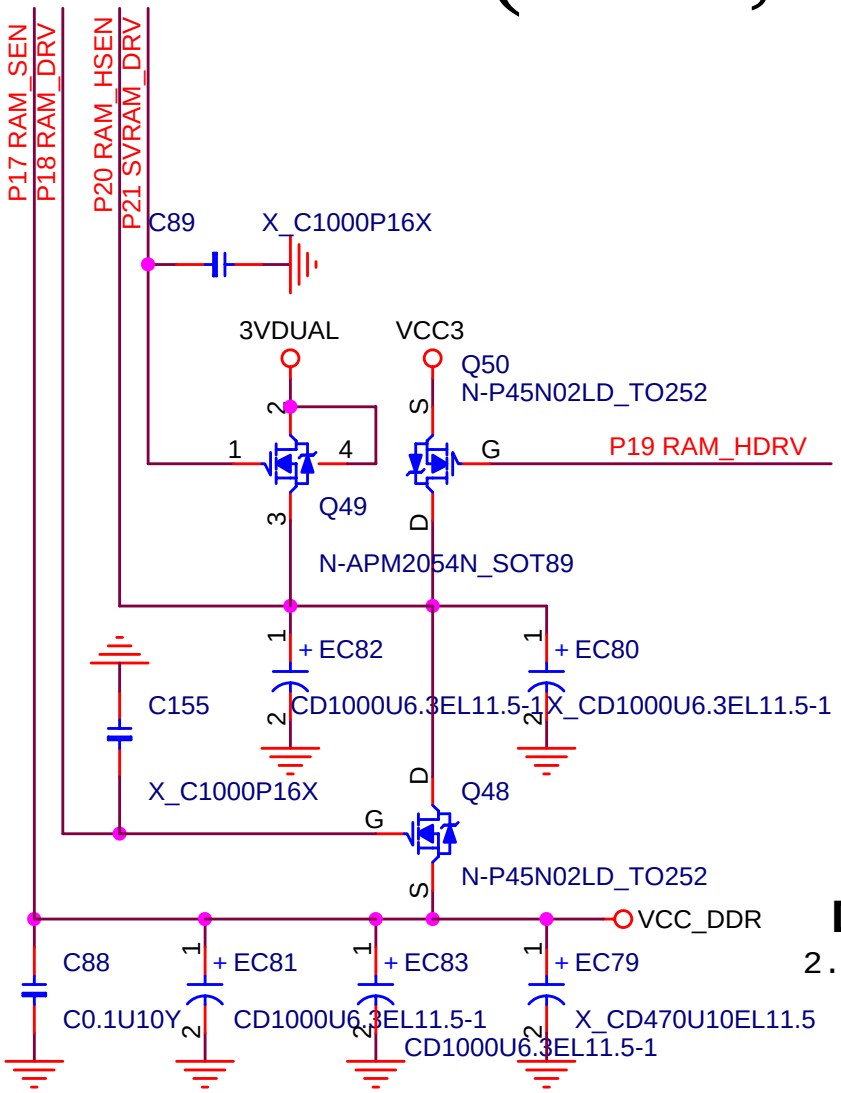
# Digital Function

- Provide ATX PWR_OK and RST_ BTN input for 2 open drain output buffer (CPU and chip PWR_OK)
- Provide PWR_OK1 for power sequence or standby voltage isolate (This pin is ATX PWR_OK buffer output it can't be RST_BTN effect)
- Provide 1 to 4 PCIRST# output buffer,The SLOT_RST# and BUF_RST# is 3.3V TTL output else is open drain (HDD_RST#, DEV_RST#)
- RSMRST# is delay 88ms from 3VSB ready
- Provide PLED0,PLED1 support S0,S1,S3,S5,under voltage indicator:
  - Under voltage issue PLED0 and PLED1 flash by turns about 1/4Hz (If this condition occur system can't power on unless plug AC power core)

# Digital Function



# Circuit design
# (DDR, Linear mode)




**VDIMM LINEAR OR PWM SELECT**

| VDIMM MODE | EXTRAM |
|---|---|
| LINEAR REGULATOR | PULL LOW |
| PWM REGULATOR | PULL HIGH |

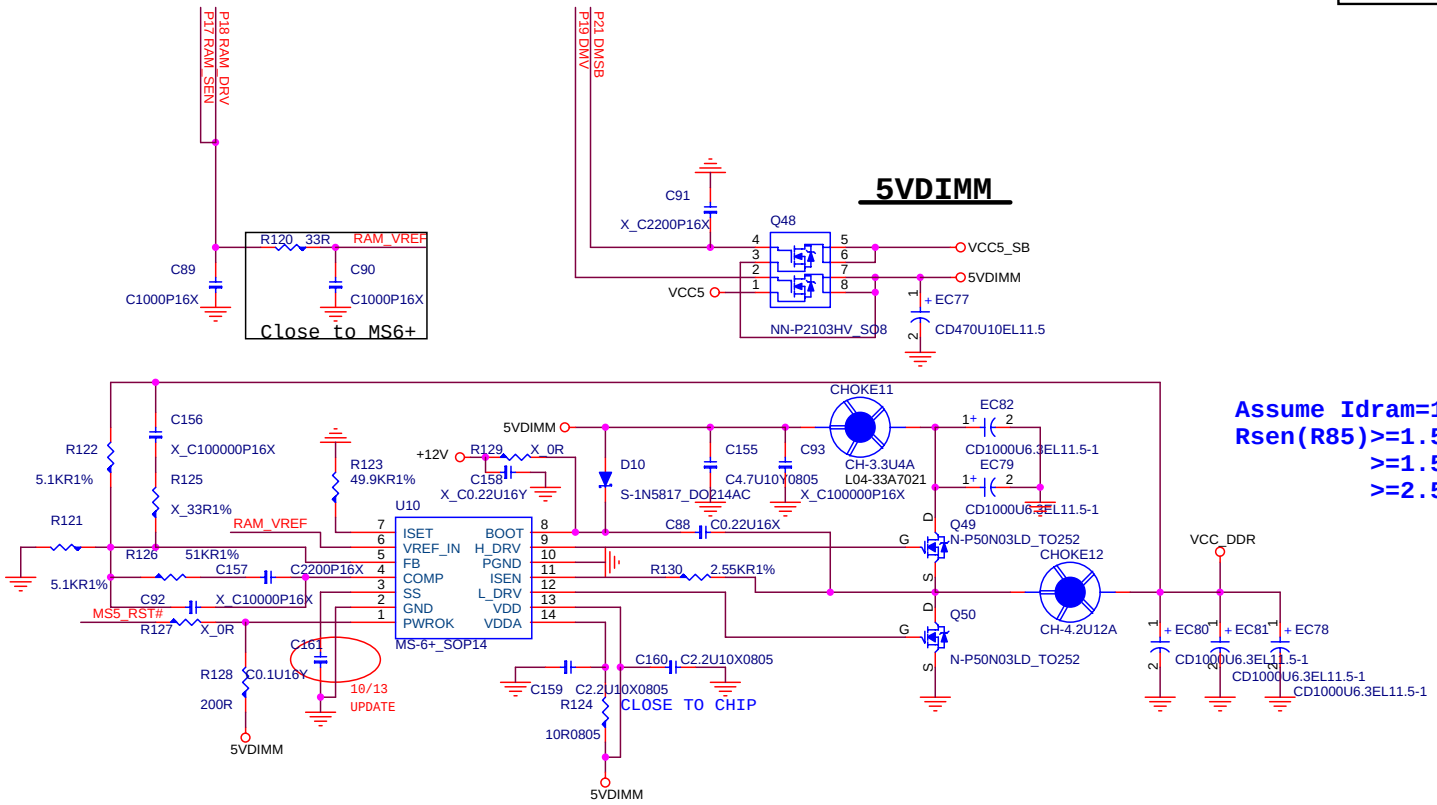
**DDR 2.5V Power**

2.5V/7A(DIMM)+5A(NB)

# Circuit Design (DDR, PWM mode)

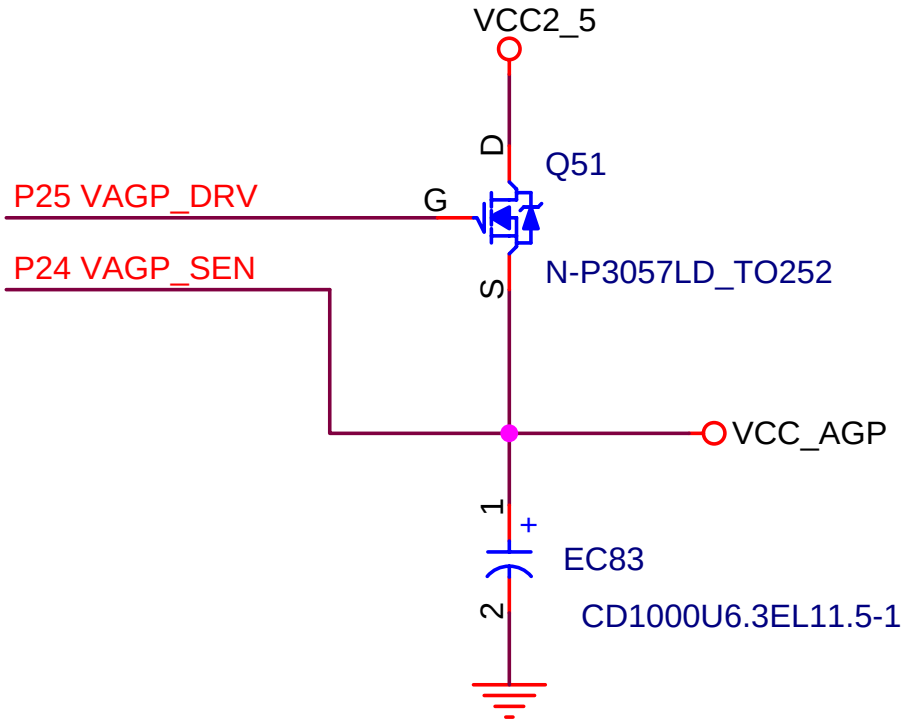
**VDIMM LINEAR OR PWM SELECT**

| VDIMM MODE | EXTRAM |
|---|---|
| LINEAR REGULATOR | PULL LOW |
| PWM REGULATOR | PULL HIGH |

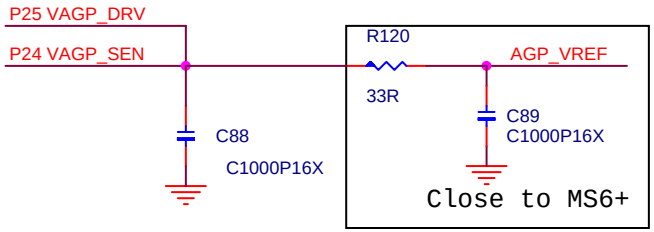



**Assume Idram=10A, P50N03LD Rds,on(max)=12mOhm**
**Rsen(R85)>=1.5*Idram*Rds,on(max)/72uA**
**>=1.5*10*12m/72u**
**>=2.5K Ohm**

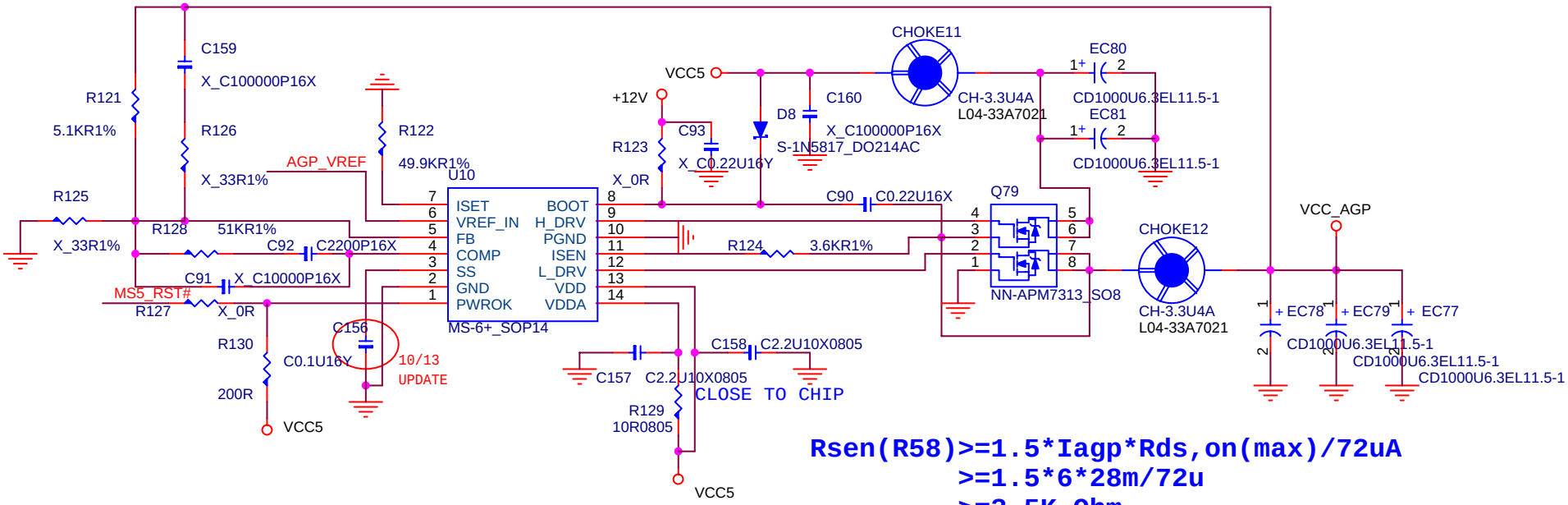
# Circuit Design
# (AGP, Linear mode)



# Circuit Design (AGP, PWM mode)




## AGP POWER

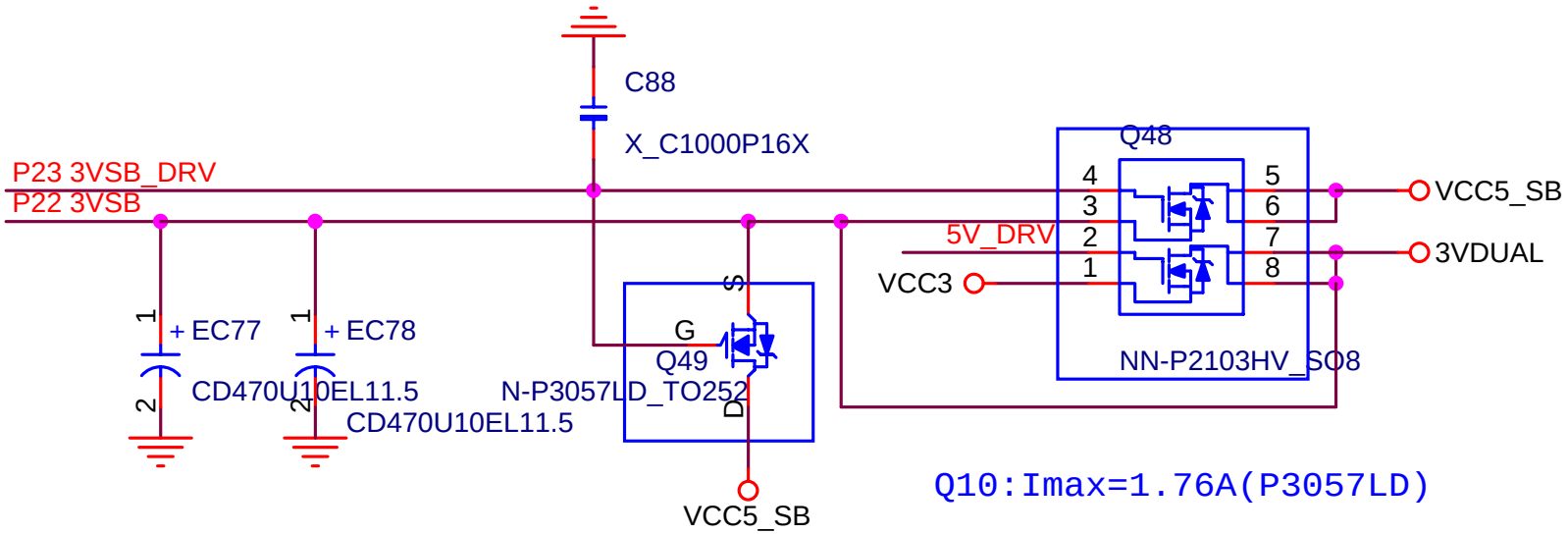



**Rsen(R58)>=1.5*Iagp*Rds,on(max)/72uA**
**>=1.5*6*28m/72u**
**>=3.5K Ohm**

# 3VSB

**3VSB MODE SELECT**

| 3VSB MODE | 3VDLDEC# |
|---|---|
| SINGLE MOSFET | PULL HIGH |
| DUAL MOSFET | PULL LOW |




Q10:Imax=1.76A(P3057LD)

3VSB REGULATE BY 5VSB  3VSB REGULATE BY 5VSB AND VCC3

**THE TWO MODE ONLY ONE MODE PRESENT**

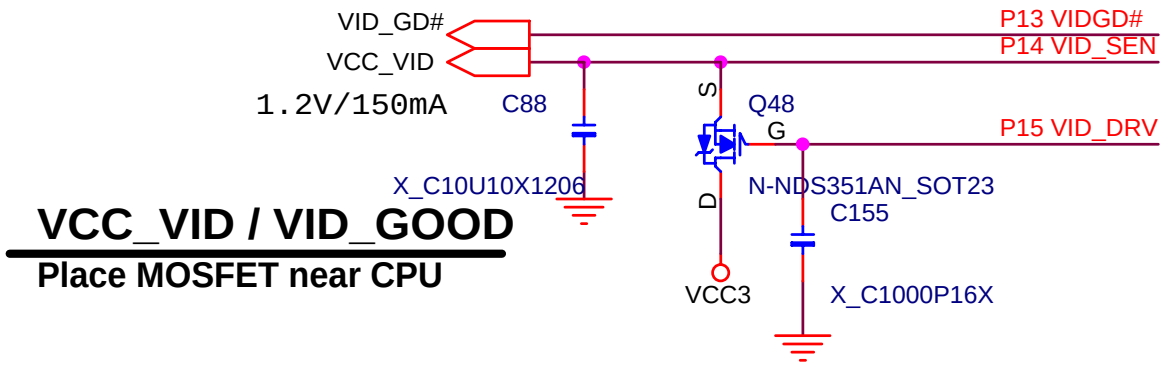
**SINGLE MODE**

THIS MODE SELECT BY PIN 47 PULL HIGH 5VSB

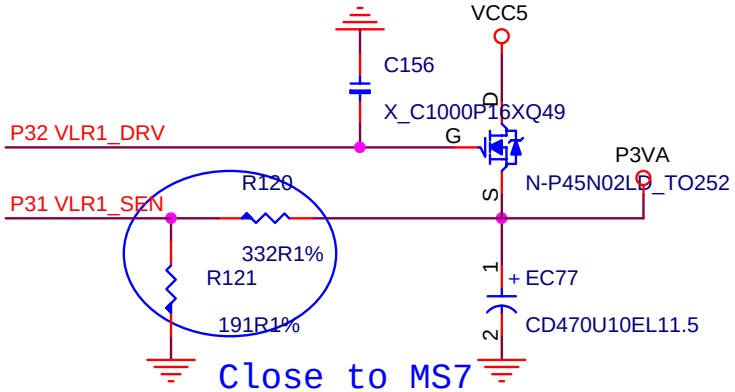
**DUAL MODE**

THIS MODE SELECT BY PIN 47 PULL LOW

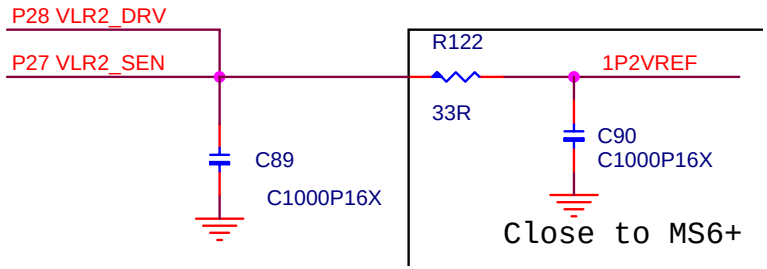
# VID, VLR1, VLR2




## VLR1



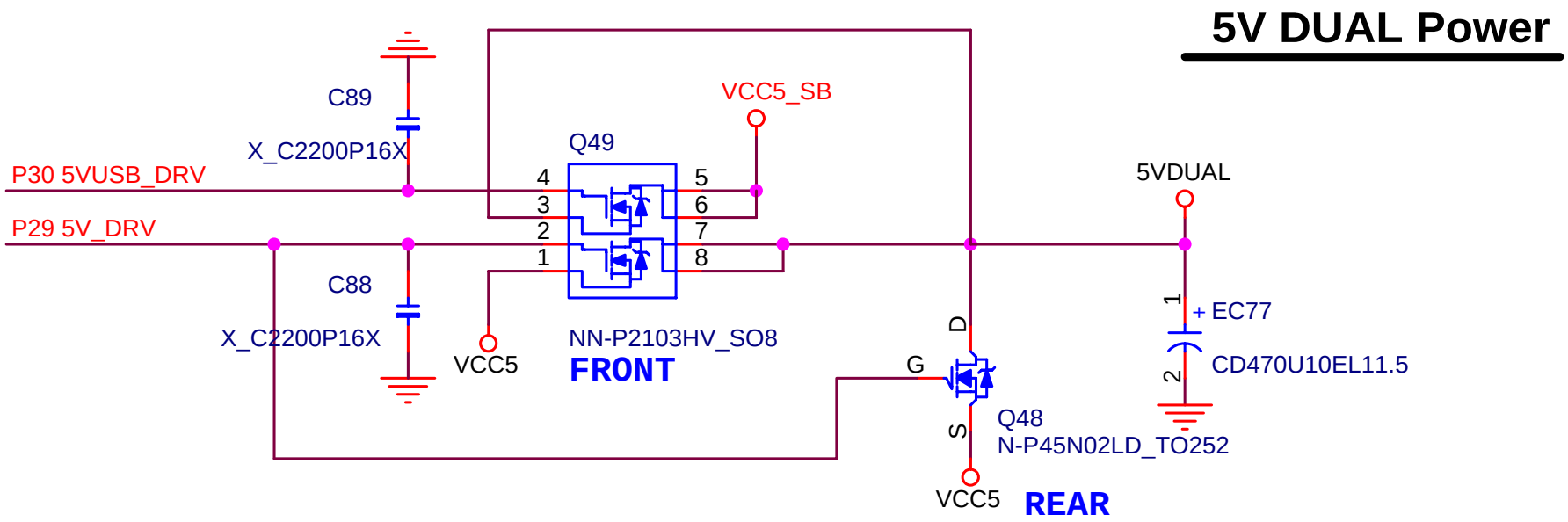

## VLR2



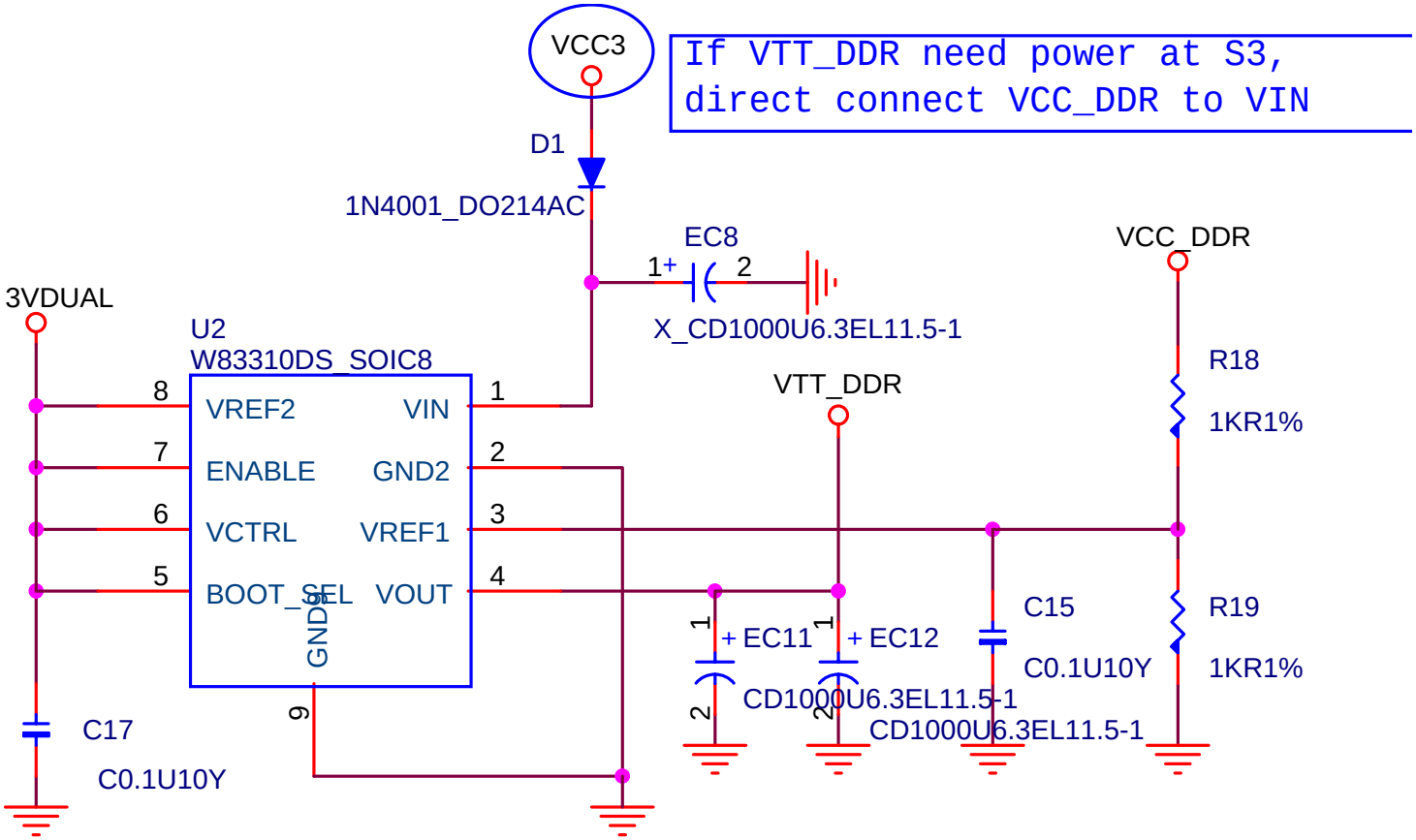
# 5VDUAL

**CR03 (5VUSB setting Register, Default 0x00h, Read/Write)**

| Bit1 | Bit0 | Condition |
|---|---|---|
| 0 | 0 | S0, S3 status support |
| 0 | 1 | S0, S3, S5 status support |
| 1 | 0 | S3, S5 status do not support |



# DDR VTT


VCC3
If VTT_DDR need power at S3,
direct connect VCC_DDR to VIN
D1
1N4001_DO214AC
EC8
1+
2
X_CD1000U6.3EL11.5-1
VCC_DDR
3VDUAL
U2
W83310DS_SOIC8
8
VREF2
VIN
1
7
ENABLE
GND2
2
6
VCTRL
VREF1
3
5
BOOT_SEL
VOUT
4
GND
9
VTT_DDR
R18
1KR1%
C15
C0.1U10Y
R19
1KR1%
EC11
EC12
CD1000U6.3EL11.5-1
CD1000U6.3EL11.5-1
C17
C0.1U10Y