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MS-7522M1

ATX V(

CPU: Nehalem-EP 1S, BloomField Processors In LGA1366 Package.

System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)
Intel ICH10R (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS133
LPC Super I/O -- Fintek F71882FG
Dual LAN --Realtek 8111C
HD Audio Codec -- RTL888/888 VC
PCIE to 1PATA/2SATA Bridge -- JMB-363
1S to 2S HW RAID-- Bridge JMB322 (1S interface from JMB-363)

Main Memory:

3-Channel A / B / C DDR-III * 6

Expansion Slots:

PCI EXPRESS X16 SLOT *2
PCI EXPRESS X1 SLOT*3
PCI SLOT * 2

PWM: VR11.1 Intersil ISL6336 (5 Phases)

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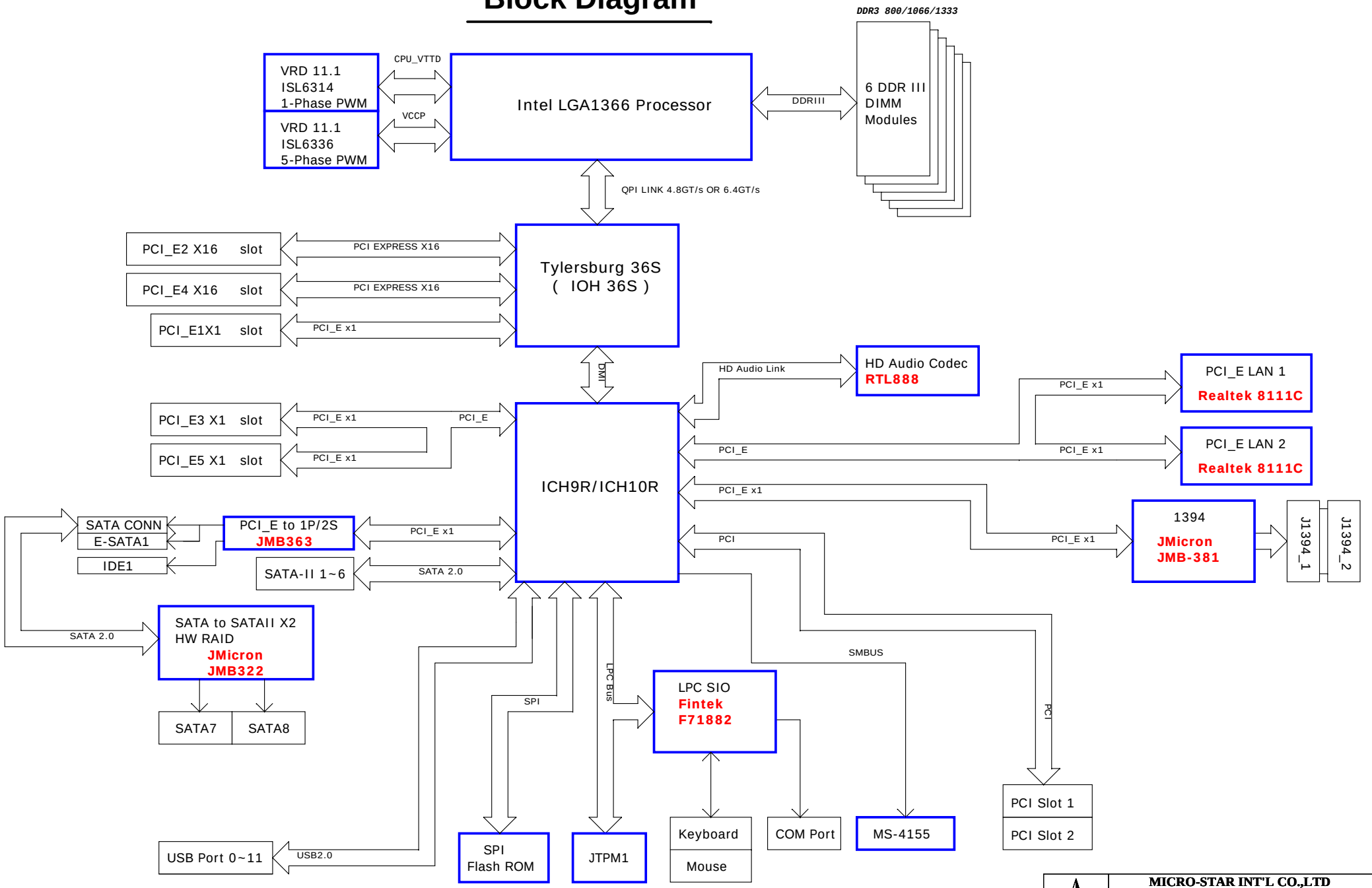
Block Diagram



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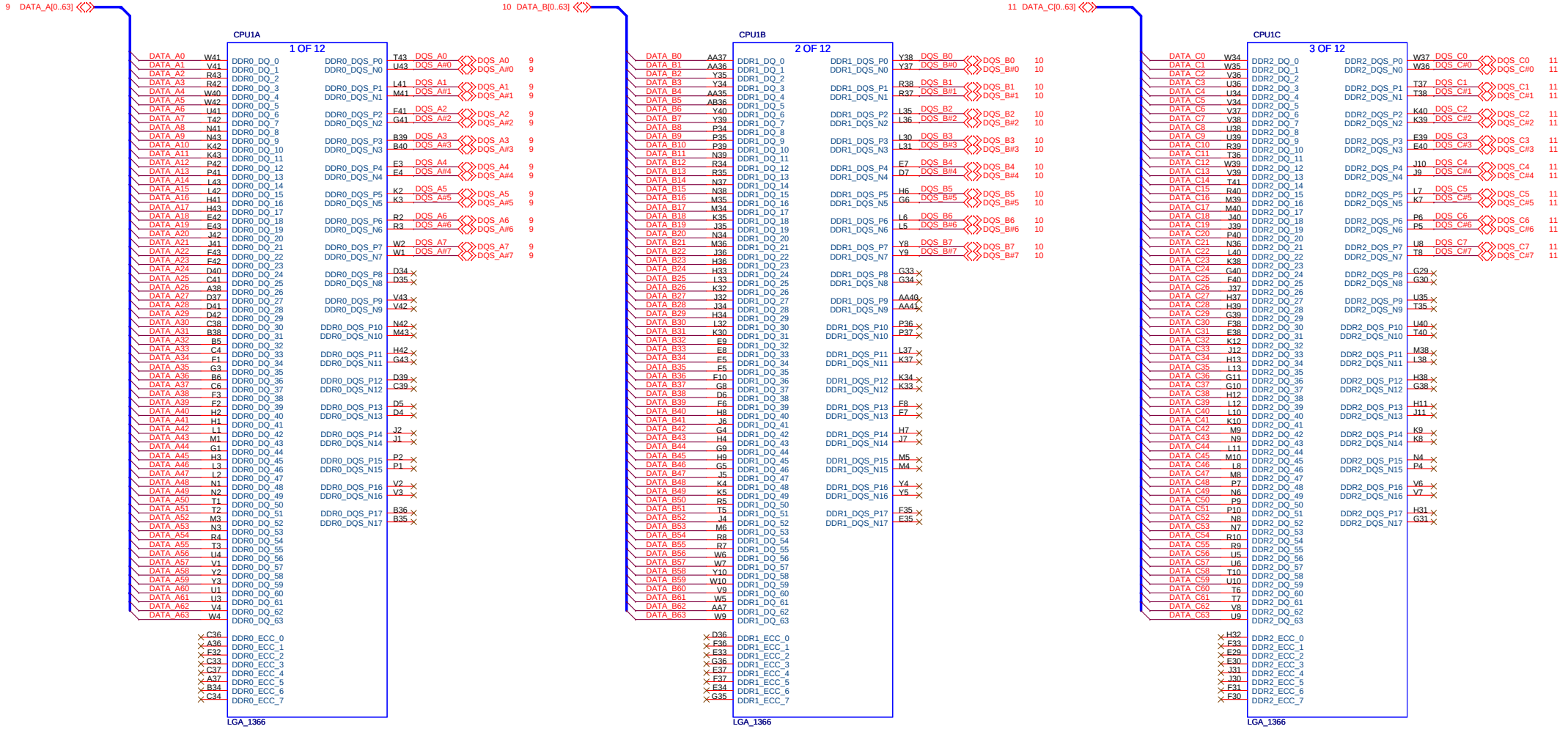

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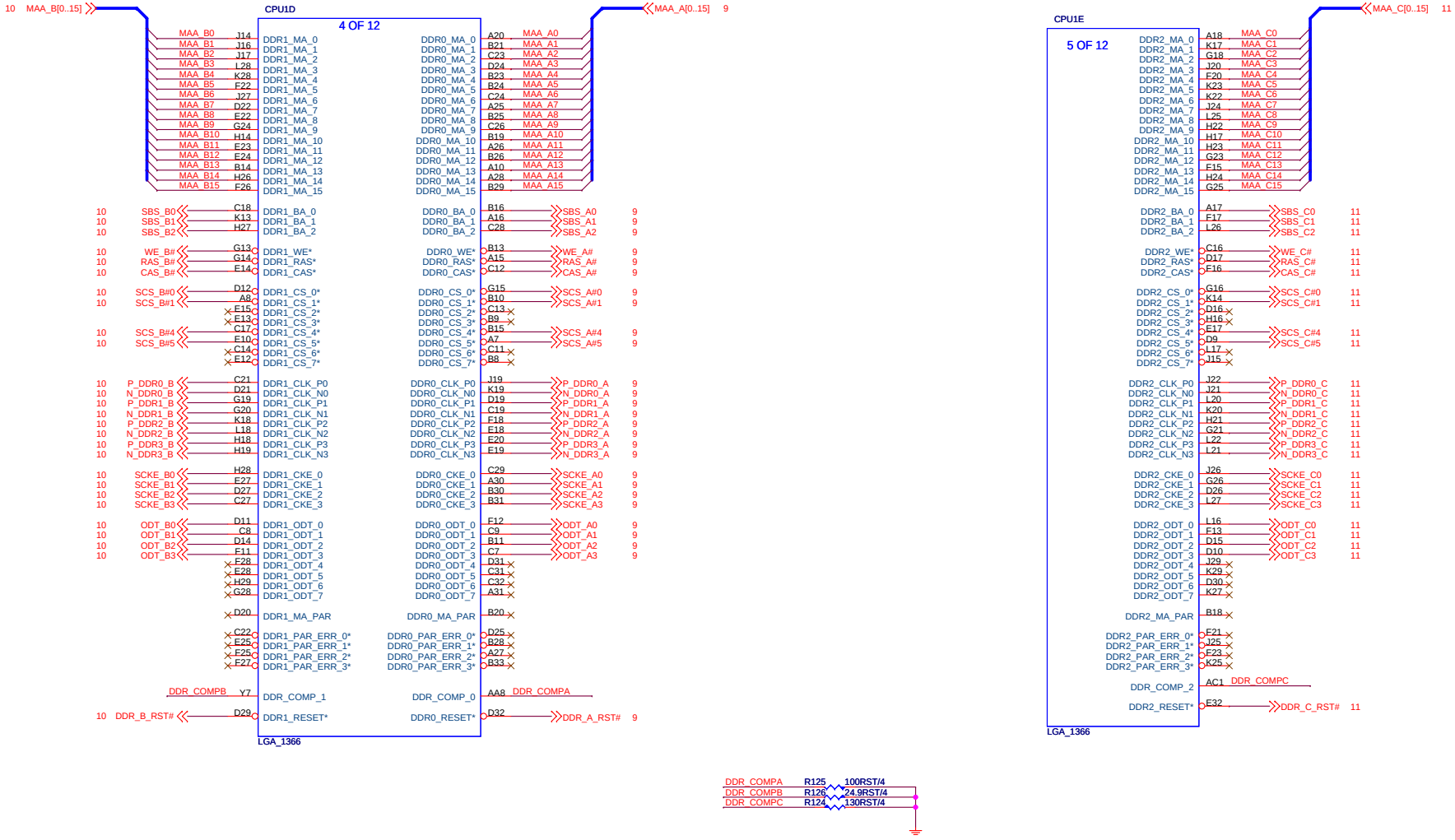

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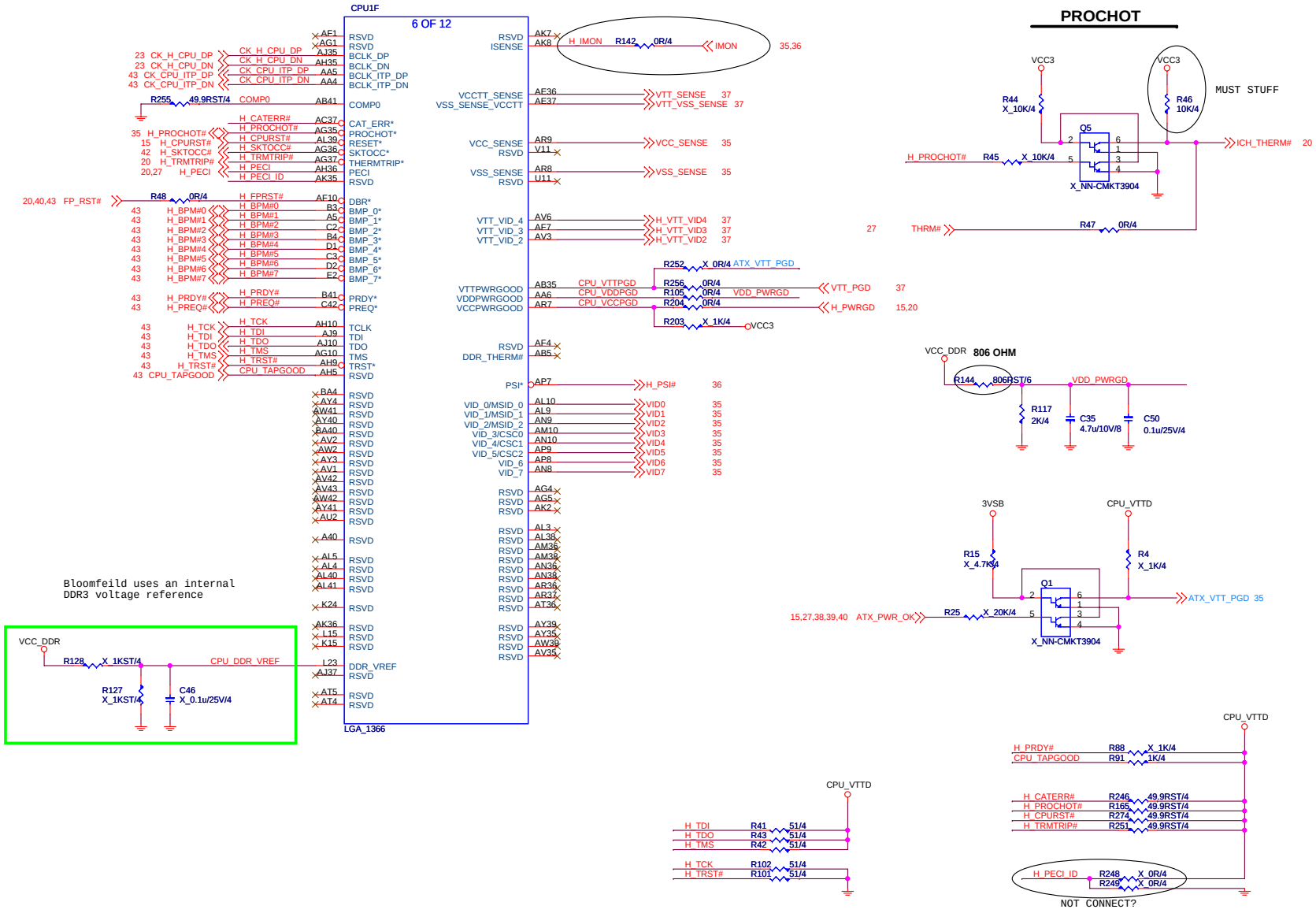
Size: Custom	Document Description: LGA1366-MEM COM/ADD/CTRL	Rev: 2.0
Date: Friday, October 24, 2008	Sheet 4 of 49	


CPU1F
6 OF 12
LGA_1366
PROCHOT
MUST STUFF
Bloomfeild uses an internal
DDR3 voltage reference
NOT CONNECT?
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LGA1366-SIGNAL
Size
Custom
Document Description
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2.0
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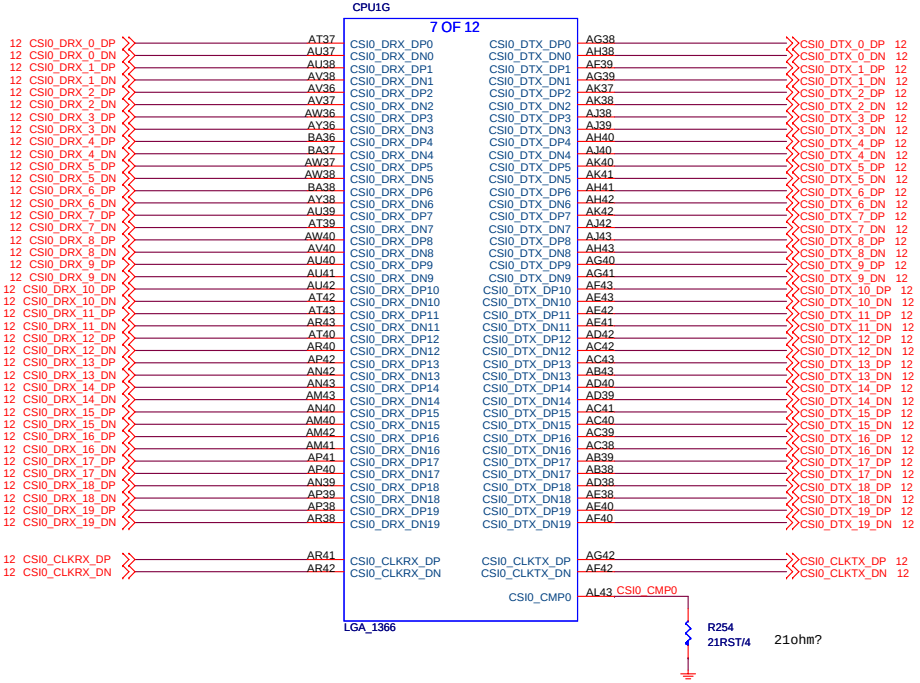

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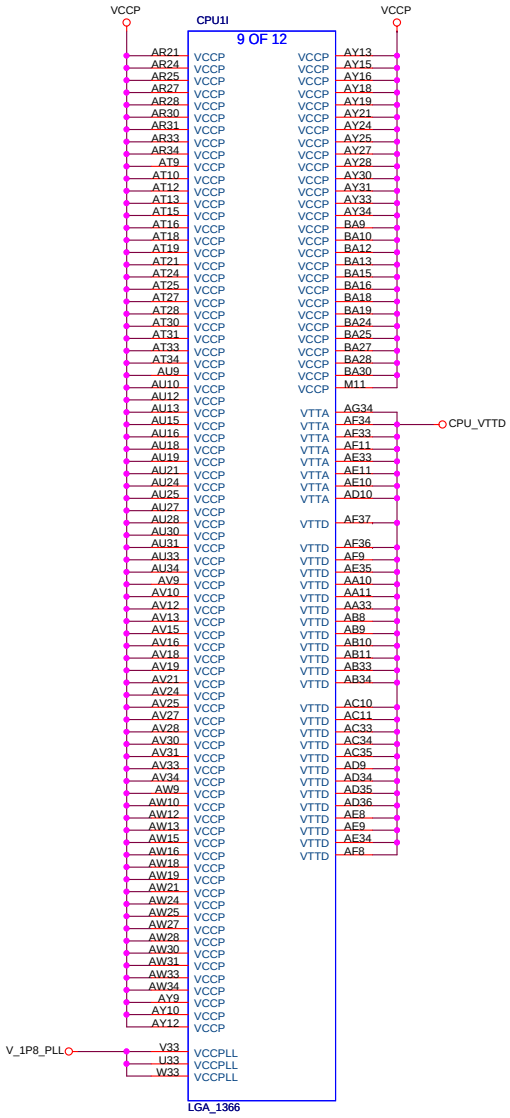

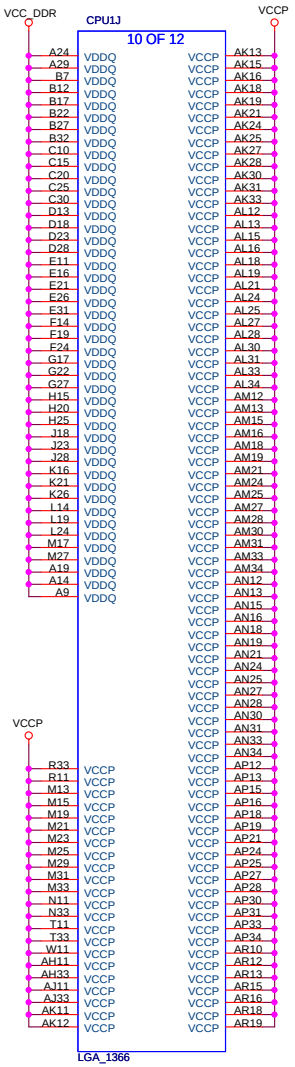

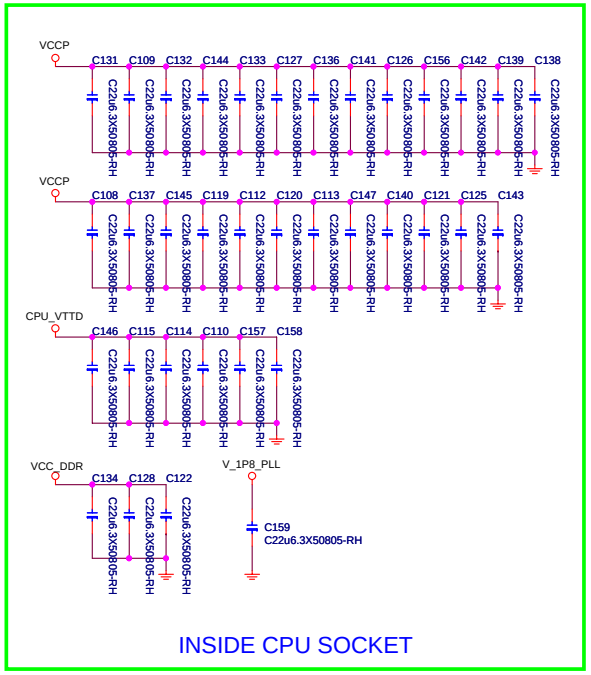

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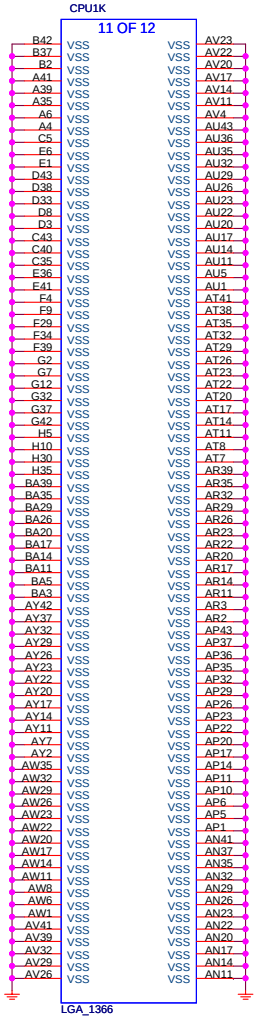

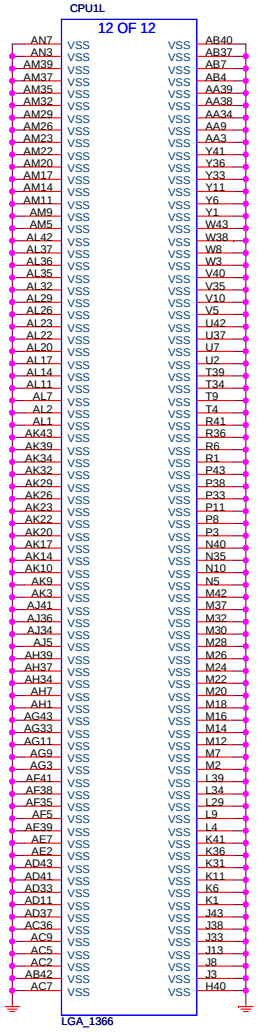

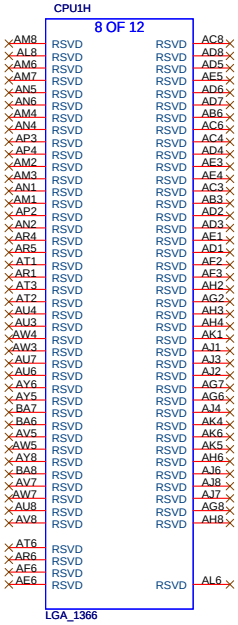

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DIMM1 / CHANNEL A0

DIMM2 / CHANNEL A1

Place DIMM Socket Power Plane

Close to the DIMM VTT_DDR Pin

UPI VOLTAGE CONSOLE

DDR3

DDR3

DDRIII-240P_BLACK-RH-8

ADDRESS = 0:0:0 [SA2:SA1:SA0]

DDRIII-240P_BLUE-RH-1

ADDRESS = 0:0:1 [SA2:SA1:SA0]

0.75 Vcc

0x62:RH=1.3K,RL=3.9K

0.25 Vcc

0x68:RH=3.9K,RL=1.3K

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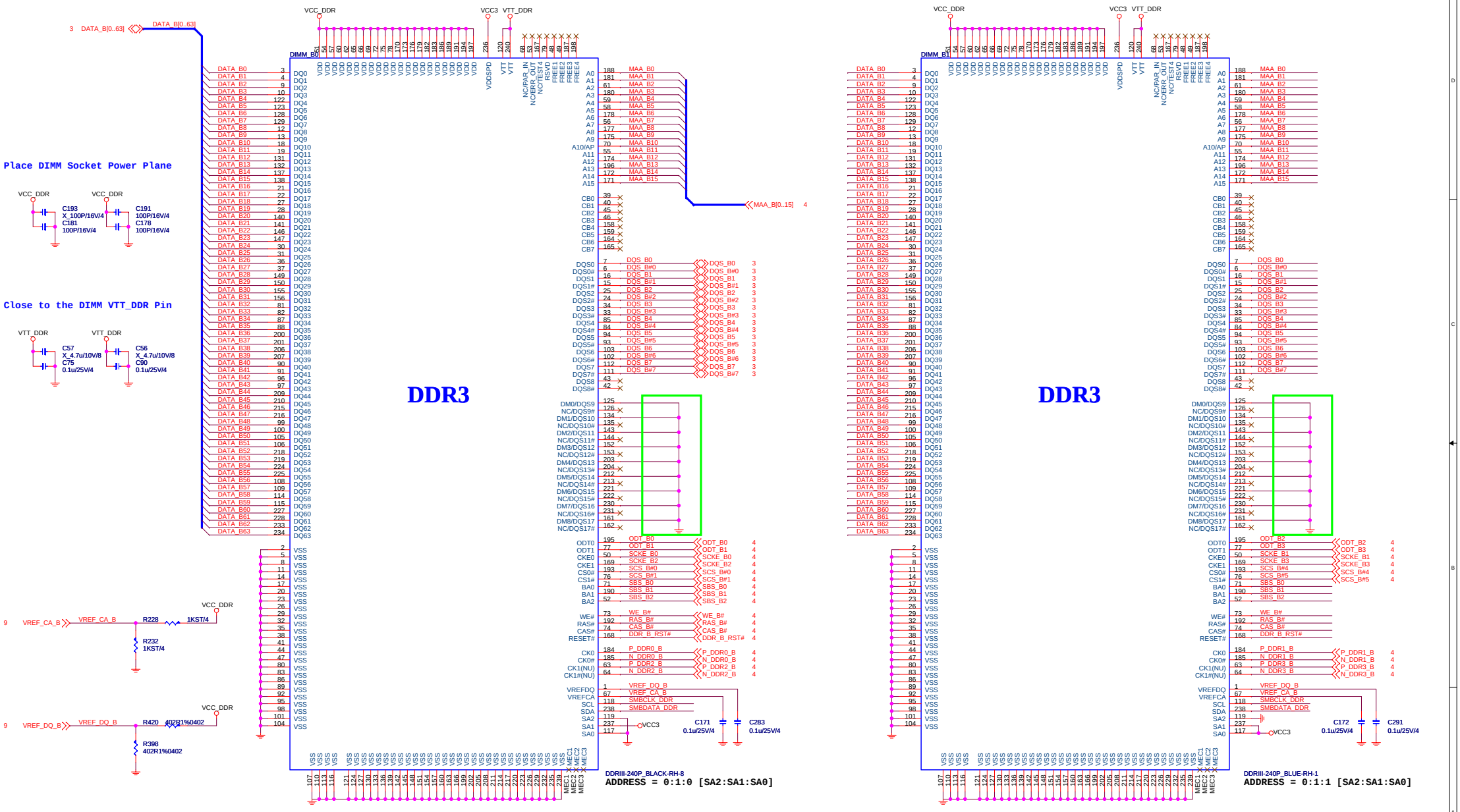
DIMM3 / CHANNEL B0

DIMM4 / CHANNEL B1



Vref-DQ : Reference voltage for DQ0–DQ63, CB0–CB7 and PAR_IN. When in single ended mode used for DQS0–DQS7.
Vref-CA : Reference voltage for A0-A15, BA0–BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.
RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

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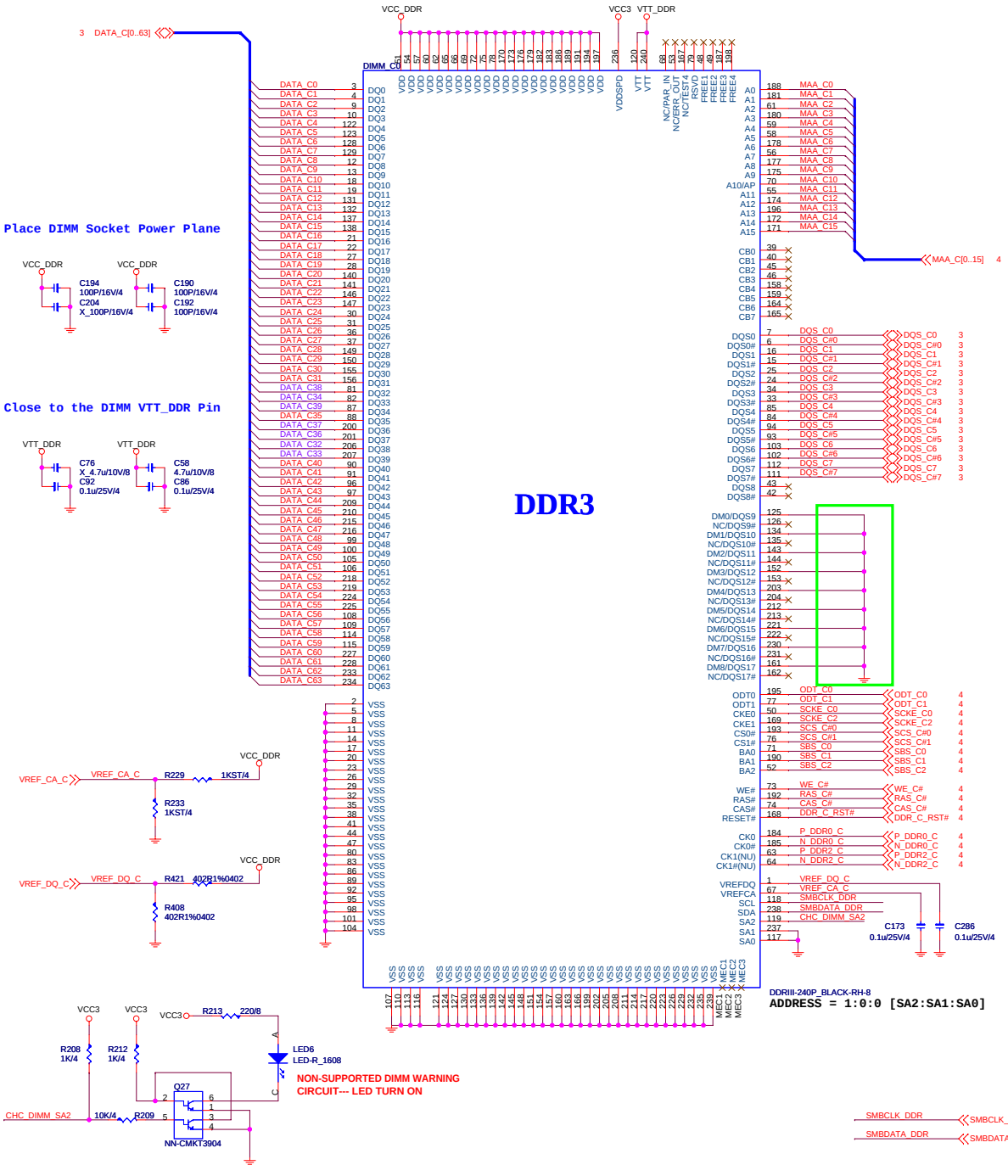
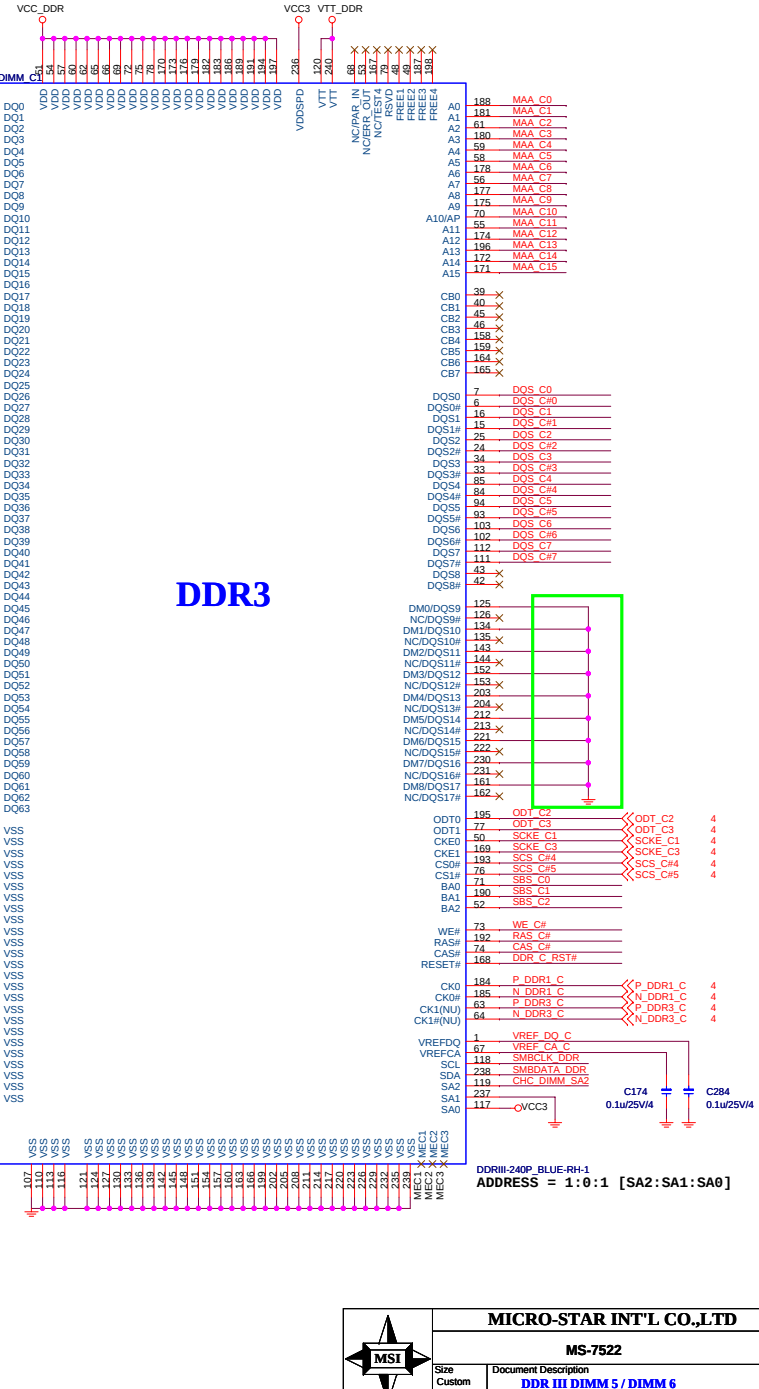
DIMM5 / CHANNEL C0



DIMM6 / CHANNEL C1



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Size: Custom	Document Description: DDR III DIMM 5 / DIMM 6 — Rev: 2.0
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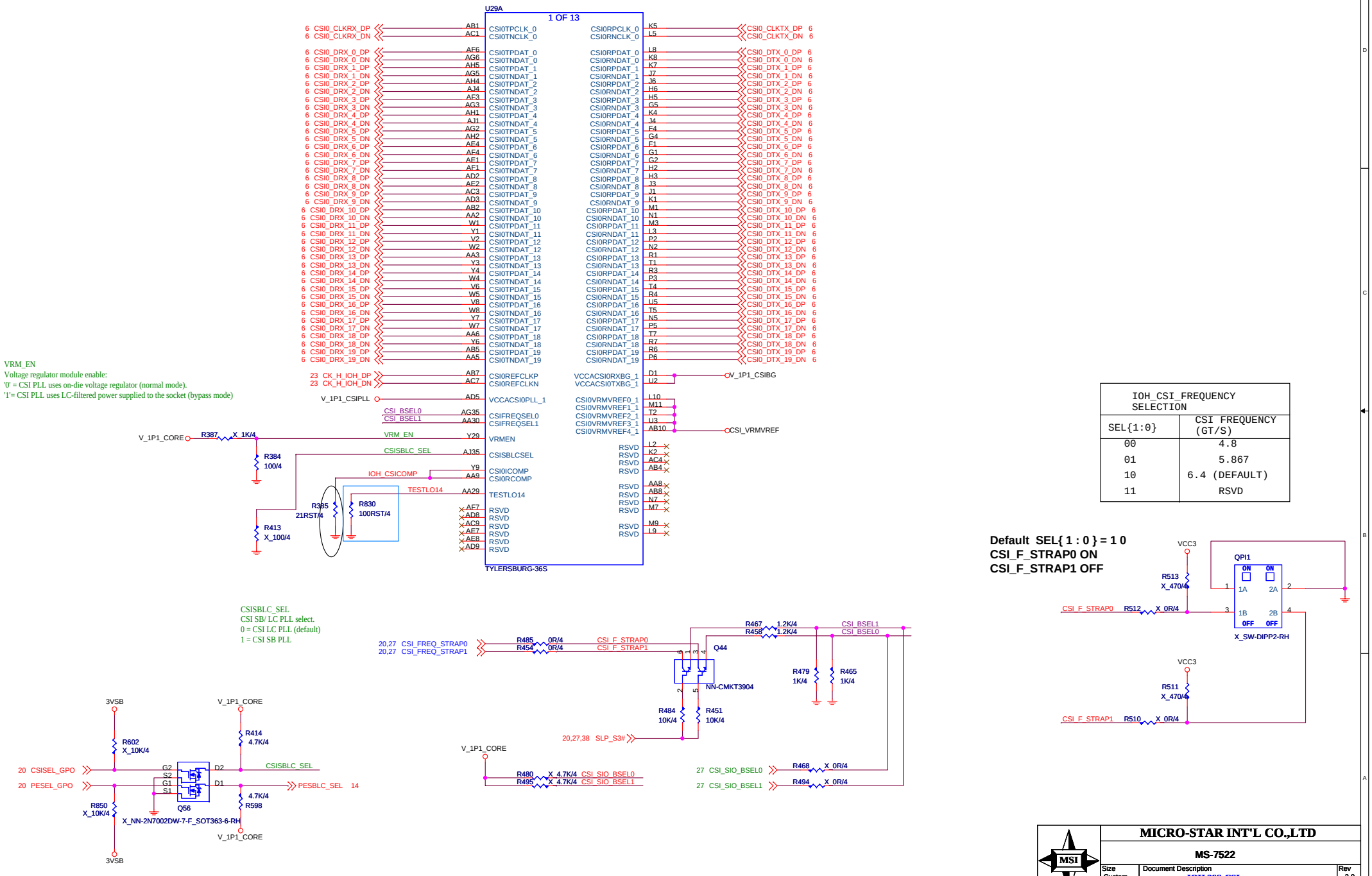
U29A
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TYLERSBURG-36S
VRM_EN
Voltage regulator module enable:
'0' = CSI PLL uses on-die voltage regulator (normal mode).
'1'= CSI PLL uses LC-filtered power supplied to the socket (bypass mode)
CSISBLC_SEL
CSI SB/ LC PLL select.
0 = CSI LC PLL (default)
1 = CSI SB PLL
IOH_CSI_FREQUENCY SELECTION
SEL{1:0}
CSI FREQUENCY (GT/S)
00 4.8
01 5.867
10 6.4 (DEFAULT)
11 RSVD
Default SEL{ 1 : 0 } = 1 0
CSI_F_STRAP0 ON
CSI_F_STRAP1 OFF
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IOH 36S-CSI
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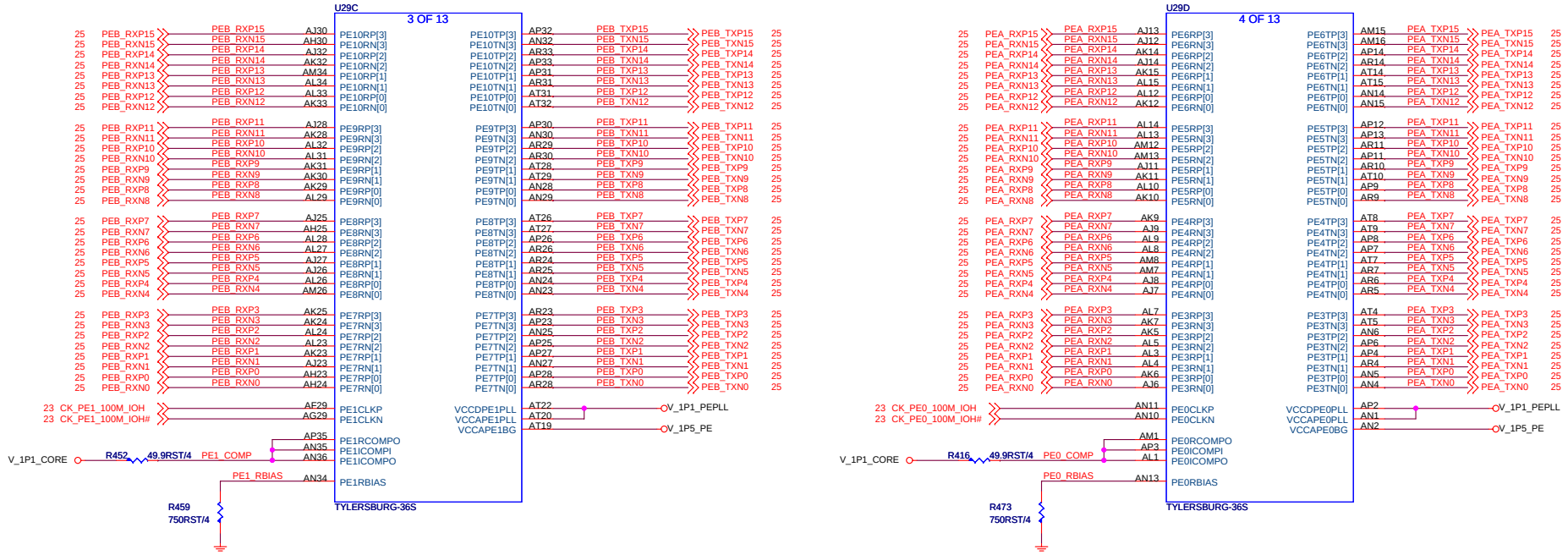

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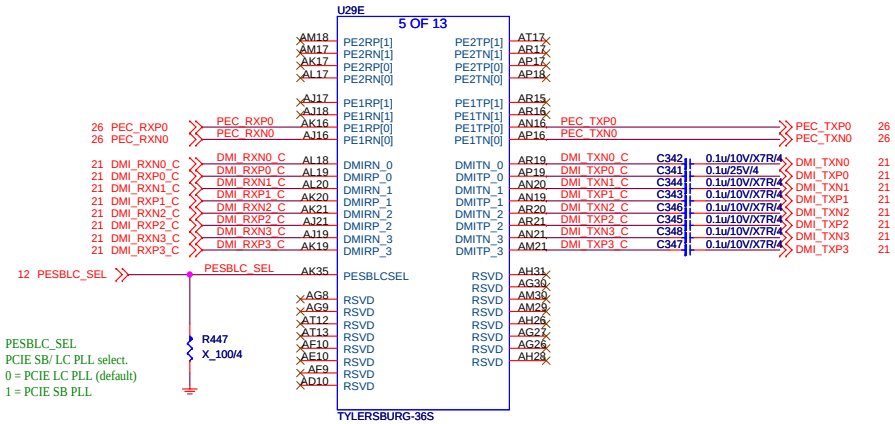

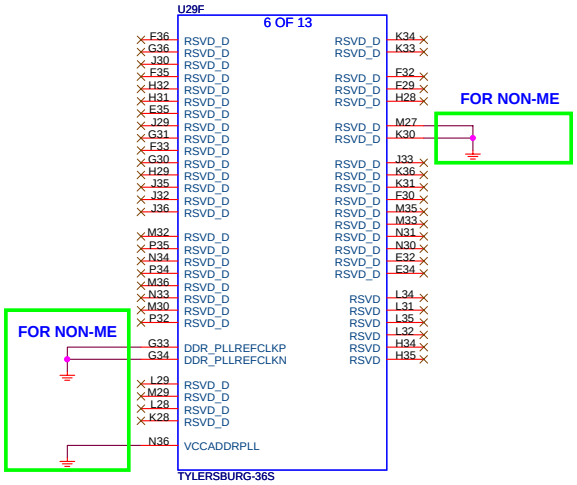

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FOR NON-ME

CL_CLK
CL_DATA
R824 10K/4
R823 10K/4

V_1P1_CORE
0.35V
R380 1KST/4
CL_VREF_IOH
R373 475RST/4
C264 0.1u/25V/4

CORERST# R299 2K/4 CL_RST#
3.3V level
1.1V level
R300 1K/4

SMBUSID
SMBus ID: Indicates SMBus ID bits [7:4].
'1' indicates an upper-address ID of 1110 (0xE).
'0' indicates an upperaddress ID of 1100 (0xC).

IOH SMBSCL/SMBSDA/SMBUSID not support yet

9,20,23,25,26,31,32,35,36,37,38,39,40,42,43 SMBCLK
9,20,23,25,26,31,32,35,36,37,38,39,40,42,43 SMBDATA
R837 X_0R/4 IOH_SMBSCL
R835 X_0R/4 IOH_SMBSDA

COREPLLPWRDET R334 0R/4
38,40 PWRGD_3V R335 X_0R/4 PLLPWRDET
5,27,38,39,40 ATX_PWR_OK R336 X_0R/4 0 ohm

PLLPWRDET R332 1K/4 AUXPWRGOOD_OP
X_2.2K
20,35,38 ICH_VRM_PGD R325 X_0R/4 0 ohm
C233 X_0.1u 1u/6.3V/4

U29G
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TYLERSBURG-36S

20 H_A20M# AC31 A20M#
20 H_FERR# AL36 FERR#
20 H_INIT# AE30 INIT#
20 H_INTR AB31 INTR
20 H_NMI AD32 NMI
20 IOH_H_SMI# AG32 SMI#
20 IOH_SYNC# AE27 LTRESET#

CL_CLK U34 CL_CLK
CL_DATA T34 CL_DATA
CL_RST# U32 CLRST#
T36 VREFCL
CL_VREF_IOH

PLLPWRDET C35 PLLPWRDET
AUXPWRGOOD C32 AUXPWRGOOD
COREPLLPWRDET AC28 COREPLLPWRDET
COREPWRGOOD D34 COREPWRGOOD
CORERST# D33 CORERST#
AL2 RESETO#

5 H_CPURST#

R400 0R/4 TBG_ITEST AE34 TESTLO9
19 TBG_SAFE TBG_SAFE AJ34 TESTLO5
19 IOH_ITPMEN IOH_ITPMEN R29 TESTHI3
T24 B34 VSS
R829 1K/4 ISCAN_MODE_TBG W27 TESTLO16
R396 1K/4 TESTLO11 AE34 TESTLO11
R365 1K/4 TESTLO17 V32 TESTLO17
R843 1K/4 TESTLO10 AF32 TESTLO10
R828 1K/4 EARLY_ISHIFT_TBG Y28 TESTLO15
R831 1K/4 TESTLO12 AC32 TESTLO12
R394 1K/4 TESTLO8 AF35 TESTLO8
R832 1K/4 TESTLO13 AB30 TESTLO13

IOH_XDP_PRESENT_GTL U28 TESTHI2
19 IOH_DFX_1 IOH_DFX_1 T27 TESTLO18
19 IOH_DFX_2 IOH_DFX_2 U29 RSVD_D
19 IOH_DFX_3 IOH_DFX_3 T31 RSVD_D

AD27 ERR_N_0
AF28 ERR_N_1
AE28 ERR_N_2

19 NODEID_2 NODEID_2 AH34 TESTLO6
19 NODEID_3 NODEID_3 AG33 RSVD
19 NODEID_4 NODEID_4 AH33 TESTLO7

VCC3
R833 10K/4 PEHPSCL AB28 PEHPSCL
R838 10K/4 PEHPSDA AD30 PEHPSDA
IOH_SMBSCL AB27 SMBSCL
V_1P1_CORE
R840 10K/4 IOH_SMBSDA AD29 SMBSDA
R841 X_1K/4 SMBUSID AE31 SMBUSID

R405 2.49KST/4 TSIREF AJ3 TSIREF
R472 1K/4 TESTLO1 AR12 TESTLO1
RN9 1K/4/8P4R TESTLO2 AN9 TESTLO2
TESTLO3 AN8 TESTLO3
TESTLO4 AM6 TESTLO4
AM3 RSVD
AM5 RSVD
27 IOH_TMERMDA AM2 TSDA
27 IOH_TMERMDC AK3 TSDC
AD26 THERMALERT_N
AC26 THERMTRIP_N

T12 TEST0 A2 TEST[0]
T14 TEST1 A36 TEST[1]
T13 TEST2 B1 TEST[2]
T15 TEST3 AT1 TEST[3]
T16 TEST4 AT36 TEST[4]

XDPCLK1_XP AH36 CK_IOH_XDP_DP R404 20RST/4 CK_XDP_DP 43
XDPCLK1_XN AG36 CK_IOH_XDP_DN R401 20RST/4 CK_XDP_DN 43

XDPDQ_0 W33 XDP_DQ0 XDP_DQ0 43
XDPDQ_1 W36 XDP_DQ1 XDP_DQ1 43
XDPDQ_2 V33 XDP_DQ2 XDP_DQ2 43
XDPDQ_3 V36 XDP_DQ3 XDP_DQ3 43
XDPDQ_4 Y34 XDP_DQ4 XDP_DQ4 43
XDPDQ_5 V35 XDP_DQ5 XDP_DQ5 43
XDPDQ_6 W34 XDP_DQ6 XDP_DQ6 43
XDPDQ_7 U35 XDP_DQ7 XDP_DQ7 43
XDPDQ_8 AD36 XDP_DQ8 XDP_DQ8 43
XDPDQ_9 AB33 XDP_DQ9 XDP_DQ9 43
XDPDQ_10 AA36 XDP_DQ10 XDP_DQ10 43
XDPDQ_11 AA33 XDP_DQ11 XDP_DQ11 43
XDPDQ_12 AE36 XDP_DQ12 XDP_DQ12 43
XDPDQ_13 AC34 XDP_DQ13 XDP_DQ13 43
XDPDQ_14 AB36 XDP_DQ14 XDP_DQ14 43
XDPDQ_15 AB34 XDP_DQ15 XDP_DQ15 43
XDPDQSN_0 Y35 XDP_DQS0_N XDP_DQS0_N 43
XDPDQSP_0 AA35 XDP_DQS0_P XDP_DQS0_P 43
XDPDQSN_1 AC35 XDP_DQS1_N XDP_DQS1_N 43
XDPDQSP_1 AD35 XDP_DQS1_P XDP_DQS1_P 43
XDPRDYACK_N Y31 XDP_RDYACK# XDP_RDYACK# 43
XDPRDYREQ_N W31 XDP_RDYREQ# XDP_RDYREQ# 43
EXTSYSTRIG AK36 EXTSYSTRIG_TBG_AK36 43

TCK T33 IOH_TCK IOH_TCK 43
TDI V26 IOH_TDI IOH_TDI 43
TDO V30 IOH_TDO IOH_TDO 43
TMS U31 IOH_TMS IOH_TMS 43
TRST# R30 IOH_TRST# IOH_TRST# 43

PEWIDTH[0] R33 PEWIDTH0 PEWIDTH0 19
PEWIDTH[1] T30 PEWIDTH1 PEWIDTH1 19
PEWIDTH[2] R36 PEWIDTH2 PEWIDTH2 19
PEWIDTH[3] N28 PEWIDTH3 PEWIDTH3 19
PEWIDTH[4] T28 PEWIDTH4 PEWIDTH4 19
PEWIDTH[5] P28 PEWIDTH5 PEWIDTH5 19
TESTHI1 P29 TESTHI1 TESTHI1 19
LEGACYIOH R32 LEGACYIOH LEGACYIOH 19
TESTLO19 R35 TESTLO19 TESTLO19 19

TESTLO21 AD33 TESTLO21 R389 10K/4
TESTLO22 C33 TESTLO22 R337 10K/4
TESTLO23 AC29 TESTLO23 R834 10K/4
TESTLO24 AA26 TESTLO24 R836 10K/4
TESTLO25 AE33 TESTLO25 R839 10K/4
TESTLO26 D36 TESTLO26 R838 10K/4
SINGLE_IOH P31 SINGLE_IOH SINGLE_IOH 19
CL_CLK_SRC N27 CL_CLK_SRC CL_CLK_SRC 19

RSVD W28
RSVD AF31 BMCINIT R845 100RST/4
RMIICLK G28 RMIICLK
RMIICLKREFOUT J26
RMIICRSDV A31 RMIICRSDV
RMIIMDC D30
RMIIMDIO D31
RMIIRXD[0] B32 RMIIRXD0
RMIIRXD[1] E29 RMIIRXD1
RMIITXD[0] E31
RMIITXD[1] J27
RMIITXEN G27

BMCINIT
BMC initialized.
0 = CSI link does not stall.
1= CSI link stalls after physical INIT waits for BMC to set CSR..

FOR NON-ME
RN7
RMIICRSDV
RMIIRXD0
RMIIRXD1
RMIICLK
10K/4/8P4R

VCC3
R437 1K/4
VCC5
R403 8.2K/4
Q41 NN-CMKT3904
C281 X_1u/6.3V/4
COREPLLPWRDET_OP
R396 100K/4
38,40 PWRGD_3V R391 X_10K/4
20,35,38 ICH_VRM_PGD R397 10K/4
C282 1u/6.3V/4
R390 X_0R/4 PWRGD_3V 38,40

VCC3 R388 10K/4 Q39 NN-CMKT3904
20,27 PLTRST# R377 10K/4
ICH GPIO56
20 IOH_CSI_RST#
3VSB R392 10K/4
VCC3 ?

IOH_CSI_RST#=0 , CONTRLL BY PLTRST#
IOH_CSI_RST#=1 , COREPLLPWRDET FOLLOW ICH_VRM_PGD

COREPLLPWRDET_OP
R367 2.2K/4
VCC3 R346 X_1K/4 Q36 X_NN-CMKT3904
5,20 H_PWRGD R341 X_10K/4
C245 1u/6.3V/4
R340 100K/4
COREPWRGOOD_OP

3VSB
R331 X_0R/4
U28 SN74AHC1G14DBV_SC70-5
U30 SN74AHC1G14DBV_SC70-5
AUXPWRGOOD_OP
AUXPGD_N
AUXPWRGOOD 20

R372 X_0R/4
U34 SN74AHC1G14DBV_SC70-5
U33 SN74AHC1G14DBV_SC70-5
COREPLLPWRDET_OP
PWRDET_N
COREPLLPWRDET

R352 X_0R/4
U32 SN74AHC1G14DBV_SC70-5
U31 SN74AHC1G14DBV_SC70-5
COREPWRGOOD_OP
COREPGD_N
COREPWRGOOD

C265 1u/6.3V/4

3VSB
spec only 2ms?
20,27 PLTRST#
U24 SN74AHC1G14DBV_SC70-5
R298 4.99KST/4
C216 1u/6.3V/4/X5R
U26 SN74AHC1G14DBV_SC70-5
CORERST#

5,20 H_PWRGD R342 X_1K/4 PRI_PWRGD_XDP 43
5 H_CPURST# R424 X_1K/4 FPGA_H_CPURST# 43
V_1P1_CORE R436 1K/4 EXTSYSTRIG_TBG_AK36 43
V_1P1_CORE R371 51/4 IOH_XDP_PRESENT_GTL

V_1P1_CORE
IOH_TDI R353 51/4
IOH_TDO R366 51/4
IOH_TMS R359 51/4
IOH_TCK R825 51/4
IOH_TRST# R358 51/4

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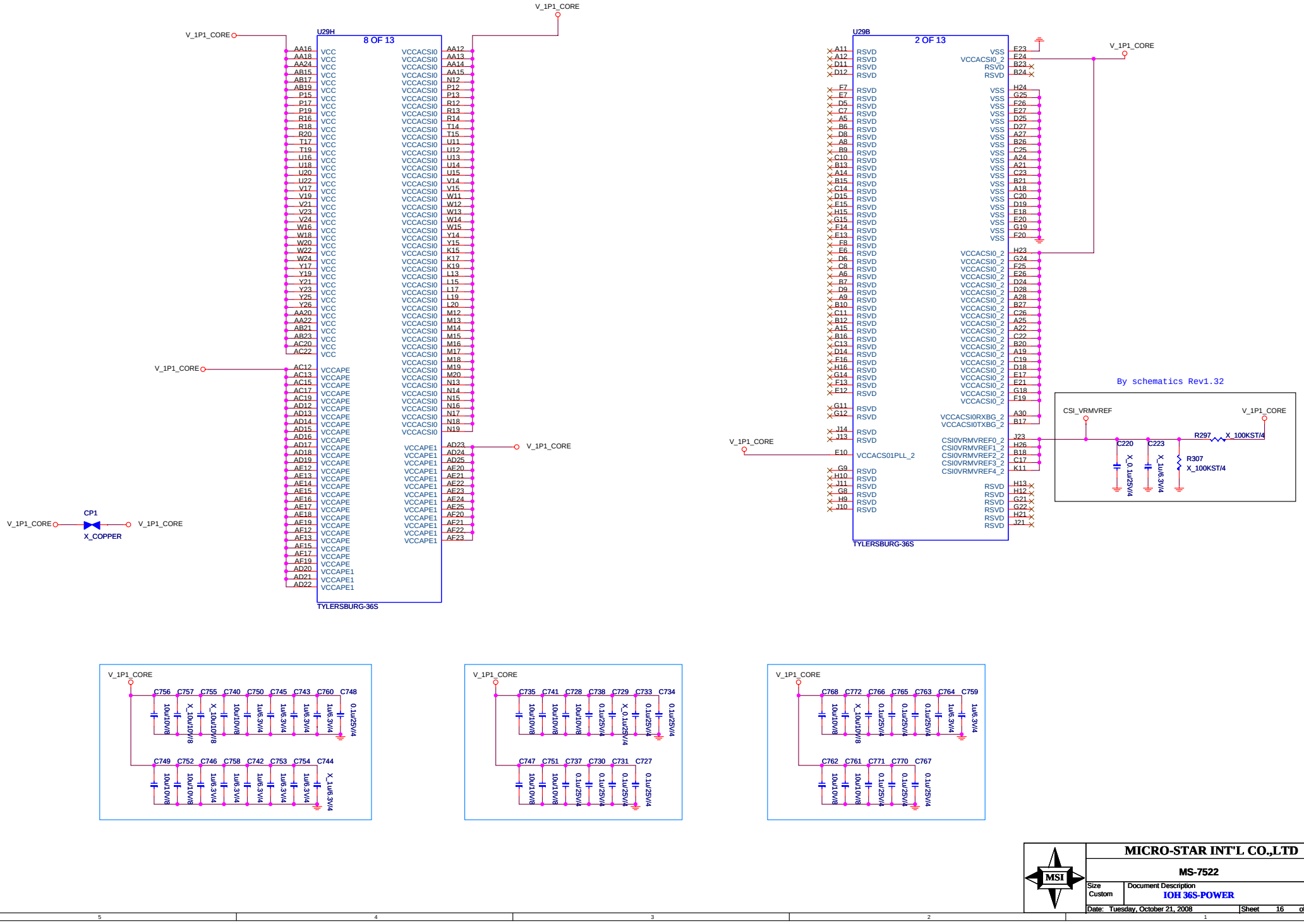

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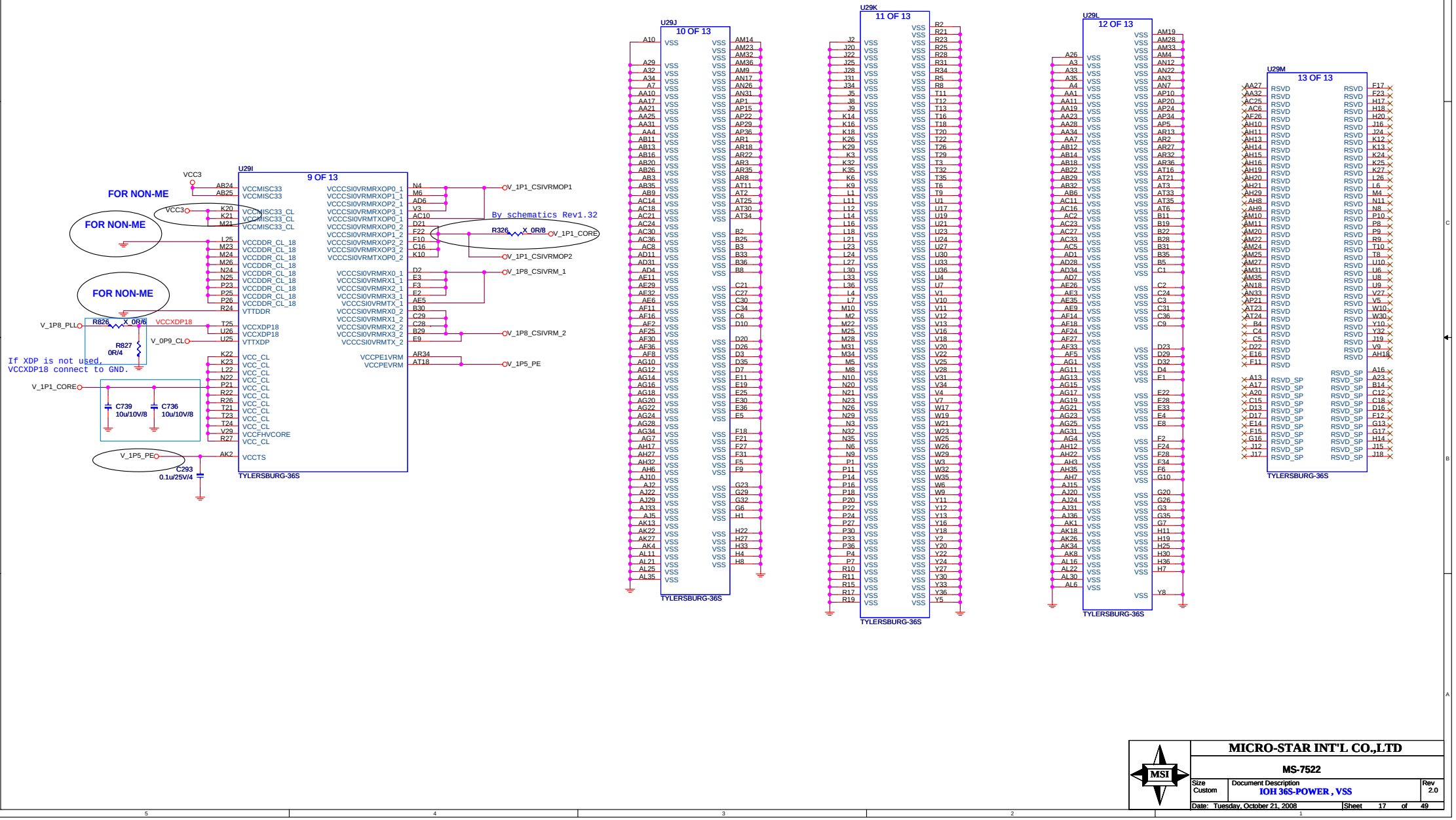

MICRO-STAR INT'L CO.,LTD		
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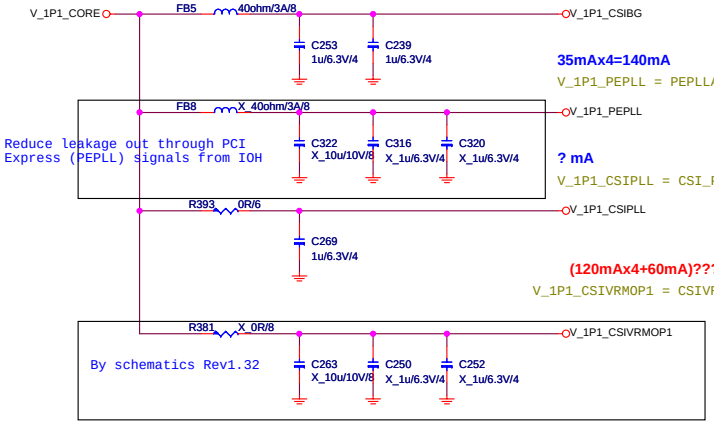
Size: Custom	Document Description: IOH 36S-POWER , VSS	Rev: 2.0
Date: Tuesday, October 21, 2008	Sheet 17 of 49	

V_1P1_CORE REPLACE WITH V_1P1_VCCA

0.7A???



10mAx2=20mA

V_1P1_CSIBG = CSIBG_RX+CSIBG_TX

35mAx4=140mA

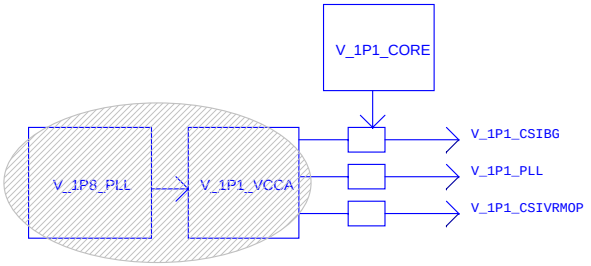
V_1P1_PEPLL = PEPLLA+PEPLLD

? mA

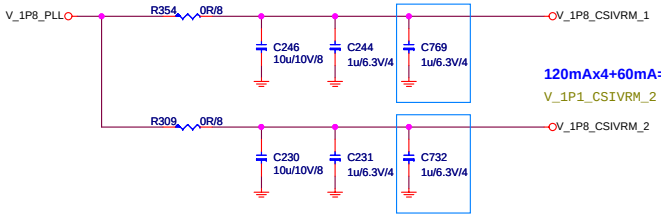
V_1P1_CSIPLL = CSI_PLL

(120mAx4+60mA)???=0.54A ??????

V_1P1_CSIVRMOP1 = CSIVRMOP_RX[1:4]+CSIVRMOP_TX1



1.08A

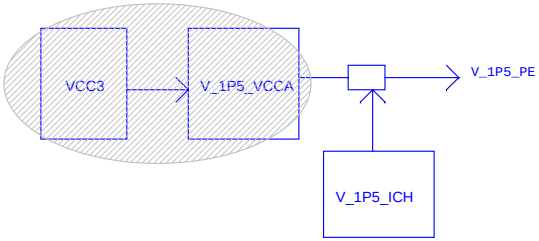


120mAx4+60mA=0.54A

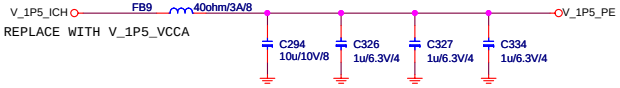
V_1P1_CSIVRM_1 = CSIVRM_RX_1+CSIVRM1_TX_1

120mAx4+60mA=0.54A

V_1P1_CSIVRM_2 = CSIVRM_RX_2+CSIVRM1_TX_2



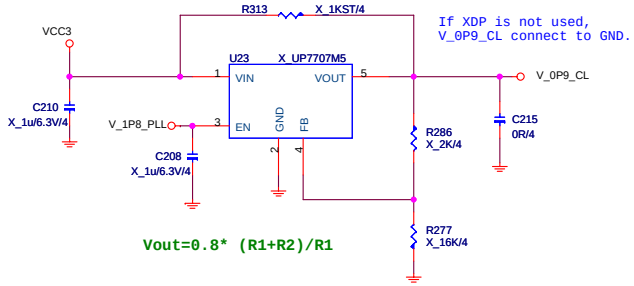
186.3mA+?



V_1P5_ICH REPLACE WITH V_1P5_VCCA

92mAx2+1.15mAx2+?=186.3mA+?

V_1P5_PE = PEVRM+PEBG0+PEBG1+VCCTS



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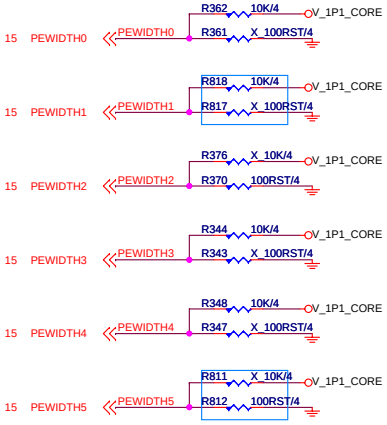
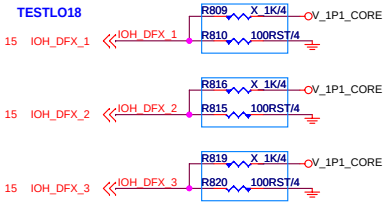
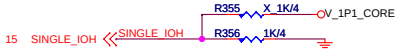
PEWIDTH0~5
PCIE Link Width Select
"110110" X2, X2, X16, X16
"111011" = 2x16
"101111" = 4x8
"011111" = Wait On Bios



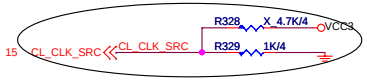
IOH_DFX_[2 , 3]
DDR frequency selection pins:
DDRFREQ[3:2] as DDR frequency selection defined as:
"00" = 133MHz input, 200MHz core
"01" = 100 MHz input, 200MHz core
"10" = RSVD
"11" = RSVD



SINGLE_IOH
Used for dual TBG IOH selection:
"0": IOH is not connected to another IOH on some CSI link (default)
"1": IOH is connected to another IOH on some CSI link

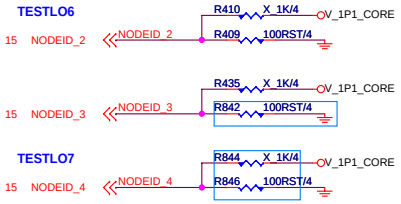


CL_CLK_SRC
Used for ME default clock source:
'1': PLL (default)
'0': Ring Oscillator (back-up)

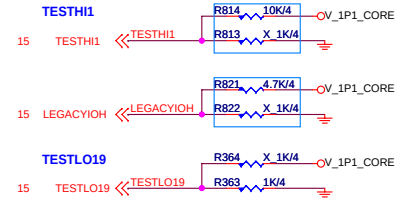


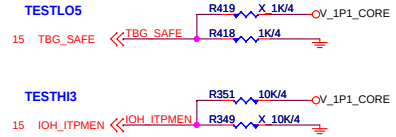
NON-ME FUNCTION ?

NODEID_3_TBG
For dual TBG IOH configuration,
it indicates which CSI port is connected
to the other IOH.
"0": CSI0
"1": CSI1



LEGACYIOH
Used to determine legacy or non-legacy selection:
"1": Legacy IOH
"0": Non-legacy IOH





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Custom	IOH 36S-STRAP	2.0

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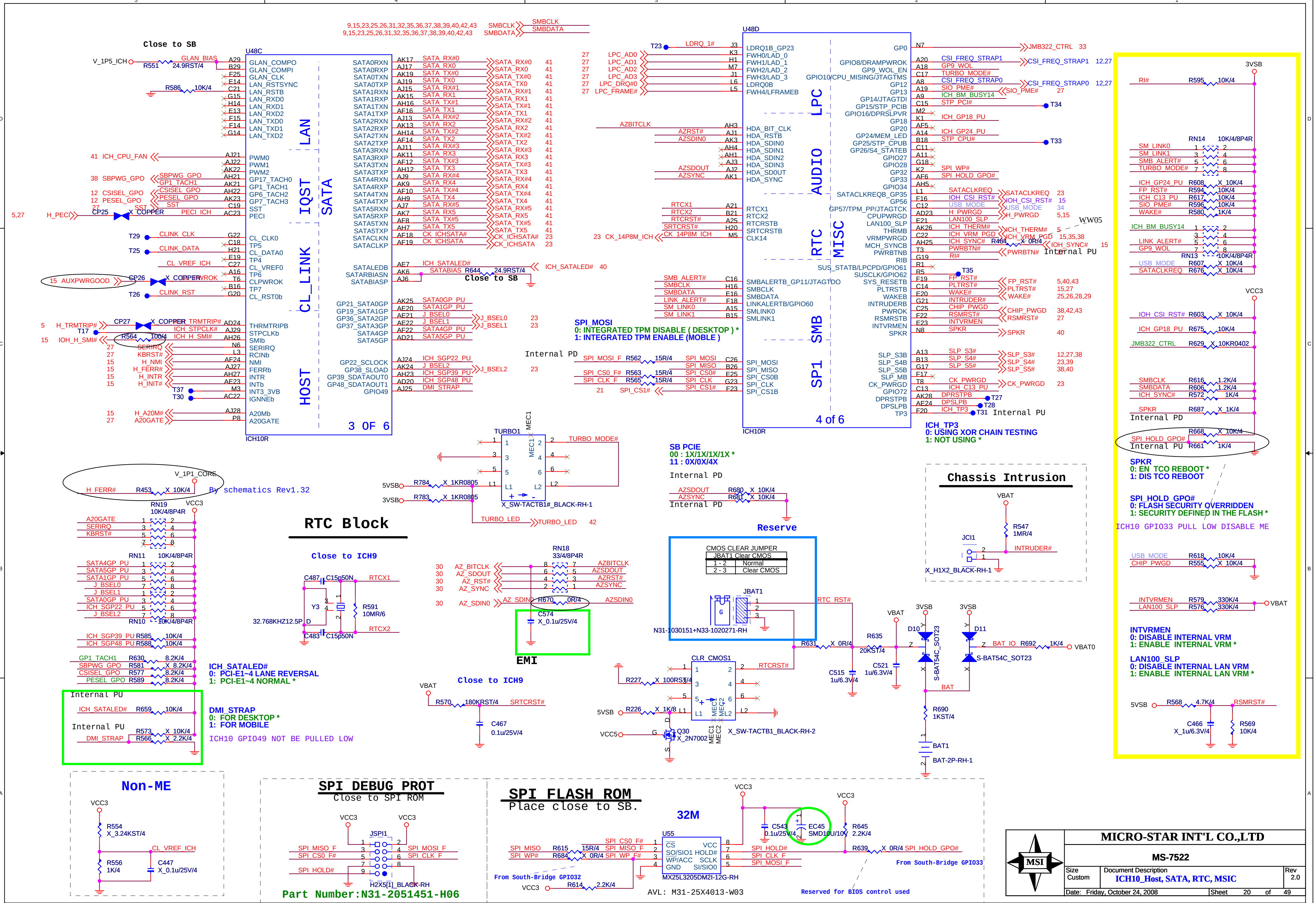

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MS-7522	
Size: Custom	Document Description: ICH10_Host, SATA, RTC, MSIC	Rev 2.0
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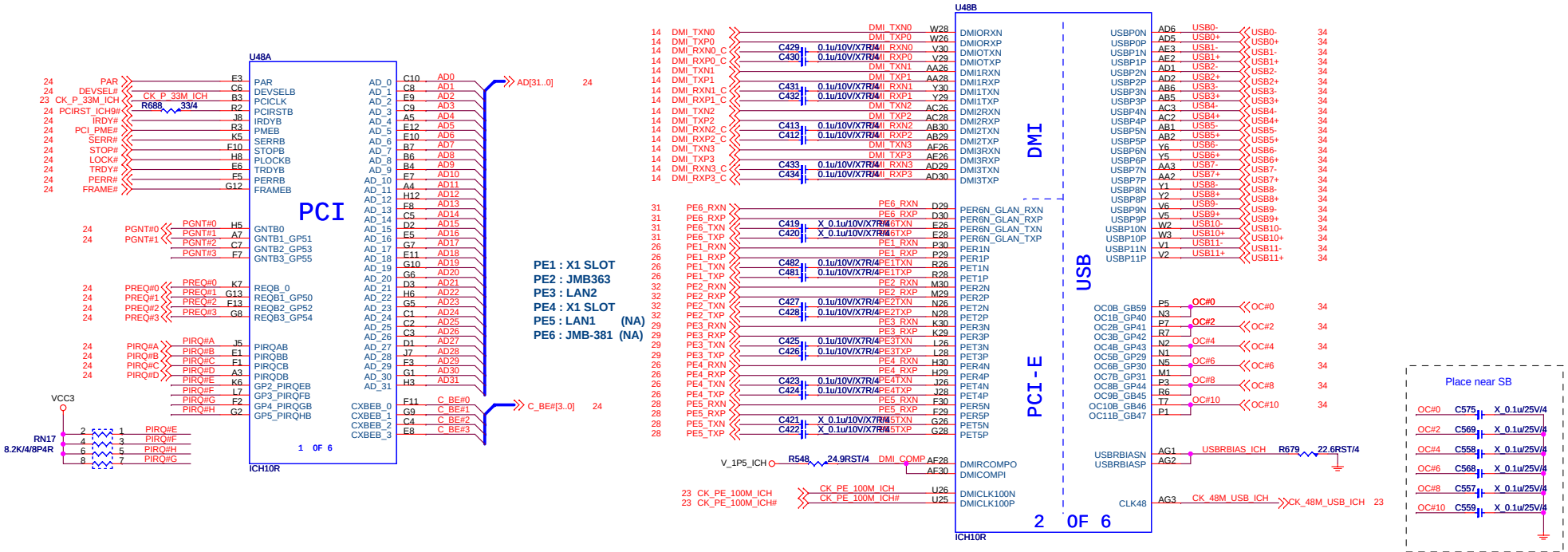
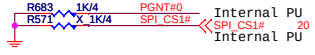
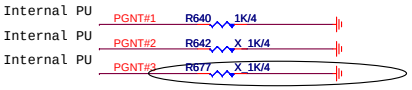


SB STRAPPING RESISTOR





BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
LPC	1	1
SPI	0	1
PCI	1	0

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)
GNT1	DC	AC	DMI AC/DC MODE 0 : AC 1 : DC

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Custom	ICH10_PCI, USB, DMI, PCIE x1	2.0

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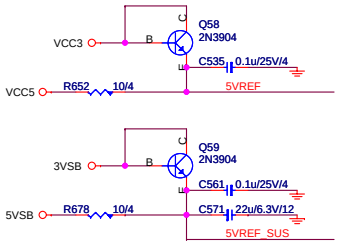
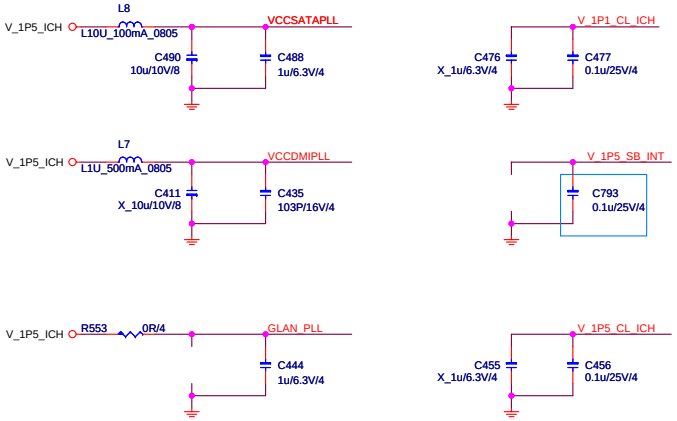
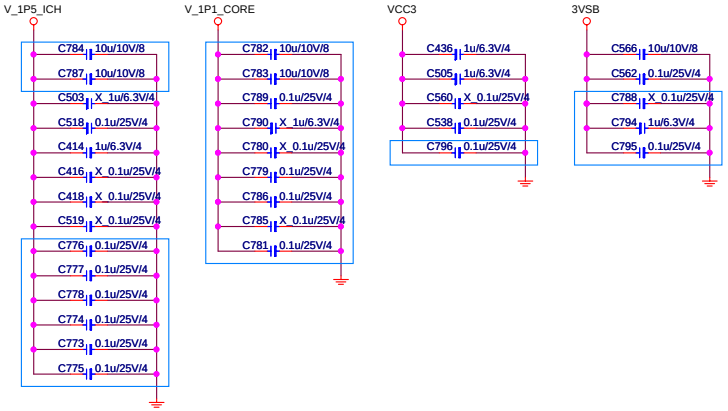
5VREF & 5VREF_SUS Sequencing Circuit

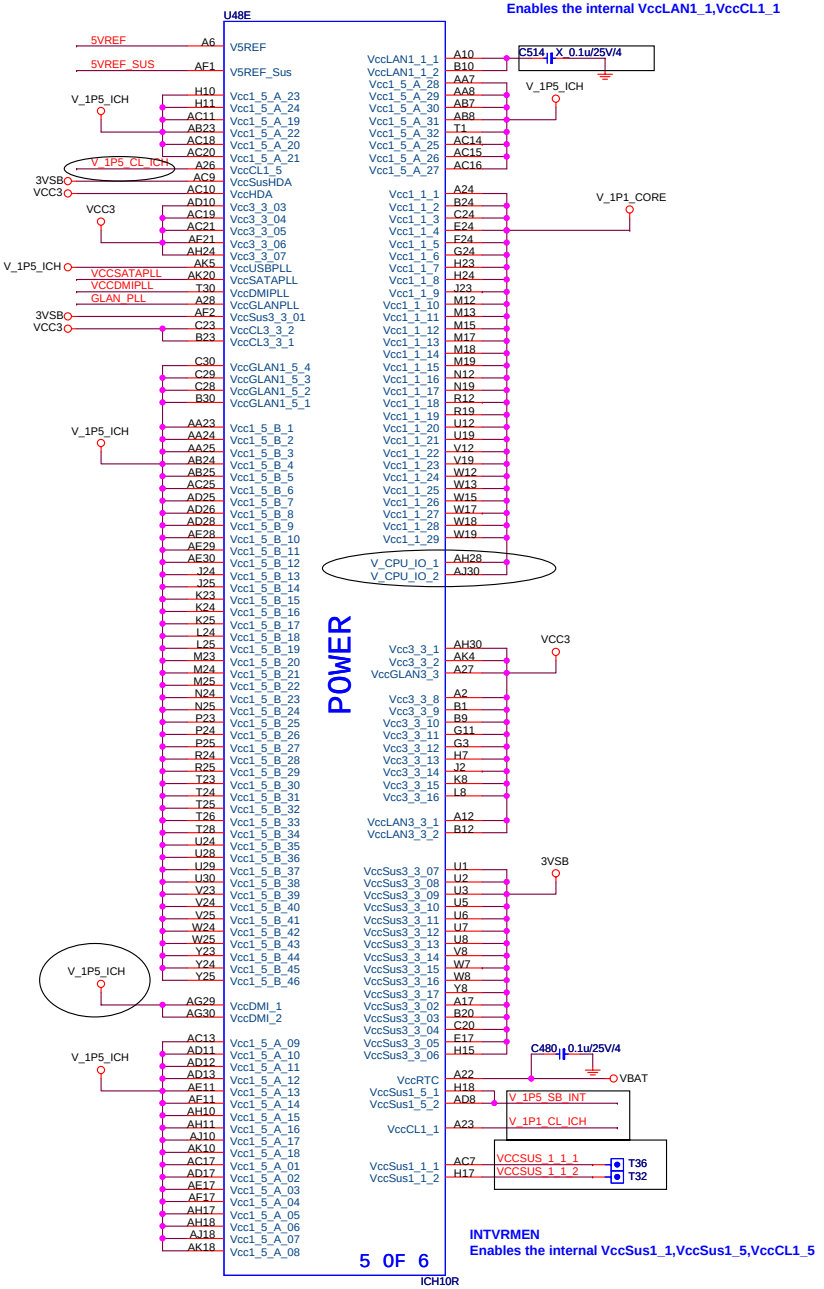


SB POWER

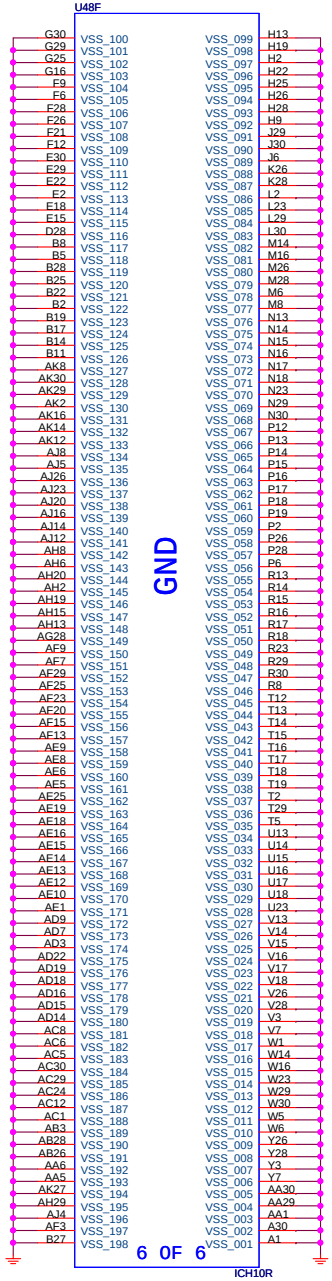




LAN100_SLP
Enables the internal VccLAN1_1,VccCL1_1



INTVRMEN
Enables the internal VccSus1_1,VccSus1_5,VccCL1_5



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Size: Custom	Document Description: ICH10_Power, GND
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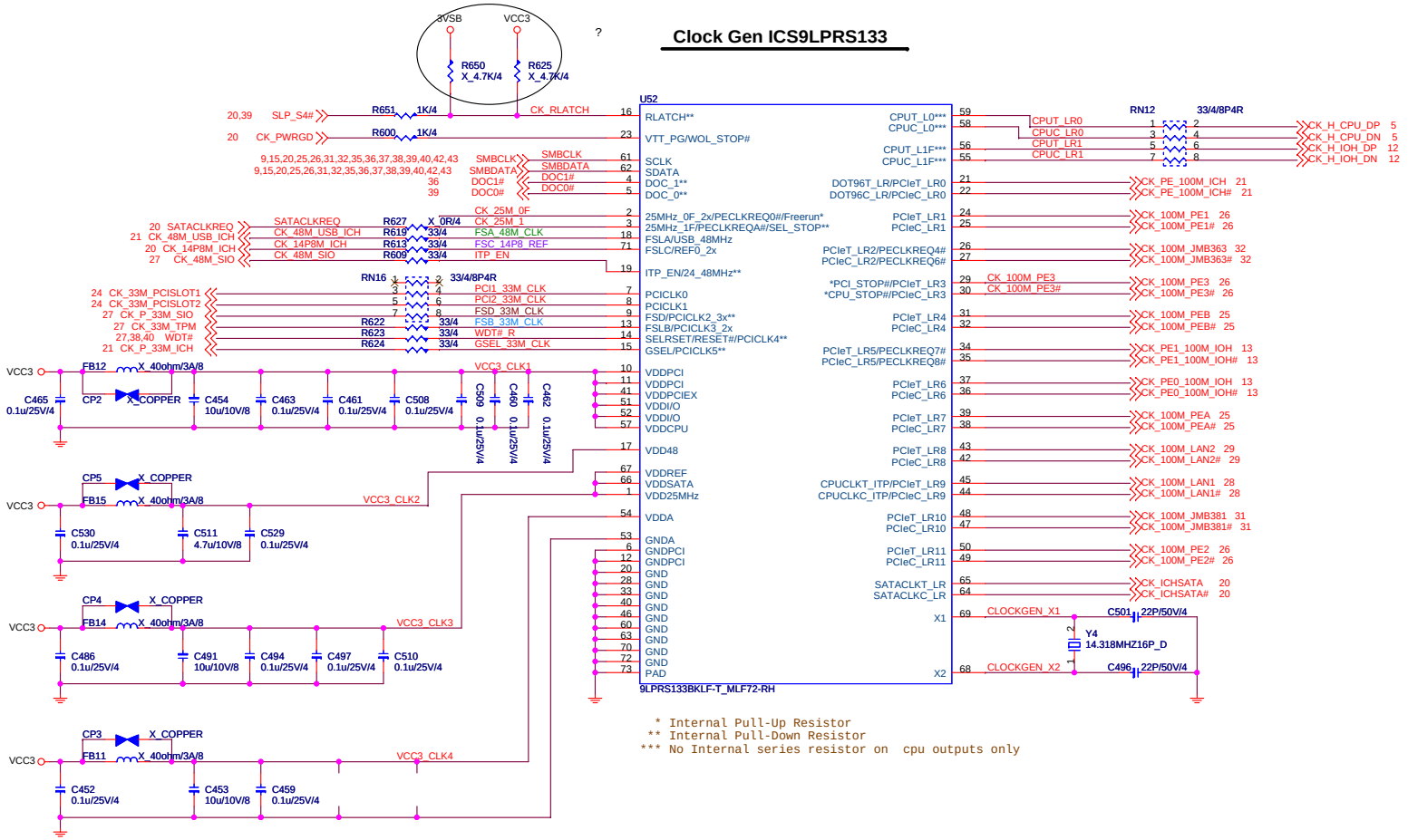
Clock Gen ICS9LPRS133



* Internal Pull-Up Resistor
** Internal Pull-Down Resistor
*** No Internal series resistor on cpu outputs only

CLOCK GEN STRAPING

0 : Pin21/22 100MHz *
1 : Pin21/22 96MHz
GSEL_33M_CLK R649 4.7K/4
Internal pull down

0 : PCICLK4
1 : RESET *
WDT#_R R648 4.7K/4 VCC3
Internal pull down

0 : PCIEX9 *
1 : CPU_ITP
ITP_EN R610 4.7K/4
Internal pull down

1 : 25MHz freerun function
CK_25M_0F R646 X_4.7K/4 VCC3
R636 X_4.7K/4
Internal pull up

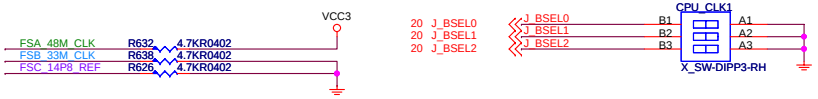
1 = Selects pin 29/30 to be PCI_STOP#/CPU_STOP#
0 = Selects pin 29/30 to be PCI_E CLK
CK_25M_1 R647 4.7K/4
Internal pull down

For ICS CPU/DIV SEL
0 : FSLD BIT3 =0 *
1 : FSLD BIT3 =1
FSD_33M_CLK R637 4.7K/4
Internal pull up

CK_14P8M_ICH C524 10P/50V/4
CK_33M_PCISLOT1 C525 X_10P/50V/4
CK_33M_PCISLOT2 C526 X_10P/50V/4
CK_P_33M_SIO C536 10P/50V/4
CK_P_33M_ICH C528 X_10P/50V/4
CK_33M_TPM C527 10P/50V/4
CK_48M_USB_ICH C507 X_10P/50V/4
CK_48M_SIO C502 X_10P/50V/4

Default 0 0 1 133 MHz
JB3 1-2 PIN 1
JB2 2-3 PIN 0
JB1 2-3 PIN 0

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz
0	0	1	133 MHz (default)
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	333 MHZ
1	0	1	100 MHZ
1	1	0	400 MHZ
1	1	1	200 MHZ



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Size: Custom	Document Description: Clock Gen ICS9LPRS133	Rev: 2.0
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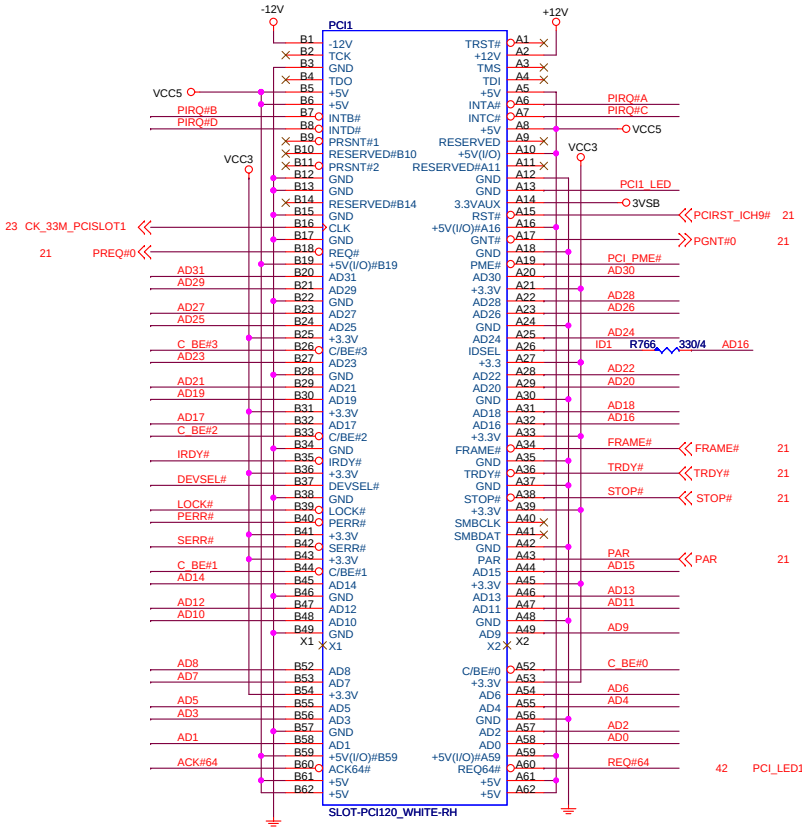
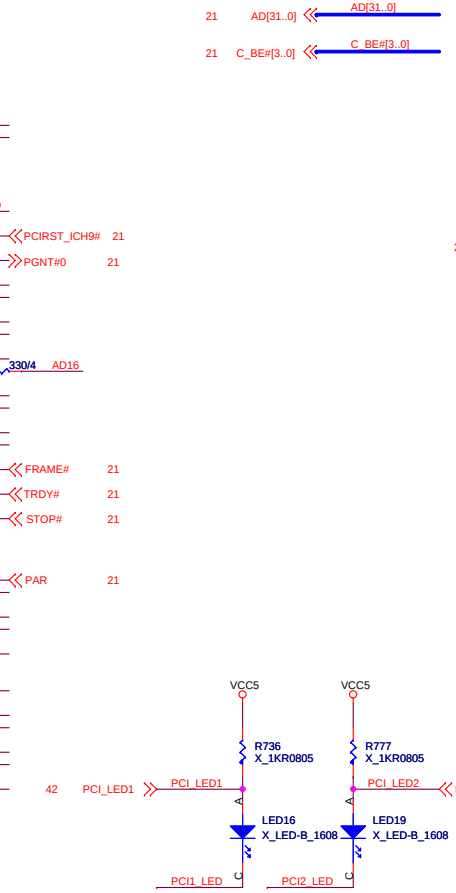
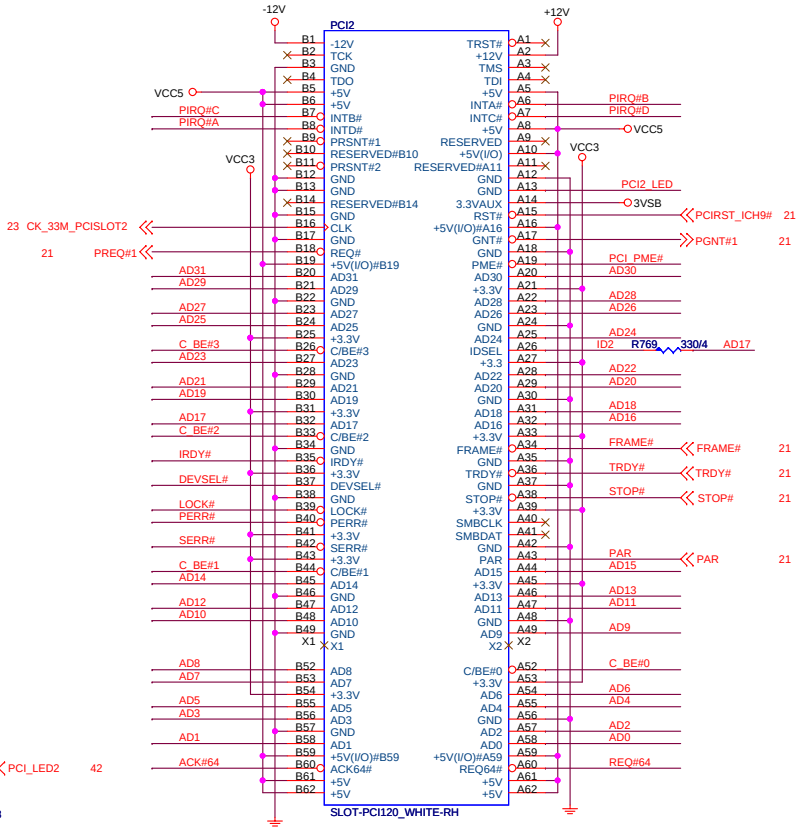
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD16
MASTER = PREQ#0
PGNT#0

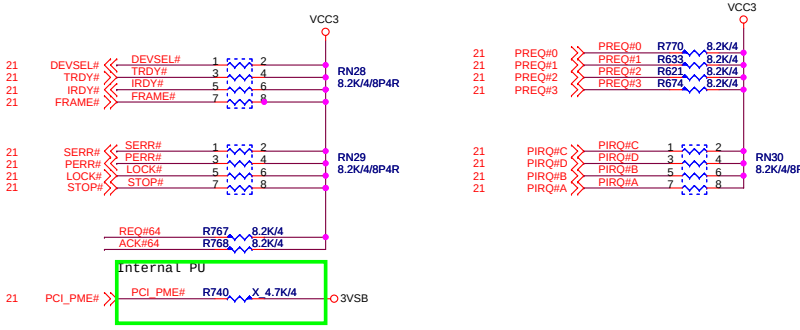


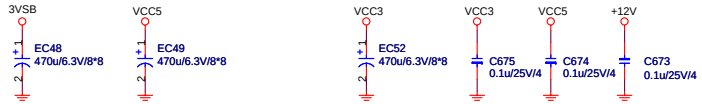
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD17
MASTER = PREQ#1
PGNT#1

PCI PULL-UP / DOWN RESISTORS





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Size: Custom	Document Description: PCI SLOT1 , 2	Rev: 2.0
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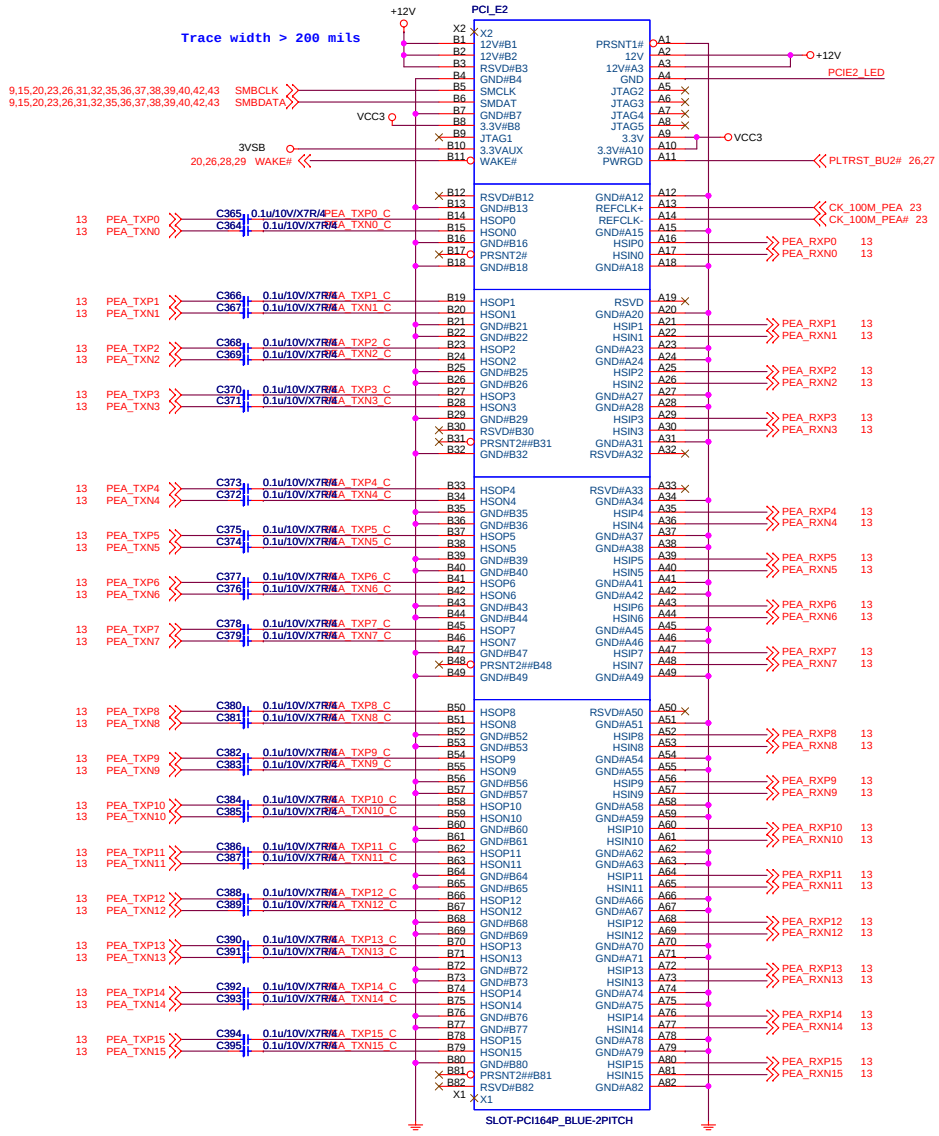
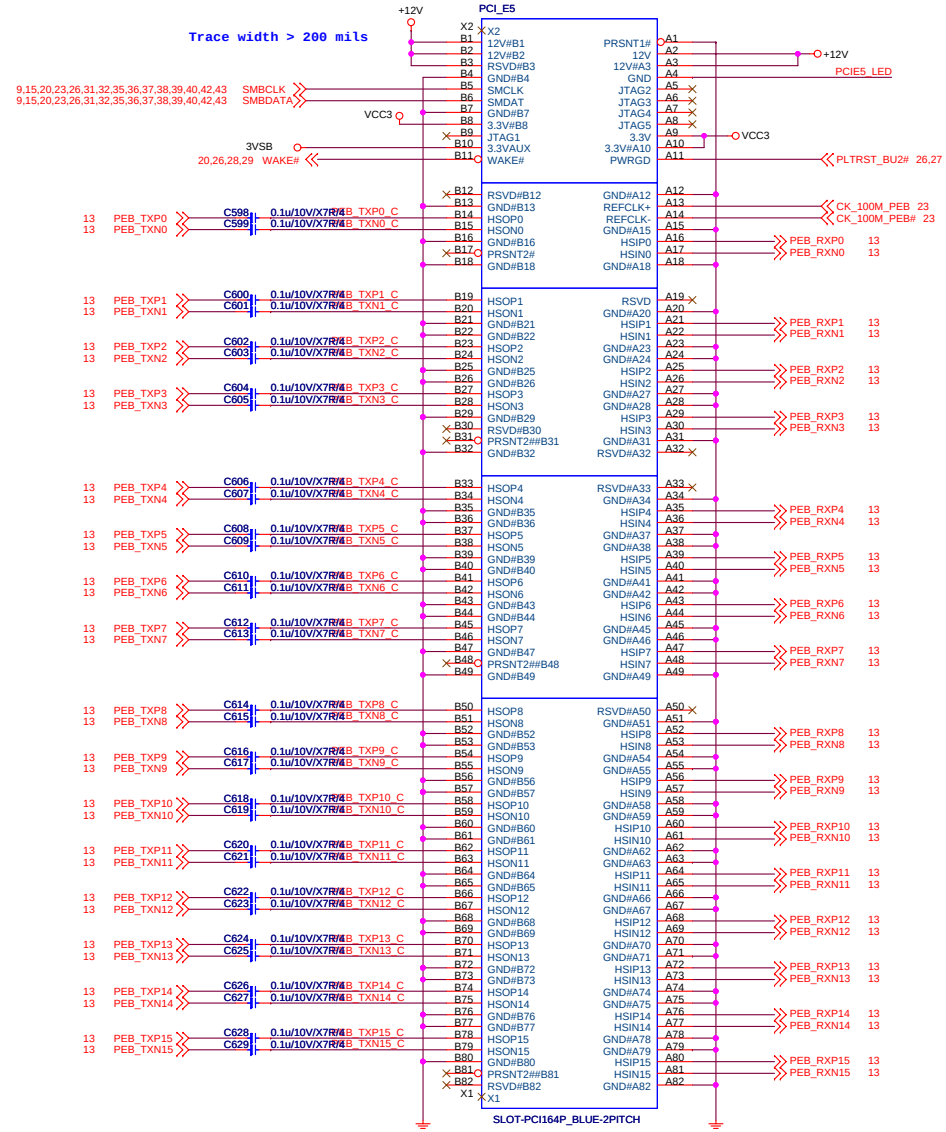
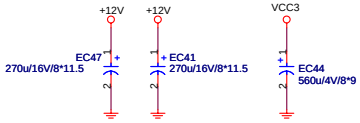
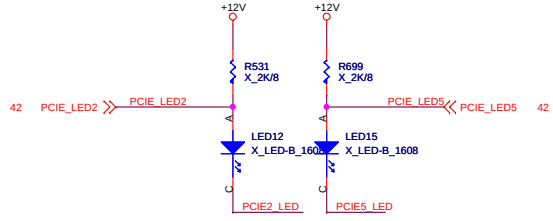
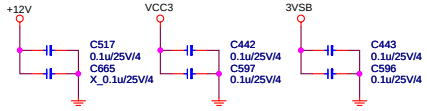
PCI_Express X16 SLOT1,2











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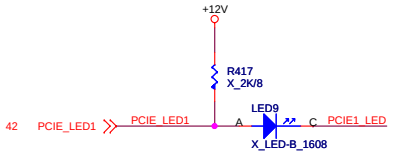
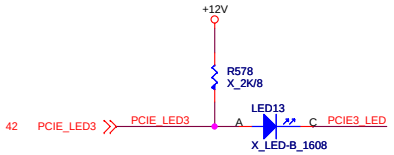
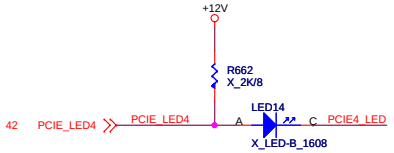
PCI_Express X1 Slot1 , 2 , 3

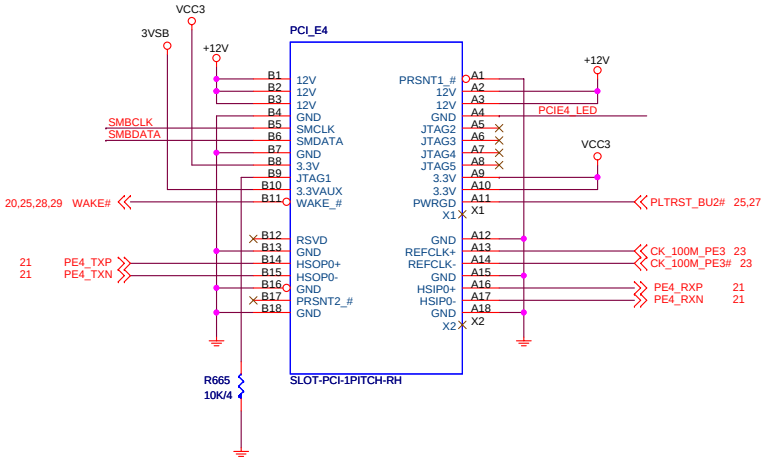
Trace width > 200mils

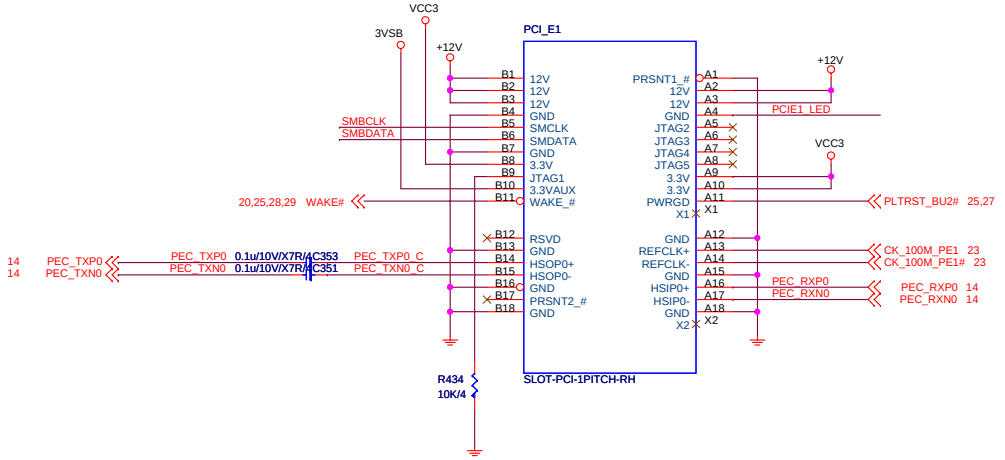
9,15,20,23,25,31,32,35,36,37,38,39,40,42,43 SMBCLK
9,15,20,23,25,31,32,35,36,37,38,39,40,42,43 SMBDATA

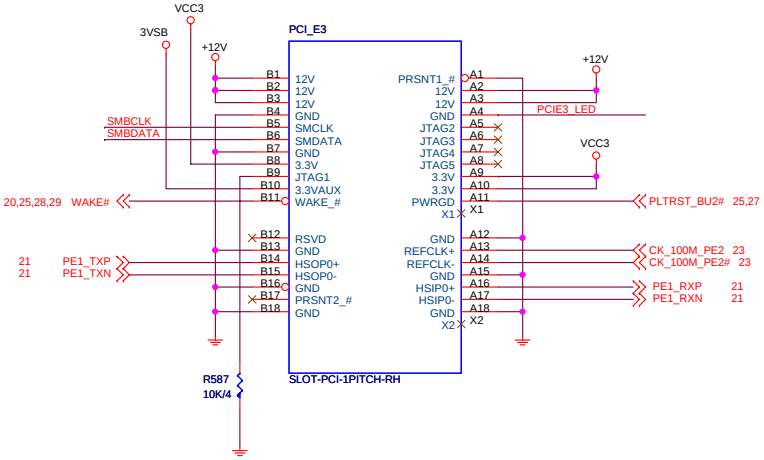


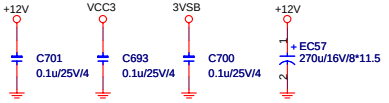












MSI	MICRO-STAR INT'L CO.,LTD	
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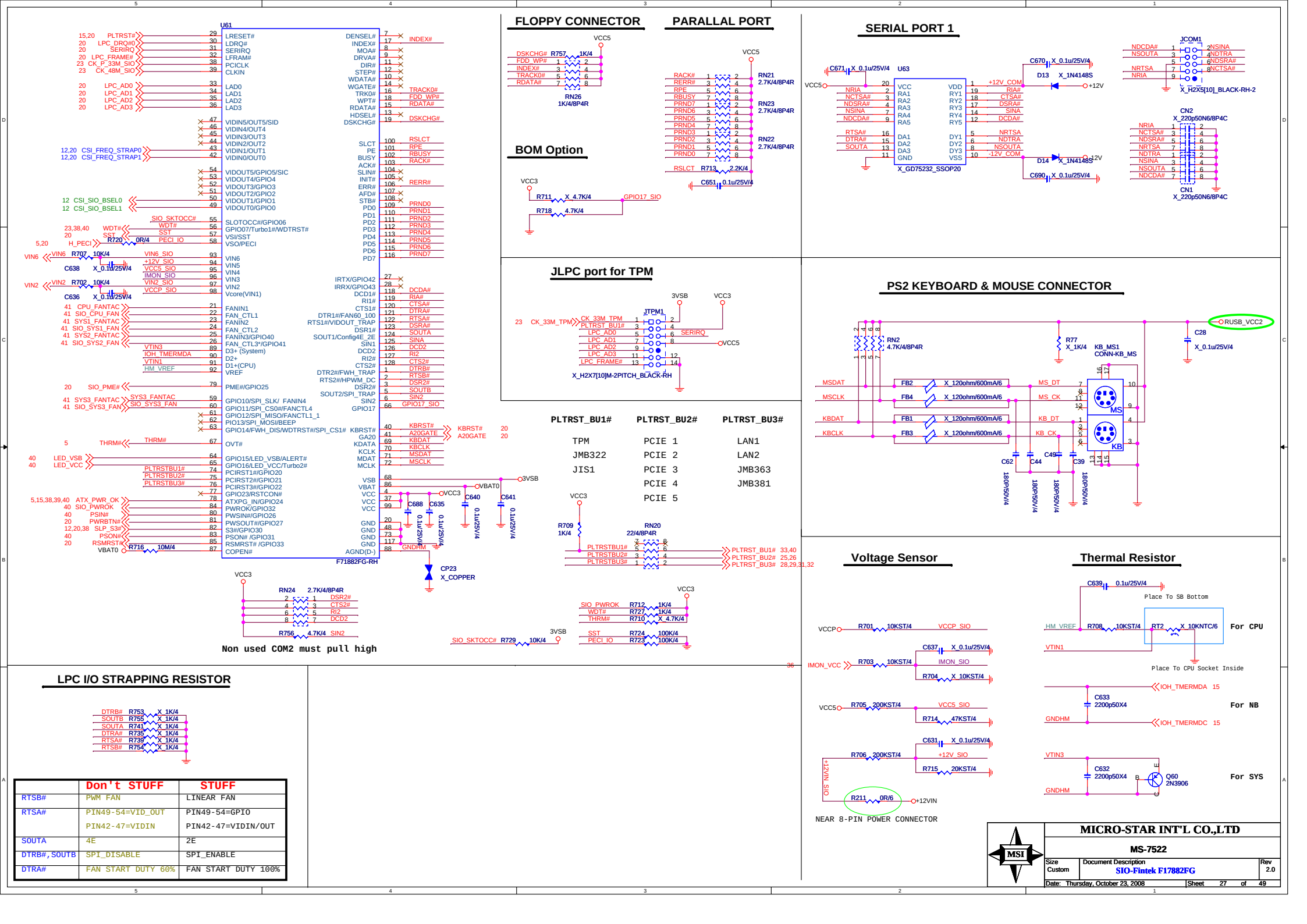
U61
F71882FG-RH
Non used COM2 must pull high
FLOPPY CONNECTOR
PARALLAL PORT
SERIAL PORT 1
BOM Option
JLPC port for TPM
PS2 KEYBOARD & MOUSE CONNECTOR
PLTRST_BU1#
PLTRST_BU2#
PLTRST_BU3#
TPM
JMB322
JIS1
PCIE 1
PCIE 2
PCIE 3
PCIE 4
PCIE 5
LAN1
LAN2
JMB363
JMB381
Voltage Sensor
Thermal Resistor
NEAR 8-PIN POWER CONNECTOR
Place To SB Bottom
Place To CPU Socket Inside
For CPU
For NB
For SYS
LPC I/O STRAPPING RESISTOR
Don't STUFF
STUFF
RTSB#
PWM FAN
LINEAR FAN
RTSA#
PIN49-54=VID_OUT
PIN42-47=VIDIN
PIN49-54=GPIO
PIN42-47=VIDIN/OUT
SOUTA
4E
2E
DTRB#,SOUTB
SPI_DISABLE
SPI_ENABLE
DTRA#
FAN START DUTY 60%
FAN START DUTY 100%
MICRO-STAR INT'L CO.,LTD
MS-7522
SIO-Fintek F71882FG
Rev 2.0
Date: Thursday, October 23, 2008
Sheet 27 of 49

For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21

LAN1_VDD33 — R522 X_0R/8 LAN1_VDDSR — C399 X_22u/6.3V/12 — C361 X_0.1u/25V/4

40mil width

C657 C346 near Pin63 200mil,C346 must be nearly Pin63

U49 PCI Express

21	PE5_TXP	23	HSIP	HSOP	29	PE5_RXP_C — C471 X_0.1u/10V/X7R/4 — PE5_RXP	21
21	PE5_TXN	24	HSIN	HSON	30	PE5_RXN_C — C472 X_0.1u/10V/X7R/4 — PE5_RXN	21
27,29,31,32	PLTRST_BU3#	20	PERSTB	LANWACKB	19	WAKE# — WAKE#	20,25,26,29
		36	ISOLATEB		
		26	REFCLK_P		
		27	REFCLK_N		
	CLK1_LANI	60	CKXTAL1		
	CLK1_LANO	61	CKXTAL2		
		64	RSET		
	LAN1_VDDSR	63	VDDSR		
	LAN1_SROUT12	1	SROUT12		
		16,37,46,53,2,59	VDD33		
		21,32,38,43,49,52,8,11,14,58	DVDD12		
		22,28	EVDD12		
		5	FB12		
		33,50,51	CLKREQB, IGPIO, OGPIO		
		62		ENSR	
		31,25,65		EGND, EGND, GNDPAD	

Clock | Transceiver Interface | EEPROM | LED

MDIP0	3	TR1_D0+	
MDIN0	4	TR1_D0-	
MDIP1	6	TR1_D1+	
MDIN1	7	TR1_D1-	
MDIP2	9	TR1_D2+	
MDIN2	10	TR1_D2-	
MDIP3	12	TR1_D3+	
MDIN3	13	TR1_D3-	
EESK	48	LAN1_EESK	
EECS	44	LAN1_EECS	
EEDI/AUX	47	LAN1_EEDI	
EEDO	45	LAN1_EEDO	
LED0	57	ACT_LED1	
LED1	56	LINK100#_1	
LED2	55		
LED3	54	LINK1000#_1	
NC1	15		
NC2	17		
NC3	18		
NC4	34		
NC5	35		
NC6	39		
NC7	40		
NC8	41		
NC9	42		

X_RTL8111C

R537 X_2.49KST/4 RSET1

R558 X_1K/4 VCC3 — LAN1_ISO — R557 X_15KST/4

3VSB — FB10 X_40ohm/3A/8 — C409 X_10u/10V/8 — C404 C406 C417 C445 C464 C401 X_0.1u/25V/4

LAN1_VDD33

LAN1_DVDD12 — C451 C457 C438 C441 C473 C468 C408 C407 C405 X_10u/10V/8, X_0.1u/25V/4

LAN1_DVDD12 — FB13 X_40ohm/3A/8 — C470 C469 X_0.1u/25V/4

LAN1_FB12

CLKREQB: If this function is not implemented, make this pin floating or connect to the ground.

LAN1_ENSR

LAN1_VDD33 — R533 X_0R/4 — R534 X_0R/4

ENSR=1, Enable switching regulator

ENSR=0, Disable switching regulator

EMI.

LAN1_VDD33 — C478 X_0.1u/25V/4

LAN1_VDD33 — R542 X_3.6K/4 — R538 X_10K/4 (10K 93C56 NC 93C46)

U47 X_M93C46-WMN6TP-RH

LAN1_EECS	1	CS	VCC 8
LAN1_EESK	2	SK	DC 7
LAN1_EEDI	3	DI	ORG 6
LAN1_EEDO	4	DO	GND 5

LAN1_VDD33 — C448 X_0.1u/25V/4

C403 X_27P/50V/4 — CLK1_LANI

Y2 X_25MHz

C402 X_27P/50V/4 — CLK1_LANO

Choke C656 C345 near Pin1 200mil

LAN1_SROUT12 — CHOKE11 X_CH-4.7u1.7A-RH — LAN1_DVDD12

C450 X_22u/6.3V/12 C440 X_0.1u/25V/4

R552 X_0R/4 — LAN1_FB12

"FB12": A trace front CHOKE to RTL8111C pin5

LAN1_DVDD12 — R333 X_0R/4

3VSB — R315 X_330/4

ACT_LED1 — C222 X_0.1u/25V/4 — C228 X_0.1u/25V/4

LAN_USB1B

LAN_LED1	19	AMBER+	
ACT_LED1	20	AMBER-	
TCT1	13	NC	
TR1_D0+	18	TD1+	
TR1_D0-	12	TD1-	
TR1_D1+	17	TD2+	
TR1_D1-	11	TD2-	
TR1_D2+	16	TD3+	
TR1_D2-	10	TD3-	
TR1_D3+	15	TD4+	
TR1_D3-	9	TD4-	
RCT1	14	NC	
LINK1000#_1	21	GREEN+	
LINK100#_1	22	GREEN-	

RJ45_USBX2_LEDX2_TX-GIGA-RH-1

C237 X_0.1u/25V/4

R327 X_0R/4 — C235 X_0.1u/25V/4 — C240 X_0.1u/25V/4

Giga-Lan
N58-22F0181-F02

Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None

19 — 20 — Yellow

Orange

21 — 22 — Green

8111C switching regulator disabled

3VSB — C485 X_1u/6.3V/4

U50 X_UP7707

	1	VIN	VOUT 5
	3	EN	GND, FB 2, 4

LAN1_DVDD12 — C475 X_0.1u/25V/4 — C446 X_10u/10V/8

R567 X_1KST/4

R574 X_2KST/4

Vout=0.8* (R1+R2)/R1

MICRO-STAR INT'L CO.,LTD

MS-7522

Size	Document Description	Rev
Custom	LAN1 - RTL8111C	2.0

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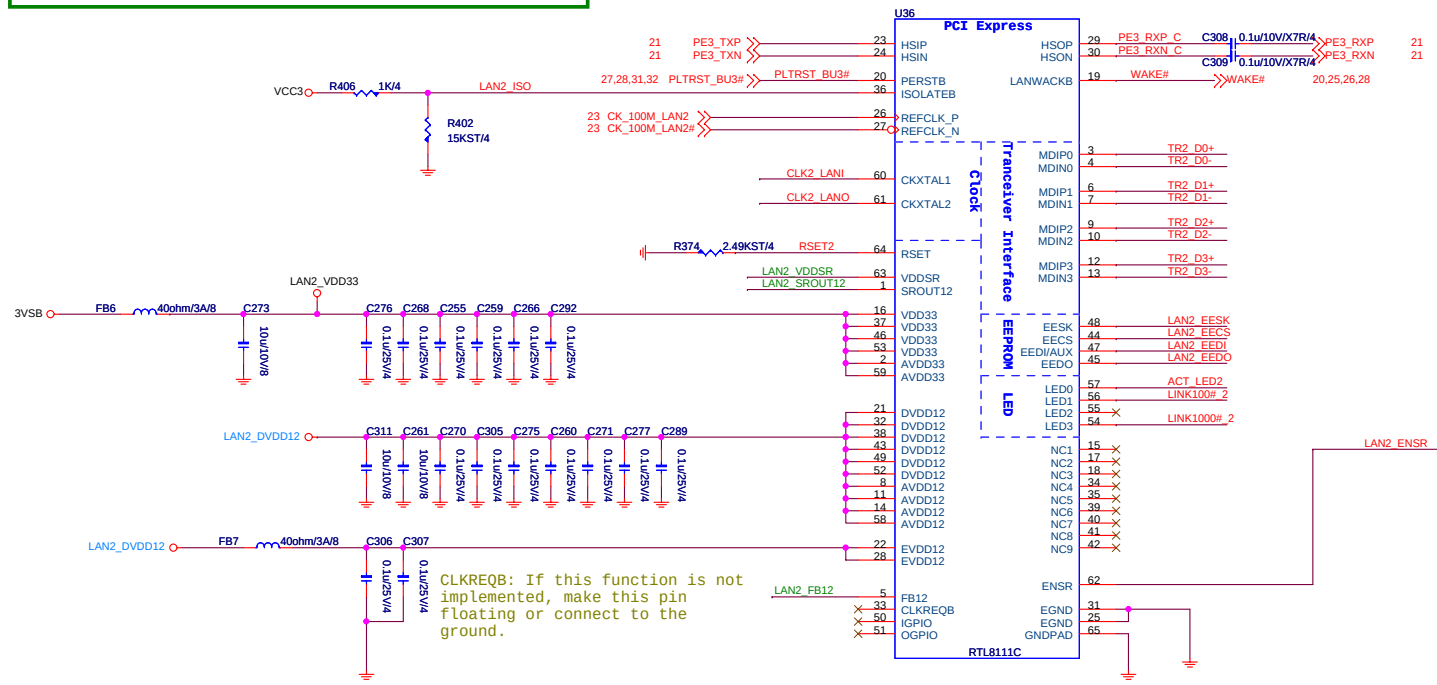
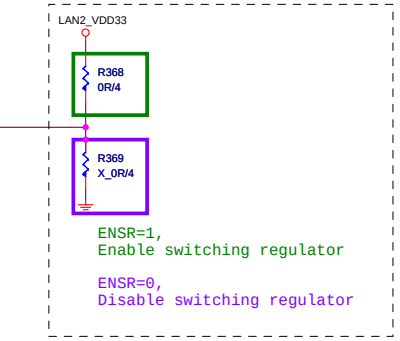
For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21

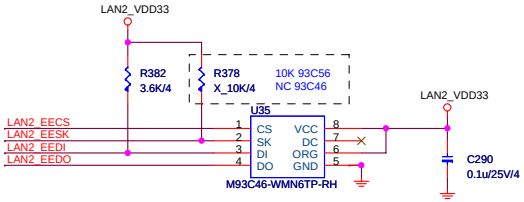
LAN2_VDD33 — R357 0R/8 — LAN2_VDDSR — C251 22u/6.3V/12 — C256 0.1u/25V/4

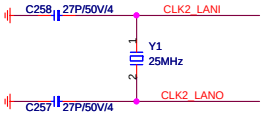
40mil width

C657 C346 near Pin63 200mil,C346 must be nearly Pin63

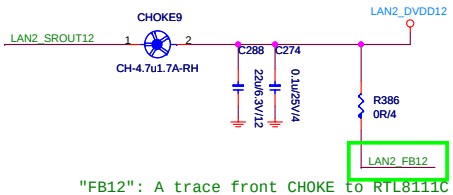




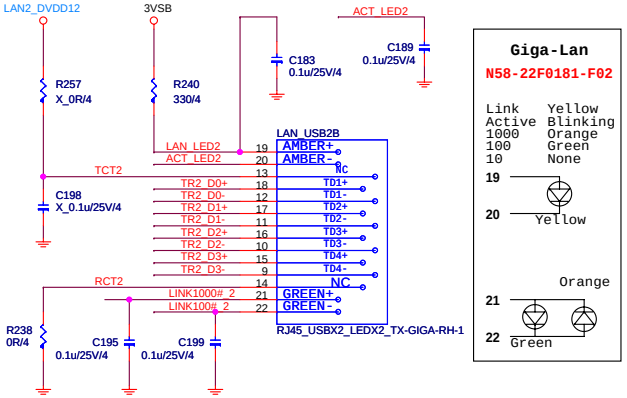




Choke C656 C345 near Pin1 200mil



"FB12": A trace front CHOKE to RTL8111C pin5



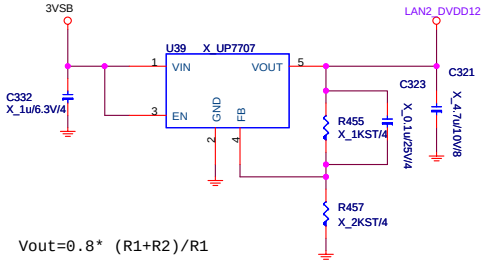
Giga-Lan
N58-22F0181-F02

Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None

19 — 20 Yellow

Orange — 21 — 22 Green

8111C switching regulator disabled



Vout=0.8* (R1+R2)/R1

MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7522		
Size: Custom	Document Description: LAN2 - RTL8111C		Rev: 2.0
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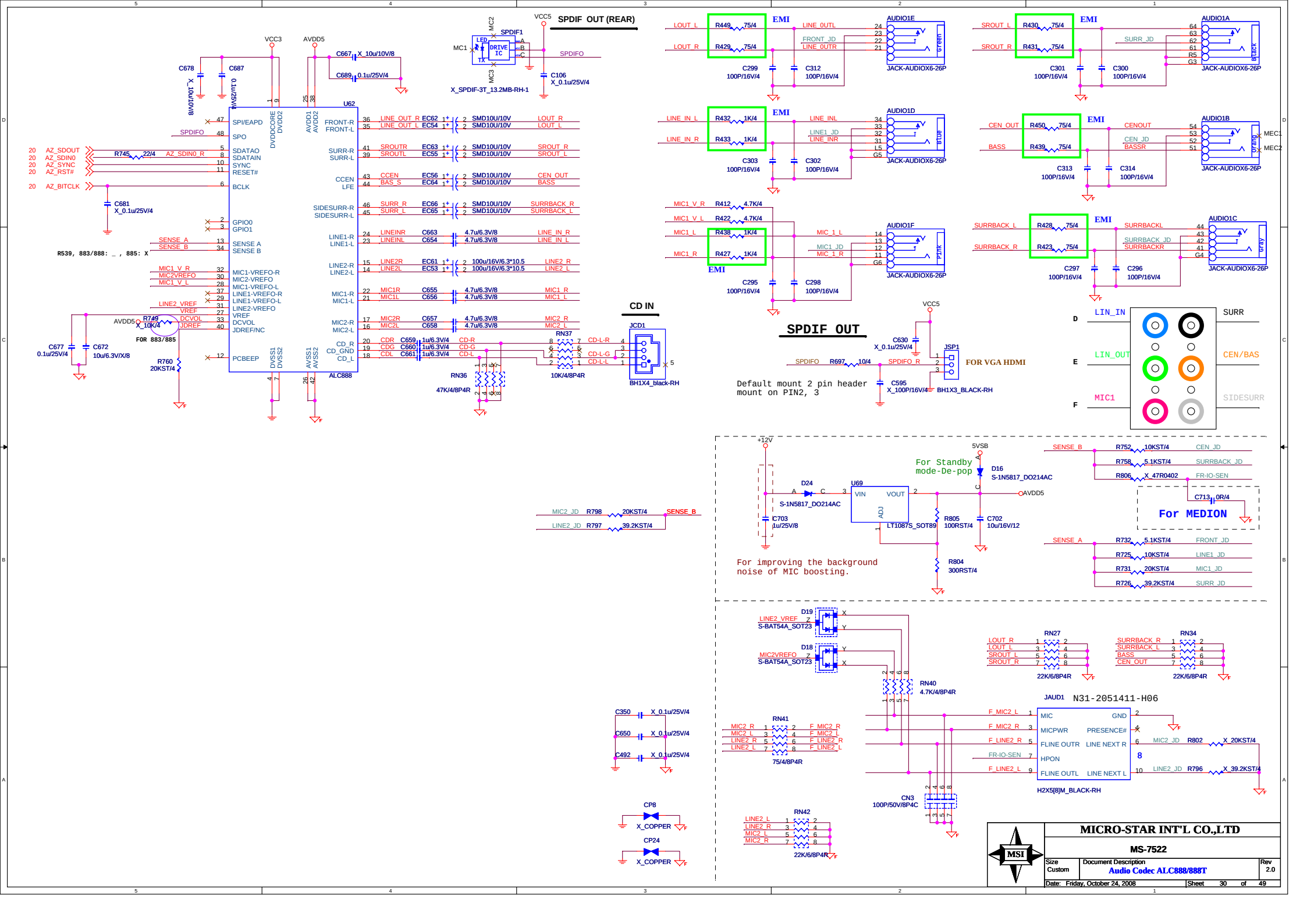
SPDIF OUT (REAR)
CD IN
SPDIF OUT
FOR VGA HDMI
Default mount 2 pin header
mount on PIN2, 3
For Standby
mode-De-pop
For improving the background
noise of MIC boosting.
For MEDION
ALC888
U62
JCD1
BH1X4_black-RH
JSP1
BH1X3_BLACK-RH
JAUD1
N31-2051411-H06
H2X5[8]M_BLACK-RH
JACK-AUDIOX6-26P
AUDIO1E
AUDIO1A
AUDIO1D
AUDIO1B
AUDIO1F
AUDIO1C
EMI
LIN_IN
LIN_OUT
MIC1
SURR
CEN/BAS
SIDESURR
MICROSTAR INT'L CO.,LTD
MS-7522
Audio Codec ALC888/888T
Rev 2.0
Date: Friday, October 24, 2008
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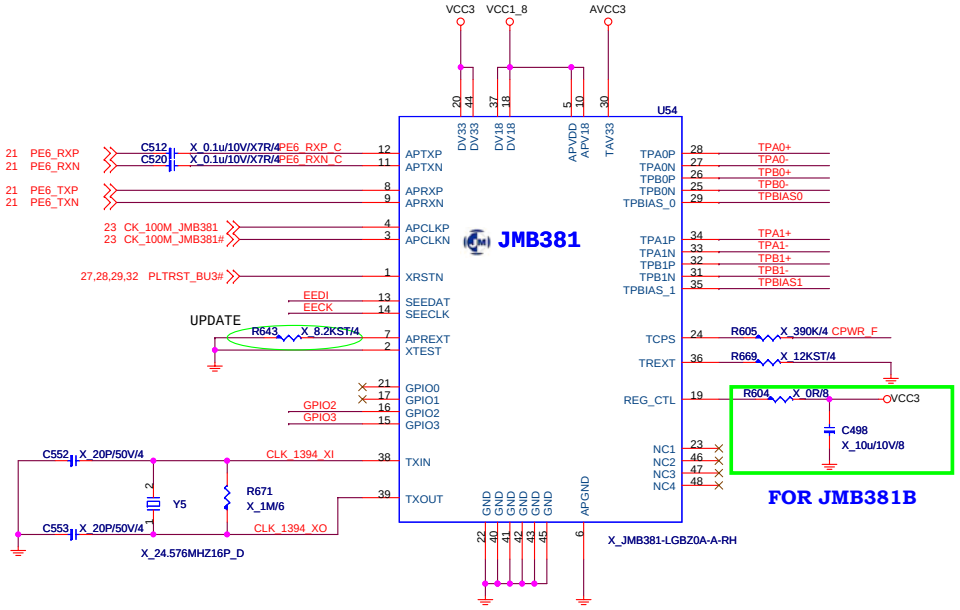
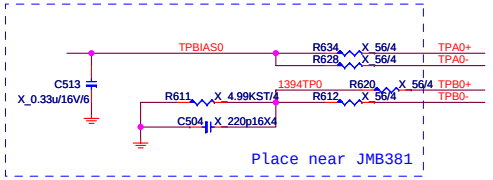
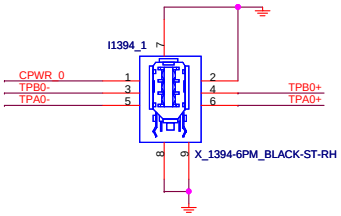
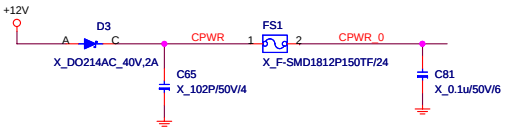
1394 CONTROLLER

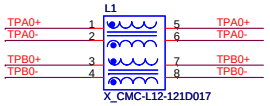


Rear 1394 port

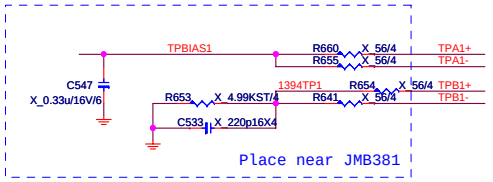


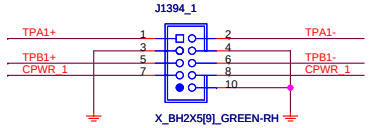




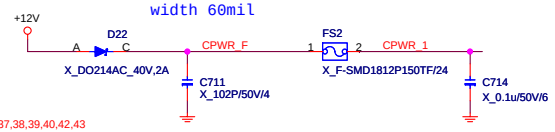


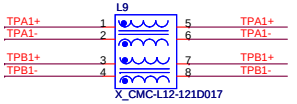
Front 1394 pin header

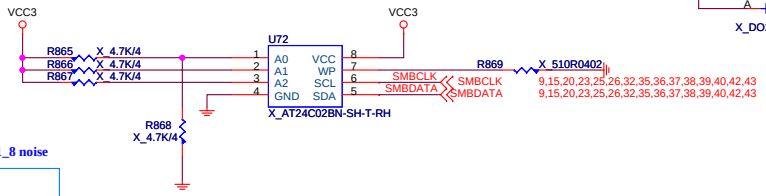


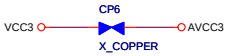


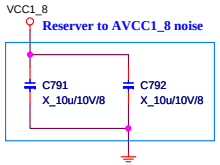
For Intel 1394 pinheader

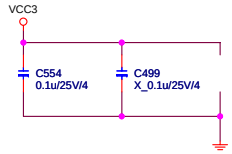


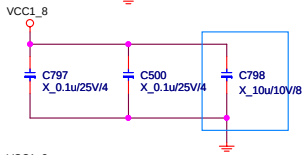


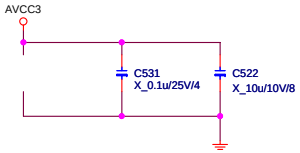


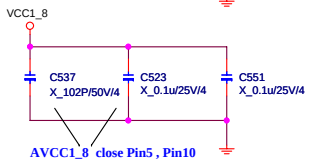




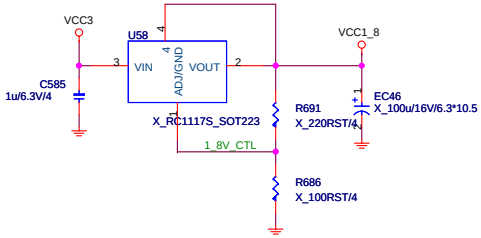


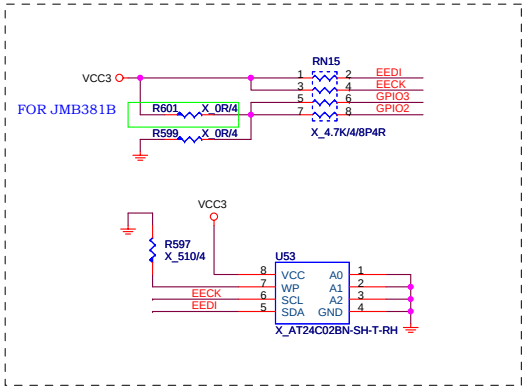






A1117 CO-LAY SOT223 (TO_261) PNP BJT





MICRO-STAR INT'L CO.,LTD	
MS-7522	
Size: Custom	Document Description: 1394 Controller - JMB381
Rev: 2.0	
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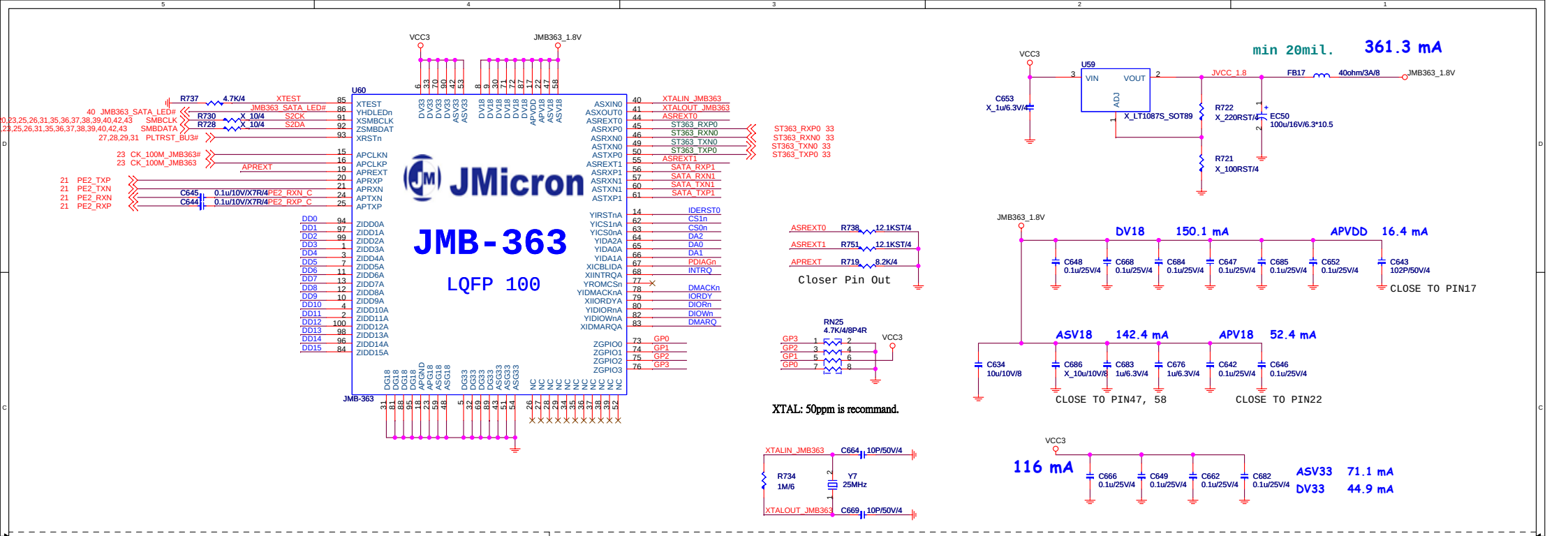
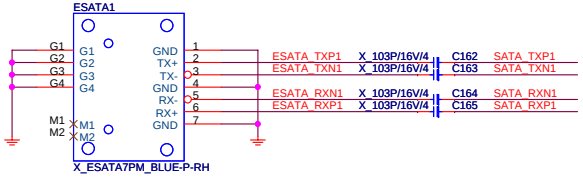
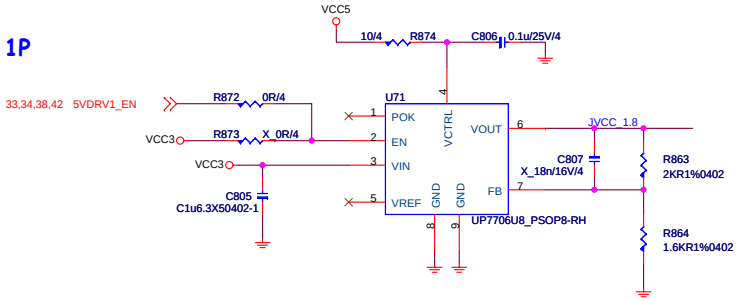
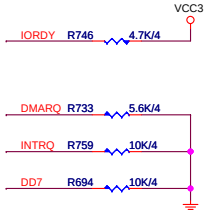


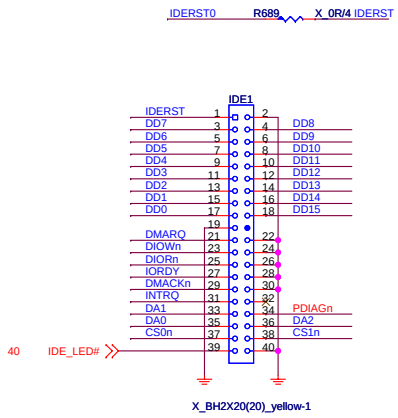
2S:
ESATA X1
the other for JMB-322 (H/W RAID).



1P







if the length of JMB-363 to IDE connector more than 4inch, that must stuff dampping resistor.

MICRO-STAR INT'L CO.,LTD		
MS-7522		
Size: Custom	Document Description: JMB363 - SATA x2/ IDE x1	Rev: 2.0
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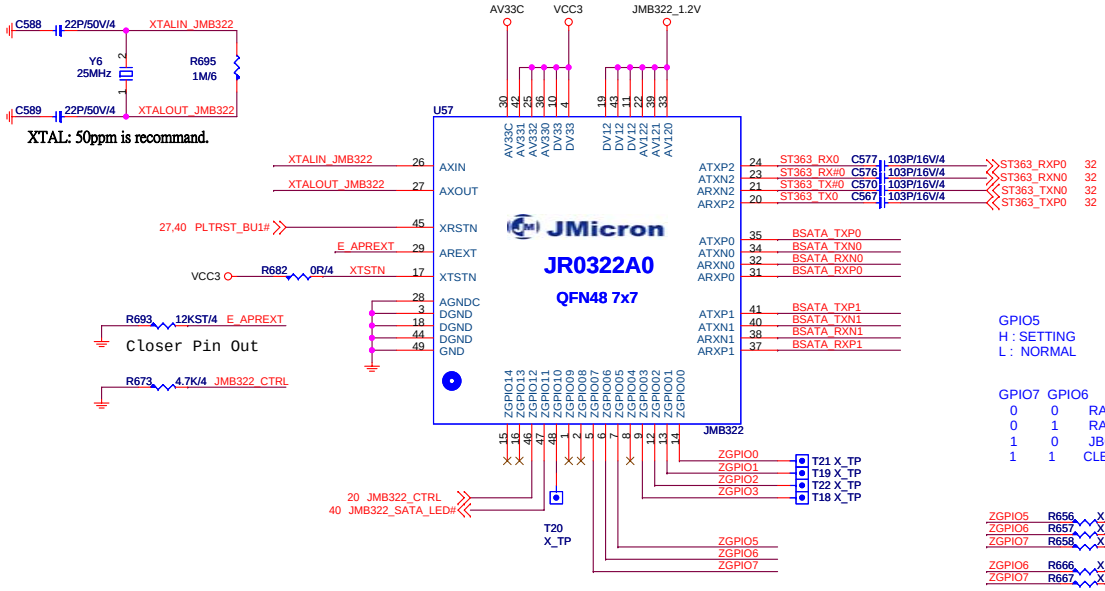
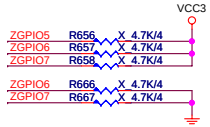
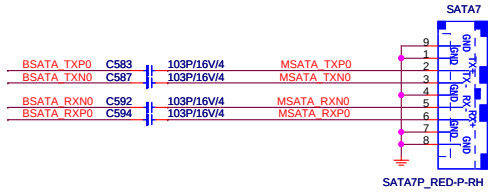
JMB322 - H/W RAID CONTROLLER

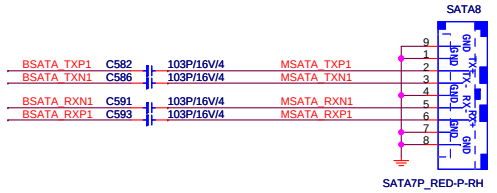


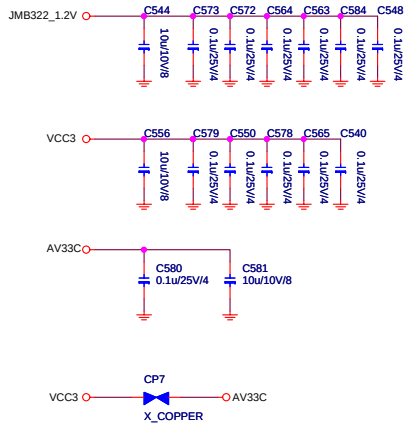
GPIO5
H : SETTING
L : NORMAL

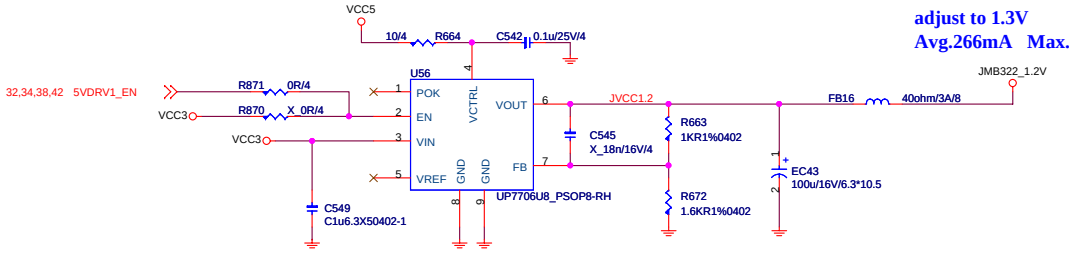
GPIO7	GPIO6	
0	0	RAID0
0	1	RAID1
1	0	JBOD
1	1	CLEAR RAID







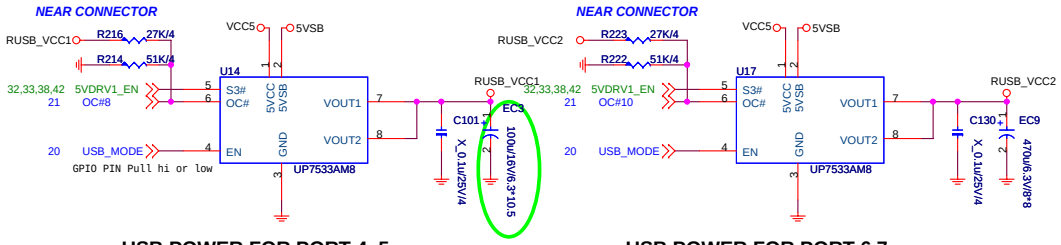




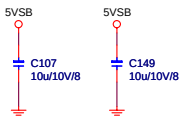
adjust to 1.3V
Avg.266mA Max.400mA

MICRO-STAR INT'L CO.,LTD		
MS-7522		
Size: Custom	Document Description: Sil5723 - RAID SATA x2	Rev: 2.0
Date: Tuesday, October 21, 2008	Sheet 33 of 49	

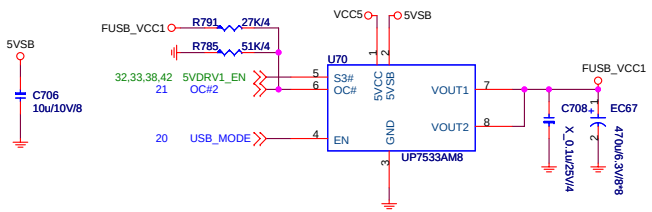
USB POWER FOR PORT 0,1



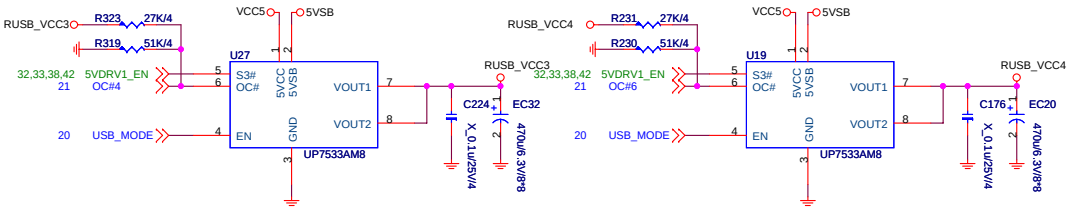
USB POWER FOR PORT 2,3



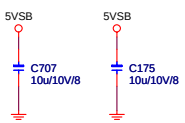
USB POWER FOR PORT 8,9



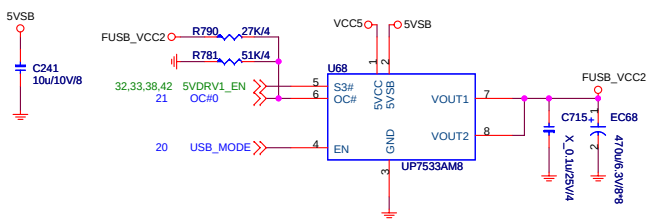
USB POWER FOR PORT 4, 5



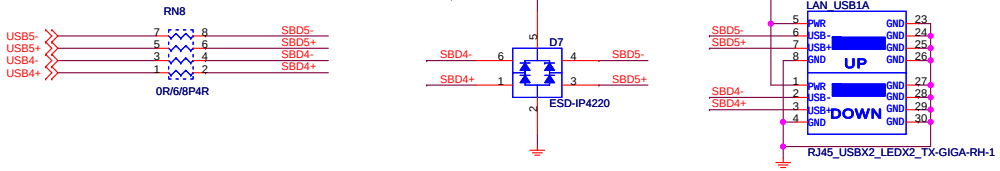
USB POWER FOR PORT 6,7



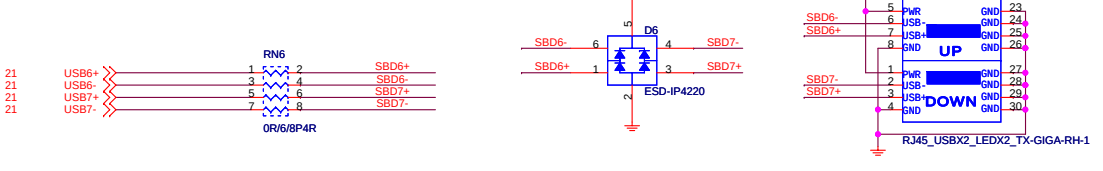
USB POWER FOR PORT 10,11



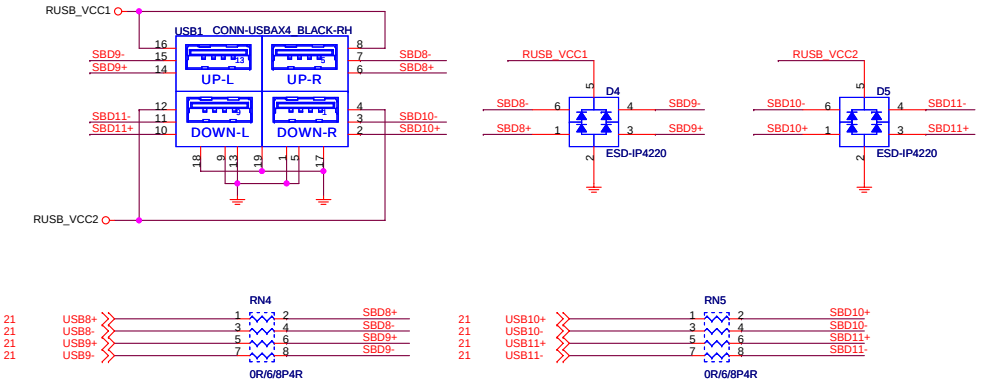
REAR USB PORT 4,5 (With LAN)



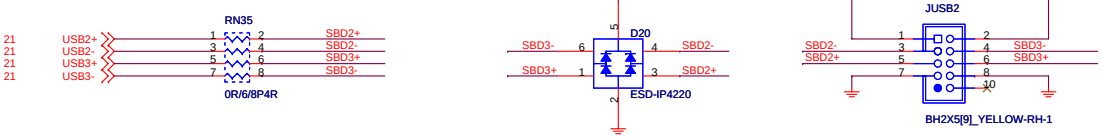
REAR USB PORT 6,7 (With LAN)



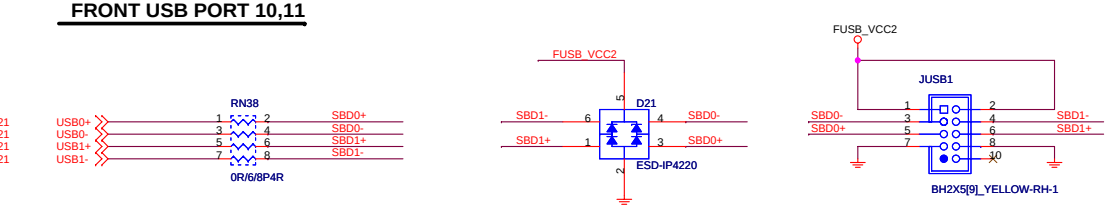
REAR USB PORT 0,1,2,3 (2x2)



FRONT USB PORT 8,9



FRONT USB PORT 10,11



MICRO-STAR INT'L CO.,LTD

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Custom	USB Connector	2.0

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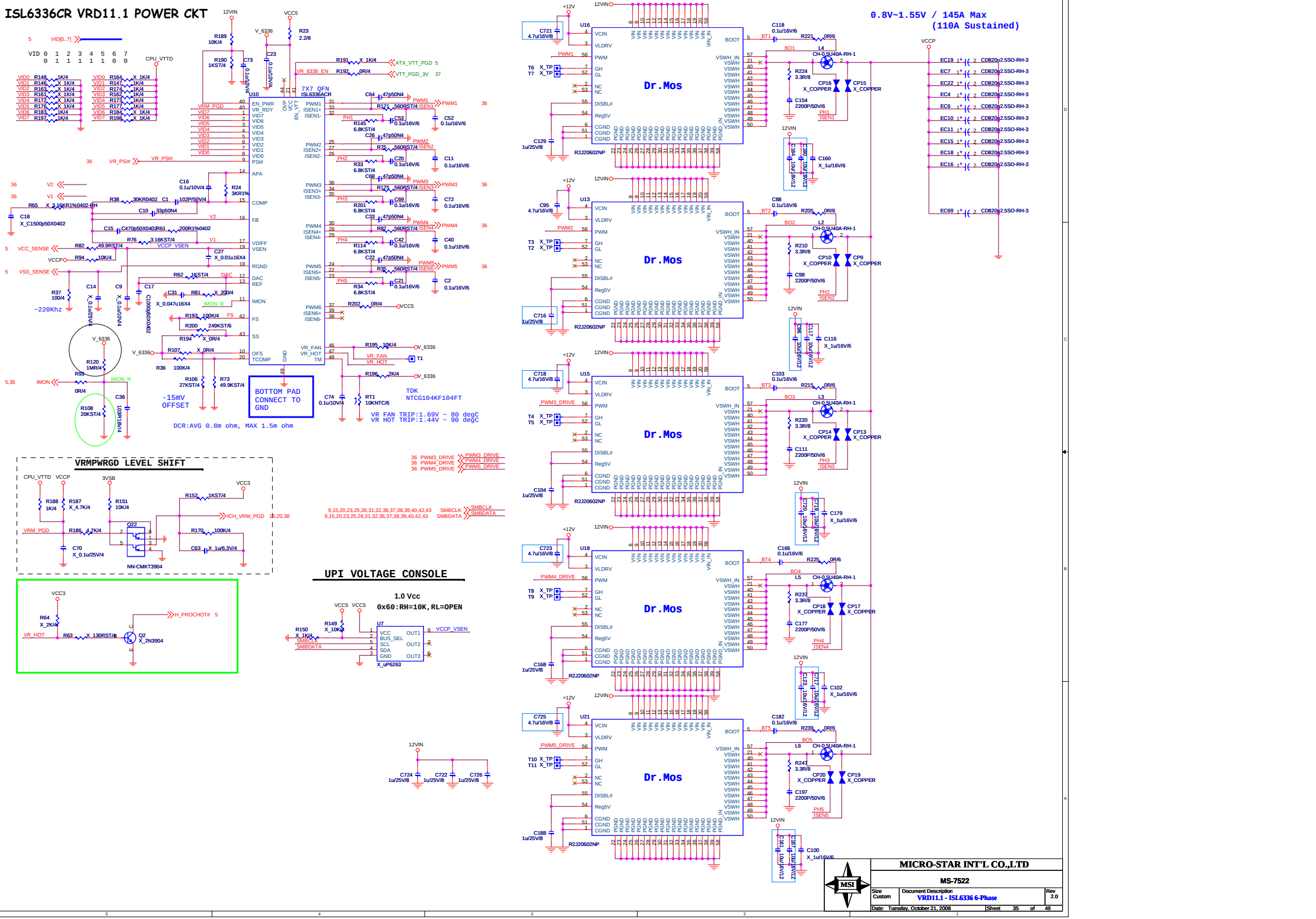
ISL6336CR VRD11.1 POWER CKT



Phase adjustment by loading

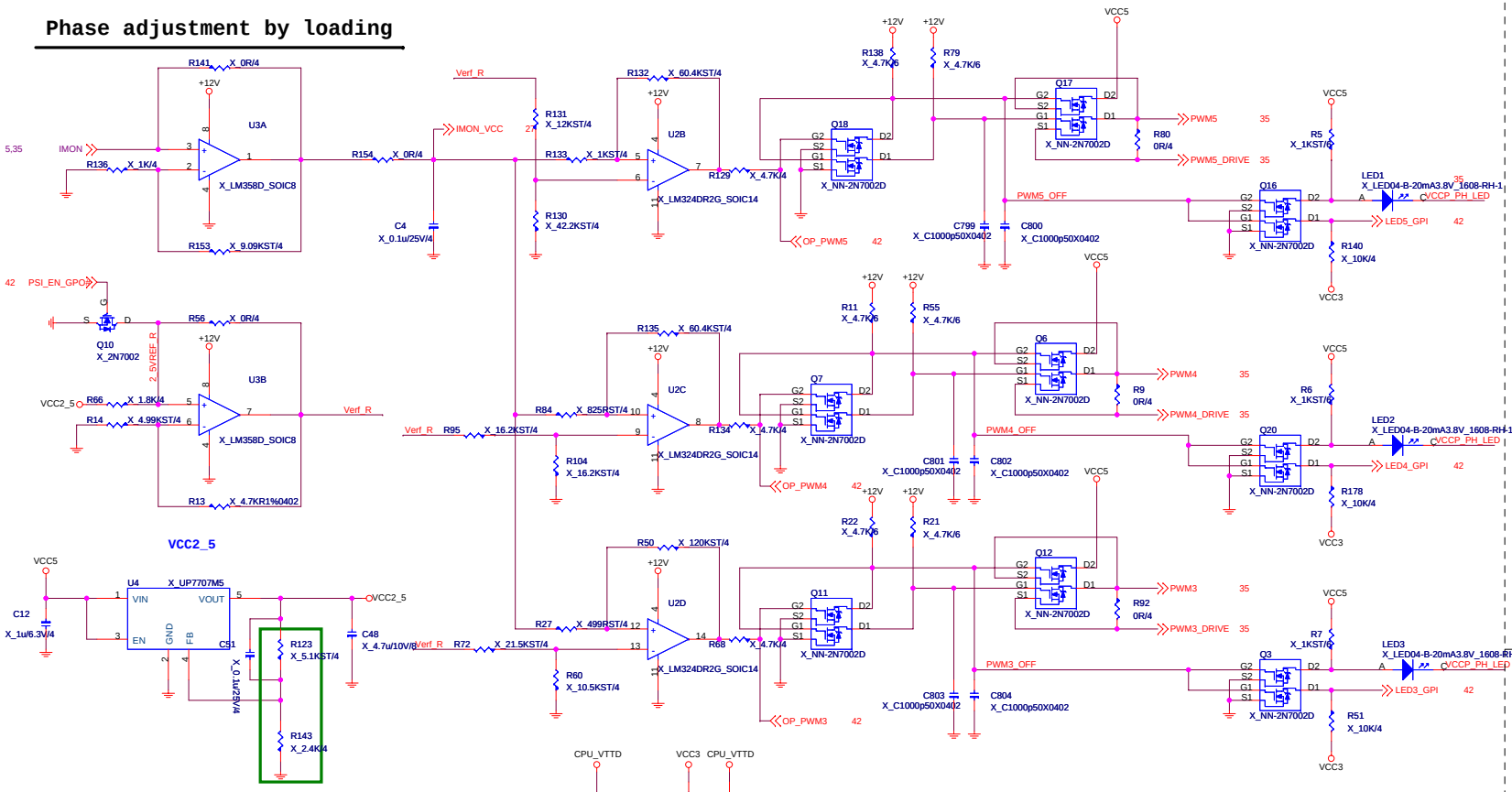
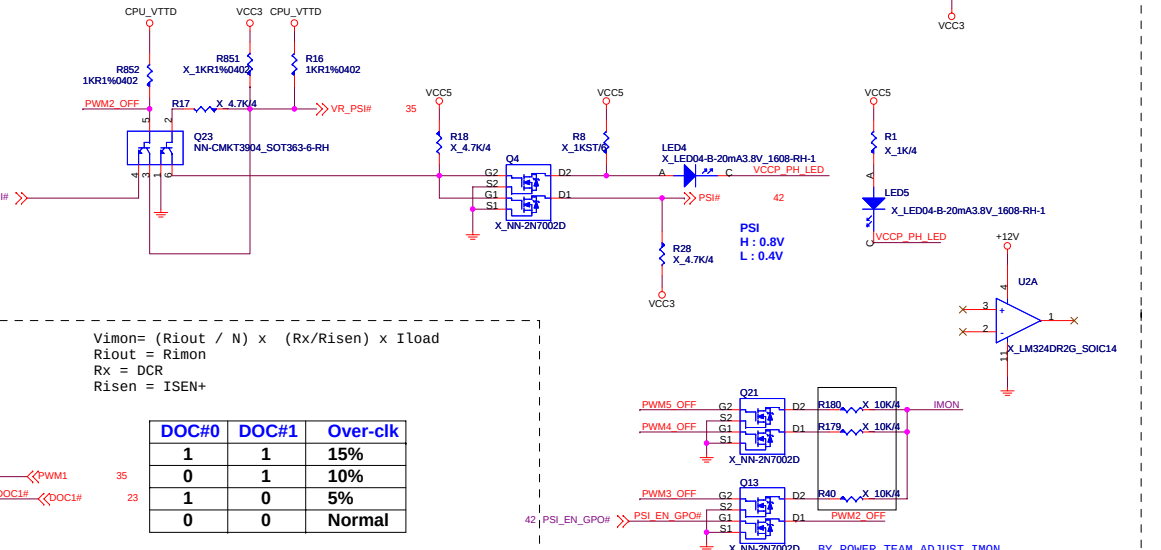


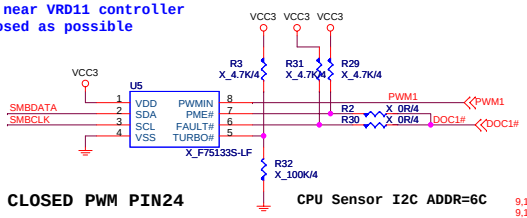
TABLE 1. PHASE DROPPING BEHAVIOR

	PSI#	FS	SS
Non-CI or (n-1)-CI Drops to 1-Phase	0	0	0
Non-CI or (n-2)-CI Drops to 2-Phase	0	0	1
2-Phase CI Drops to 1-Phase	0	1	0
2-Phase CI Drops to 2-Phase	0	1	1
Normal	1	x	x



EASY DOT FUNCTION

Place near VRD11 controller as closed as possible



CLOSED PWM PIN24

CPU Sensor I2C ADDR=6C

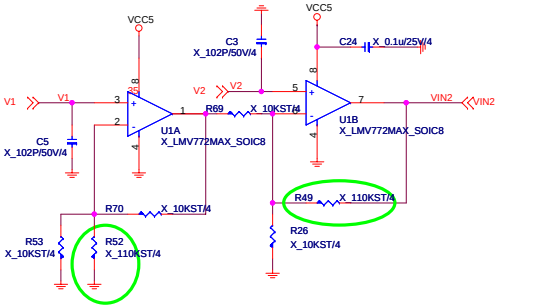
Vimon= (Riout / N) x (Rx/Risen) x Iload
Riout = Rimon
Rx = DCR
Risen = ISEN+

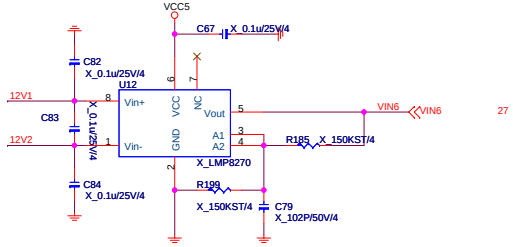
DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

9,15,20,23,25,26,31,32,35,37,38,39,40,42,43 SMBDATA
9,15,20,23,25,26,31,32,35,37,38,39,40,42,43 SMBCLK

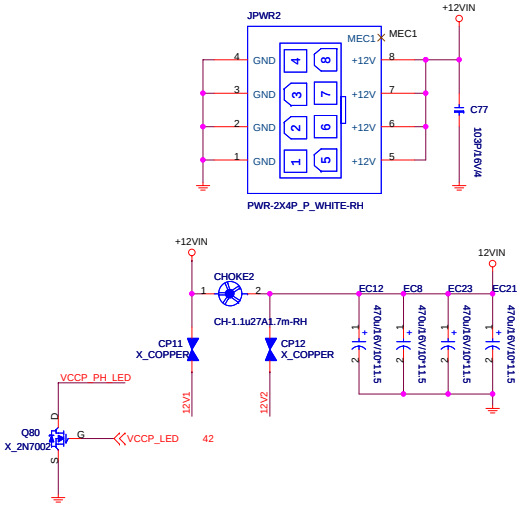
BY POWER TEAM ADJUST IMON

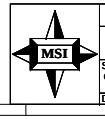
Power Wattage Monitor





CPU +12VIN POWER CONN.





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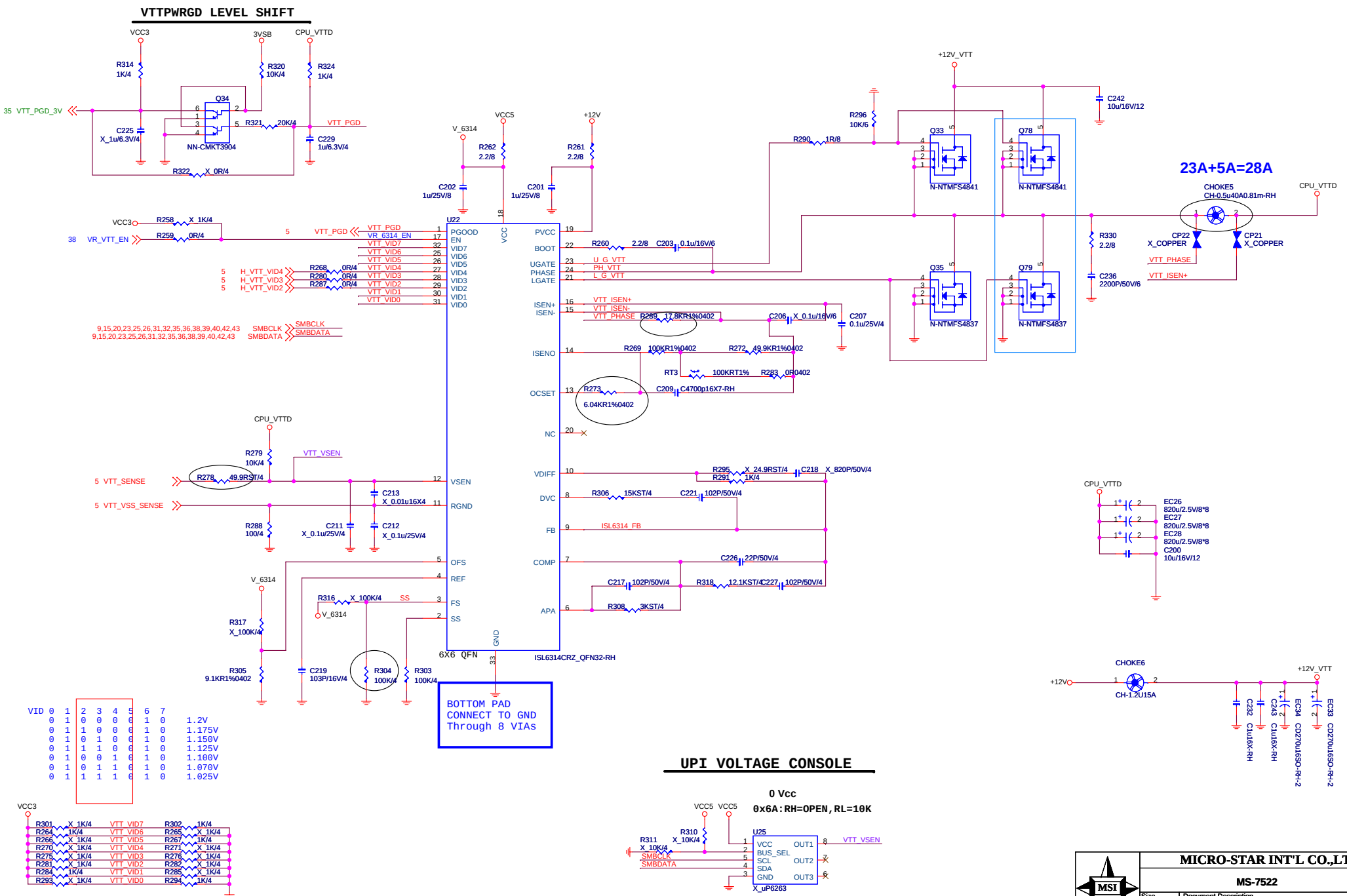
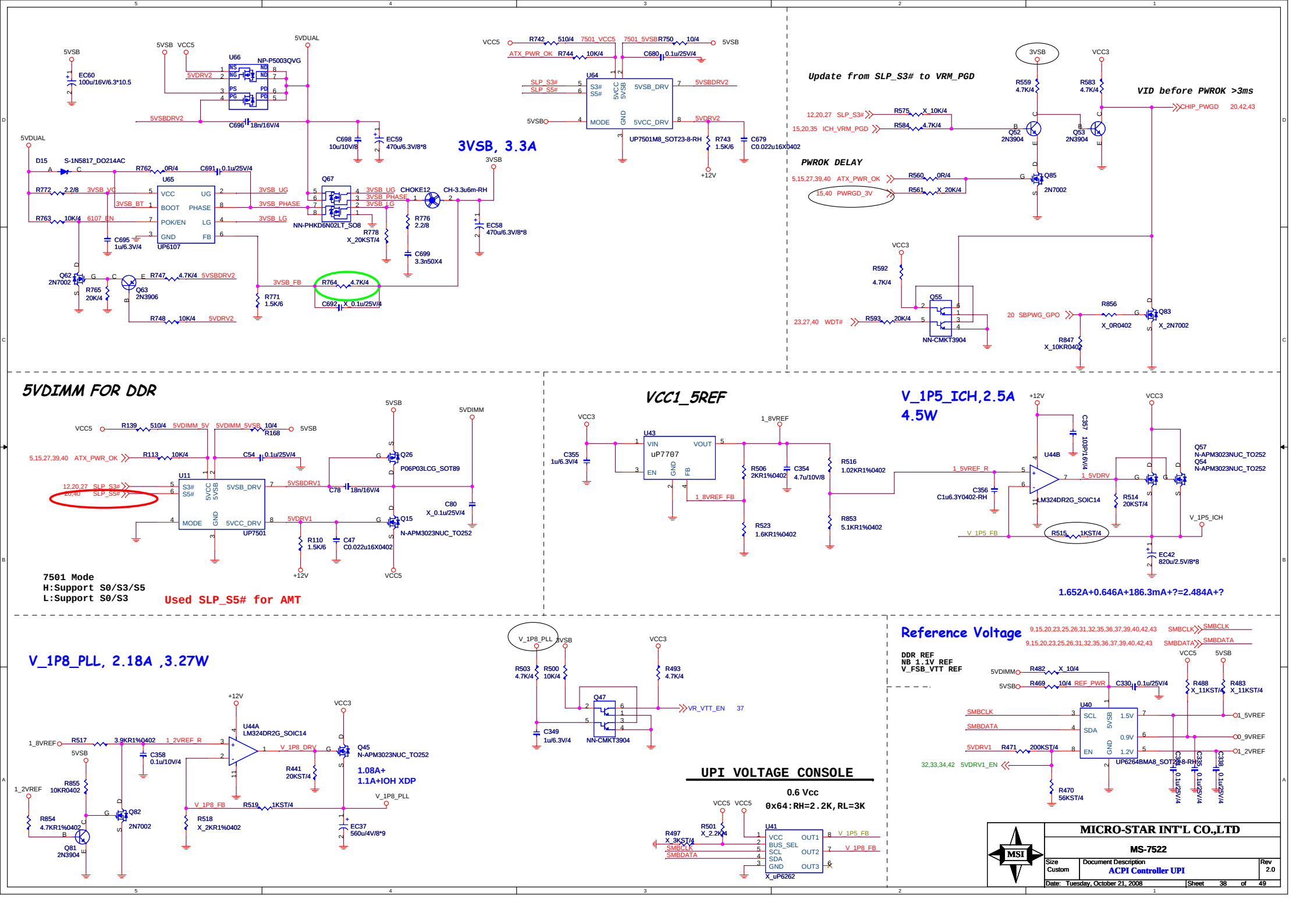
ISL6314CR POWER CKT FOR VTT 1.1V




3VSB, 3.3A
Update from SLP_S3# to VRM_PGD
VID before PWROK >3ms
PWROK DELAY
5VDIMM FOR DDR
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
Used SLP_S5# for AMT
VCC1_5REF
V_1P5_ICH,2.5A
4.5W
1.652A+0.646A+186.3mA+?=2.484A+?
V_1P8_PLL, 2.18A ,3.27W
1.08A+
1.1A+IOH XDP
UPI VOLTAGE CONSOLE
0.6 Vcc
0x64:RH=2.2K,RL=3K
Reference Voltage
DDR_REF
NB_1.1V_REF
V_FSB_VTT_REF
MICRO-STAR INT'L CO.,LTD
MS-7522
ACPI Controller UPI
Rev 2.0
Tuesday, October 21, 2008
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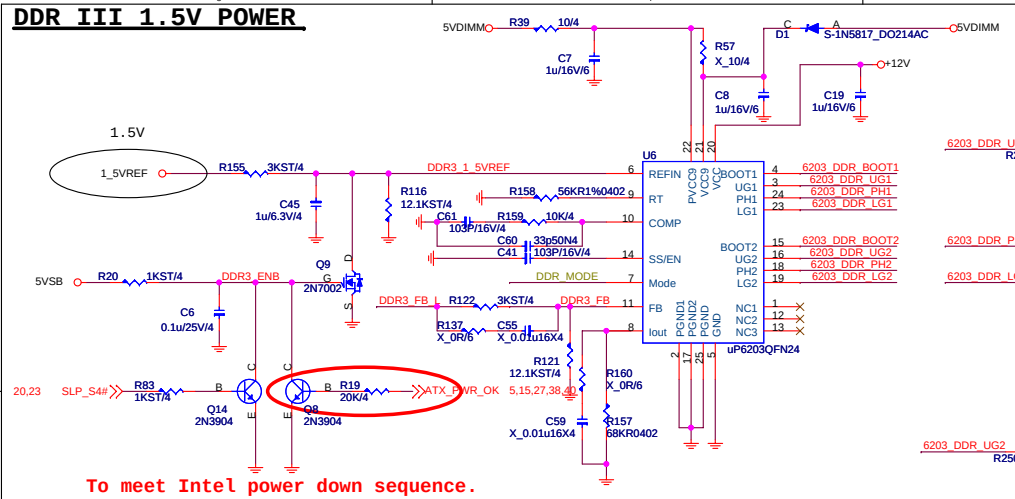
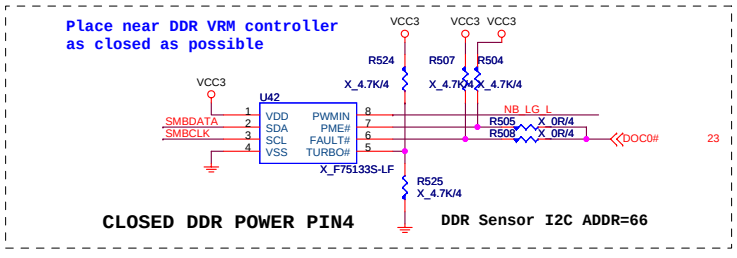
DDR III 1.5V POWER

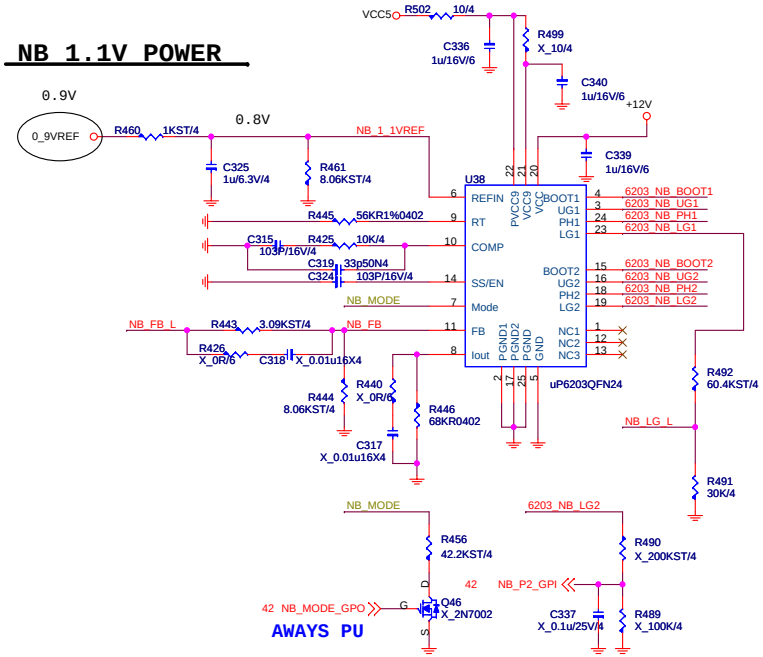


To meet Intel power down sequence.



9,15,20,23,25,26,31,32,35,36,37,38,40,42,43 SMBDATA
9,15,20,23,25,26,31,32,35,36,37,38,40,42,43 SMBCLK

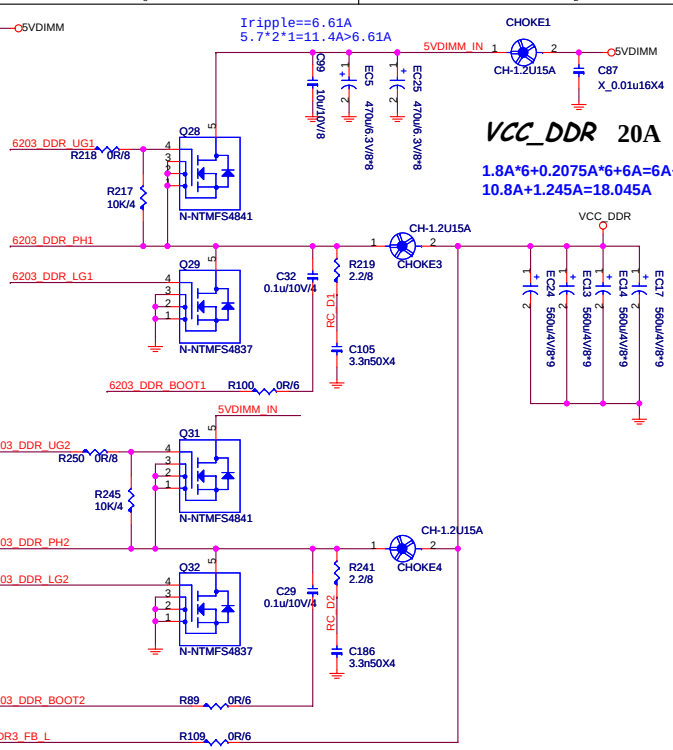
NB 1.1V POWER



Iripple==6.61A
5.7*2*1=11.4A>6.61A

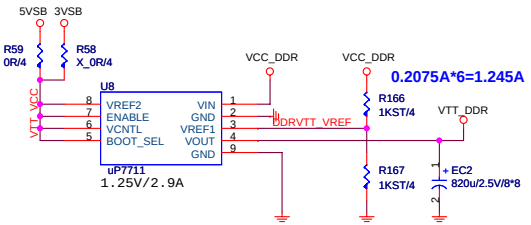
VCC_DDR 20A

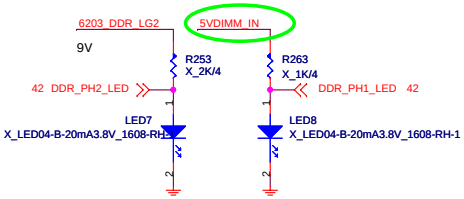
1.8A*6+0.2075A*6+6A=6A+
10.8A+1.245A=18.045A

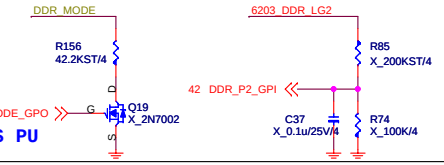


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





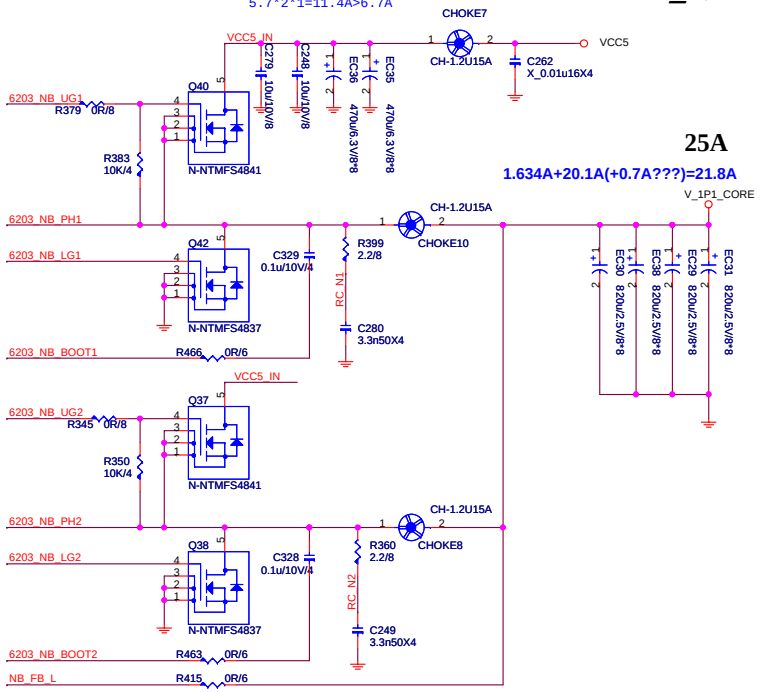


Iripple=6.7A
5.7*2*1=11.4A>6.7A

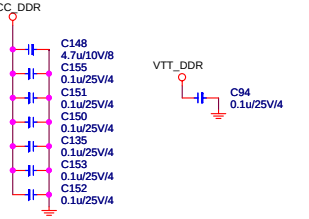
NB_1.1V

25A

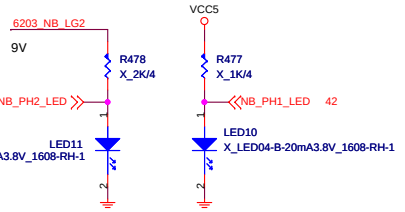
1.634A+20.1A(+0.7A???)=21.8A



VR TO DIMM SOCKET



LDO TO DIMM SOCKET



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MS-7522		
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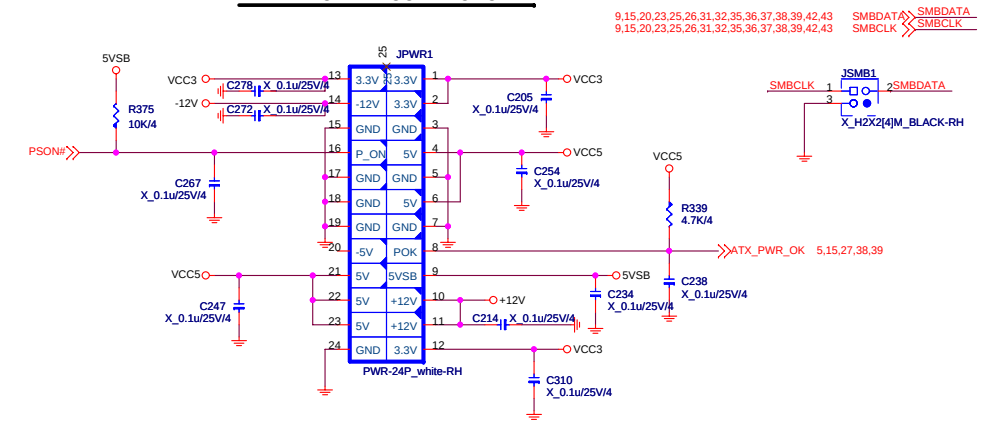
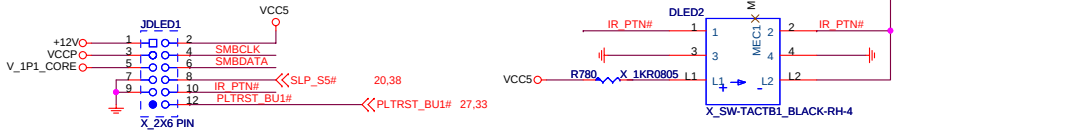
ATX POWER CONNECTOR



SPI Port

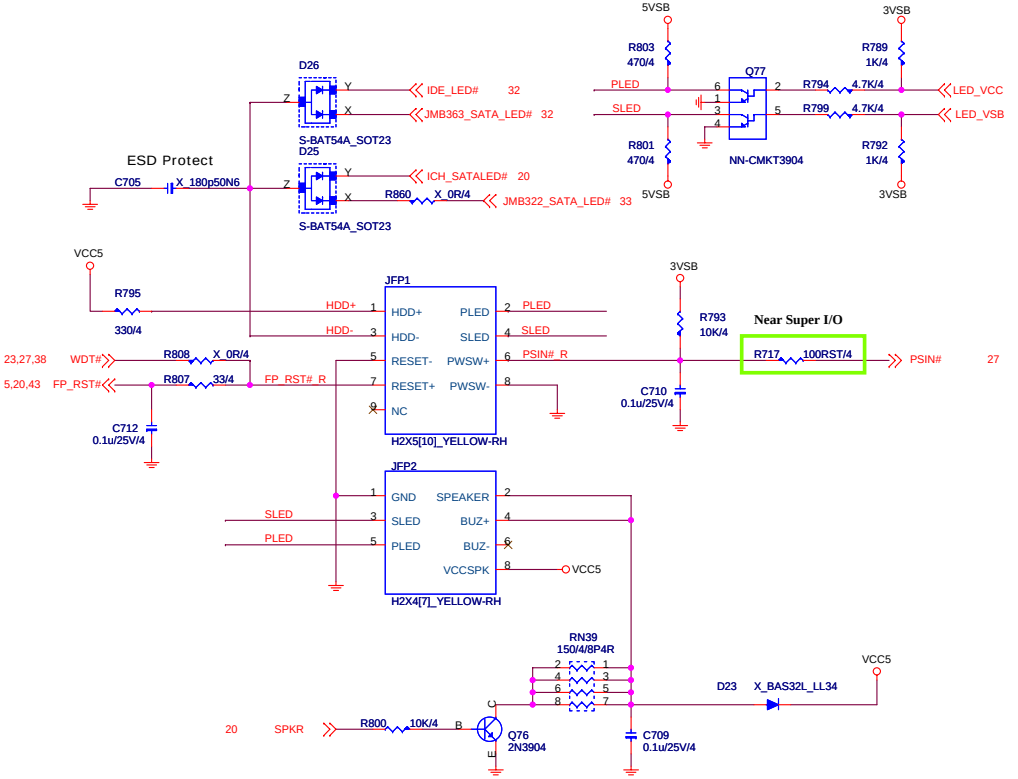
SIN2, SOUT2 link to Super IO COM2



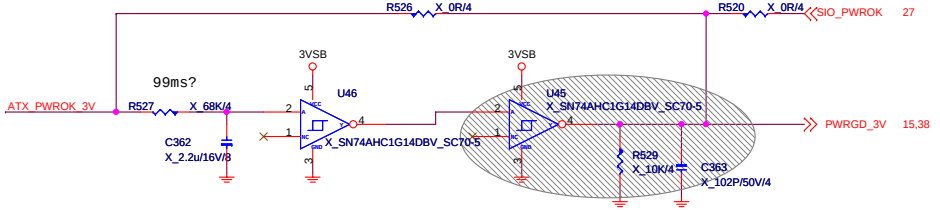
FRONT PANNEL

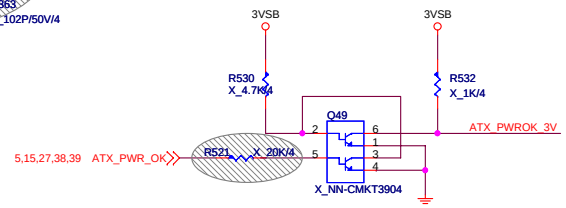
For MSI / Intel Front Panel

LED (By Fintek 71882)



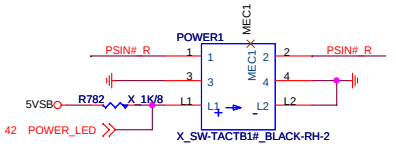
CHIPSET POWER GOOD CIRCUIT





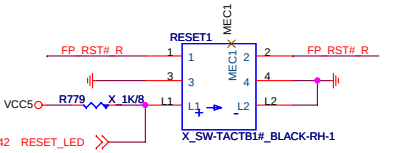
POWER ON BUTTON

LED shine:S0 ~ S5

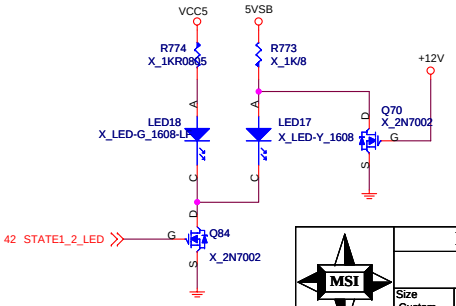


RESET BUTTON

LED shine:S0



POWER LED(S0/S3)



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MS-7522		
Size: Custom	Document Description: ATX Connector / Front Panel	Rev: 2.0
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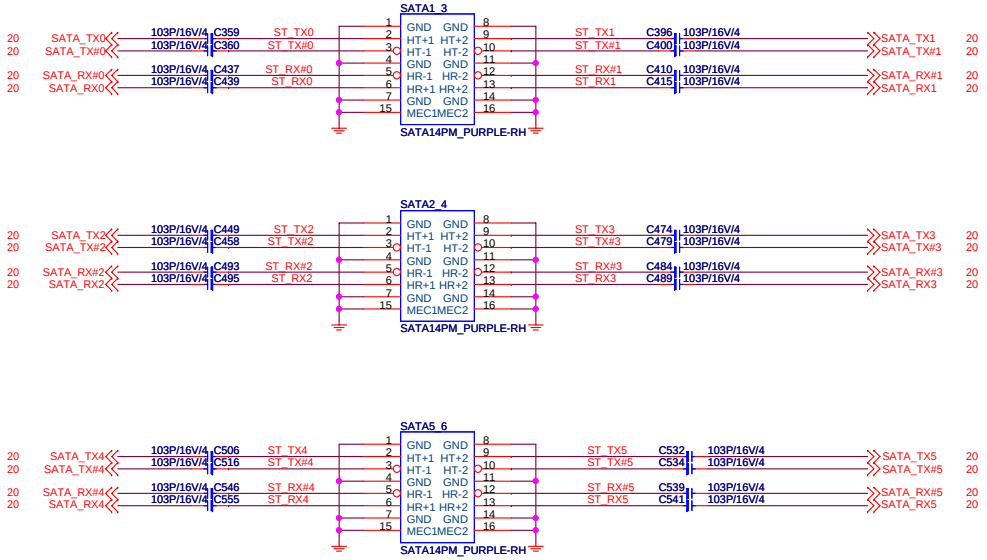
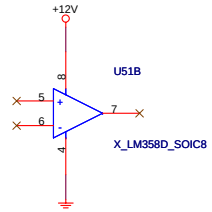
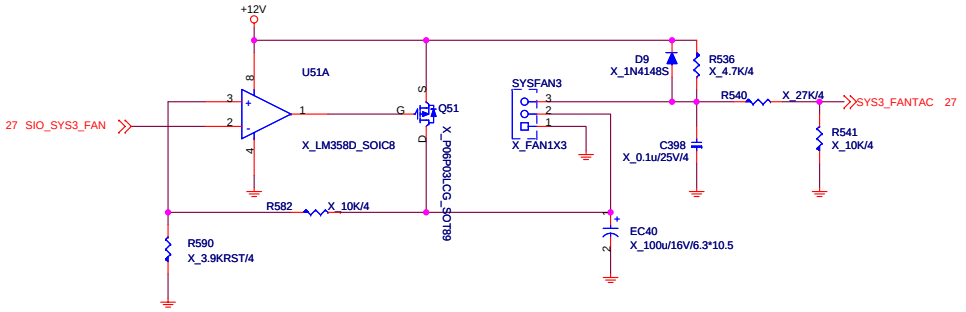
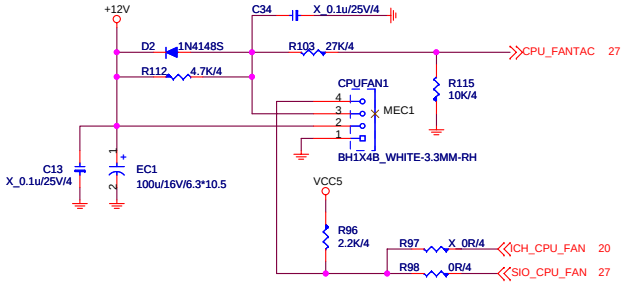
SATA-II Connector



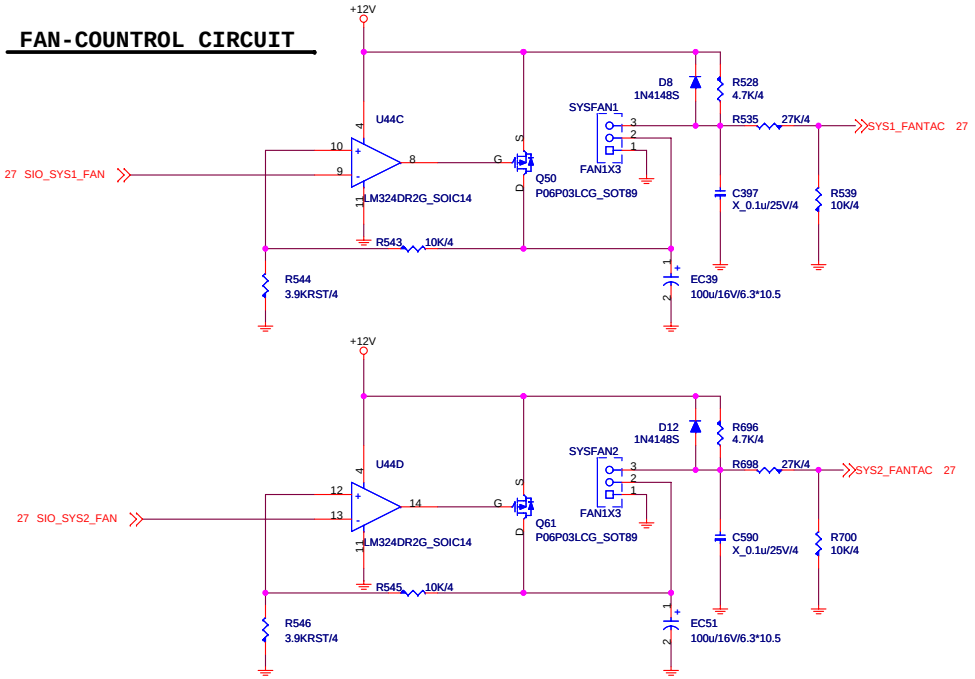


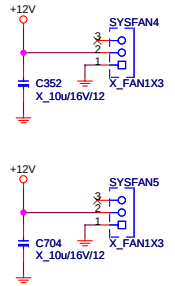


CPU FAN



FAN-COUNTROL CIRCUIT





MICRO-STAR INT'L CO.,LTD

MS-7522

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Custom	ICH SATA / FAN Control	2.0

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GPIO Controller

9,15,20,23,25,26,31,32,35,36,37,38,39,40,43 SMBDATA
9,15,20,23,25,26,31,32,35,36,37,38,39,40,43 SMBCLK

VCC3

RN1 X_8P4R-1KR0402: PSI_EN_GPO#, DDR_MODE_GPO, NB_MODE_GPO

RN3 X_8P4R-1KR0402: PWM5_0FF_GPO, PWM4_0FF_GPO, PWM3_0FF_GPO

Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)
0 0 0 1

C43 X_0.1u/25V/4, C38 X_1u/6.3V/4, VCC3

R86 10K/4, C25 X_C1u6.3X50402-1

U9 X_W83L604G-RH
SMBCLK, SMBDATA, PWM5_0FF_GPO, PWM4_0FF_GPO, PWM3_0FF_GPO
LED0/GP10, LED1/GP11 A0/GP17, LED2/GP12 A1/GP16, LED3/GP13 A2/GP15
VSS, BEEP/GP14
GP20 GP25, GP21 GP24, GP22 GP23
SCL, SDA, 3VDD, RST#, INT#

PSI_EN_GPO# 36
DDR_MODE_GPO 39
NB_MODE_GPO 39
36 LED5_GPI
36 LED4_GPI
36 LED3_GPI
DDR_P2_GPI 39
NB_P2_GPI 39
PSI# 36

Only PSI_EN_GPO Default High
Others Default Low

PWM3_0FF_GPO → Q25 X_2N7002 → OP_PWM3 36

Q24 X_NN-2N7002D: PWM4_0FF_GPO → OP_PWM4 36; PWM5_0FF_GPO → OP_PWM5 36

防測試線路

5VSB
R509 10K/4
Q48 X_NN-2N7002D: 5 H_SKTOCC# → 5VDRV1_EN 32,33,34,38; 20,38,43 CHIP_PWGD

GPIO Controller - B LED / VTT / PHASE6

STRAP_GP17 R857 X_4.7K/4 3VSB

BUTTON1_2_3_LED R875 X_1K/4

VCCP_LED R859 X_1K/4
STATE1_2_LED R861 X_1K/4

RN31 X_8P4R-1KR0402: PCIE_SLOT4_5_LED, PCIE_SLOT1_2_3_LED, PCI_SLOT1_2_LED

DDR_1_2_LED R858 X_1K/4
NB_LED R862 X_1K/4

Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)
0 0 0 1

C694 X_0.1u/25V/4, C333 X_1u/6.3V/4, 3VSB

U67 X_W83L604G-RH
SMBCLK, SMBDATA, PCI_SLOT1_2_LED, PCIE_SLOT1_2_3_LED, PCIE_SLOT4_5_LED, STATE1_2_LED, VCCP_LED, BUTTON1_2_3_LED
LED0/GP10, LED1/GP11 A0/GP17, LED2/GP12 A1/GP16, LED3/GP13 A2/GP15
VSS, BEEP/GP14
GP20 GP25, GP21 GP24, GP22 GP23
SCL, SDA, 3VDD, RST#, INT#

STRAP_GP17
DDR_1_2_LED
NB_LED

R775 X_10K/4
C697 X_C1u6.3X50402-1

40 STATE1_2_LED
36 VCCP_LED

Only VTT_PSI_GPO# Default High
Others Default Low

Q68 X_NN-2N7002D: NB_LED → NB_PH1_LED 39; NB_LED → NB_PH2_LED 39

Q75 X_NN-2N7002D: BUTTON1_2_3_LED → RESET_LED 40; BUTTON1_2_3_LED → POWER_LED 40

EMI CAP

VCC5
C30 0.1u/25V/4, C89 0.1u/25V/4

EM74 X_E23-5611010-RH
EM73 X_E23-5611010-RH

Q64 X_NN-2N7002D: PCI_SLOT1_2_LED → PCI_LED1 24; PCI_SLOT1_2_LED → PCI_LED2 24

Q43 X_NN-2N7002D: PCIE_SLOT1_2_3_LED → PCIE_LED1 26; PCIE_SLOT1_2_3_LED → PCIE_LED2 25

Q69 X_NN-2N7002D: PCIE_SLOT1_2_3_LED → PCIE_LED3 26; BUTTON1_2_3_LED → TURBO_LED → TURBO_LED 20

Q65 X_NN-2N7002D: PCIE_SLOT4_5_LED → PCIE_LED4 26; PCIE_SLOT4_5_LED → PCIE_LED5 25

Q66 X_NN-2N7002D: DDR_1_2_LED → DDR_PH1_LED 39; DDR_1_2_LED → DDR_PH2_LED 39

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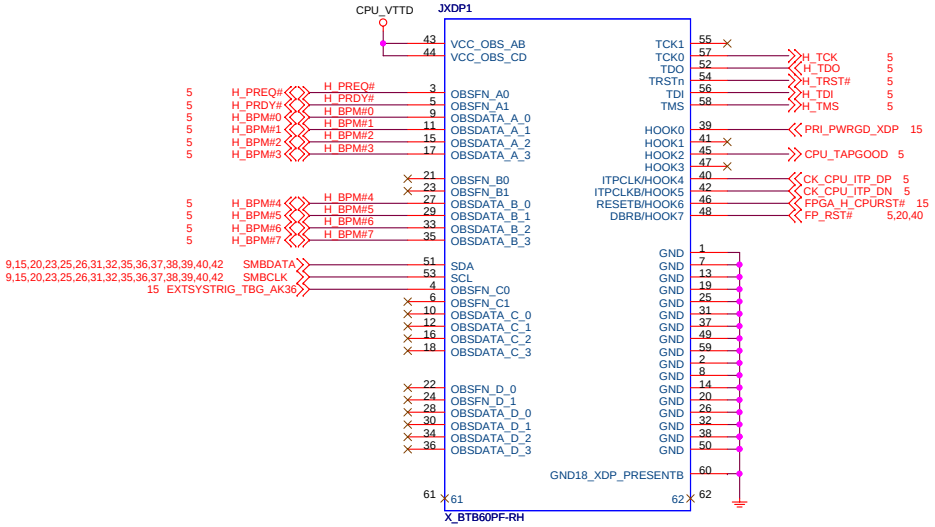
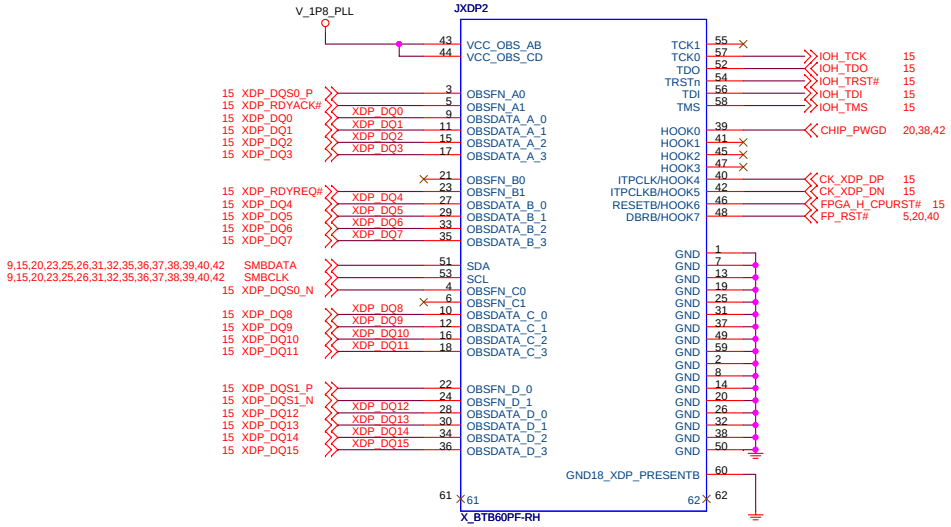
Reserve debug port 5020



Reserve debug port 5020



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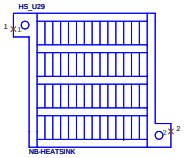
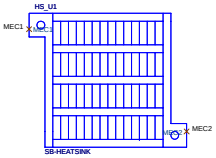
HEATSINK NUMBER到時要改與NB SB NUMBER一致

PD0-0752220-G37, 精成
* PD0-0752220-E48, 競華

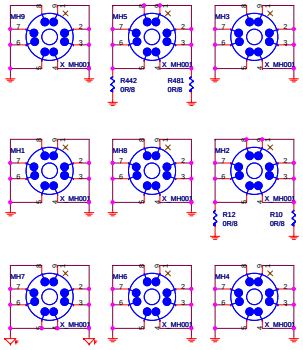




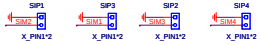
Optical Fiducial Marks-120

Optical Fiducial Marks-100

Mounting Holes



Simulation



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Size: Custom	Document Description: Manual Parts	Rev: 2.0
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