

MS-7732 Ver: 1.1 ATX : 304.8 X 205mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Slot * 3

PWM:

Controller:VRD12 UP1625 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: IP6103

CPU SA : OP+MOS

DDR: UP6103

PCH: UP6103

ACPI:

UPI

Other:

SATA3.0 x2 (ASM1061)+ SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x4

USB3.0 RearX2

D-SUB *1 DVI*1

TPM Header *1

COM Header *1

LPT Header *1

on BOARD BUZZER


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三個BOM:

A.H61 Full Spec(全固)

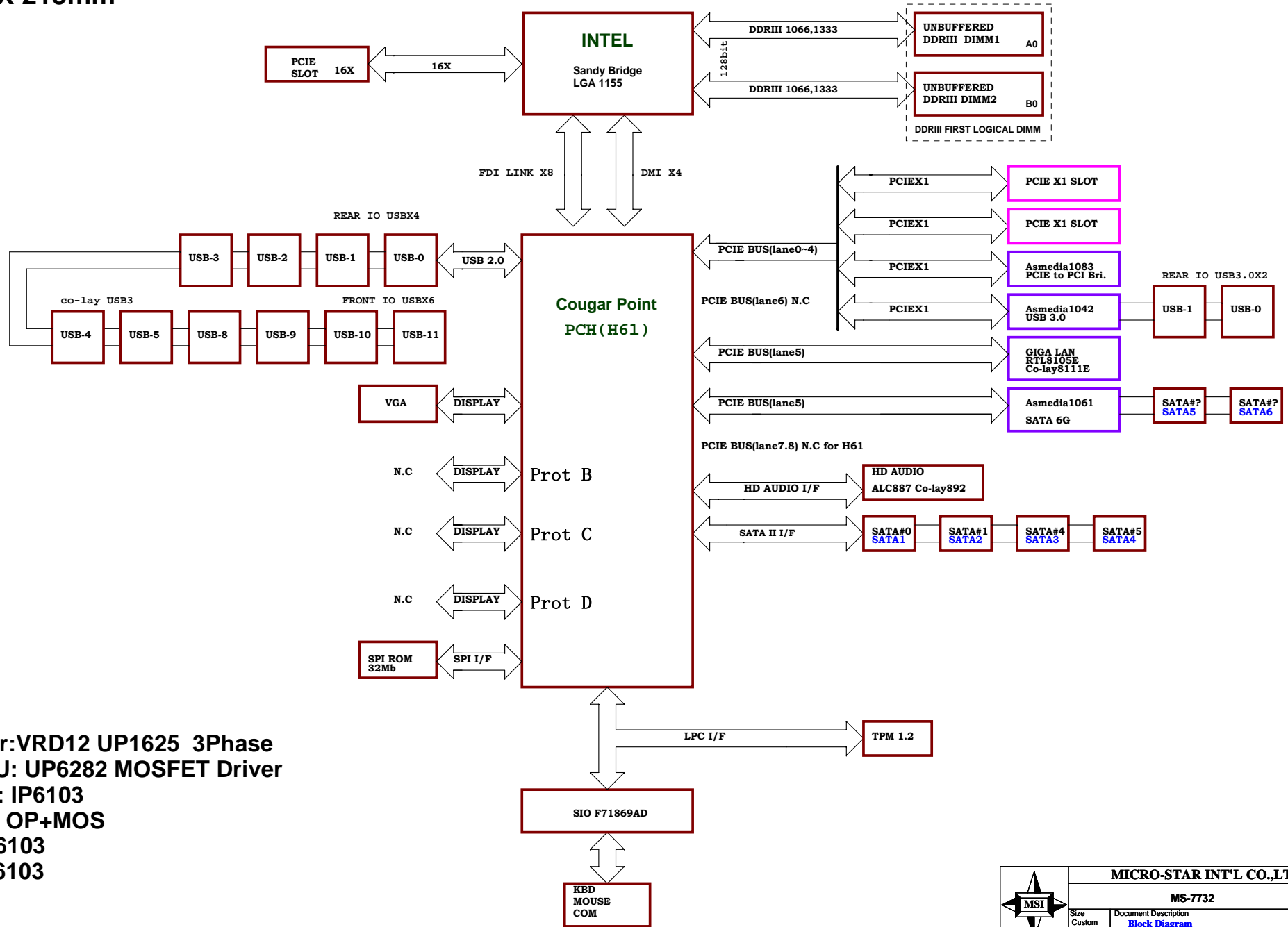
B.H61 No USB3 & SATA 6G(全固)

C.H61 網吧板(全固)

			MICRO-STAR INT'L CO.,LTD	
			MS-7732	
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Custom	Cover Sheet	1.1		
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MS-7732 Ver: 1.0

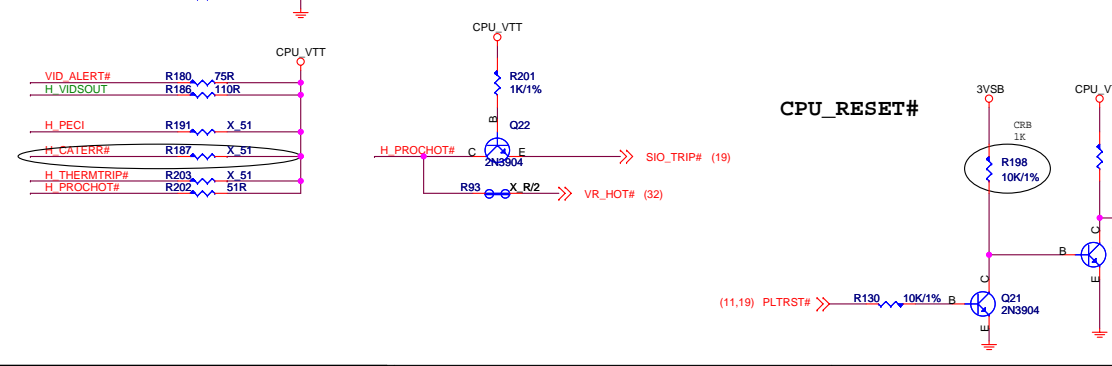
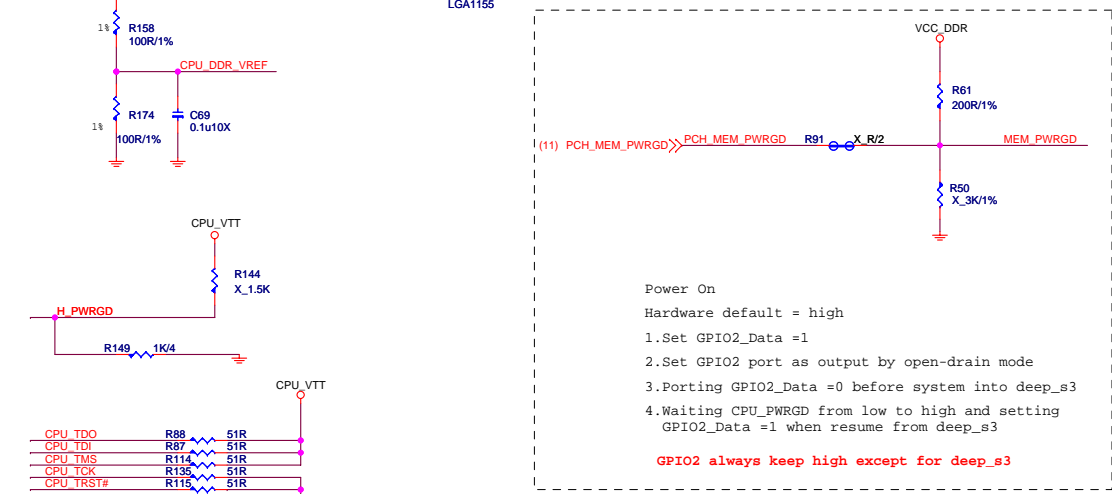
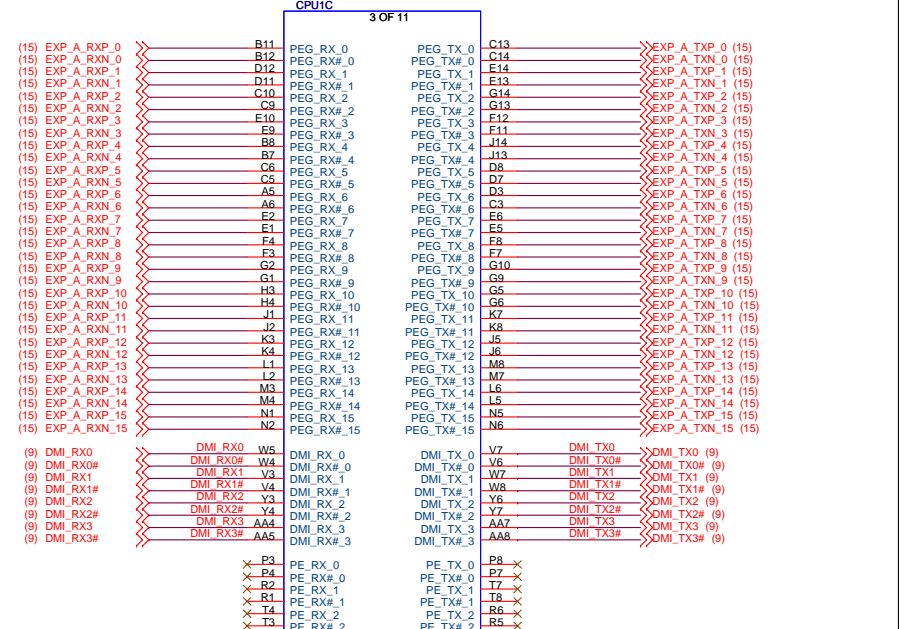
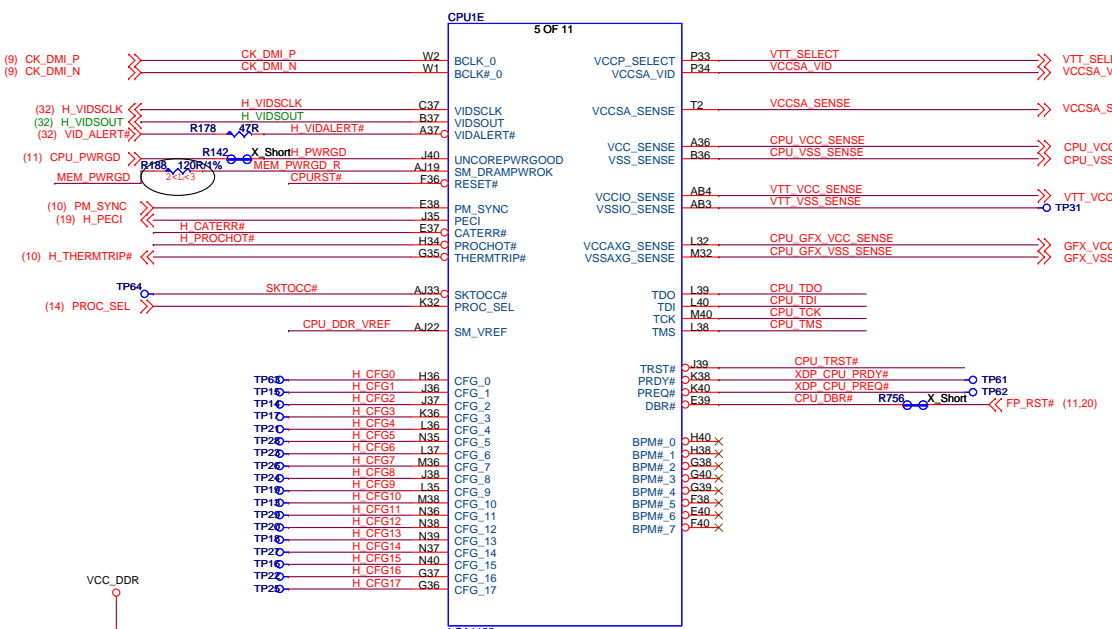
ATX : 305 X 215mm



PWM:

Controller:VRD12 UP1625 3Phase
 CPU+GPU: UP6282 MOSFET Driver
 CPU VTT: IP6103
 CPU SA : OP+MOS
 DDR: UP6103
 PCH: UP6103

MICRO-STAR INT'L CO.,LTD		
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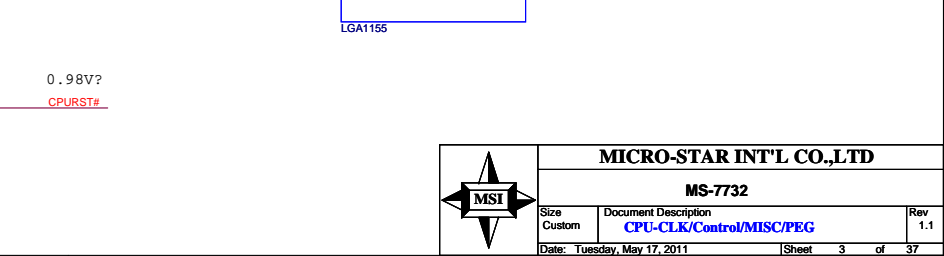
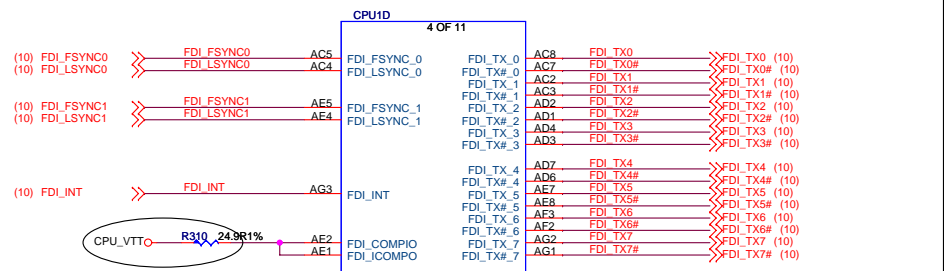
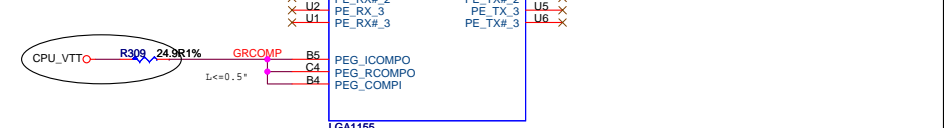


(11) PCH_MEM_PWRGD >> PCH_MEM_PWRGD R91 X R/2 >> MEM_PWRGD

Power On
Hardware default = high

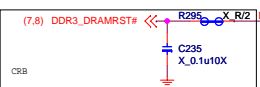
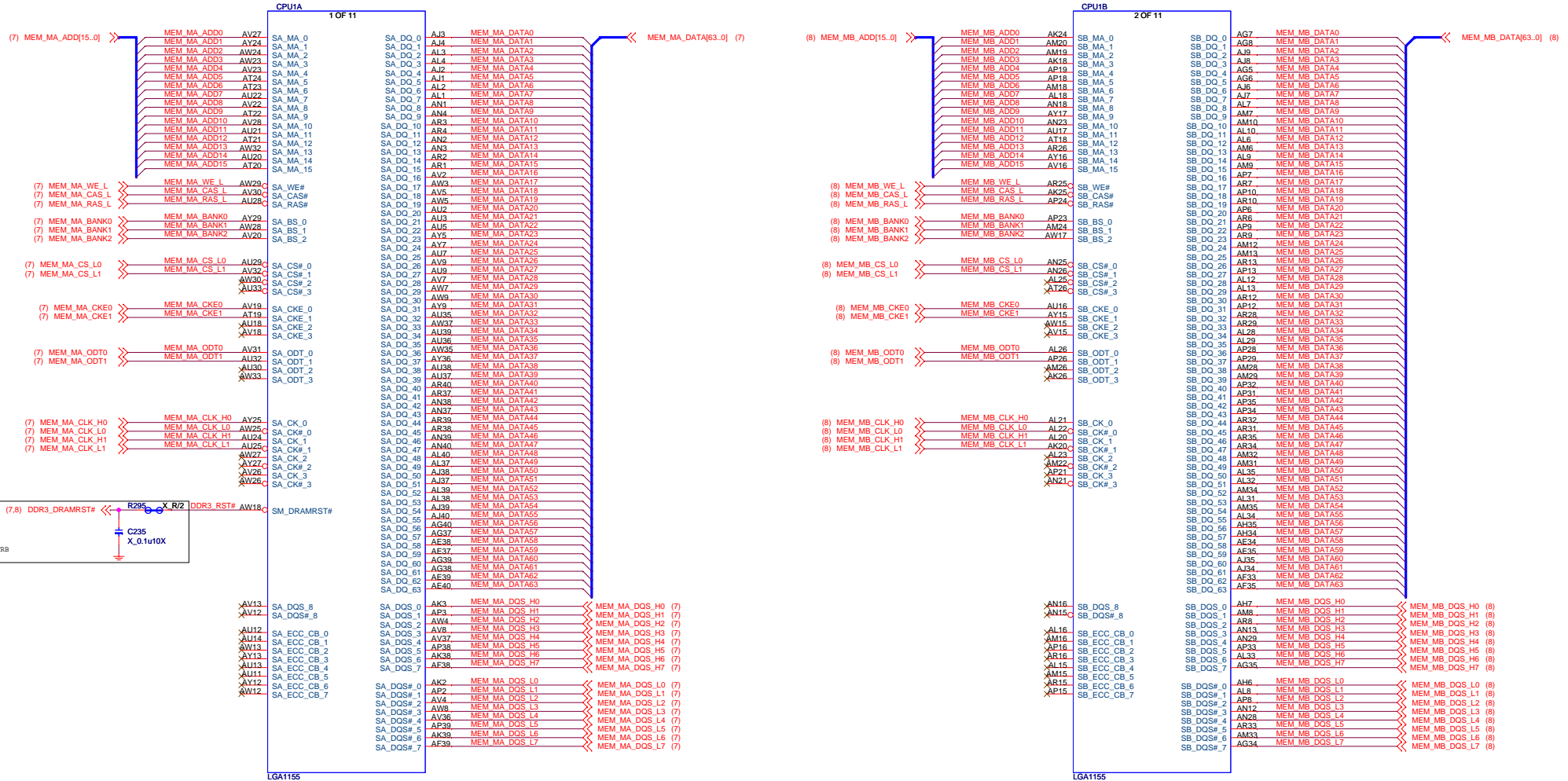
- 1.Set GPIO2_Data = 1
- 2.Set GPIO2 port as output by open-drain mode
- 3.Porting GPIO2_Data = 0 before system into deep_s3
- 4.Waiting CPU_PWRGD from low to high and setting GPIO2_Data = 1 when resume from deep_s3

GPIO2 always keep high except for deep_s3



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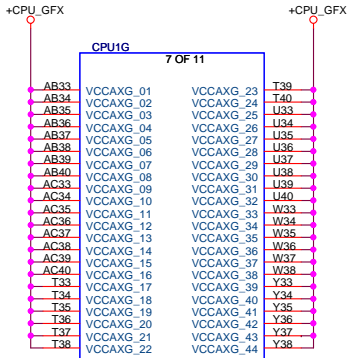
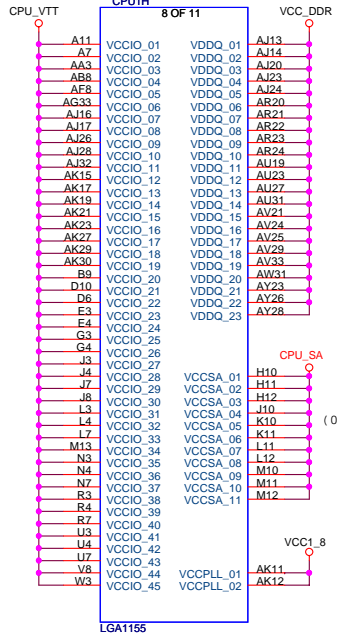
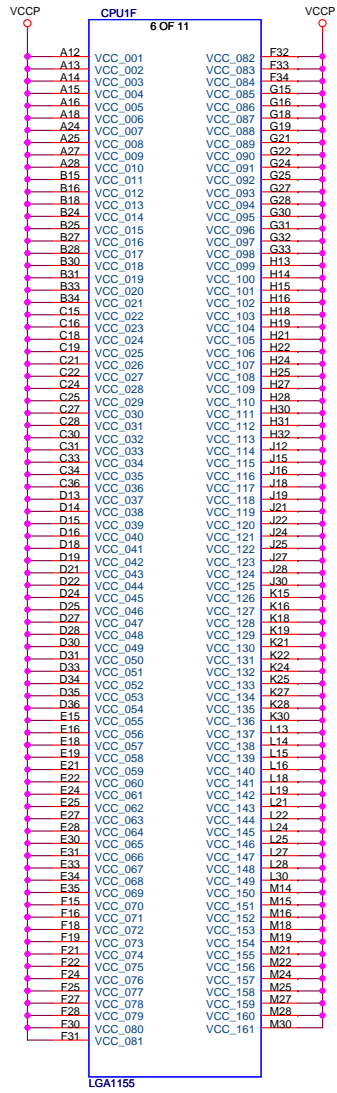


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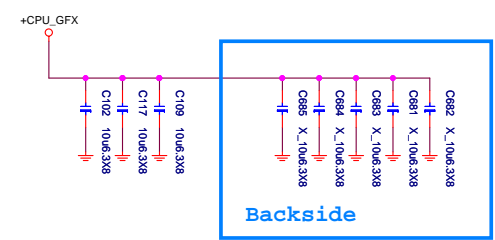
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(1.05V / 1.00V)



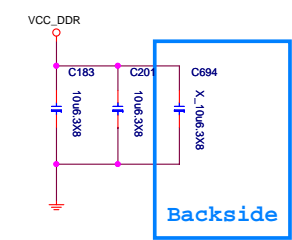
VCCP: 112A
 CPU_VTT: 8.2A
 CPU_SA: 8.8A
 VCC_DDR: 4.5A
 VCC1_8: 1.6A

+CPU_GFX Decoupling

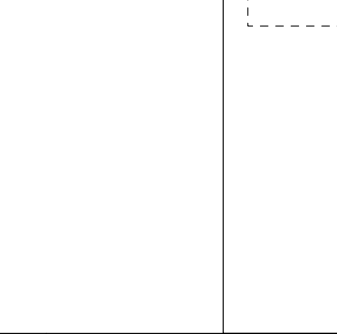
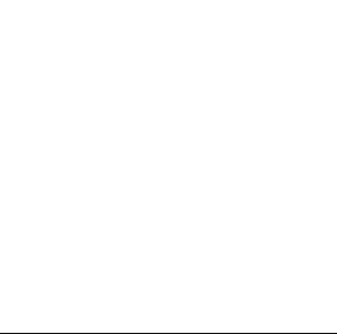
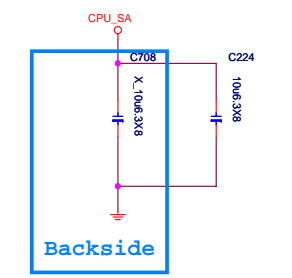


CPU SOCKET CAVITY CAPS

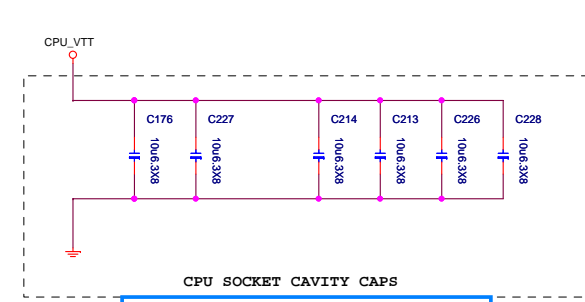
+1.5V_DDR3-Decoupling



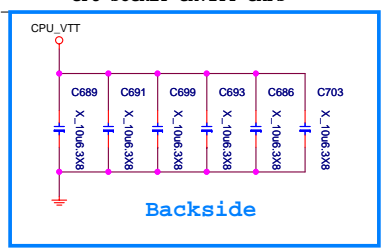
CPU SOCKET CAVITY CAPS



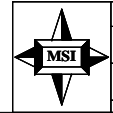
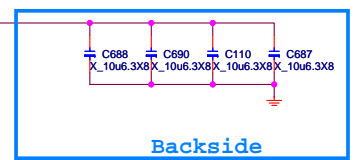
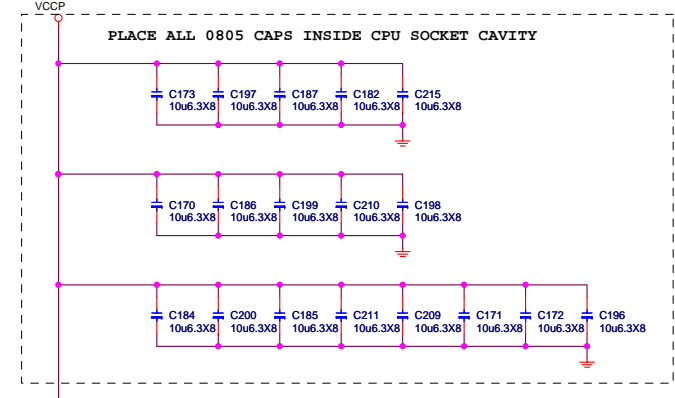
+CPU_VTT Decoupling



CPU SOCKET CAVITY CAPS



+CPU_VCCP-Decoupling

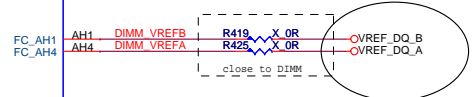


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CPU11 9 OF 11			
A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA31	VSS_006	VSS_096	AM8
AA34	VSS_007	VSS_097	AM39
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM6
AA38	VSS_011	VSS_101	AN10
AA6	VSS_012	VSS_102	AN11
AB5	VSS_013	VSS_103	AN14
AC1	VSS_014	VSS_104	AN17
AC6	VSS_015	VSS_105	AN19
AD33	VSS_016	VSS_106	AN22
AD36	VSS_017	VSS_107	AN24
AD38	VSS_018	VSS_108	AN27
AD39	VSS_019	VSS_109	AN30
AD40	VSS_020	VSS_110	AN31
AD5	VSS_021	VSS_111	AN32
AD8	VSS_022	VSS_112	AN33
AE	VSS_023	VSS_113	AN34
AE33	VSS_024	VSS_114	AN35
AE36	VSS_025	VSS_115	AN36
AF1	VSS_026	VSS_116	AN5
AF34	VSS_027	VSS_117	AN6
AF37	VSS_028	VSS_118	AN8
AF40	VSS_029	VSS_119	AN9
AF5	VSS_031	VSS_121	AP1
AF6	VSS_032	VSS_122	AP11
AF7	VSS_033	VSS_123	AP14
AG36	VSS_034	VSS_124	AP17
AH2	VSS_035	VSS_125	AP22
AH3	VSS_036	VSS_126	AP25
AH34	VSS_037	VSS_127	AP27
AH36	VSS_038	VSS_128	AP30
AH37	VSS_039	VSS_129	AP36
AH38	VSS_040	VSS_130	AP37
AH39	VSS_041	VSS_131	AP4
AH40	VSS_042	VSS_132	AP40
AH5	VSS_043	VSS_133	AP5
AH8	VSS_044	VSS_134	AR11
AH12	VSS_045	VSS_135	AR17
AJ18	VSS_046	VSS_136	AR18
AJ21	VSS_048	VSS_138	AR19
AJ25	VSS_049	VSS_139	AR27
AJ27	VSS_050	VSS_140	AR30
AJ36	VSS_051	VSS_141	AR36
AJ5	VSS_052	VSS_142	AR5
AK1	VSS_053	VSS_143	AT1
AK14	VSS_054	VSS_144	AT10
AK15	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	AT35
AK8	VSS_072	VSS_162	AT36
AK9	VSS_073	VSS_163	AT37
AL11	VSS_074	VSS_164	AT38
AL14	VSS_075	VSS_165	AT39
AL17	VSS_076	VSS_166	AT4
AL19	VSS_077	VSS_167	AT40
AL24	VSS_078	VSS_168	AT5
AL27	VSS_079	VSS_169	AT6
AL30	VSS_080	VSS_170	AT7
AL36	VSS_081	VSS_171	AT8
AL5	VSS_082	VSS_172	AT9
AM1	VSS_083	VSS_173	AU1
AM11	VSS_084	VSS_174	AU15
AM14	VSS_085	VSS_175	AU26
AM17	VSS_086	VSS_176	AU34
AM2	VSS_087	VSS_177	AU4
AM21	VSS_088	VSS_178	AU6
AM23	VSS_089	VSS_179	AU8
AM25	VSS_090	VSS_180	AV10

CPU1J 10 OF 11			
AV11	VSS_181	VSS_281	H37
AV14	VSS_182	VSS_282	H39
AV17	VSS_183	VSS_283	H5
AV2	VSS_184	VSS_284	H6
AV36	VSS_185	VSS_285	H9
AV38	VSS_186	VSS_286	J11
AV6	VSS_187	VSS_287	J17
AW10	VSS_188	VSS_288	J20
AW11	VSS_189	VSS_289	J23
AW14	VSS_190	VSS_290	J26
AW16	VSS_191	VSS_291	J29
AW36	VSS_192	VSS_292	J32
AW6	VSS_193	VSS_293	K1
AY11	VSS_194	VSS_294	K12
AY14	VSS_195	VSS_295	K13
AY18	VSS_196	VSS_296	K14
AY35	VSS_197	VSS_297	K17
AY4	VSS_198	VSS_298	K2
AY6	VSS_199	VSS_299	K20
AY8	VSS_200	VSS_300	K23
B10	VSS_201	VSS_301	K26
B13	VSS_202	VSS_302	K29
B14	VSS_203	VSS_303	K33
B17	VSS_204	VSS_304	K35
B23	VSS_205	VSS_305	K37
B26	VSS_206	VSS_306	K39
B29	VSS_207	VSS_307	K5
B32	VSS_208	VSS_308	K6
B35	VSS_209	VSS_309	L10
B38	VSS_210	VSS_310	L17
B6	VSS_211	VSS_311	L20
C11	VSS_212	VSS_312	L23
C12	VSS_213	VSS_313	L26
C17	VSS_214	VSS_314	L29
C20	VSS_215	VSS_315	L8
C23	VSS_216	VSS_316	M1
C26	VSS_217	VSS_317	M17
C29	VSS_218	VSS_318	M2
C32	VSS_219	VSS_319	M20
C36	VSS_220	VSS_320	M23
C7	VSS_221	VSS_321	M26
C8	VSS_222	VSS_322	M29
D17	VSS_223	VSS_323	M33
D2	VSS_224	VSS_324	M35
D20	VSS_225	VSS_325	M37
D23	VSS_226	VSS_326	M39
D26	VSS_227	VSS_327	M5
D29	VSS_228	VSS_328	M6
D32	VSS_229	VSS_329	M9
D37	VSS_230	VSS_330	N8
D39	VSS_231	VSS_331	P1
D4	VSS_232	VSS_332	P2
D6	VSS_233	VSS_333	P36
D9	VSS_234	VSS_334	P38
E11	VSS_235	VSS_335	P40
E12	VSS_236	VSS_336	P5
E17	VSS_237	VSS_337	PE
E20	VSS_238	VSS_338	R33
E23	VSS_239	VSS_339	R35
E26	VSS_240	VSS_340	R37
E29	VSS_241	VSS_341	R39
E32	VSS_242	VSS_342	R6
E36	VSS_243	VSS_343	T1
E7	VSS_244	VSS_344	T5
E8	VSS_245	VSS_345	T6
F1	VSS_246	VSS_346	U6
F10	VSS_247	VSS_347	V1
F13	VSS_248	VSS_348	V2
F14	VSS_249	VSS_349	V33
F17	VSS_250	VSS_350	V34
F2	VSS_251	VSS_351	V35
F20	VSS_252	VSS_352	V36
F23	VSS_253	VSS_353	V37
F26	VSS_254	VSS_354	V38
F29	VSS_255	VSS_355	V39
F35	VSS_256	VSS_356	V40
F37	VSS_257	VSS_357	V5
F39	VSS_258	VSS_358	W6
F6	VSS_259	VSS_359	Y5
F9	VSS_260	VSS_360	Y8
G11	VSS_261		
G12	VSS_262		
G14	VSS_263		
G17	VSS_264		
G20	VSS_265		
G23	VSS_266		
G26	VSS_267		
G29	VSS_268		
G34	VSS_269		
G7	VSS_270		
G8	VSS_271		
H1	VSS_272		
H17	VSS_273	VSS_NCTF_01	A4
H2	VSS_274	VSS_NCTF_02	AV39
H20	VSS_275	VSS_NCTF_03	AY37
H23	VSS_276	VSS_NCTF_04	B3
H26	VSS_277		
H29	VSS_278		
H33	VSS_279		
H35	VSS_280		

CPU1K 11 OF 11			
AV1	RSVD_001	RSVD_036	L33
D40	RSVD_002	RSVD_037	L34
AB6	RSVD_003	RSVD_038	L9
AD37	RSVD_004	RSVD_039	M34
AE6	RSVD_005	RSVD_040	N34
AF4	RSVD_007	RSVD_043	P35
AG4	RSVD_008	RSVD_044	P37
AJ11	RSVD_009	RSVD_045	P39
AJ29	RSVD_010	RSVD_046	R34
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AJ31	RSVD_012	RSVD_048	R38
AN20	RSVD_013	RSVD_049	R40
AP20	RSVD_014	RSVD_050	J31
AT11	RSVD_015	RSVD_051	AD34
AT14	RSVD_016	RSVD_052	AD35
AU10	RSVD_017	RSVD_053	K31
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AV34	RSVD_019		
AW2	RSVD_020		
AW34	RSVD_021		
AY10	RSVD_022		
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C79	RSVD_026		
D38	RSVD_027		
H7	RSVD_028		
H8	RSVD_029		
J33	RSVD_030		
J34	RSVD_031	NCTF_01	A38
J9	RSVD_032	NCTF_02	AU40
K34	RSVD_033	NCTF_03	AW38
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LGA1155

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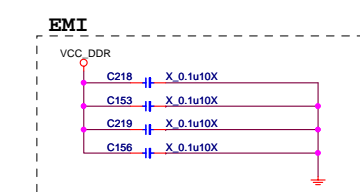
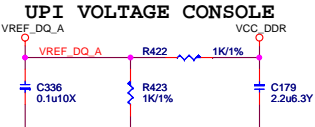
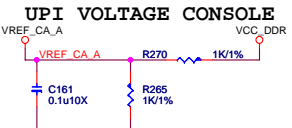
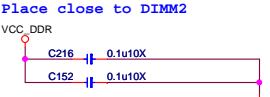
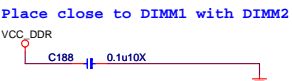
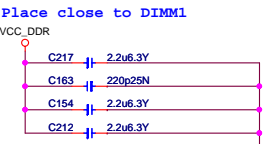
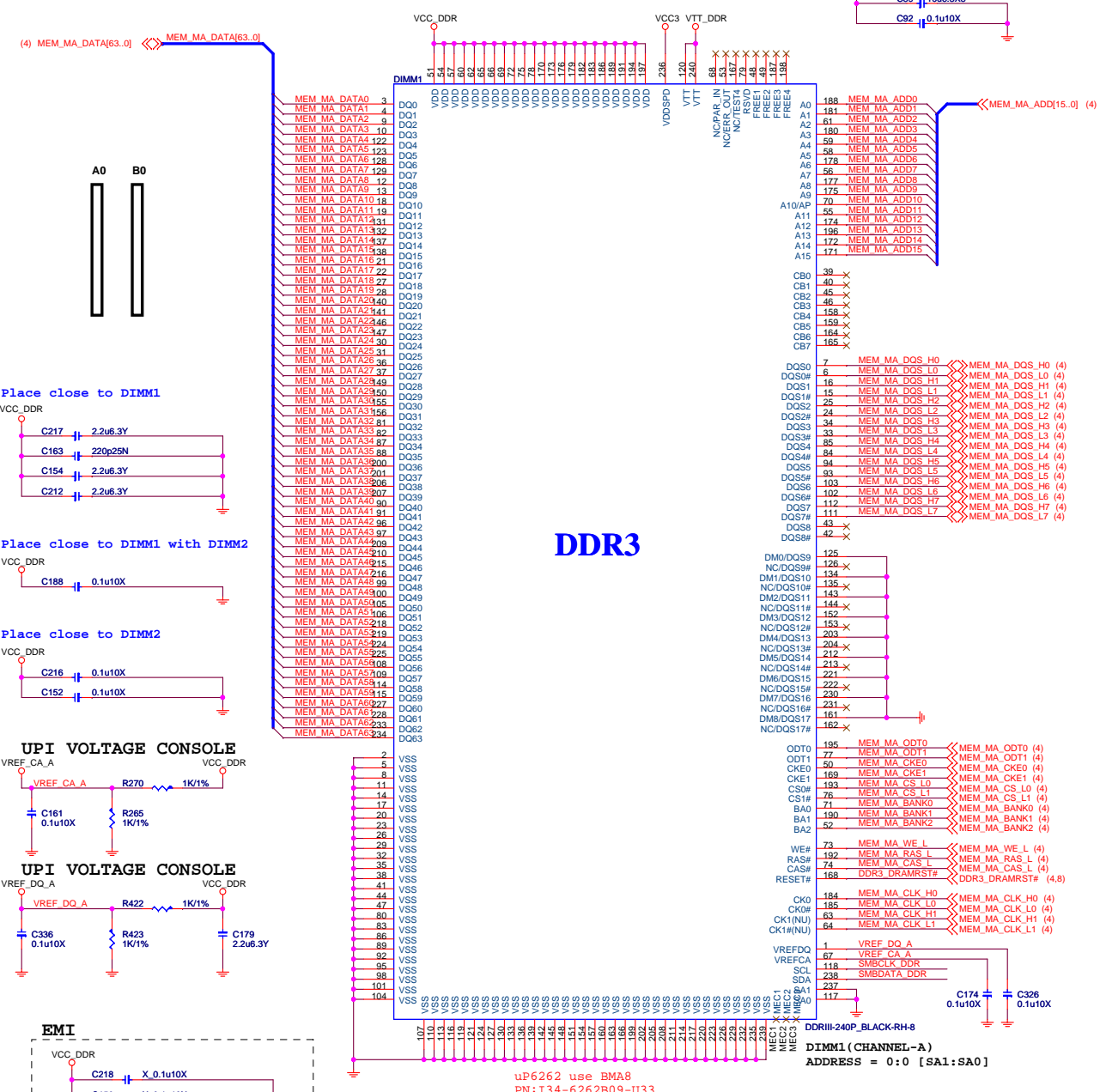
MS-7732

Size: Custom | Document Description: CPU-GND | Rev: 1.1

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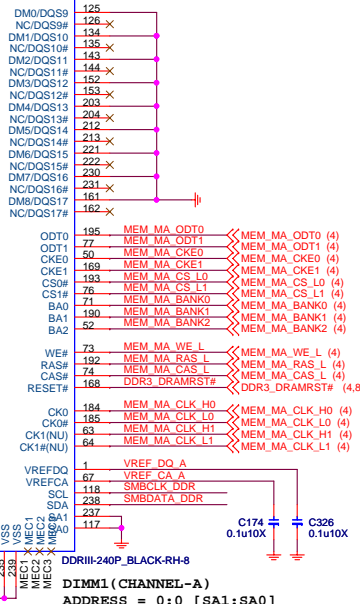
DDRIII DIMM_A0

DDRIII DIMM_A1

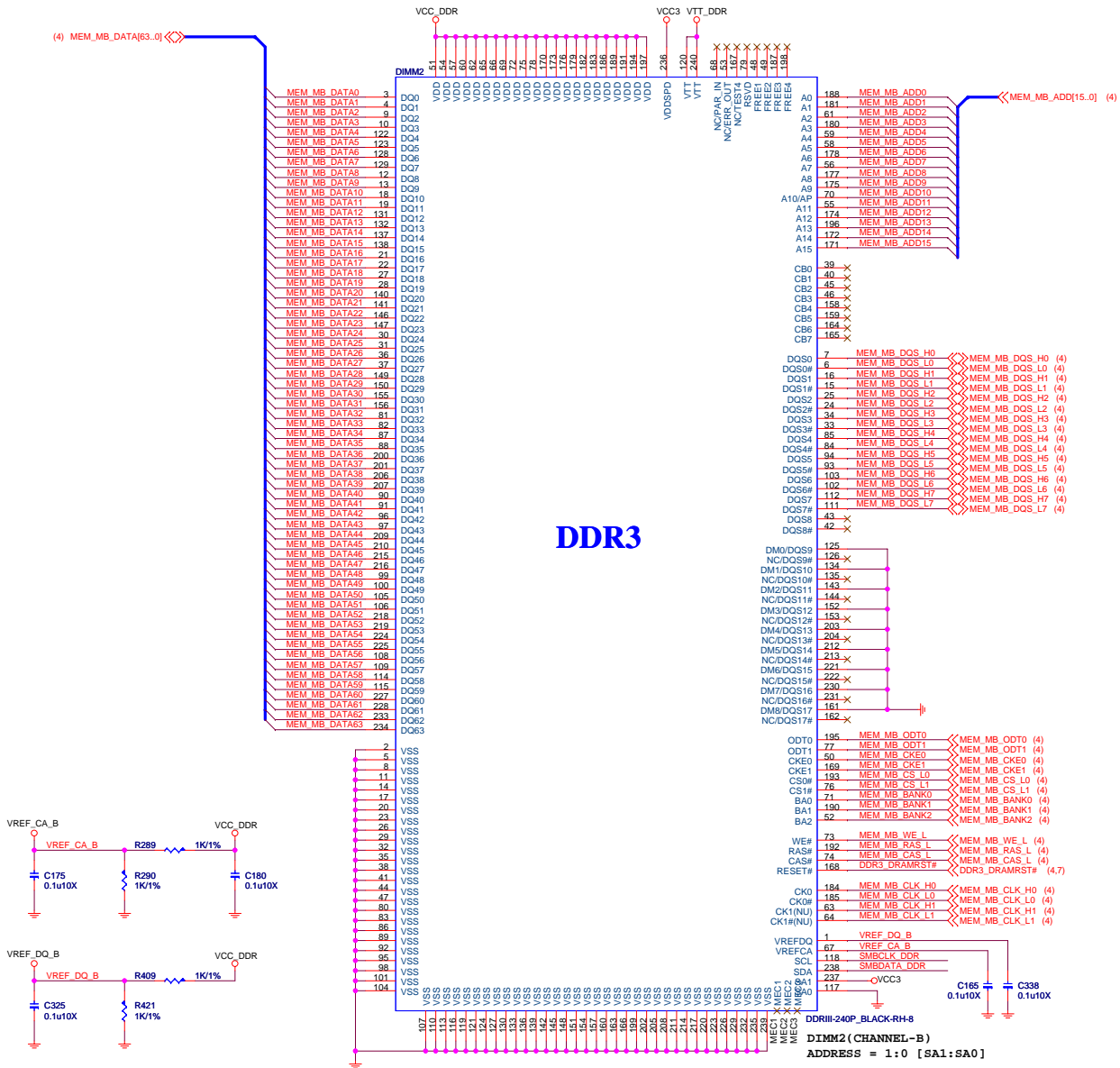


DDR3

uP6262 use BMA8
PN: I34-6262B09-U33



DDR3 DIMM_B0

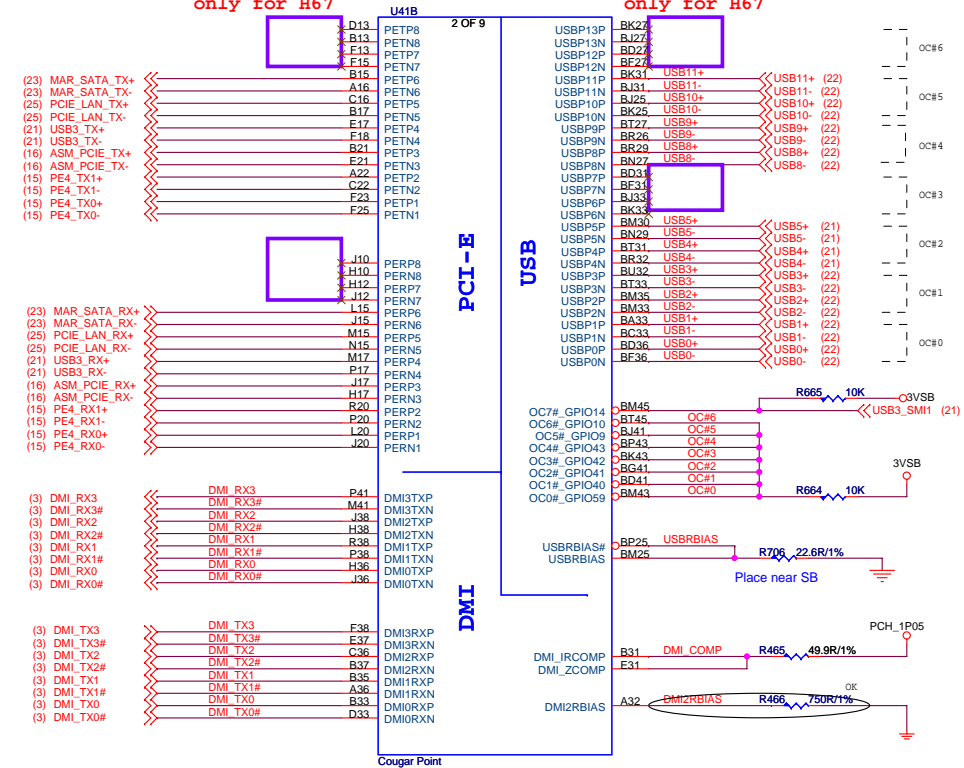


SMBCLK_DDR << SMBCLK_DDR (7)
SMBDATA_DDR << SMBDATA_DDR (7)

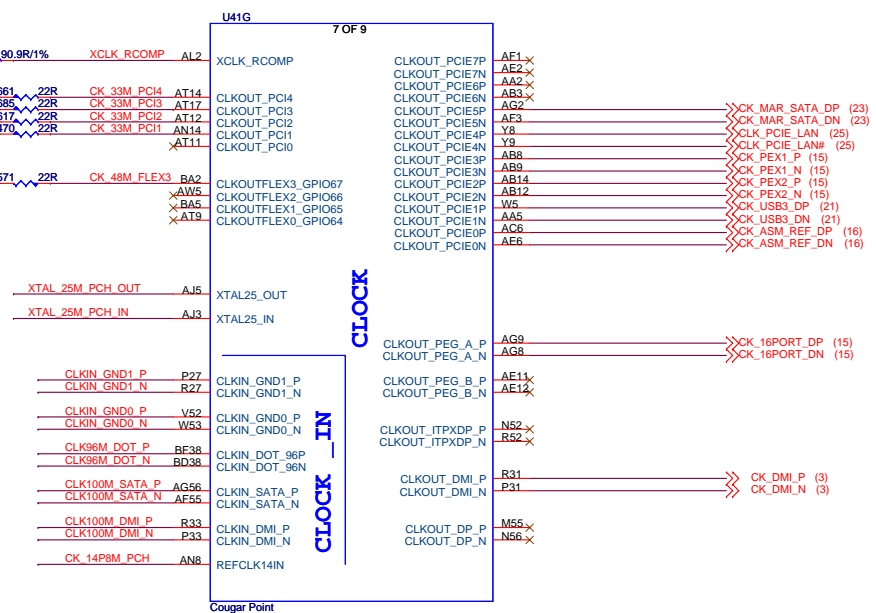
MICRO-STAR INT'L CO.,LTD		
MS-7732		
Size	Document Description	Rev
Custom	DDR III DIMM 3 / DIMM 4	1.1
Date: Tuesday, May 17, 2011	Sheet	8 of 37

only for H67

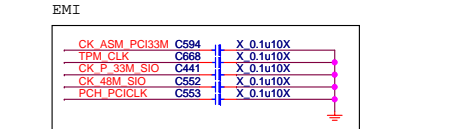
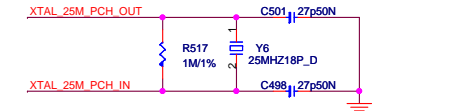
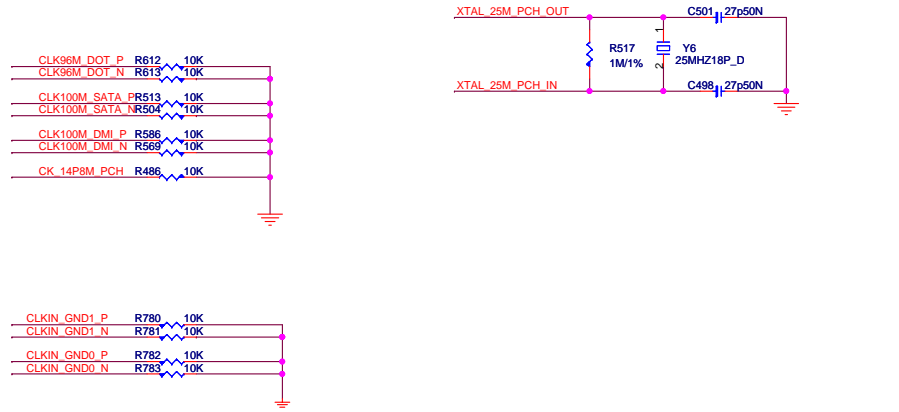
only for H67



Programmable output clock to 48MHZ



no clock gen pull down

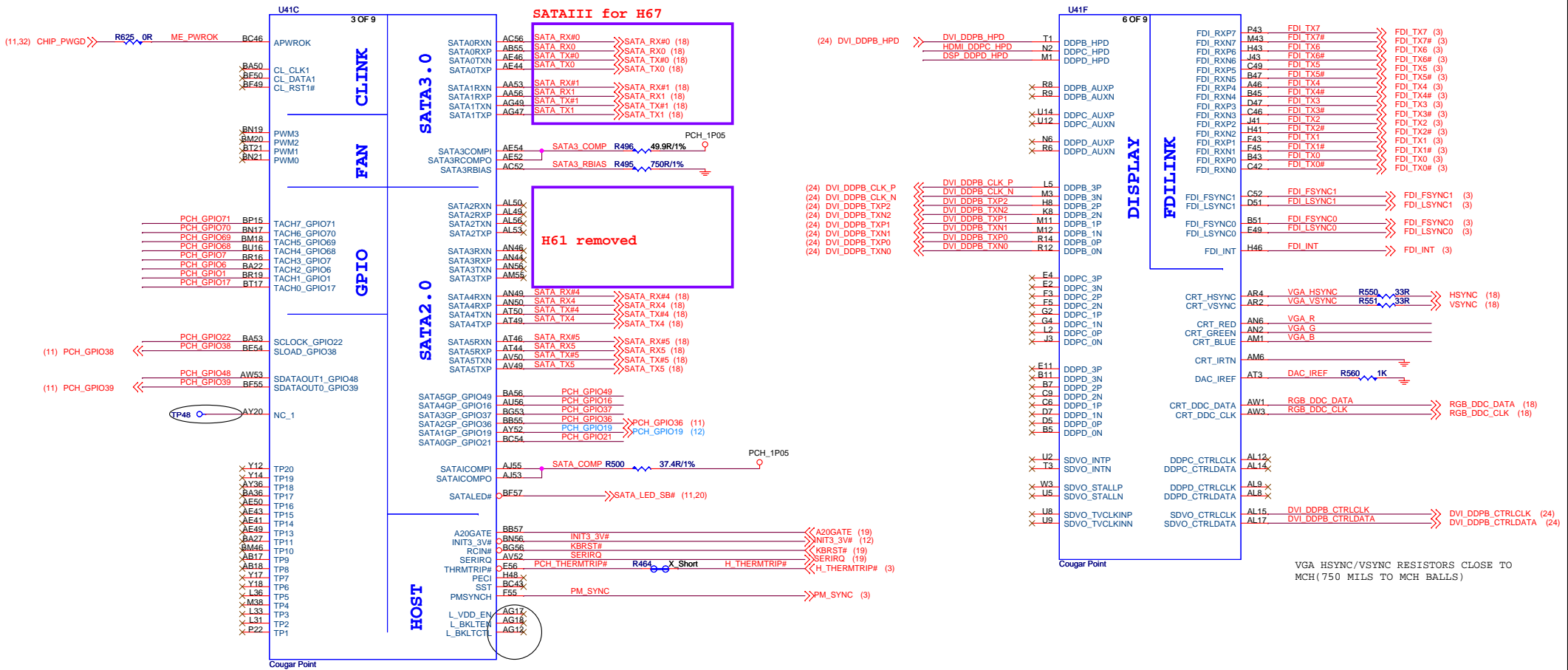


MICRO-STAR INT'L CO.,LTD

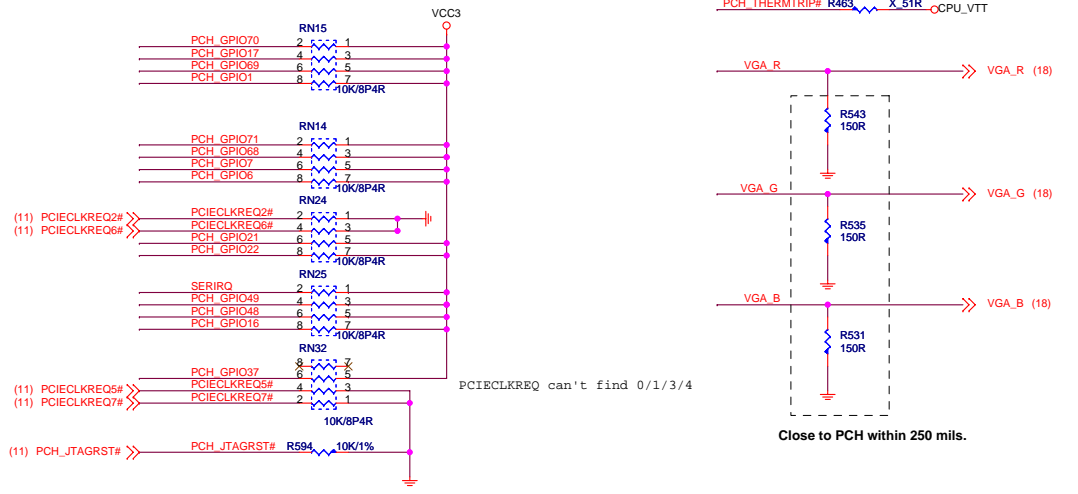
MS-7732

Size Custom Document Description CP-PCI/E/DMI/USB/CLK Rev 1.1

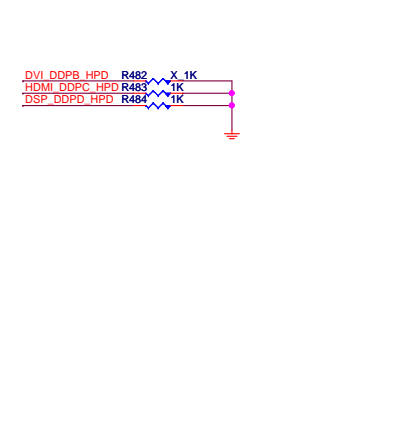
Date: Tuesday, May 17, 2011 Sheet 9 of 37



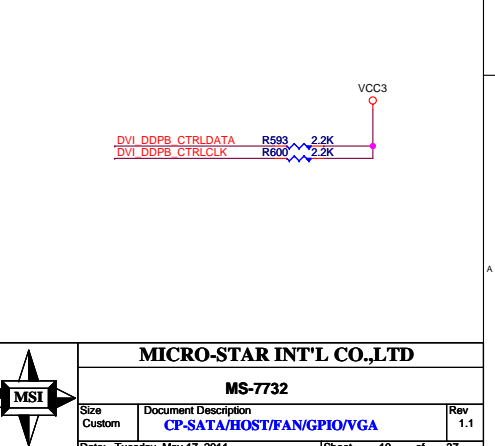
Pull HIGH for PCH



No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)

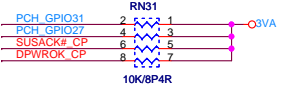
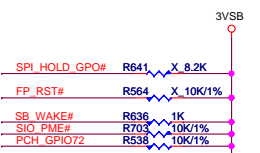
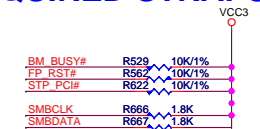


MICRO-STAR INT'L CO.,LTD

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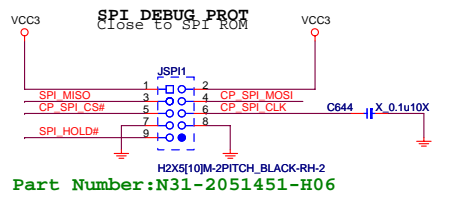
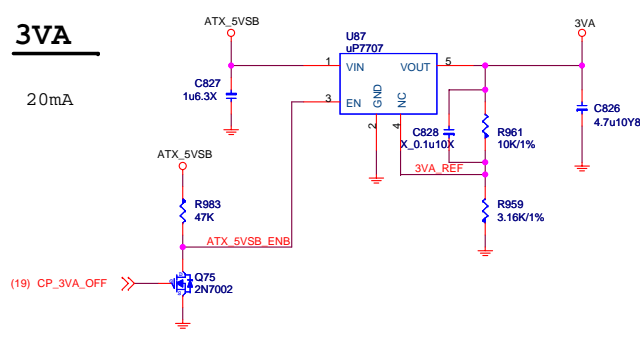
Size Custom	Document Description CP-SATA/HOST/FAN/GPIO/VGA	Rev 1.1
Date: Tuesday, May 17, 2011	Sheet 10 of 37	

REQUIRED STRAPS



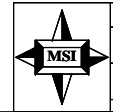
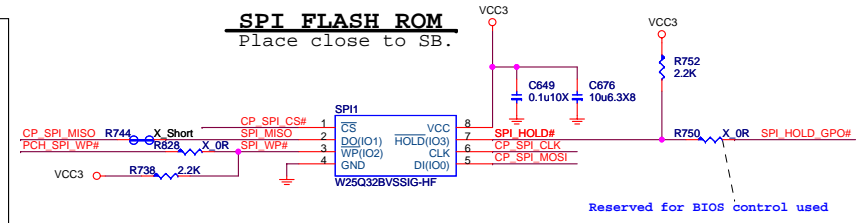
3VA

20mA

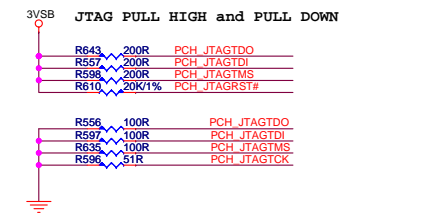
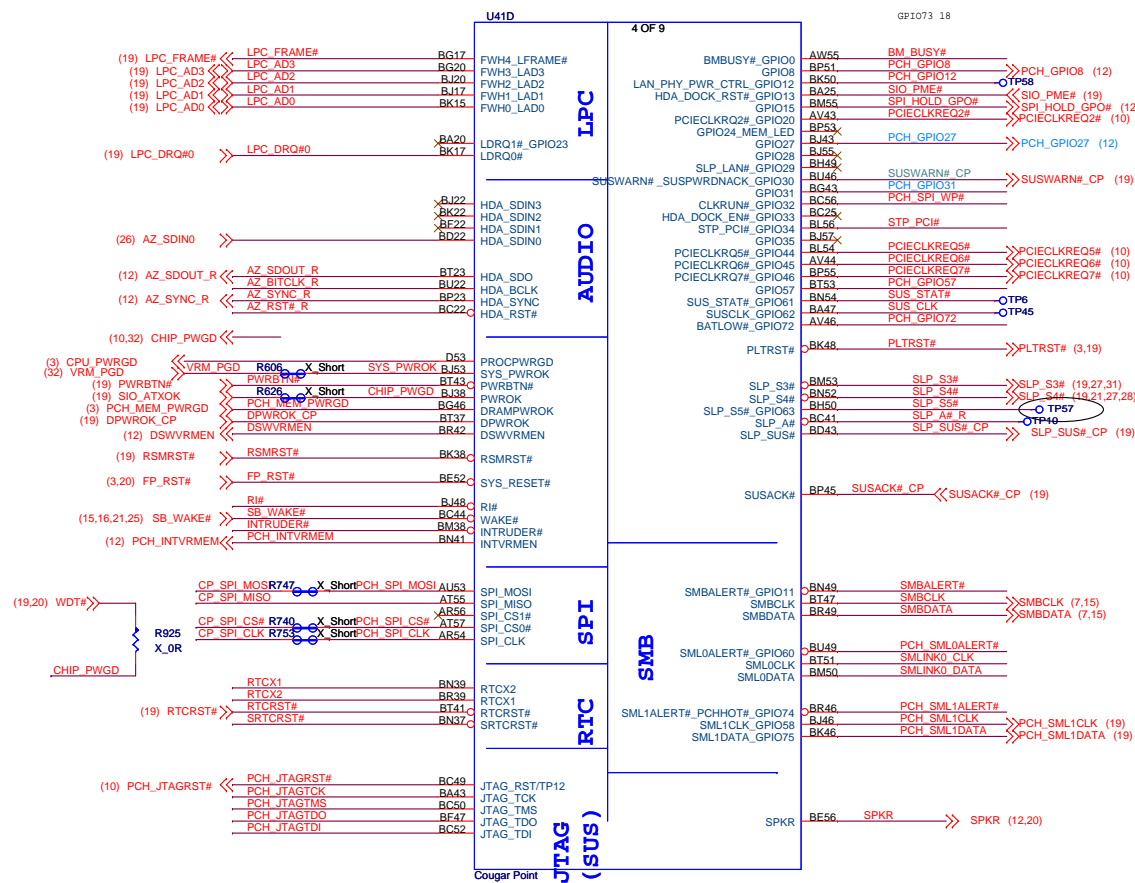


SPI FLASH ROM

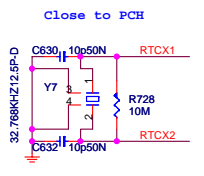
Place close to SB.



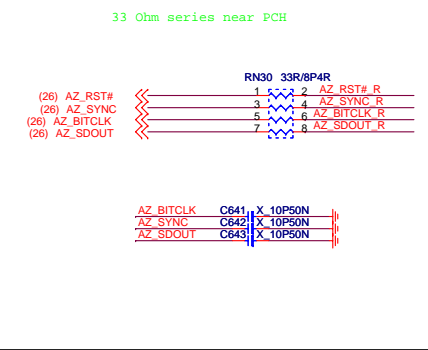
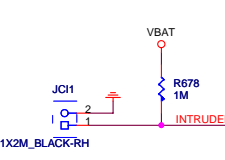
MICRO-STAR INT'L CO.,LTD			
MS-7732			
Size	Document Description	Rev	
Custom	CP-SMB/LPC/AUDIO/RTC	1.1	
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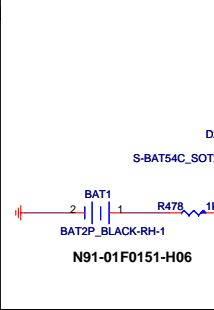
RTC Block



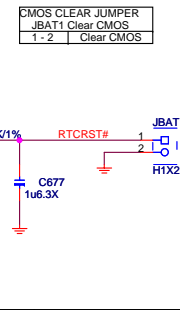
Chassis Intrusion



RTC and CLR_CMOS

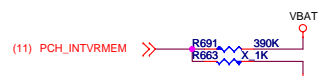
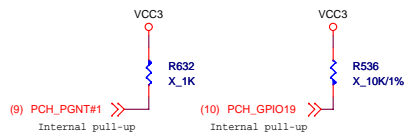


Clear CMOS



PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



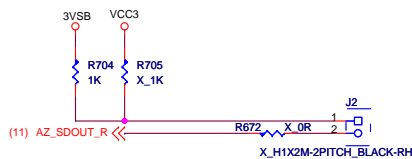
INTVRMEM
 0: DISABLE INTERNAL VRM
 1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



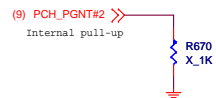
DSWVRMEN
 0 : Disable Internal Deep Sleep 1.05 V regulators.
 1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

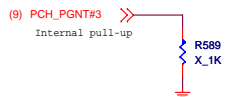


HDA_SDO
 Disable ME in Manufacturing Mode when pull LOW ????

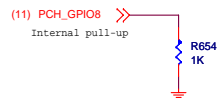
HDA_SDO has internal pull down. Default should be connected to SDIN of codec, no pull up/down. To Disable ME need to have a jumper to pull high



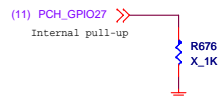
DMI AC/DC MODE
 0 : AC
 1 : DC *



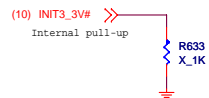
Topblock swap override when pull-low
 Signal has a weak internal pull-up



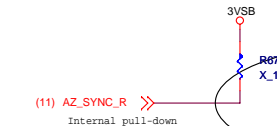
GPIO8
 0 : Integrated Clocking Enable (FCIM) *
 1 : Buffer Through Mode Enable (BTM)



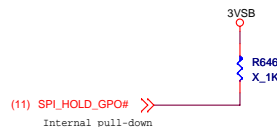
GPIO28
 0 : OD PLL VR disabled
 1 : OD PLL VR enabled *
 Signal has a weak internal pull-up



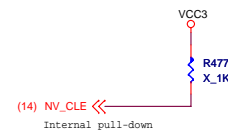
INIT3_3V#
 0 : ??????????????????
 1 : ?????????????????? *



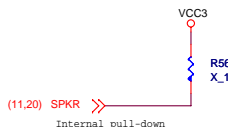
HDA_SYNC
 OD PLL VR SUPPLY SEL
 0: 1.8V SUPPLY *
 1: 1.5V SUPPLY



GPIO15
 0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
 1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



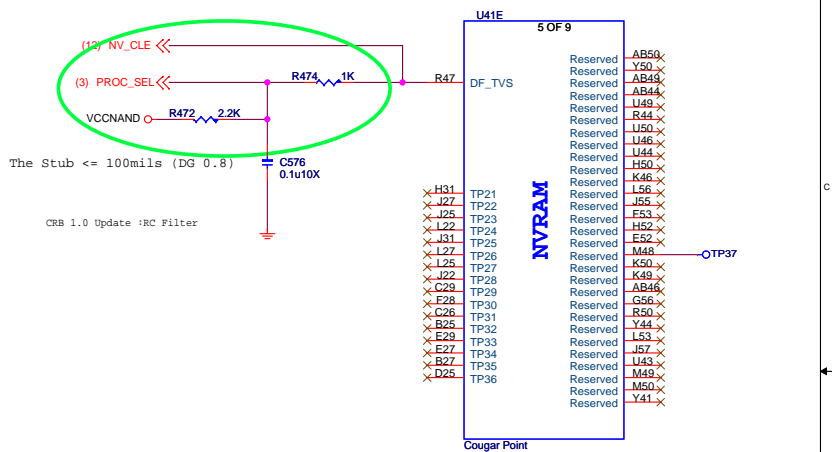
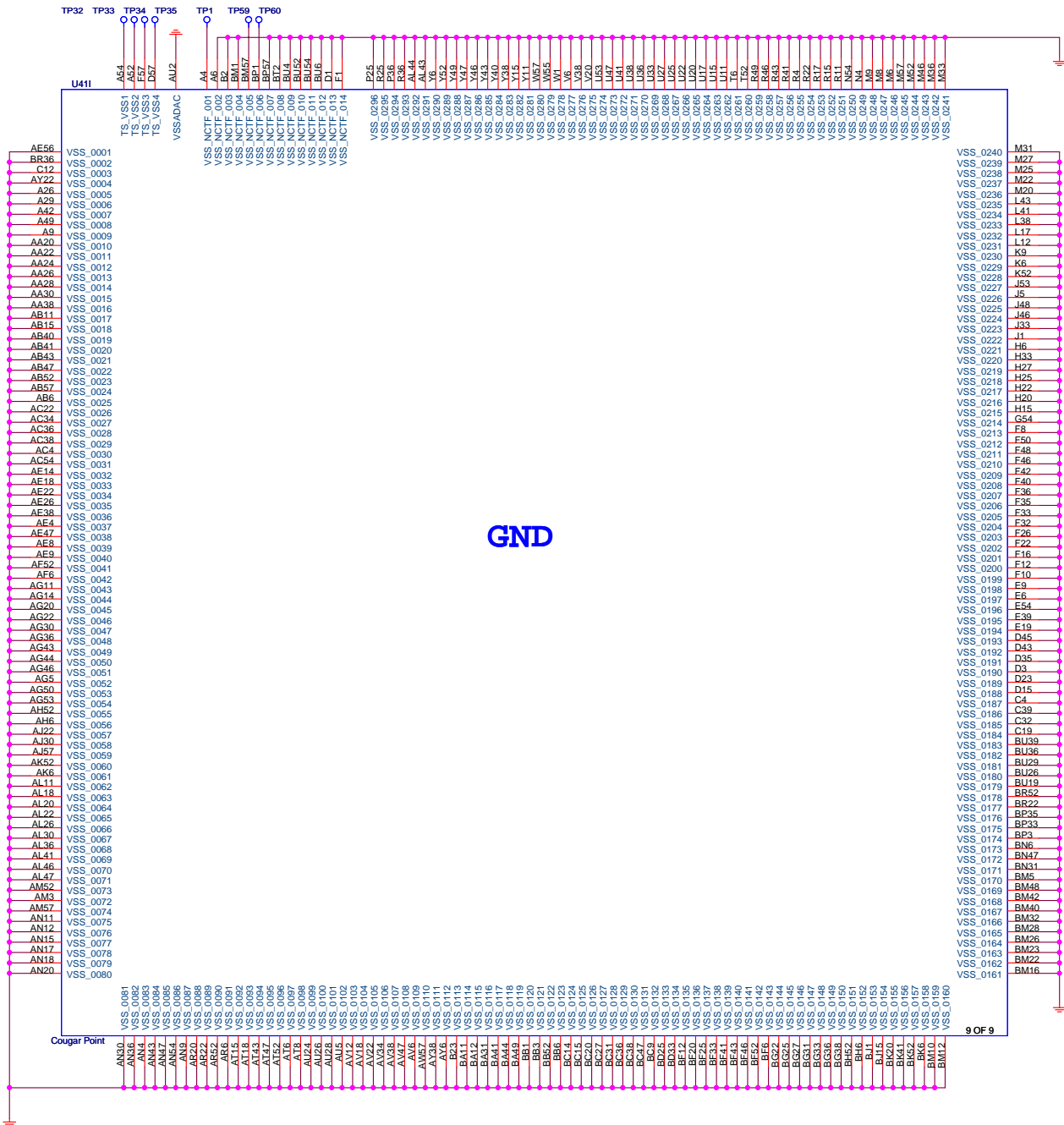
DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
 0 : EN TCO REBOOT *
 1 : DIS TCO REBOOT

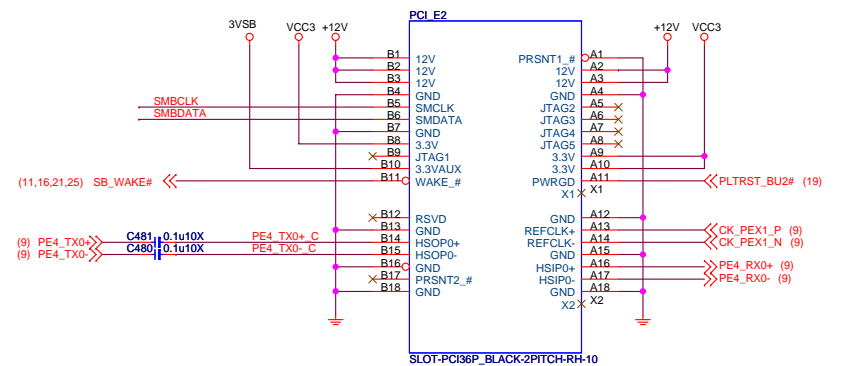
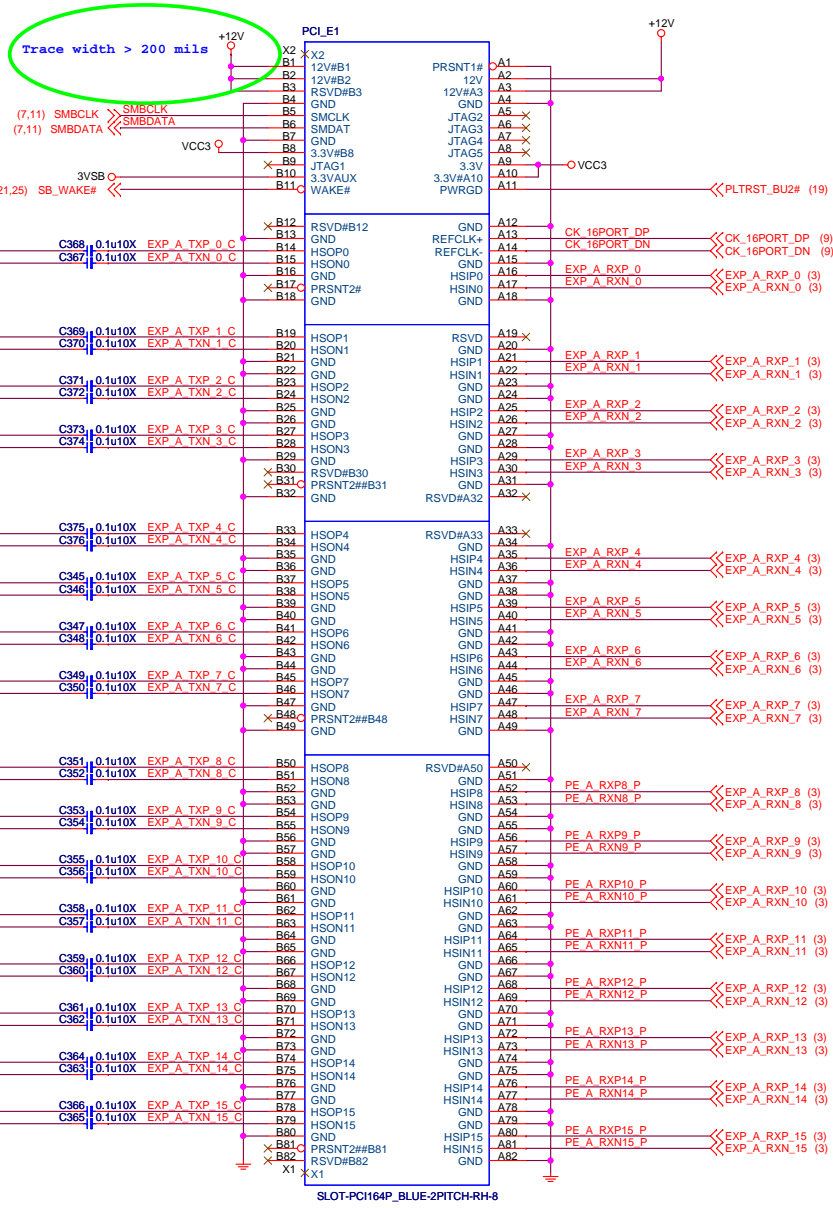
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
 0: Can not to reset the processor.

MICRO-STAR INT'L CO.,LTD		
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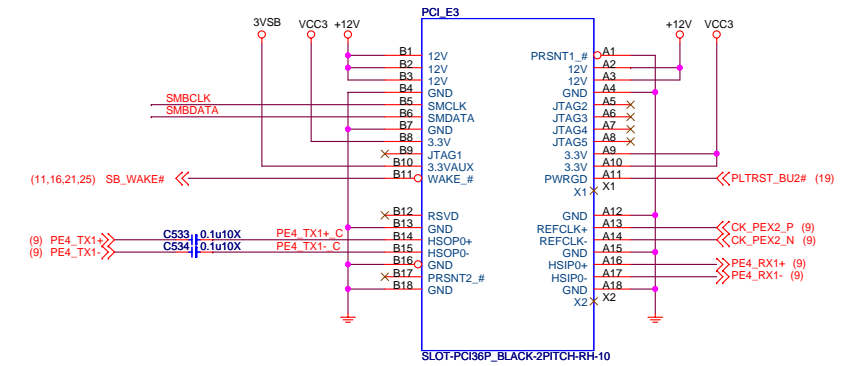


PCI_Express X16 slot

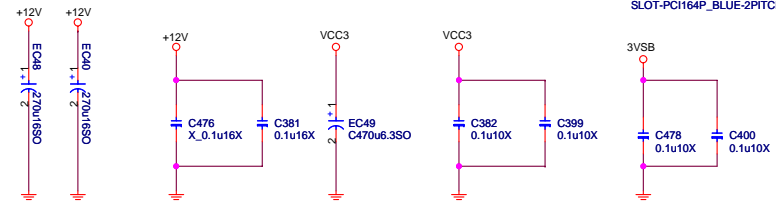
PCI EXPRESS x1-PORT



PCI EXPRESS x1-PORT



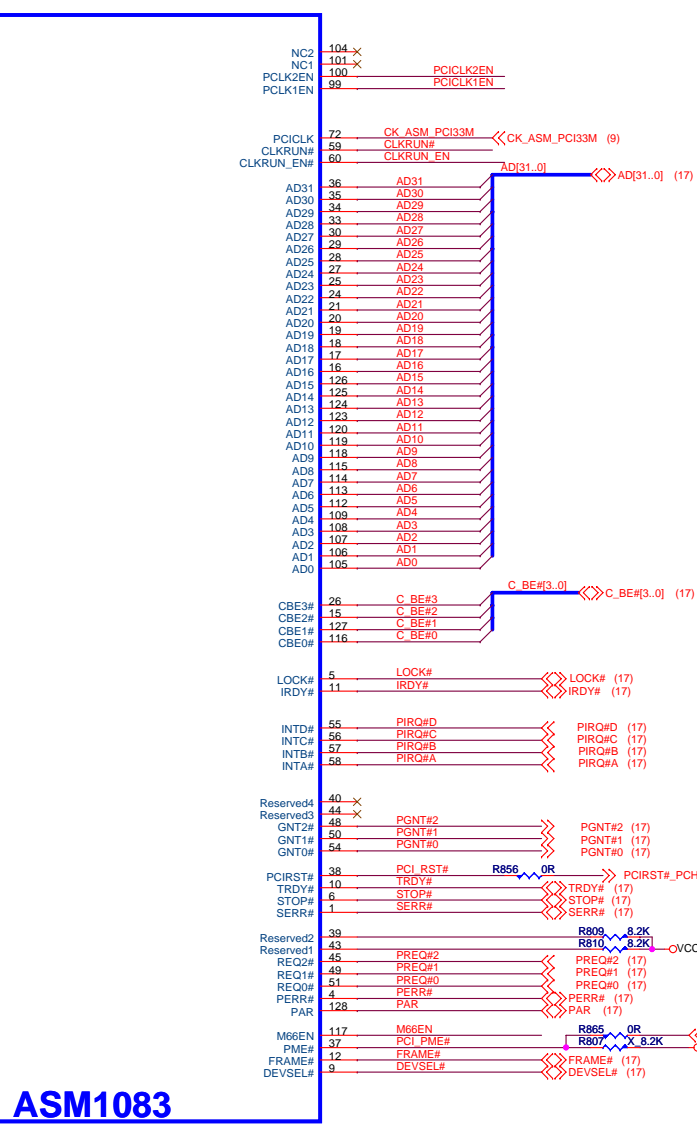
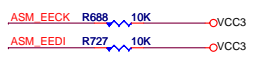
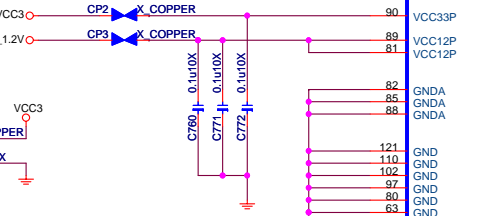
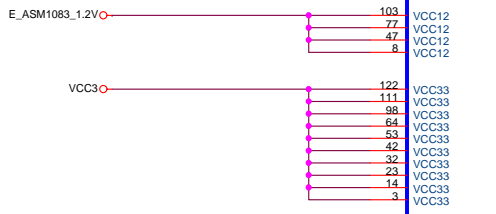
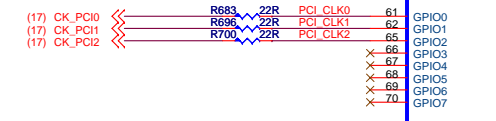
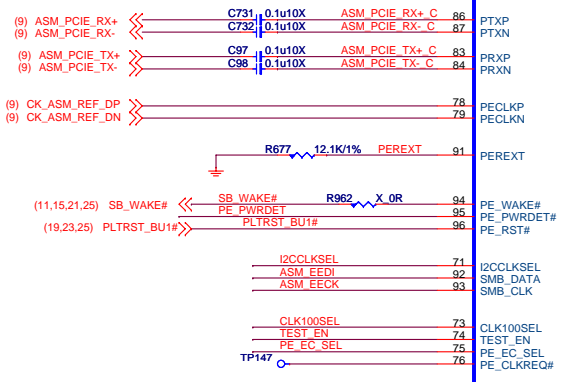
PCI Express X16 slot(X1)	
+12V	- 5.5 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A
PCI Express X1 slot (X2)	
+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A



MICRO-STAR INT'L CO.,LTD

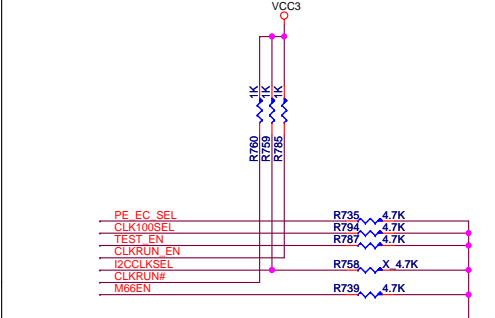
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ASM1083

H/W Strapping



PE_EC_SEL-
 "H" for Express Card mode
 "L" for PCIe Riser Card mode

CLK100SEL-
 "H" for PECLK input only
 "L" for PECLK & PCICLK input

TEST_EN-
 "H" for Test Mode Enable
 "L" for Test Mode Disable

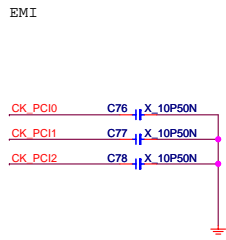
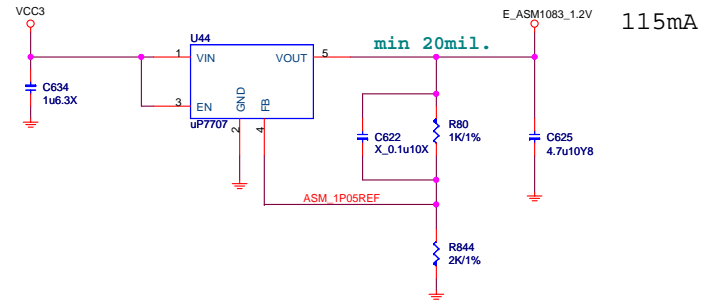
CLKRUN_EN-
 "H" for CLKRUN Mode Disable
 "L" for CLKRUN Mode Enable

I2CCLKSEL-
 "H" is 135KHz I2CCLK
 "L" is 67.5KHz I2CCLK

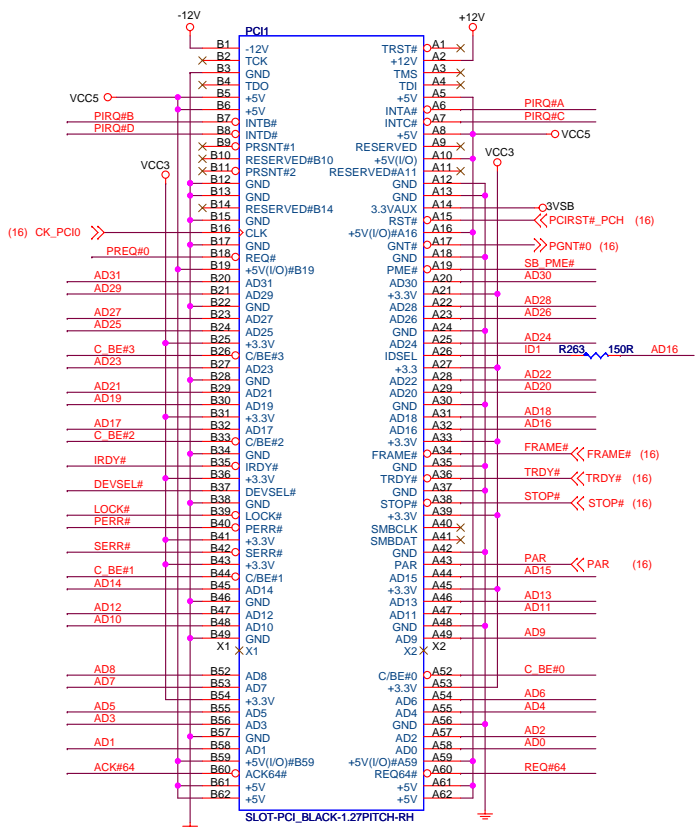


MICRO-STAR INT'L CO.,LTD		
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Custom	ASM1083 PCI Bri.	1.1
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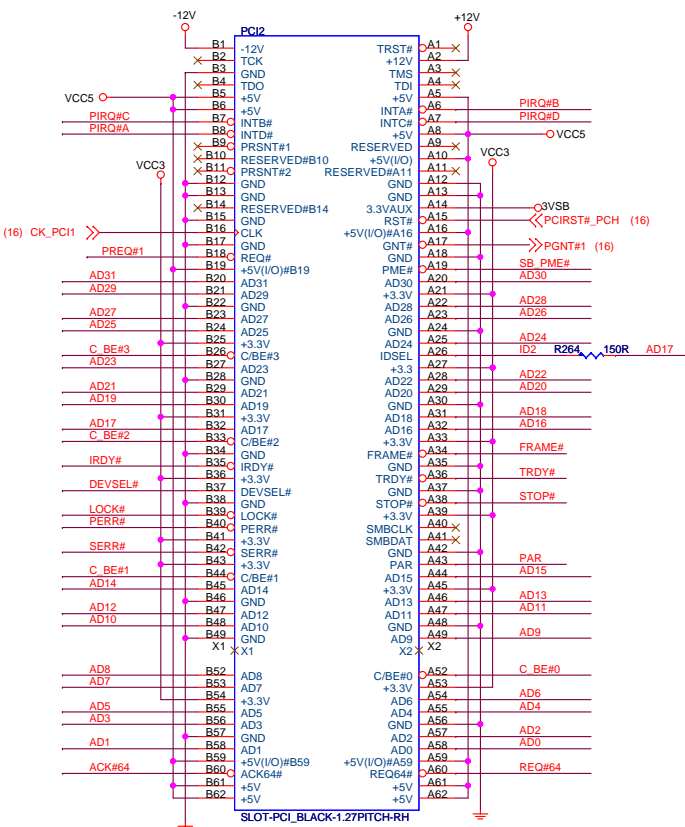
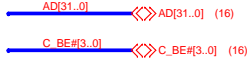
remove EEPROM



E MI

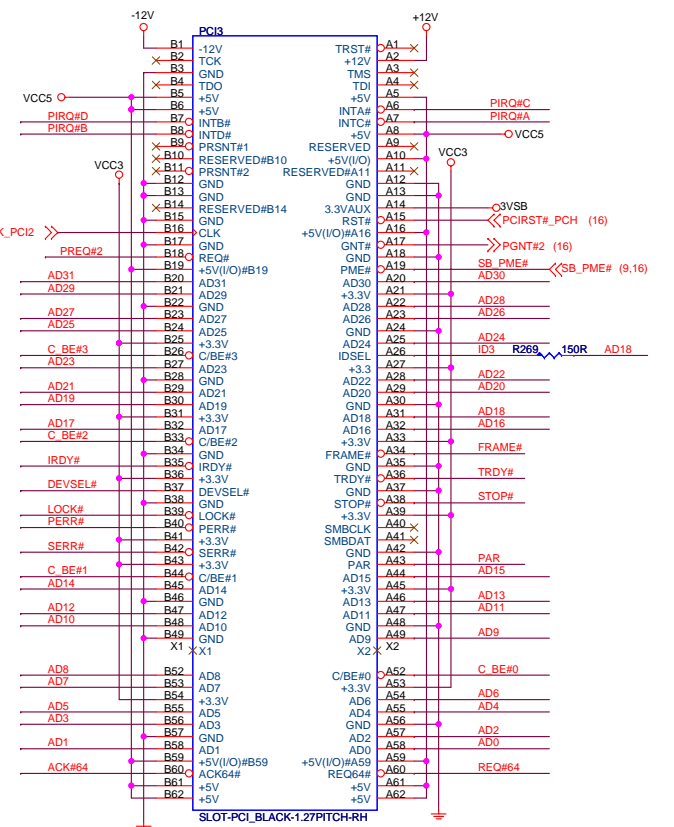
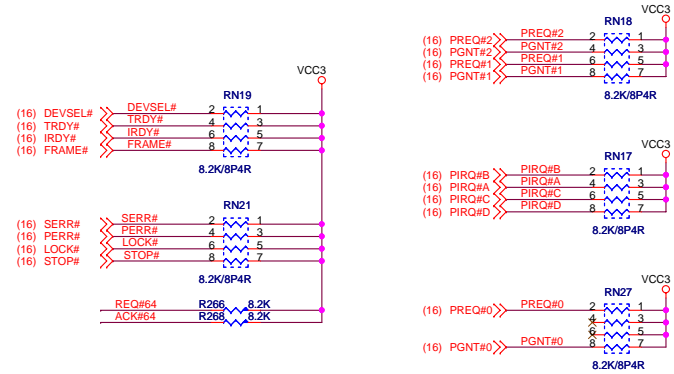


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



IDSEL = AD18
MASTER = PREQ#2
PIRQ#C

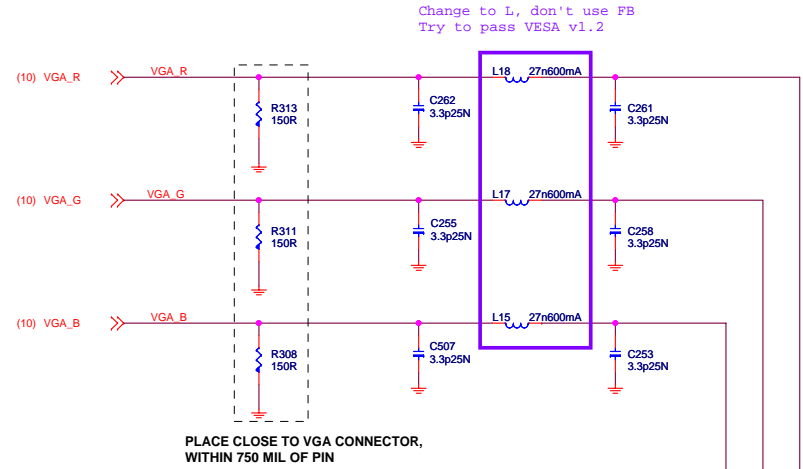
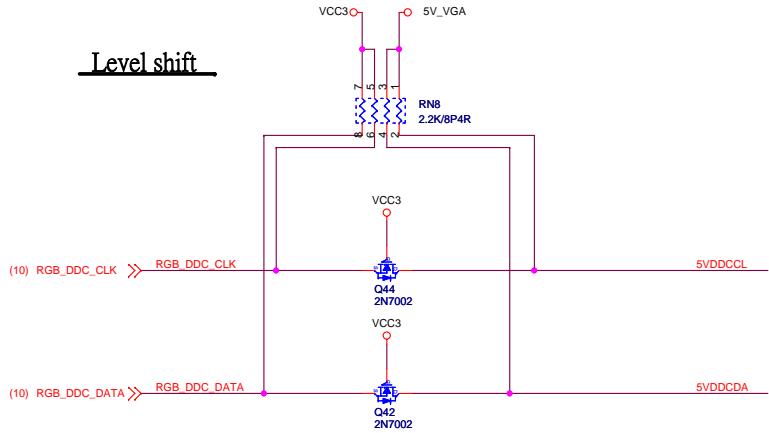
PCI slot (X3)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A



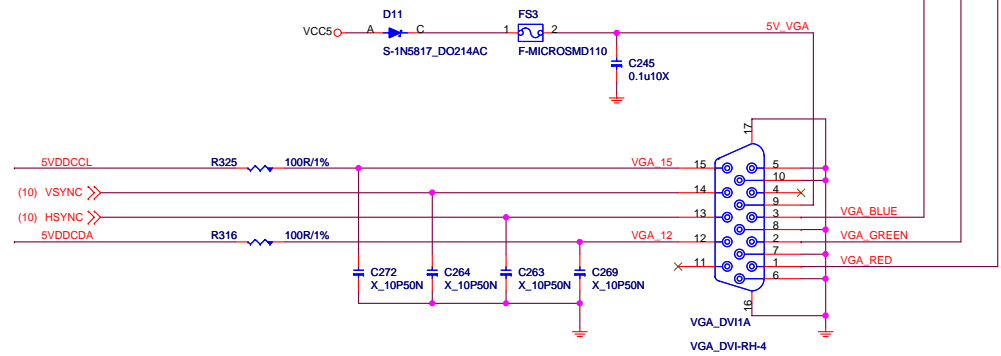
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



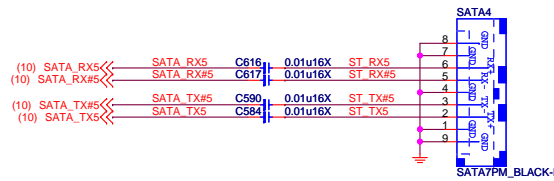
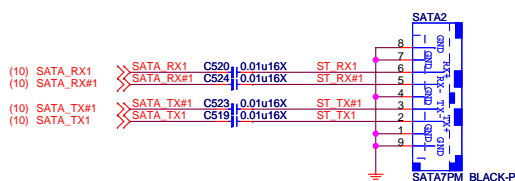
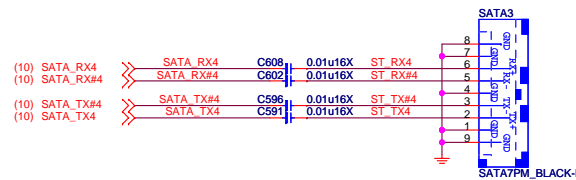
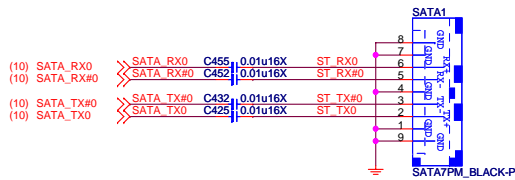
PLACE CLOSE TO VGA CONNECTOR, WITHIN 750 MIL OF PIN



H67 SATA 6G PORT 0,1

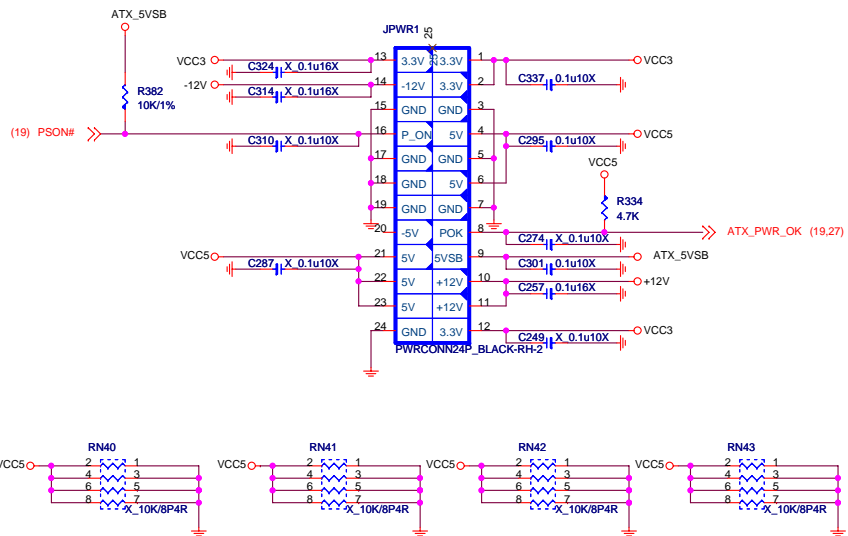
H61 PORT 0/1 Support 3G

SATA 3G PORT 4,5

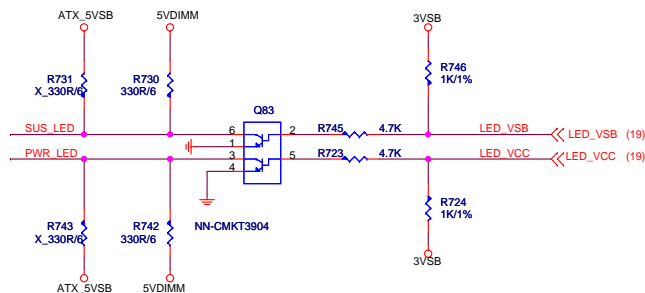


	MICRO-STAR INT'L CO.,LTD	
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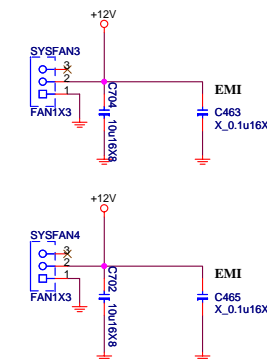
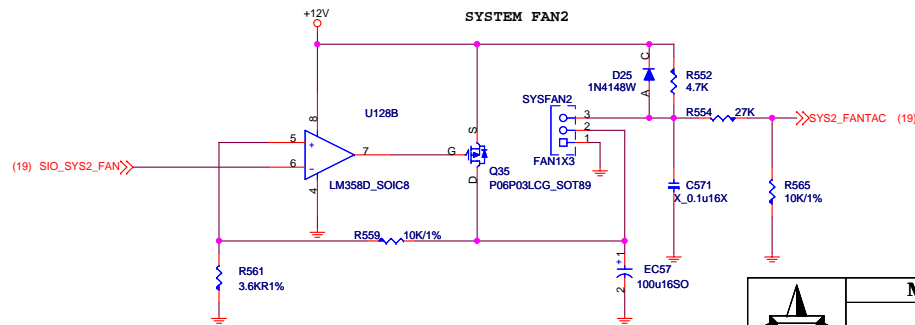
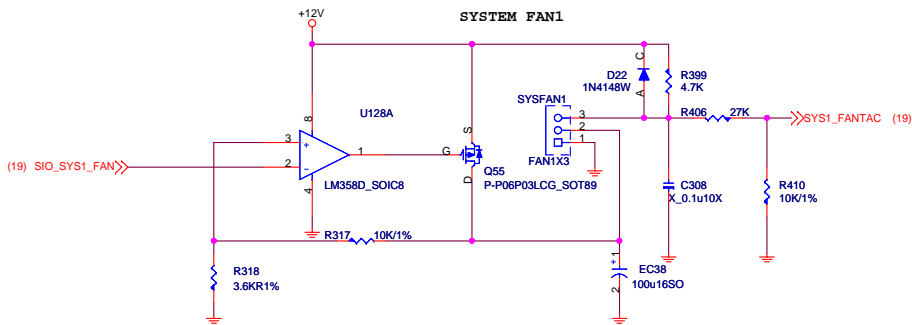
ATX POWER CONNECTOR



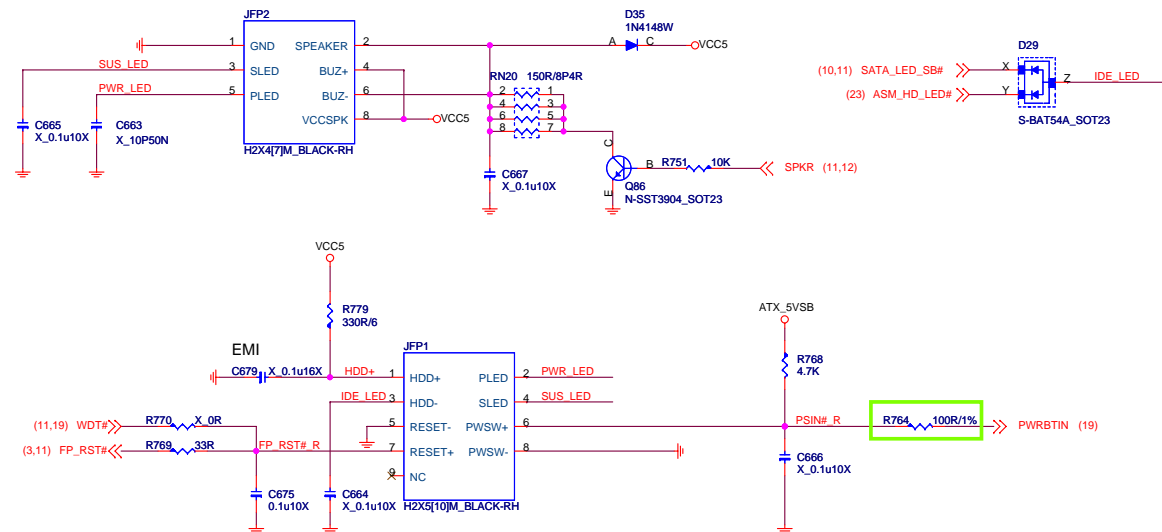
LED (for Fintek 71869)



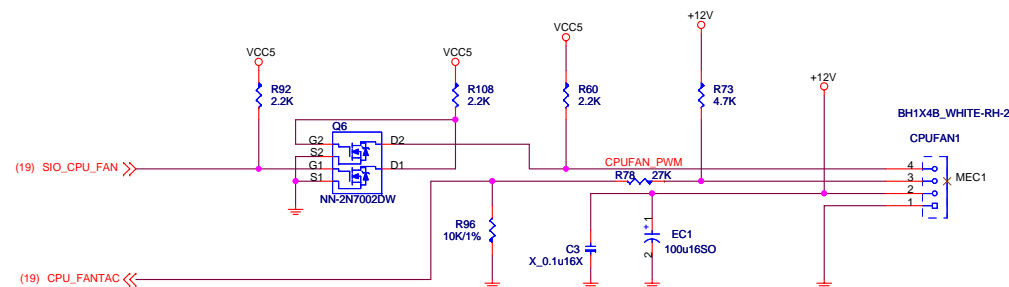
SYSTEM FAN-CONTROL CIRCUIT



FRONT PANEL



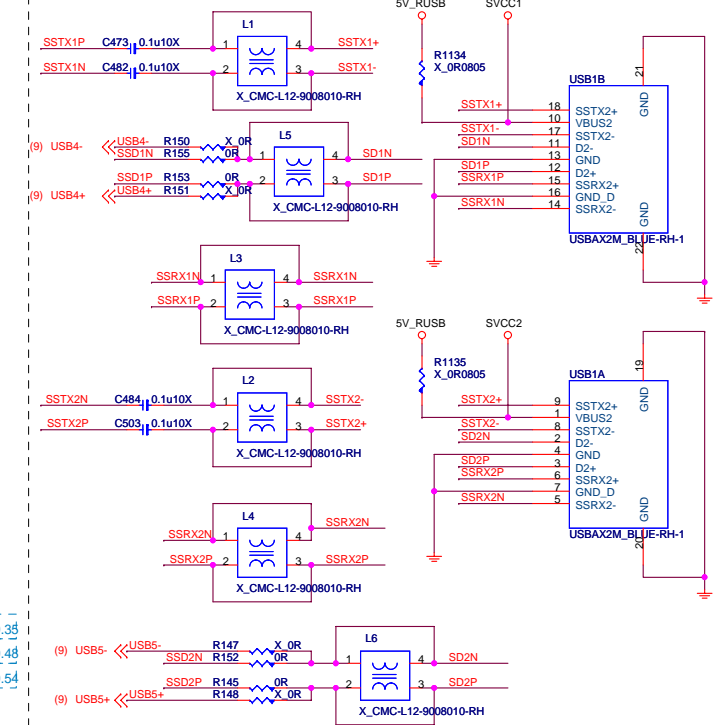
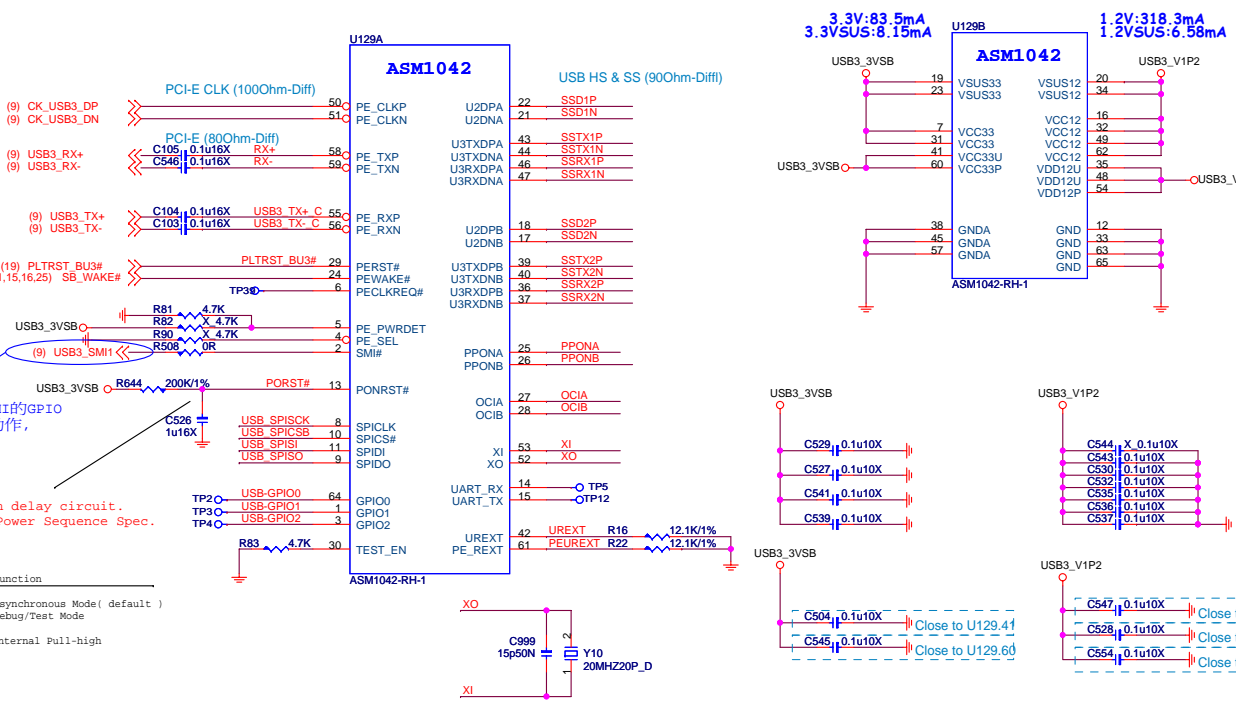
CPU FAN-CONTROL CIRCUIT



MICRO-STAR INT'L CO.,LTD		
MS-7732		
Size Custom	Document Description ATX PWR-Connector & Front Panel & EMI	Rev 1.1
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ASM1042 USB3.0

Rear USB3 CONN



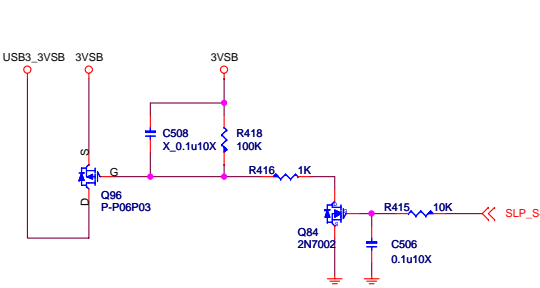
拉出接至SB有支援SMI的GPIO
且由於此pin為low動作，
所以SB端需pull hi

Please self-design delay circuit.
PORST# Must meet Power Sequence Spec.

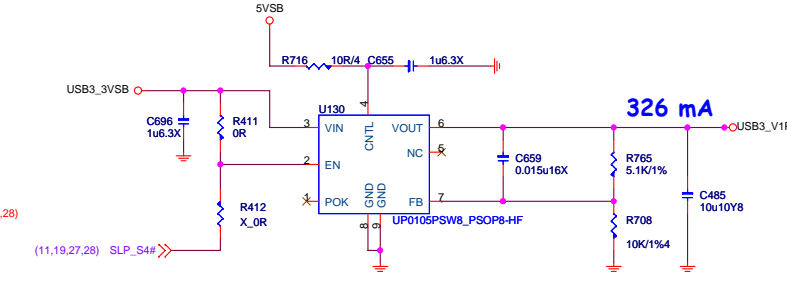
GPIO0	GPIO1	GPIO2	Function
1	1	0	Asynchronous Mode(default)
1	1	1	Debug/Test Mode
0	0	x	

* GPIO0 GPIO1 GPIO2 internal Pull-high

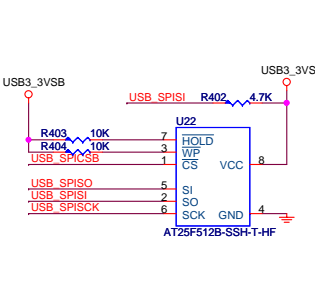
ASM1042 3VSB Circuit



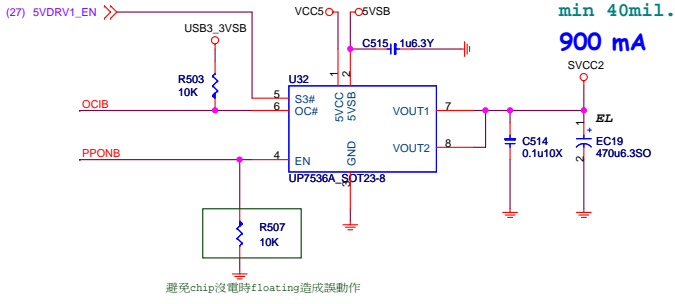
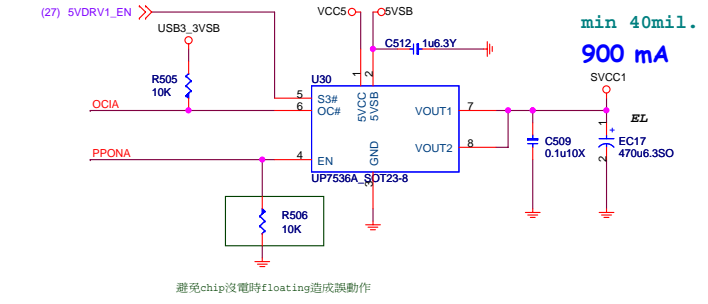
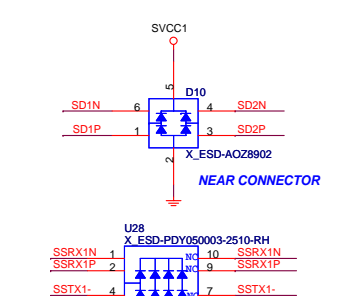
ASM1042 1.2VSB Power



EEPROM



ESD Protection



避免chip沒電時floating造成誤動作

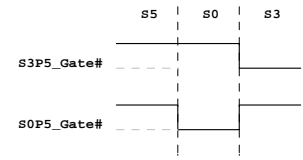
避免chip沒電時floating造成誤動作

MICRO-STAR INT'L CO.,LTD

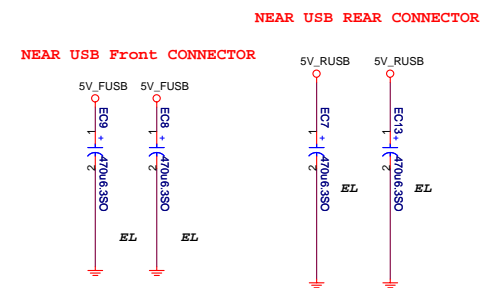
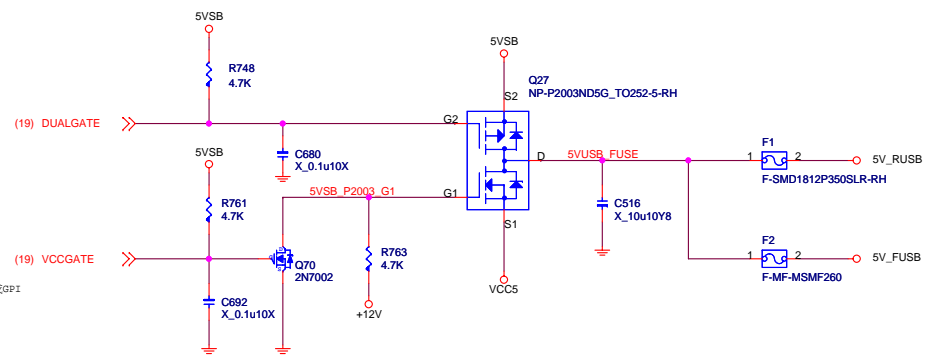
MS-7732

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5V_RUSB Switch



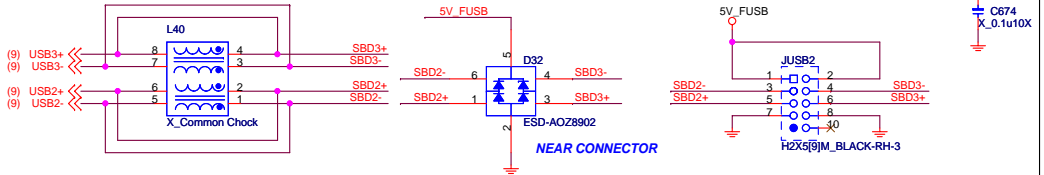
如果S3底下USB要沒電,請S10S進入S3之後將DUALGATE po成GP1



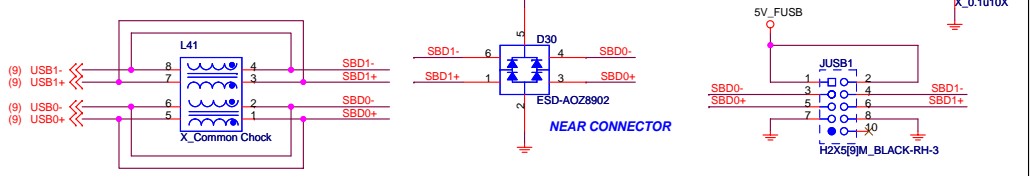
Front USB Connector

For H61 6,7,12,13 Port should be remove

FRONT USB PORT 2,3

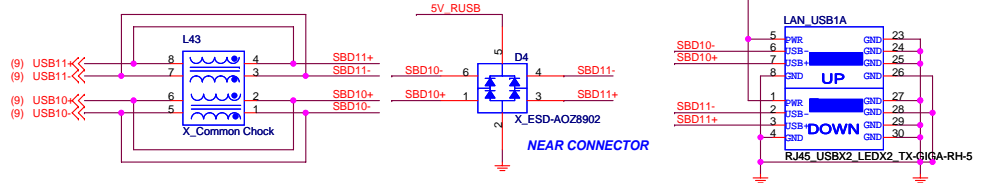


FRONT USB PORT 0,1

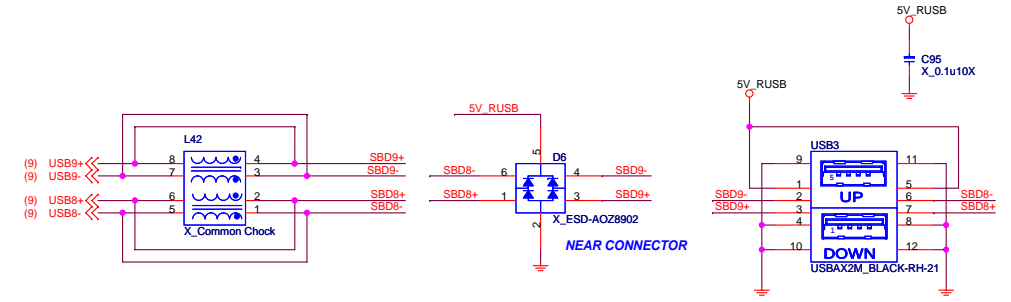


Rear USB Connector

REAR USB PORT 10,11 (With LAN)

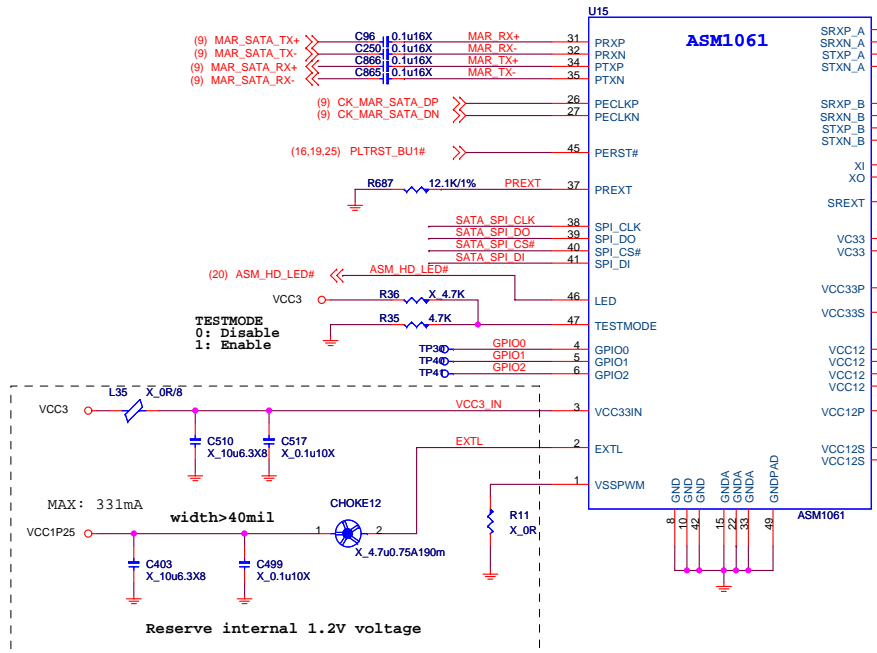


REAR USB PORT 8,9 (With PS2)



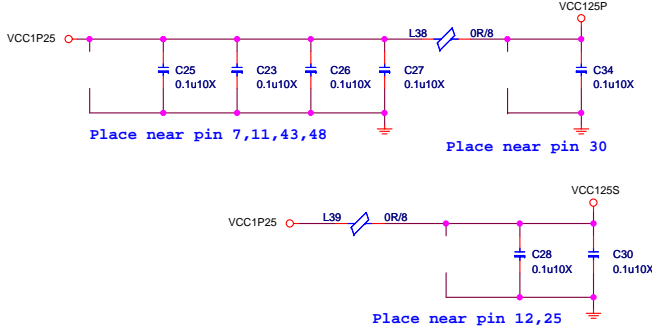
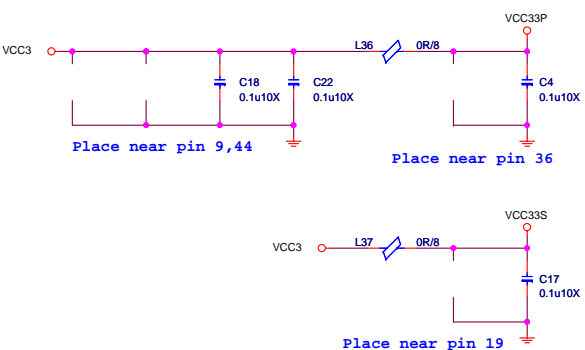
	MICRO-STAR INT'L CO.,LTD		
	MS-7732		
Size	Document Description	Rev	
Custom	USB Connector	1.1	
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ASM1061 SATA6G

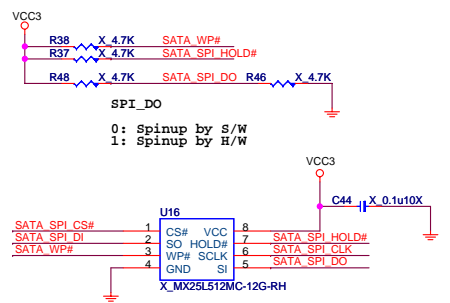
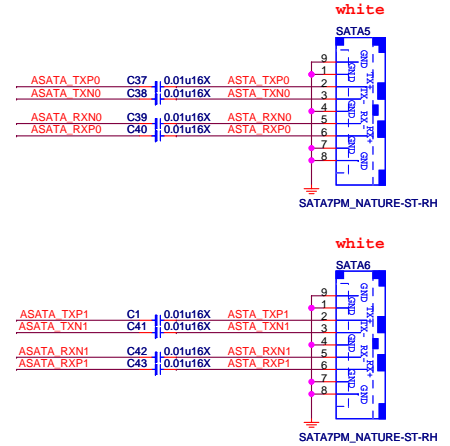
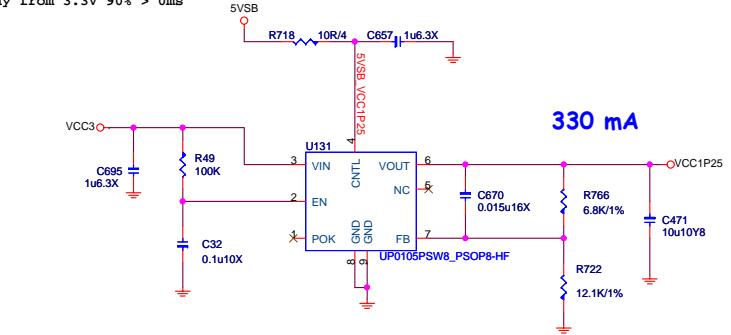


ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



1.2V delay from 3.3V 90% > 0ms



MICRO-STAR INT'L CO.,LTD

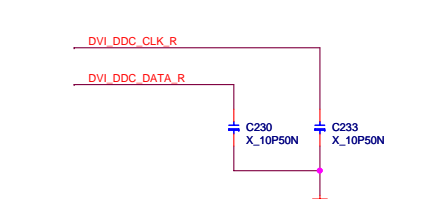
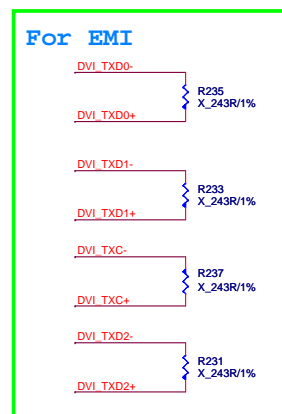
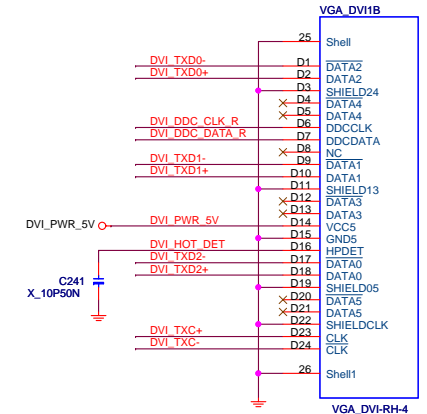
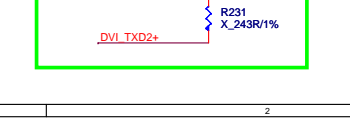
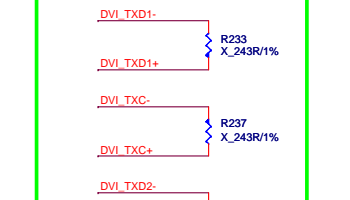
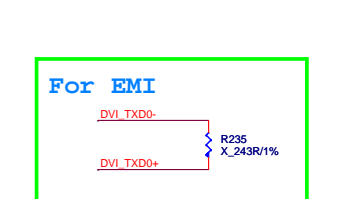
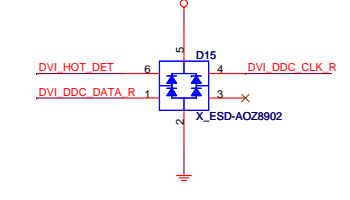
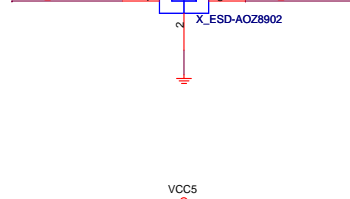
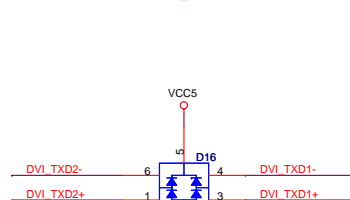
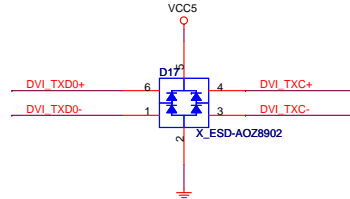
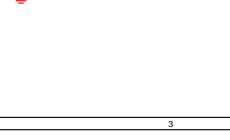
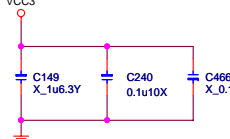
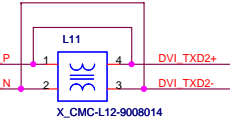
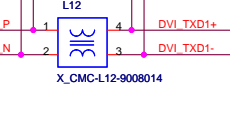
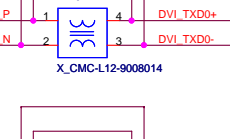
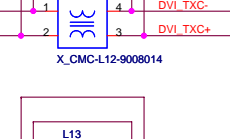
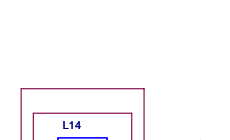
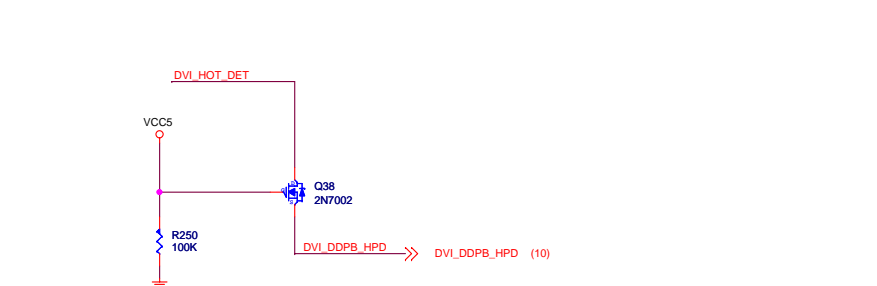
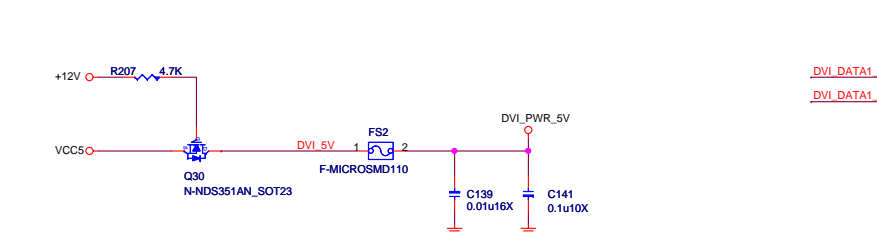
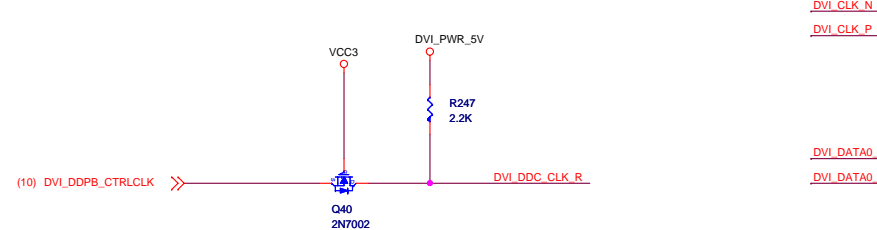
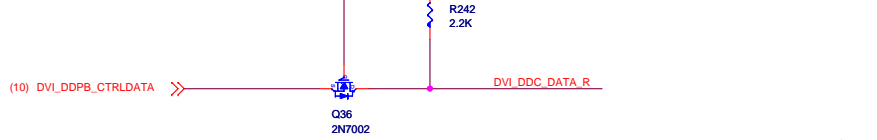
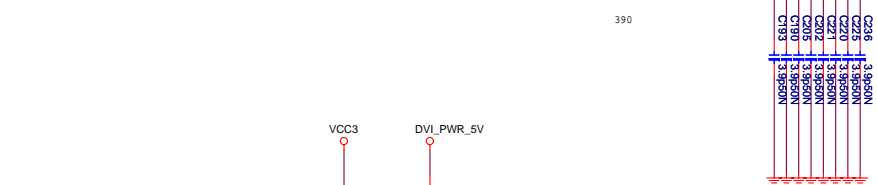
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DVI level shifter

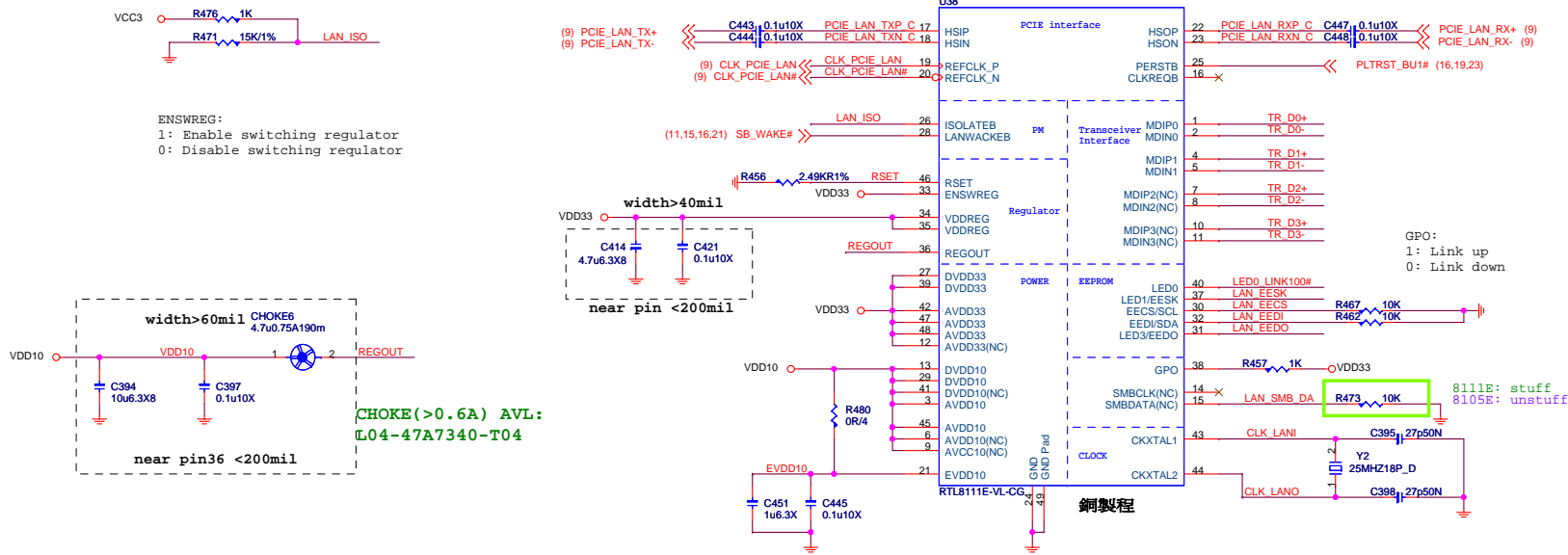
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



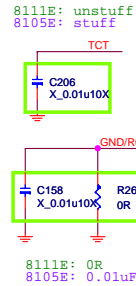
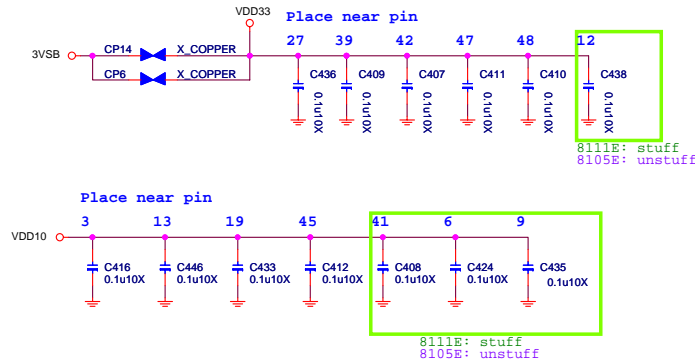
MICRO-STAR INT'L CO.,LTD		
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RTL8111E Giga LAN

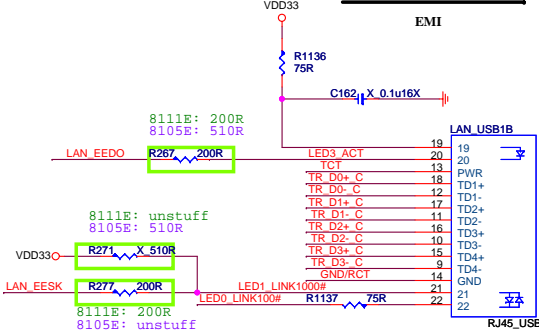
RTL8105E 10/100M LAN



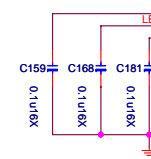
3.3v Power on rise time : 1-100ms. MAX: 163mA



LAN Connector



only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



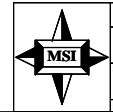
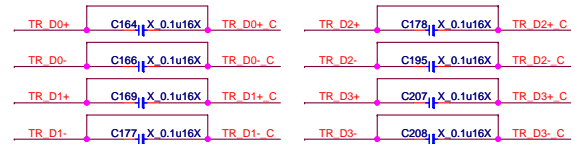
Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0771	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None	10	None
19		19	
20	250R Yellow	20	Yellow
21		21	Orange
22	250R Green	22	Green

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
SO ALDPS	3.2	11

8111E POWER Consumption

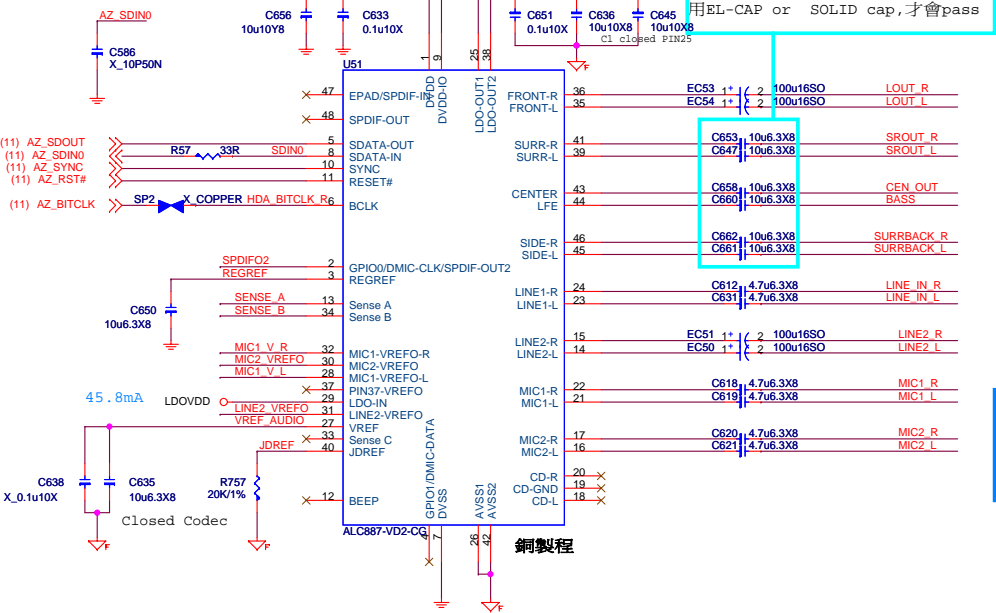
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13



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Custom	LAN - RTL8111E / 8105E	1.1
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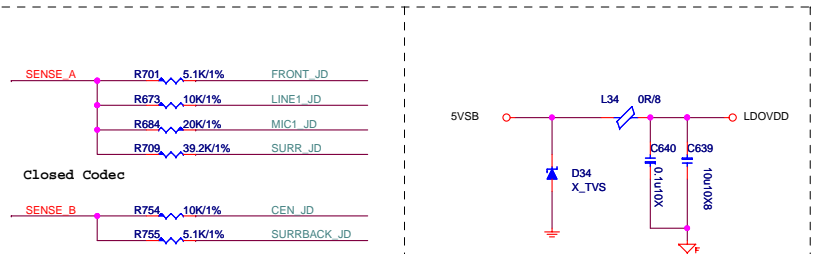
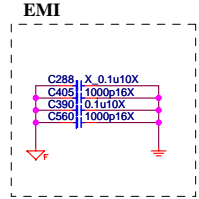
ALC887-VD

ALC892

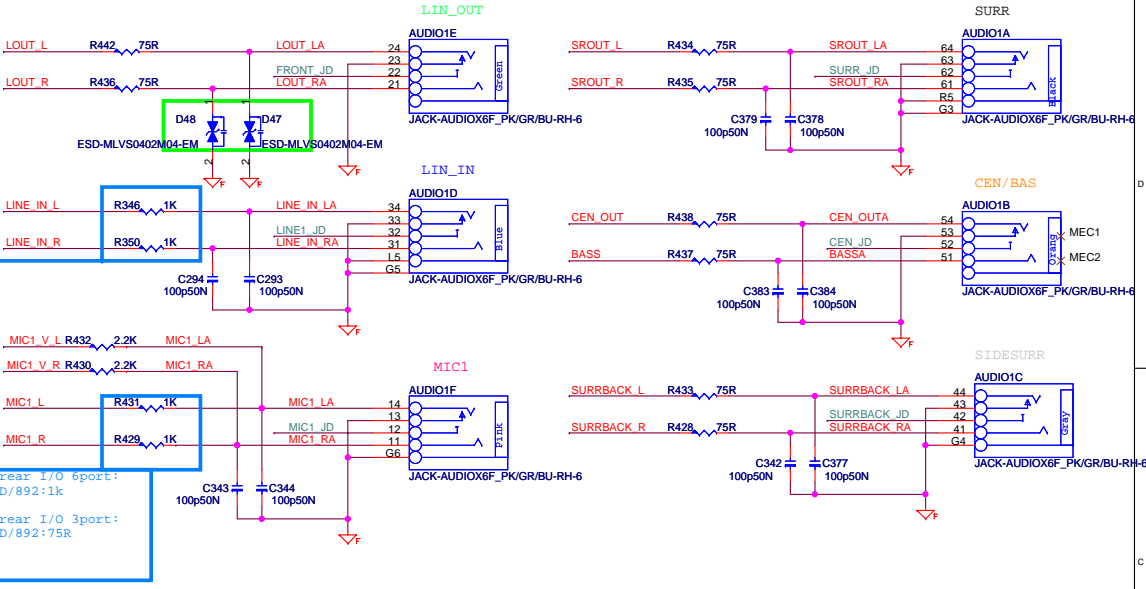
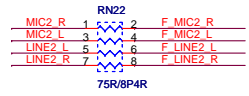
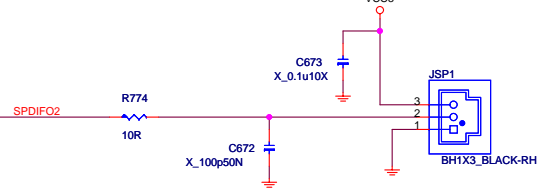


用SMD CAP 手動量測會FAIL在THD+N
用EL-CAP or SOLID cap, 才會pass

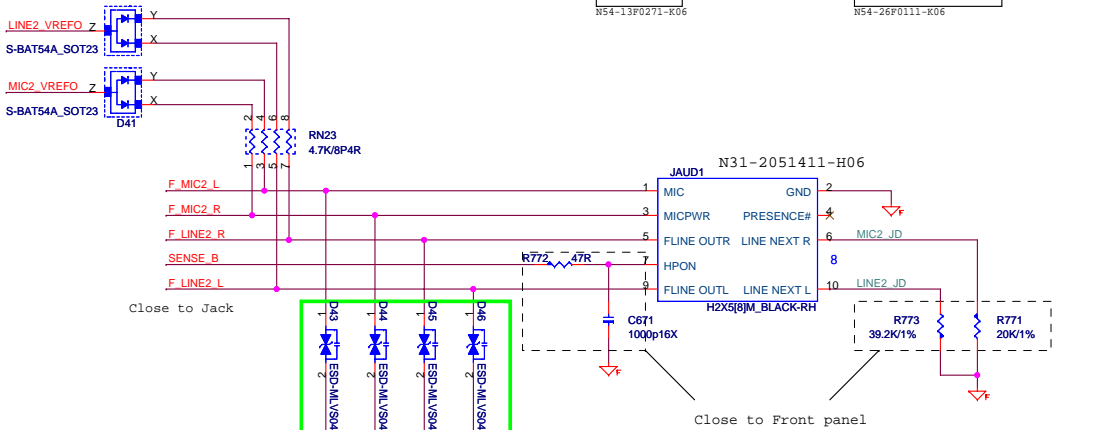
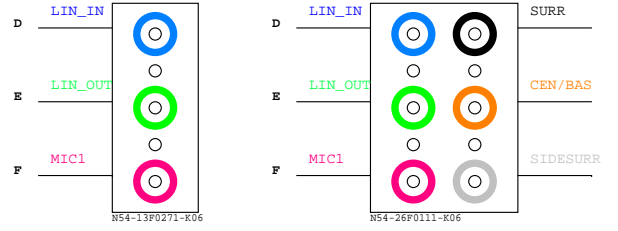
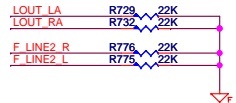
銅製程



SPDIF OUT

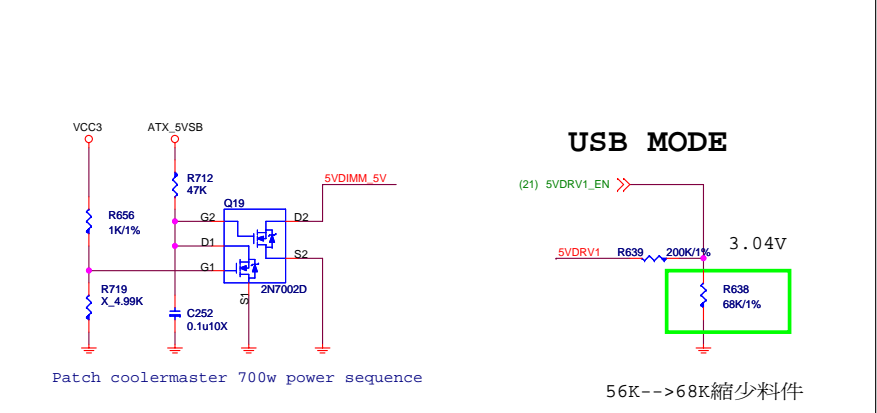
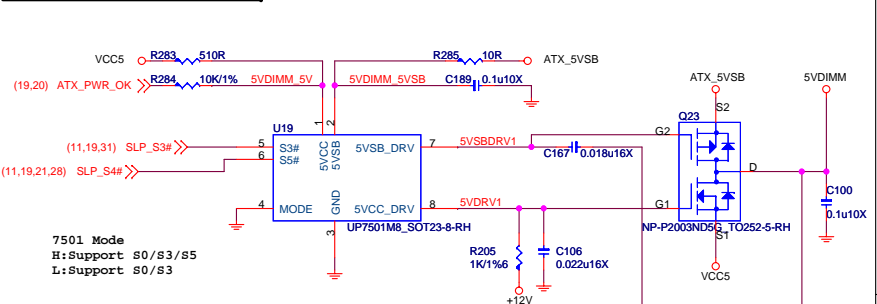


當串接電容有極性時，需上對地電阻

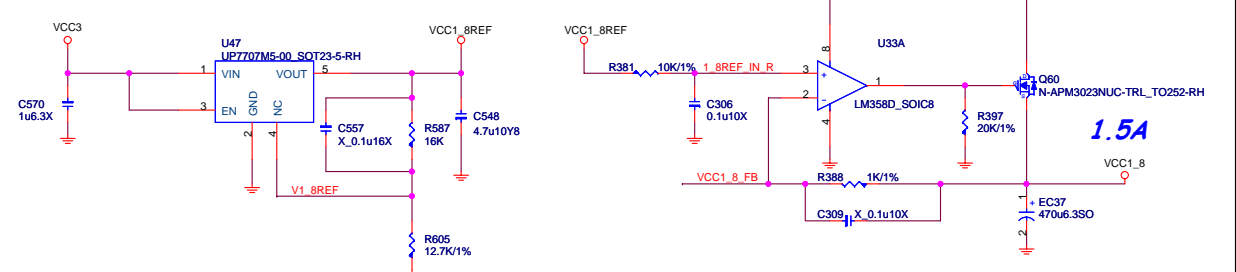


MICRO-STAR INT'L CO.,LTD		
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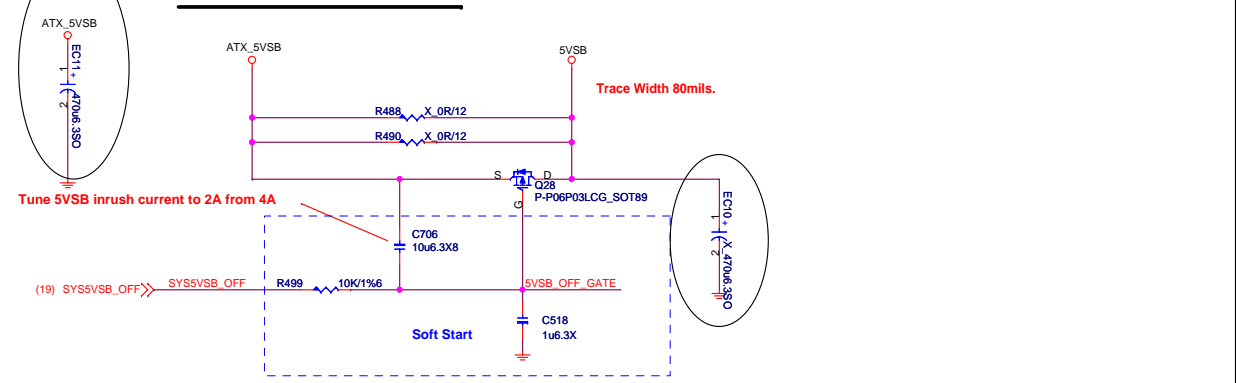
5VDIMM FOR DDR



VCC1_8REF

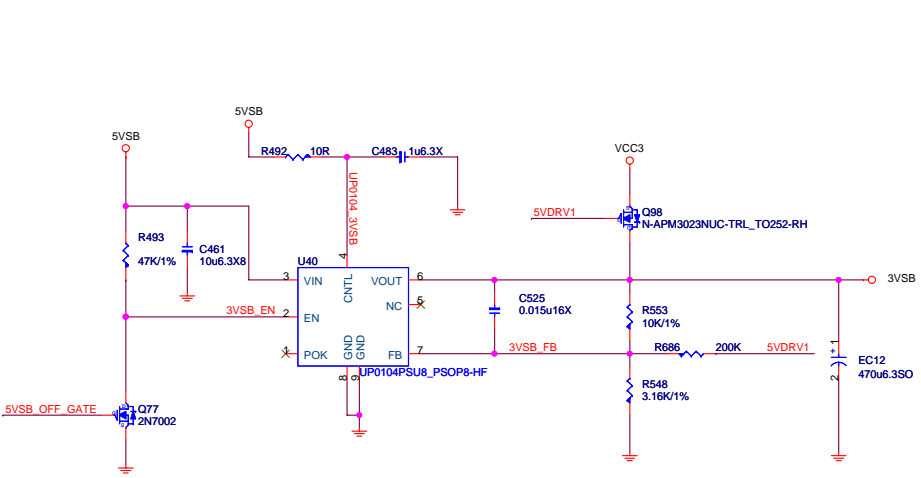


5VSB Power Switch

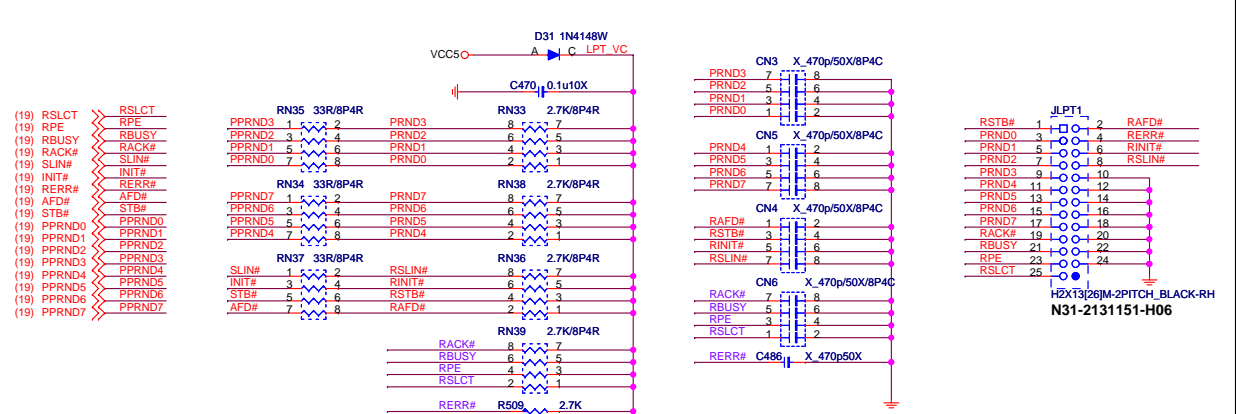


3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



PARALLAL PORT



MICRO-STAR INT'L CO.,LTD

MS-7732

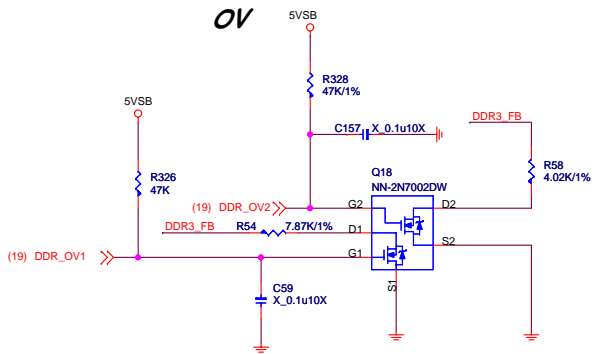
Size Custom Document Description
ACPI Controller UPI/Parallel

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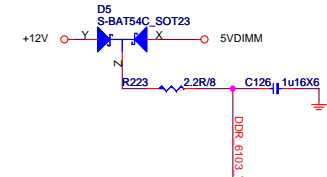
DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT

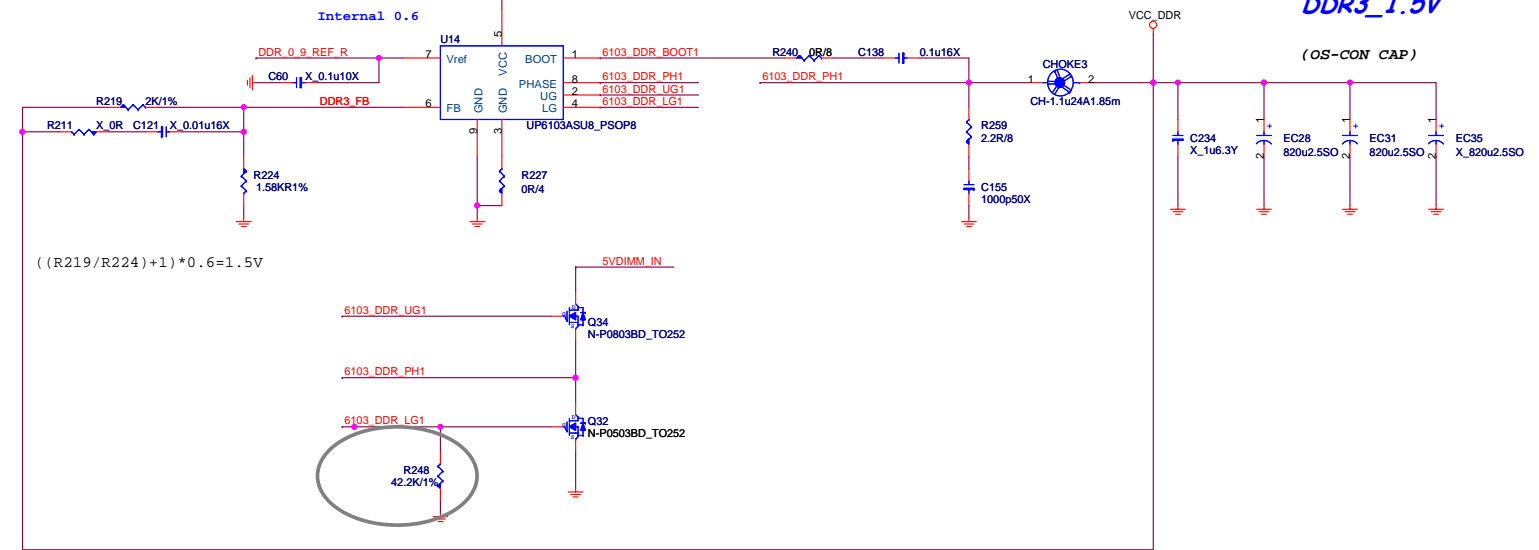
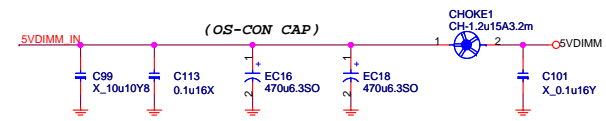
OV



MODE	第一階	Default	第二階	第三階
DDR_OV1	LOW	HIGH	LOW	HIGH
DDR_OV2	LOW	LOW	HIGH	HIGH
VALUE	1.35V	1.5V	1.65V	1.8V



Ripple=7.7A
5.7*2*1=11.4A>7.7A

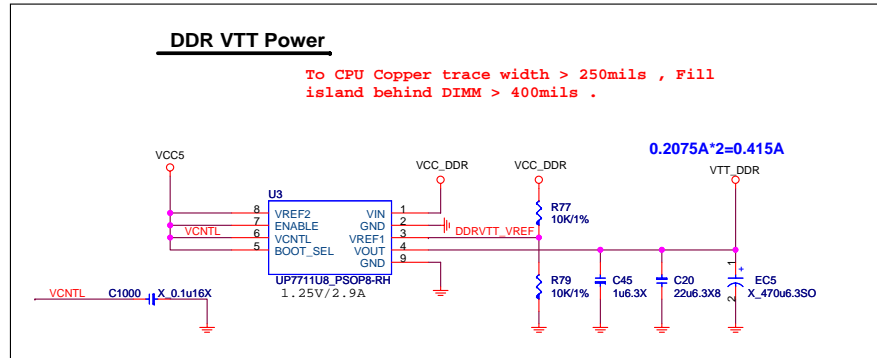
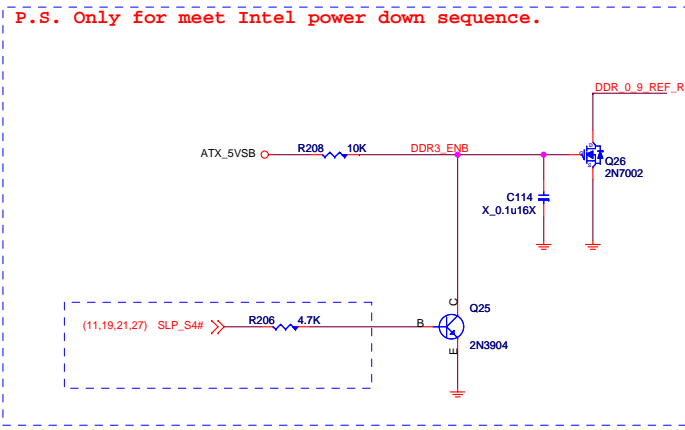


$((R219/R224)+1) * 0.6 = 1.5V$

UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

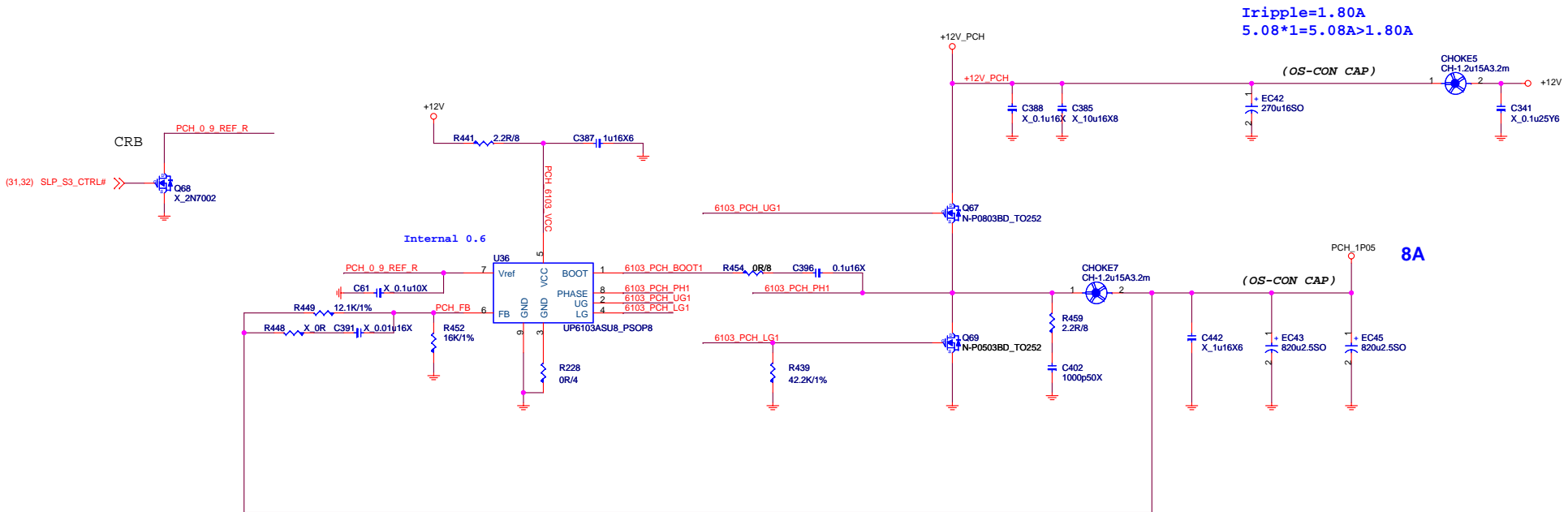


To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.

0.2075A*2=0.415A

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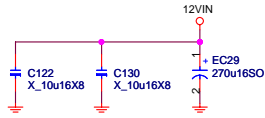
PCH Power:1.05V
PCH Core 6.2A+1.8A=8A
6.2A FOR PCH
1.8A FOR ME CORE



CPU_VTT:1.05/1.00

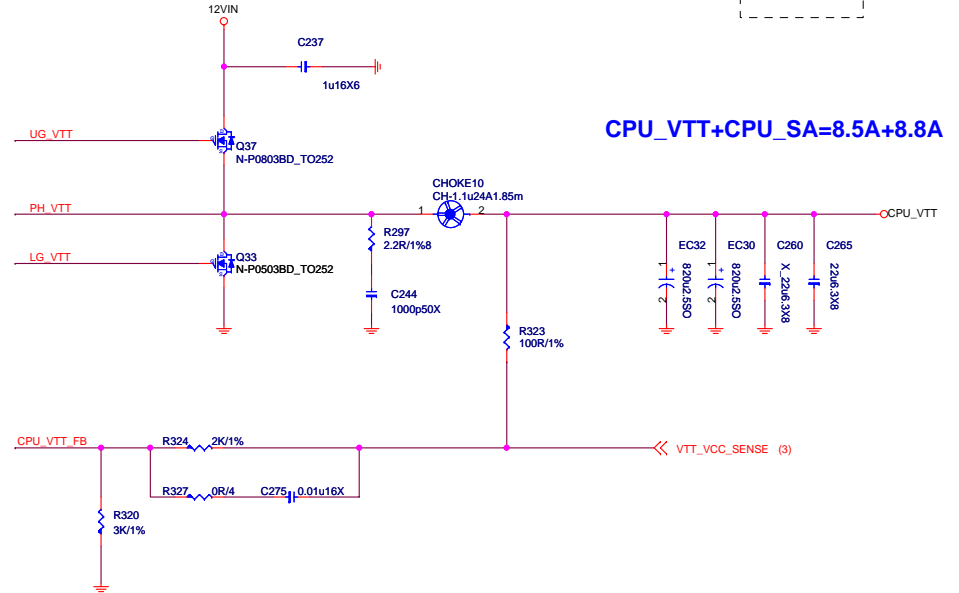
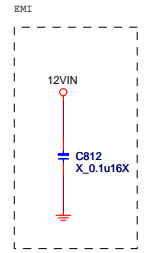
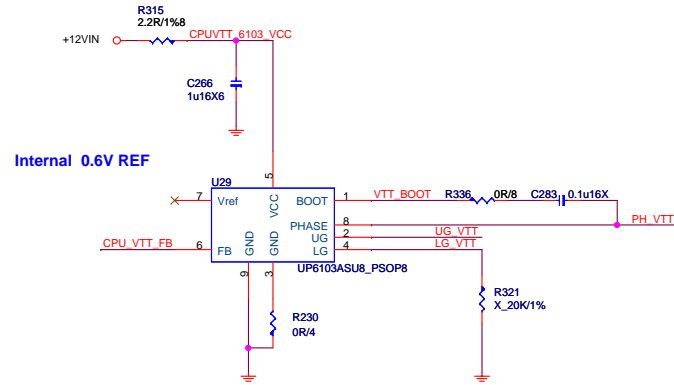
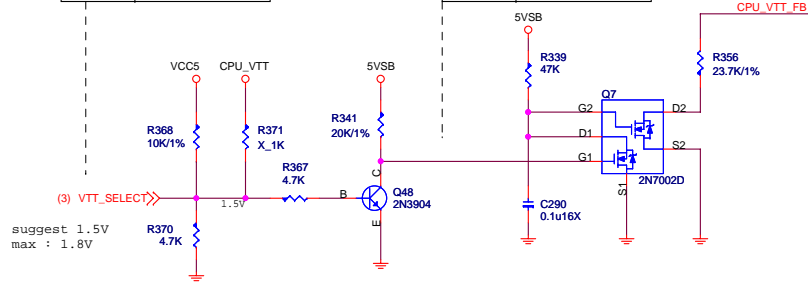
CPU VTT 8.5A + SA Core =17.3A

$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

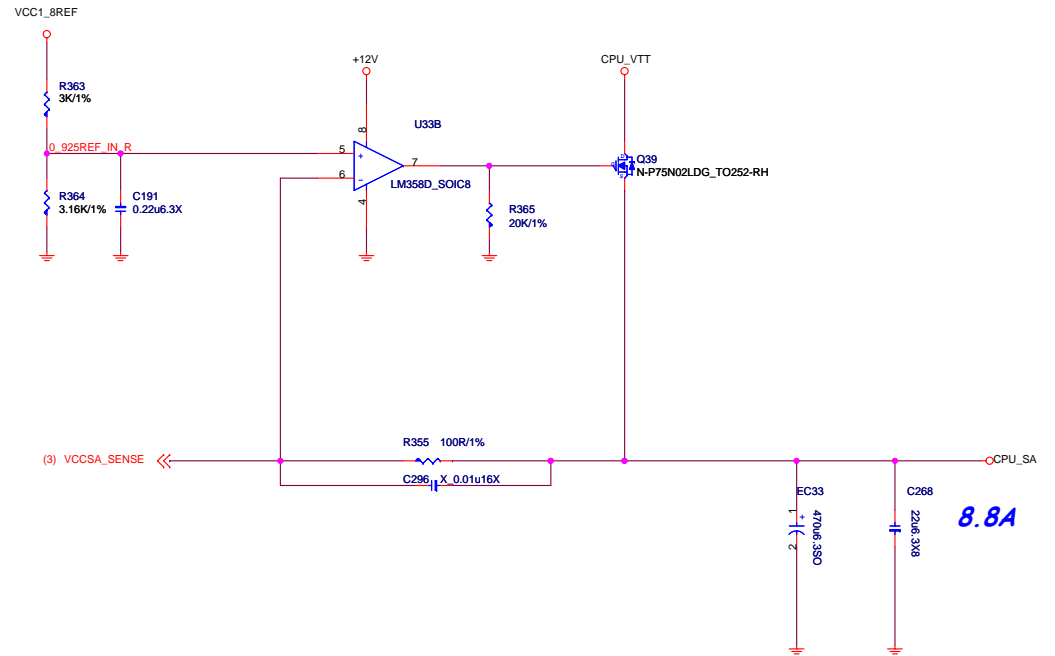
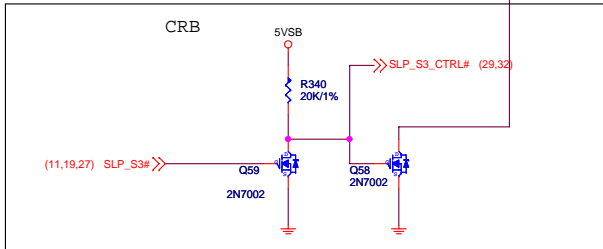
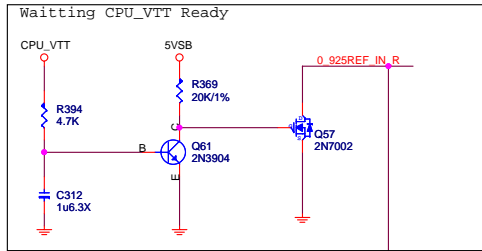
VTT_SELECT Table	
Low	1.05V
High	1.0V



MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description CPU_VTT - uP6103-1-Phase	Rev 1.1
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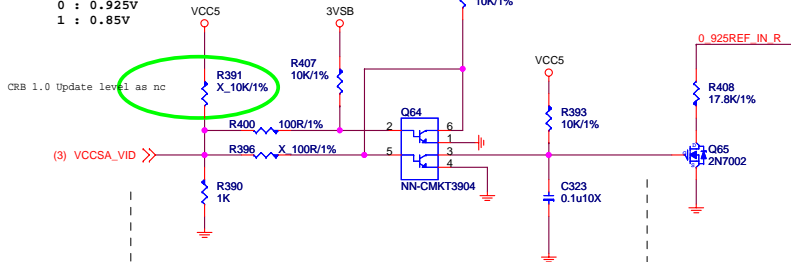
CPU_SA:0.925/0.85

SA Core = 8.8A



8.8A

VCCSA_VID
0 : 0.925V
1 : 0.85V



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.85V
High	0.925V



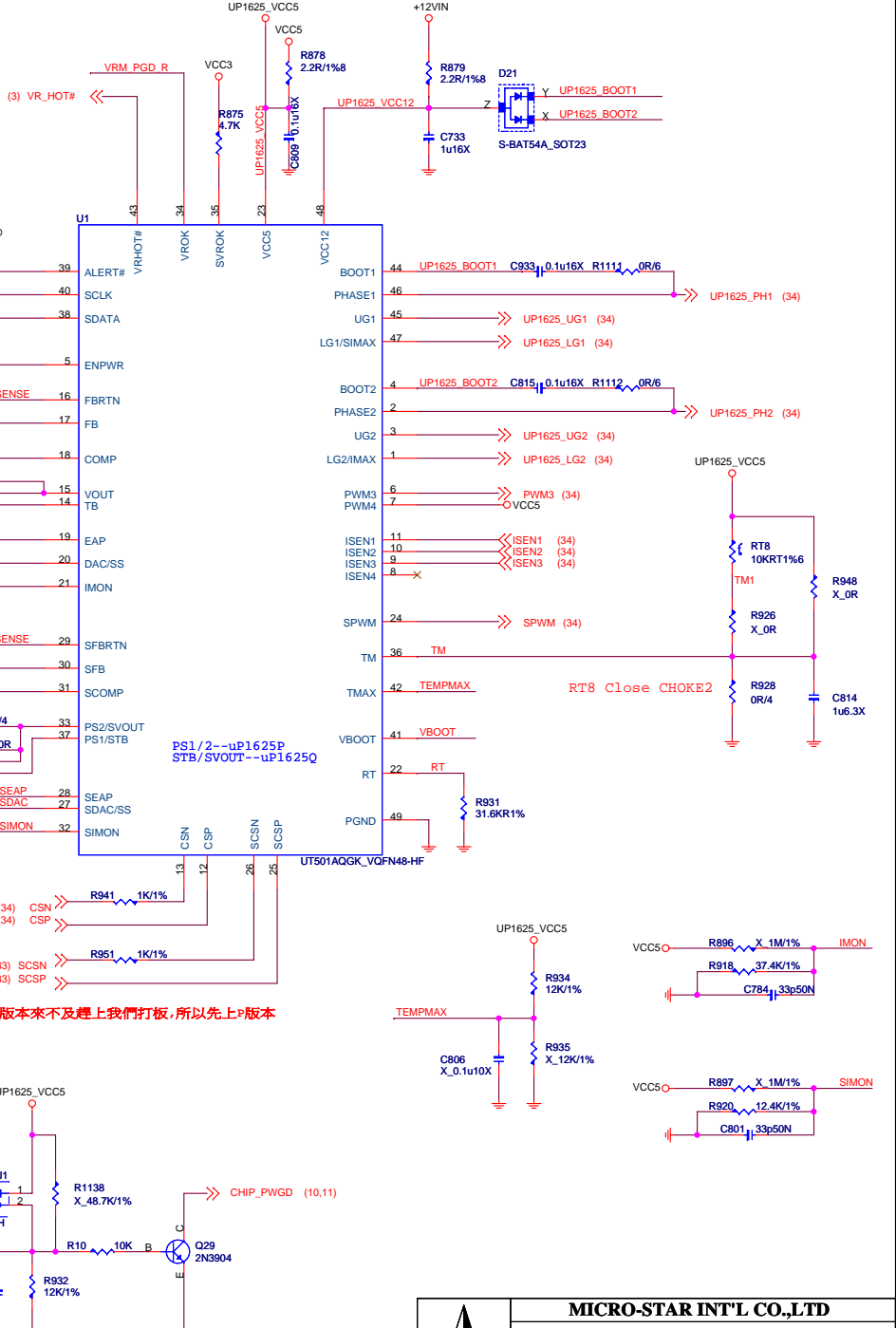
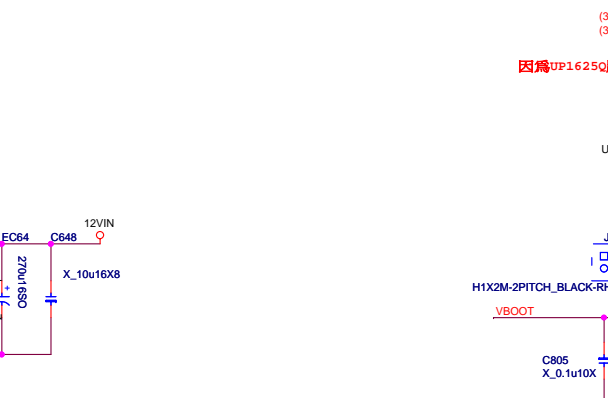
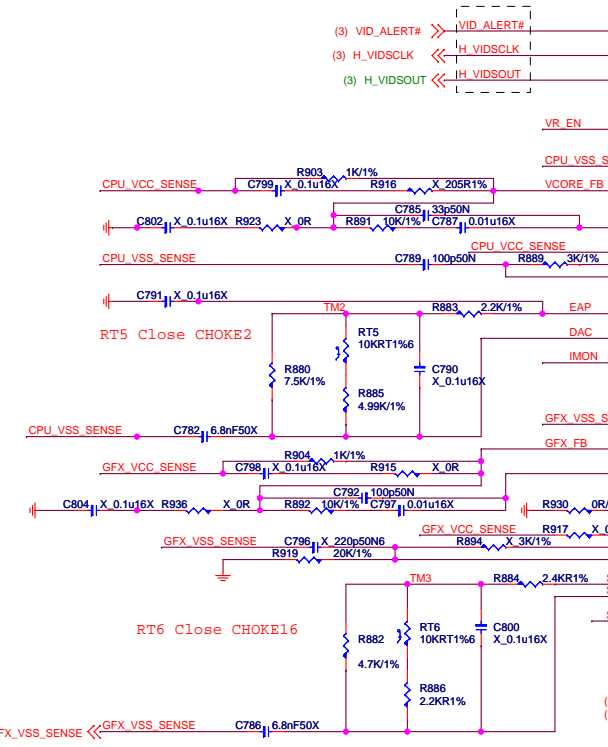
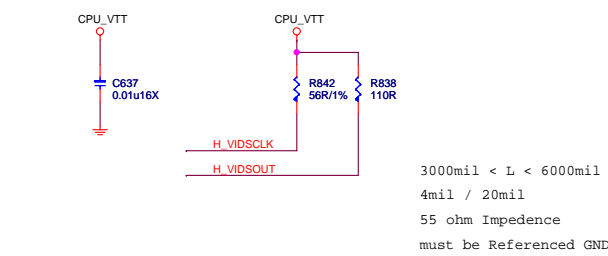
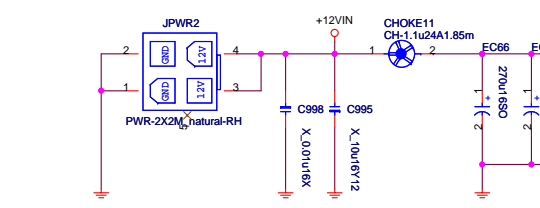
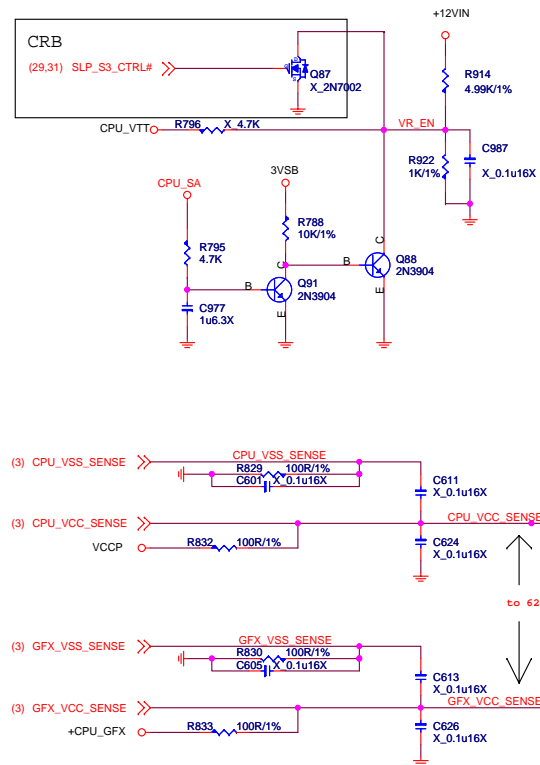
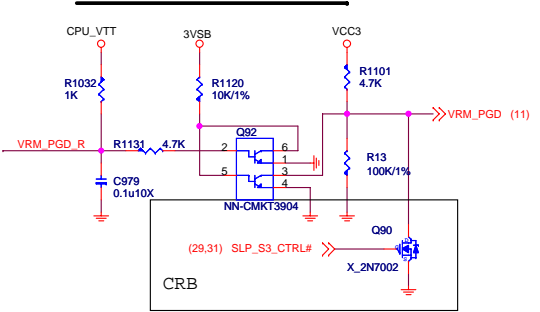
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Size	Document Description	Rev
Custom	CPU_SA - uP6103 1-Phase	1.1

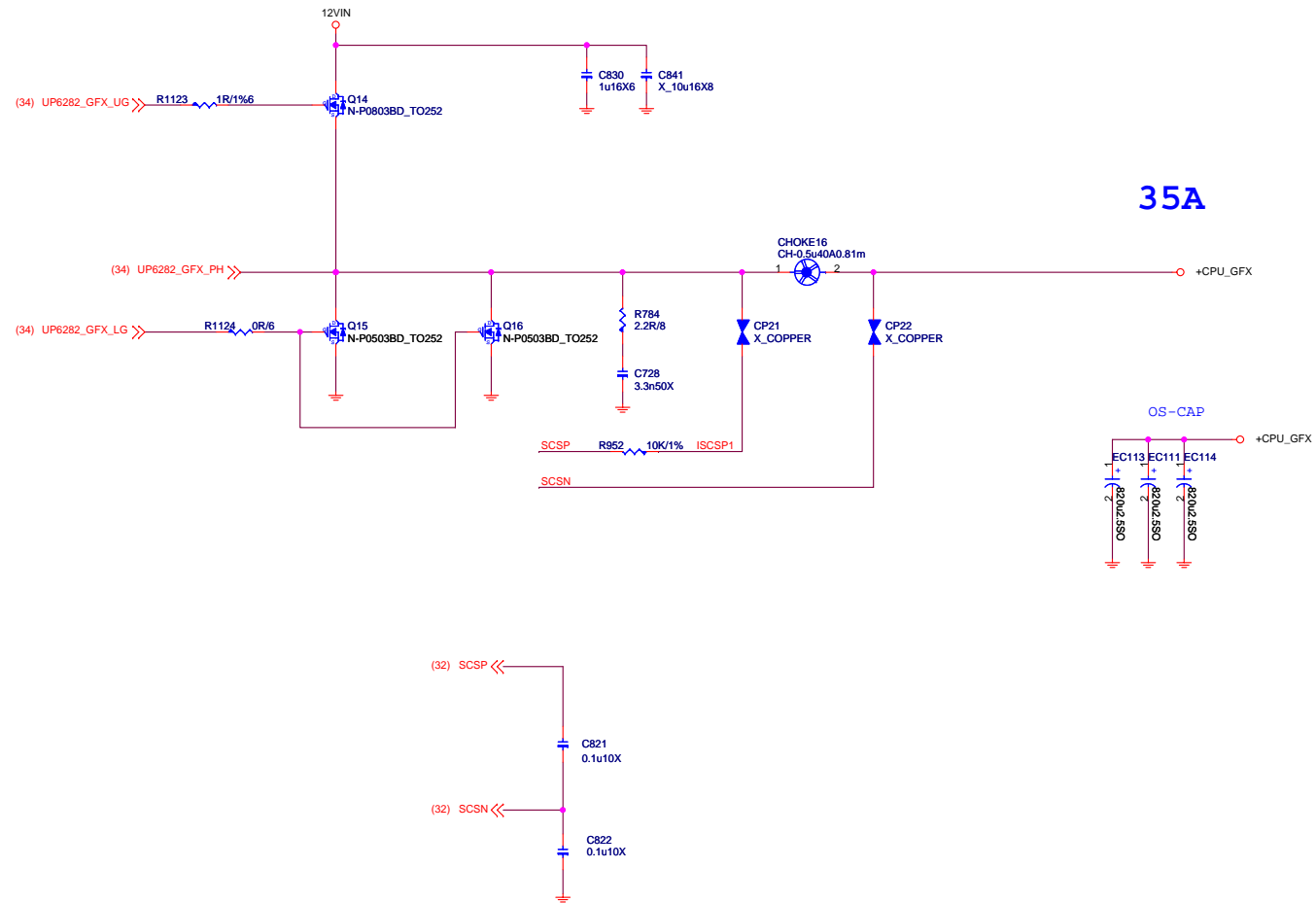
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VRMPWRGD LEVEL SHIFT



因為UP16250版本來不及趕上我們打板,所以先上P版本

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	Size Custom	Document Description VRD12 - UP16234 4+1-Phase
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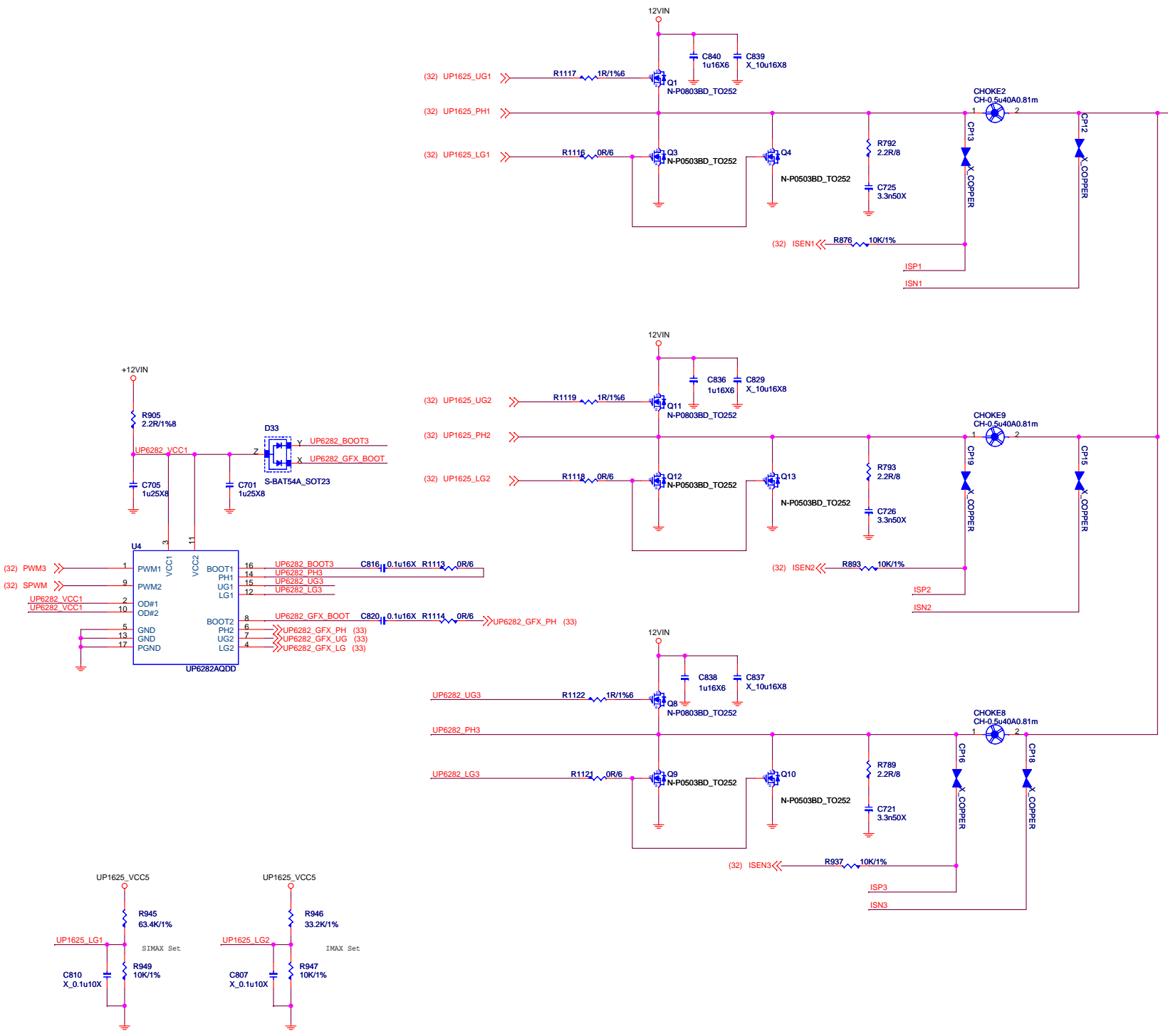


MICRO-STAR INT'L CO.,LTD

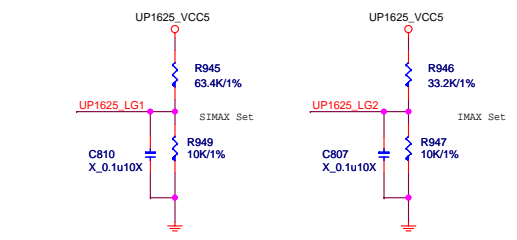
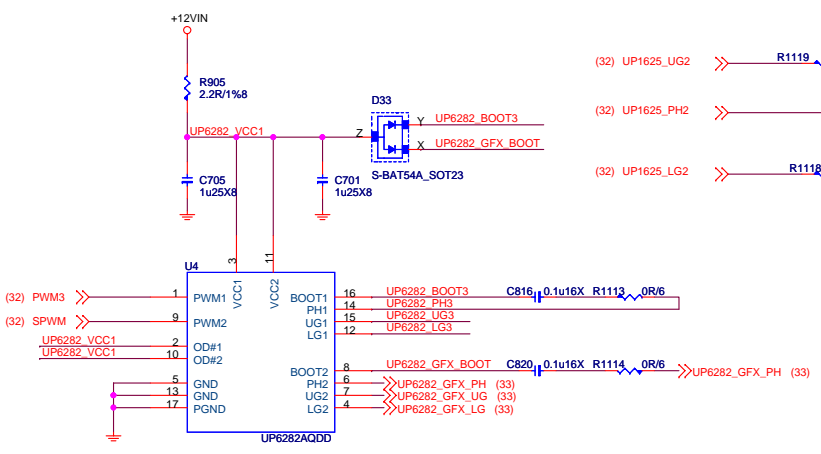
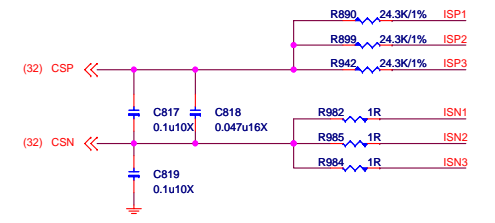
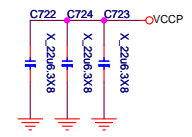
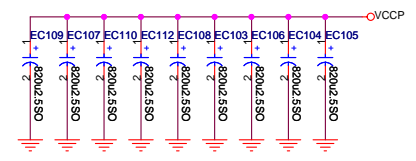
MS-7732

Size	Document Description	Rev
Custom	UP6234 1-Phase GPU	1.1

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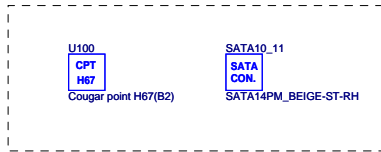
0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm



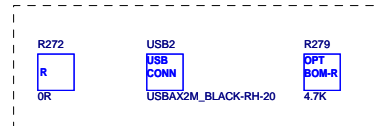
MICRO-STAR INT'L CO.,LTD		
MS-7732		
Size Custom	Document Description UP6234 6-Phase CPU	Rev 1.1
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OPT	Configure	BOM	Function	Marketing Name	M.P. ERP NO.
	CFG-7732-A	601-7732-01S	MS-7732 1.0 H61MU-E45 Intel H61+2*DDRIII+1*PCIe16,2*PCIe1,1*PCI+DVI/D-sub +4*SATAII+2*SATAIII+2*USB3.0+8*USB2+6 Flexible audio ports+Gb lan,EuP,(All Solid Cap),RoHS	PH61A-P35 (B3)	
A	CFG-7732-B	601-7732-02S	MS-7732 1.0 OPT:A H61MU-E45 Intel H61+2*DDRIII+1*PCIe16,2*PCIe1,1*PCI+D-sub +4*SATAII+10*USB2+6 Flexible Audio ports+Gb lan,EuP,(All Solid Cap),RoHS	PH61-P33 (B3)	601-7732-010
B	CFG-7732-C	601-7732-03S	MS-7732 1.0 OPT:B H61MU-E45 Intel H61+2*DDRIII+1*PCIe16,2*PCIe1,1*PCI+DVI/D-sub +2*SATAII+6*USB2+3 Flexible Audio ports+Gb lan,EuP,(All Solid Cap),RoHS	PH61-SP35 (B3)	601-7732-020 OPT:C

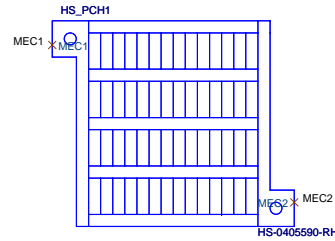
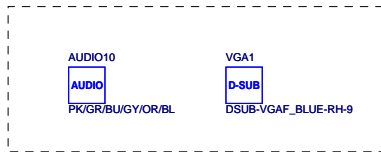
H67 OPT.



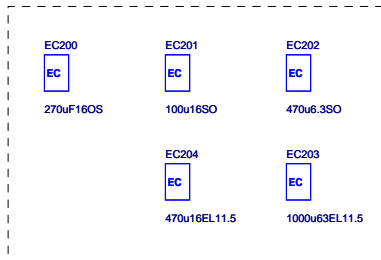
USB 3.0



AUDIO & VGA CON OPT.



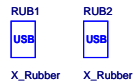
EL/OS OPT.



7732-1.0



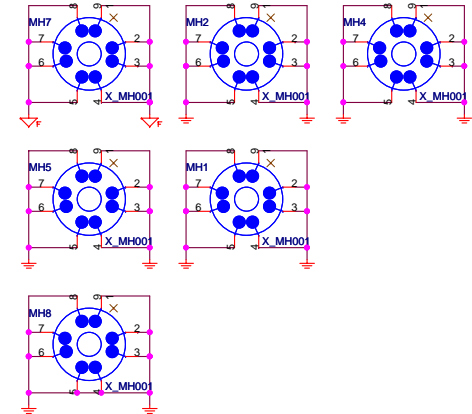
	銀	電泳黑	白色
CPU鐵座	E21-7557040-L06	E21-7670020-L06	E21-7557050-L06



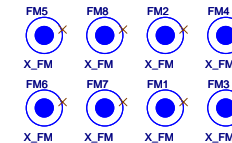
Simulation



Mounting Holes



Optical Fiducial Marks-120



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PK0-0773210-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)
 PK0-0773210-G37, 精成, 77, 寶安恩斯邁廠 (MSIS)
 PK0-0773210-E36, E&E, 23, 寶安恩斯邁廠 (MSIS)
 PK0-0773210-E36, E&E, 27, 寶安恩斯邁廠 (MSIS)
 PK0-0773210-E48, 麗華, 23, 寶安恩斯邁廠 (MSIS)
 PK0-0773210-E48, 麗華, 27, 寶安恩斯邁廠 (MSIS)