

PCB STACK UP

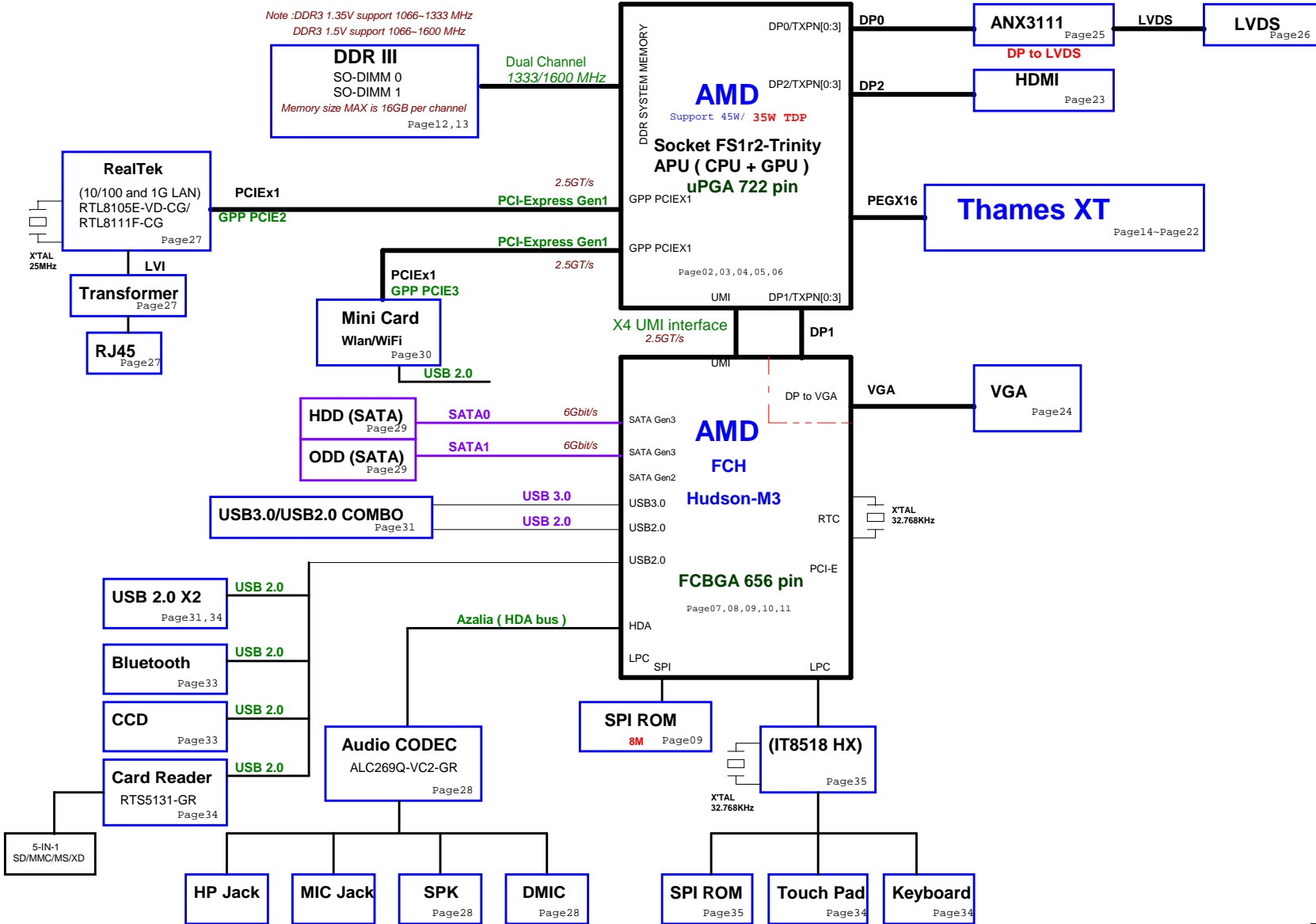
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : SVCC
- LAYER 6 : IN2
- LAYER 7 : GND
- LAYER 8 : BOT

FAN /THERMAL
EMC2103-2
Page32

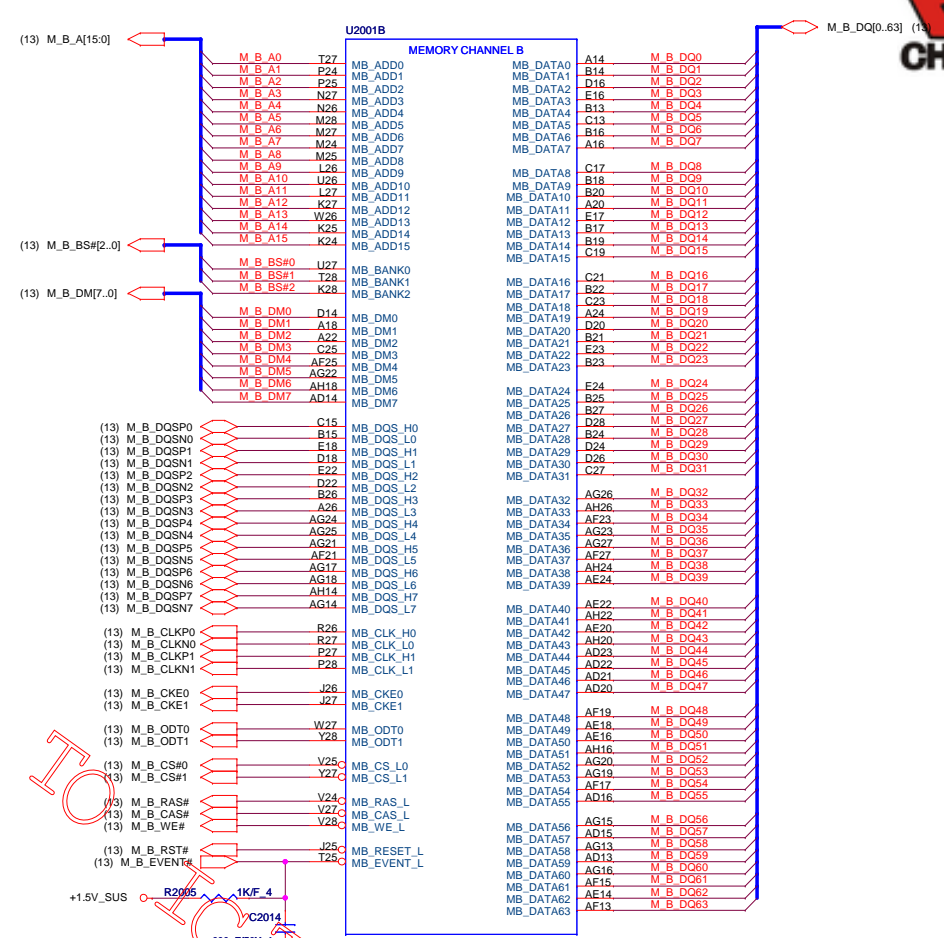
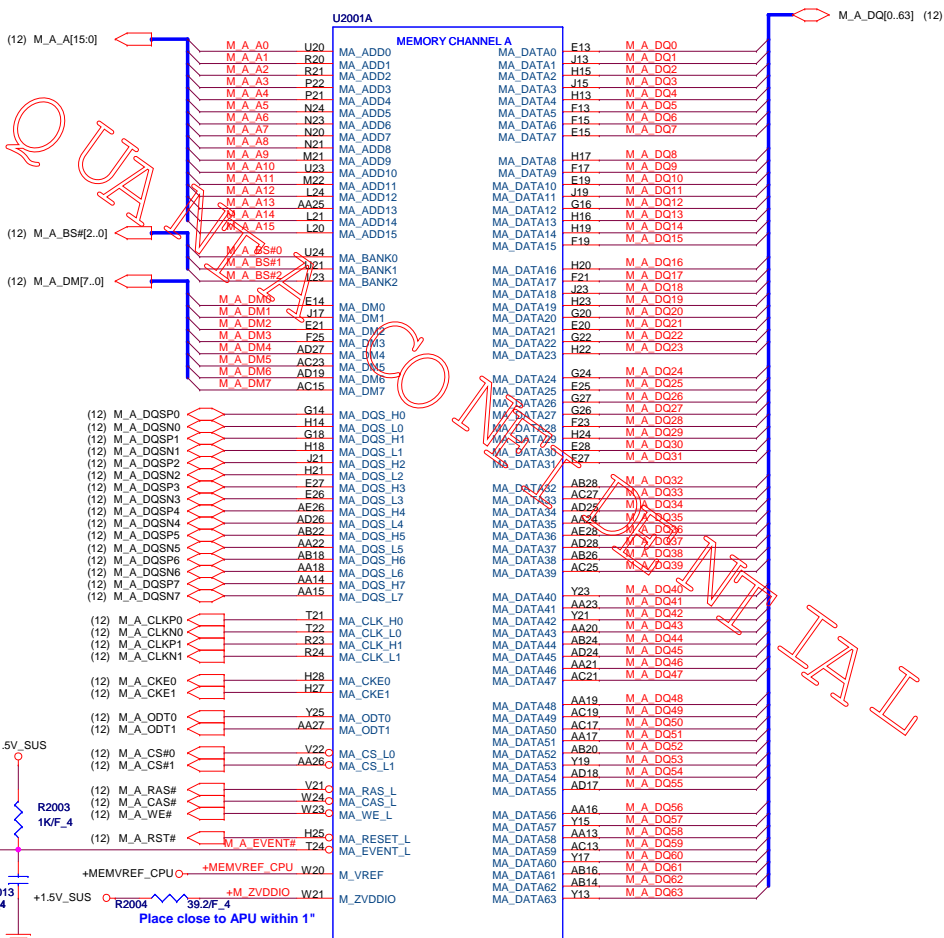
BLOCK DIAGRAM

Note :DP means Display Port Interface

Note :DDR3 1.35V support 1066-1333 MHz
DDR3 1.5V support 1066-1600 MHz

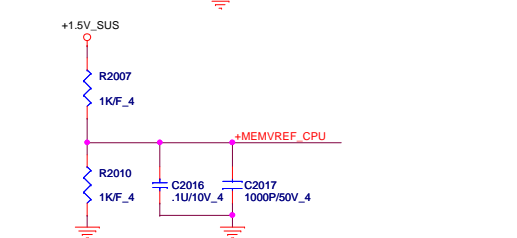


Discharge (8024737)	Page37
Charge (TP951216)	Page38
DDR3/0.75V (TP951216)	Page40
3V/5V (TP951123ARGER)	Page39
+1.1V_DUAL & 1.1V (TP9511211)	Page41
+1.2V_VDDPR/+2.5 (TP9511211)	Page42
VDD/+VDDNB_CORE (ISL6277RRT2-T)	Page43
DGPU (ISL6277RRT2-T)	Page44
1.8V	Page45
GPU	Page46



Trinity APU

Trinity APU

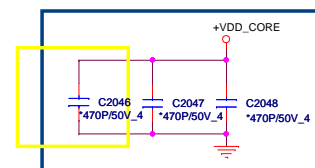


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Quanta Computer Inc.		
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	APU 2/5(DDR3 MEM I/F)	2A
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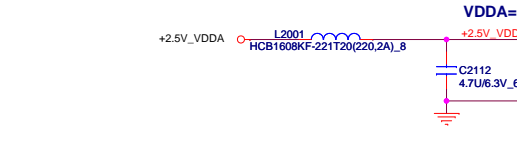
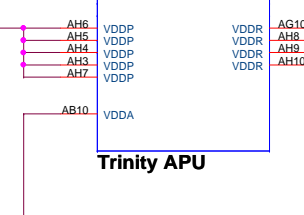
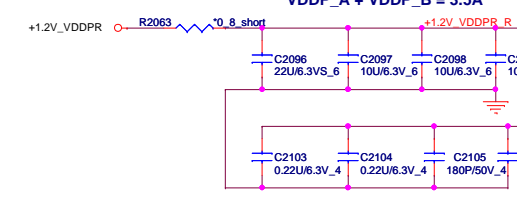
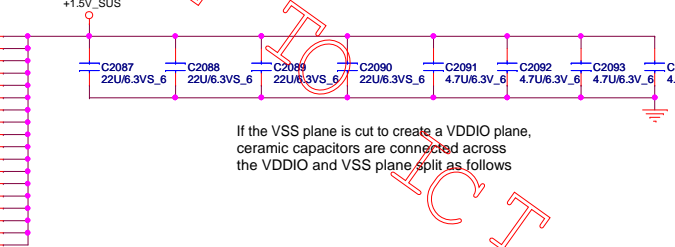
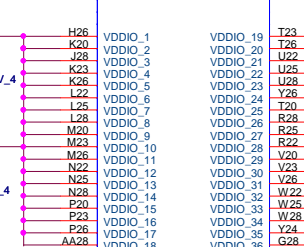
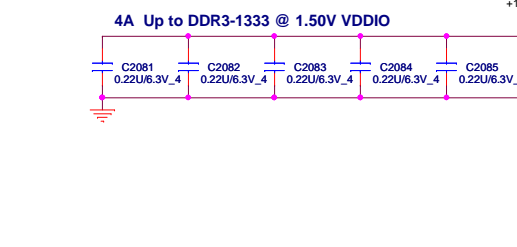
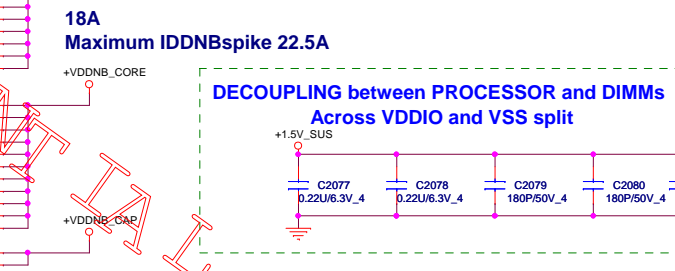
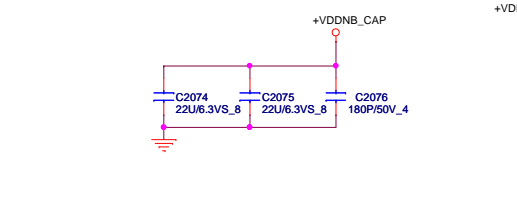
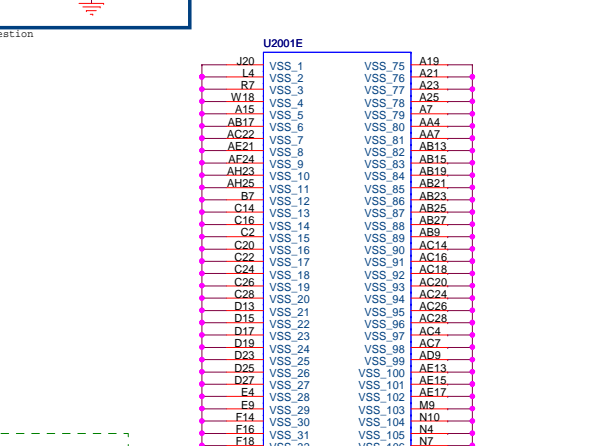
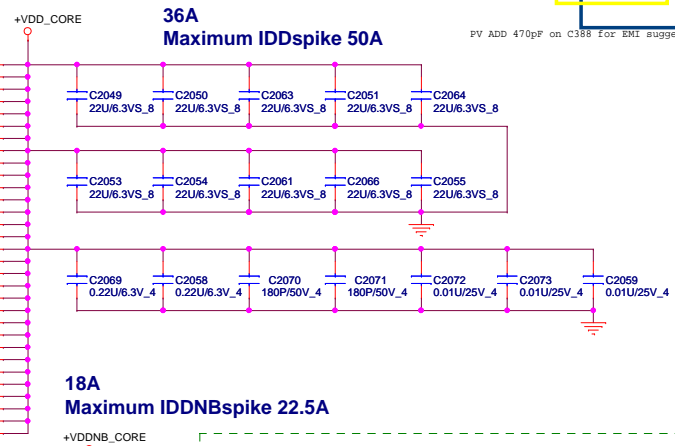
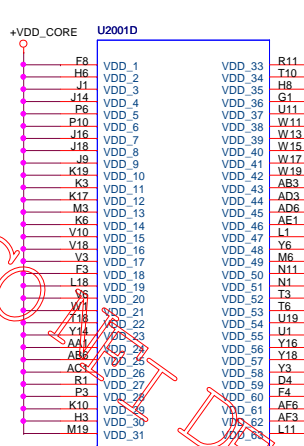
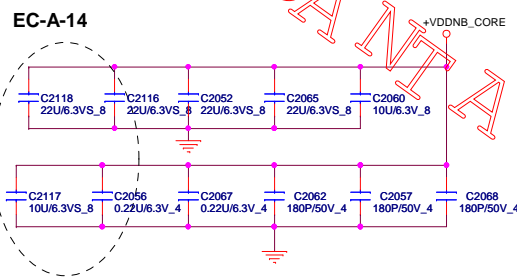


APU POWER TABLE

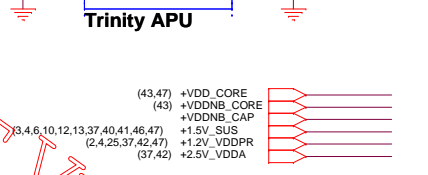
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



SI EMI



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows



PROJECT : LZ3C
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Size: 3,4,6,10,12,13,37,40,41,46,47
Document Number: APU 4/5(Power/GND)
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VID Override Circuit

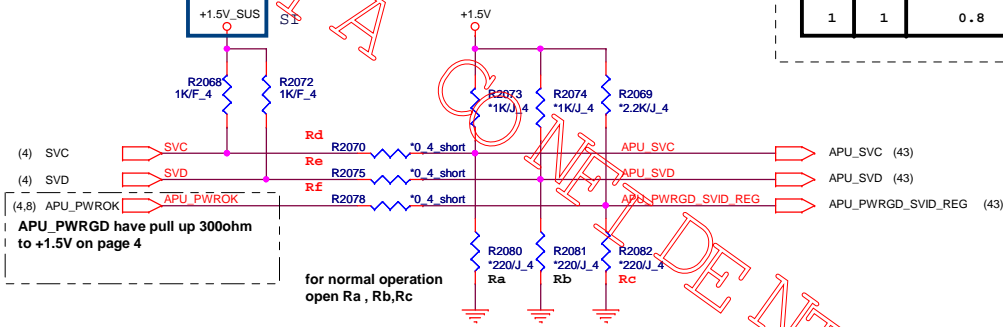
(4,25,30,41,43) +1.5V
(3,4,5,10,12,13,37,40,41,46,47) +1.5V_SUS

06



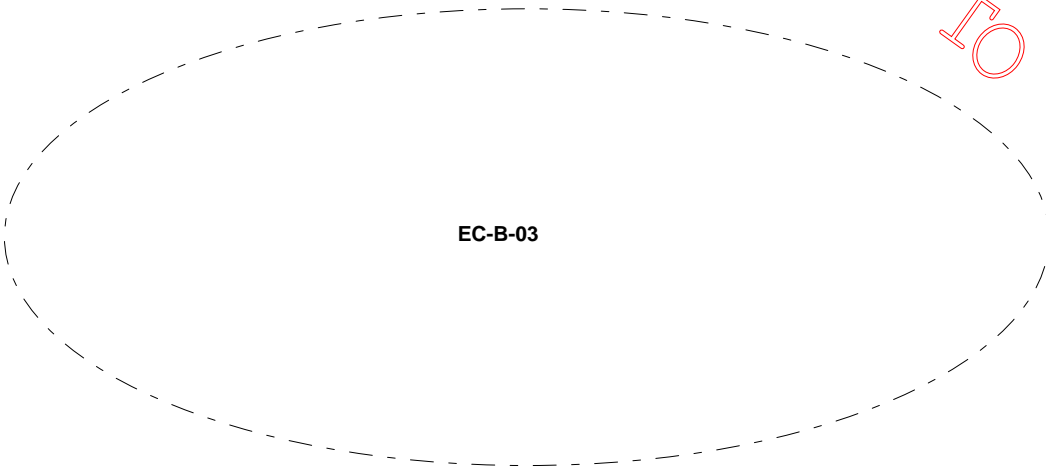
BOOT VOLTAGE			
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID, Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



(4,8) APU_PWRGD have pull up 300ohm to +1.5V on page 4

for normal operation
open Ra , Rb,Rc

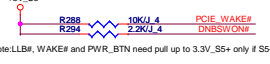
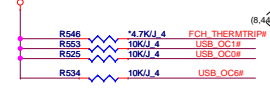
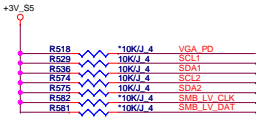
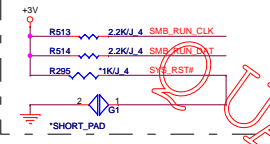
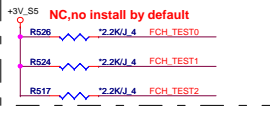


EC-B-03

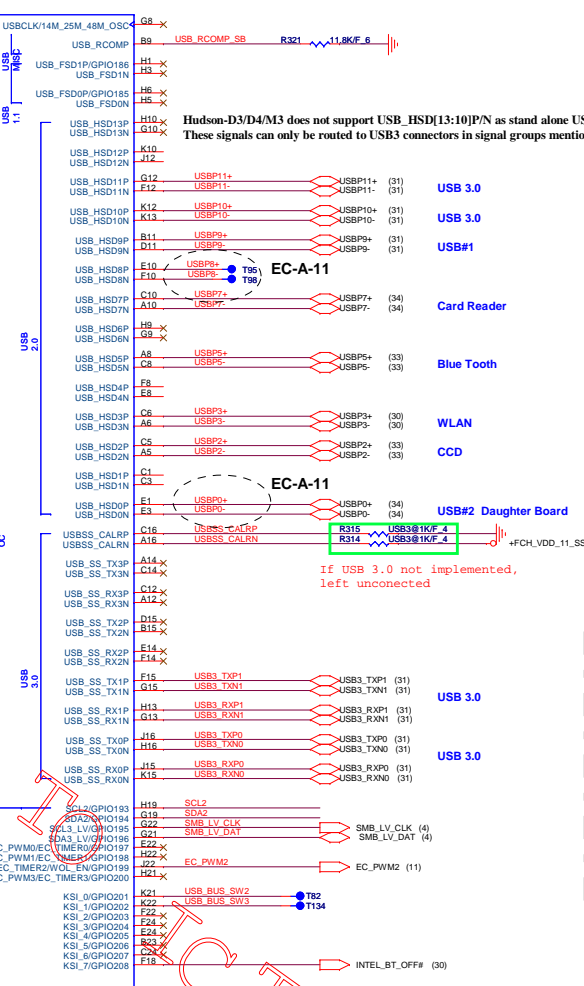
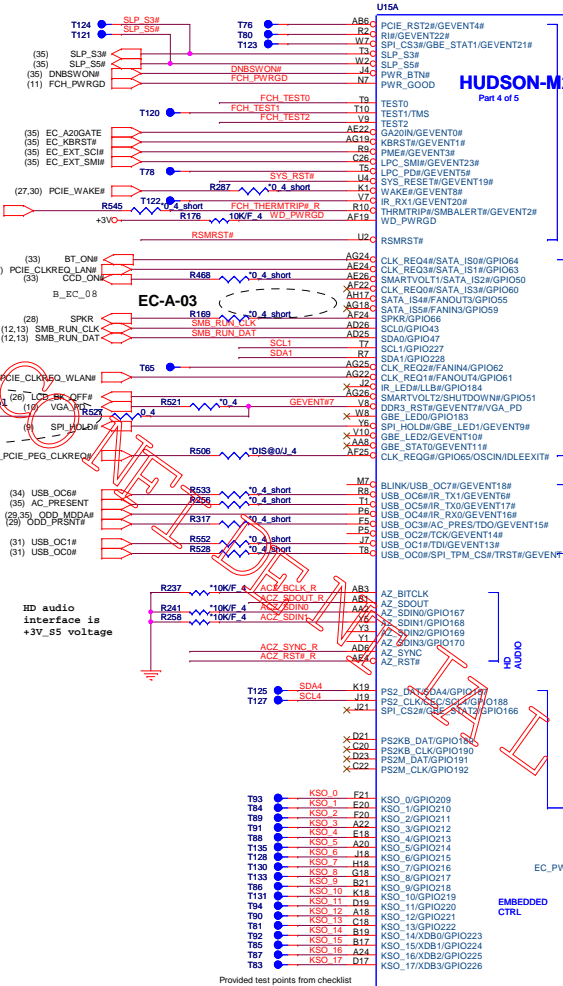
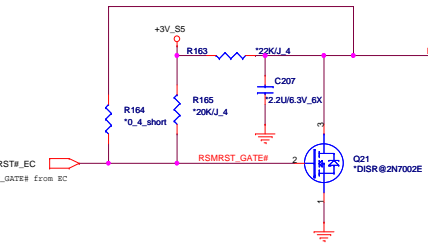
PROJECT : LZ3C
Quanta Computer Inc.

Size	Document Number	Rev
	APU 5/5(Other)	2A
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QUANTA CONFIDENTIAL TO IC T FOR REVIEW

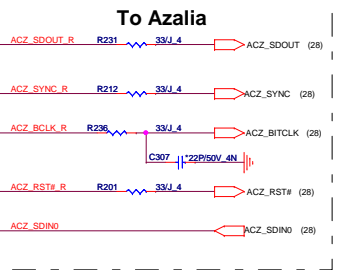


Note: LLB#, WAKE# and PWR_BTN need pull up to 3V_S5+ only if S5+ mode is supported



Note: USB 3.0 1:1 MAP to USB2.0 PORT
As Below:

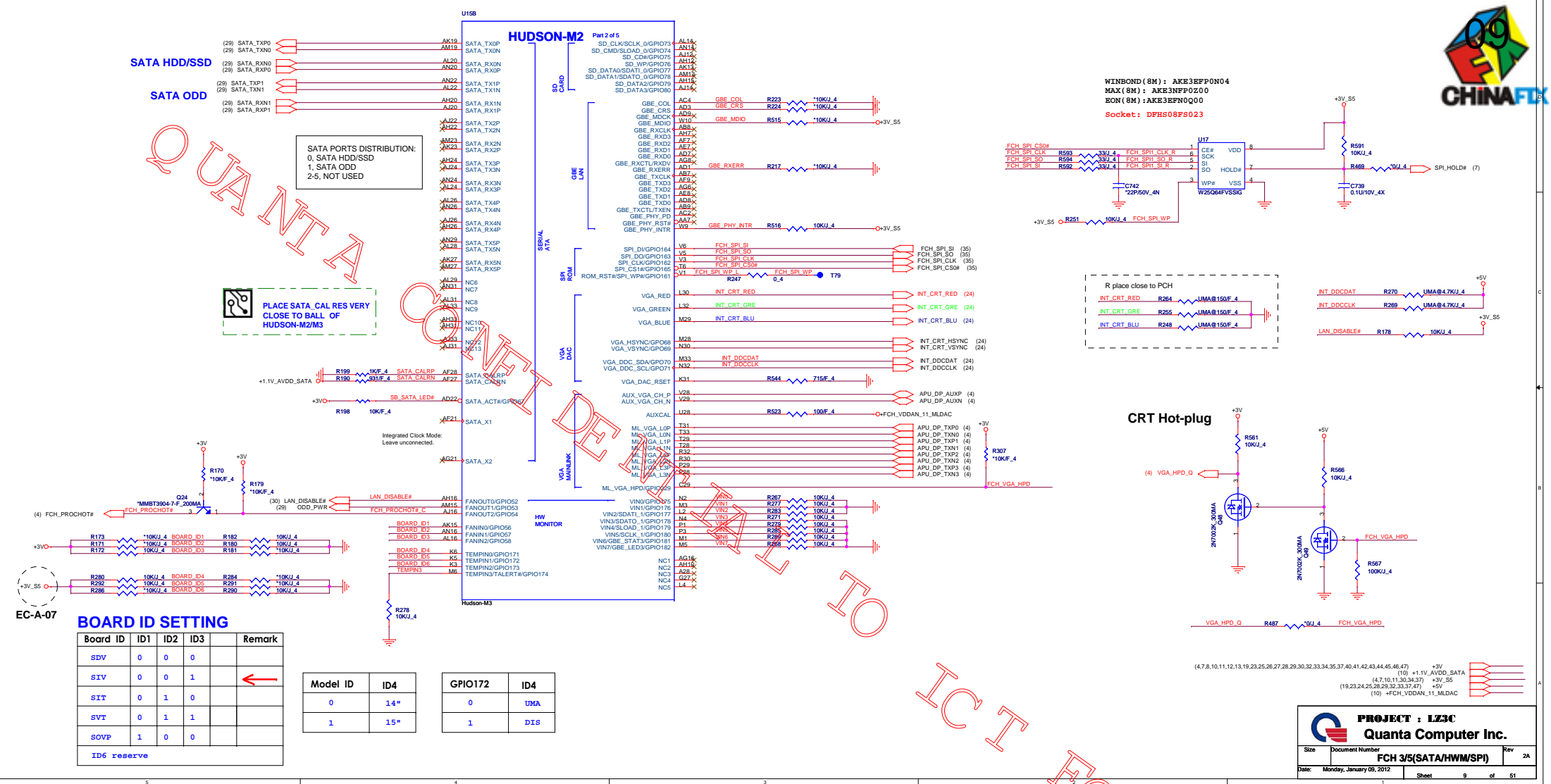
SSUSB0+USB10	USB3.0 PORT 0
SSUSB1+USB11	USB3.0 PORT 1
SSUSB2+USB12	NA
SSUSB3+USB13	NA



FOR REVIEW

PROJECT : LZ3C
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	FCH 1/5(GPIO/USB/AZ)	2A
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SATA HDD/SSD

(29) SATA_TXP0
(29) SATA_TXN0
(29) SATA_RXN0
(29) SATA_RXP0
(29) SATA_TXP1
(29) SATA_TXN1
(29) SATA_RXN1
(29) SATA_RXP1

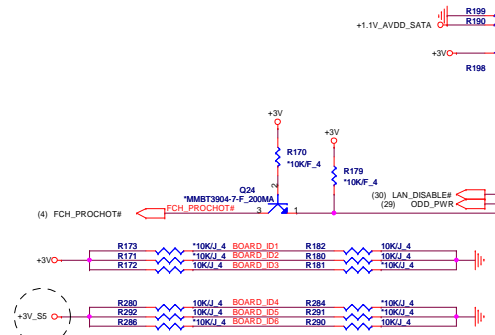
SATA ODD

(29) SATA_TXP0
(29) SATA_TXN0
(29) SATA_RXN0
(29) SATA_RXP0
(29) SATA_TXP1
(29) SATA_TXN1
(29) SATA_RXN1
(29) SATA_RXP1

SATA PORTS DISTRIBUTION:

0: SATA HDD/SSD
1: SATA ODD
2-5: NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3



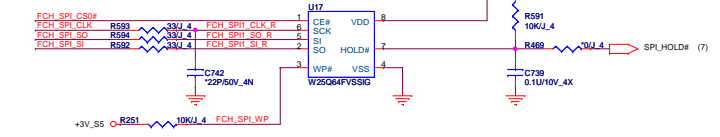
BOARD ID SETTING

Board ID	ID1	ID2	ID3	Remark
SDV	0	0	0	
SIV	0	0	1	
SIT	0	1	0	
SVT	0	1	1	
SOVP	1	0	0	
ID6 reserve				

Model ID	ID4
0	14"
1	15"

GPIO172	ID4
0	UMA
1	DIS

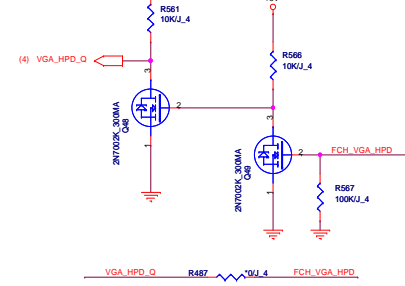
WINBOND (8M) : AKE3EFPN04
MAX (8M) : AKE3EPF020
BON (8M) : AKE3EPFNQ00
Socket : DFH808P023



R place close to FCH

INT_CRT_RED R264 UMA@150F 4
INT_CRT_GREEN R255 UMA@150F 4
INT_CRT_BLUE R248 UMA@150F 4

CRT Hot-plug



(4,7,8,10,11,12,13,19,23,25,26,27,28,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +3V
(10) +1.1V_AVDD_SATA
(4,7,10,11,30,34,37) +3V_SS
(19,23,24,25,26,29,32,33,37,47) +5V_SS
(10) +FCH_VDDAN_L1_MLDAC

PROJECT : LZ3C
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Size Document Number **FCH 3/5(SATA/HWM/SPI)** Rev 2A

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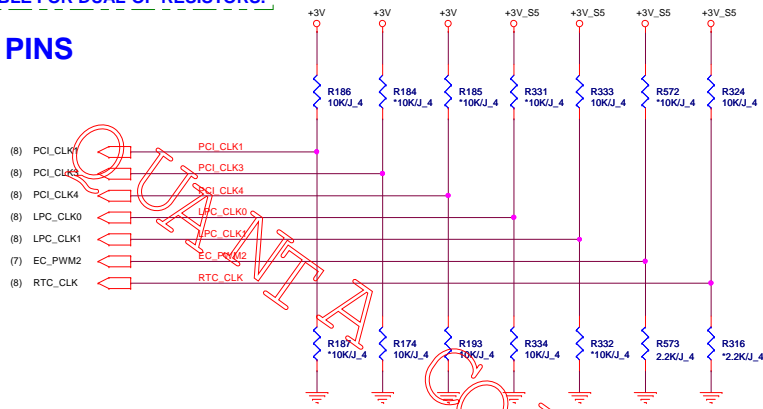


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

(4,7,8,9,10,12,13,19,23,25,26,27,28,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +3V
(4,7,9,10,30,34,37) +3V_S5

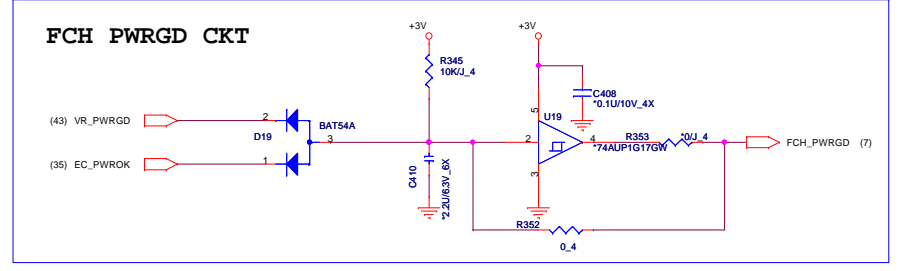


STRAPS PINS



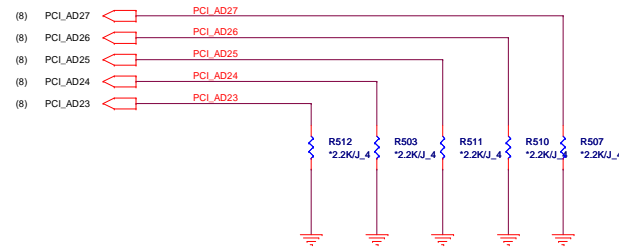
REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE ENABLED	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM	S5 PLUS MODE ENABLED



DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]



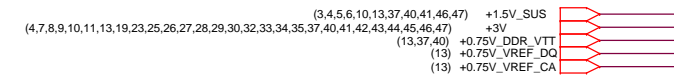
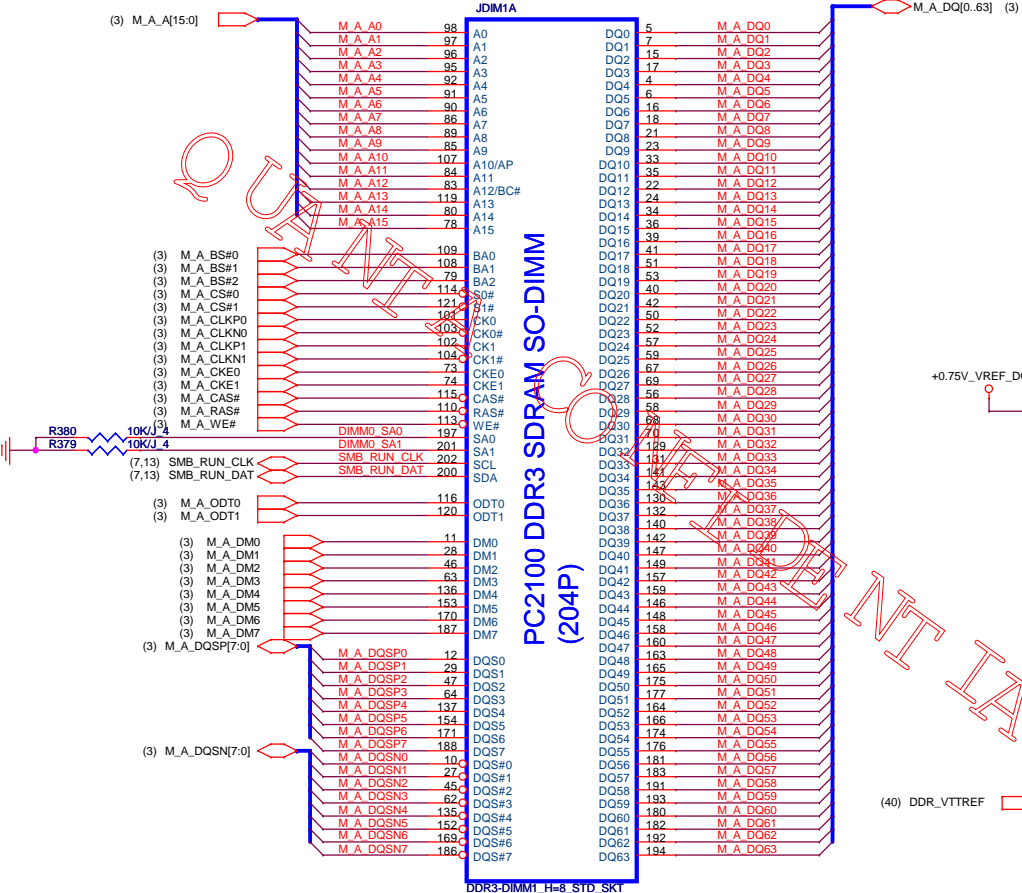
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

PROJECT : LZ3C
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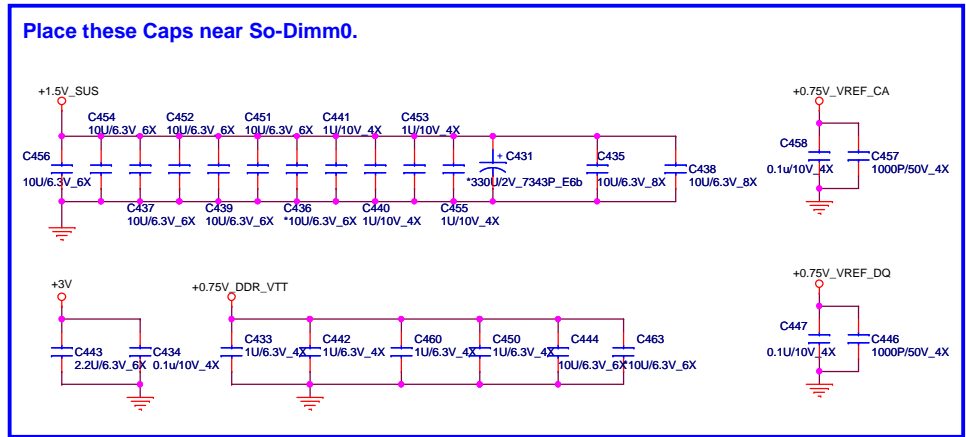
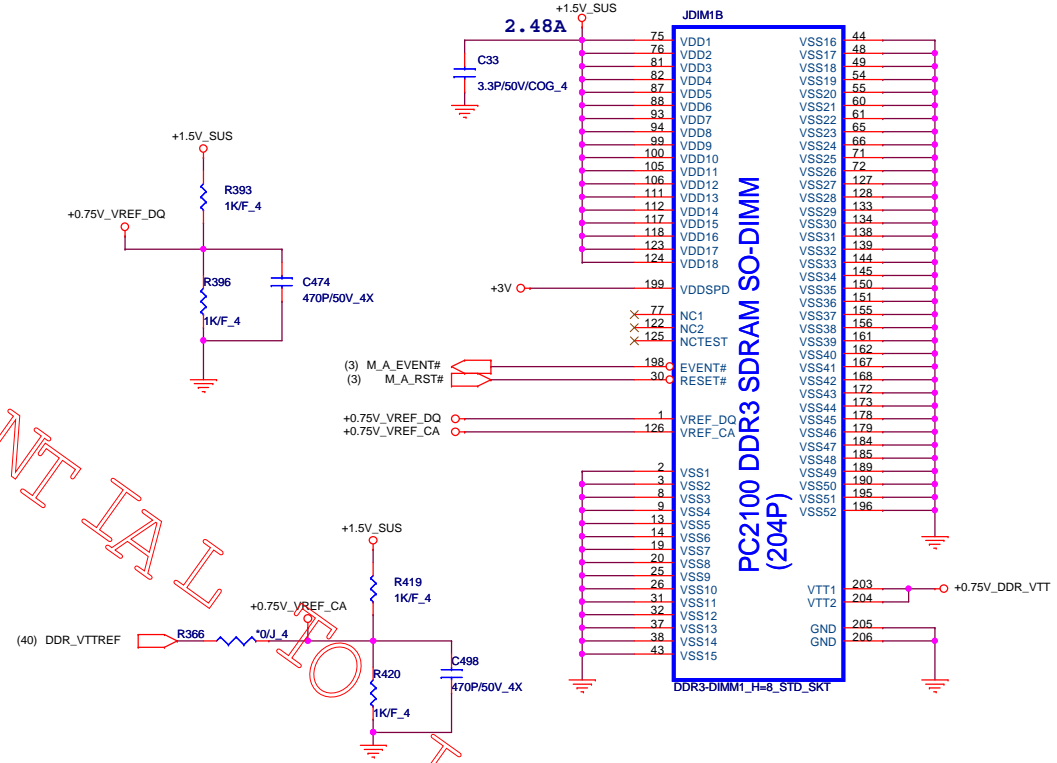
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FOR REVIEW

DDR STD (DDR)



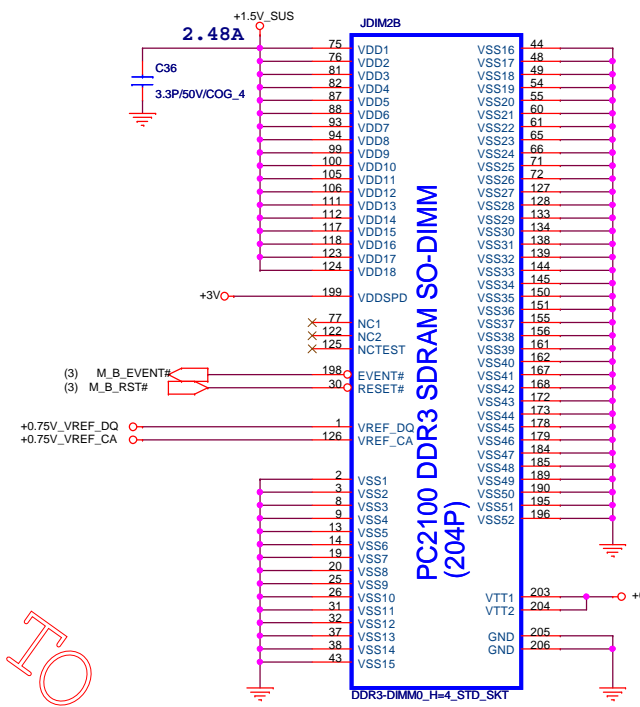
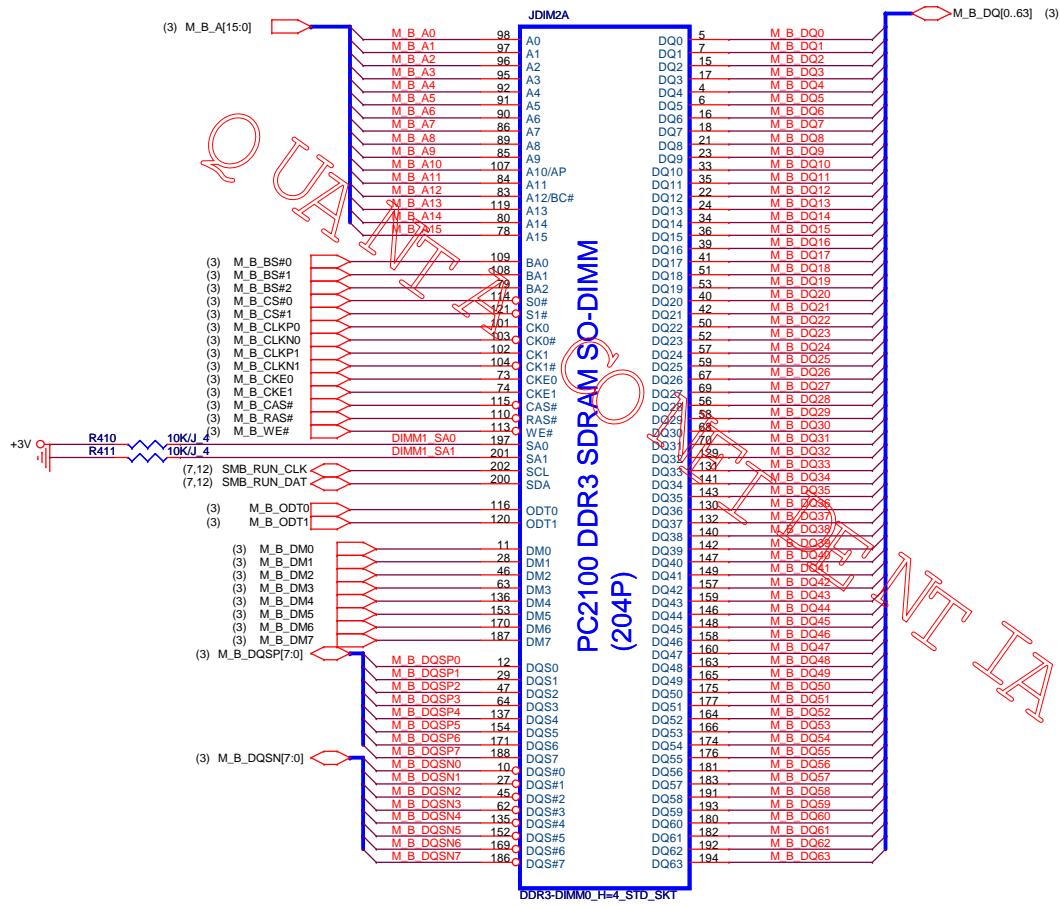
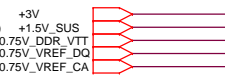
12



FOR REVIEW

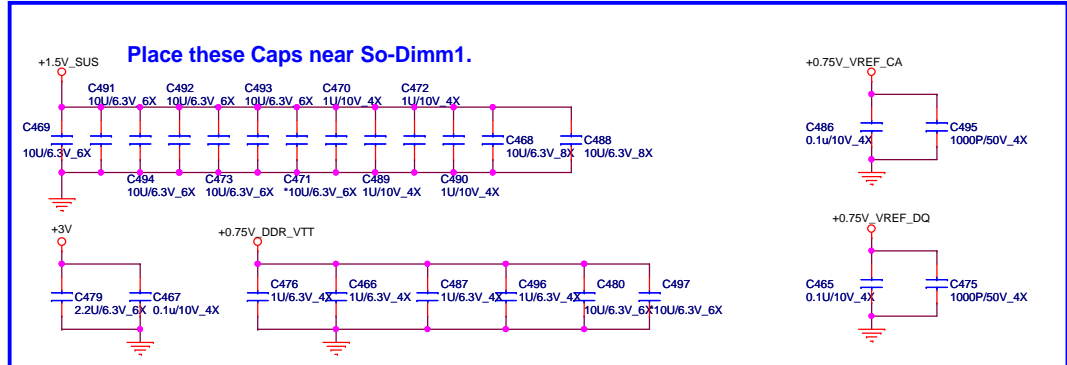
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	DDRIII SO-DIMM-0	2A
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PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)



INITIAL TO I C T FOR REVIEW

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Size	Document Number	Rev
	DDRIII SO-DIMM-1	2A
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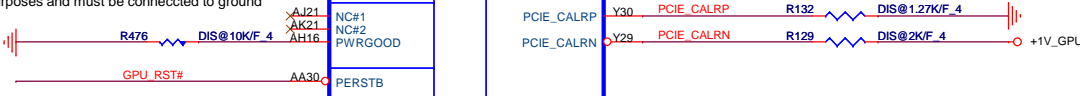
U30A

(15,17,18,46) +1V_GPU
(15,16,17,19,22,46) +3V_GPU

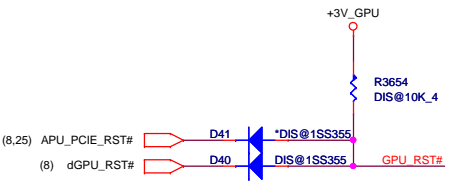


PCI EXPRESS INTERFACE

For M97 only Madison and Park the PWRGOOD ball is for test purposes and must be connected to ground



DIS@Seymour/Thames_M2



ICHT FOR REVIEW

PROJECT : LZ3C
Quanta Computer Inc.

Size	Document Number	Rev
	Seymour/Thames-M2 PCIE I/F	2A

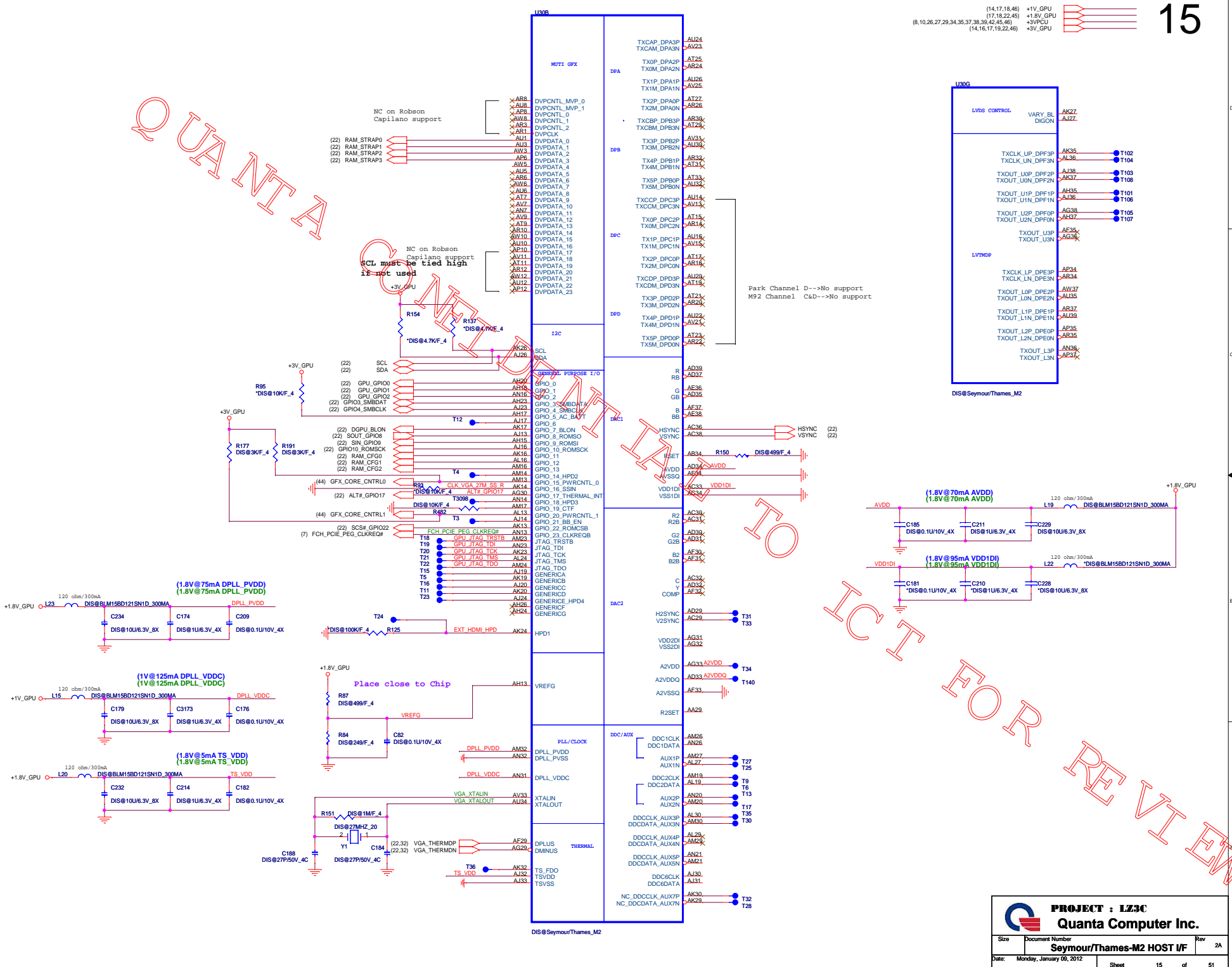
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(14,17,18,46) +1V_GPU
 (17,18,22,45) +1.8V_GPU
 (8,10,26,27,29,34,35,37,38,39,42,45,46) +3VPCU
 (14,16,17,19,22,46) +3V_GPU

QUANTA

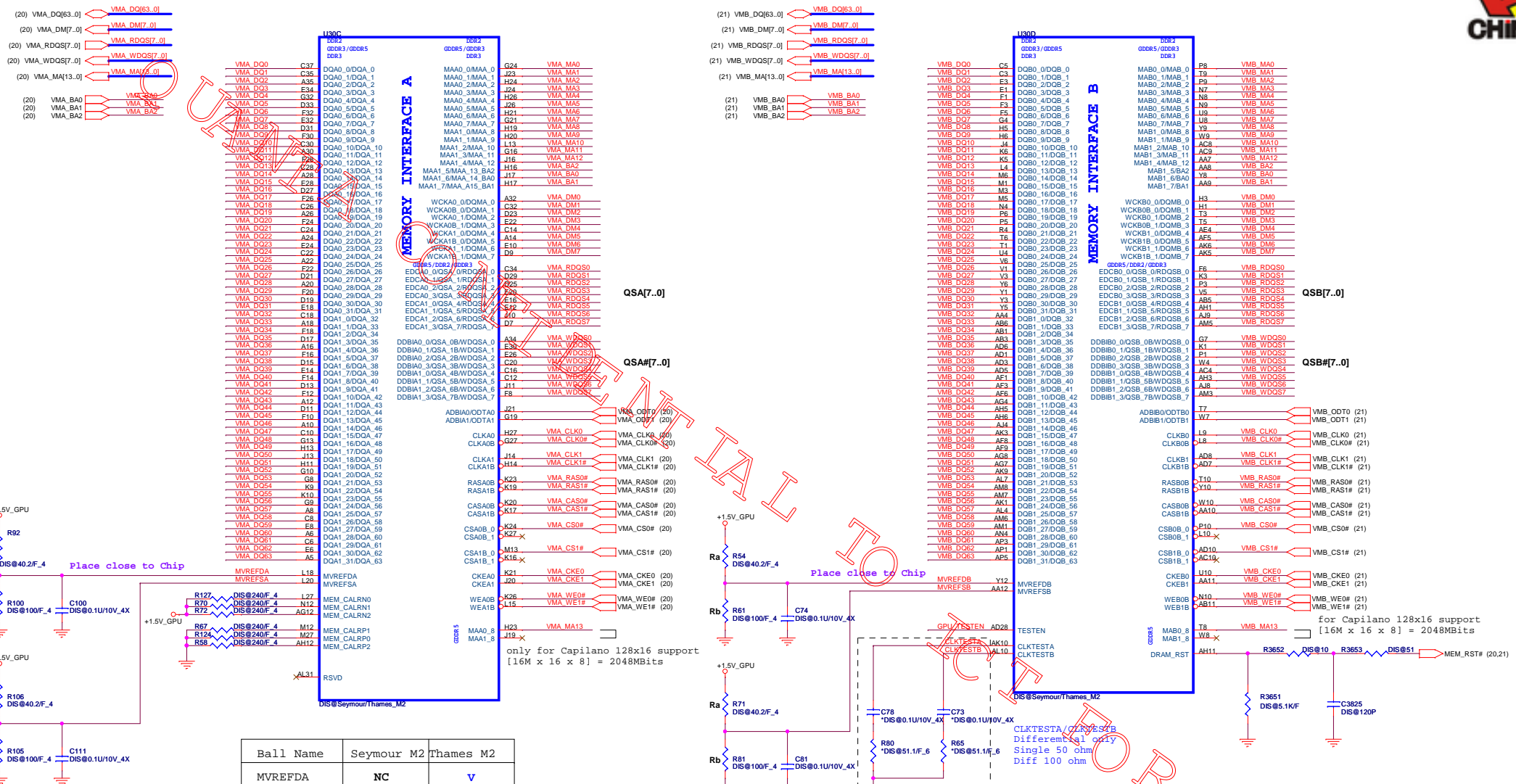
HOST I/O

FOR REVIEW



Thames XT use Memory Group

(14,15,17,19,22,46) +3V_GPU
(17,20,21,46,47) +1.5V_GPU



DDR3/GDDR3 Memory Stuff Option

Robson/Capilano	DDR3
MVDDQ	1.5V
Ra	40.2R
Rb	100R

Ball Name	Seymour M2	Thames M2
MVREFDA	NC	V
MVREFSA	NC	V
MVREFDB	V	V
MVREFSB	V	V
MEM_CALRN0	NC	V
MEM_CALRN1	V	V
MEM_CALRN2	NC	V
MEM_CALRP0	NC	V
MEM_CALRP1	V	V
MEM_CALRP2	NC	V

TESTEN	Description
0	Internal Debug use only
1	JTAG signals enable

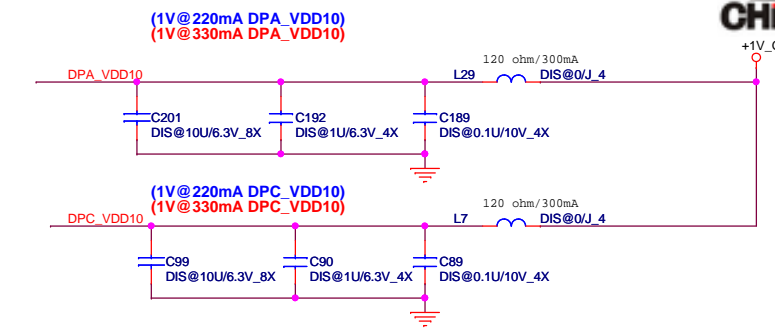
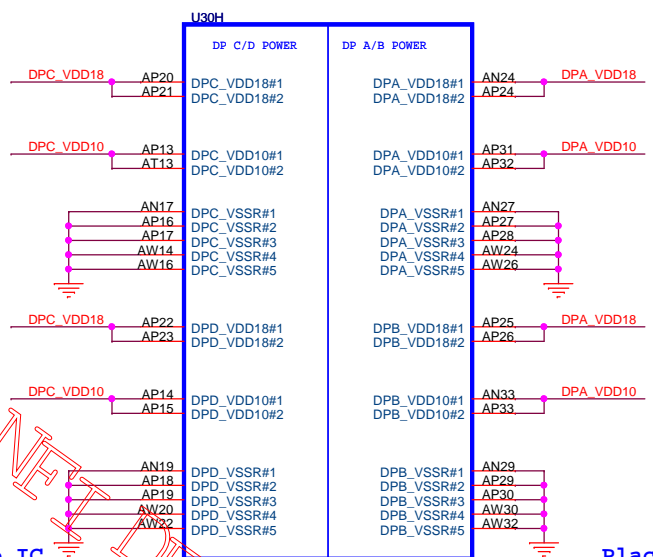
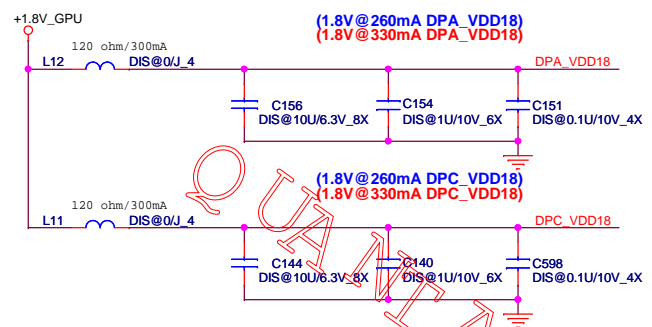
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Quanta Computer Inc.

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(15,17,22,45) +1.8V_GPU
(14,15,17,46) +1V_GPU

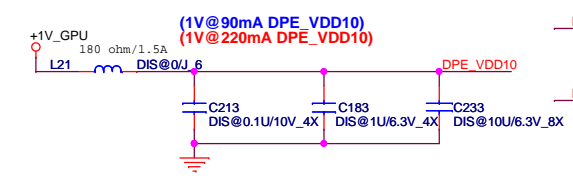
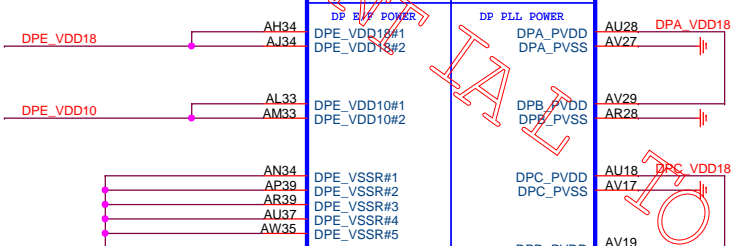
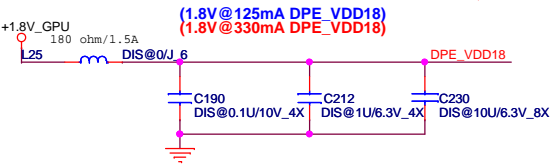


Place close to IC

R96 DIS@150/F_4 DPCD_CALR AW18

Place close to IC

AW28 DPAB_CALR R486 DIS@150/F_4



Place close to IC

R495 DIS@150/F_4 DPEF_CALR AM39

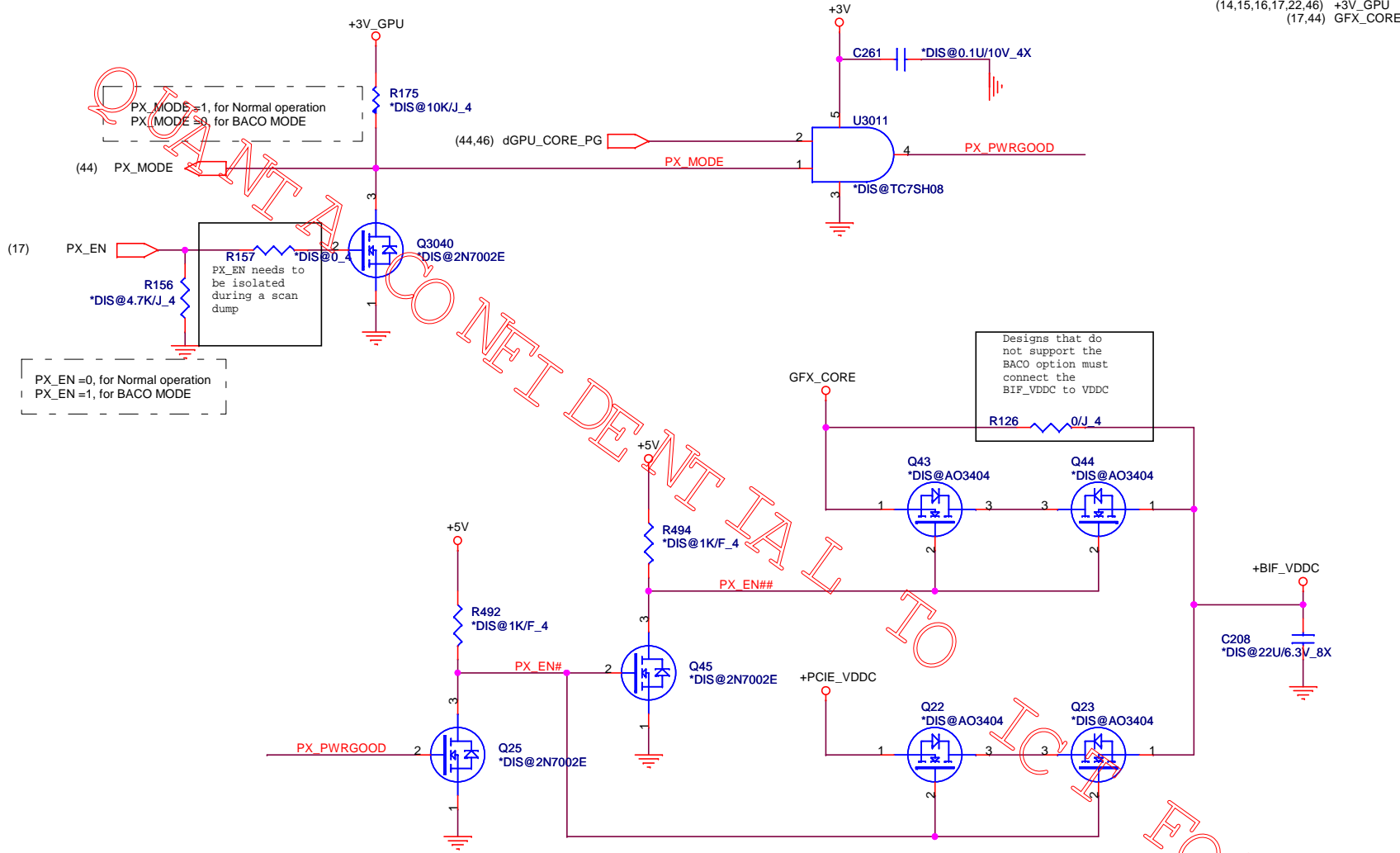
DIS@Seymour/Thames_M2

IC IT FOR

PROJECT : LZ3C
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	Seymour/Thame-M2 DPPW_GND	2A
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	Seymour -M2 BACO	2A
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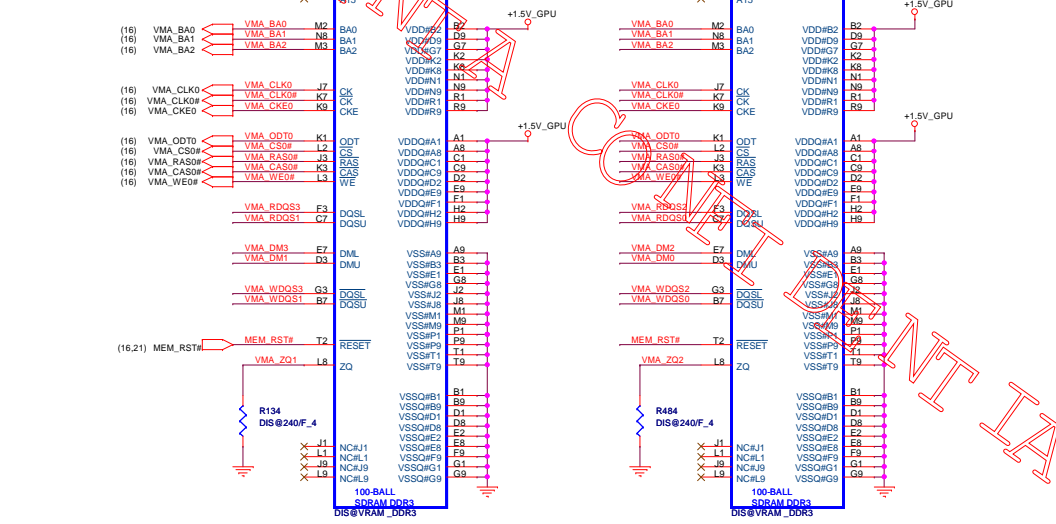
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

(16,17,21,46,47) +1.5V_GPU

20

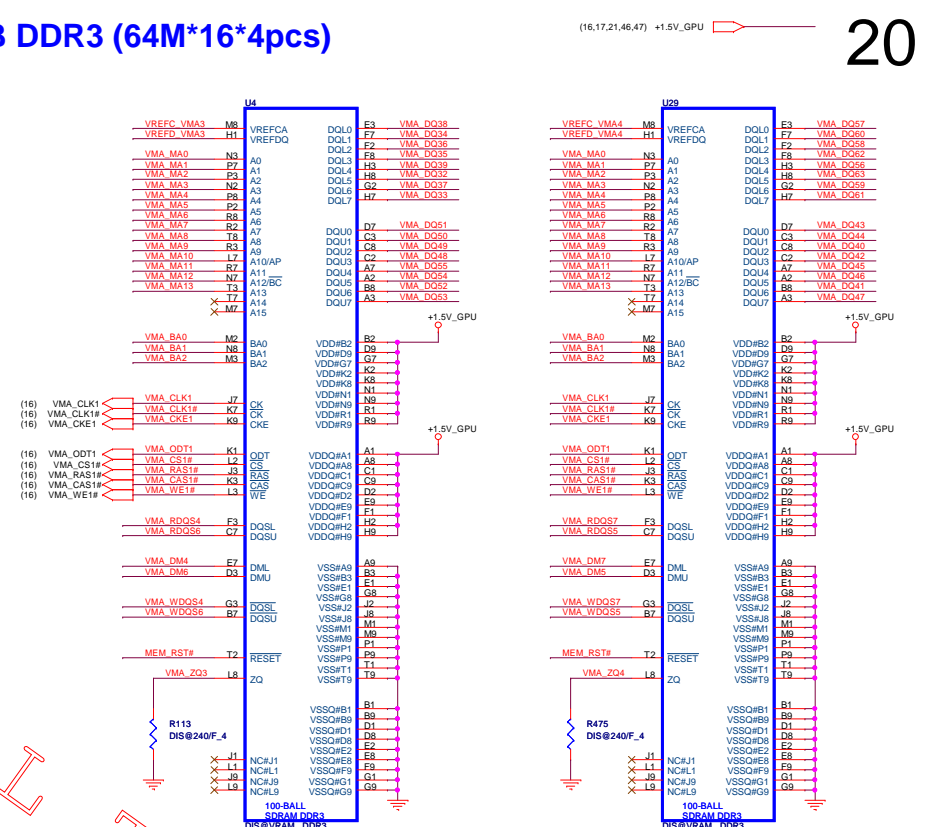


- (16) VMA_DQ[63..0] VMA_DM[63..0]
- (16) VMA_DM[7..0] VMA_DM7[0]
- (16) VMA_RDQS[7..0] VMA_RDQS7[0]
- (16) VMA_WDQS[7..0] VMA_WDQS7[0]
- (16) VMA_MA[13..0] VMA_MA13[0]



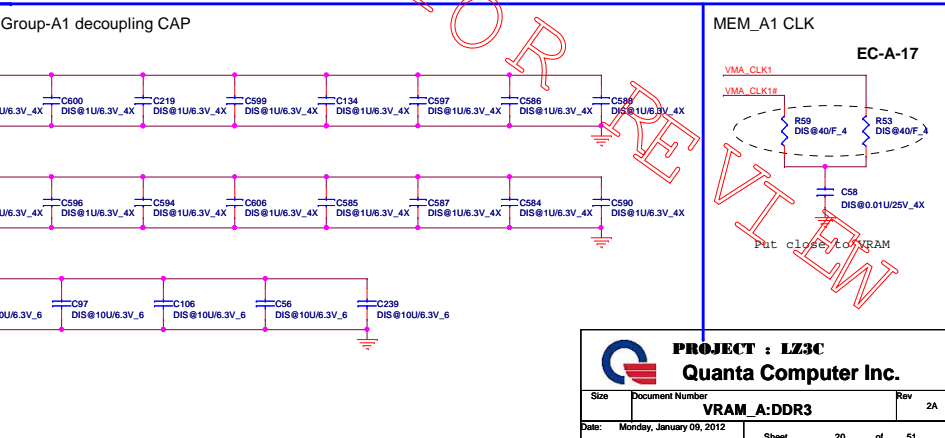
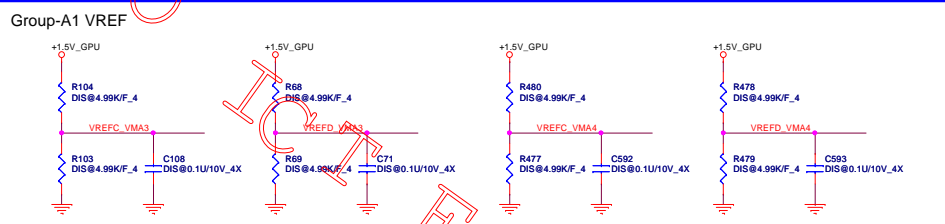
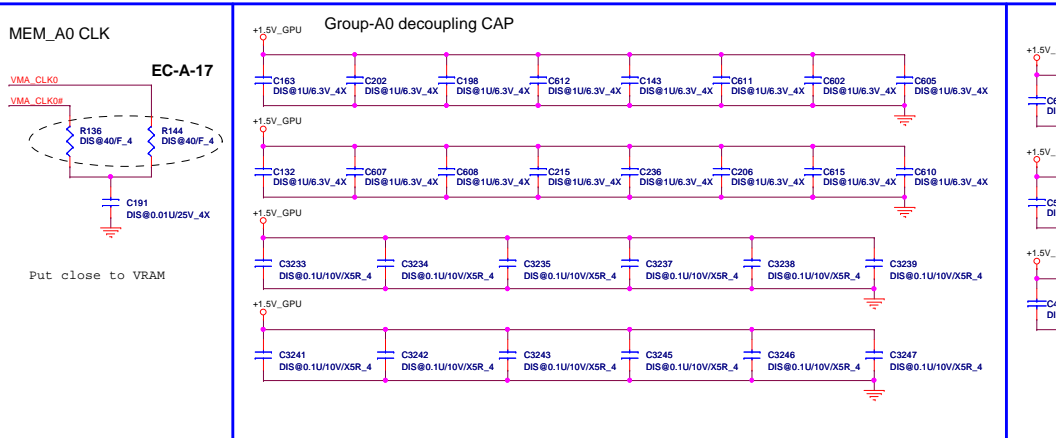
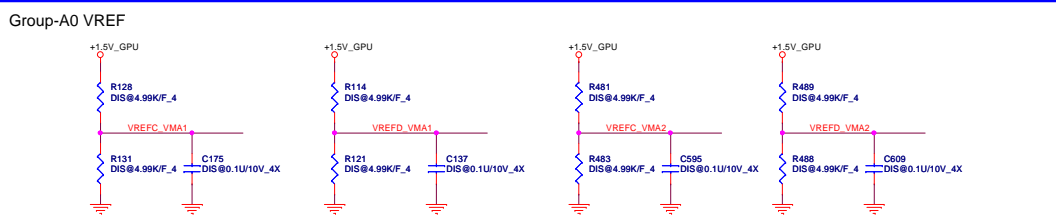
TOP Left

BOT Left



BOT Right

TOP Right



PROJECT : LZ3C
Quanta Computer Inc.

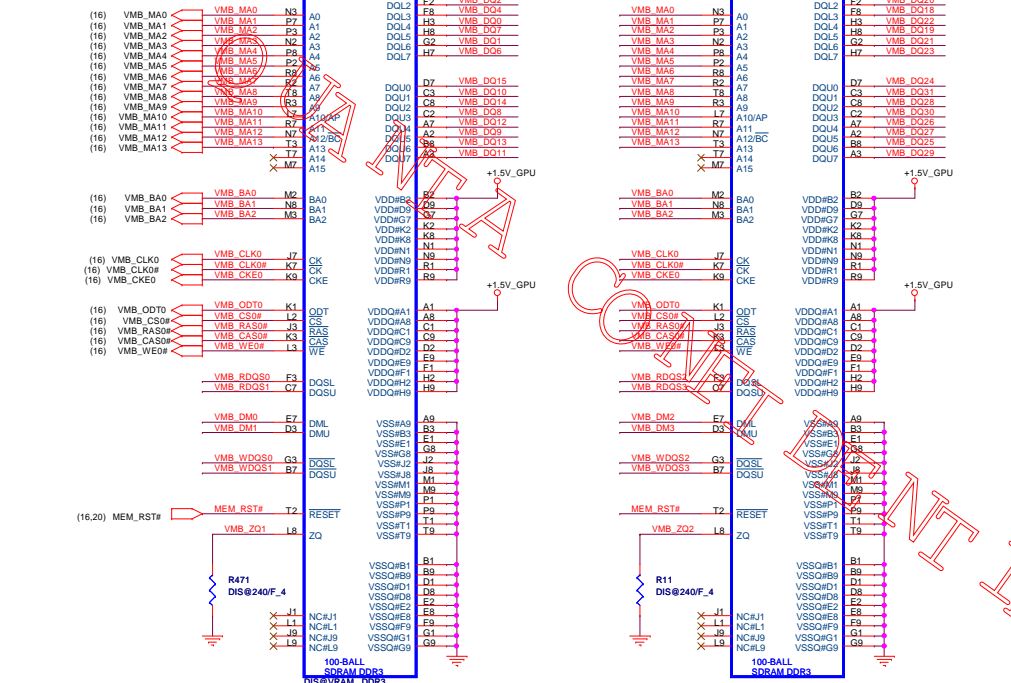
Size	Document Number	Rev
	VRAM A:DDR3	2A
Date:	Monday, January 09, 2012	Sheet 20 of 51

CHANNEL B: 512MB DDR3 (64M*16*4pcs)



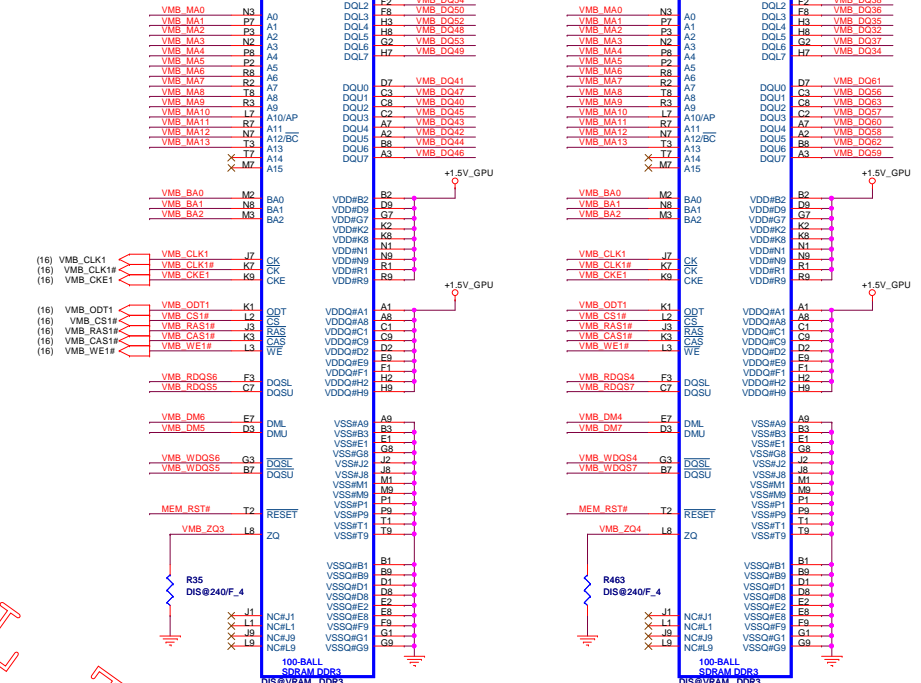
(16,17,20,46,47) +1.5V_GPU

- (16) VMB_DQ[63..0]
- (16) VMB_DM[7..0]
- (16) VMB_RDQS[7..0]
- (16) VMB_WDQS[7..0]
- (16) VMB_MA[13..0]



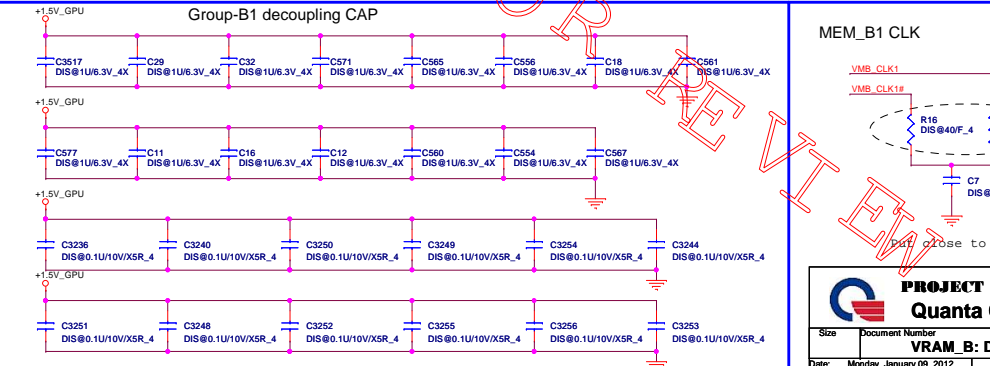
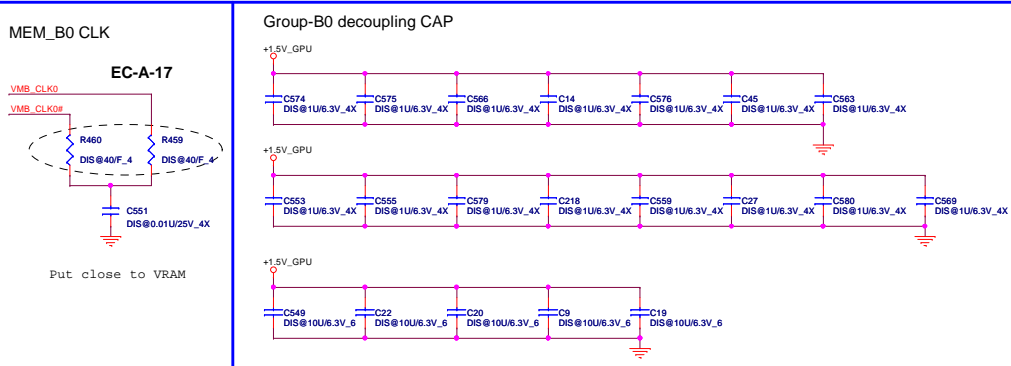
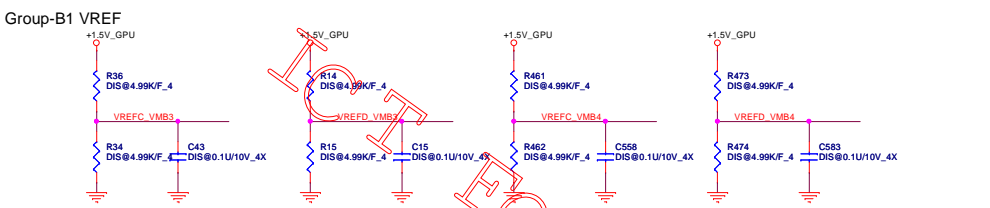
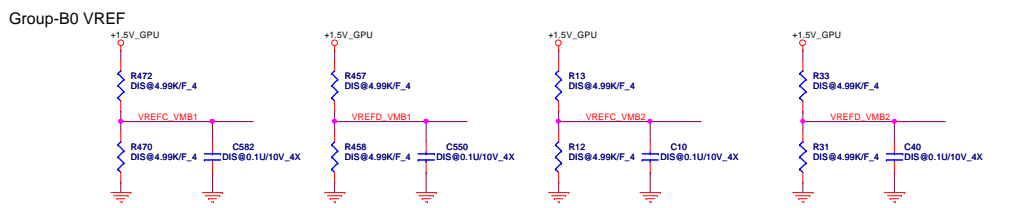
BOT Down

TOP Down



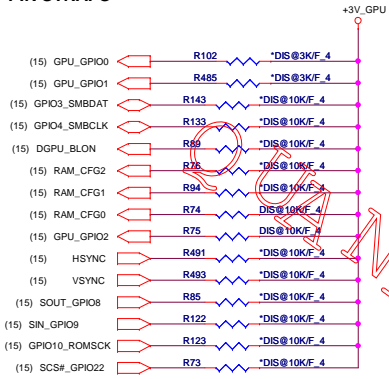
TOP Up

BOT Up



PROJECT : LZ3C
Quanta Computer Inc.
 Size Document Number Rev
VRAM_B: DDR3-64M*16*4PCS 2A
 Date: Monday, January 09, 2012 Sheet 21 of 51

PIN STRAPS

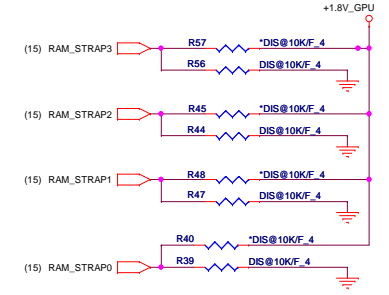


Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
HSYNC	VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

VRAM Memory TYPE

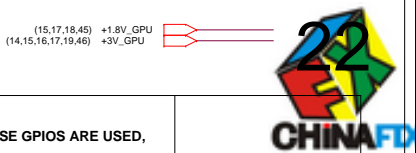
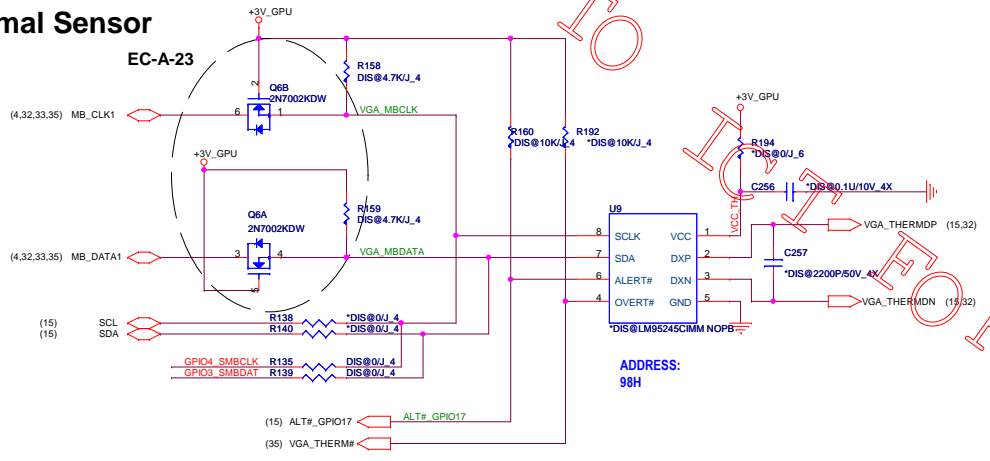
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 (64M*16-1Gb)	1GB	0	0	1	0
	H5TQ2G63BFR-11C	AKD5MGWTW00 (128M*16-1Gb)	2GB	0	0	0	0
	H5TQ2G63DFR-11C	AKD5MGWTW16 (128M*16-1Gb)	2GB	0	1	0	0
Samsung	K4W1G1646G-BC11	AKD5EGGT500 (64M*16-1Gb)	1GB	0	0	1	1
	K4W2G1646C-HC11	AKD5MGWT500 (128M*16-1Gb)	2GB	0	0	0	1



CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX_M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	1	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[10] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor



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Quanta Computer Inc.

Size: _____ Document Number: _____ Rev: 2A

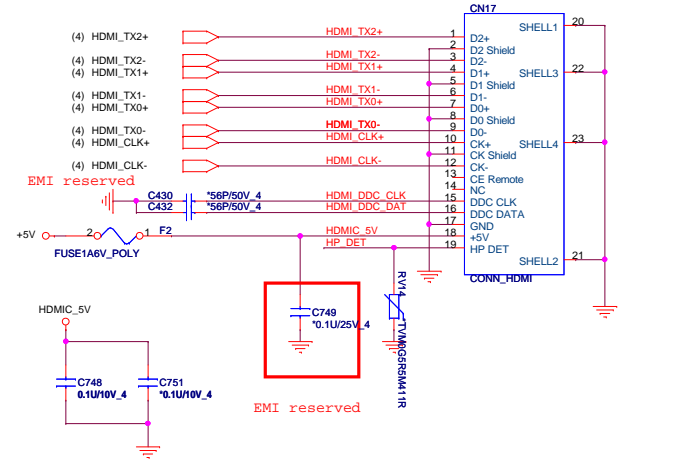
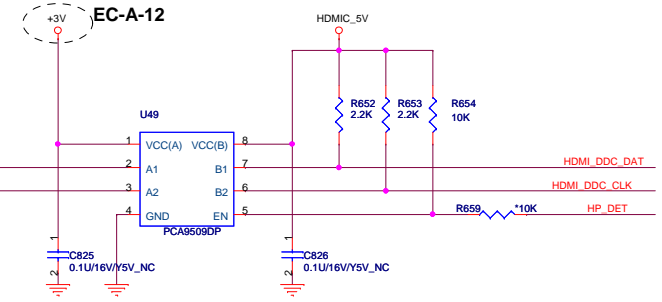
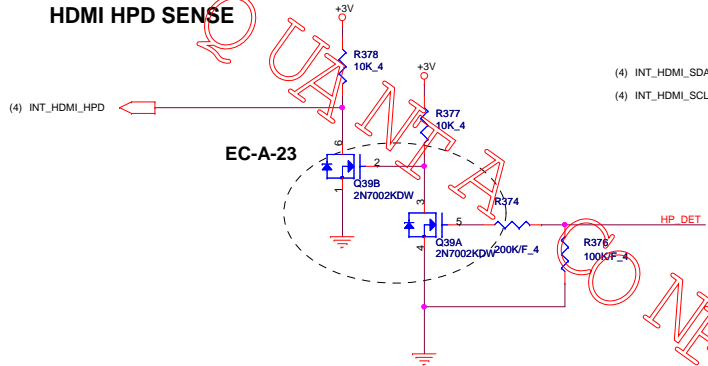
Memory strip/Thermal

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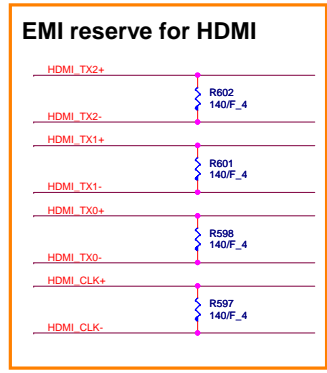
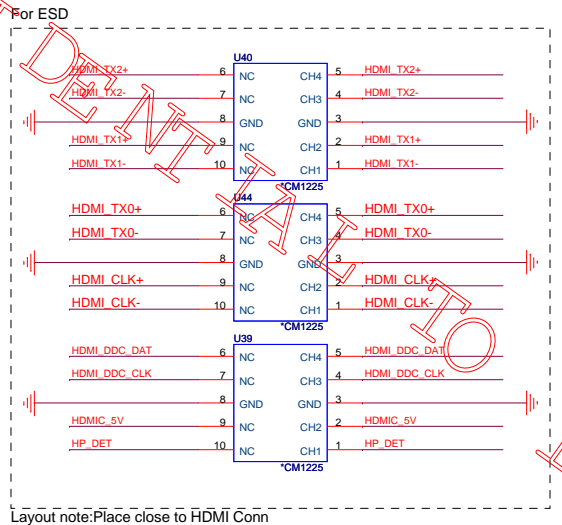
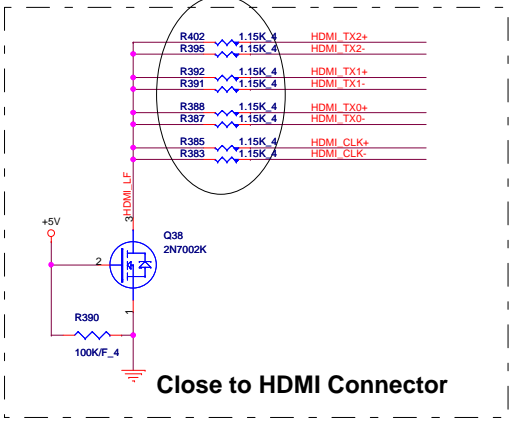


(4,6,25,30,41,43) +1.5V
 (9,19,24,25,28,29,32,33,37,47) +5V
 (4,7,8,9,10,11,12,13,19,25,26,27,28,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +3V

HDMI HPD SENSE



EC-B-05

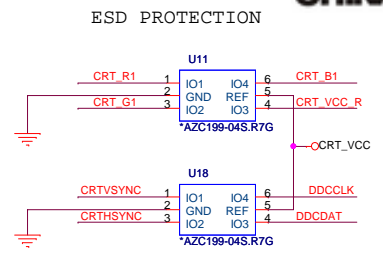
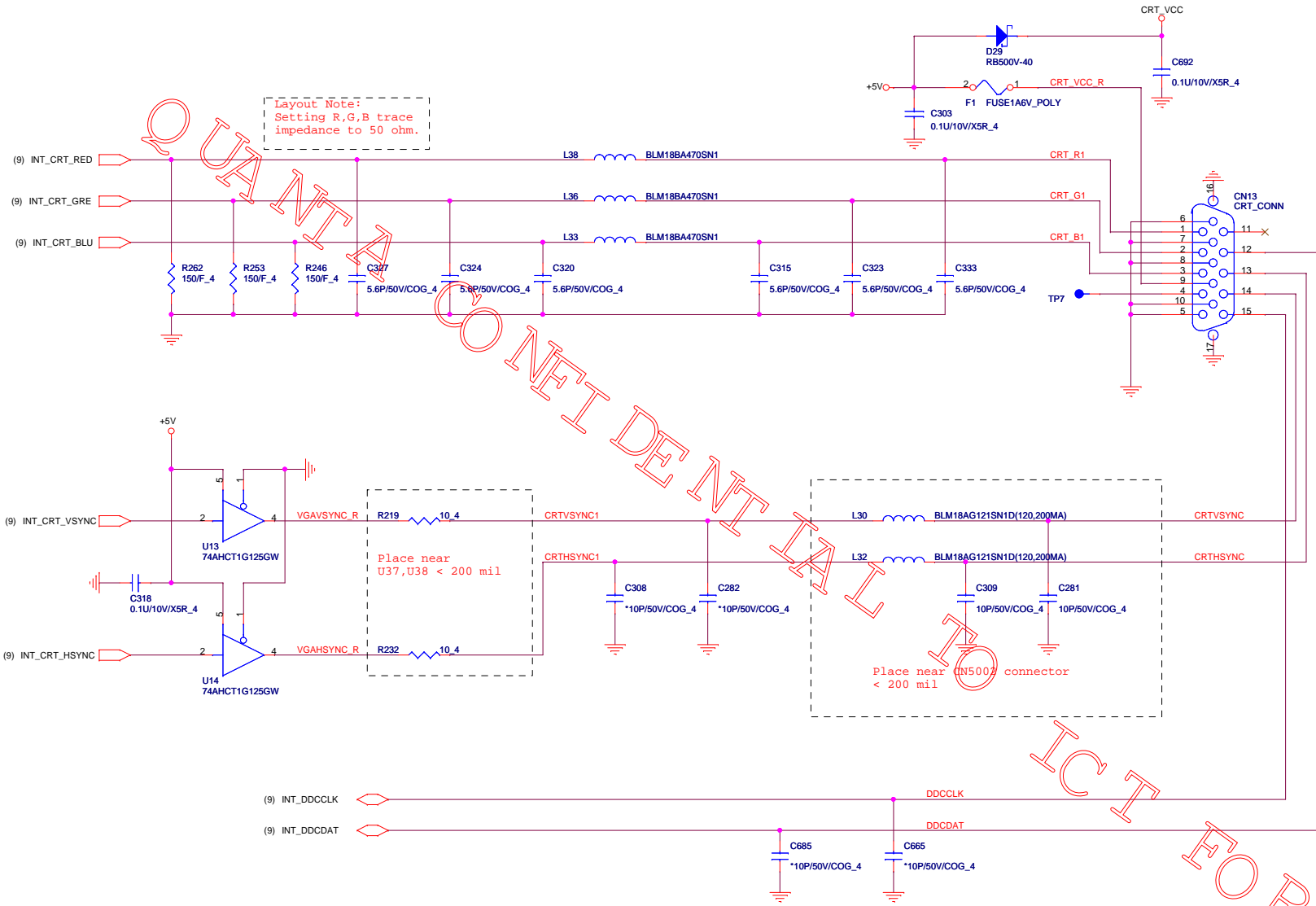


		PROJECT : LZ3C Quanta Computer Inc.	
Size Custom	Document Number	HDMI CONN	Rev 2A
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FOR REVIEW



Layout Note:
Setting R,G,B trace impedance to 50 ohm.

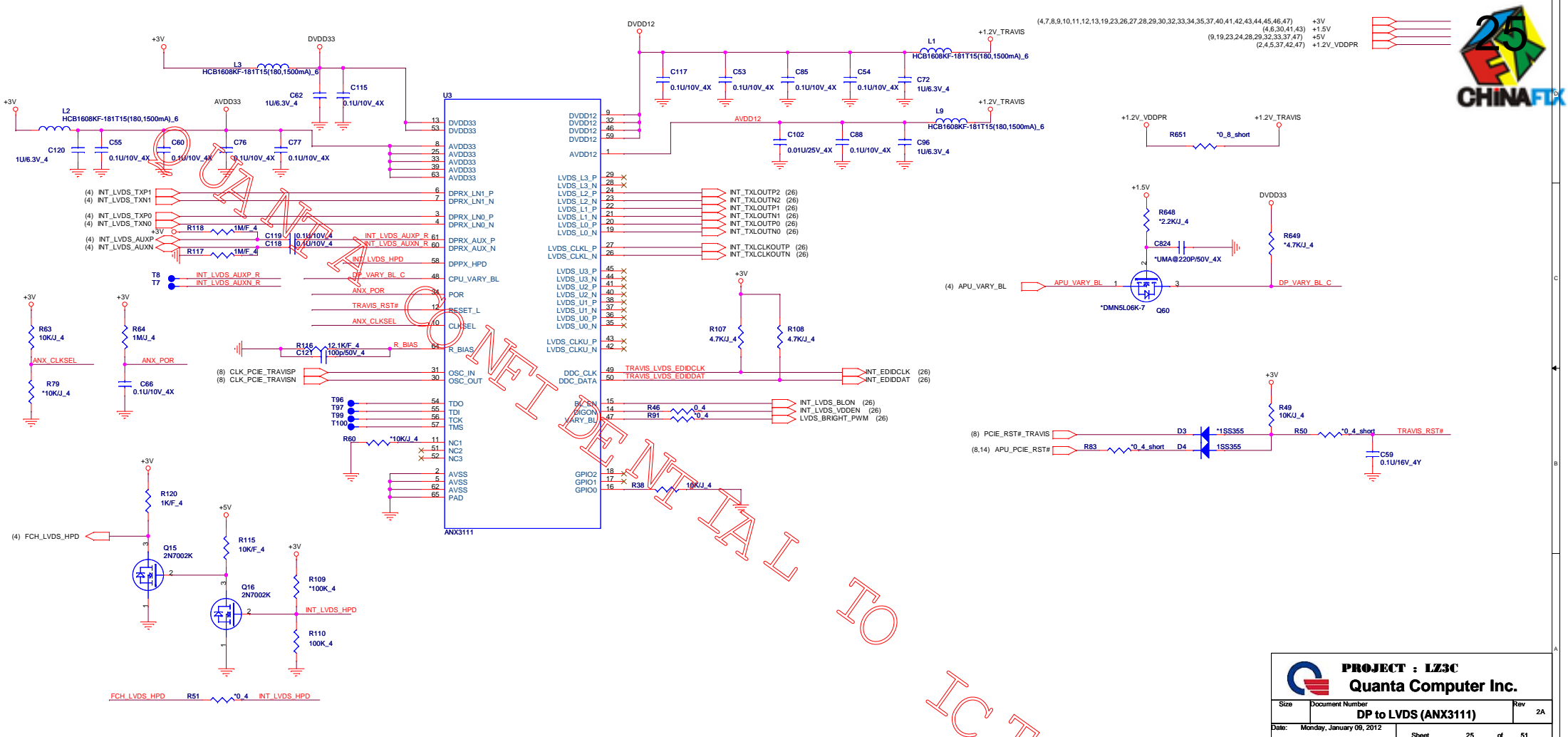


Place near U37,U38 < 200 mil

Place near CN5002 connector < 200 mil

REVIEW

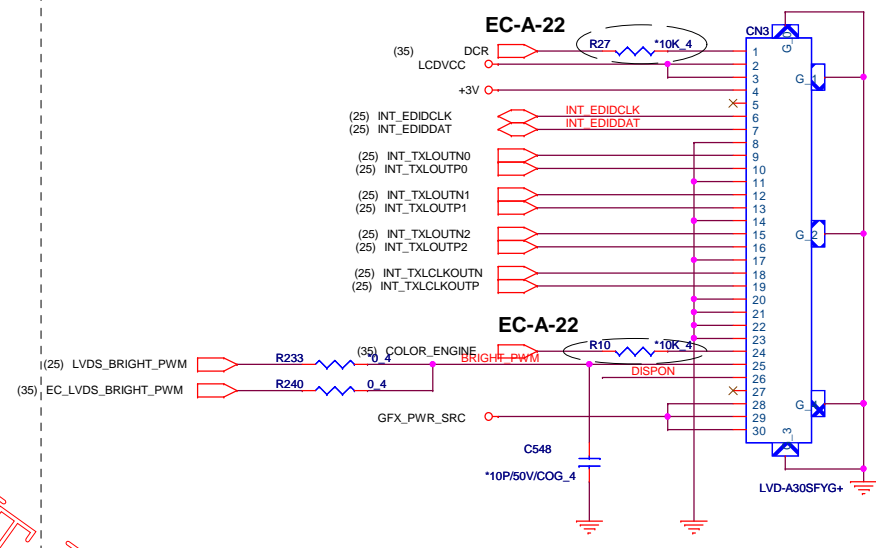
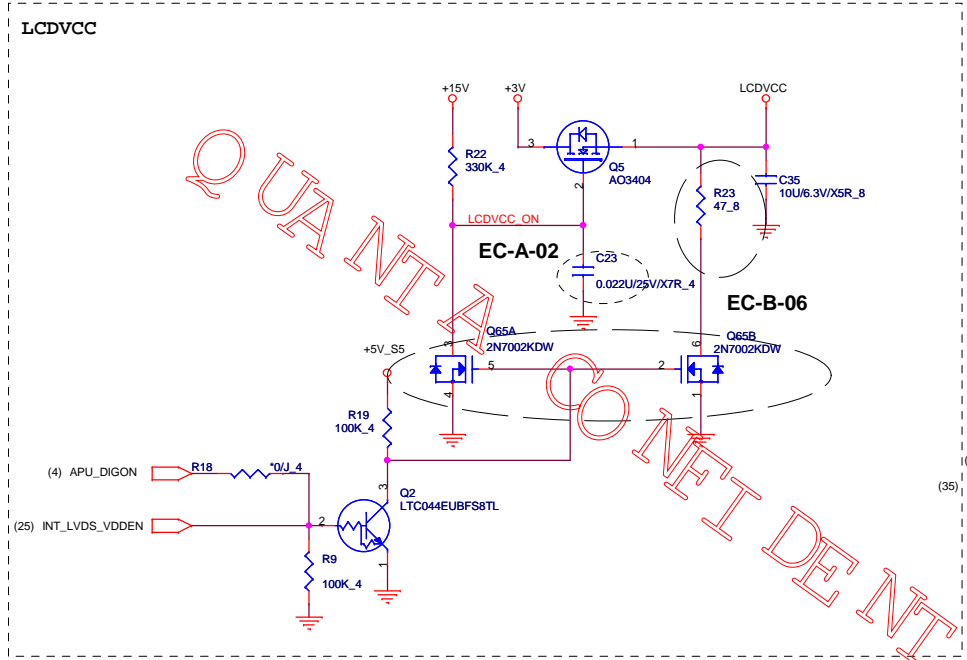
PROJECT : LZ3C		
Quanta Computer Inc.		
Size Custom	Document Number CRT_CONN	Rev 2A
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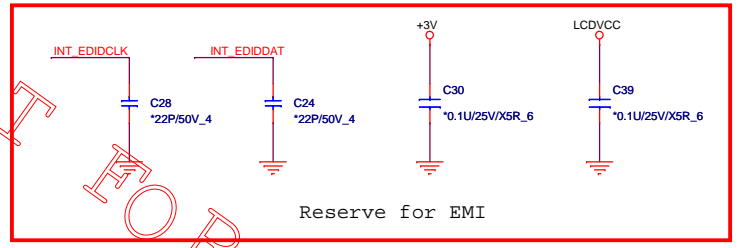
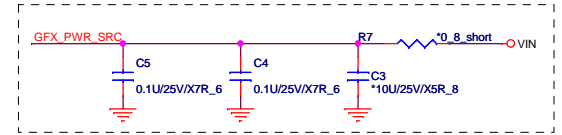
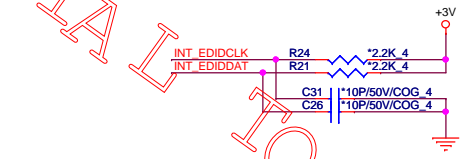
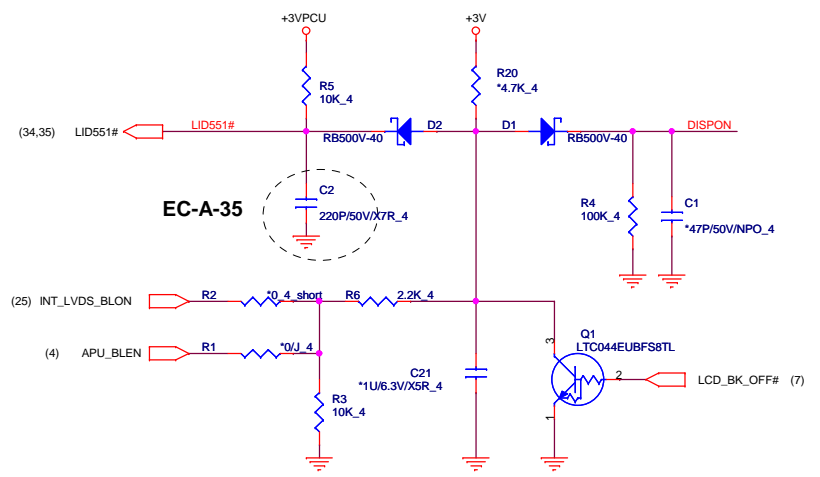
		PROJECT : LZ3C	
		Quanta Computer Inc.	
Size	Document Number	Rev	2A
DP to LVDS (ANX3111)			
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(4,7,8,9,10,11,12,13,19,23,25,27,28,29,30,32,33,34,35,37,40,41,42,43,44,45,46,47)
 (10,29,33,37,39,41,46)
 (31,34,37,47)
 (8,10,27,29,34,35,37,38,39,42,45,46)

+3V
 +15V
 +5V_S5
 +3VPCU

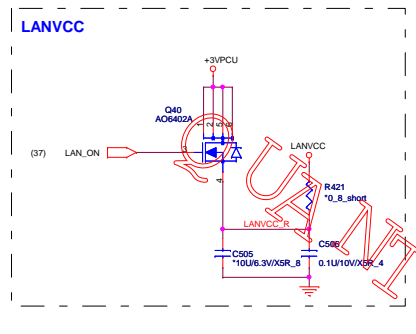


back light

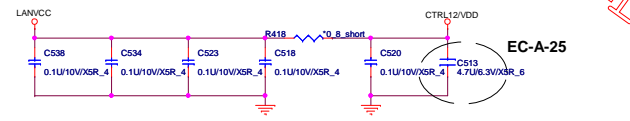
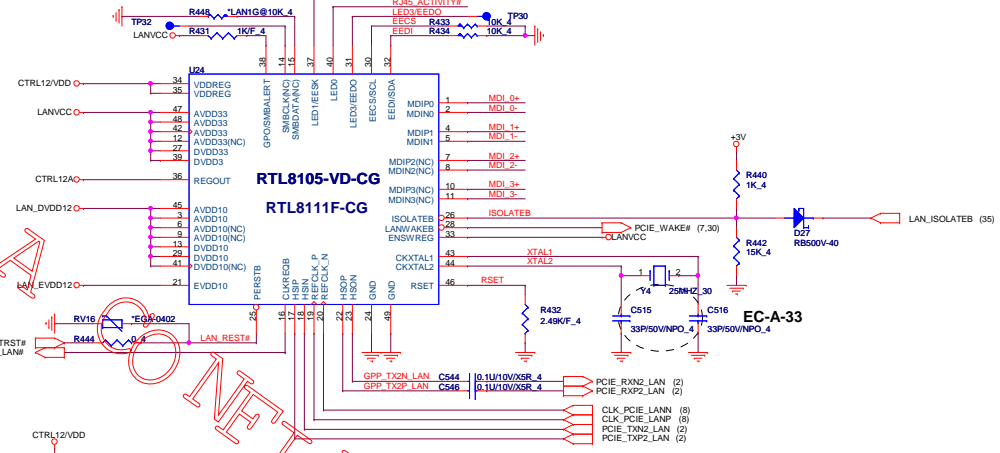


PROJECT : LZ3C
Quanta Computer Inc.

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* R448 open when use RTL8105E

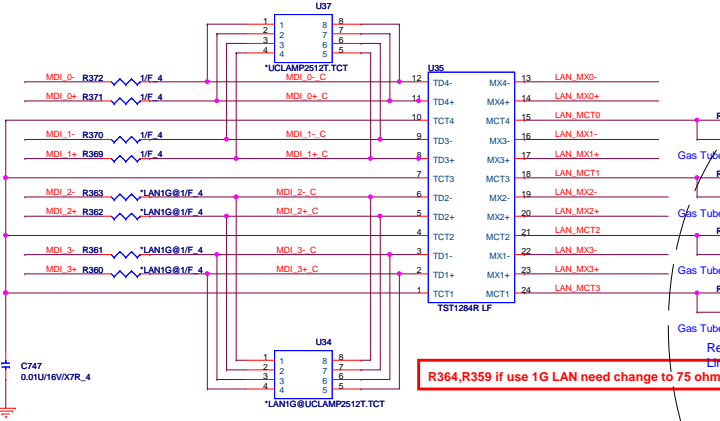


* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40.
 Place C5113, C5094 closed to U5006 pins44,45.

* C476 and C472 are for U24 LAN_EVDD12 pin 21.

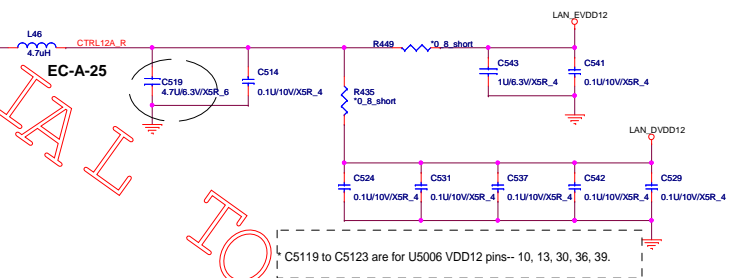
Layout: All termination signal should have 20 mil trace

Transformer



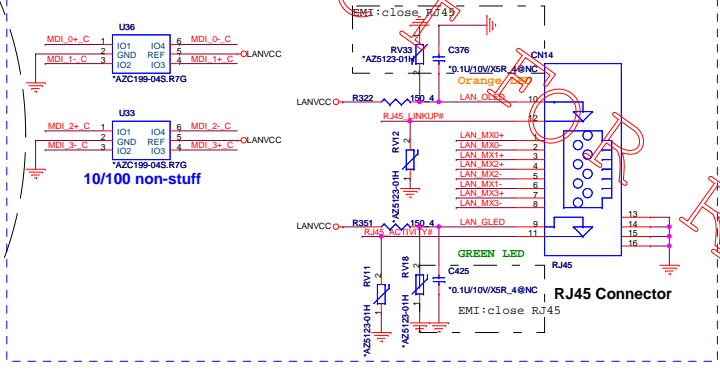
Layout: All termination signal should have 30 mil trace

R364, R359 if use 1G LAN need change to 75 ohm



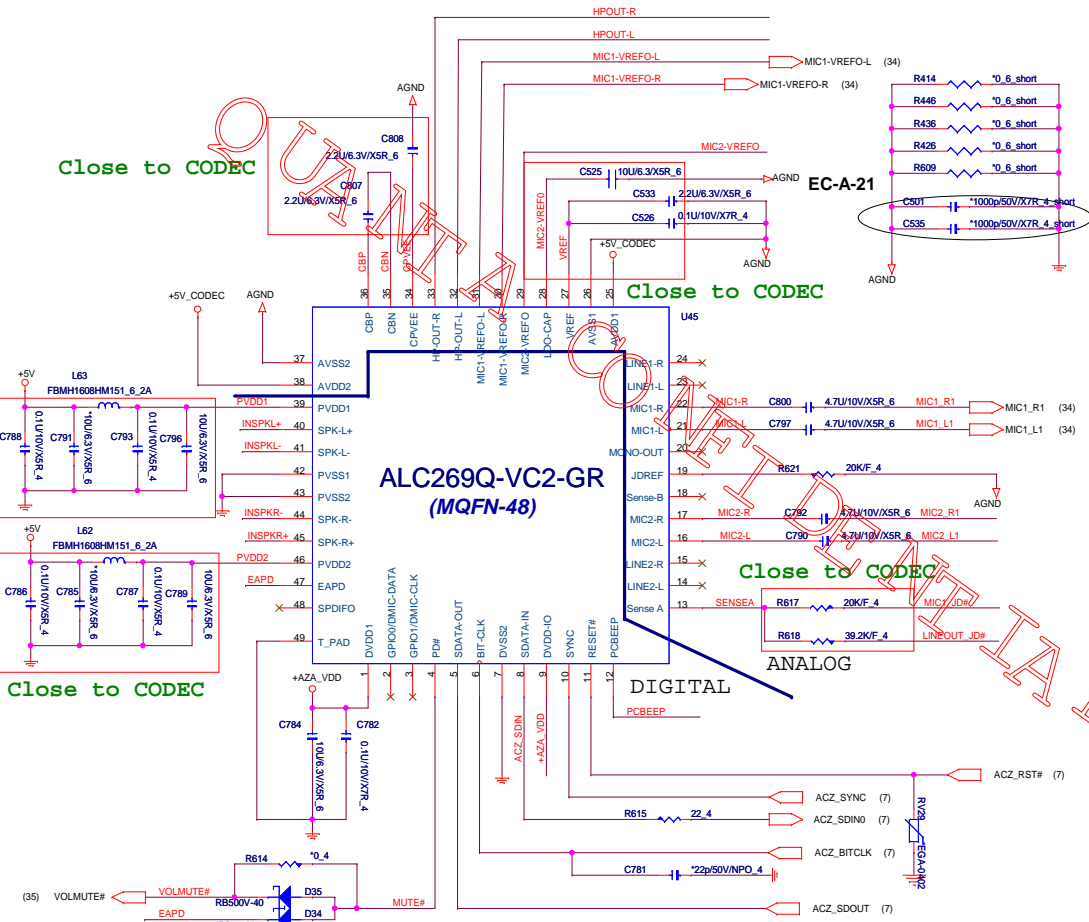
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

RJ45 Connector

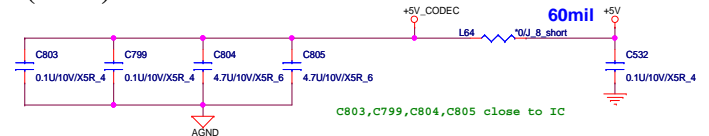


REVIEW

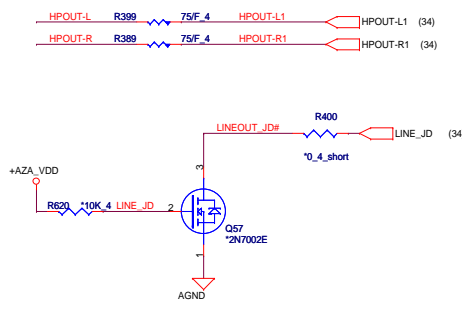
CODEC(ADO)



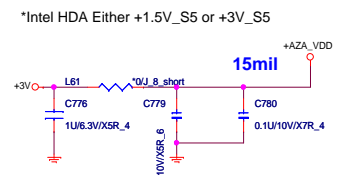
Codec Power(ADO)



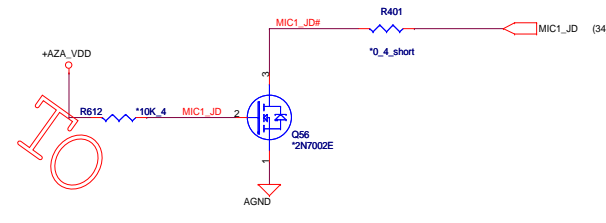
Earphone(AMP)



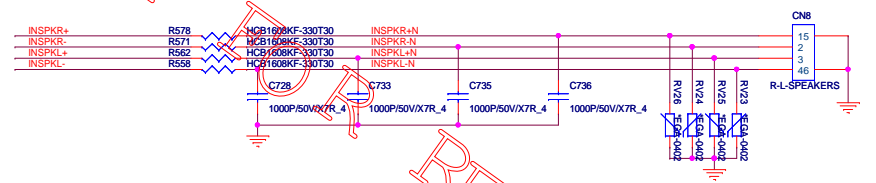
HDA Power(ADO)



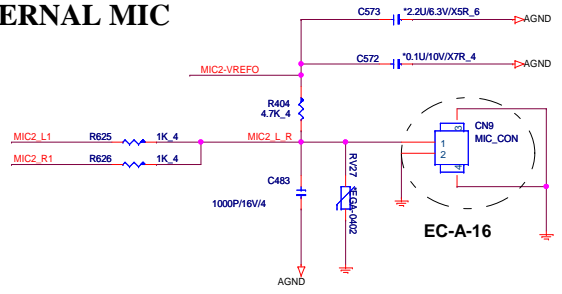
System MIC(AMP)



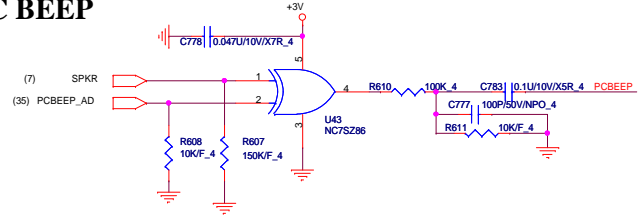
Speaker(AMP)



INTERNAL MIC



PC BEEP

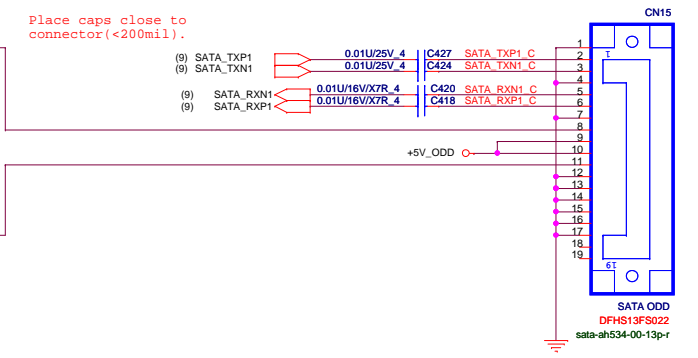
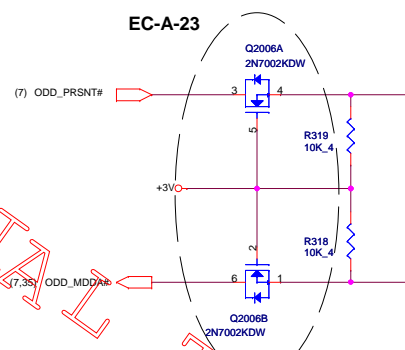
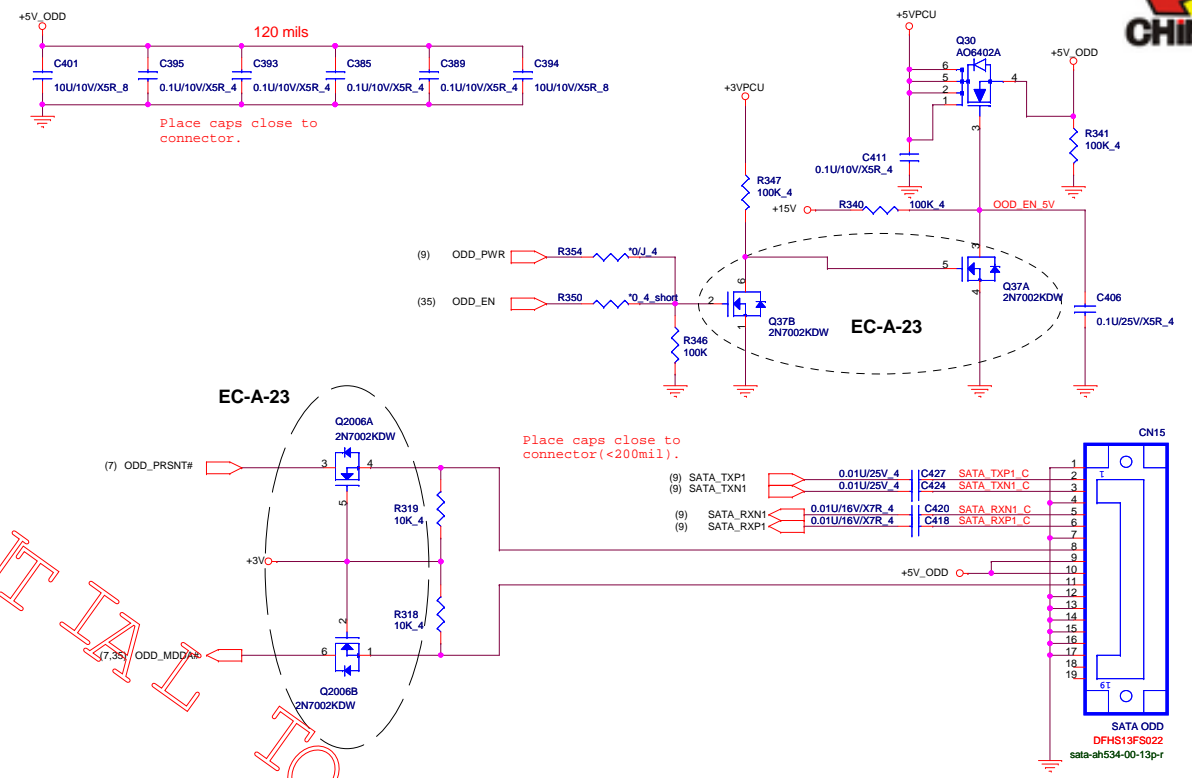


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Quanta Computer Inc.		
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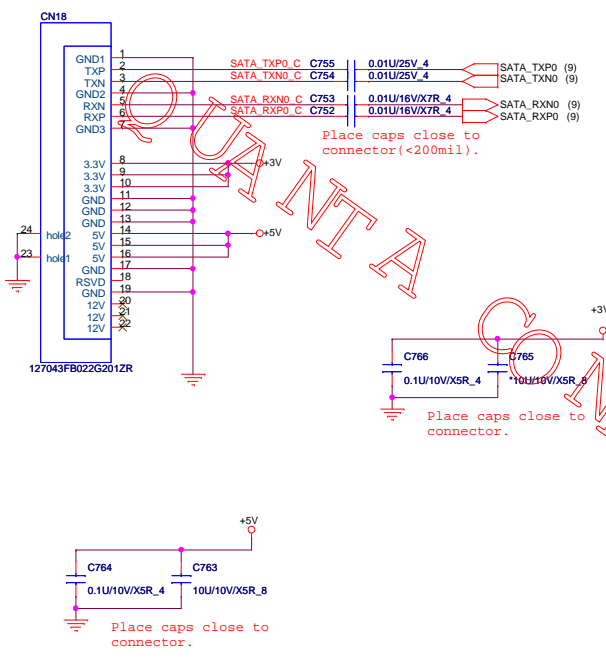


(4,7,8,9,10,11,12,13,19,23,25,26,27,28,30,32,33,34,35,37,40,41,42,43,44,45,46,47) +5V_S5
 (37,38,39,40,41,42,43,44,45,46) +3V
 (8,10,26,27,34,35,37,38,39,42,45,46) +3VPCU
 (10,26,33,37,39,41,46) +15V

SATA ODD Connector.



SATA HDD Connector.

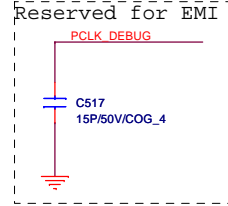


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Quanta Computer Inc.		
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SATA HDD/CD-ROM		
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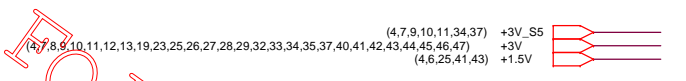
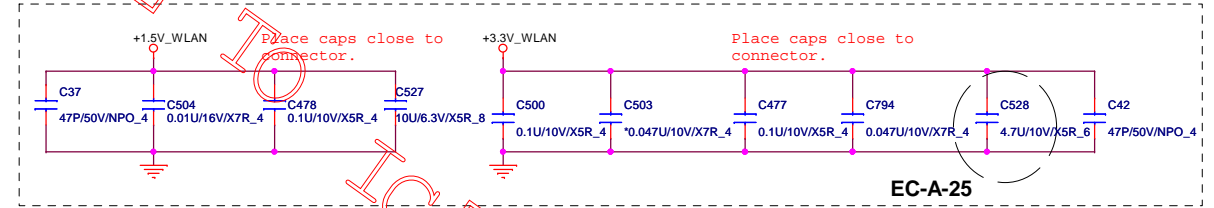
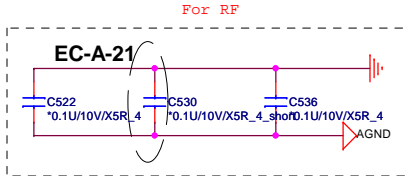
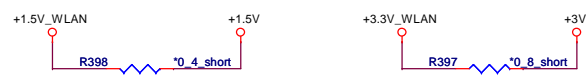
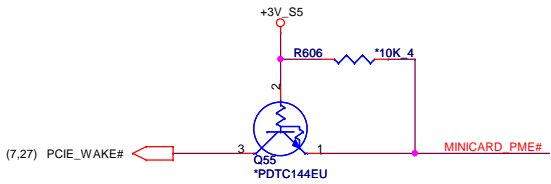
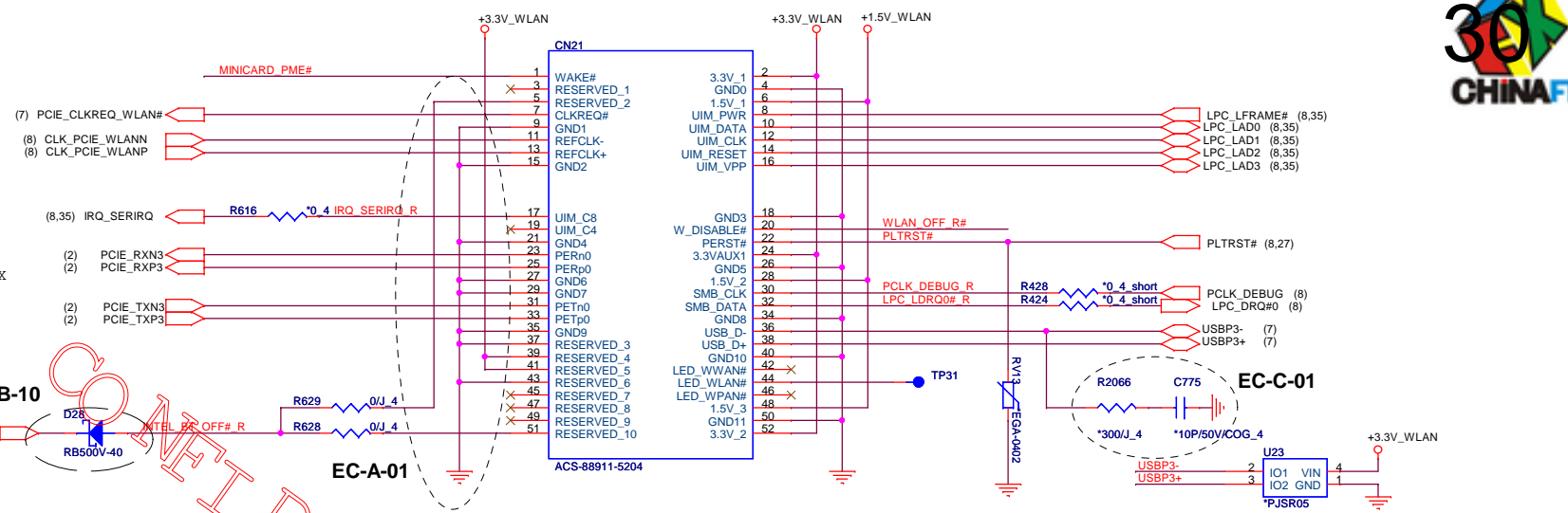
REVIEW

CONFIDENTIAL TO IC T FOR REVIEW

MiniCard WLAN connector



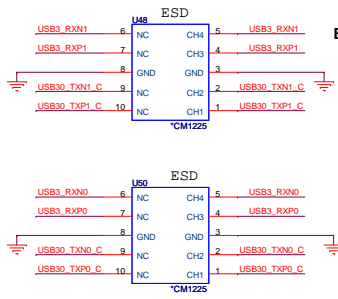
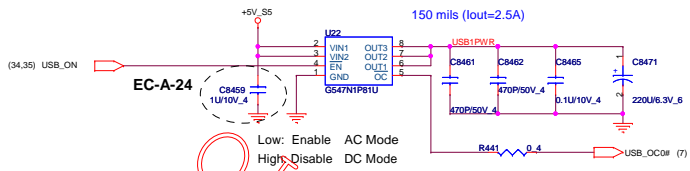
PCI-Express TX and RX direct to connector



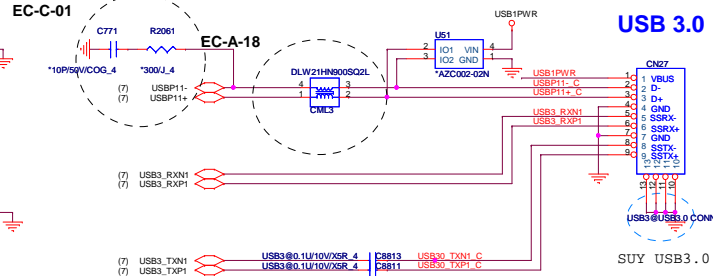
PROJECT : LZ3C
Quanta Computer Inc.

Size: Custom	Document Number: MINI-Card WLAN	Rev: 2A
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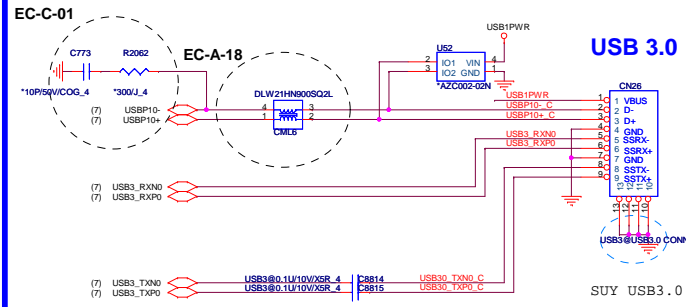
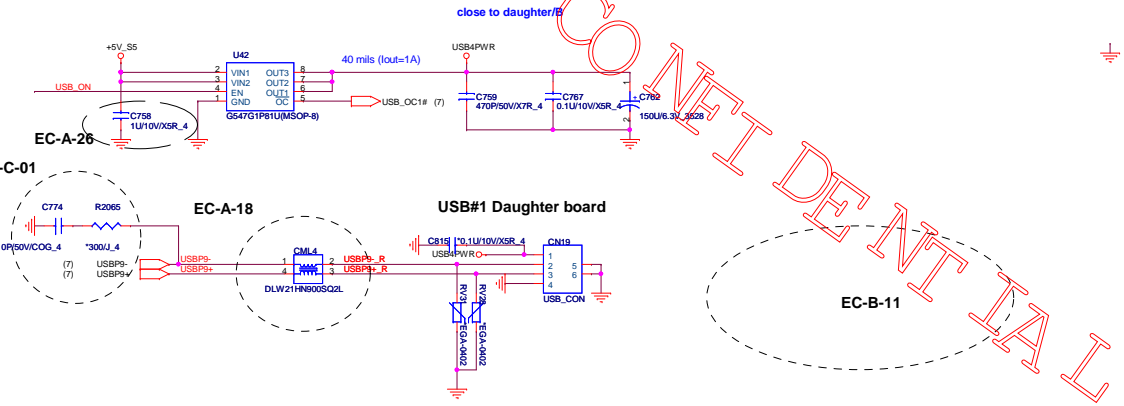
QUANTA
CONFIDENTIAL
FOR REVIEW



USB3.0 X 2/USB2.0 COMBO



USB2.0*1



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Quanta Computer Inc.		
Size: Custom	Document Number: USB3.0 x 2/USB 2.0 x 1	Rev: 2A
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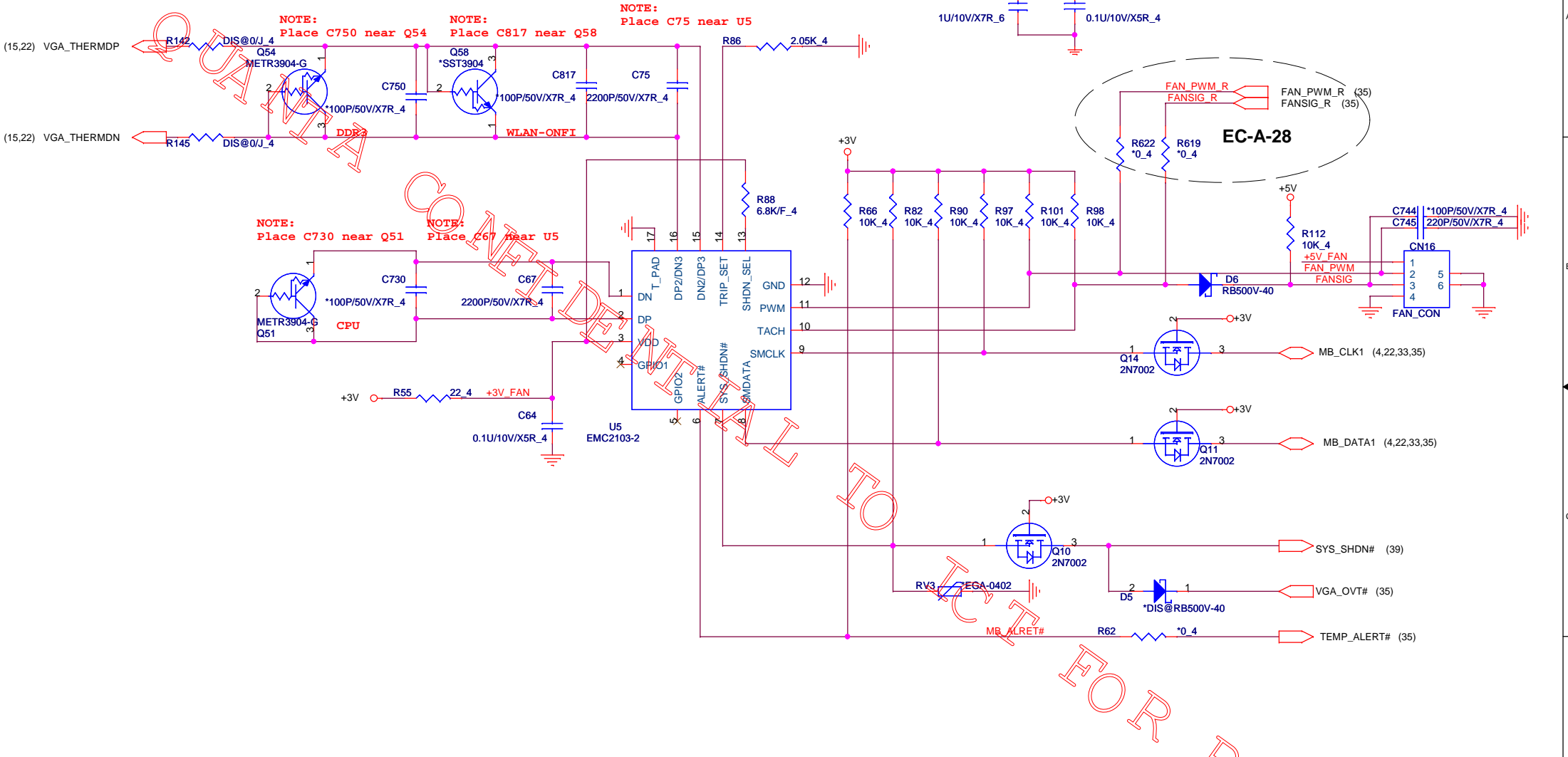
QUANTA CONFIDENTIAL

TO ICT FOR REVIEW

FAN CONTROL

(4,7,8,9,10,11,12,13,19,23,25,26,27,28,29,30,33,34,35,37,40,41,42,43,44,45,46,47) +3V
 (9,19,23,24,25,28,29,33,37,47) +5V

32



(15,22) VGA_THERMDP
 (15,22) VGA_THERMDN

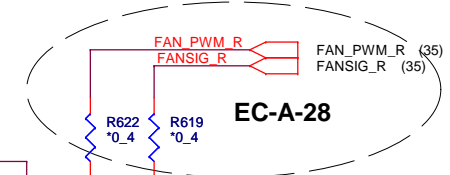
NOTE:
Place C750 near Q54

NOTE:
Place C817 near Q58

NOTE:
Place C75 near U5

NOTE:
Place C730 near Q51

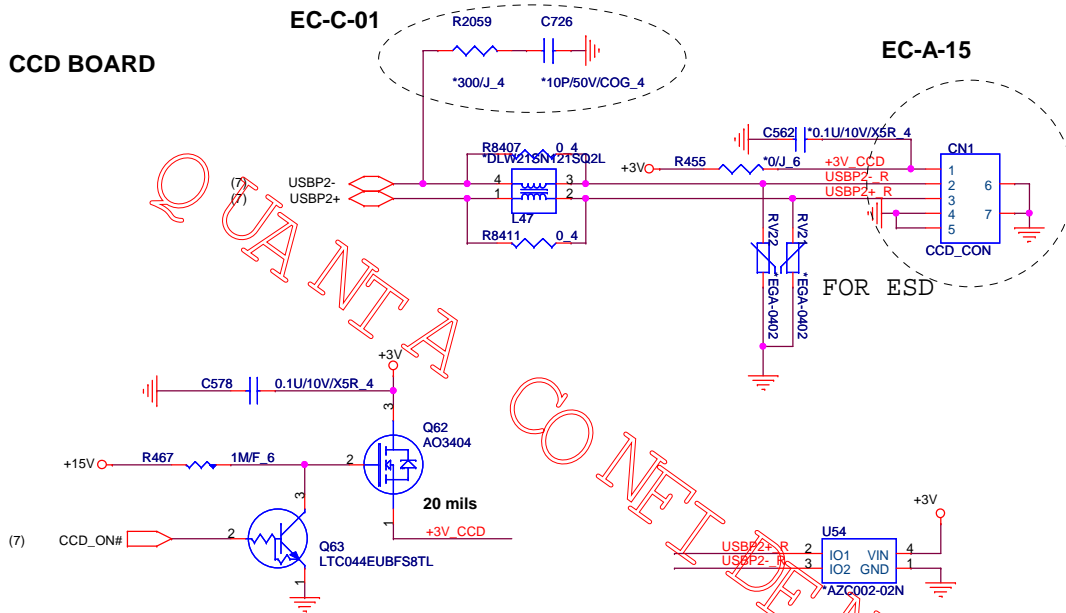
NOTE:
Place C67 near U5



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Quanta Computer Inc.

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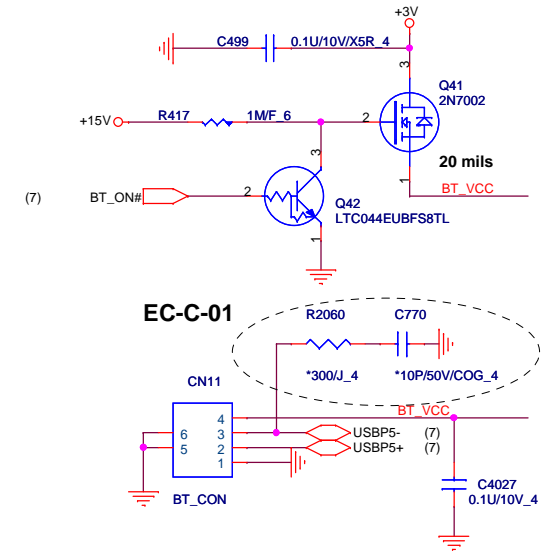
CCD BOARD



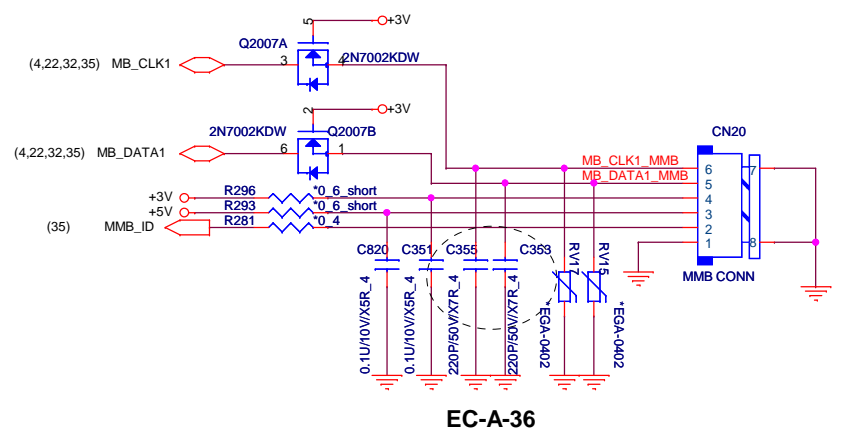
(4,7,8,9,10,11,12,13,19,23,25,26,27,28,29,30,32,34,35,37,40,41,42,43,44,45,46,47) +3V
 (10,26,29,37,39,41,46) +15V
 (9,19,23,24,25,28,29,32,37,47) +5V



BLUETOOTH

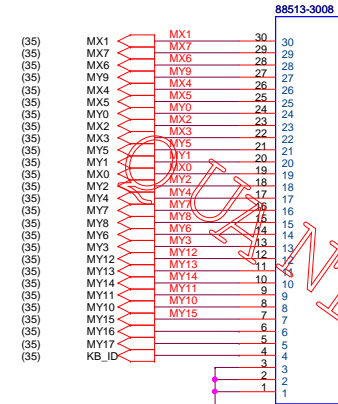


MMB

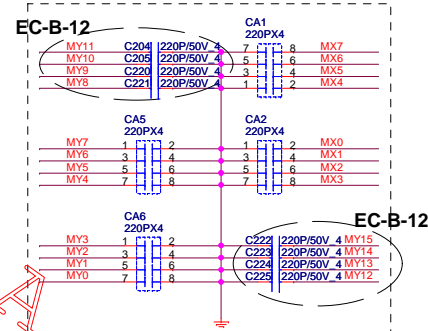


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	BT/USB2.0*2	2A	
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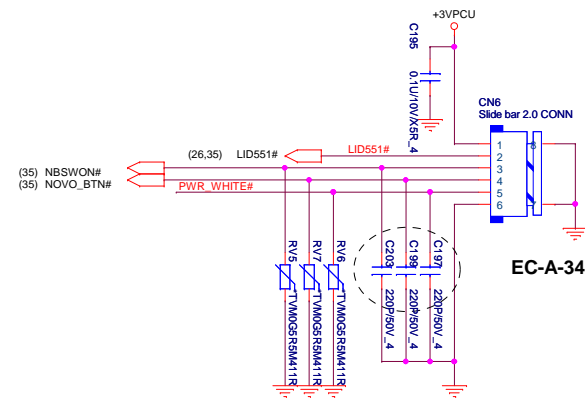
KEYBOARD



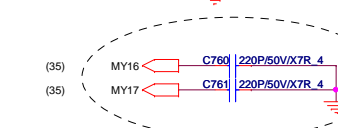
EC-A-19 For EMI request



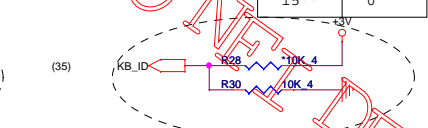
POWER BOARD



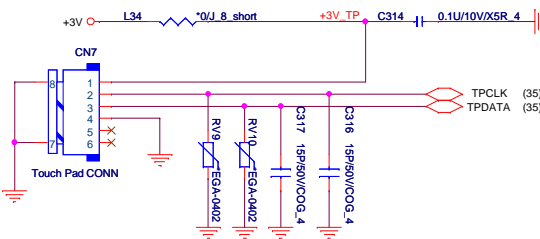
EC-A-32



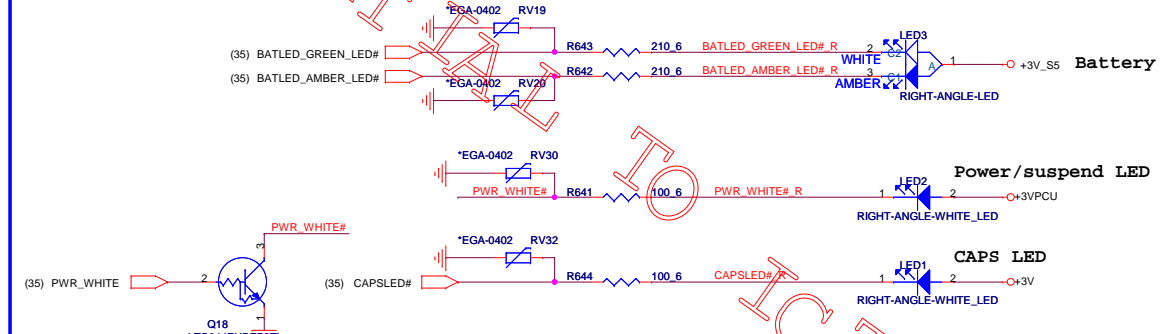
EC-A-13



Touch pad

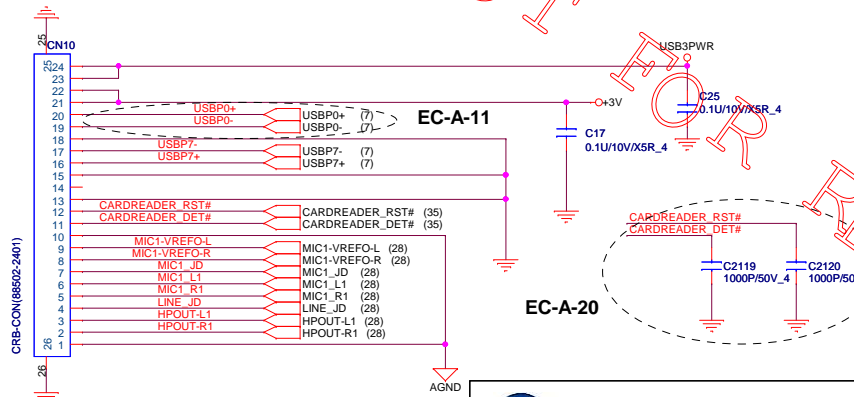
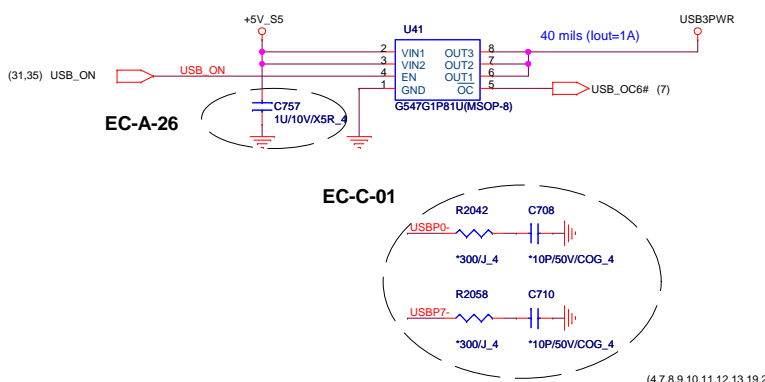


LED



Card reader B to B

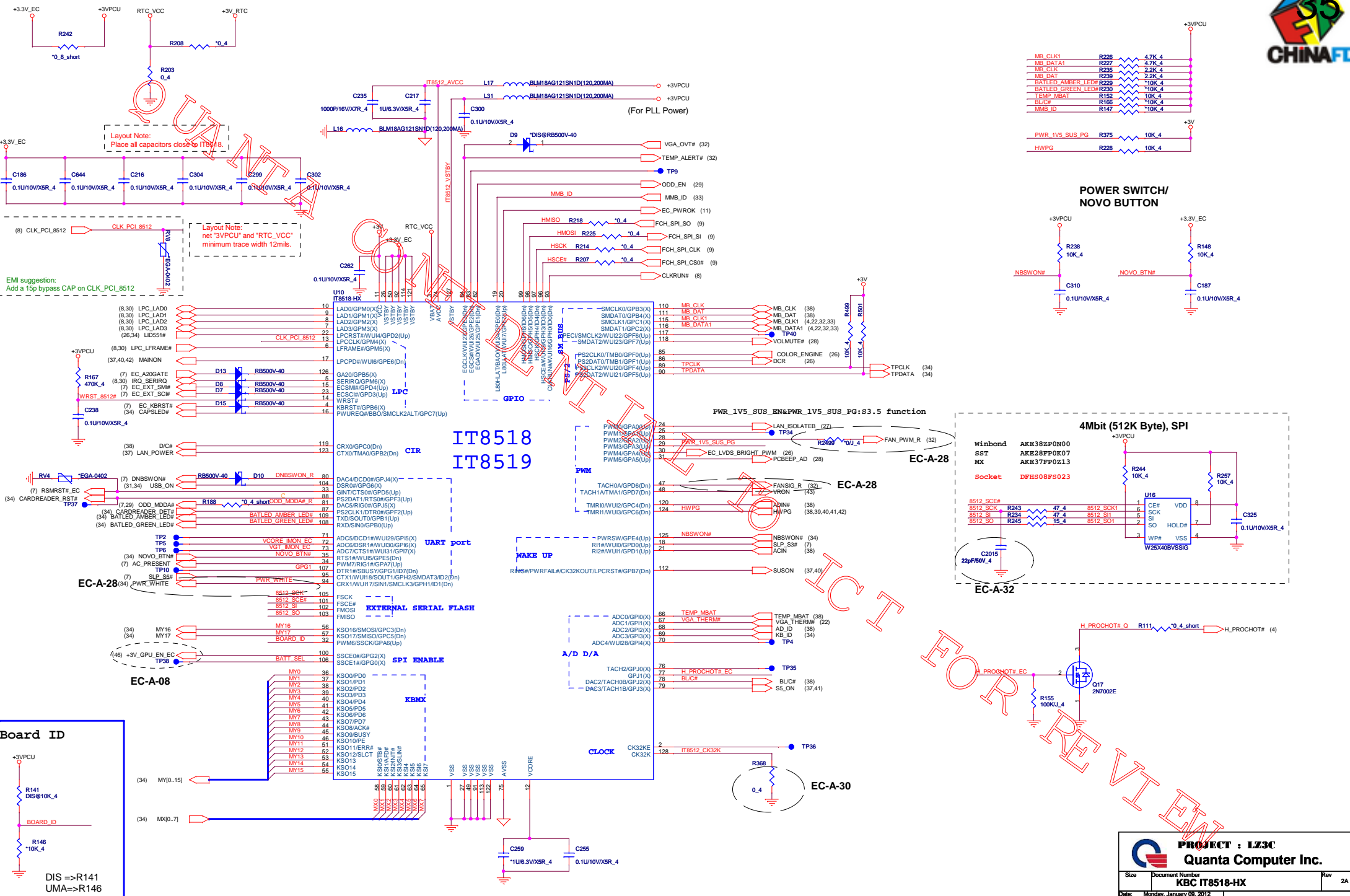
close to card reader B to B



PROJECT : LZ3C
Quanta Computer Inc.

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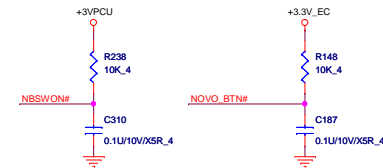
(9,19,23,24,25,28,29,32,33,37,47) +5V
 (8,10,26,27,29,35,37,38,39,42,45,46) +3VPCU
 (4,7,9,10,11,30,37) +3V_S5
 +3V



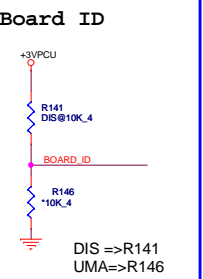
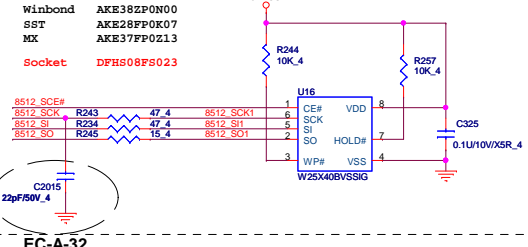
MB_CLK1	R226	4.7K	4
MB_DATA1	R227	4.7K	4
MB_CLK	R228	2.2K	4
MB_DAT	R230	2.2K	4
BATLED_AMBER_LED#	R229	*10K	4
BATLED_GREEN_LED#	R230	*10K	4
TEMP_MBAT	R152	10K	4
BLU_C#	R166	*10K	4
MMB_ID	R147	*10K	4

PWR_LV5_SUS_PG	R375	10K	4
HWPG	R228	10K	4

POWER SWITCH/NOVO BUTTON



4Mbit (512K Byte), SPI



Screw for ME



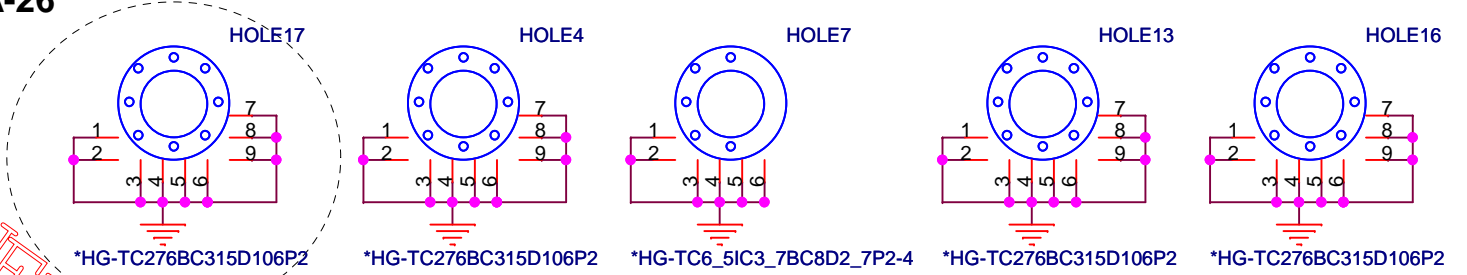
VGA

HOLE18 HOLE20

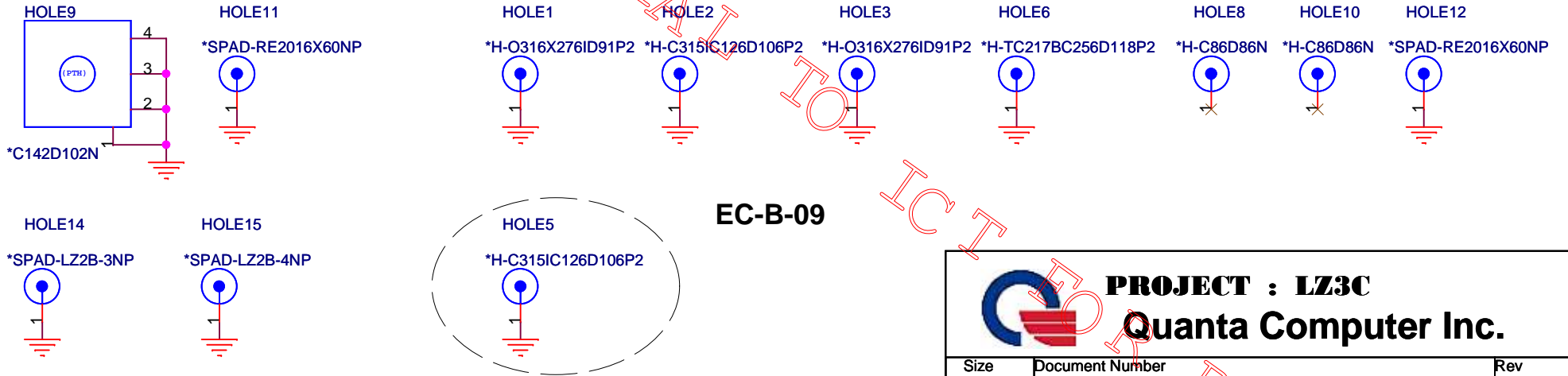
DIS@H-TC5_5BC4I3D3P2 DIS@H-TC5_5BC4I3D3P2

SMT NUT H=4 / 7mm

EC-A-26



CPU BKT

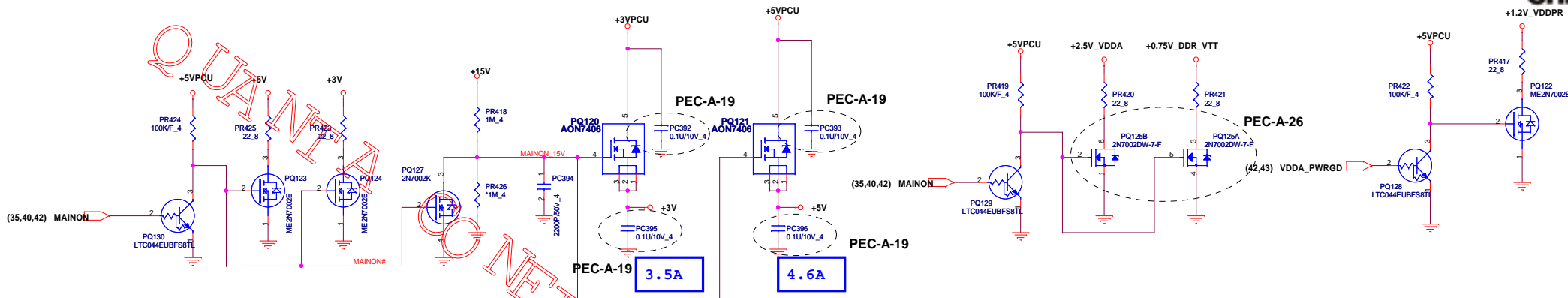


EC-B-09

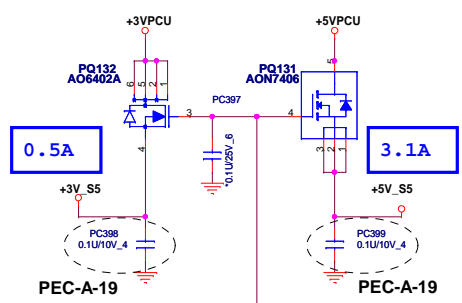
		PROJECT : LZ3C Quanta Computer Inc.	
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DISCHARGE

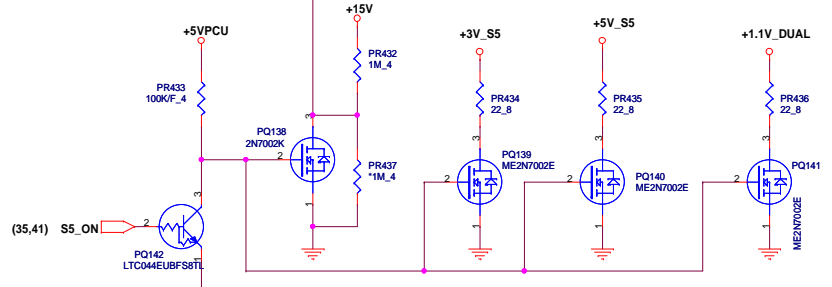
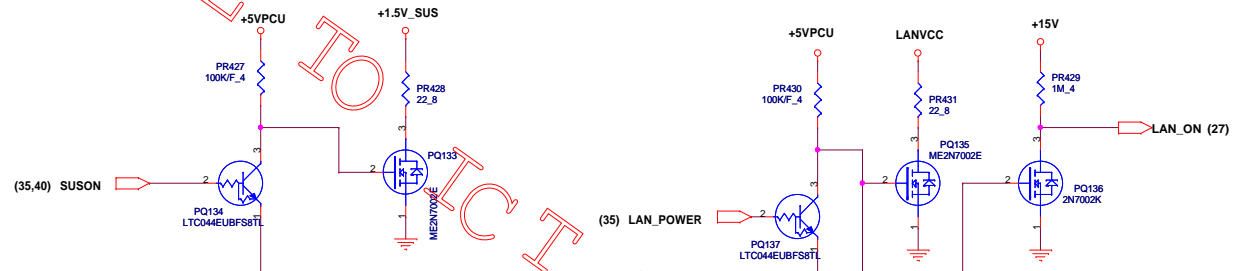
+3V, +5V



3V_S5, 5V_S5

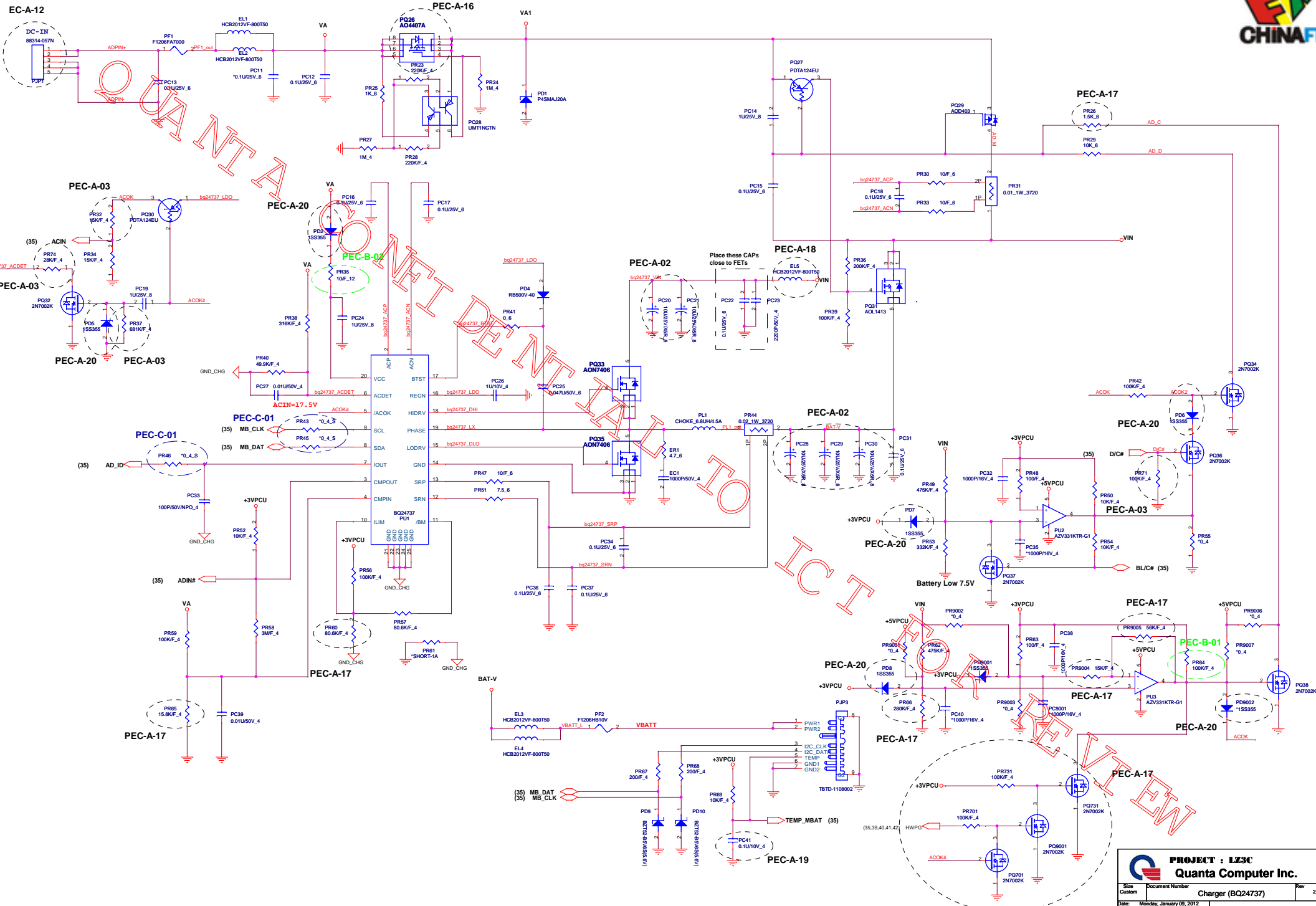


LANVCC



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Quanta Computer Inc.			
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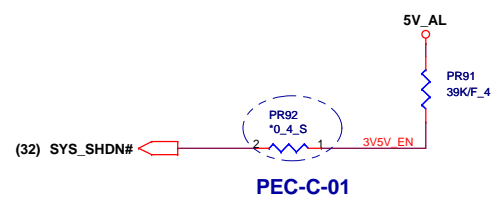
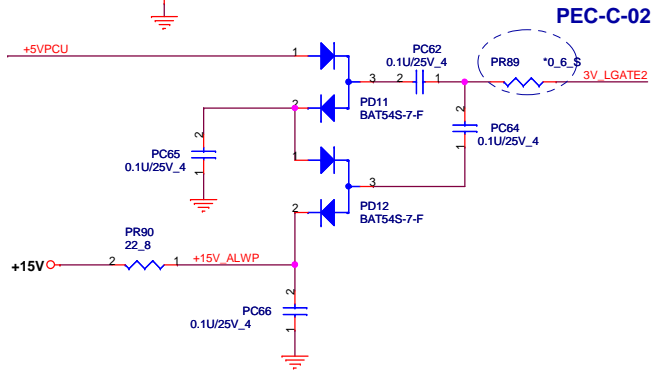
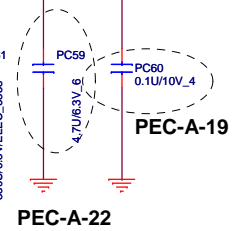
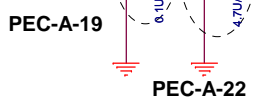
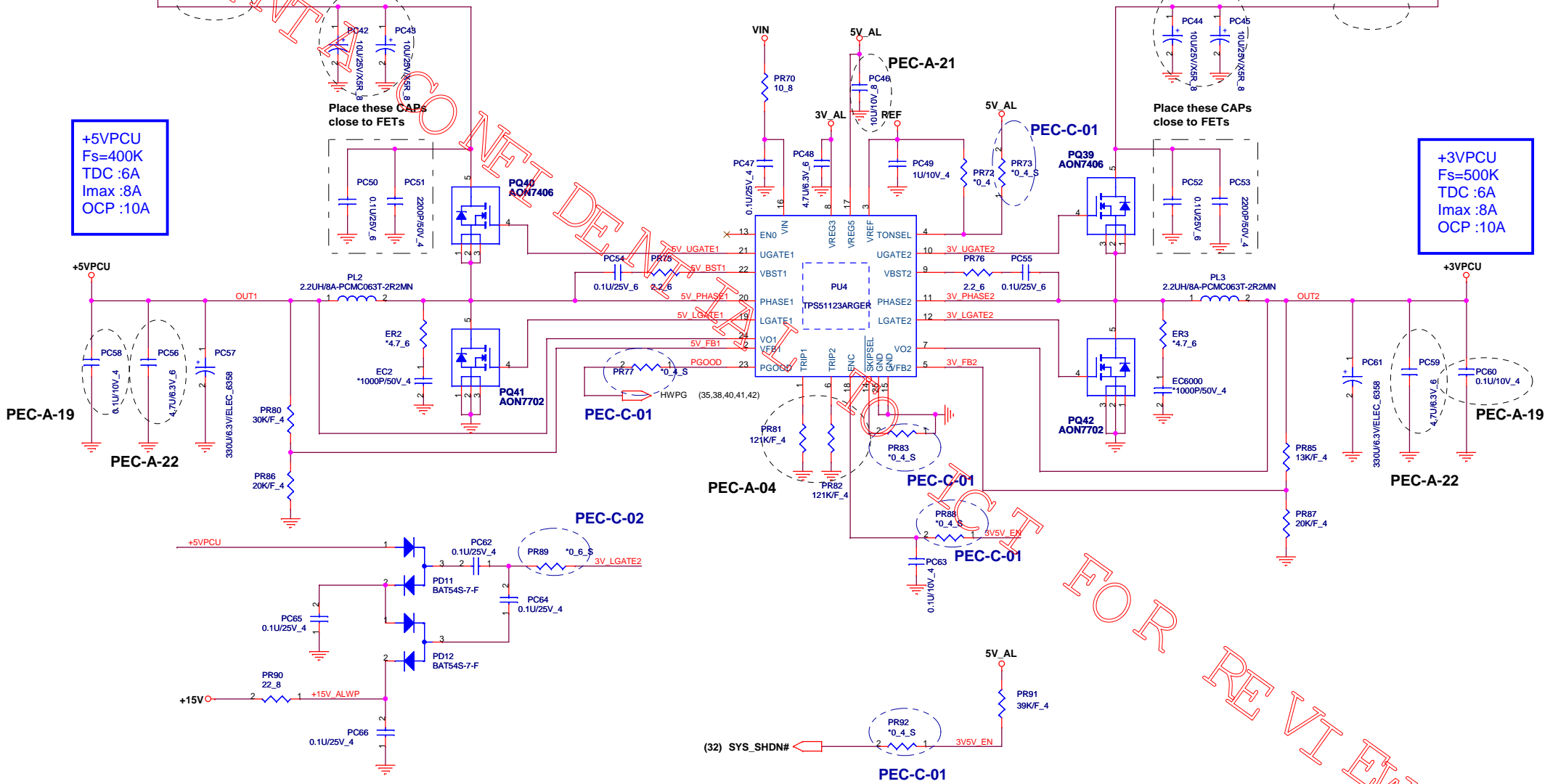
QUANTA CONFIDENTIAL TO BE USED FOR REVIEW





+5VPCU
 Fs=400K
 TDC :6A
 I_{max} :8A
 OCP :10A

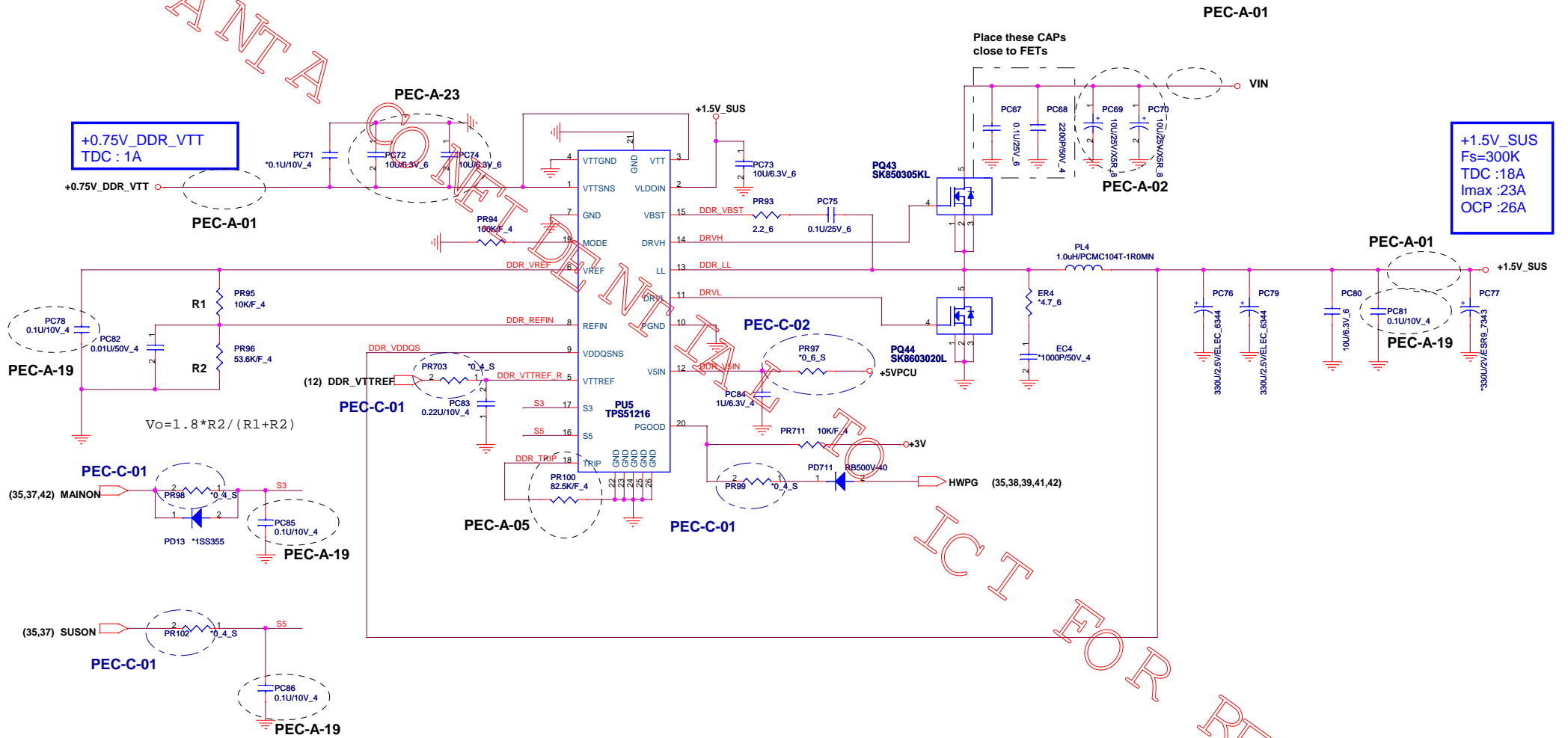
+3VPCU
 Fs=500K
 TDC :6A
 I_{max} :8A
 OCP :10A

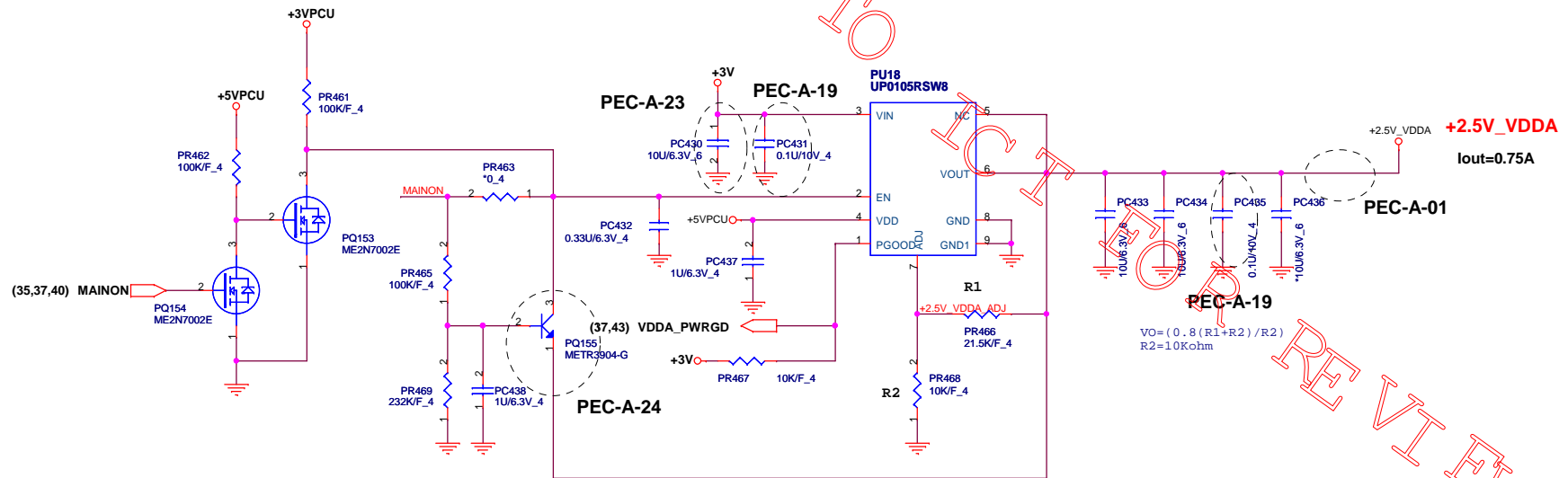
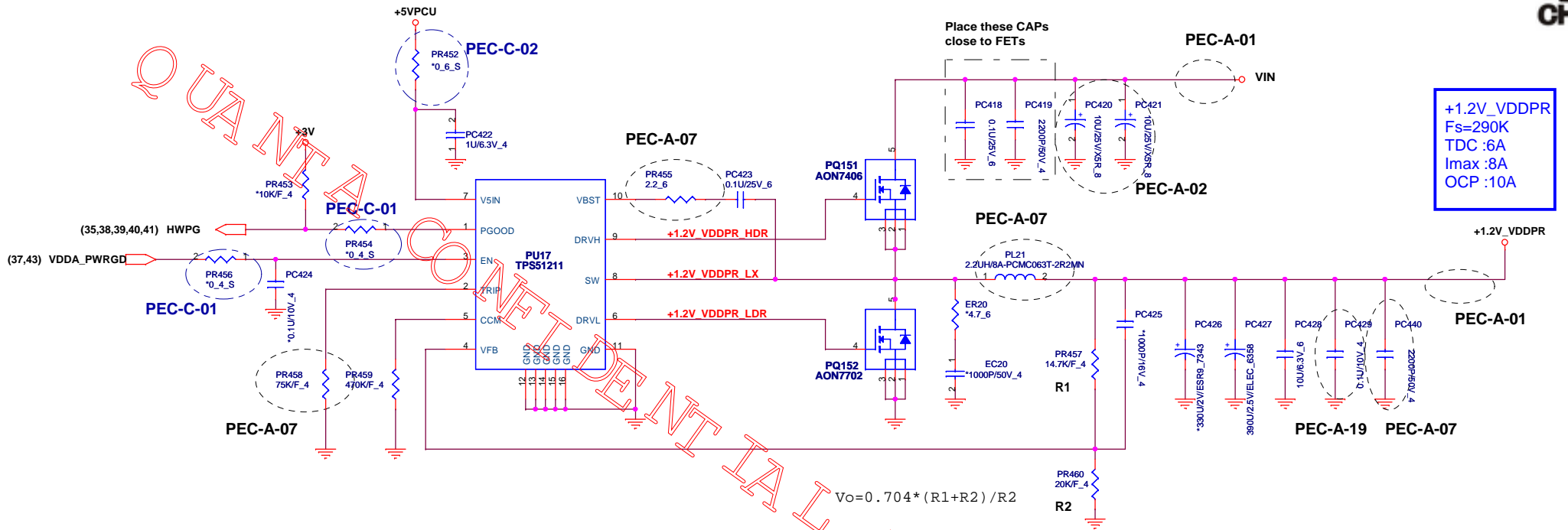


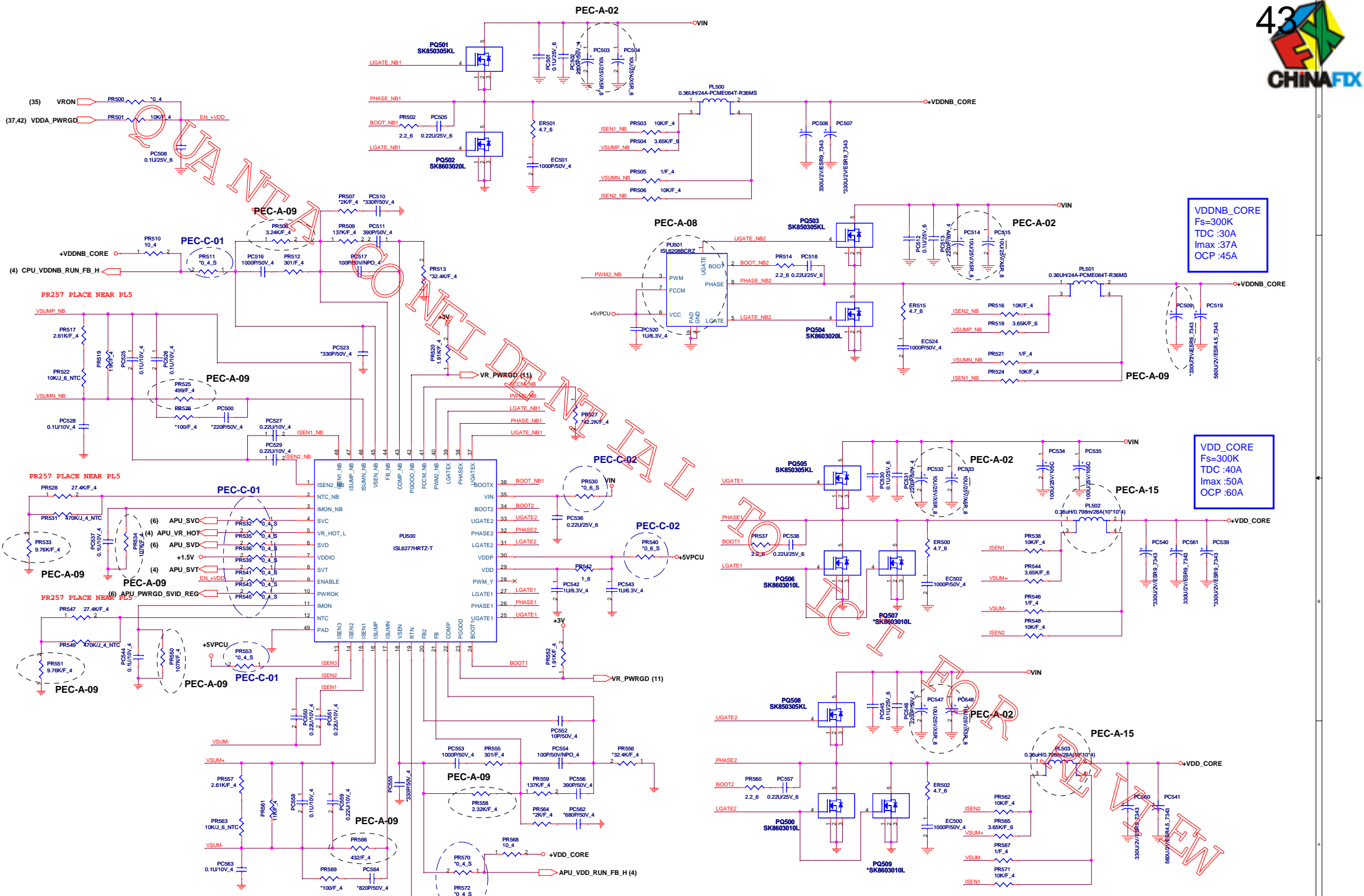
FOR REVIEW

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Quanta Computer Inc.			
Size Custom	Document Number 3V/5V (TPS51123ARGER)	Rev 2A	
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QUANTA





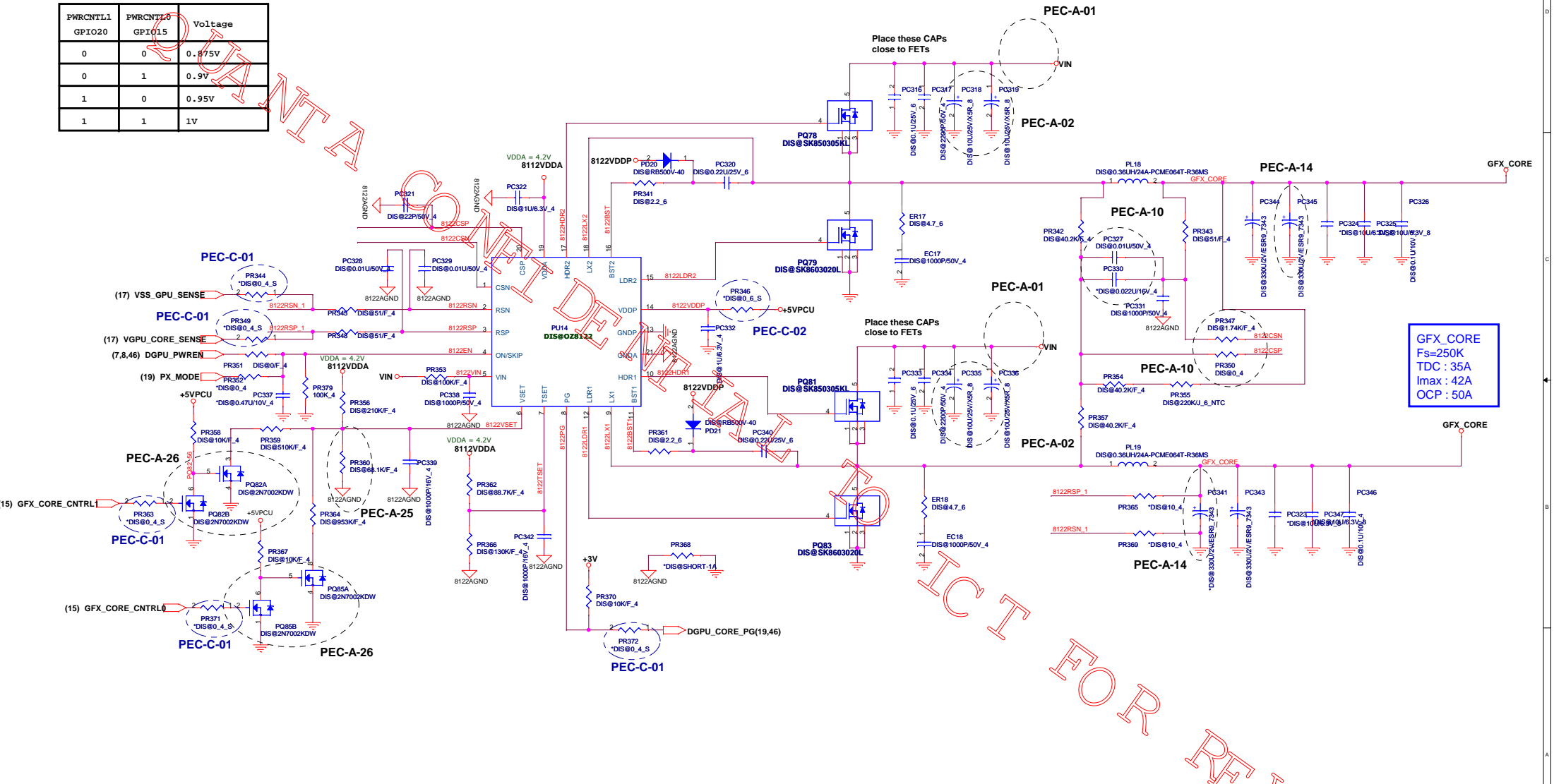


VDDNB_CORE
Fs=300K
TDC :30A
Imax :37A
OCP :45A

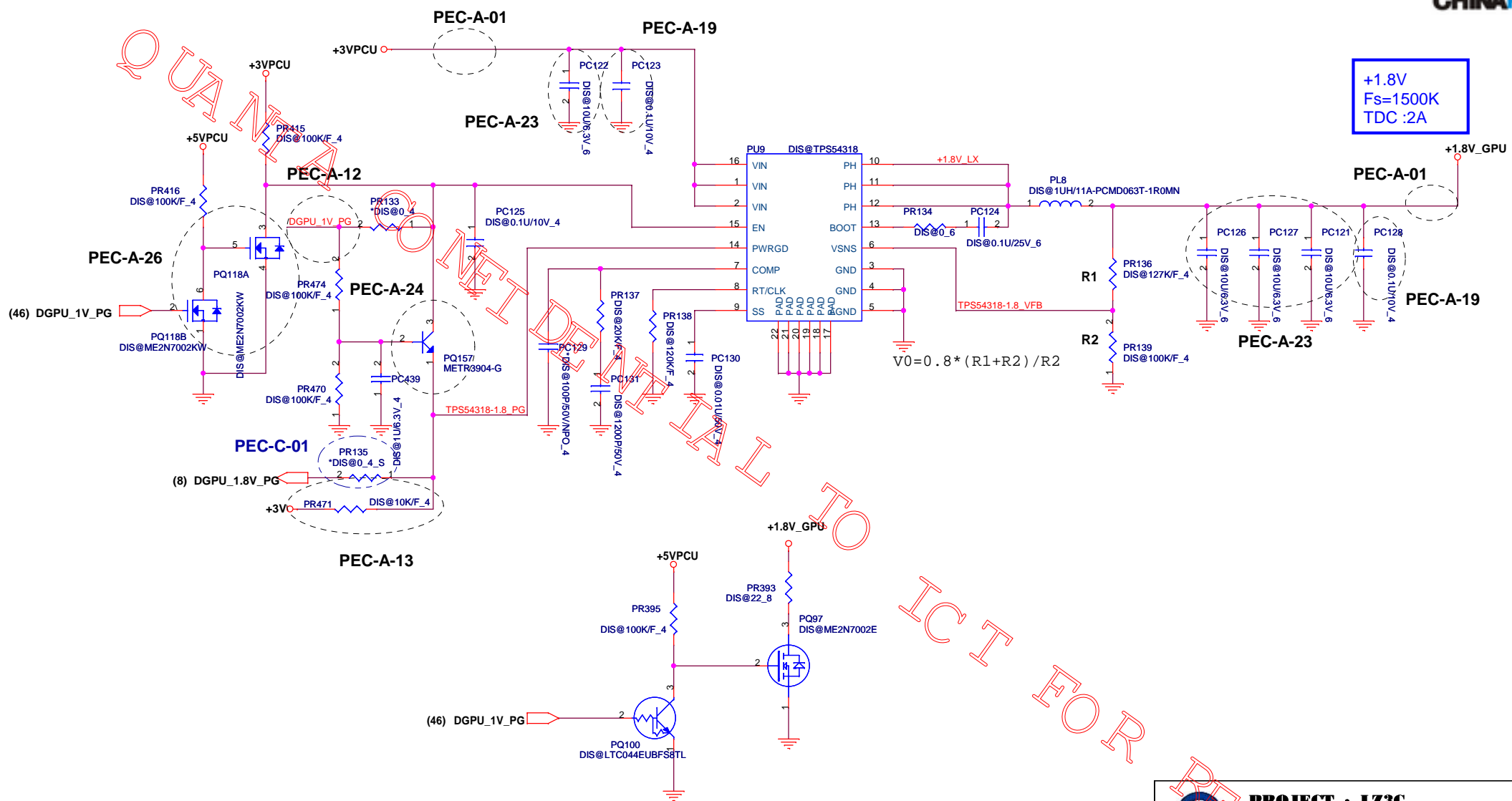
VDD_CORE
Fs=300K
TDC :40A
Imax :50A
OCP :60A

Thames XT M2

PWRCNTL1 GPIO20	PWRCNTL0 GPIO15	Voltage
0	0	0.875V
0	1	0.9V
1	0	0.95V
1	1	1V




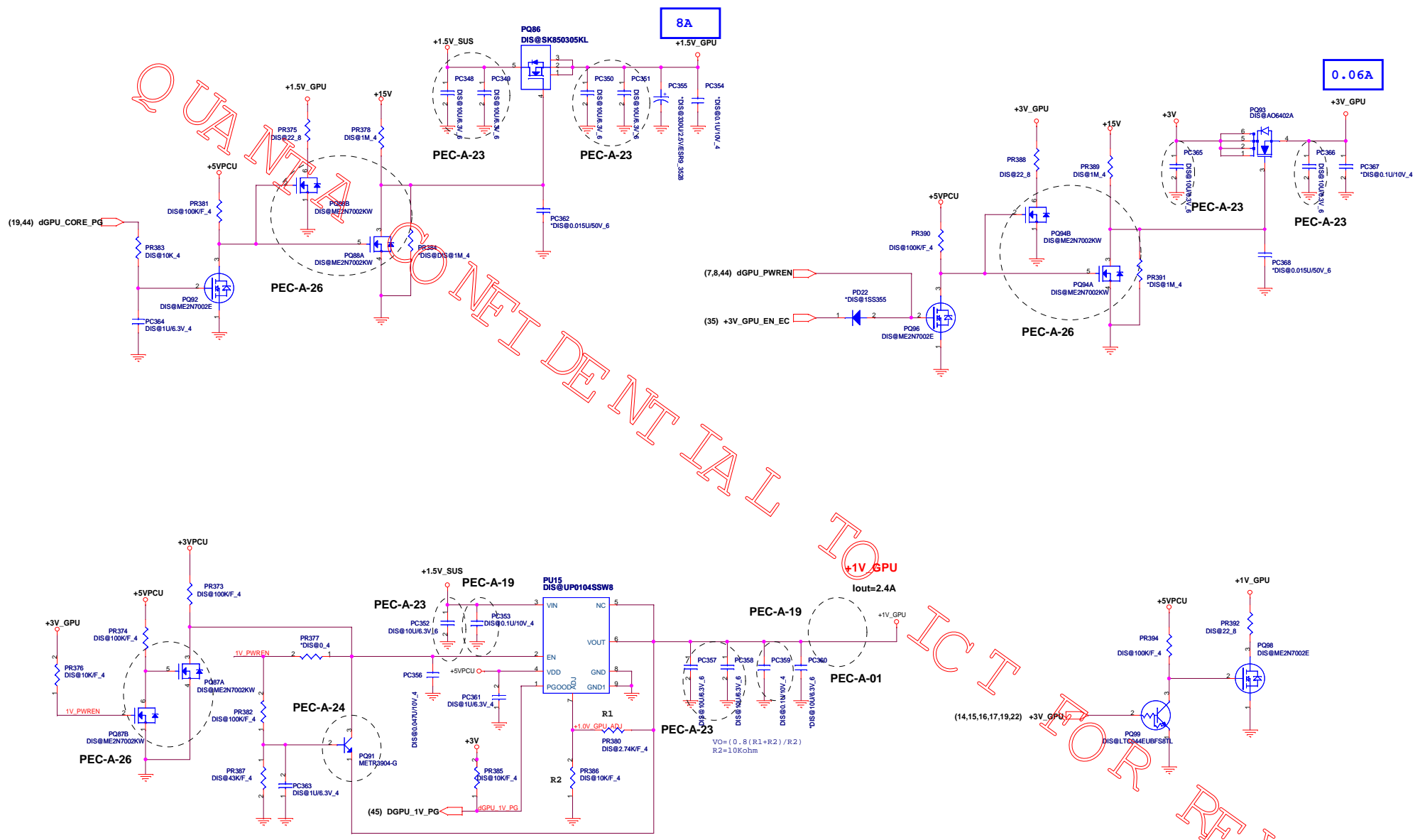
GFX_CORE
 Fs=250K
 TDC : 35A
 Imax : 42A
 OCP : 50A



+1.8V
Fs=1500K
TDC :2A

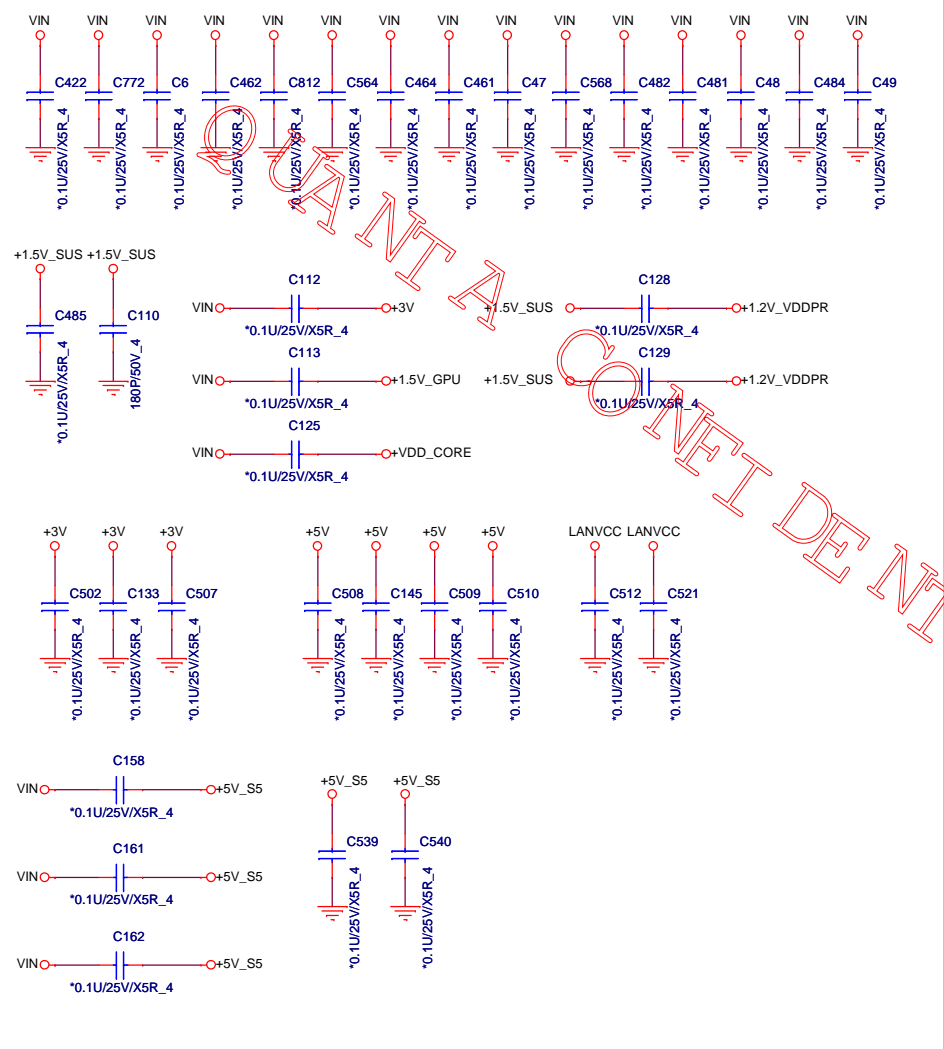
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		PROJECT : LZ3C	
Quanta Computer Inc.			
Size B	Document Number 1.8V (TPS54318)	Rev 2A	
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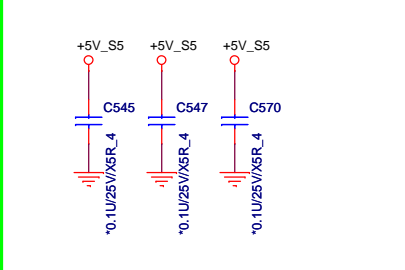


QUANTA COMPUTER INC. CONFIDENTIAL TO IC HOUSE FOR REVIEW

ESD suggestion



EMI suggestion



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		PROJECT : LZ3C	
		Quanta Computer Inc.	
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2011

SDV~SIV

EC NO.	DG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	30	08/23	CN21	Change connection form pin19 to pin 5 due to module choose as below #5: Liteon #53: Cyber TAN POP R628 & R629
EC-A-02	26	08/23	C23	C23 change from 0603 to 0402
EC-A-03	4,8	08/23	U2001,U15	DELETE SOME TPS
EC-A-04	4	08/24	U2001	add pull high resistor R2053~R2057 for JTAG signals.
EC-A-05	4	08/24	R2033	reserve R2033 for Test35
EC-A-06	8	08/25	R189	change R189 to 0 ohm
EC-A-07	9	08/25	R280,R286,R292	pull up resistor from +3V to +3V_S5
EC-A-08	23	09/02	U49	U49.1 need connect to +3V to meet D.G.
EC-A-09	35	09/06	U35	move net +3V_GPU_EN_EC to pin 100
EC-A-10	5	09/06	U2001	add C2117 & C2116 & C2118 to improve +VDDNB_CORE ripple
EC-A-11	7	09/06	U15	change usb port 0 & 8 setting(0 for debug port)
EC-A-12	38	09/06	PJP1	change pin define for PJP1
EC-A-13	34	09/06	R30	pop R30 for Z585 K/B ID setting
EC-A-14	8	09/07	G3	Add short pad for RTC
EC-A-15	33	09/26	CN1	add pin 5 for CN1
EC-A-16	28	09/26	CN9	change CN9 footprint
EC-A-17	20,21	09/26	R16/R17/R459/R460 /R53/R59/R136/R144	change value to 40 ohm for vendor suggest
EC-A-18	31	10/05	CML3/CML4/CML6/R8406 R8410/R8405/R8409/R8198 R8200	add CML4(CX21SQ2L000) and delete R8406/R8410 for EMI request and CML3/4/6 change footprint to choke-dlw21s-4p add CML3&CML6(CX21SQ2L000) and delete R8405/R8409/R8198/R8200 for EMI request
EC-A-19	34	10/05	CA1~CA6	POP for EMI request
EC-A-20	34	10/05	C2119,C2120	add C2119 for CARDREADER_DET# and C2120 for CARDREADER_RST# from EMI request

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Quanta Computer Inc.

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EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-21	28 30	10/05	C501,C535 C530	change footprint to short pad from EMI request
EC-A-22	26	10/05	R10/R27	Not support DCR & COLOR_ENGINE from customer request
EC-A-23	26 23 29 29	10/05	Q19,Q20,Q6 Q34,Q35,Q39 Q31,Q36,Q37 Q27,Q28,Q2006	change to dual mosfet Q6 change to dual mosfet Q39 delete Q31,Q36 and add dual channel MOSFET Q37 delete Q27,Q28 and add dual channel MOSFET Q2006
EC-A-24	31	10/05	C8459	change to 1uF/10V/0402
EC-A-25	27 30	10/06	C513,C519 C528	change to 4.7uF/6.3V/0603
EC-A-26	31 34	10/05	C758 C757	change to 1u/10V/X5R_4
EC-A-27	36	10/05	hole17	add hole17
EC-A-28	32/35	10/06	R2498/R2499/R619/R622	reserve R2498/R2499/R619/R622 for EC control FAN
EC-A-29	8	10/06	U15	change dGPU_1.8V_PG to GPIO46
EC-A-30	35	10/06	R368	reserve for GPIO pin
EC-A-31				
EC-A-31				
EC-A-32	34	10/07	C760,C761	POP for EMI request
EC-A-32	35	10/07	C2015	Change from 220p to 22p, POP for EMI request
EC-A-33	27	10/14	C515,C516	Change from 27p to 33p, vendor test result.
EC-A-34	34	10/14	C197,C199,C203	Change from 1000p to 220p, POP for EMI request
EC-A-35	26	10/18	C2	Change from 0.1U to 220p, POP for EMI request
EC-A-36	33	10/14	C353,C355	Change from 10p to 220p, POP for EMI request
EC-B-01	10	11/04	R343	Change connect power rail to +15V to prevent MosFET burn
EC-B-02	35	11/14	U10	reserve PWR_1V5_SUS_EN&PWR_1V5_SUS_PG:S3.5 function
EC-B-03	06	11/15		delete HDT function
EC-B-04	04	11/18	R2496,R2497	pop for EC can read graphic temp

EC NO.	DG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-05	23	11/18	R383,R385 R387,R388 R391,R392 R395,R402	tune resistor to meet AMD spec.
EC-B-06	26	11/18	Q3,Q4,Q65,R23	Delete Q3,Q4 add Q65 and R23 change to 47 ohm
EC-B-07	8	11/18	R309,R312	change to 0 ohm due to non pci device.
EC-B-08	19	11/18		R126 pop & depop C208,C261,Q22,Q23,Q25,Q43,Q44,Q45,Q3040,R156,R157,R175,R492,R494,U3011 for PX5 implement
EC-B-09	36	11/30	HOLE5	Added screw hole for ME request(the same hole2).
EC-B-10	30	12/06	D28	reserve to prevent leakage
EC-B-11	31	12/06	U53	remove
EC-B-12	25	12/06	CA3/CA4/C204/C205 C220/C221/C222 C223/C224/C225	CA3,CA4 change to 0402*8(C204,C205,C220,C221,C222,C223,C224,C225)
EC-B-13	7	12/06	R527	reserve for dgpu_pwr_en
EC-B-14	27	12/06		Reserve for Surge Line to GND Gas Tube Discharge
EC-C-01	30	01/03	R2066,C775	Add resistor(300ohm) and CAP(10PF) to meet AMD spec.
	31		R2065,C774	
	33		R2061,C771	
	34		R2062,C773	
			R2059,C726	
			R2060,C770	
			R2042,C708	
			R2058,C710	



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SDV-SIV

2011

EC NO.	DC.	DATE	DART REFERENCE	DESCRIPTION
PEC-A-01	38,39,40,41,42	09/21	PJP4,PJP5,PJP6,PJP7,PJP8,PJP9,PJP32,PJP33,PJP34,PJP35,PJP36,PJP26,PJP29,PJP16,PJP17,PJP31	Change open pad to short pad.
PEC-A-02	38,39,40,41,43,44	09/22	PC20,PC21,PC28,PC29,PC30,PC42,PC43,PC44,PC45,PC69,PC70,PC403,PC404,PC420,PC421,PC503,PC504,PC514,PC532,PC533,PC547,PC548,PC318,PC319,PC335,PC336	Change MLCC 10UF size from 1206 to 0805.
PEC-A-03	38	09/22	PR32,PR37,PR71,PR78,PR74	Adjust AC plug-in detect function.
PEC-A-04	39	09/22	PR81,PR82	PR81,PR82 change from 140K to 121K for 3V/5V OCP.
PEC-A-05	40	09/22	PR100	PR100 change from 124K to 82.5K for 1.5V/SUS OCP.
PEC-A-06	41	09/22	PR444,PR444,PL20	PR444 change from 100K to 75K for 1.1V_DUAL OCP. PR440 change from 0 ohm to 2.2 ohm for improve ringing voltage. PL20 change from 1uH to 2.2uH for improve ripple.
PEC-A-07	42	09/22	PR455,PR458,PL21,PC440	PR458 change from 100K to 75K for 1.1V_DUAL OCP. PR455 change from 0 ohm to 2.2 ohm for improve ringing voltage. PL21 change from 1uH to 2.2uH for improve ripple. add PC440 2200P cap for improve 1.2V output noise.
PEC-A-08	43	09/22	PU501	Change PU501 driver IC size from 3*3 to 2*2.
PEC-A-09	43	09/22	PR508,PR525,PR533,PR534,PR551,PR550,PR566,PR558,PC509	Adjust VDD/NB core load line/OCP/OTP function.
PEC-A-10	44	09/22	PR347,PC330,PC327,PR350	Adjust GFX core OCP function.
PEC-A-11	44	09/22		Change GFX core power budget for ATI Seymour XT(15w).
PEC-A-12	45	09/08	PU9	Change from MAINON to DGPU_1V_PG
PEC-A-13	45	09/22	PR471	add pull high resistor PR471 for DGPU_1.8V_PG.
PEC-A-14	44	09/26	PC341	Reduce 1pcs GFX core 7343 size output Cap for ATI Seymour XT(15w).
PEC-A-15	43	09/26	PL502,PL503	Change VDD core choke footprint for SMT request.
PEC-A-16	38	09/26	PQ26	Delete AQ427 MOSFET from BOM source.
PEC-A-17	38	09/29	PQ701,PR701,PQ731,PR65,PR60,PR26,PR66,PR9004,PR9005,	Adjust Battery discharge function.
PEC-A-18	38	09/29	EL5	add charger input bead for EMI.
PEC-A-19	37,38,39,40,41,42,45,46,	10/04	PC439,PC408,PC399,PC393,PC81,PC431,PC435,PC392,PC396,PC60,PC41,PC398,PC395,PC35,PC36,PC78,PC8,PC359,PC353,PC128,PC123	Change P/N from CH4104K9B03 to CH41002KB93.
PEC-A-20	38	10/04	PD5,PD8,PD2,PD6,PD7,PD9002	Change P/N from BC1SS355Z07 to BC1SS355Z21.
PEC-A-21	39	10/04	PC46	Change P/N from CH61001ME96 to CH6102K9A01.
PEC-A-22	39	10/04	PC56,PC59	Change P/N from CH6472K9A02 to CH6472M9901.
PEC-A-23	40,41,42,45,46	10/04	PC74,PC72,PC127,PC122,PC106,PC121,PC412,PC351,PC430,PC348,PC350,PC365,PC358,PC349,PC357,PC352,PC366	Change P/N from CH61001ME96 to CH6101M9905.
PEC-A-24	42,45,46	10/04	PQ155,PQ91,PQ157	Change P/N from BA039040019 to BA0390400H0.
PEC-A-25	44	10/04	PR360	Change P/N from CS36652FB16 to CS36812FB15.
PEC-A-26	37,44,45,46	10/17	PQ123,PQ124,PQ125,PQ126,PQ139,PQ140,PQ82,PQ102,PQ101,PQ85,PQ116,PQ119,PQ88,PQ90,PQ87,PQ89,PQ94,PQ95	change to dual mosfet.
PEC-B-01	38	11/18	PR64	Adjust Battery discharge function.
PEC-B-02	38	11/22	PR35	Change footprint from RC0603 to RC1206.

CONFIDENTIAL

TO ICT FOR REVIEW