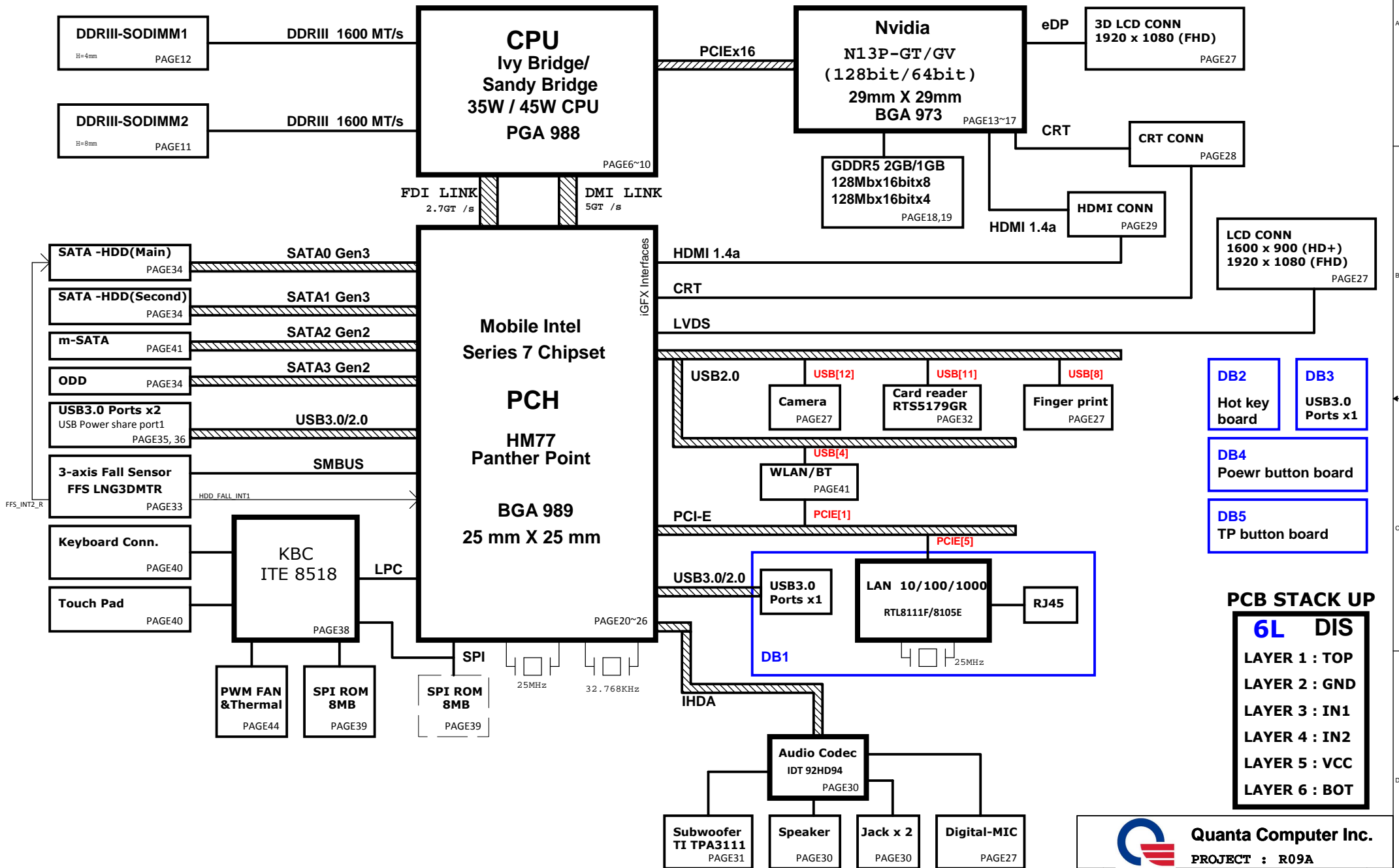
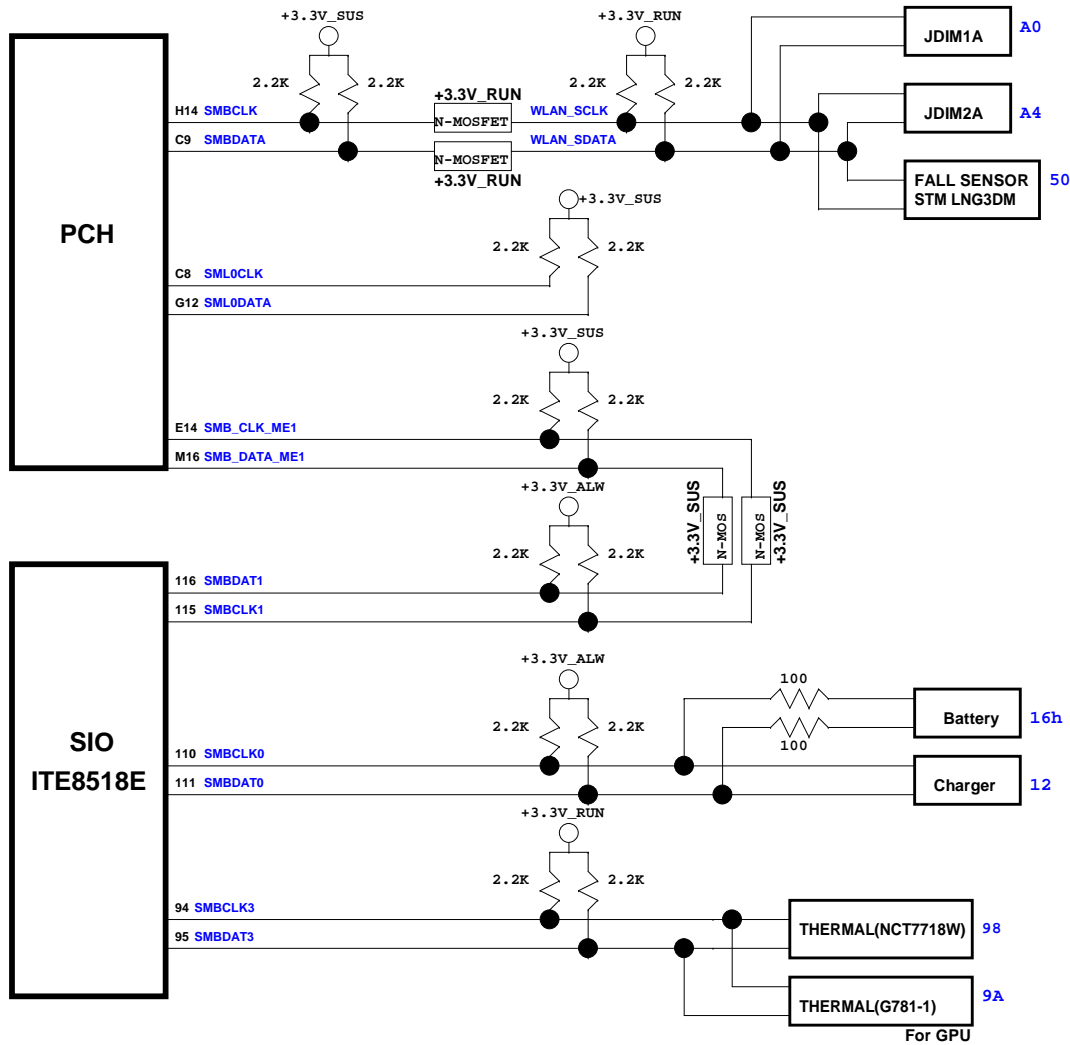


# R09/A 17" OPT BLOCK DIAGRAM



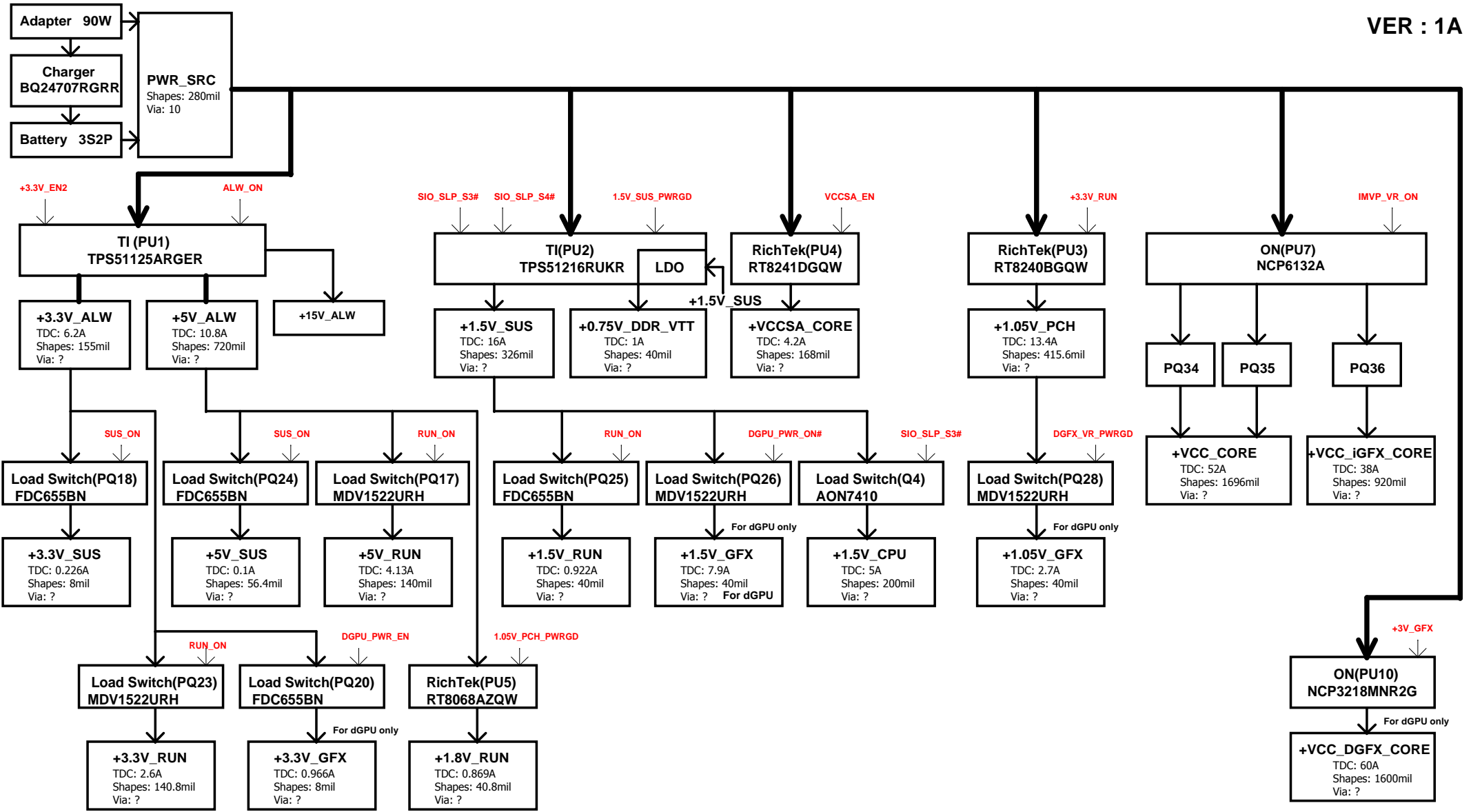


Function	IC	SMBus Address
DDR3	JDIM1A	A0
	JDIM2A	A4
Thermal IC	G781-1P8	1001101xb (9Ah)
	EMC1422	1001100xb (98h)
Charge IC	BQ24707ARGRR	0b00010010 (0x12)
Battery	Battery	16h
Fall Sensor	LNG3DM	01010000 (50h)

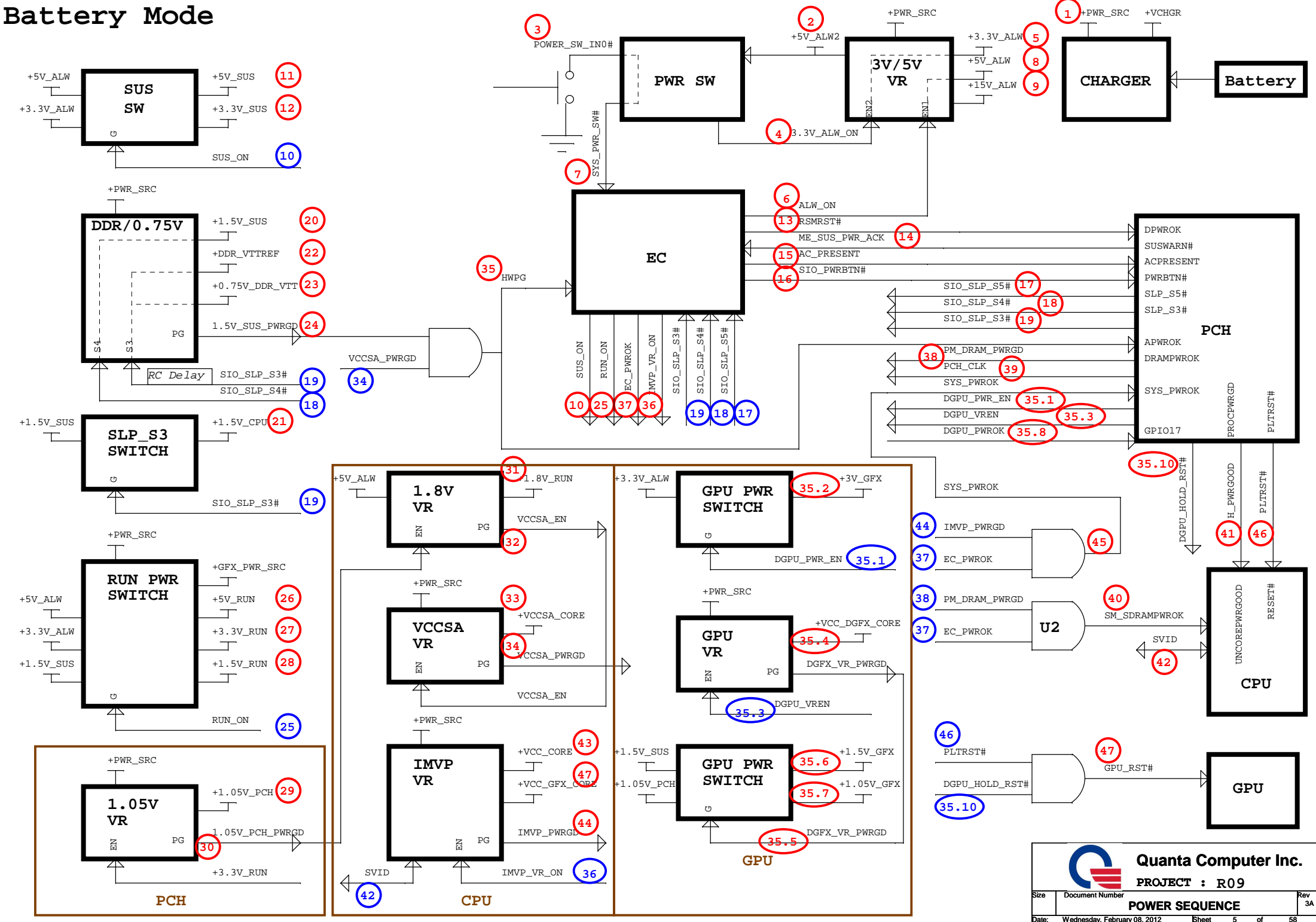
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0 / Power share)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT/WiMAX)
USB5	NC
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	NC
USB10	Card Reader
USB11	Express Card
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD Main
SATA1	HDD Second
SATA2	mSATA
SATA3	ODD
SATA4	NC
SATA5	NC

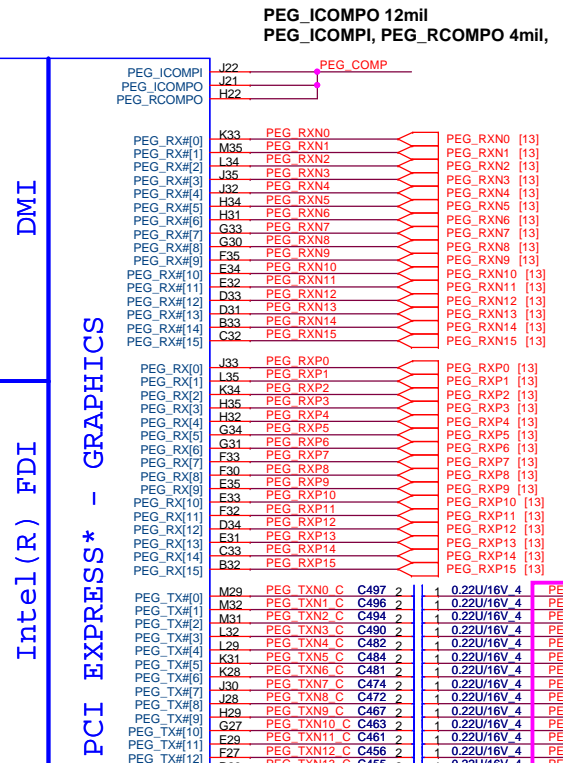
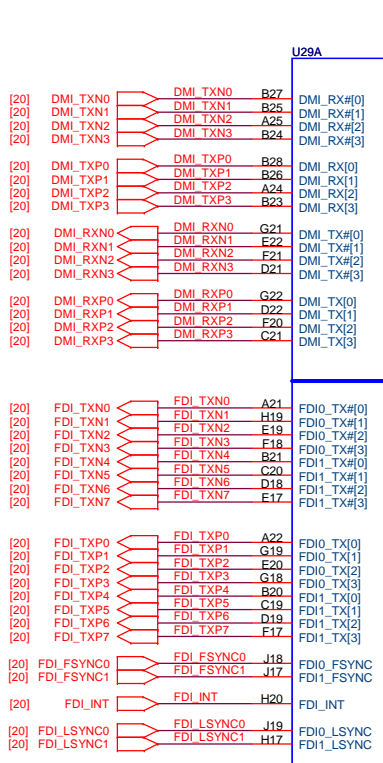
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	NC
PCIE 3	NC
PCIE 4	NC
PCIE 5	LAN
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC



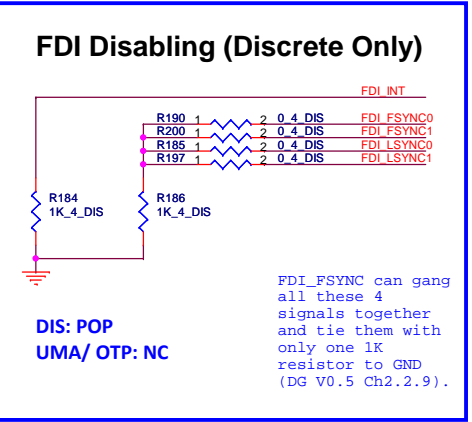
# Battery Mode



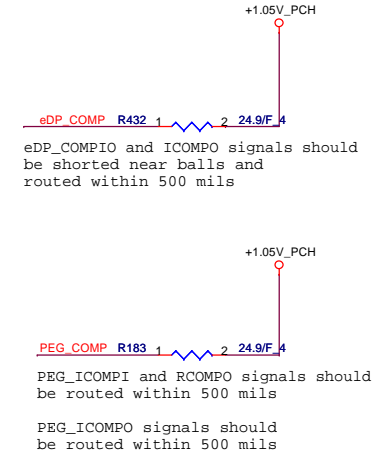
# Ivy Bridge Processor (RESERVED, CFG)



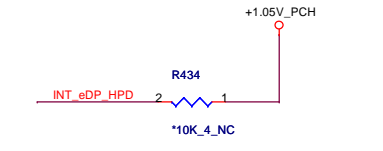
eDP\_ICOMPO 12mil  
eDP\_COMPIO 4mil  
Programing Disable eDP interface(BIOS)



## DP & PEG Compensation



## eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

0.22uF AC coupling Caps for PCIe GEN1/2/3 - GT  
0.1uF AC coupling Caps for PCIe GEN1/2 - GV

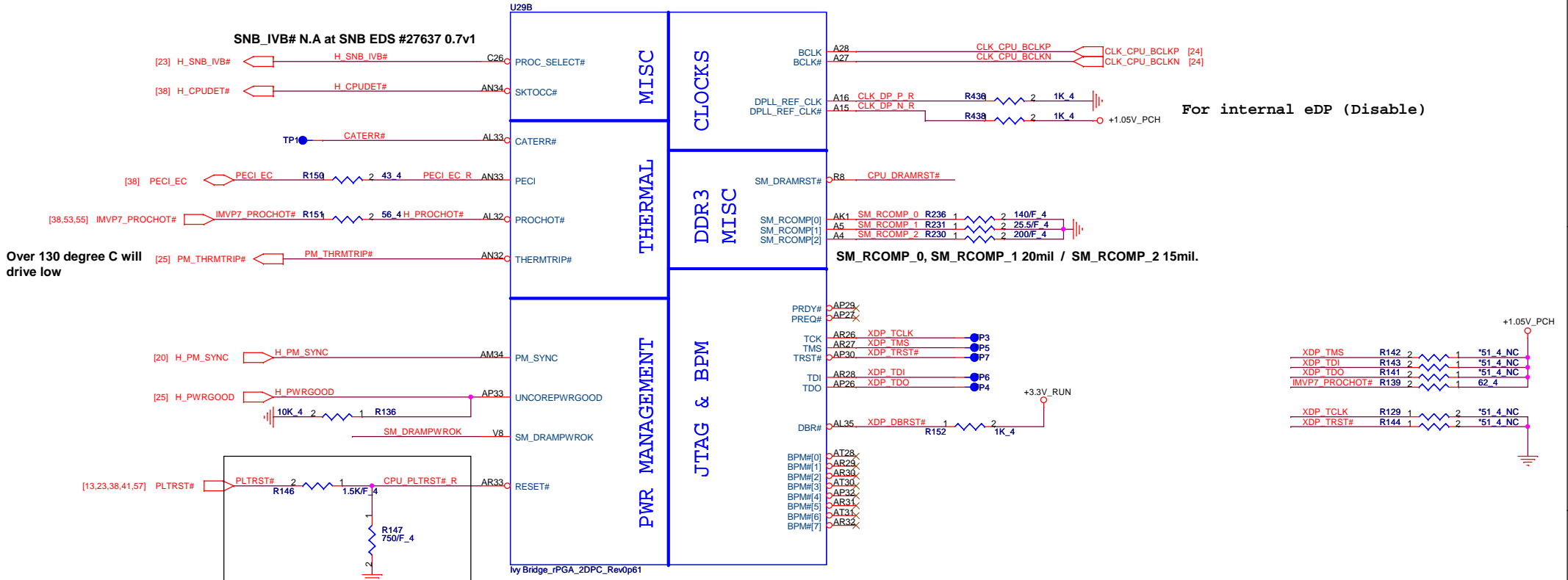
VGA (U3)	AC coupling Cap	PN	TX location	RX location (page13)
N13P-GV	0.1uF CAP CHIP 0.1U 16V(10%,X7R,0402)	CH4103K1B08	C452,C451,C455, C456,C461,C463, C467,C472,C450, C453,C454,C457, C460,C459,C465, C473	C125,C126,C147 C145,C123,C124 C152,C153,C121 C122,C151,C150 C119,C120,C149 C148
N13P-GT	0.22uF CAP CHIP 0.22U 16V(10%,X7R,0402)	CH4223K1B00	ALL	ALL

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Size: Document Number  
**Ivy Bridge 1/5**  
Rev 3A

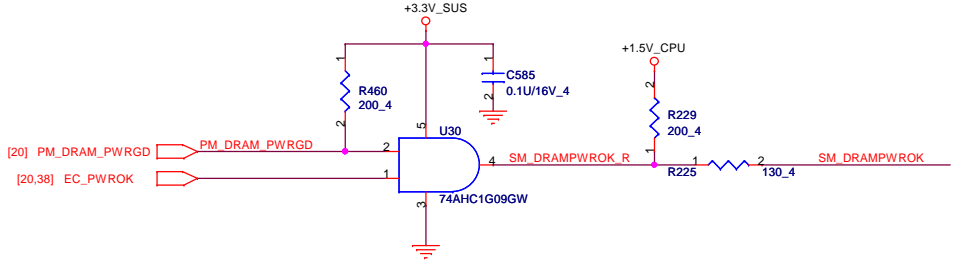
Date: Monday, March 05, 2012 Sheet 6 of 58

# Ivy Bridge Processor (CLK,MISC,JTAG)



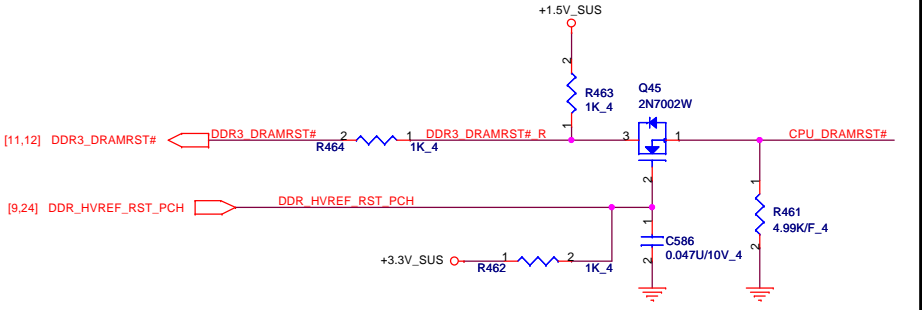
Intel spec VinH min =VCCIO x 0.7

Follow #DG1.5 471984 P128  
DDR Power Gating Topology

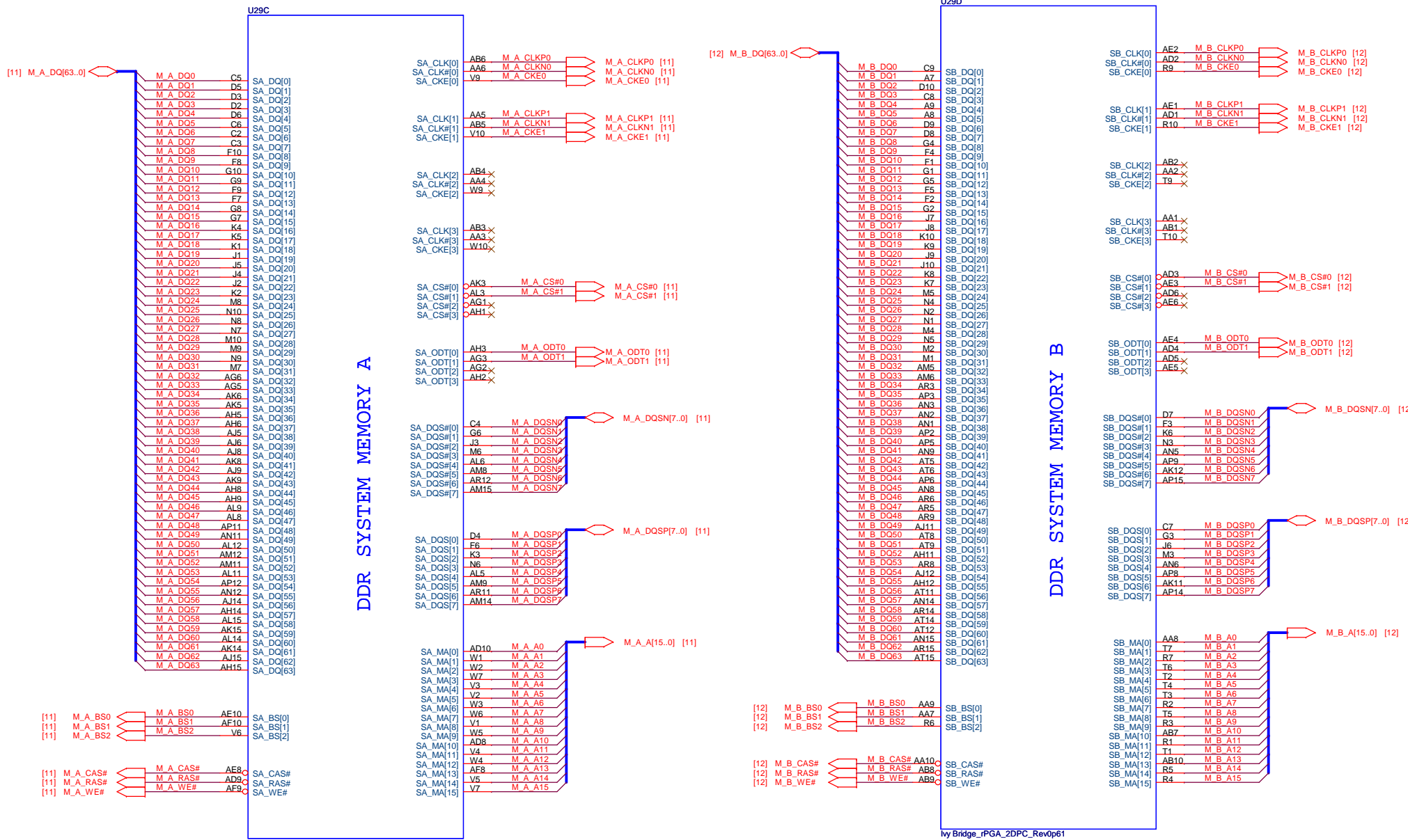


when 1,2 is high, 4 is high-impedance OFF-state

Follow #DG1.5 471984 P130  
DRAMRST# Routing Illustration



# Ivy Bridge Processor (DDR3)



Ivy Bridge\_rPGA\_2DPC\_Rev0p61

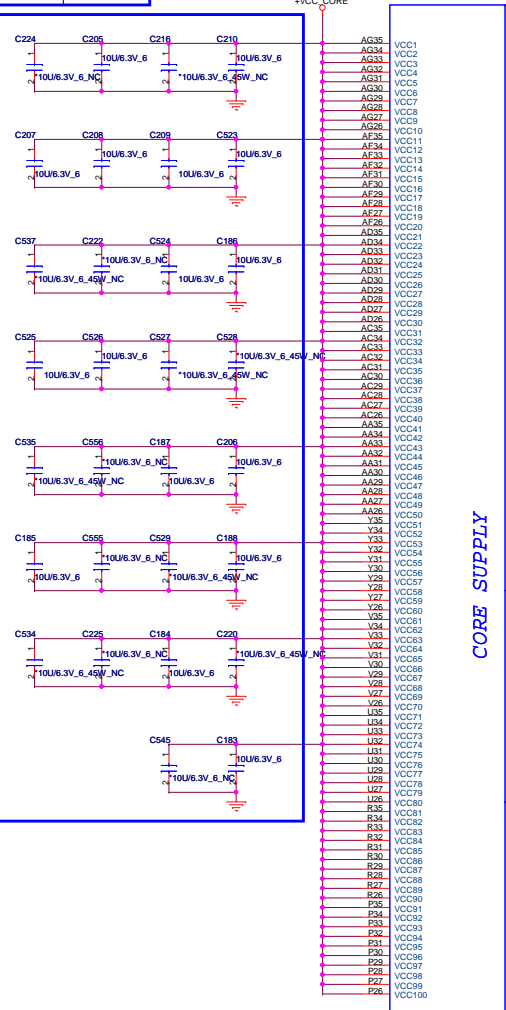
Ivy Bridge\_rPGA\_2DPC\_Rev0p61



Ivy Bridge Processor (GRAPHIC POWER)

Table with 2 rows and 2 columns: 35W 16pcs, 45W 24pcs

CPU Core Power IVY, SNB: 35W - 53A, IVY, SNB: 45W - 94A, 10F X24



POWER

PEG AND DDR

CORE SUPPLY

SENSE LINES

1.05V\_PCH SNB: 8.5A, IVY: 8.5A, 10F X12

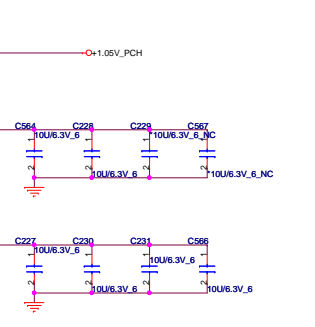


Table with 4 columns: Power Rail Sense Line, R1, R2, Trace Impedance, Trace Length Match. Includes entries for VCC\_SENSE / VSS\_SENSE, VCCXAG\_SENSE / VSSXAG\_SENSE, VCCIO\_SENSE / VSS\_SENSE\_VCCIO, and VCCSA.

CPU VGT SNB: 33A, IVY: 33A, 10uF X12

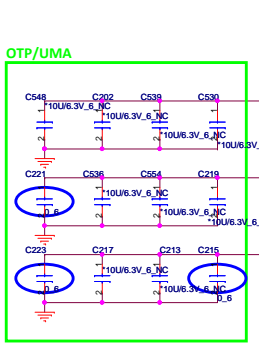


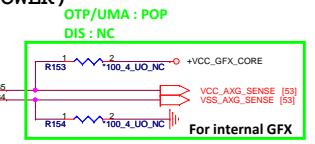
Table with 3 columns: DIS, RESISTOR CHIP, UMA/OPT. Includes values like 0 ohm, C221,C223,C215, 0.1/10W+-5%(0603), and 10uF.

POWER

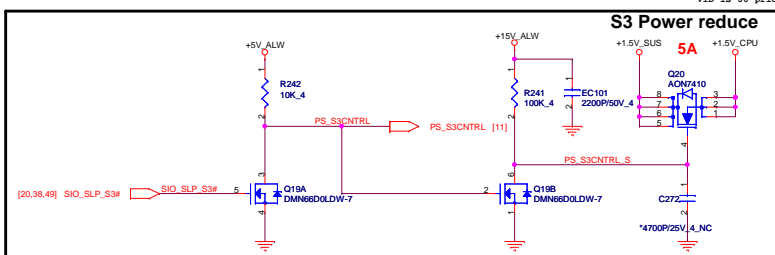
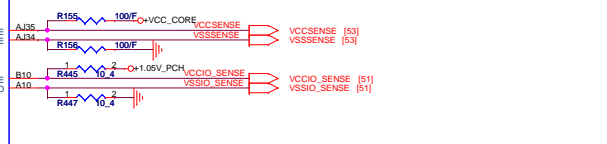
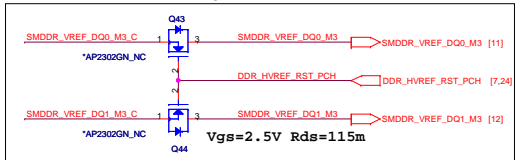
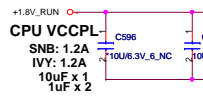
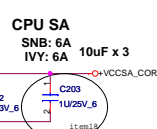
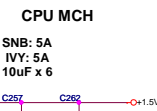
GRAPHICS

SA RAIL

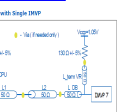
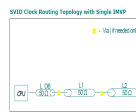
MISC



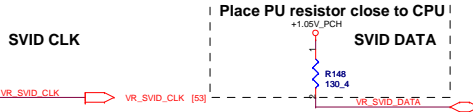
CAD Note: +VDDR\_REF\_CPU should have 10 mil trace width



Take care Q20 Vgs(MAX)=2.5



Layout note: need routing together and ALERT need between CLK and DATA

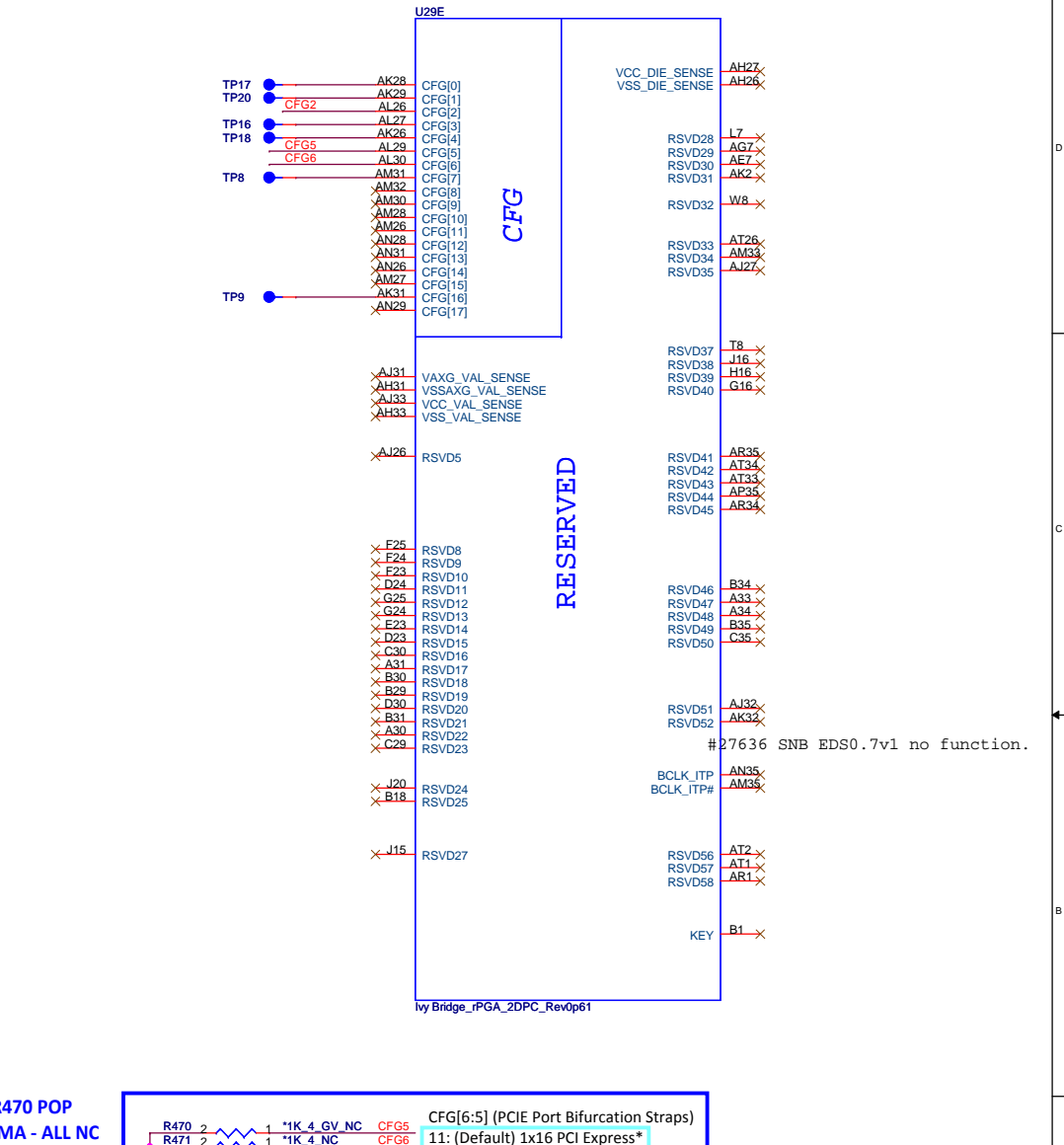
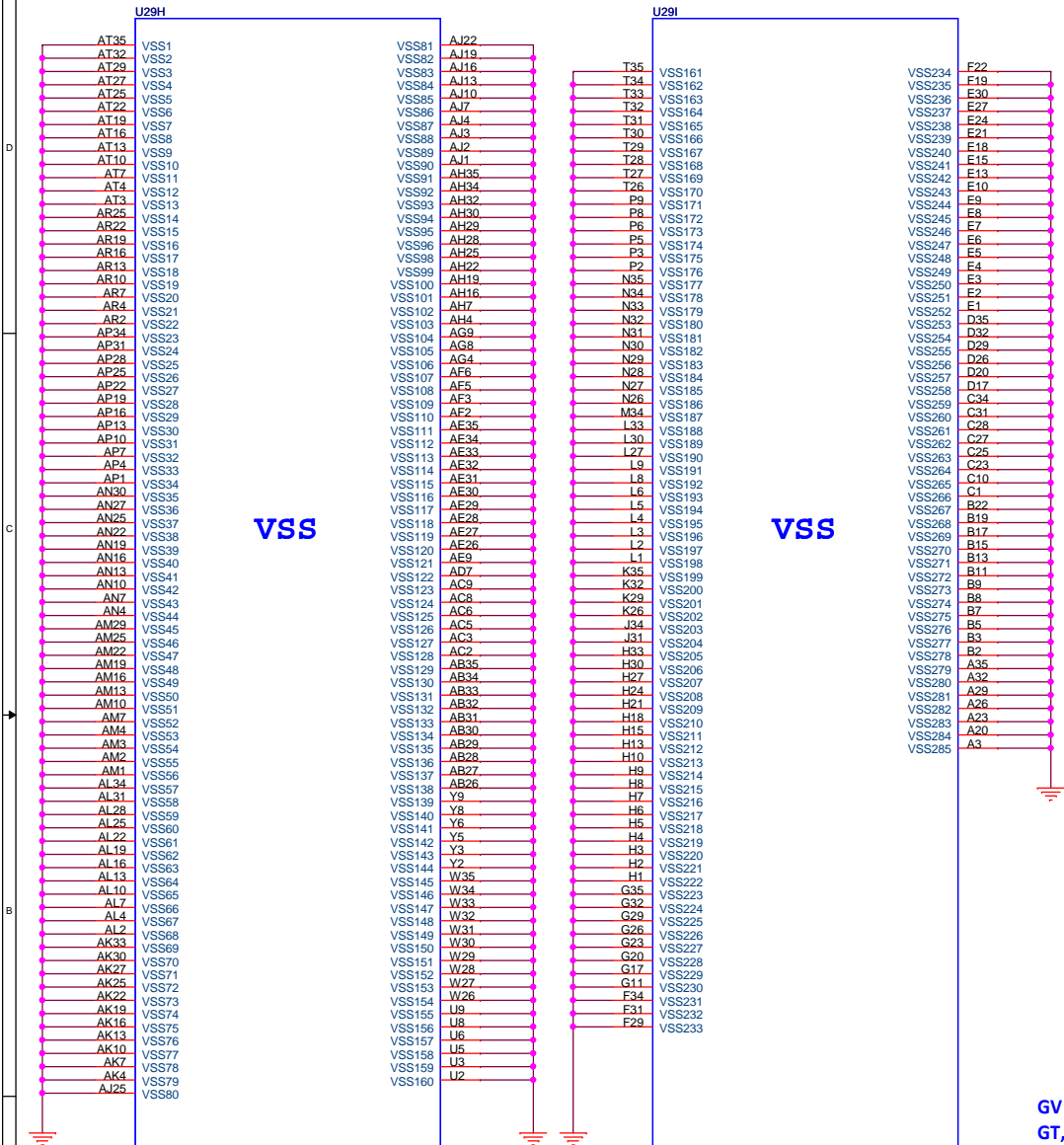


Place PU resistor close to CPU

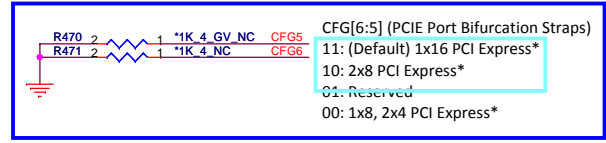


# Ivy Bridge Processor (GND)

# Ivy Bridge Processor (RESERVED, CFG)



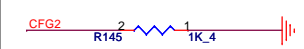
GV - R470 POP  
GT, UMA - ALL NC




## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

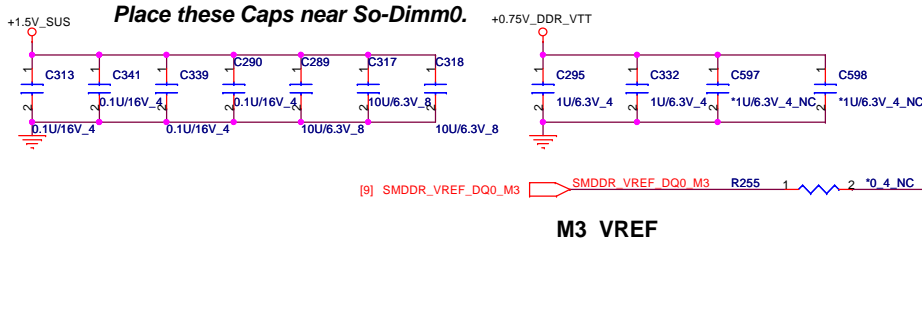
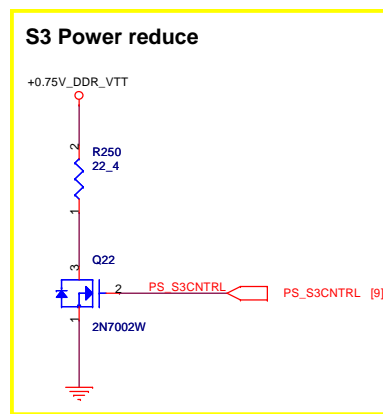
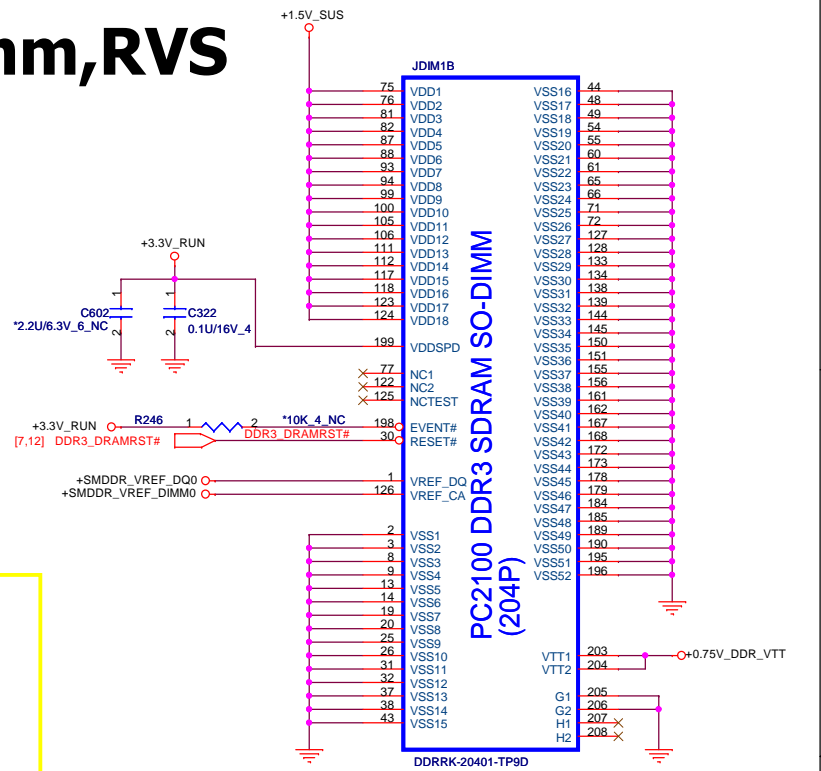
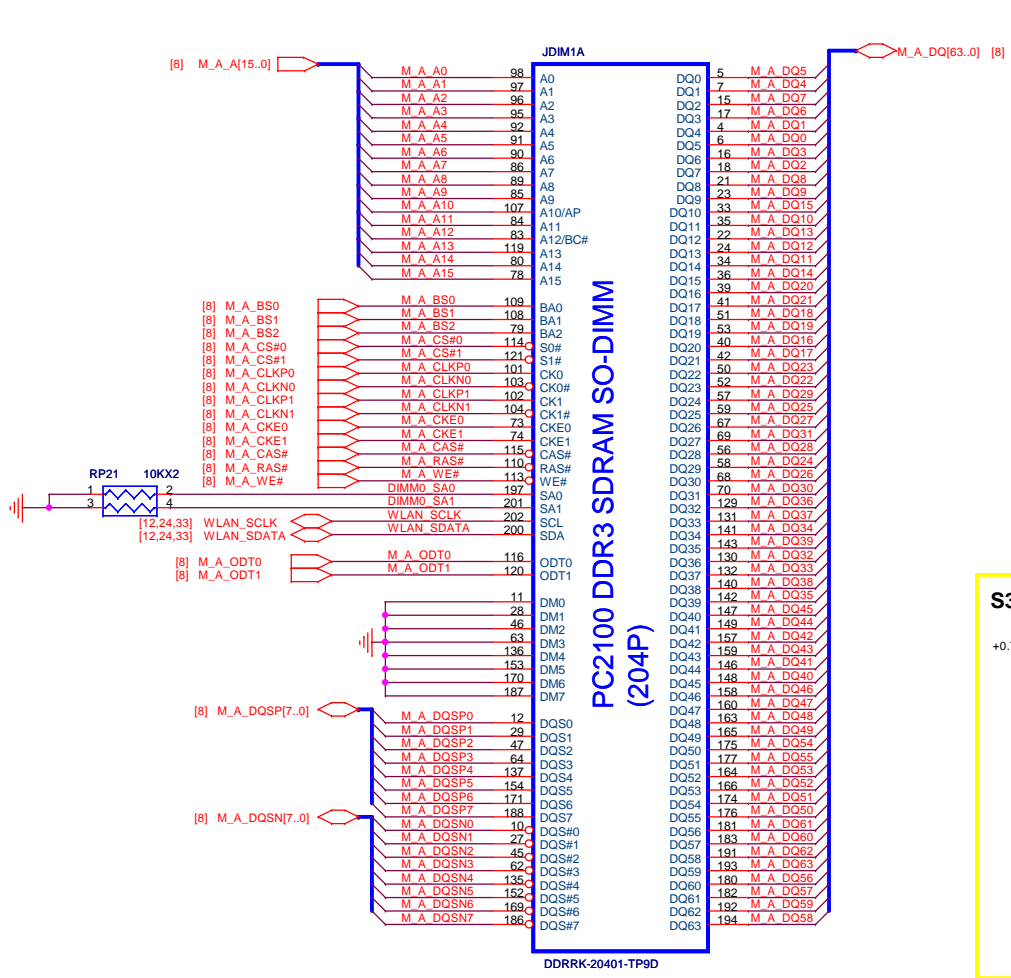




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PROJECT : R09A

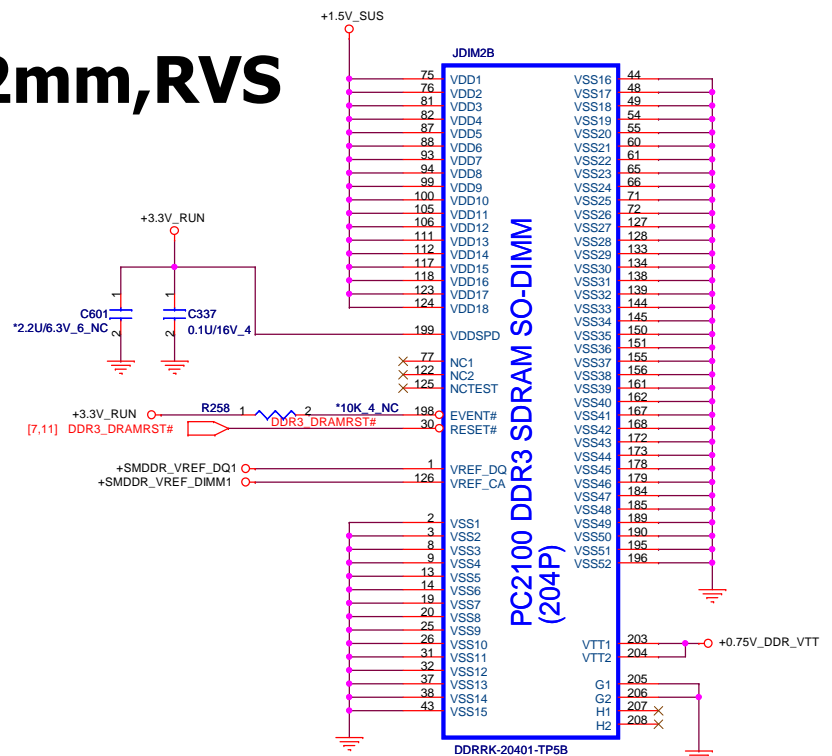
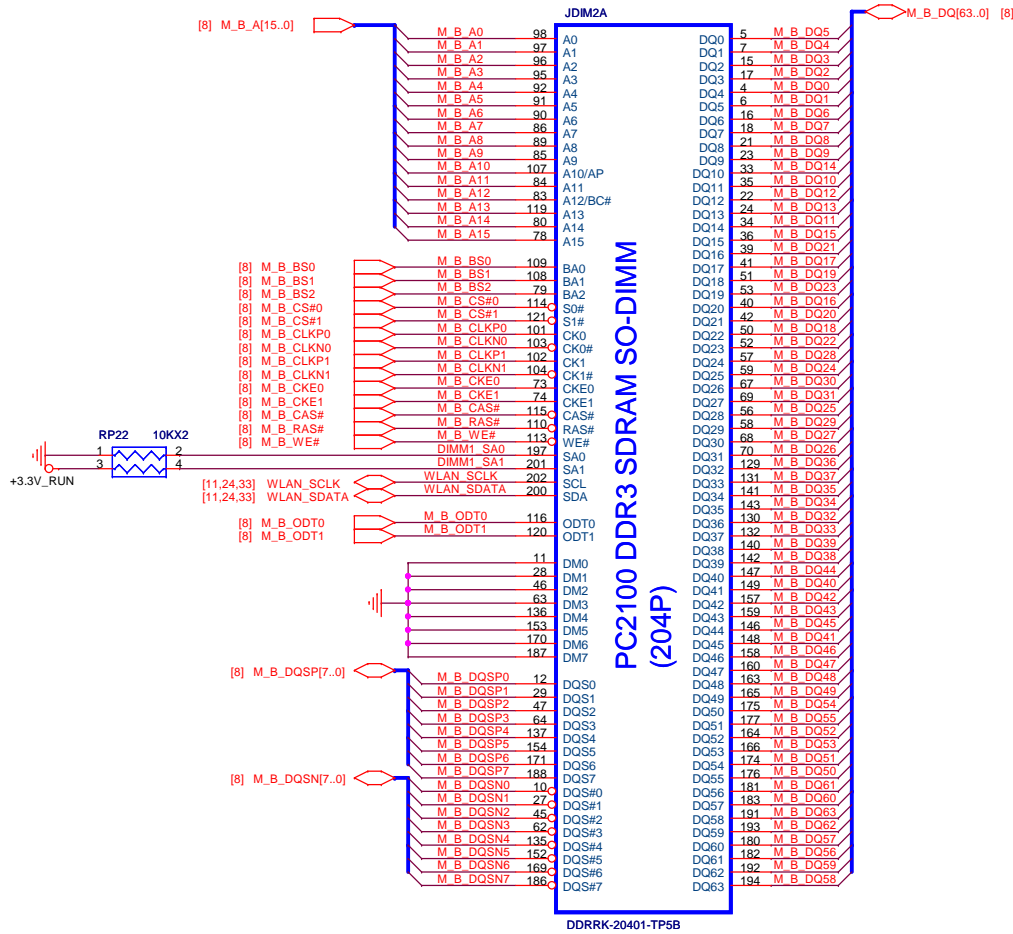
Size	Document Number	Rev
	<b>Ivy Bridge 5/5</b>	3A
Date:	Saturday, March 03, 2012	Sheet 10 of 58

# H=9.2mm,RVS

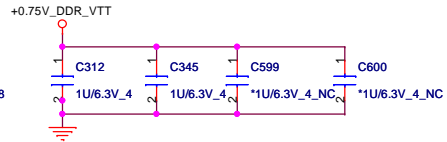
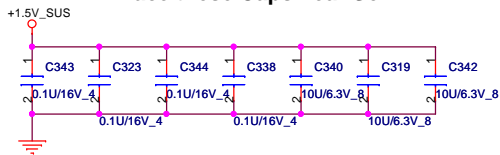


Place these Caps near So-Dimm0.

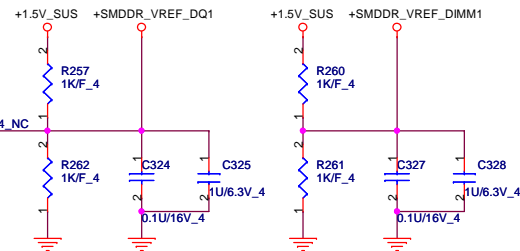
# H=5.2mm,RVS



Place these Caps near So-Dimm1.

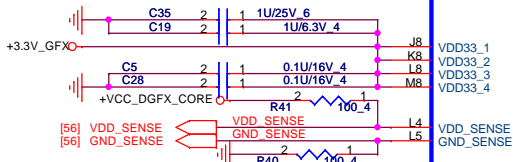
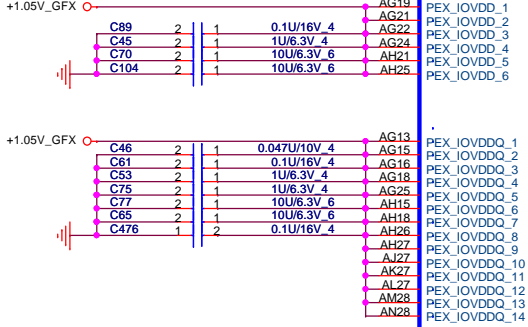


M1 VREF

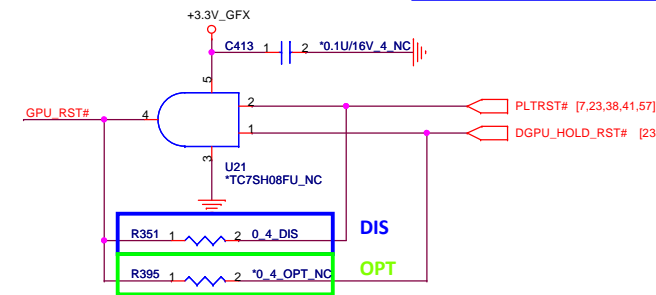
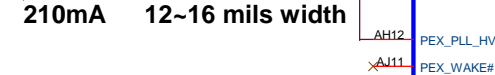
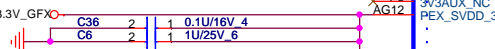
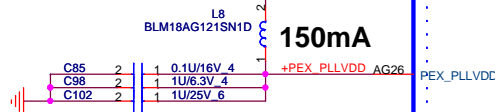


M3 REF

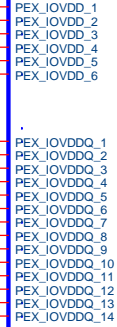
### PEX\_IOVDD/Q <3.3A



12~16 mils width

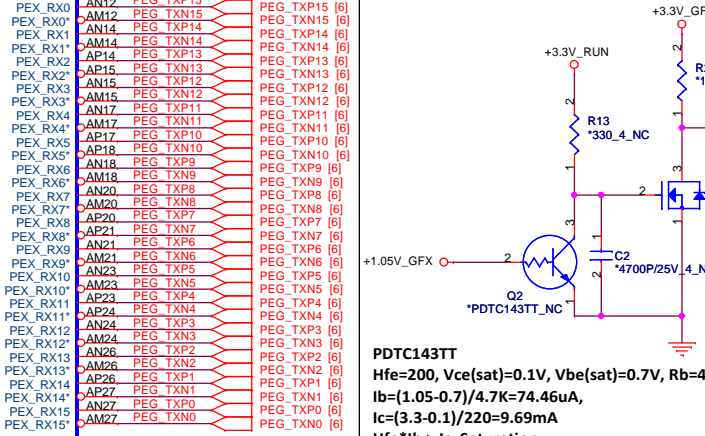


### U24A N13P-GT-A2

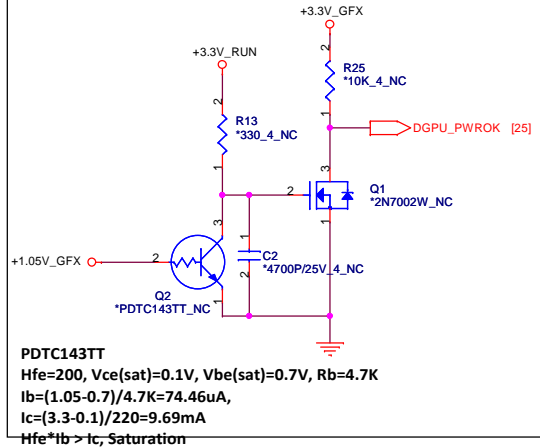


### GB4-128

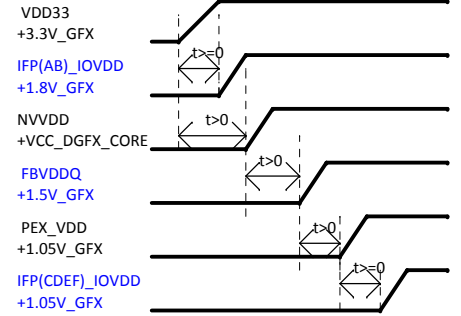
### PCI EXPRESS



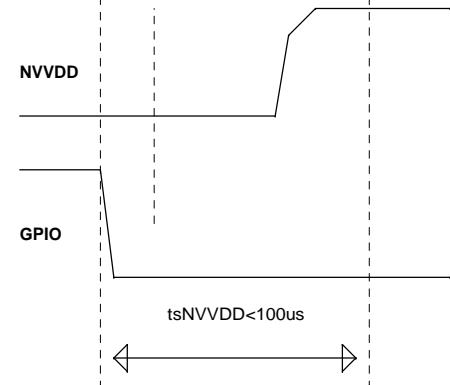
### GPU all PWROK



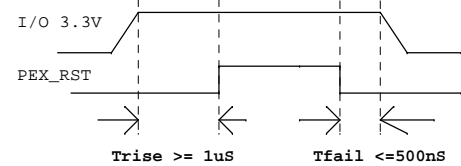
### Power up sequence



### NVVDD Maximum Settling Time



### PEX\_RST timing



0.22uF AC coupling Caps for PCIE GEN1/2/3  
 0.1uF AC coupling Caps for PCIE GEN1/2



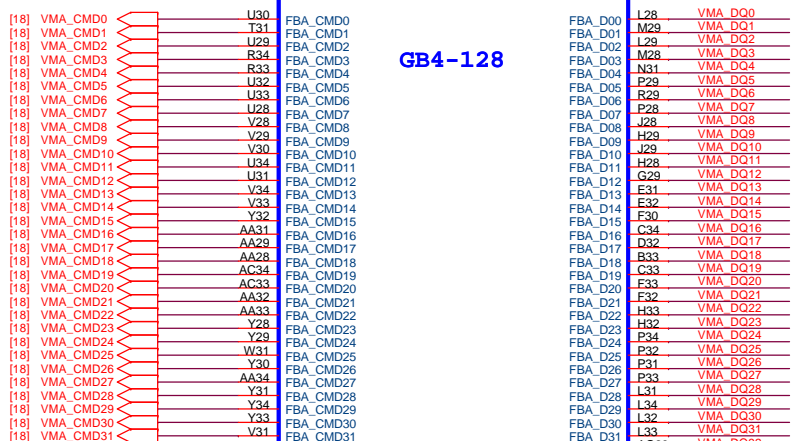
Quanta Computer Inc.

PROJECT : R09A

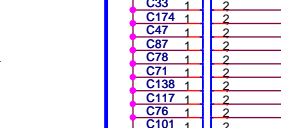
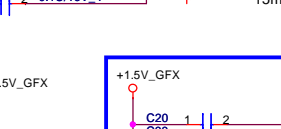
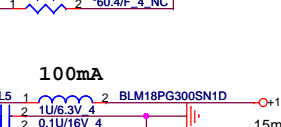
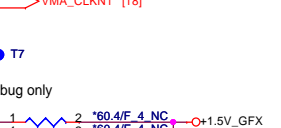
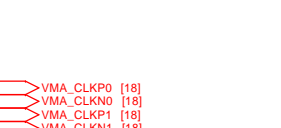
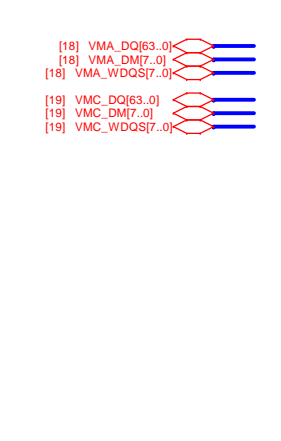
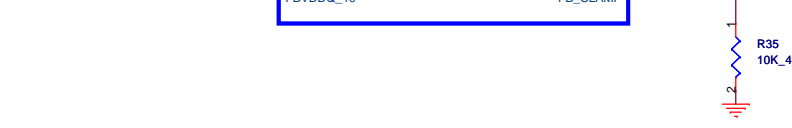
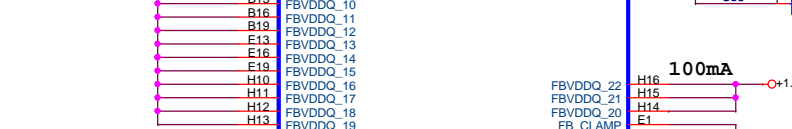
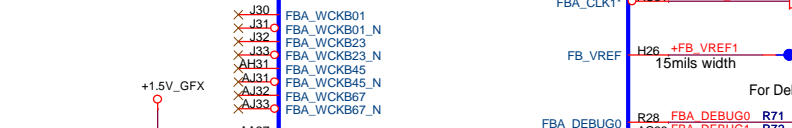
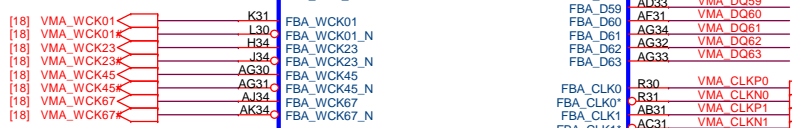
Size Document Number N13P-GS (PCIE I/F) 1/5 Rev 3A

Date: Monday, March 05, 2012 Sheet 13 of 58

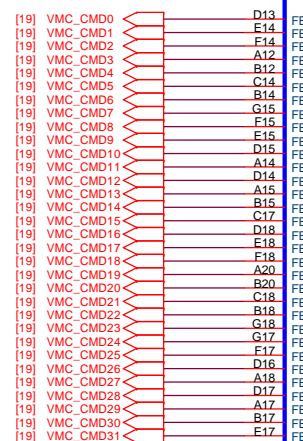
U24B  
N13P-GT-A2



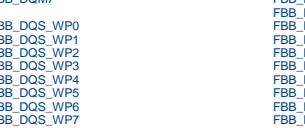
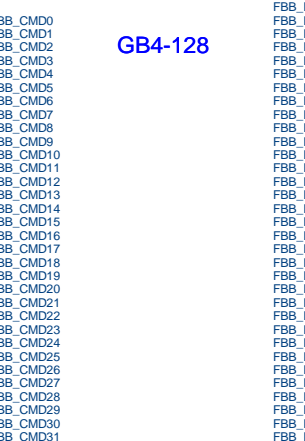
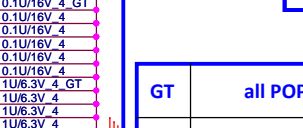
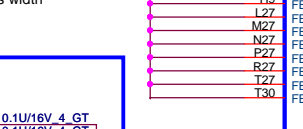
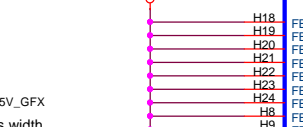
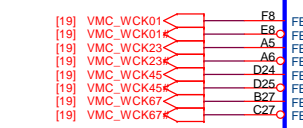
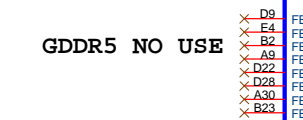
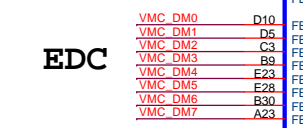
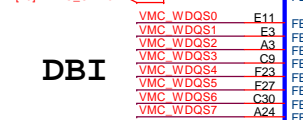
GB4-128



U24C  
N13P-GT-A2



GB4-128



< 0-31 >	< 32-63 >	Memory CS*
CMD0	CMD16	A3_BA3
CMD1	CMD17	A4_BA2
CMD2	CMD18	A5_BA1
CMD3	CMD19	WE*
CMD4	CMD20	A7_A8
CMD5	CMD21	A6_A11
CMD6	CMD22	ABT*
CMD7	CMD23	A12_RFU
CMD8	CMD24	A0_A10
CMD9	CMD25	A1_A9
CMD10	CMD26	RAS*
CMD11	CMD27	RAS*
CMD12	CMD28	RST*
CMD13	CMD29	CKE*
CMD14	CMD30	CAS*
CMD15	CMD31	CAS*

DBI

EDC

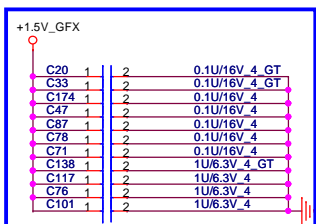
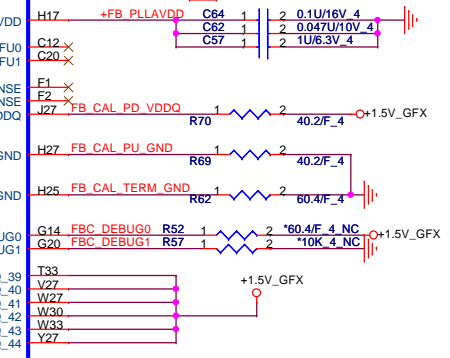
GDDR5 NO USE

DBI

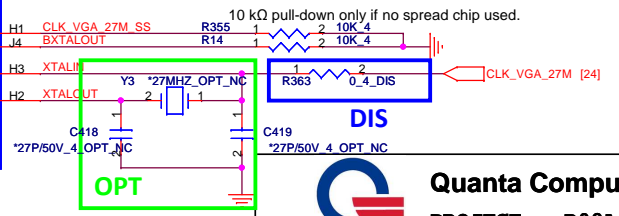
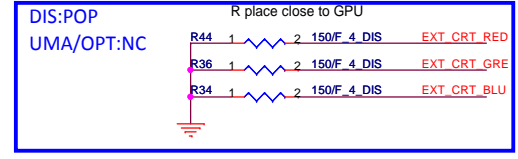
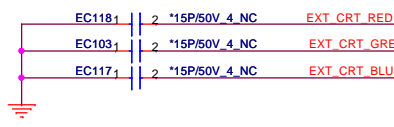
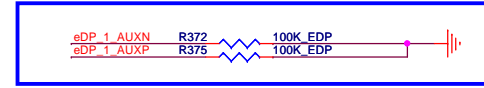
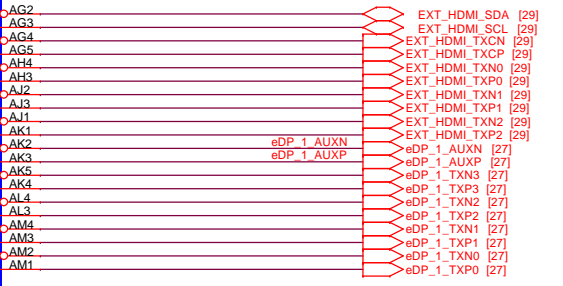
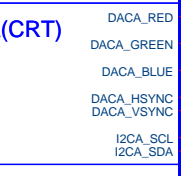
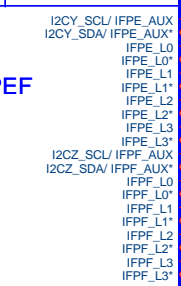
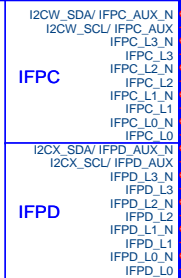
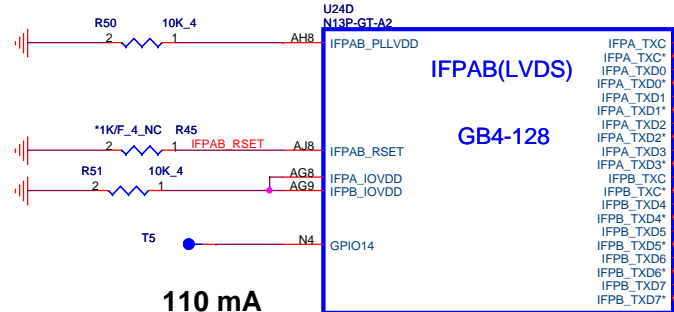
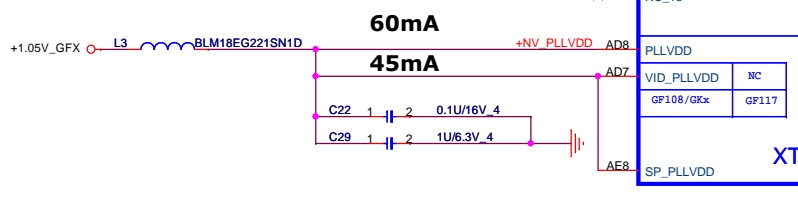
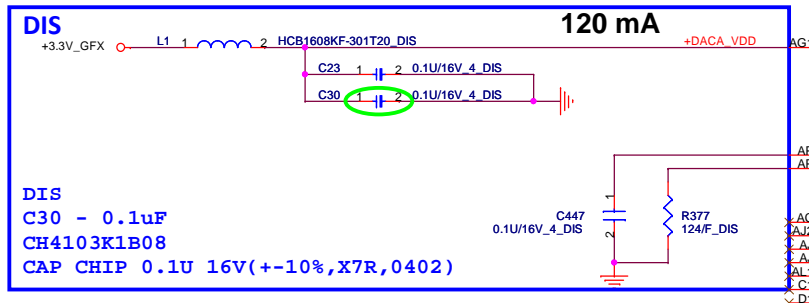
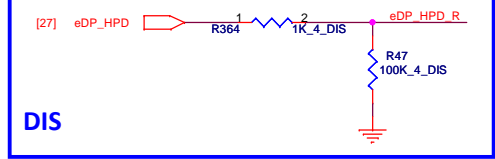
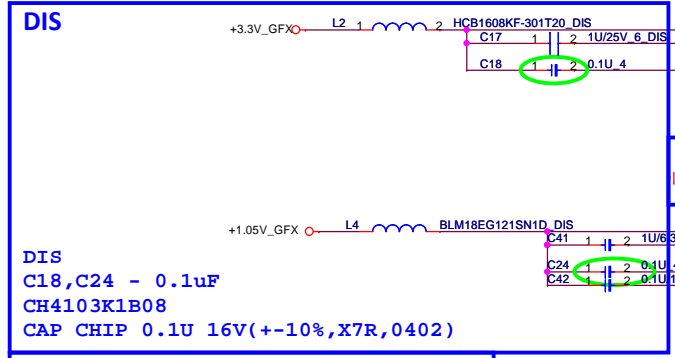
EDC

GDDR5 NO USE

MEMORY I/F C

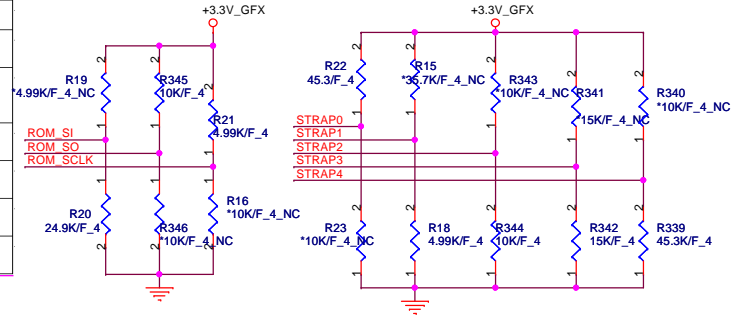


GT	all POP
GV	NC C20,C33,C138



### N13P-GT

	N13P-GT-OPT	N13P-GT-DIS
ROM_SCLK	5K-PU	5K-PU
ROM_SO	10K-PU	10K-PU
ROM_SI	GDDR5 Hynix-128MX16*25K-PD Samsung-128Mx16-30K-PD	GDDR5 Hynix-128MX16*25K-PD Samsung-128Mx16-30K-PD
STRAP-1	5K-PD	5K-PD
STRAP-2	10K-PD	10K-PD
STRAP-3	5K-PD	15K-PD
STRAP-4	45K-PD	45K-PD



### N13P-GV

For N13P-GV-B-A2, the h/w strap setting must be modified as below

ROM\_SO PD 10K  
ROM\_SI PD 10K  
ROM\_SCLK PD 10K  
Strap 4 PD 10K

For Hynix 128MX16 GDDR5  
Strap 3 PD 10K  
Strap 2 PU 10K  
Strap 1 PD 10K  
**Strap 0 PD 10K**

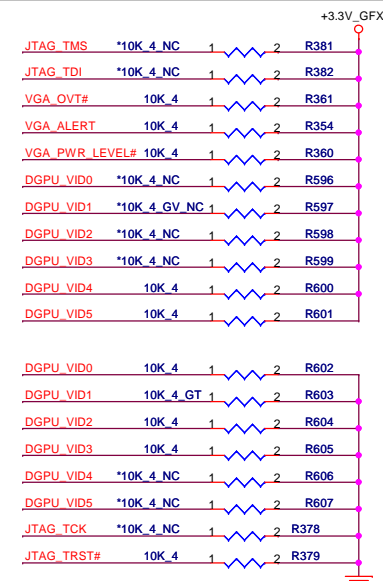
For Samsung 128MX16 GDDR5  
Strap 3 PD 10K  
Strap 2 PU 10K  
Strap 1 PD 10K  
**Strap 0 PU 10K**

Default: Hynix VRAM (0100) VRAM Configuration Table

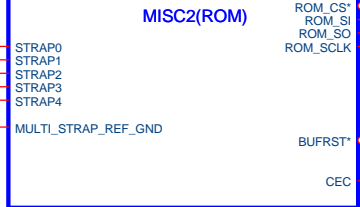
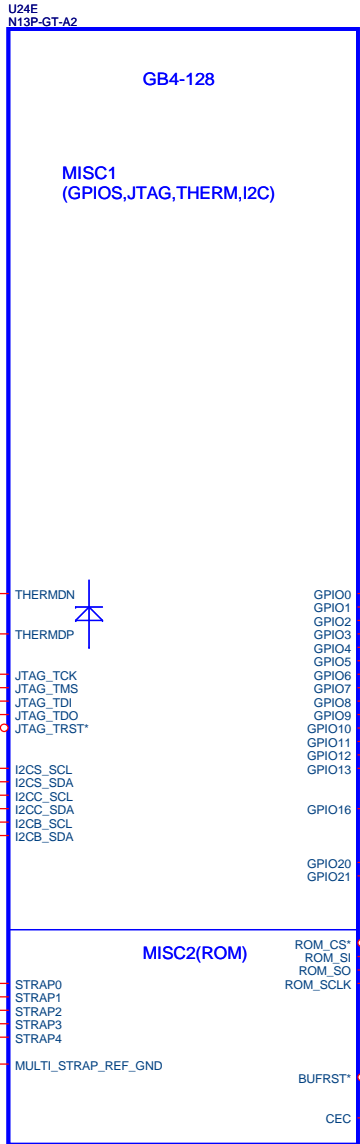
RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0100	GDDR5 128Mx16, 2500MHz	Hynix	AKG5MWUW14	H5GQ2H24MFR-T2C	PD 25K
0101	GDDR5 128Mx16, 2500MHz	Samsung	AKG5MWD7509	K4G20325FD-F	PD 30K

SOR_EXPOSED[3:0]	STRAP3
0000	Optimus PD 5K
0010	Discret only PD 15K

Display configuration table



GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	NVDD VID4
1	OUT	N/A	NVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID1
6	OUT	N/A	NVDD VID2
7	OUT	N/A	3D VERSION LEFT/RIGHT SIGNAL
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	MEMORY VREF CONTROL
11	OUT	N/A	NVDD VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVDD VID5

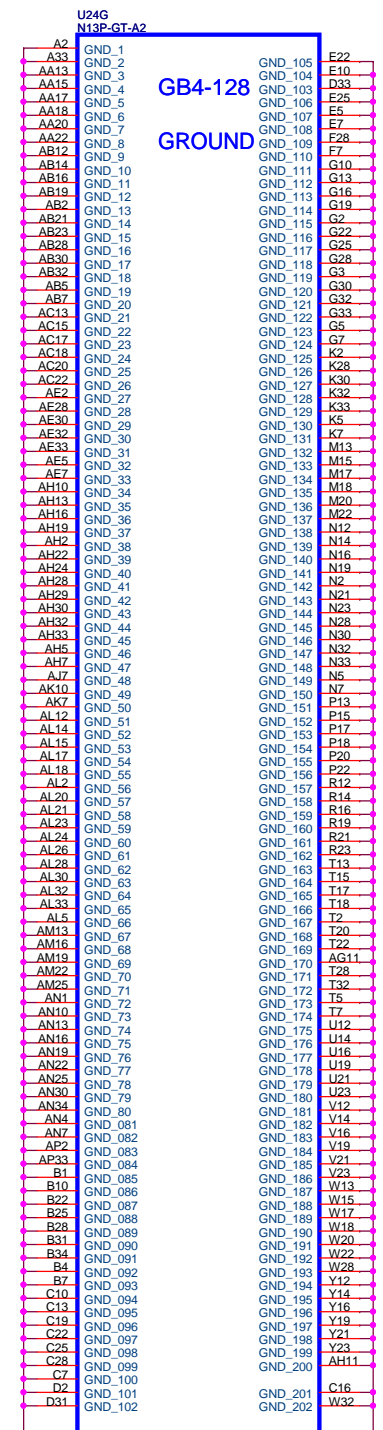
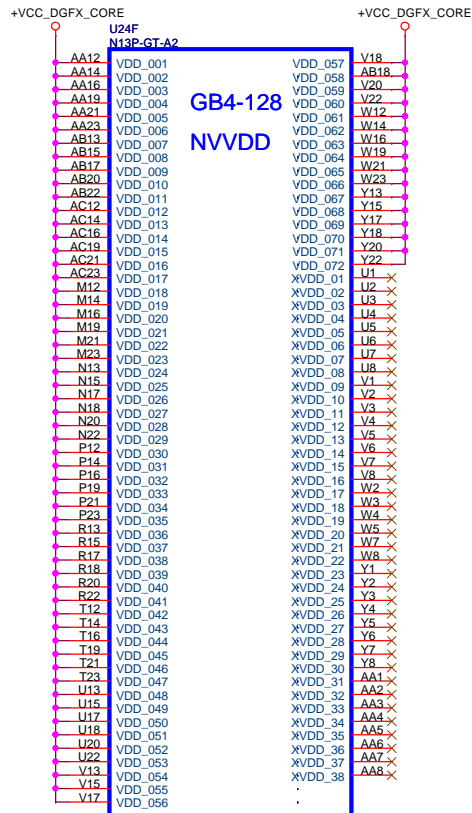


	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GV (QS)	0.875V	0	1	0	0	1	1
N13P-GT (QS)	0.9V	0	0	0	0	1	1

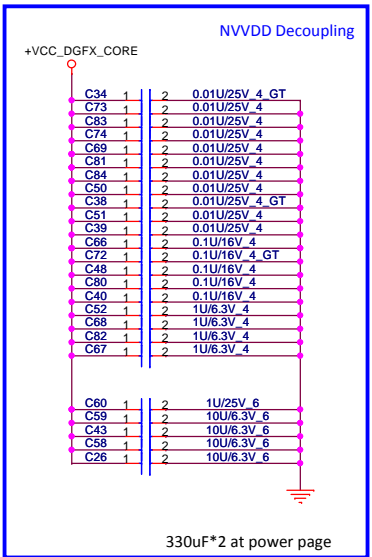
**Quanta Computer Inc.**  
PROJECT : R09T

Size: Document Number: N13P-GT (GPIO&STRAPS) 4/5 Rev 2B  
Date: Wednesday, March 21, 2012 Sheet 16 of 57





GT: 60A	all POP
GV: 42A	NC C34,C38,C72



LOWER HALF

UPPER HALF

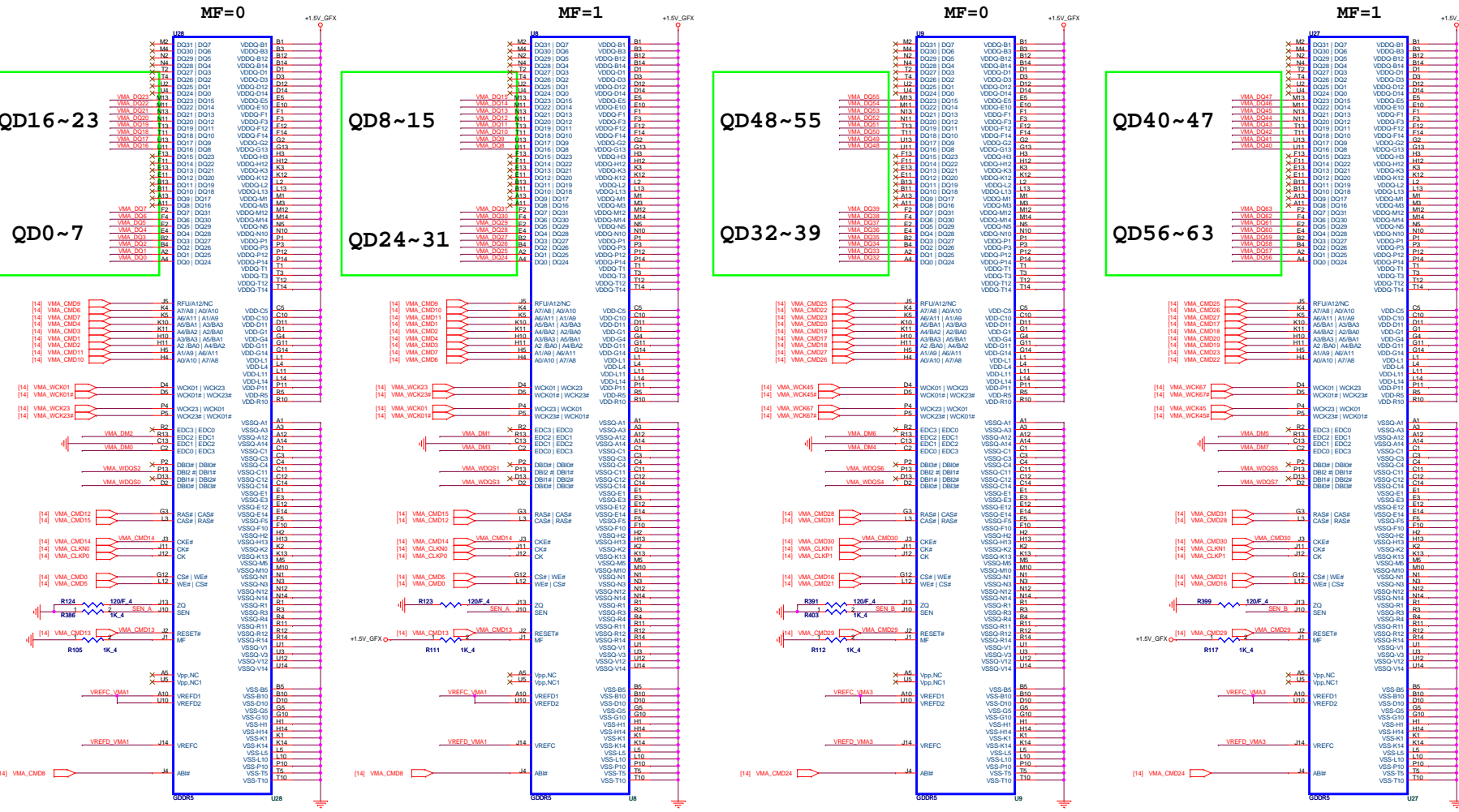
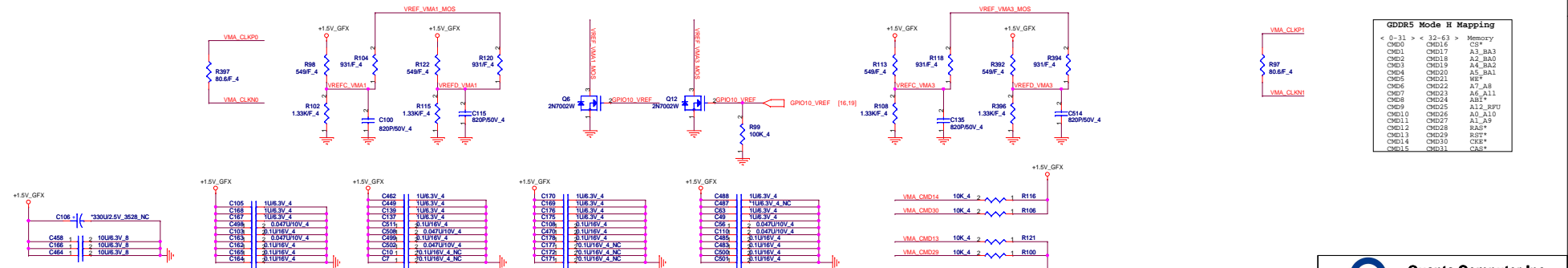


Table titled 'GDDR5 Mode H Mapping' showing memory bank and bit assignments for channels C0 through C8.



CHANNEL B: 1024MB GDDR5

LOWER HALF

UPPER HALF

MF=0

MF=1

MF=0

MF=1

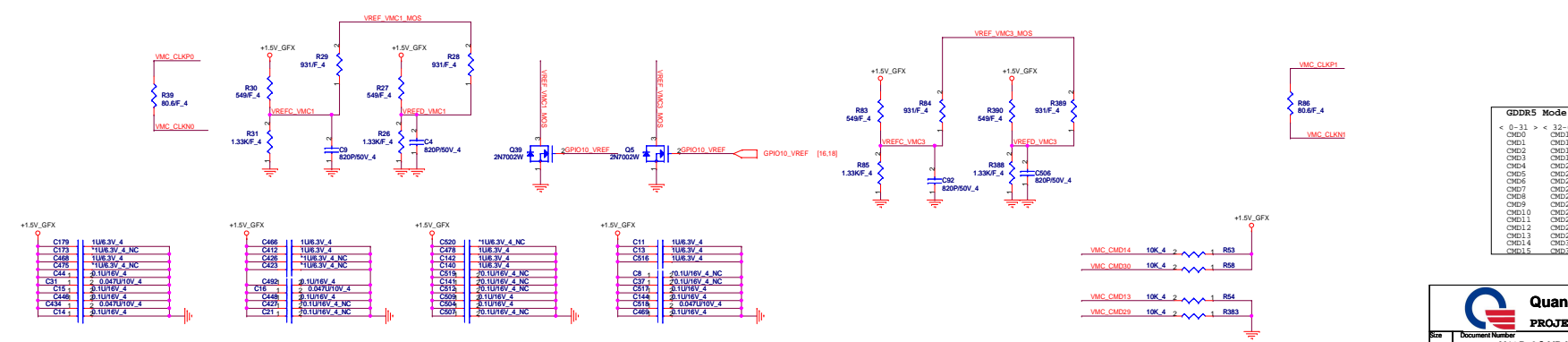
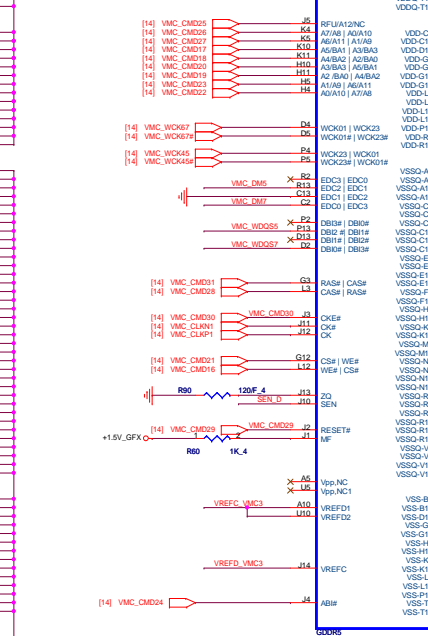
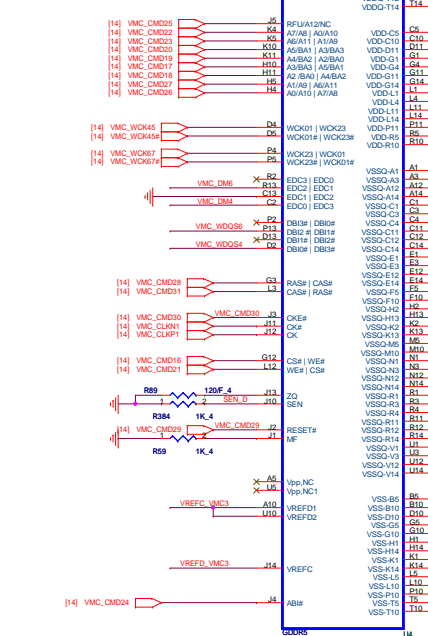
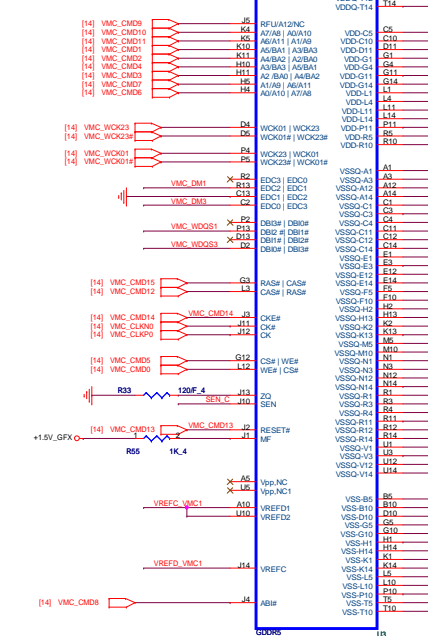
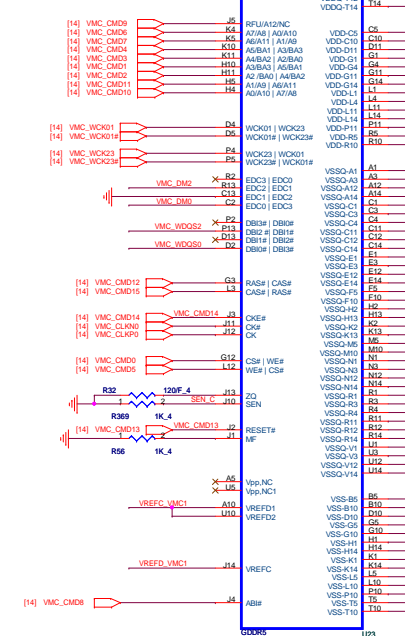
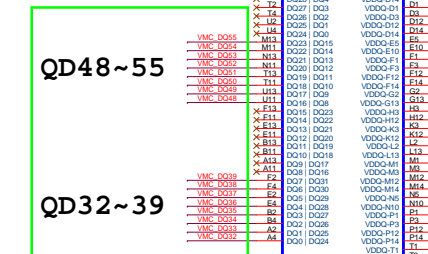
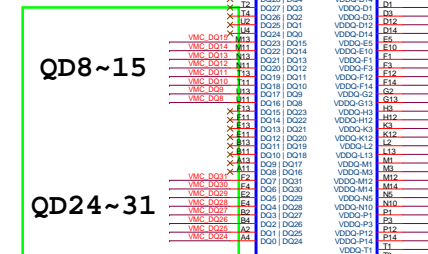
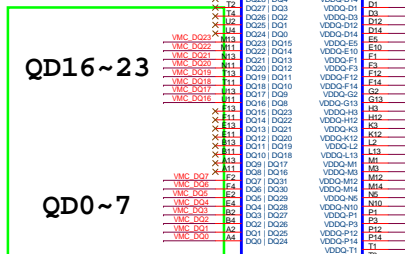
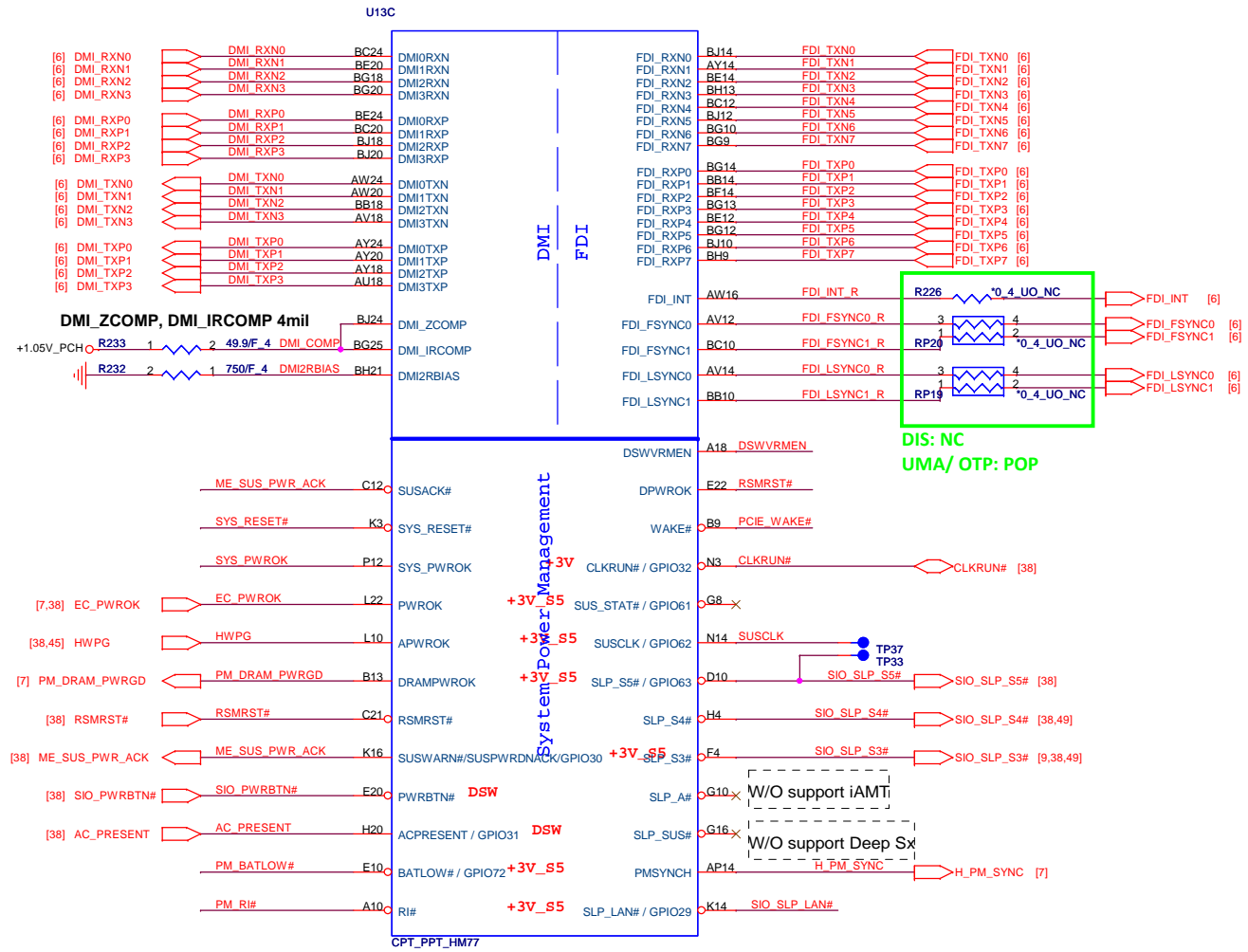
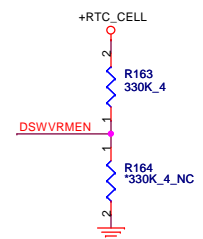
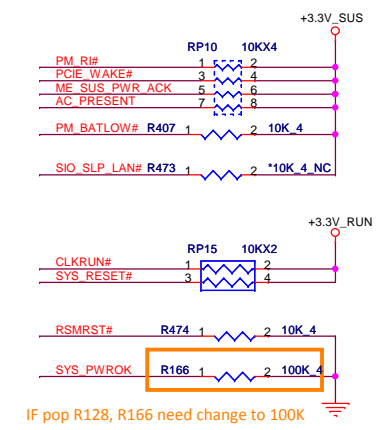


Table titled 'GDDR5 Mode H Mapping' listing memory bank mappings for modes 0-31 and 32-63.

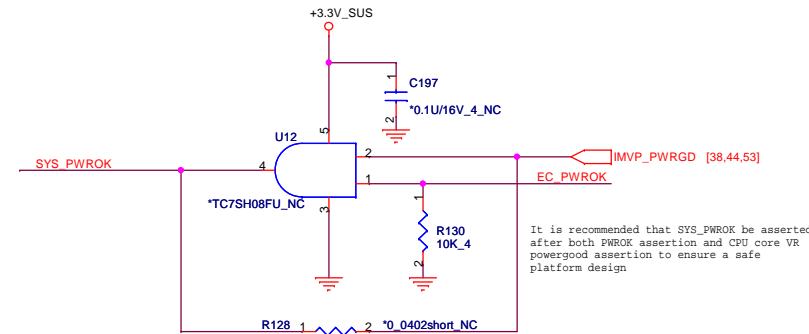
# Cougar Point/Panther Point (DMI, FDI, PM)



## PCH Pull-high/low(CLG)

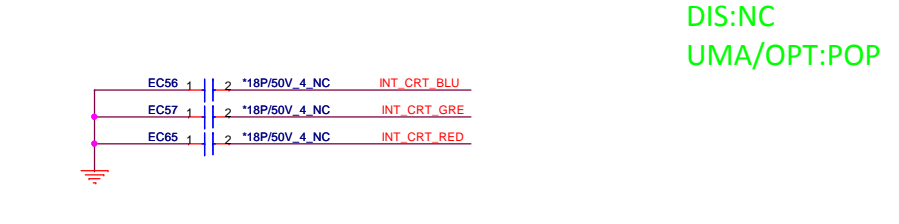
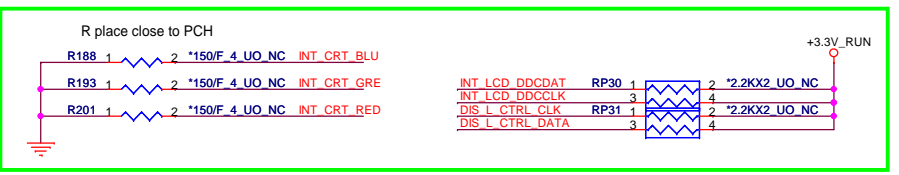
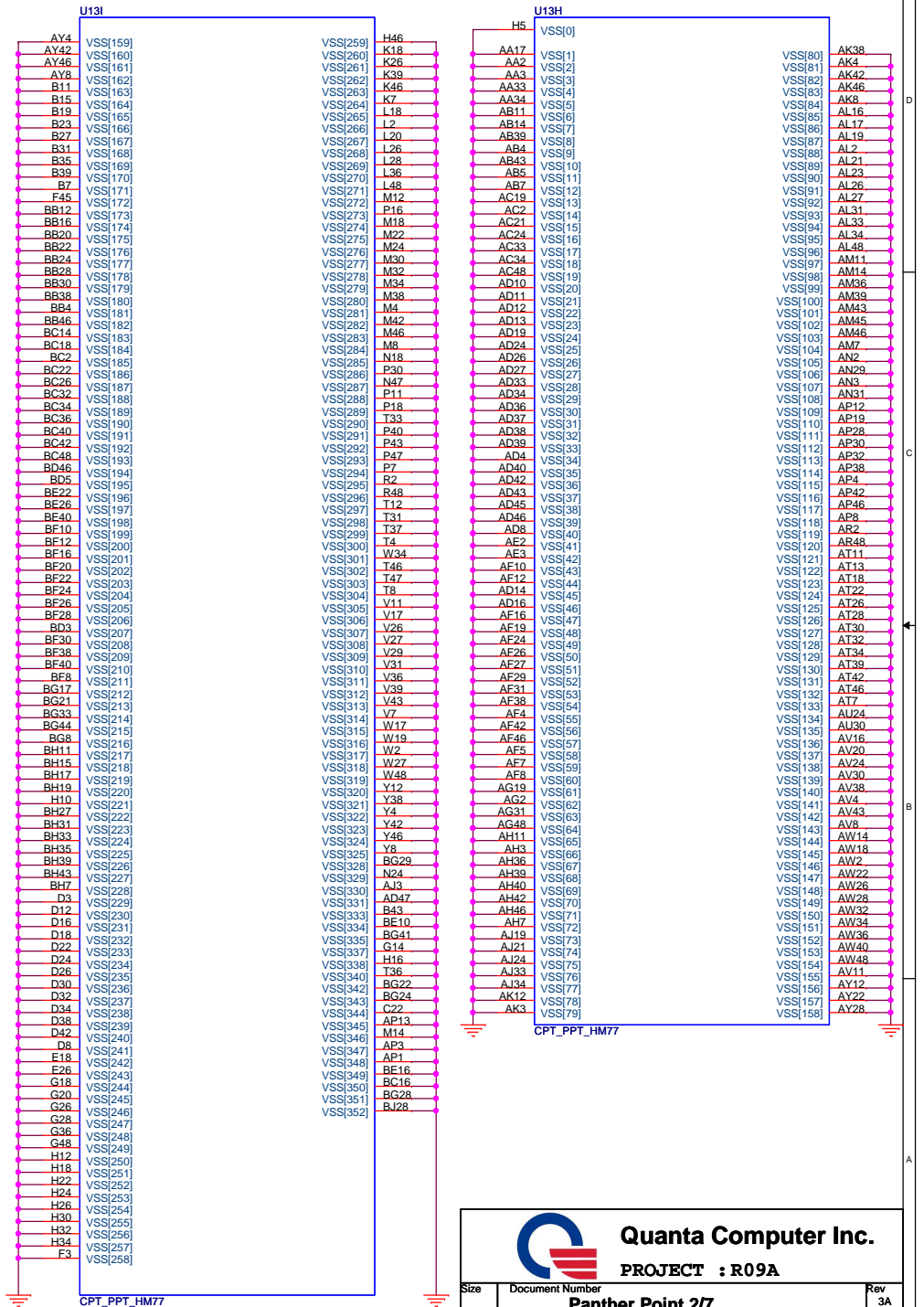
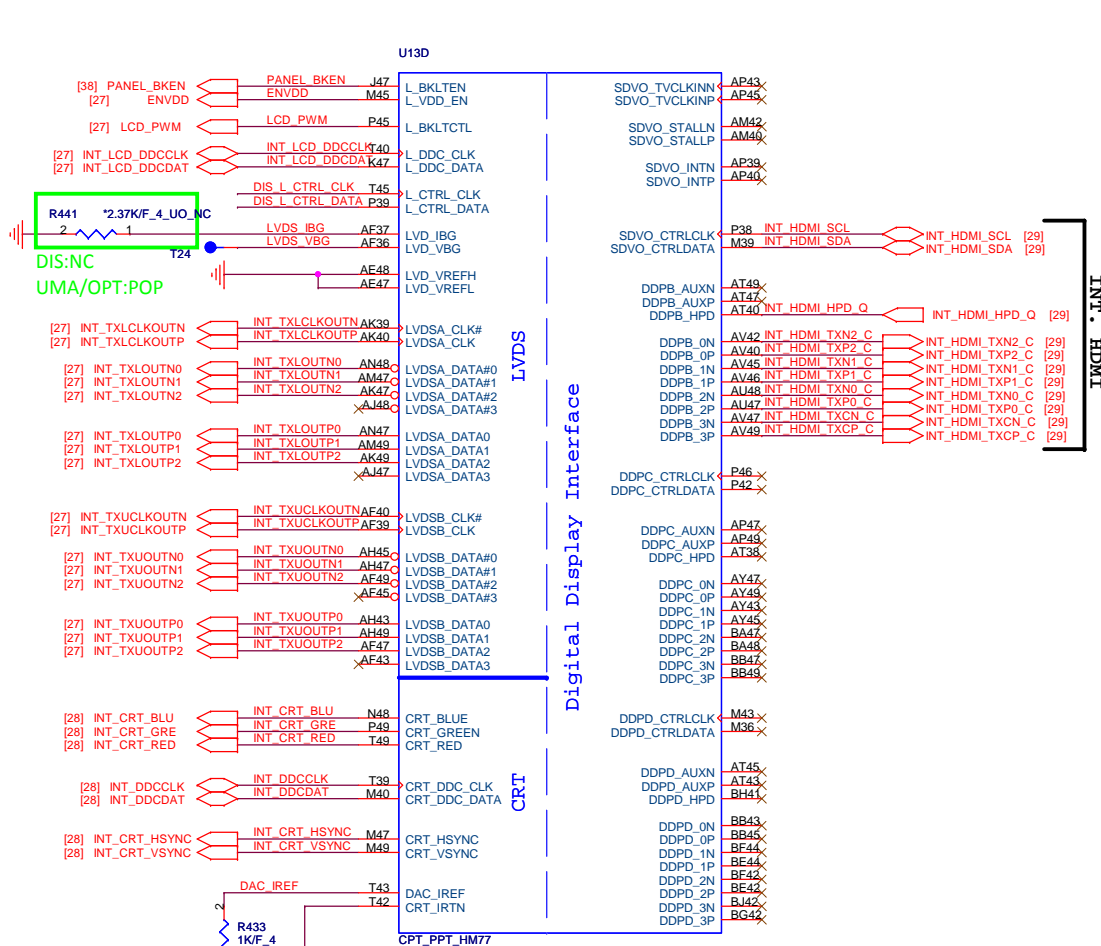



On Die DSW VR Enable  
 High = Enable (Default)  
 Low = Disable



# Cougar Point/Panther Point (LVDS,DDI)

# Cougar Point/Panther Point (GND)

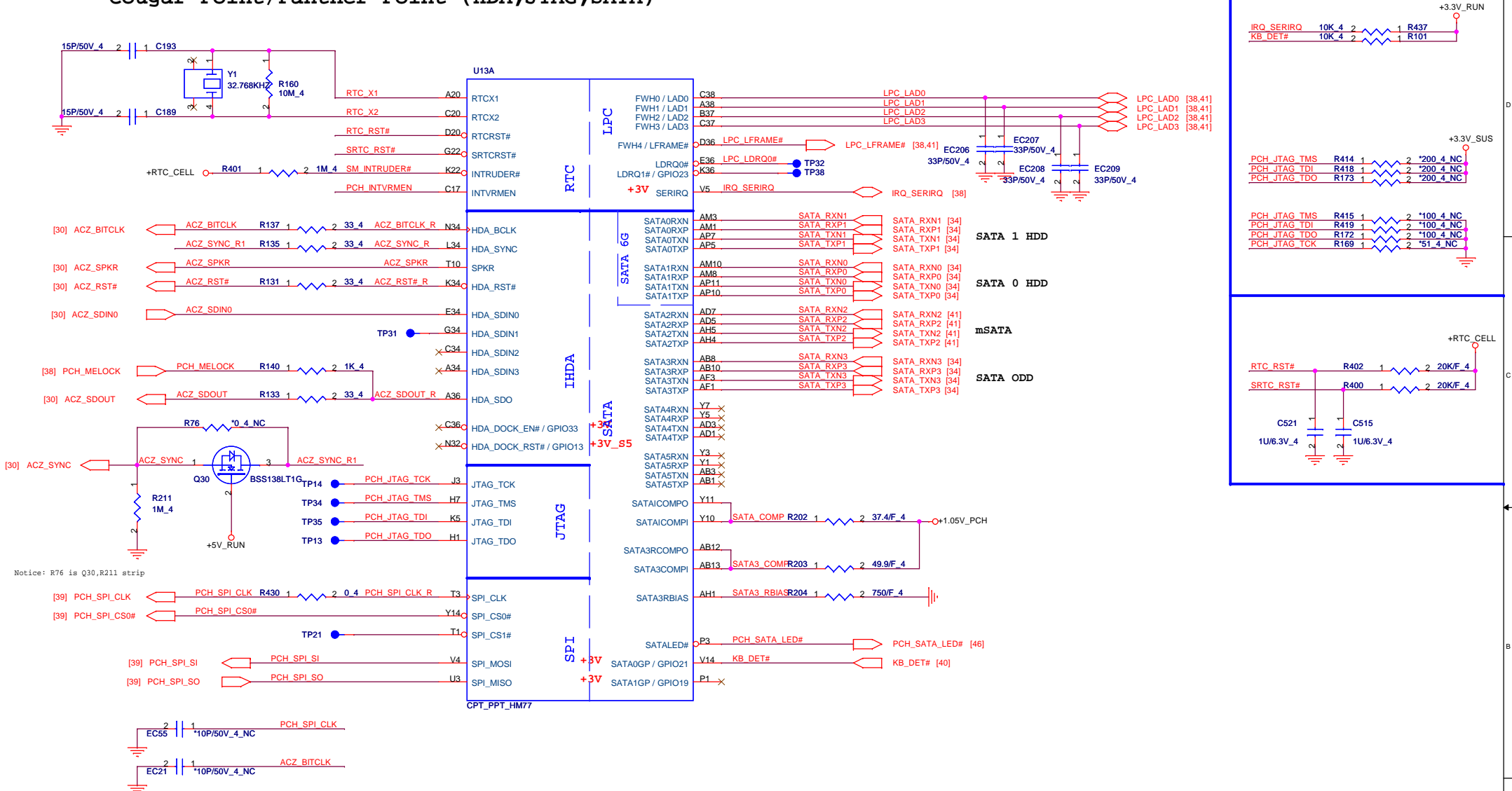




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	<b>Panther Point 2/7</b>		
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# Cougar Point/Panther Point (HDA,JTAG,SATA)

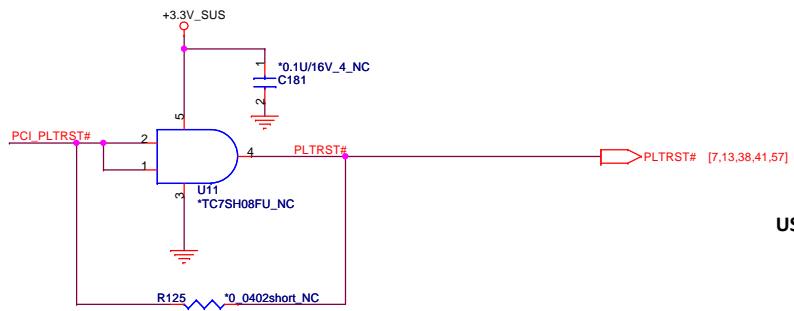
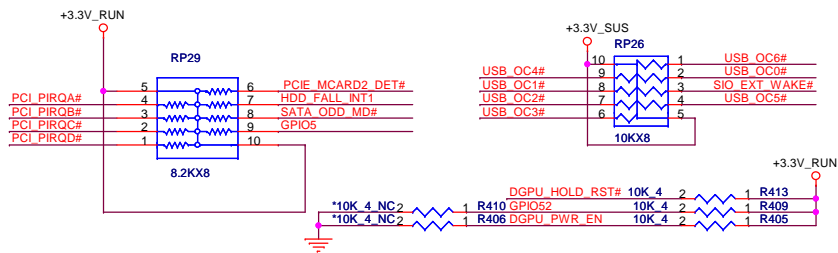


Notice: R76 is Q30,R211 strip

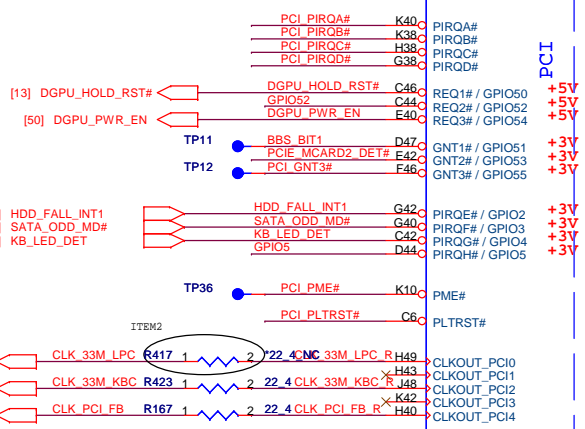
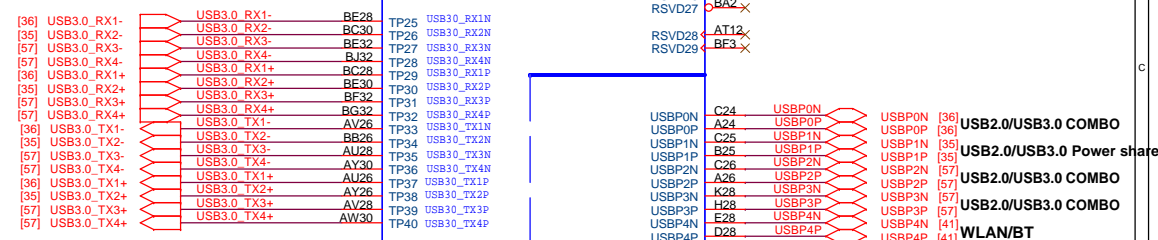
**PCH Strap Table**

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	NC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	NC
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○ R162 1 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○ R134 1 2 1K 4 ACZ_SYNC R

# Cougar Point-M/Panther Point (PCI,USB,NVRAM)

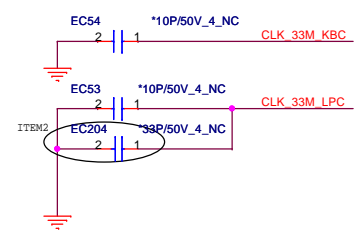
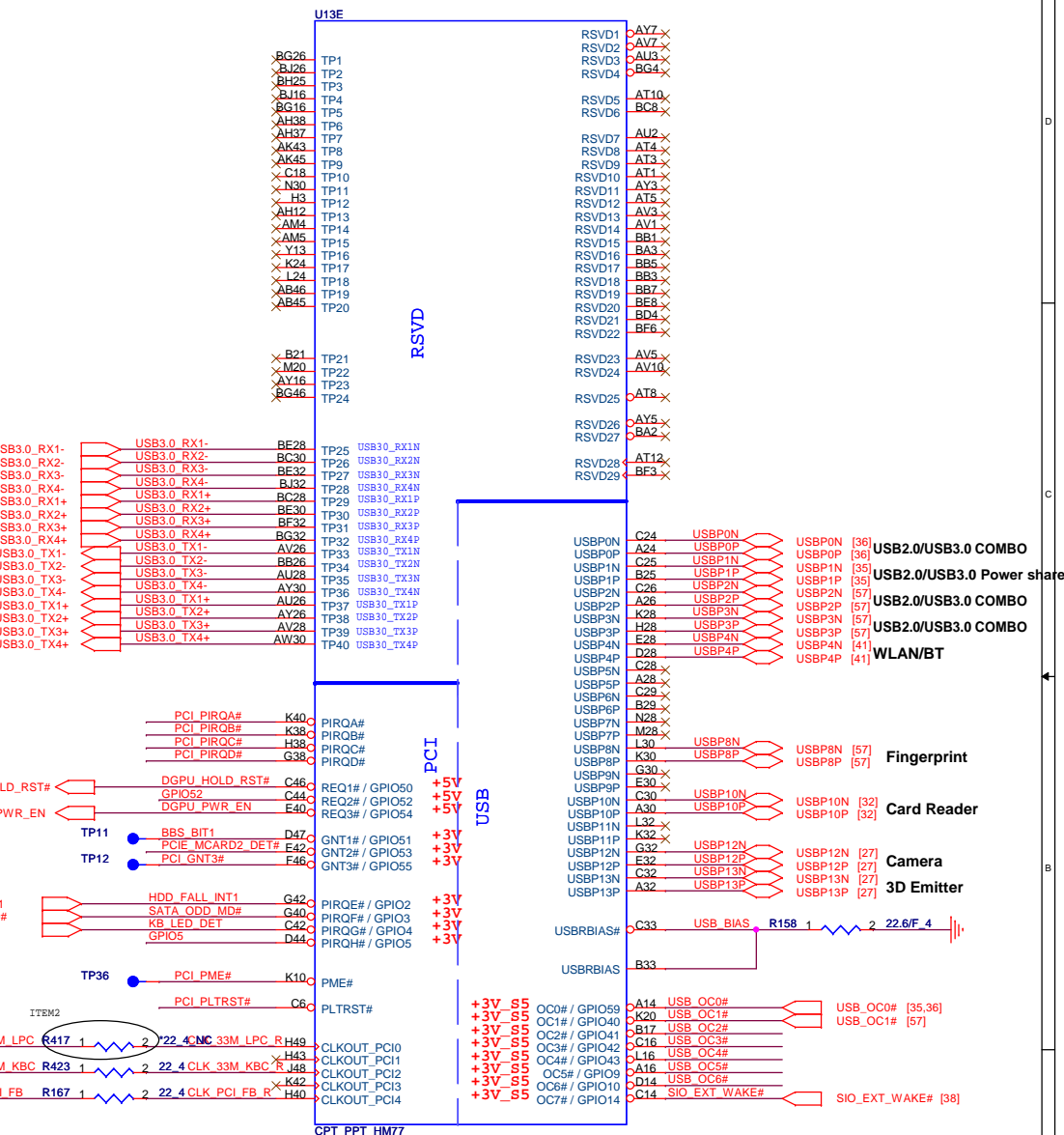
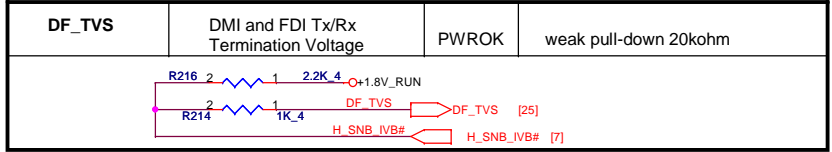


## USB3.0

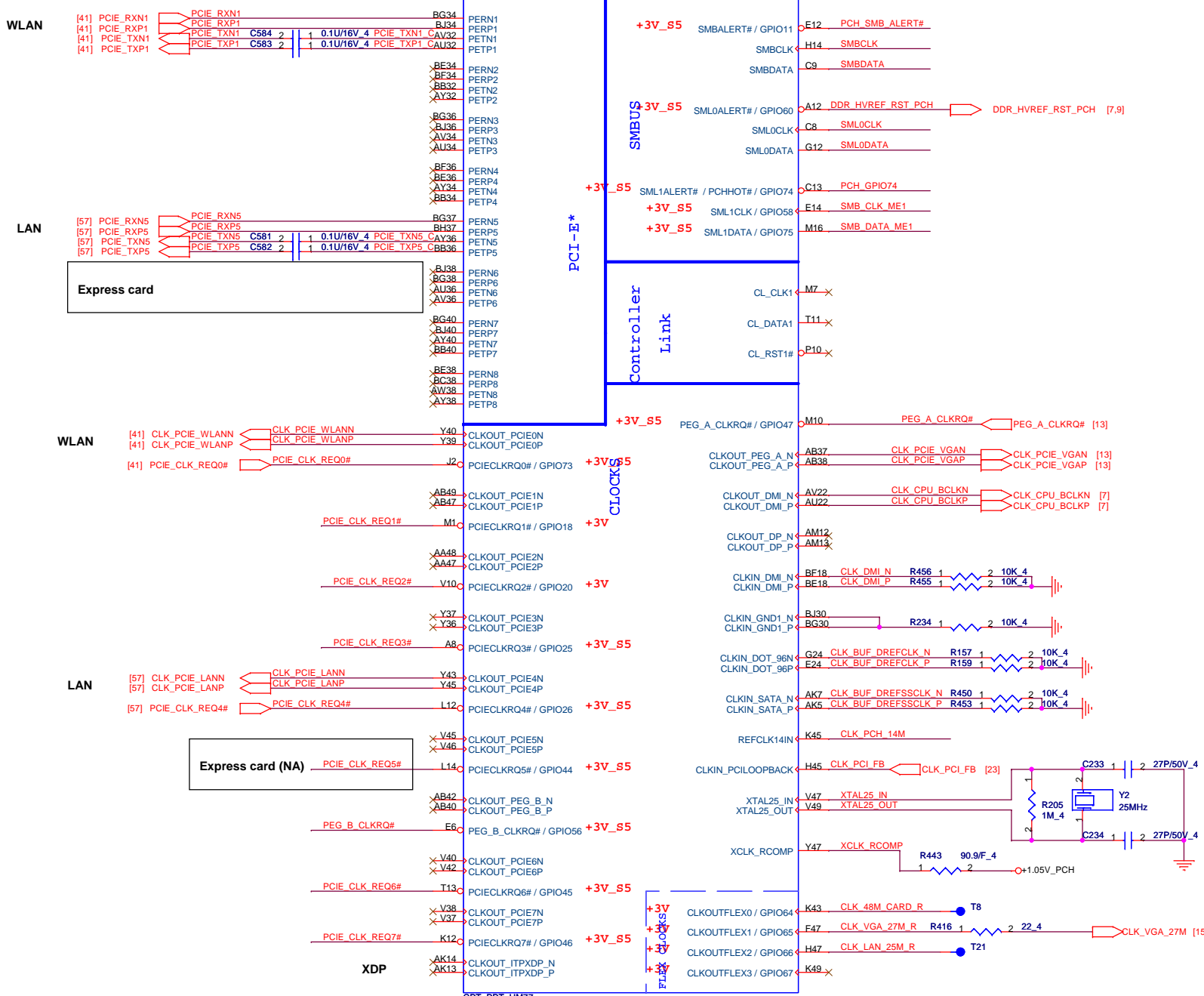


Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>Bit 0</th> <th>Bit 1</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
			Bit 0	Bit 1	Boot Location							
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										

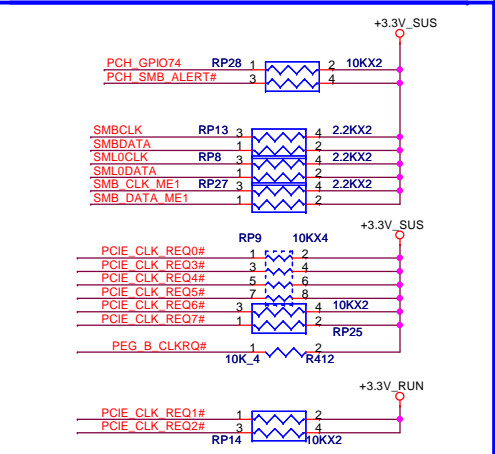
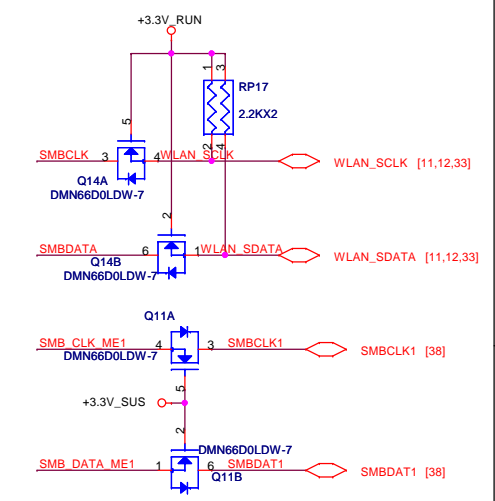
Default weak pull-up on GNT0/1#  
[Need external pull-down for LPC BIOS]



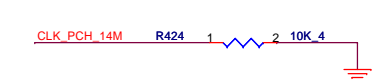
# U13B Cougar Point-M/Panther Point (PCI-E, SMBUS, CLK)



## SMBus/Pull-up (CLG)



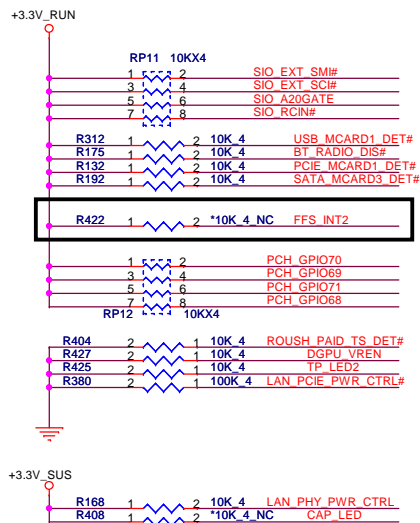
## Stuff for Integrated CLK Gen Mode



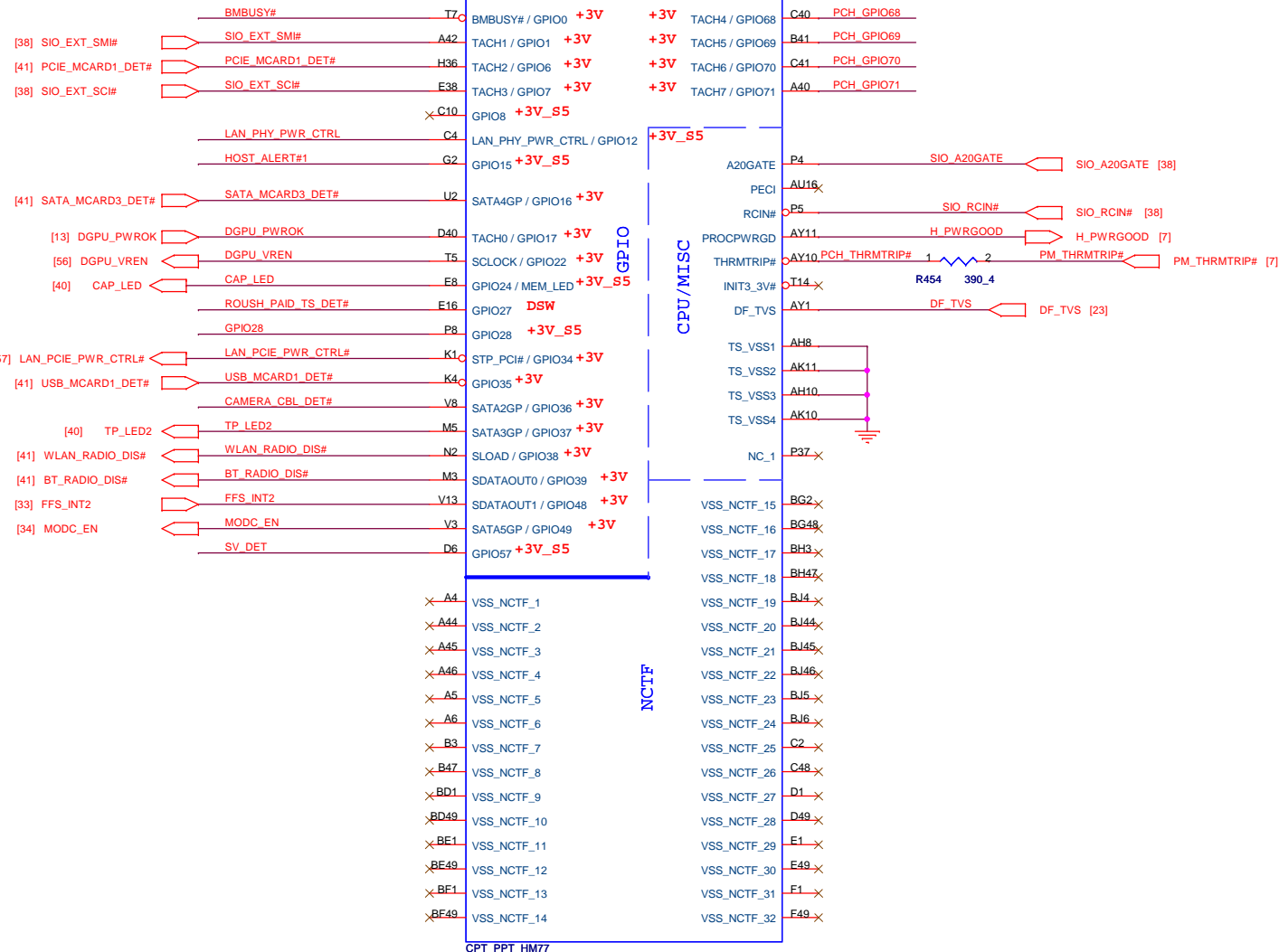
	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48 / 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27 / 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)



# Cougar Point/Panther Point (GPIO,VSS\_NCTF,RSVD)



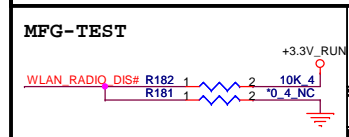
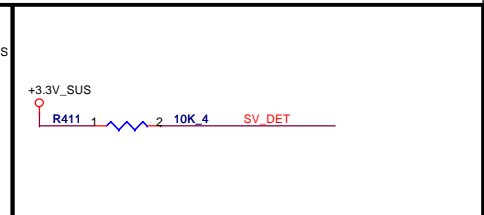
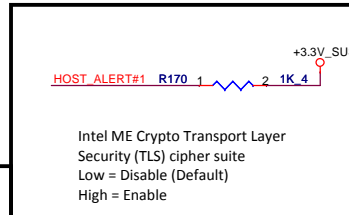
Vostro POP - NA



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

**CHECK LIST:**  
When Unused as GPIO or SATA\*GP - Use 8.2K-10K pull-down to ground.

BMBUSY#:  
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3\_3.  
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.



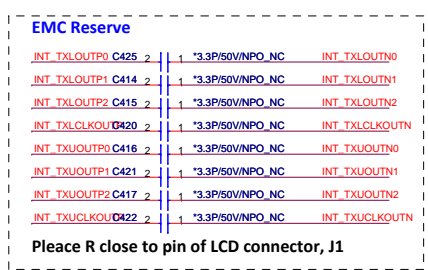
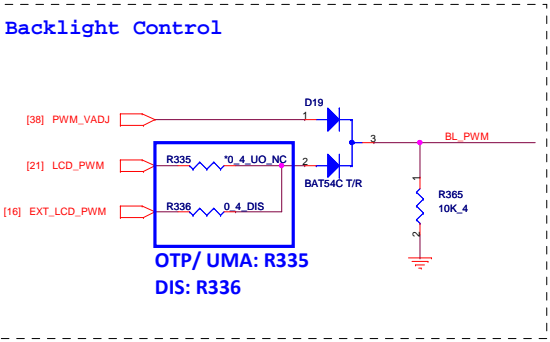
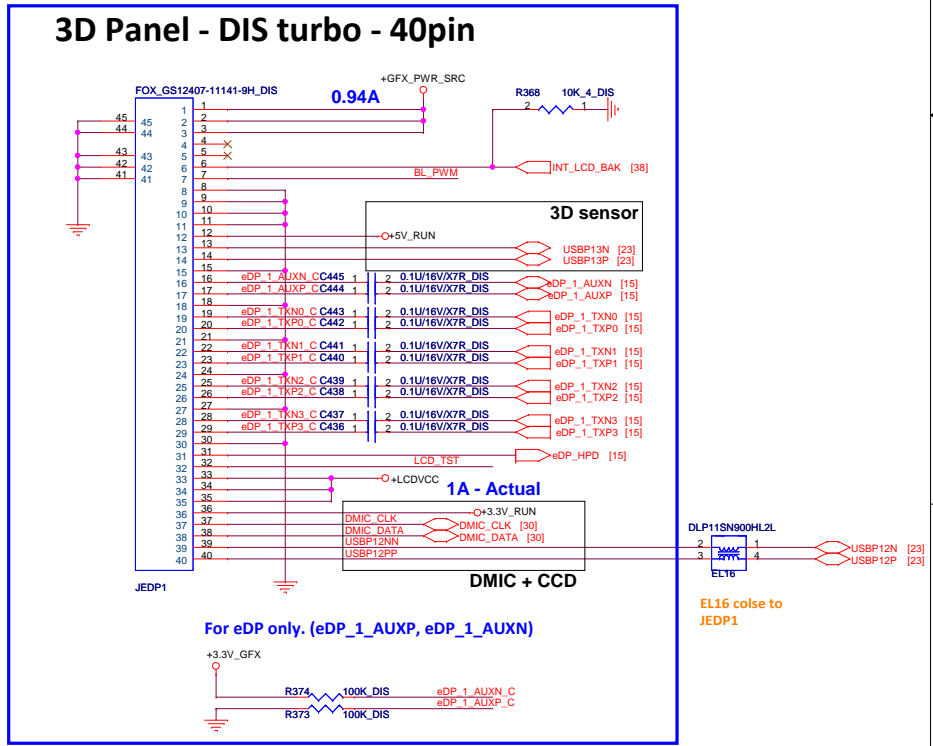
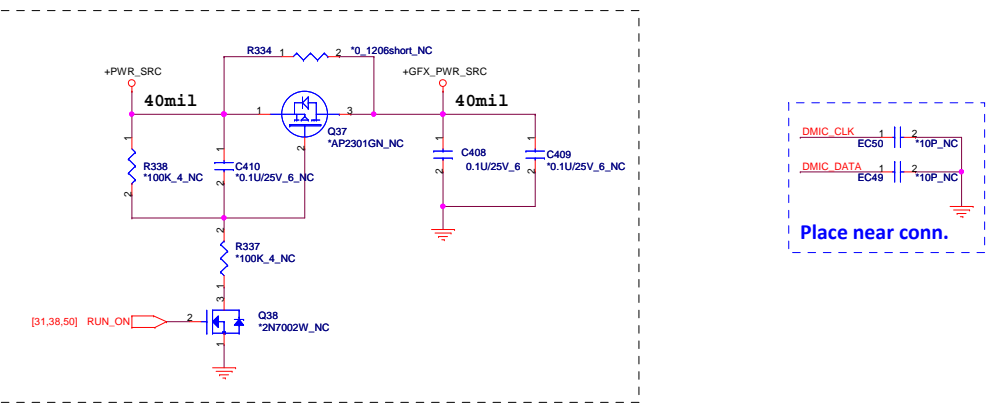
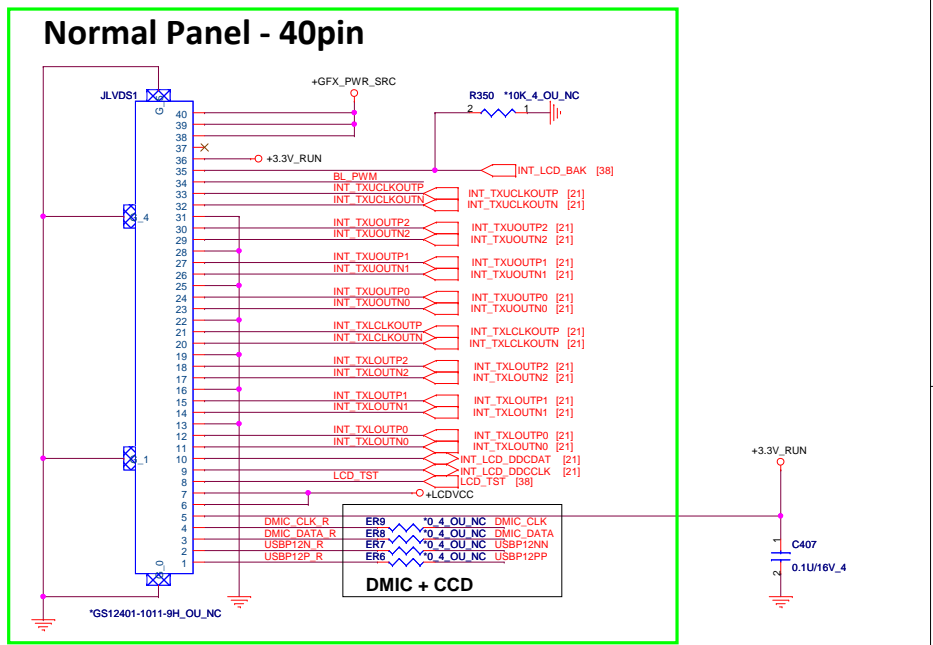
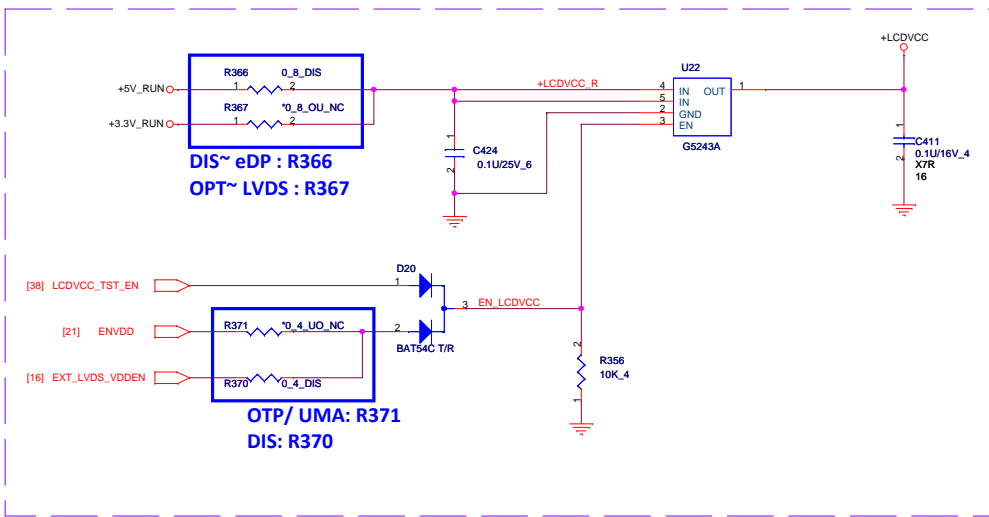
**Quanta Computer Inc.**  
PROJECT : R09A

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		3A

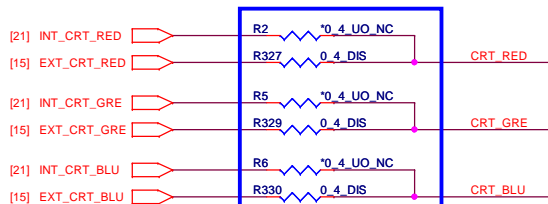
**Panther Point 6/7**

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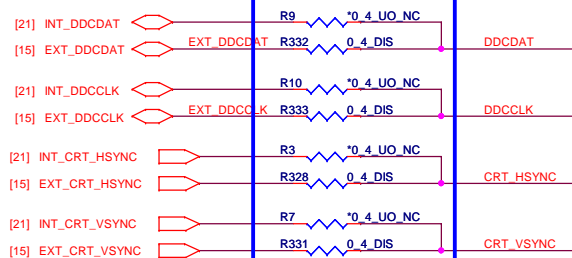




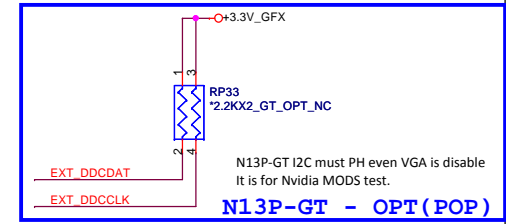
# VGA



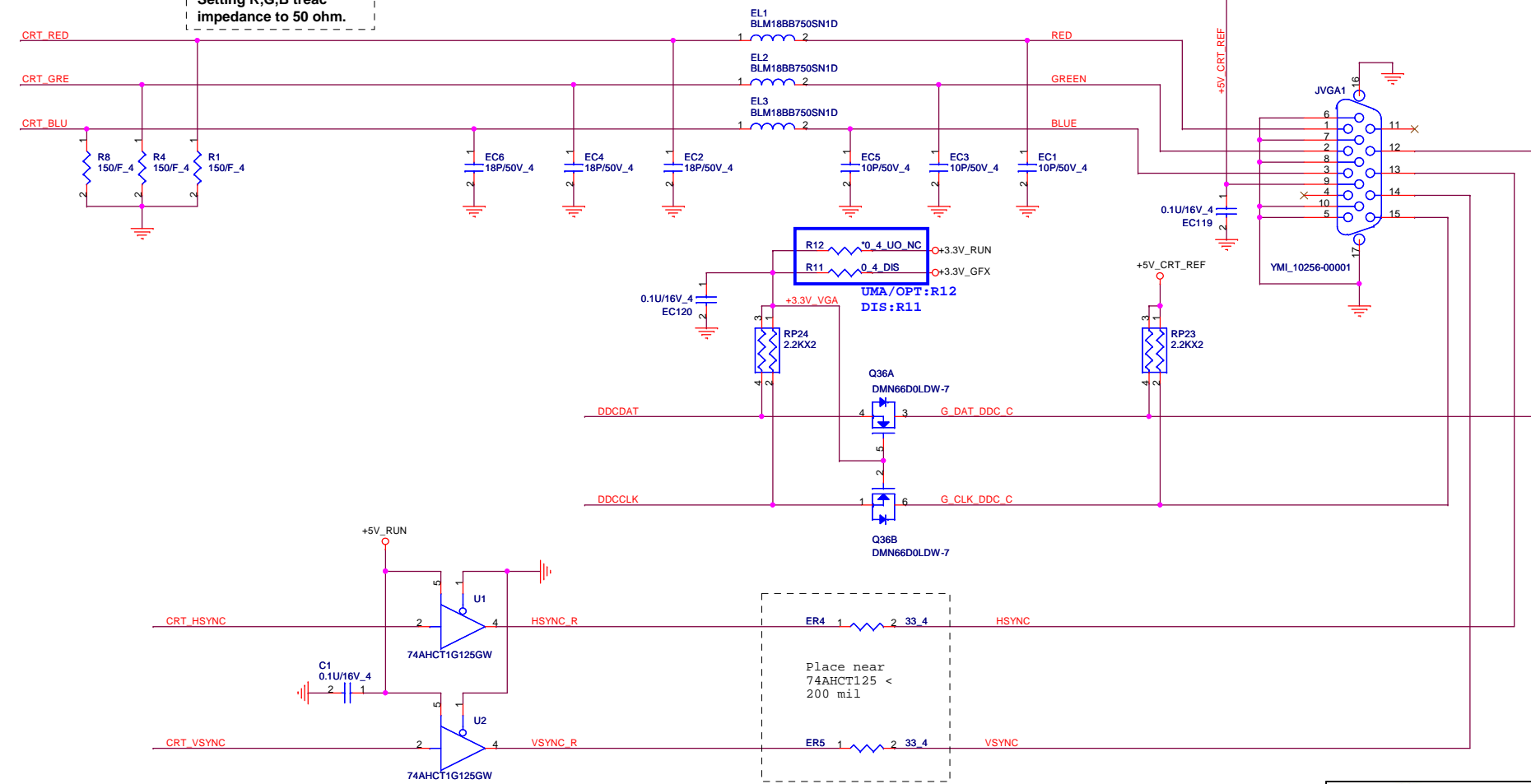
**DIS: EXT POP**  
**UMA/OPT: INT POP**



**DIS: EXT POP**  
**UMA/OPT: INT POP**



**Layout Note:**  
Setting R,G,B treac  
impedance to 50 ohm.



place near  
74AHCT125 <  
200 mil

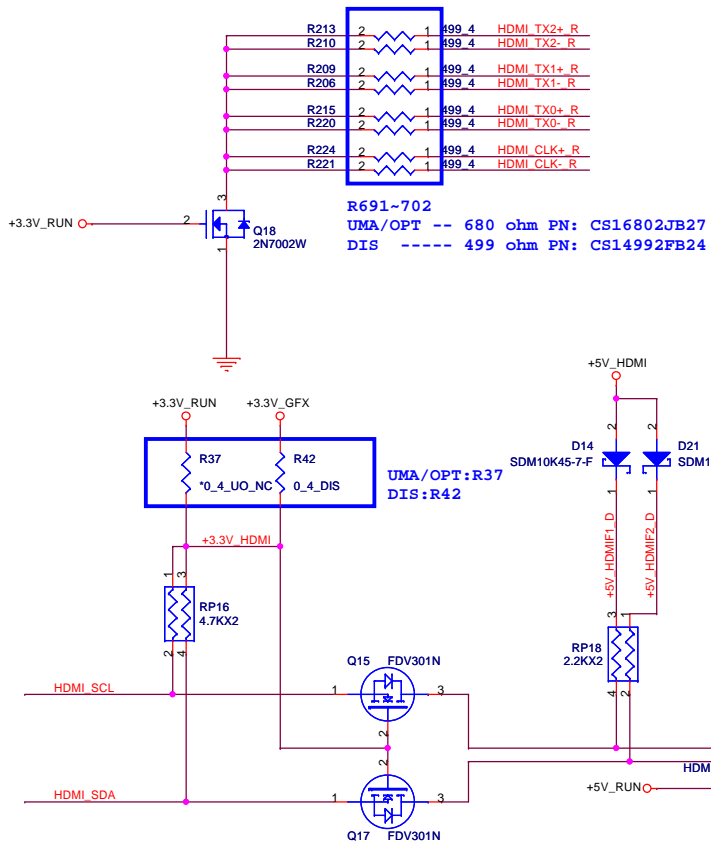
# HDMI W/O Re-driver

## DIS HDMI

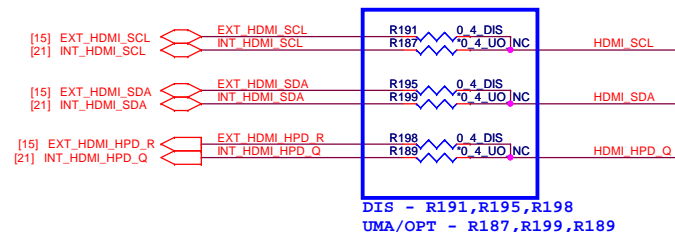
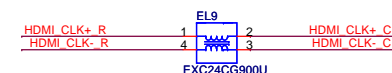
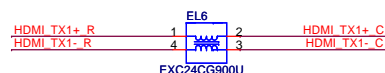
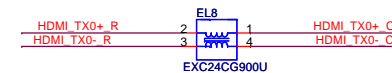
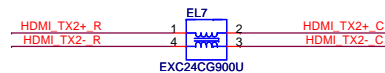
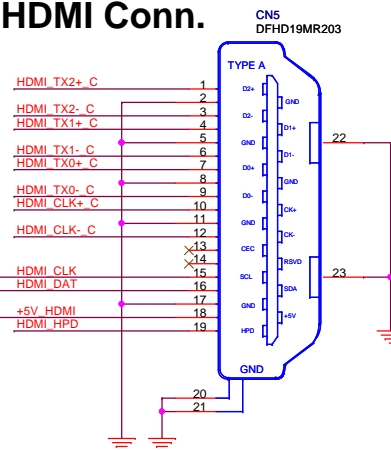
[15] EXT_HDMI_TXP2	EXT_HDMI_TXP2	C239	1	2	0.1U/16V 4 DIS	HDMI TX2+ R
[15] EXT_HDMI_TXN2	EXT_HDMI_TXN2	C237	1	2	0.1U/16V 4 DIS	HDMI TX2- R
[15] EXT_HDMI_TXP1	EXT_HDMI_TXP1	C236	1	2	0.1U/16V 4 DIS	HDMI TX1+ R
[15] EXT_HDMI_TXN1	EXT_HDMI_TXN1	C235	1	2	0.1U/16V 4 DIS	HDMI TX1- R
[15] EXT_HDMI_TXP0	EXT_HDMI_TXP0	C241	1	2	0.1U/16V 4 DIS	HDMI TX0+ R
[15] EXT_HDMI_TXN0	EXT_HDMI_TXN0	C244	1	2	0.1U/16V 4 DIS	HDMI TX0- R
[15] EXT_HDMI_TXCP	EXT_HDMI_TXCP	C250	1	2	0.1U/16V 4 DIS	HDMI CLK+ R
[15] EXT_HDMI_TXCN	EXT_HDMI_TXCN	C247	1	2	0.1U/16V 4 DIS	HDMI CLK- R

## OTP/UMA HDMI

[21] INT_HDMI_TXP2_C	INT_HDMI_TXP2_C	C240	1	2	*0.1U/16V 4 UO_NC	HDMI TX2+ R
[21] INT_HDMI_TXN2_C	INT_HDMI_TXN2_C	C238	1	2	*0.1U/16V 4 UO_NC	HDMI TX2- R
[21] INT_HDMI_TXP1_C	INT_HDMI_TXP1_C	C232	1	2	*0.1U/16V 4 UO_NC	HDMI TX1+ R
[21] INT_HDMI_TXN1_C	INT_HDMI_TXN1_C	C226	1	2	*0.1U/16V 4 UO_NC	HDMI TX1- R
[21] INT_HDMI_TXP0_C	INT_HDMI_TXP0_C	C242	1	2	*0.1U/16V 4 UO_NC	HDMI TX0+ R
[21] INT_HDMI_TXN0_C	INT_HDMI_TXN0_C	C246	1	2	*0.1U/16V 4 UO_NC	HDMI TX0- R
[21] INT_HDMI_TXCP_C	INT_HDMI_TXCP_C	C252	1	2	*0.1U/16V 4 UO_NC	HDMI CLK+ R
[21] INT_HDMI_TXCN_C	INT_HDMI_TXCN_C	C249	1	2	*0.1U/16V 4 UO_NC	HDMI CLK- R

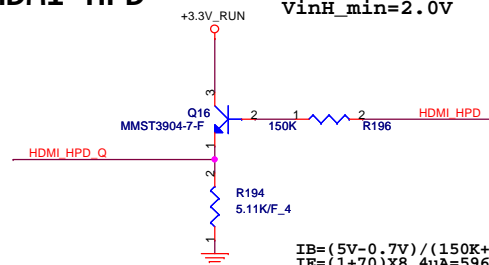


## HDMI Conn.



## HDMI HPD

HDMI\_HPDP spec  
VinH\_min=2.0V



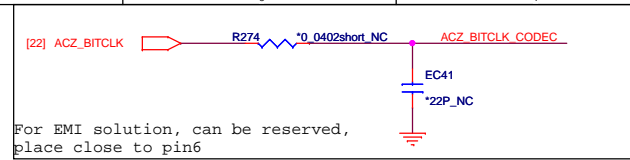
$$I_B = (5V - 0.7V) / (150K + (70+1)5.1K) = 8.4\mu A$$

$$I_E = (1+70) \times 8.4\mu A = 596.4\mu A$$

$$V_E = 596.4\mu A \times 5.1K = 3.04V$$

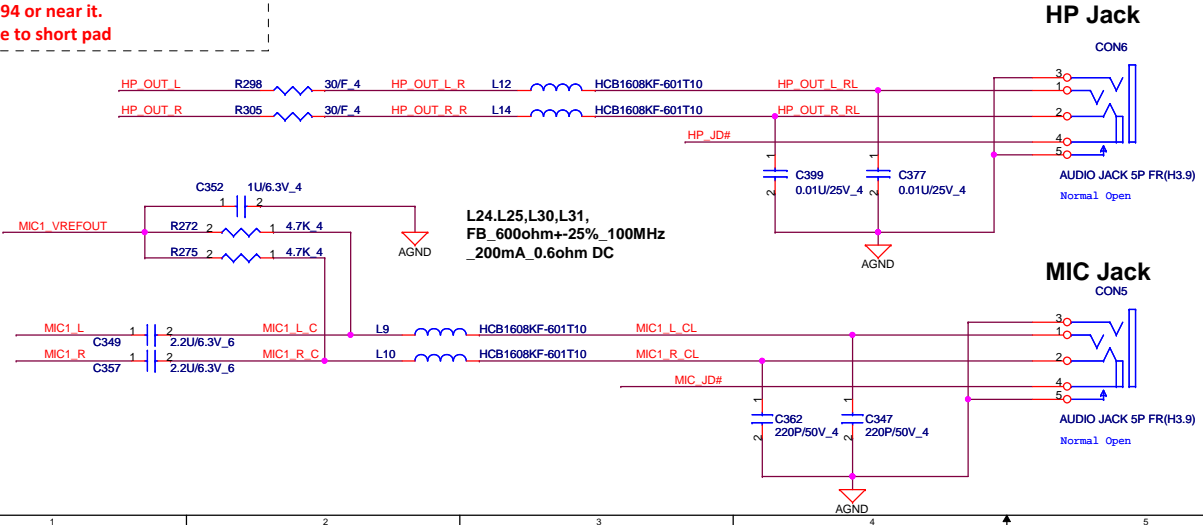
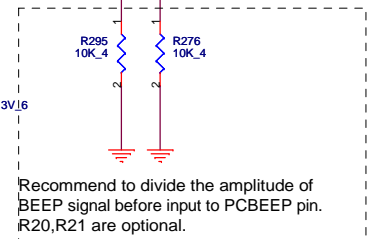
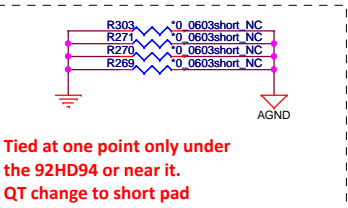
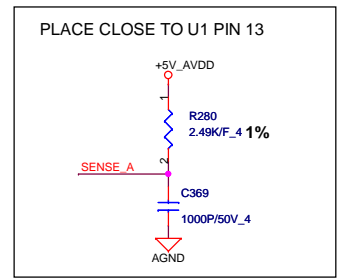
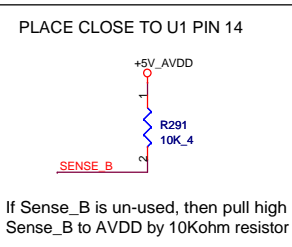
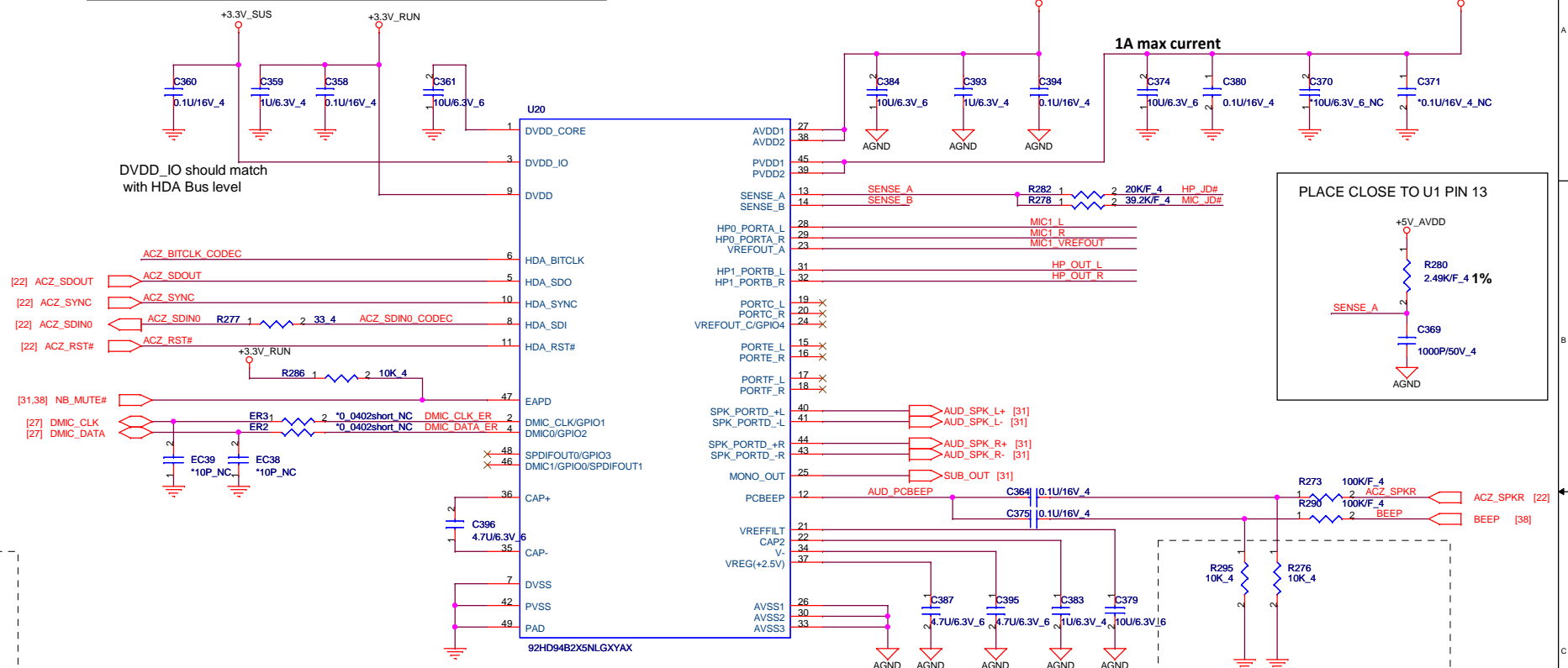
$$B = 70$$

# CODEC

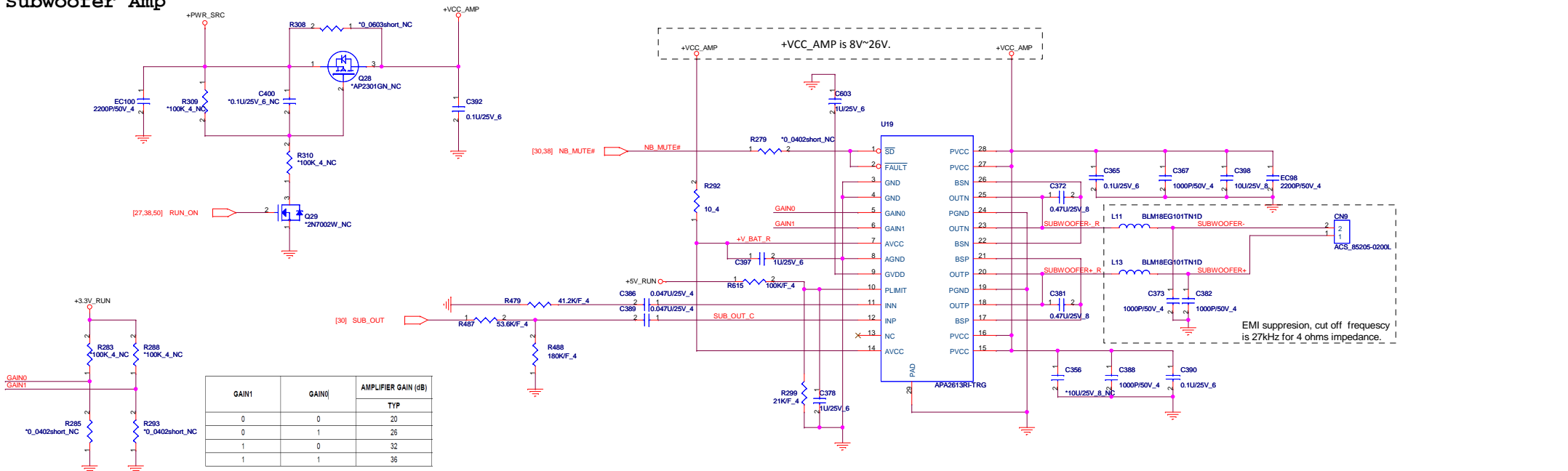


For EMI solution, can be reserved, place close to pin6

Notes:  
Keep PVDD supply and speaker traces routed on the DGND plane.  
Keep away from AGND and other analog signals



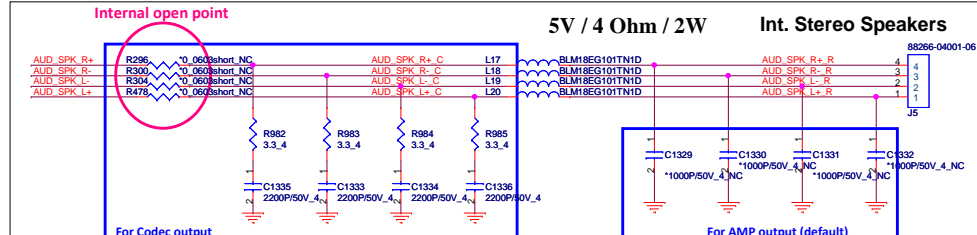
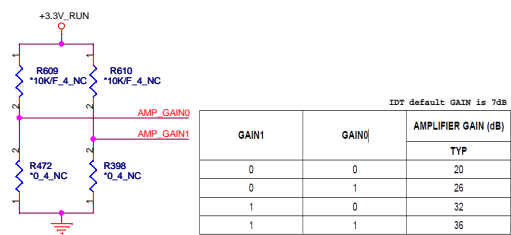
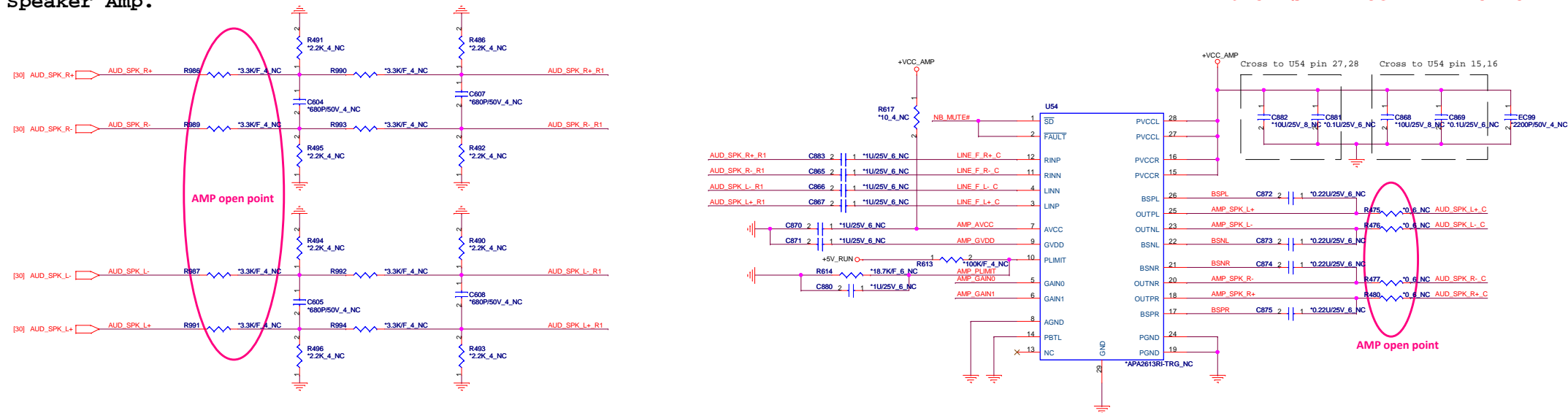
# Subwoofer Amp



# Speaker Amp.

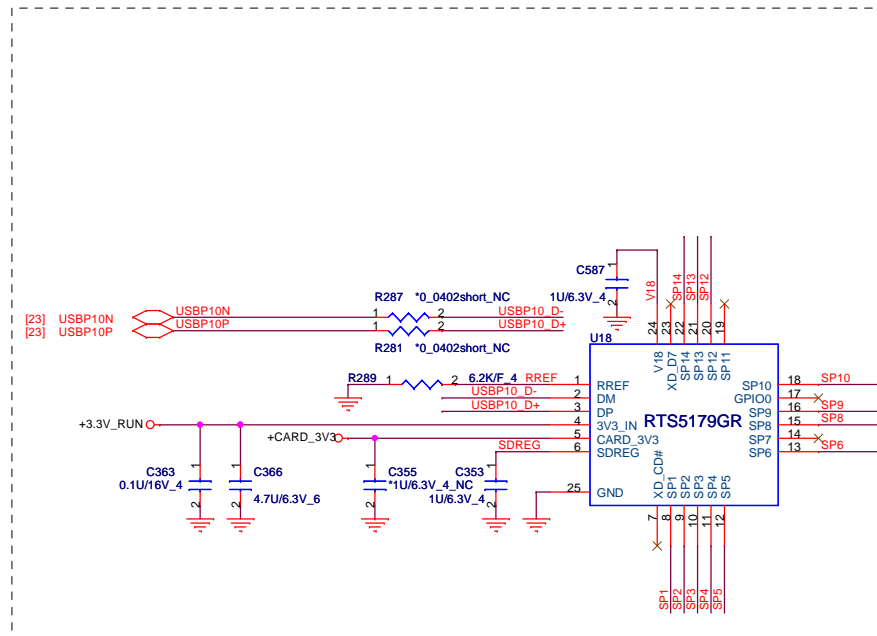
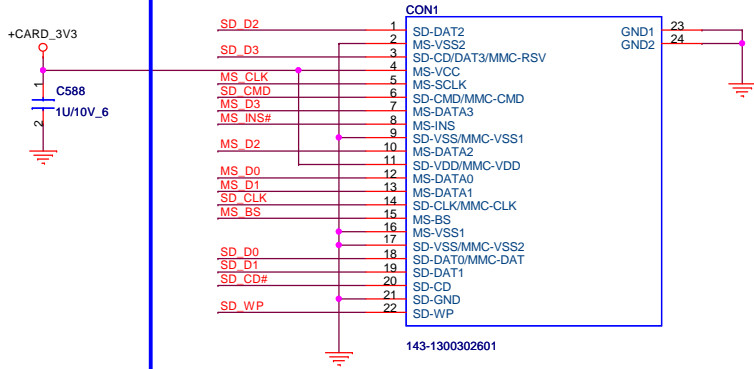
R491,R495,R494,R496 default NC

APA2613 is P2P to TI TPA3113

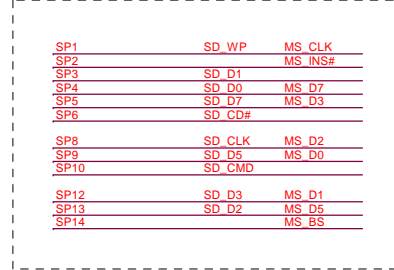
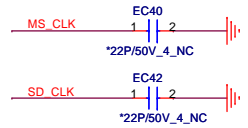
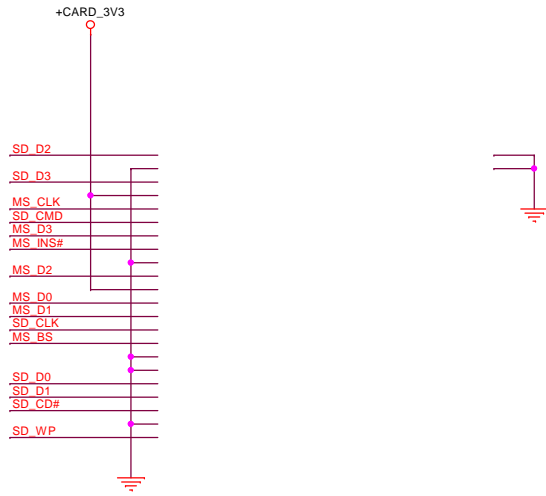


# Cardreader (RTS5179GR) Support SD3.0 USH50

For INSPIRON Placement (R09,R09A,R09T)



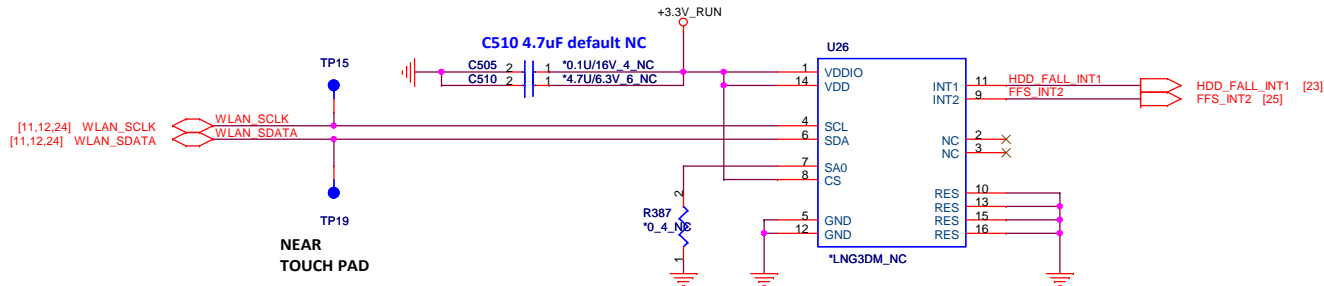
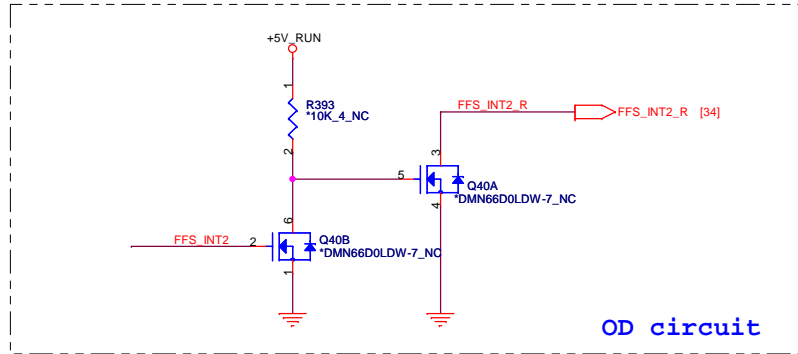
NA



Share Pin



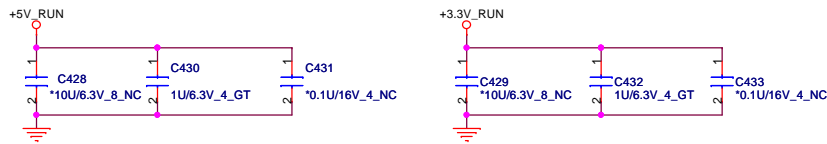
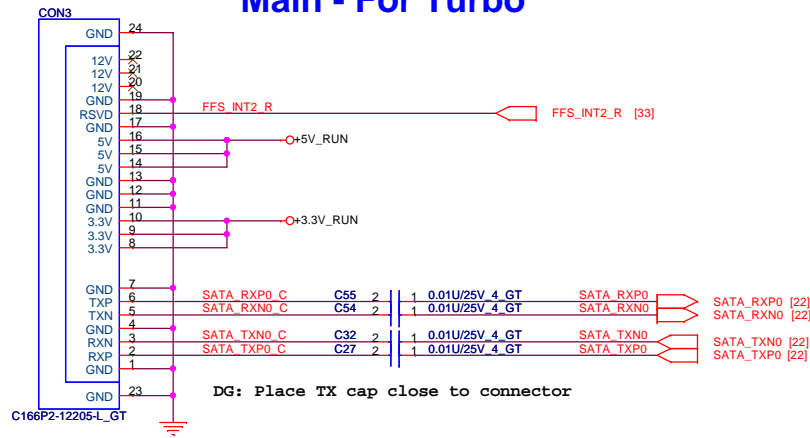
# 3-axis Fall Sensor - NC



SA0 is low: I2C device address is 00110000 (30h)  
 SA0 is high: I2C device address is 00110010 (32h)

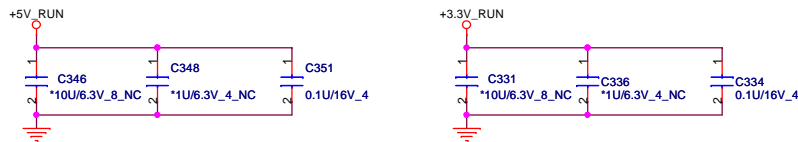
# HDDX2

## Main - For Turbo

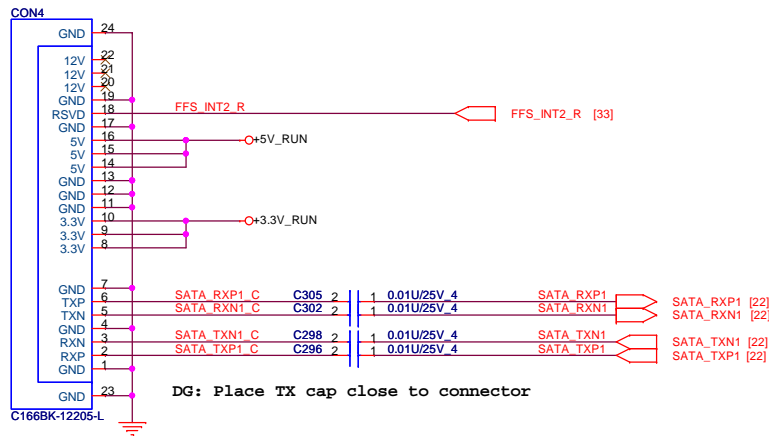


Default C351, C430 POP

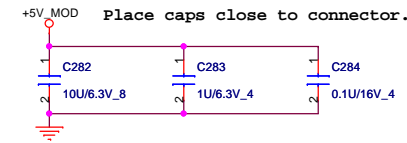
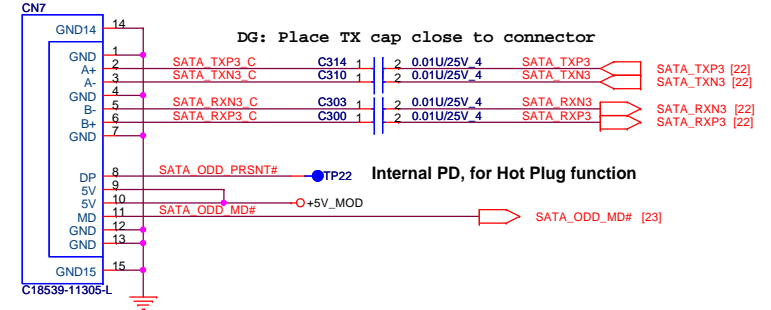
Default C334, C432 POP



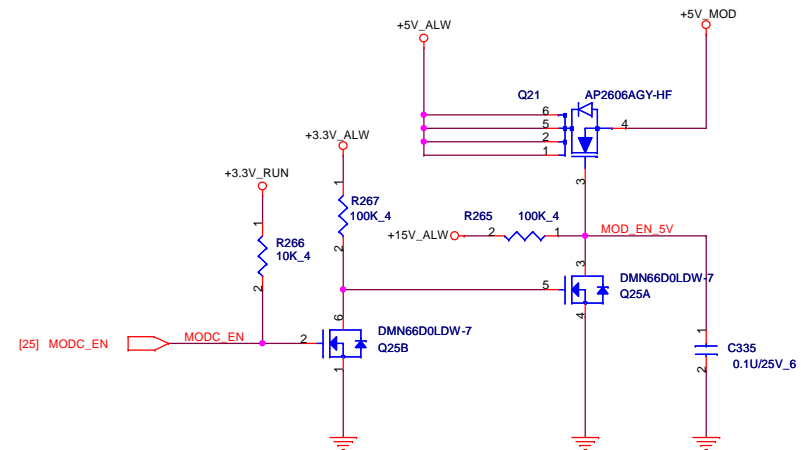
## Second - For Inspiron



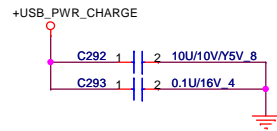
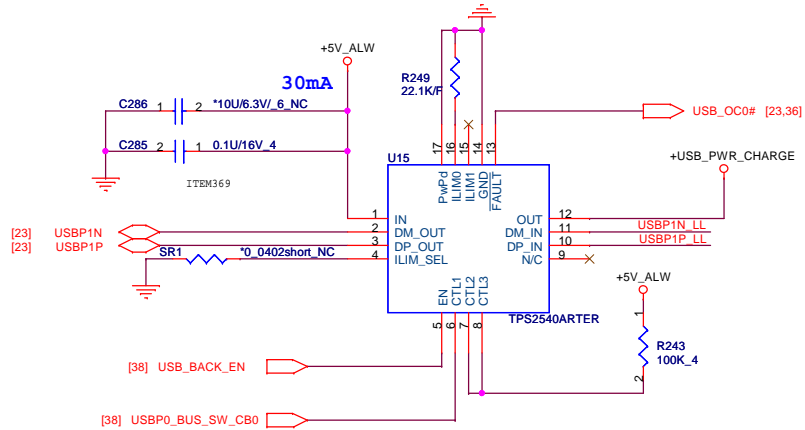
# ODD



## Support Zero power ODD

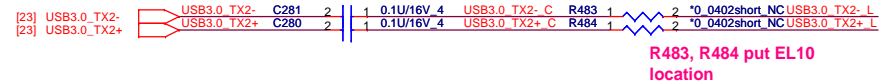
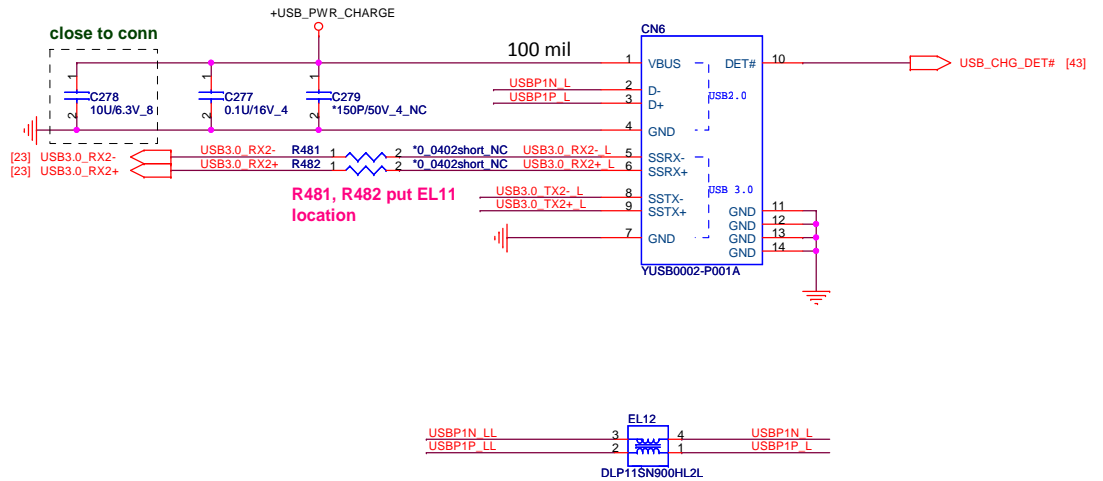


# USB3.0x1 with Power share

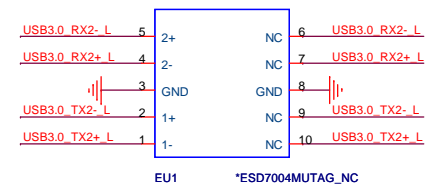


	R249	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

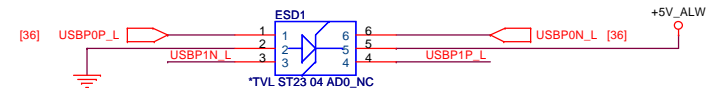
USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A



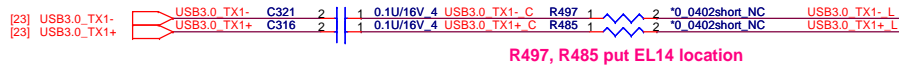
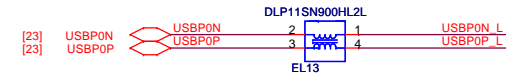
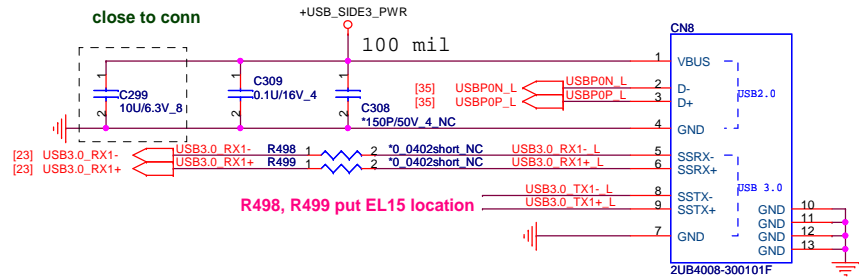
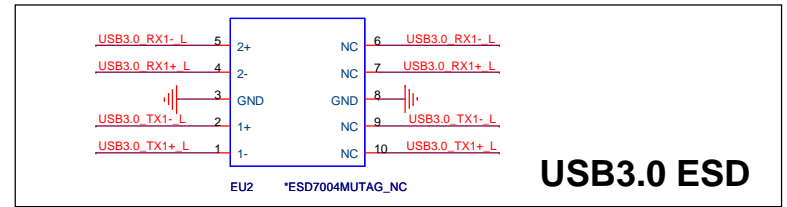
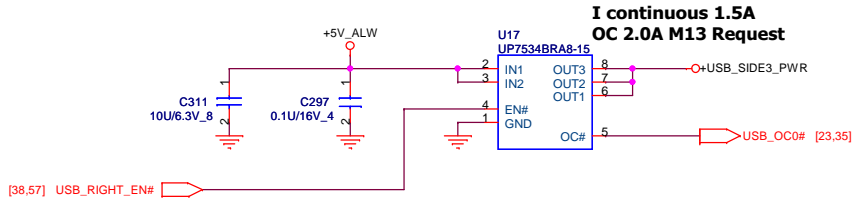
## USB 3.0 ESD

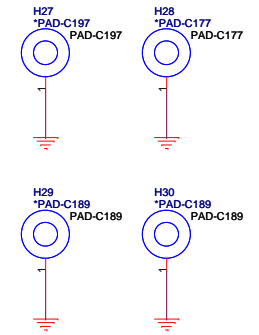
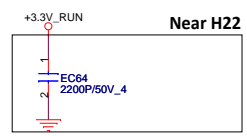
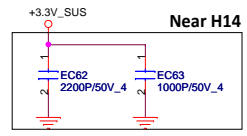
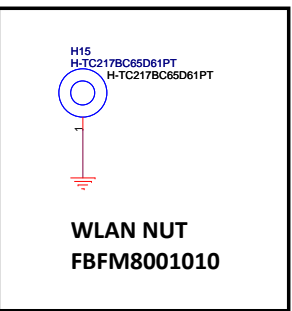
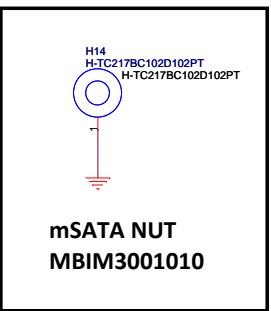
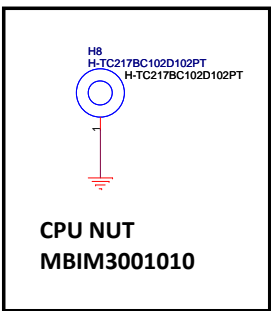
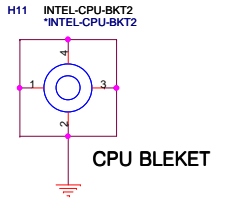
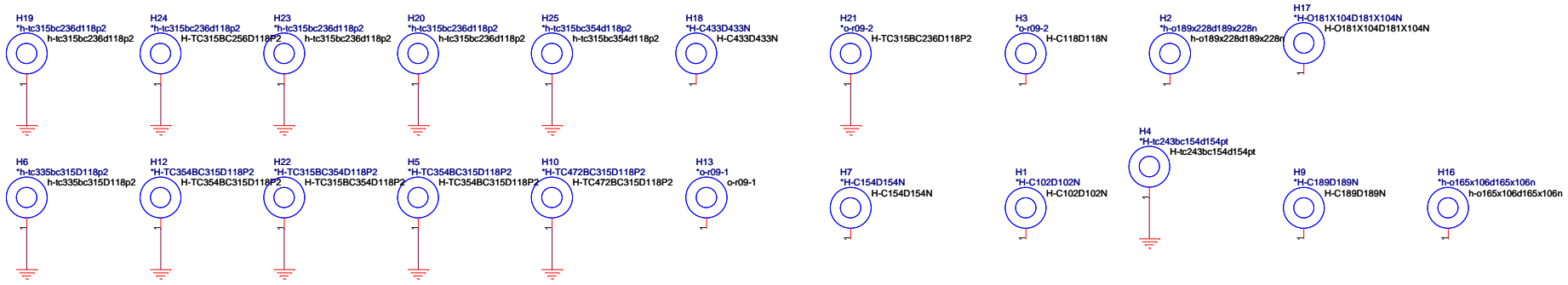


## USB 2.0 ESD

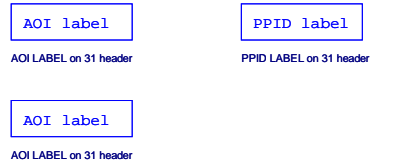
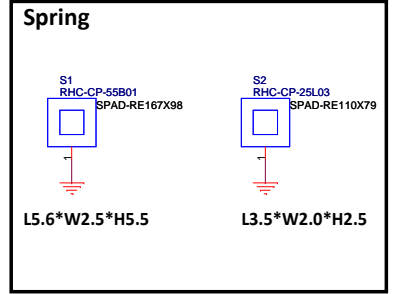
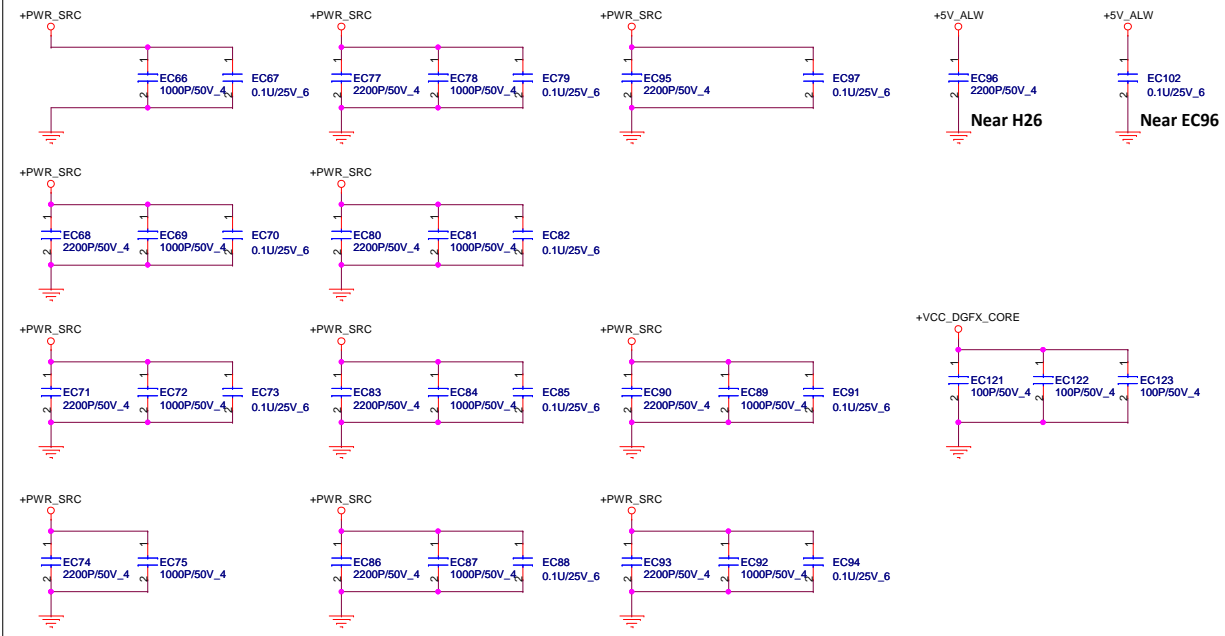


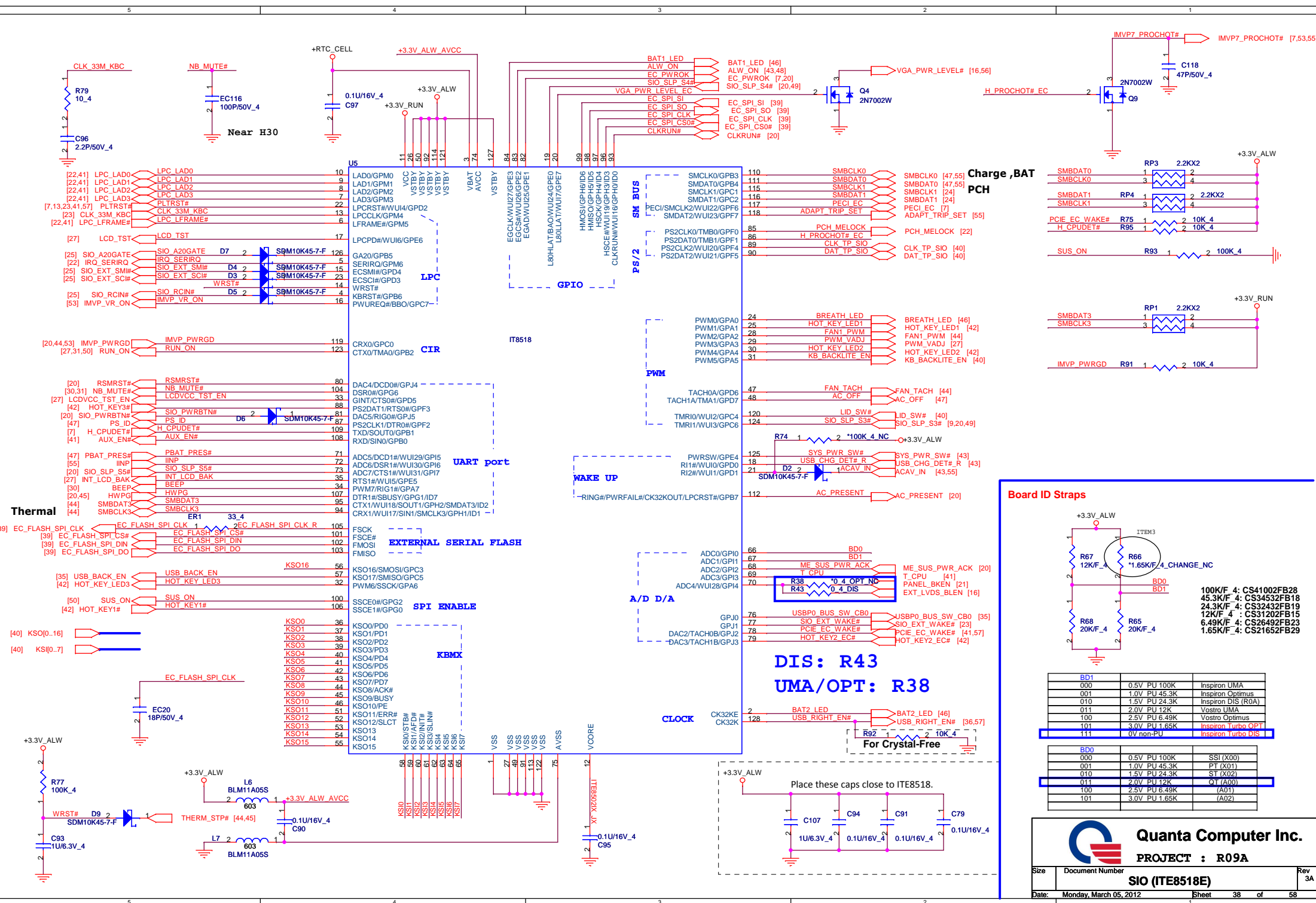
# USB3.0x1





**Near**  
C423/ESD2/H8/PR204/PR235/pq20/PL5/PC121/H10/R334/PL7/EC45






### Board ID Straps

BD1	0.5V PU 100K	Inspiron UMA
000	1.0V PU 45.3K	Inspiron Optimus
010	1.5V PU 24.3K	Inspiron DIS (ROA)
011	2.0V PU 12K	Vostro UMA
100	2.5V PU 6.49K	Vostro Optimus
101	3.0V PU 1.65K	Inspiron Turbo OPT
111	0V non-PU	Inspiron Turbo DIS

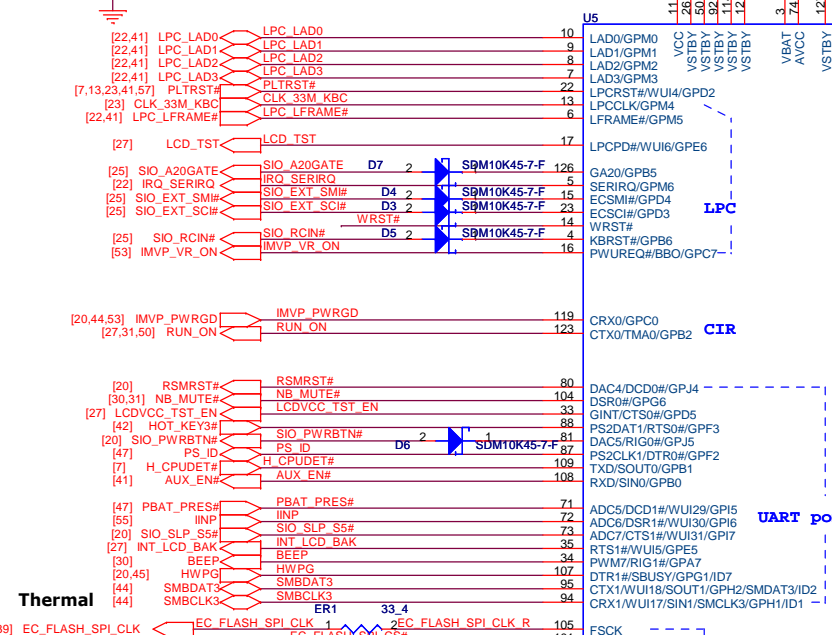
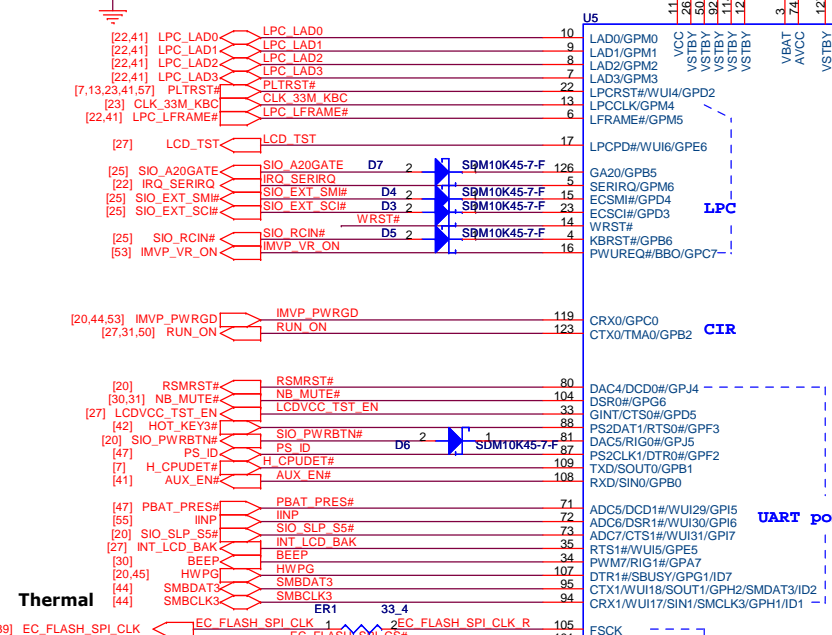
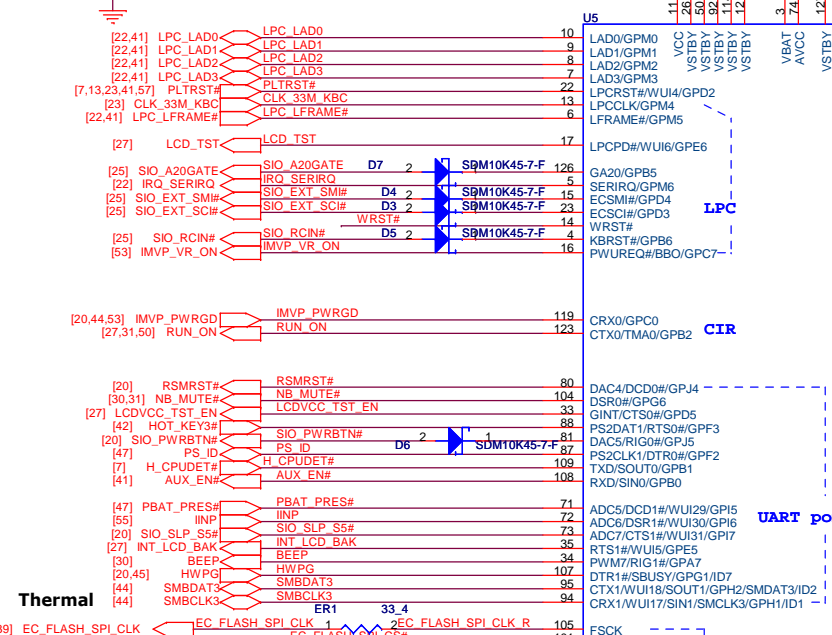
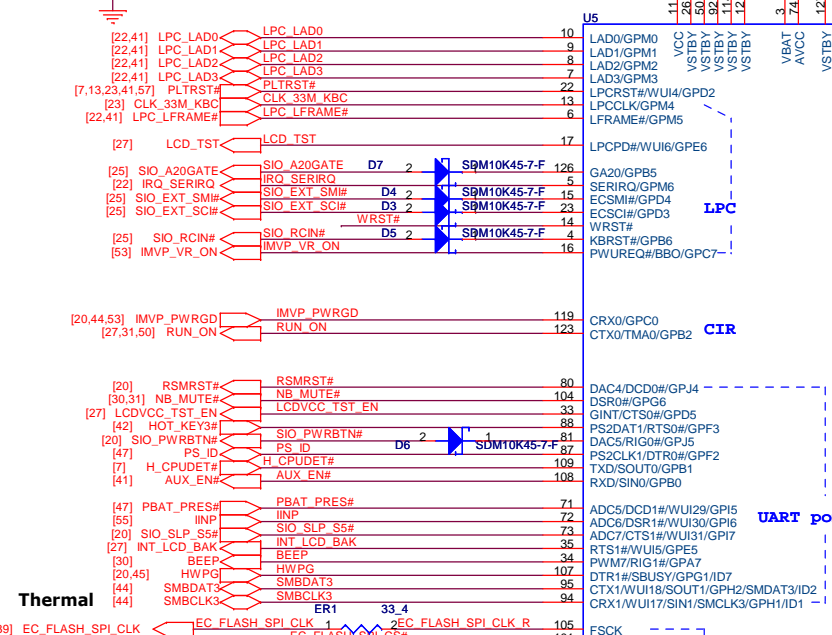
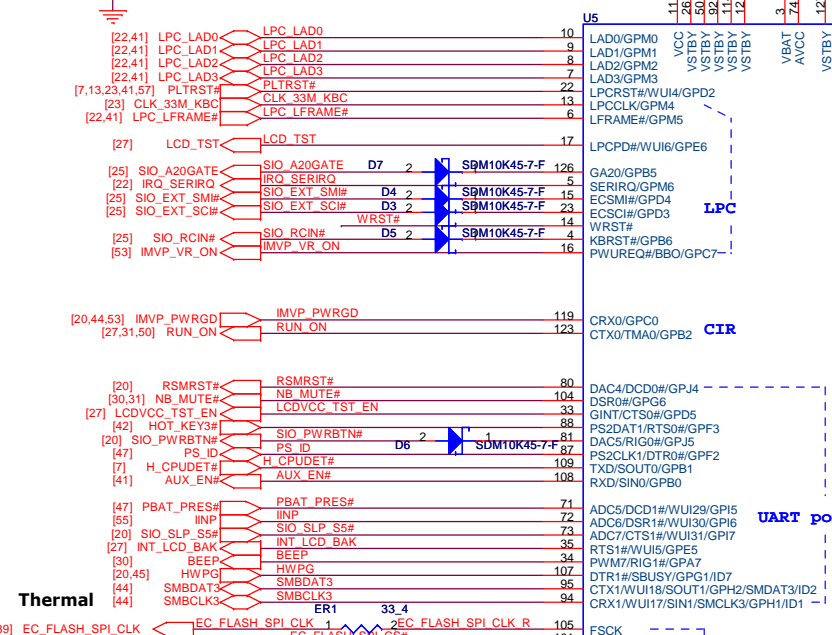
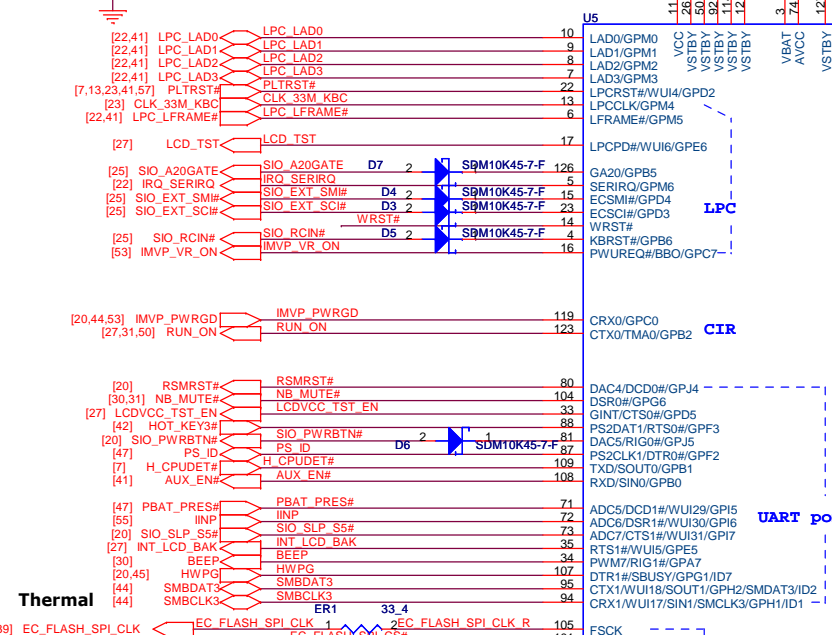
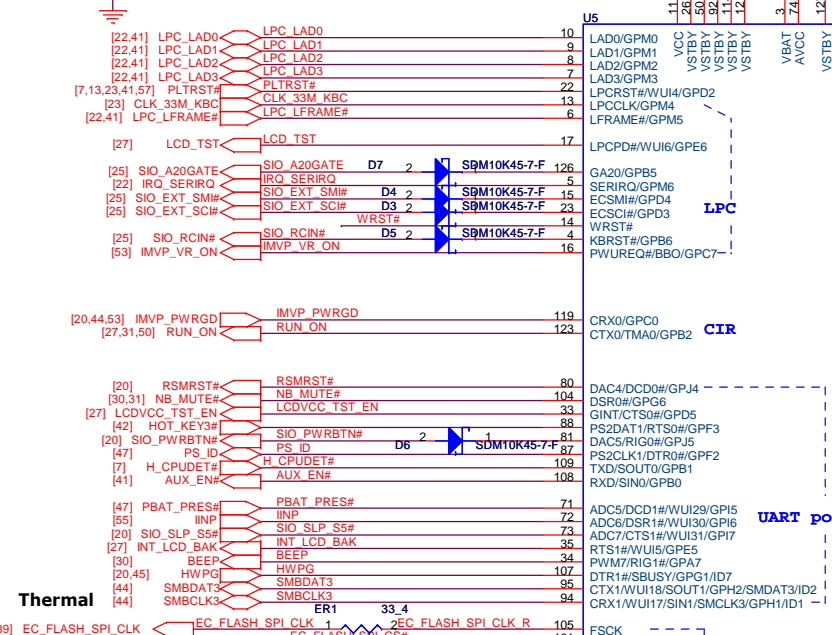
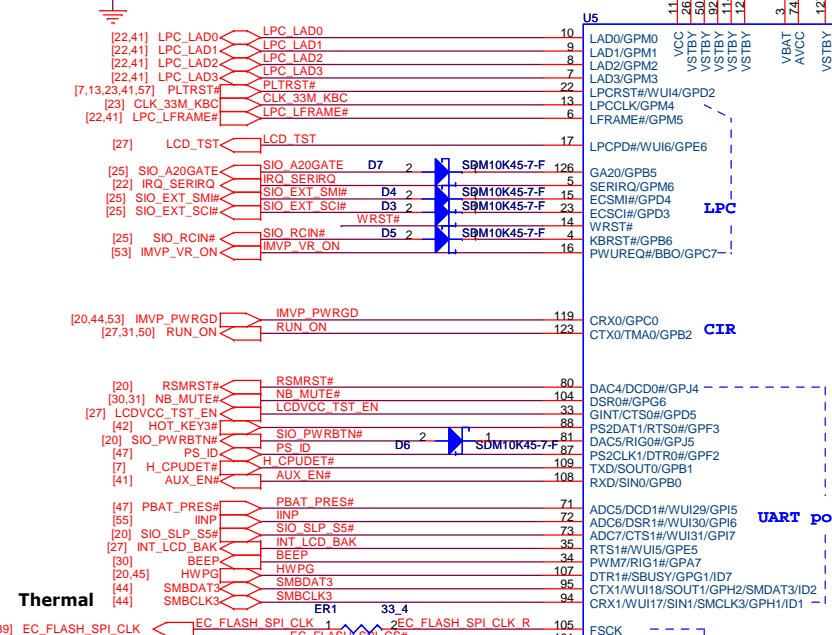
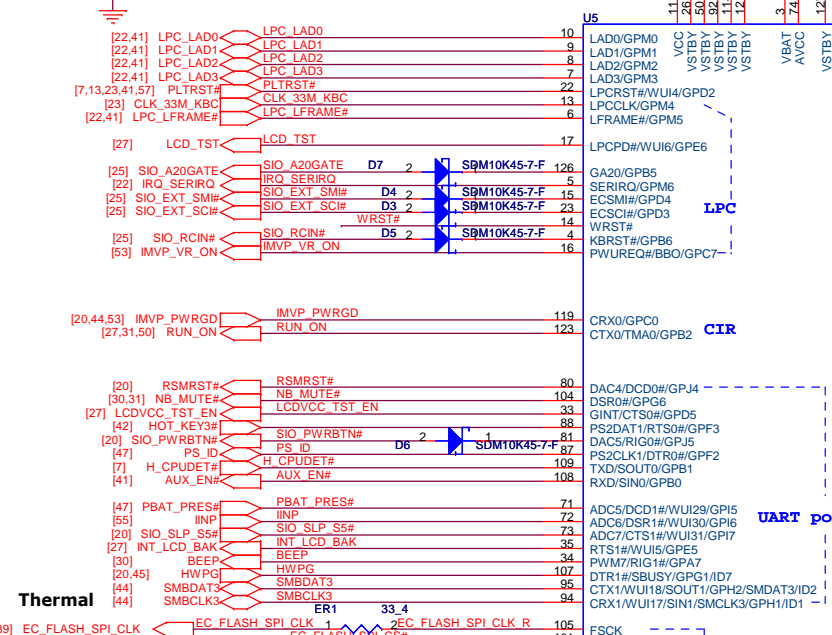
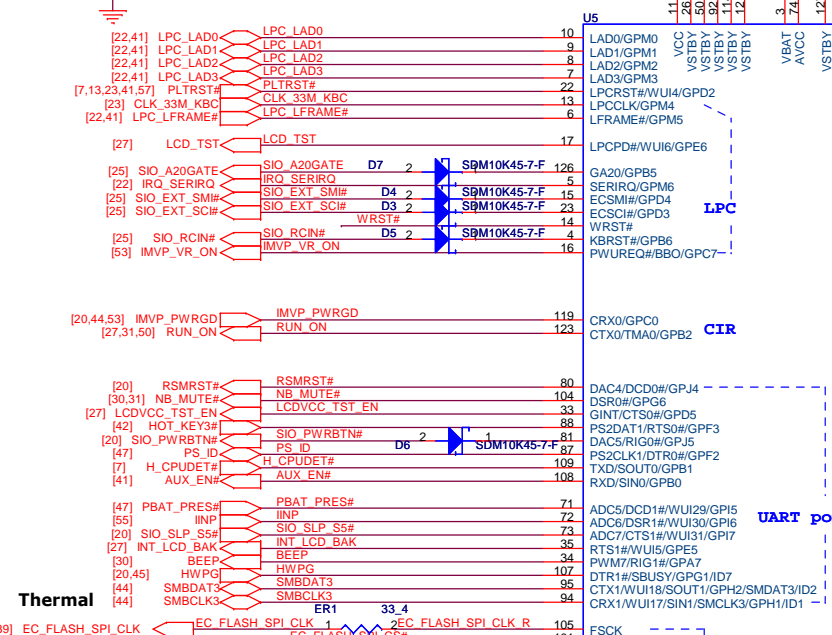
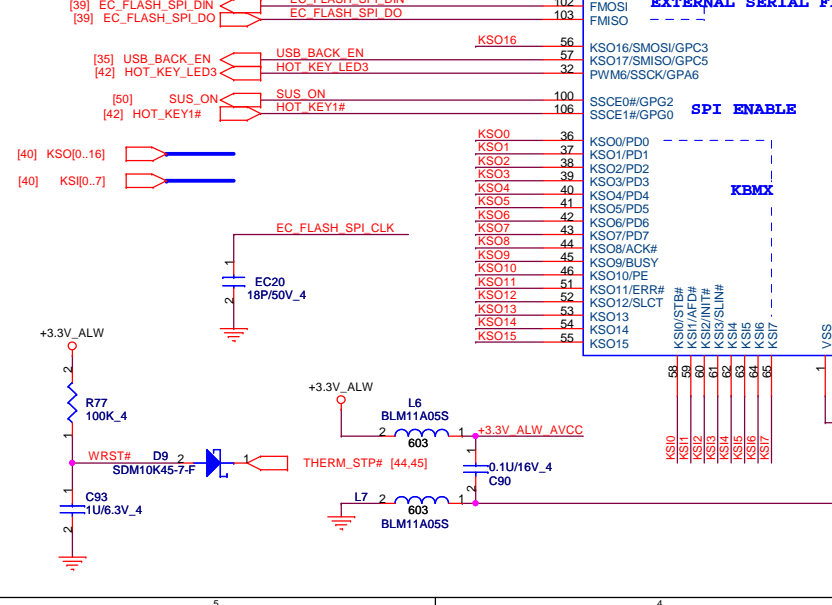
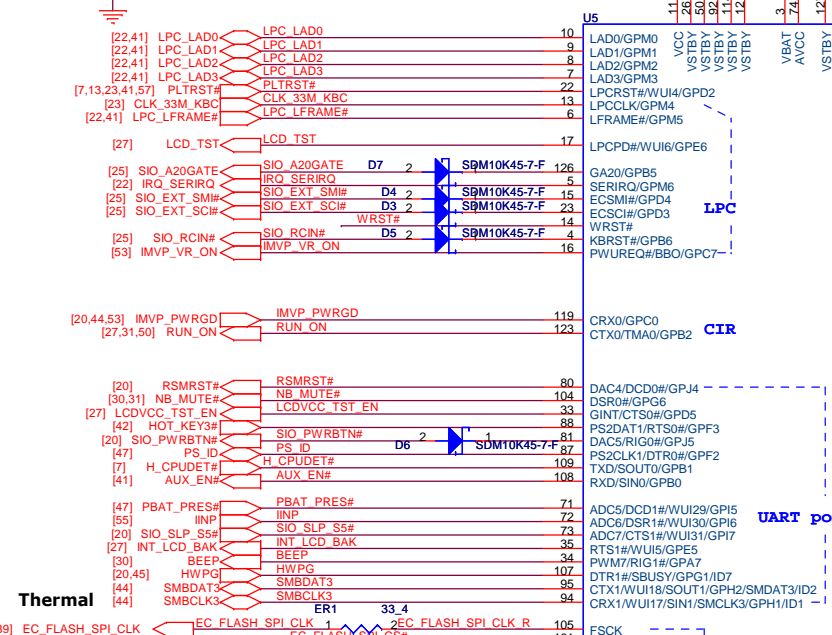
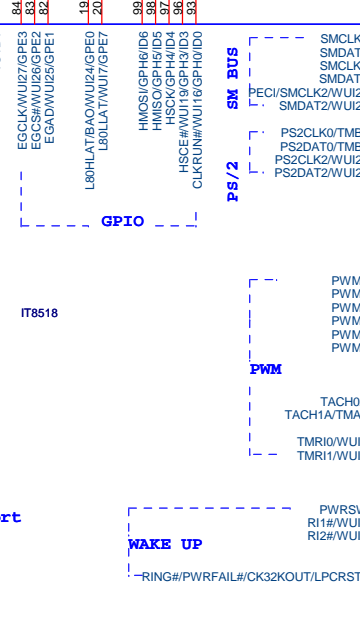
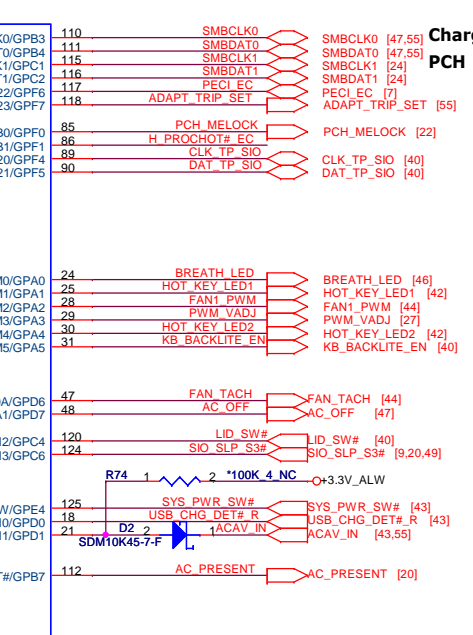
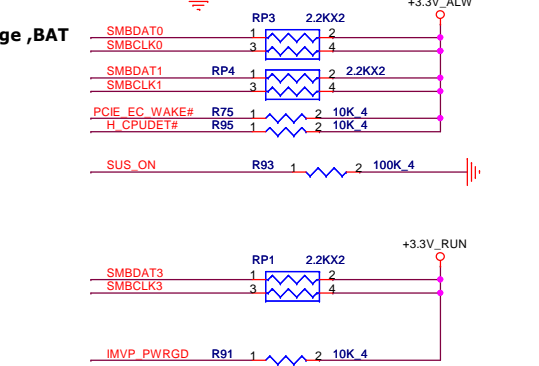
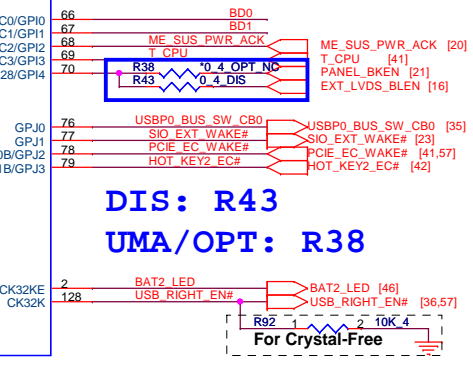
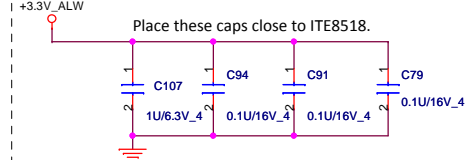
B00	0.5V PU 100K	SSI (X00)
001	1.0V PU 45.3K	PT (X01)
010	1.5V PU 24.3K	ST (X02)
011	2.0V PU 12K	QT (A00)
100	2.5V PU 6.49K	A01
101	3.0V PU 1.65K	A02



## Quanta Computer Inc.

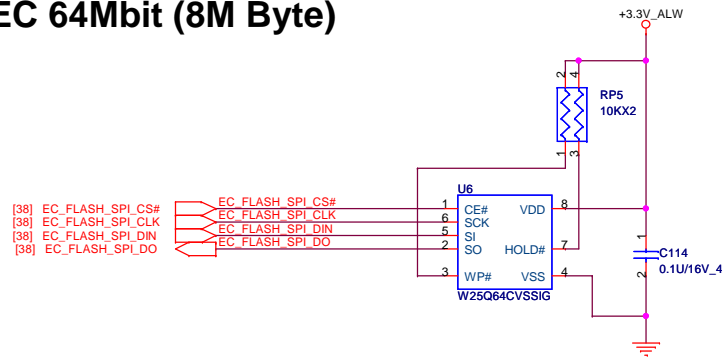
**PROJECT : R09A**

Size	Document Number	Rev
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Date:	Monday, March 05, 2012	Sheet 38 of 58

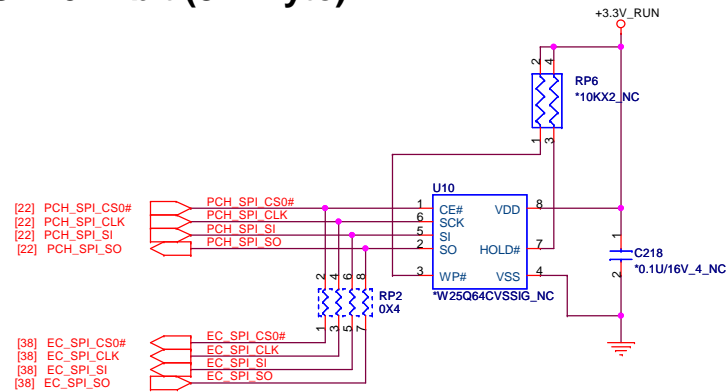


# FLASH / RTC

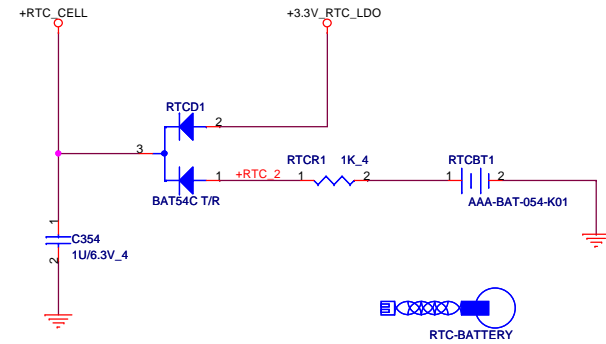
## For EC 64Mbit (8M Byte)



## For PCH 64Mbit (8M Byte)

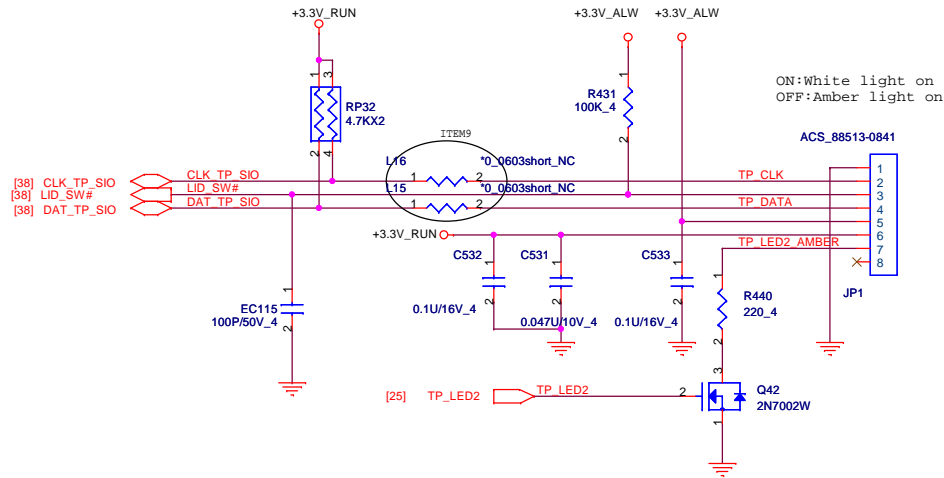


## RTC

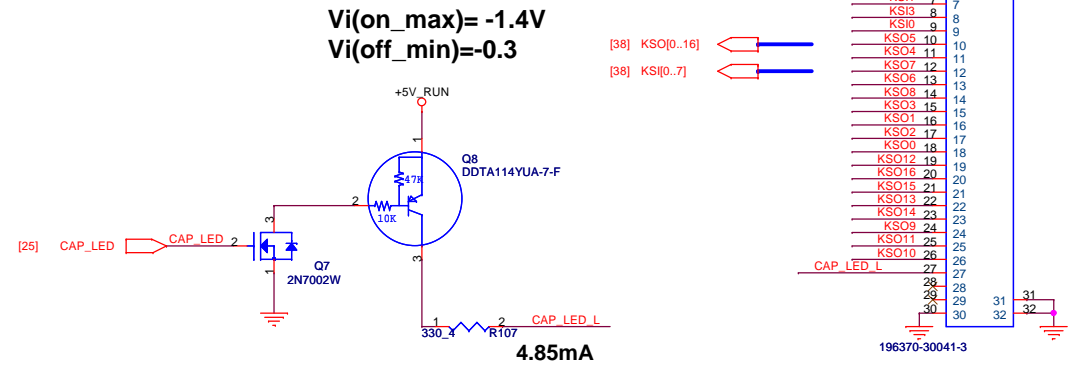


Double, 25°C, Vf=0.4V, If=25mA  
 one, 25°C, Vf=0.35V, If=15.8mA

# Touch Pad CONNECTOR

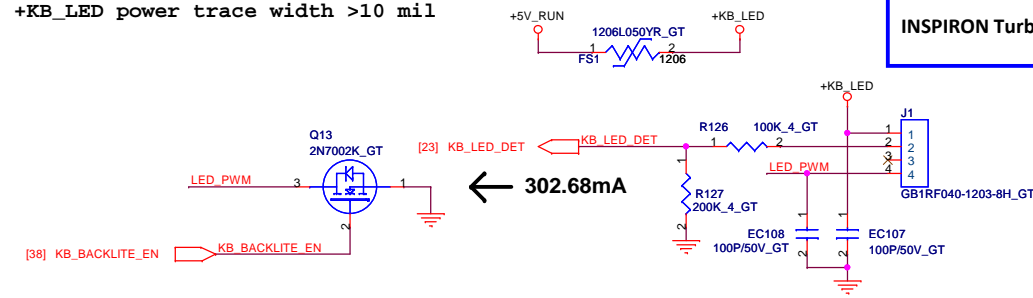


# KEYBOARD CONNECTOR

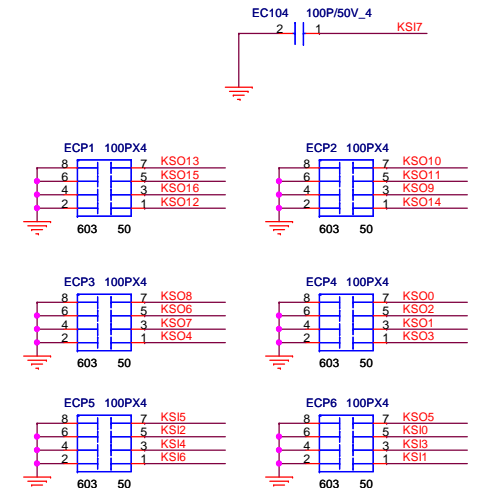


# Key board illumination

+KB\_LED power trace width >10 mil



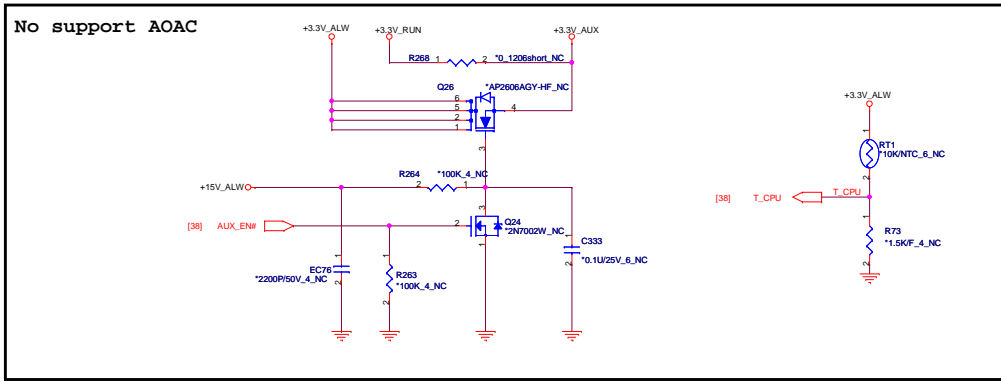
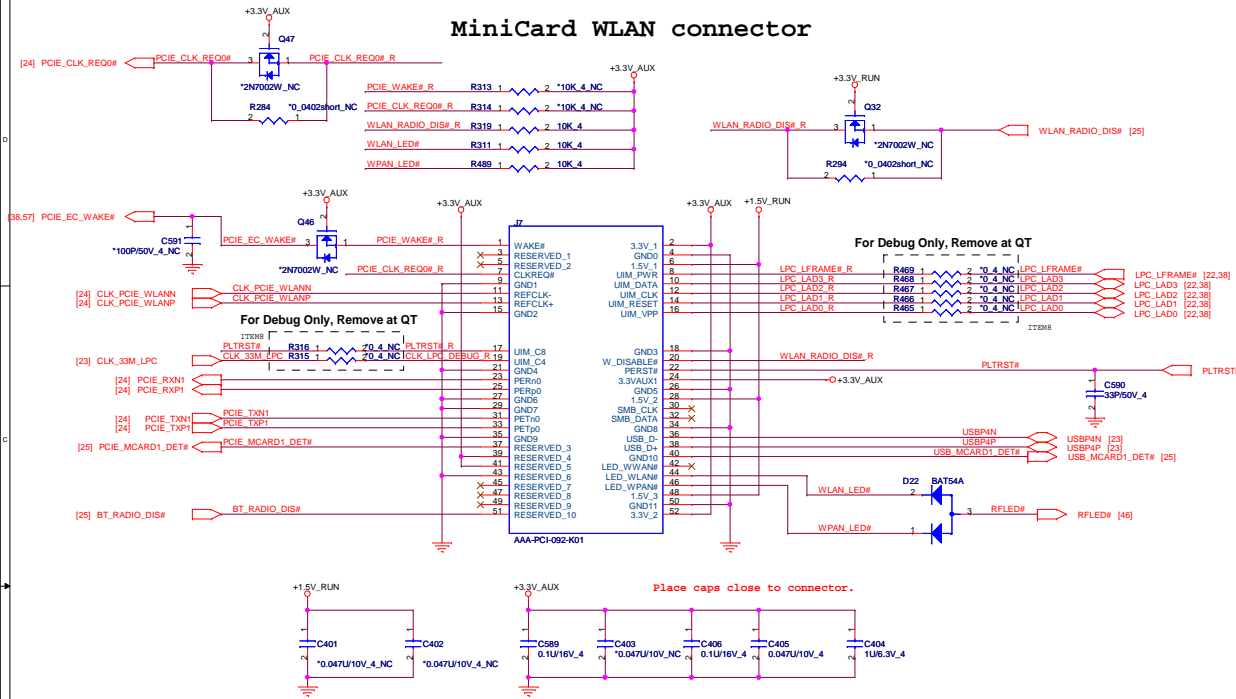
INSPIRON	NC
INSPIRON Turbo	POP



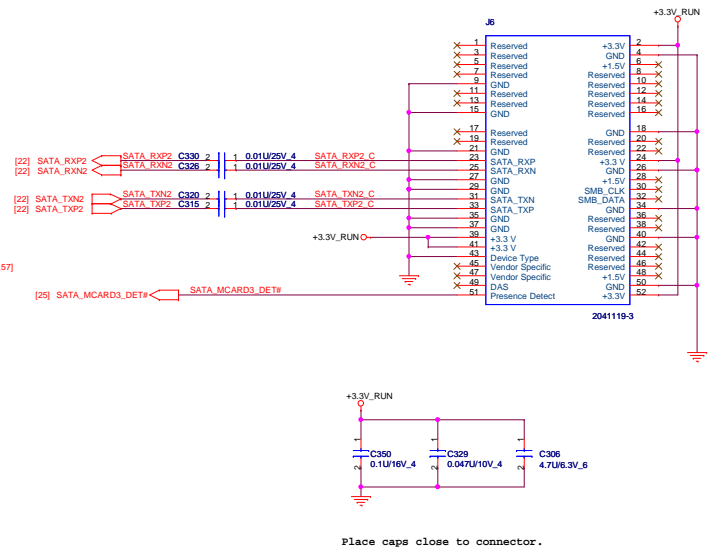
Layout Note: 100P CAPS CLOSE TO JKB1



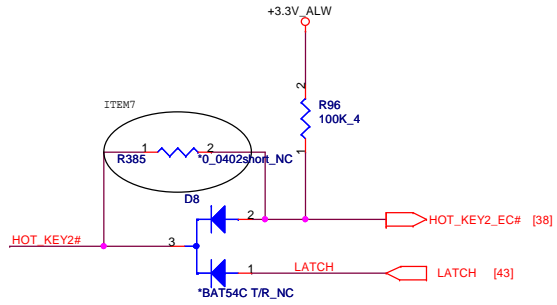
## MiniCard WLAN connector



## MiniCard mSATA connector

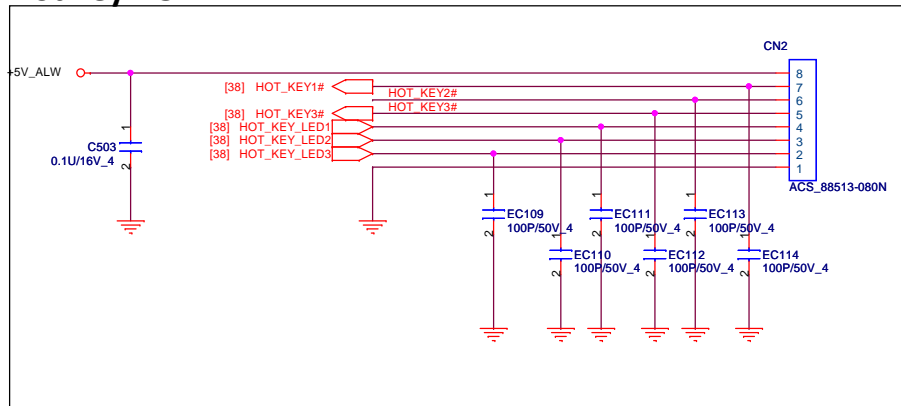


# HOT\_KEY2 support Pre-Boot Recovery



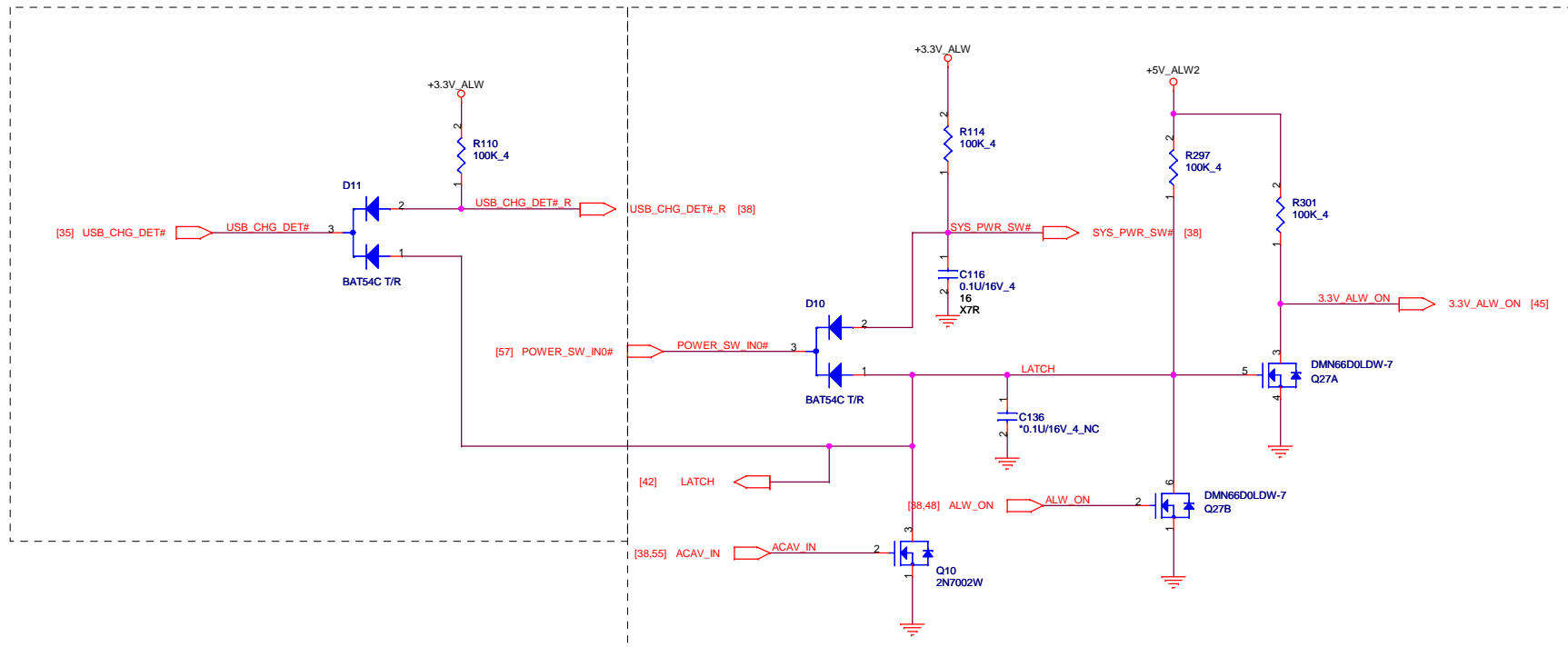
INSPIRON: R385 pop, D8 NC

# Hot key BOARD

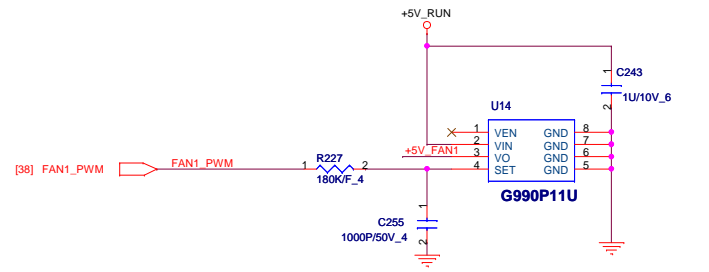
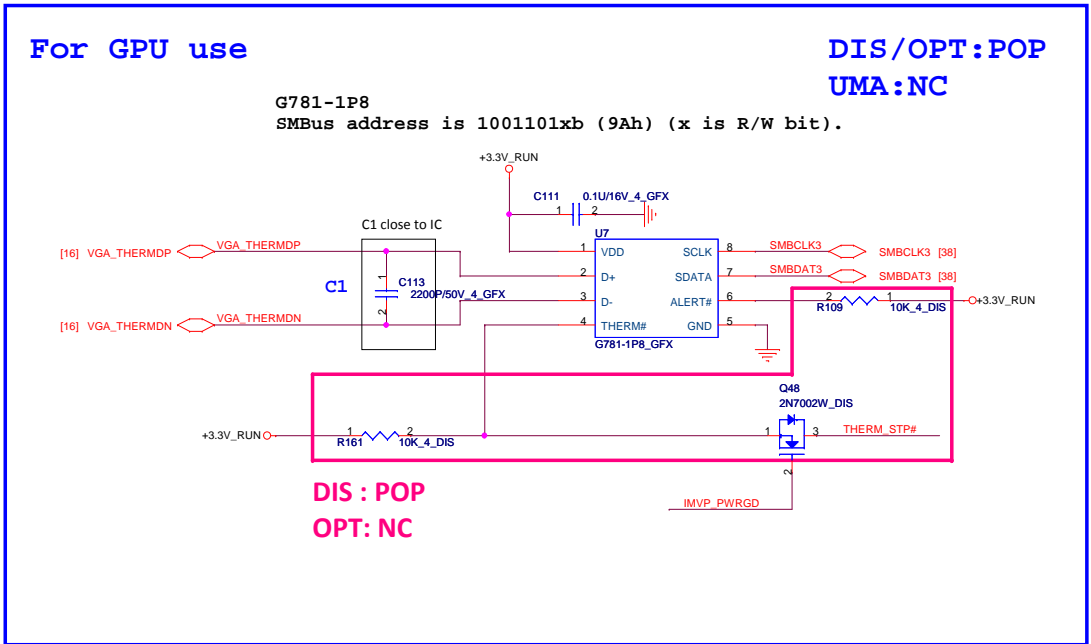


For USB charger usage

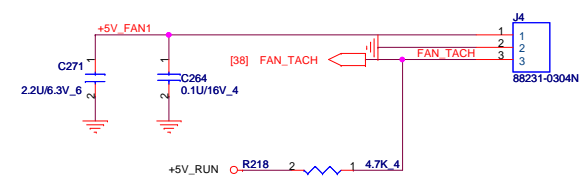
3V ALW ON POWER LOGIC



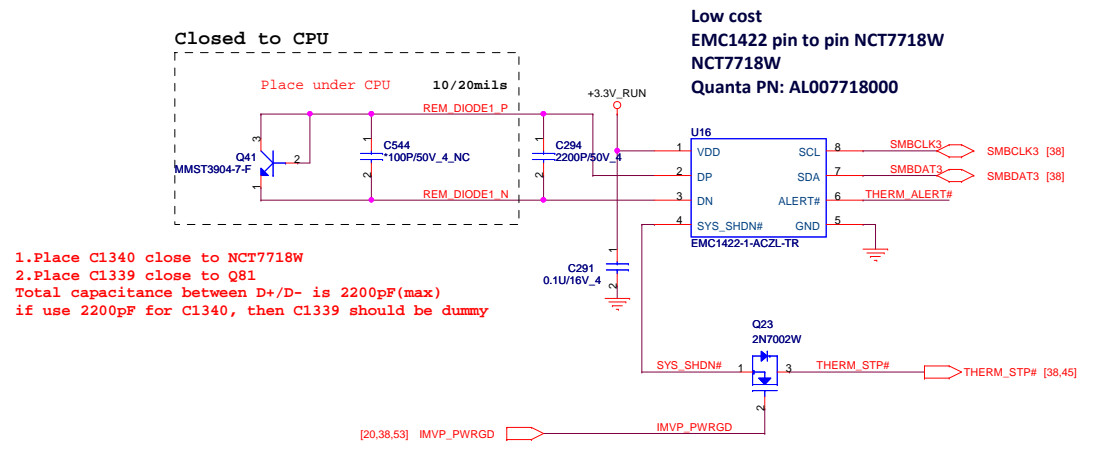
**THERMAL IC**



**FAN CONN**



**For CPU use**

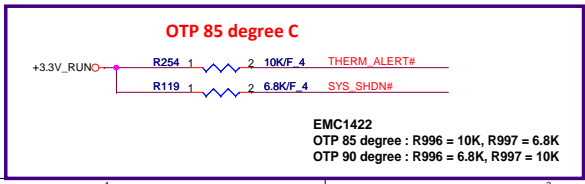


**NCT7718W SMBus address is 1001100xb (98h) (x is R/W bit).**

SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#	2K	7.5K	10.5K	14K	18.7K
77'C	87'C	97'C	107'C	117'C	
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

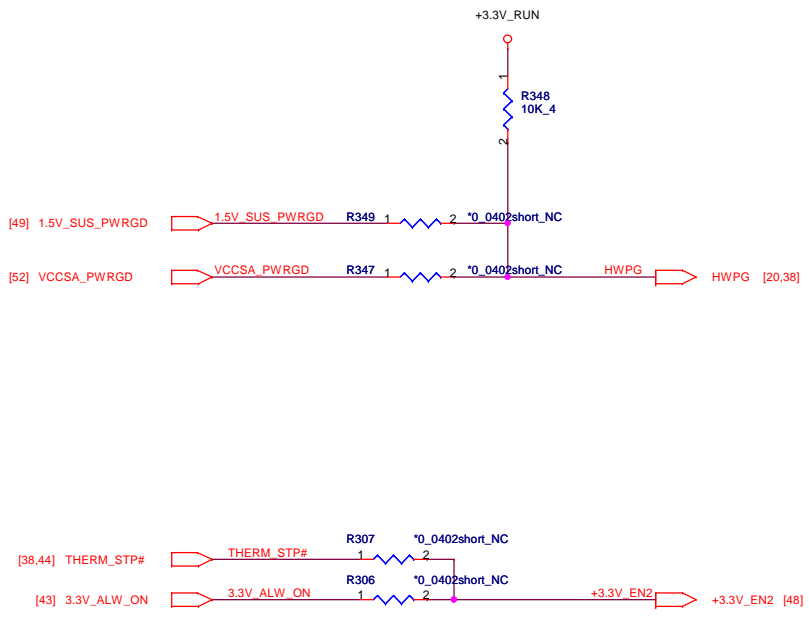
**EMC1422 SMBus address is 1001\_100xb (98h) (x is R/W bit).**

SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	6.8K	10K	15K	22K	33K
77'C	83'C	89'C	95'C	101'C	107'C	
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

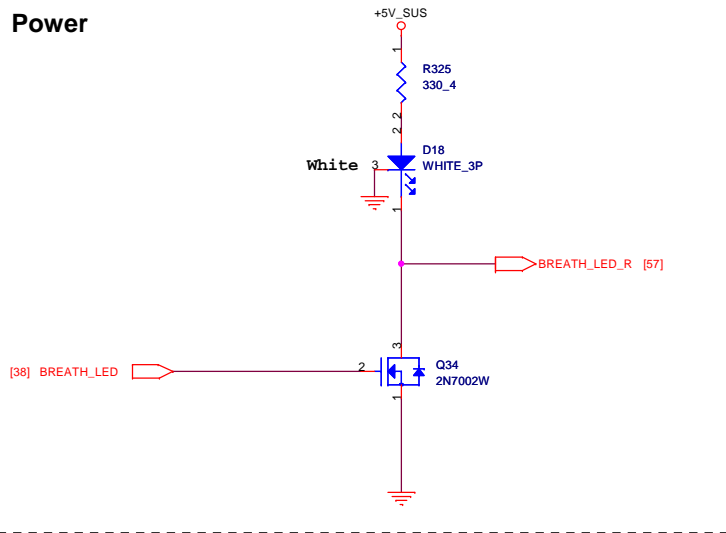


**Quanta Computer Inc.**  
**PROJECT : R09A**

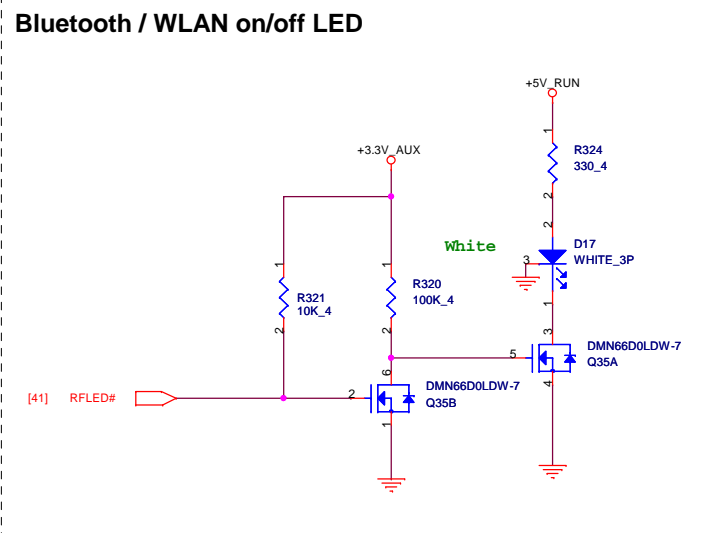
Size Document Number Rev 3A  
**FAN & THERMAL**  
Date: Monday, March 05, 2012 Sheet 44 of 58



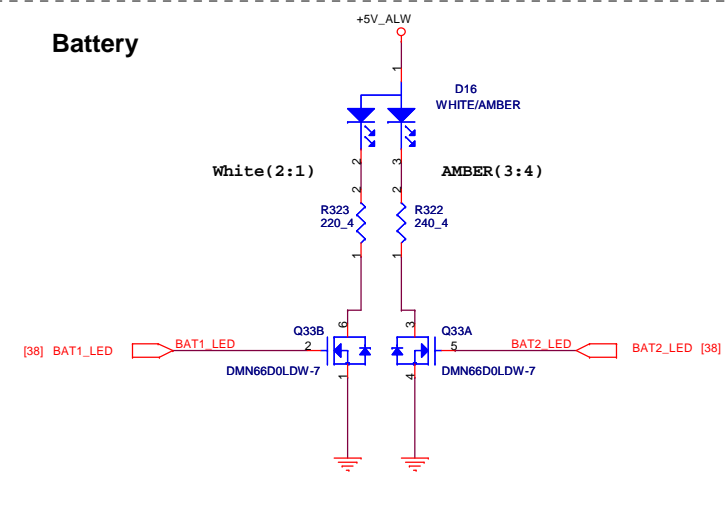
**Power**



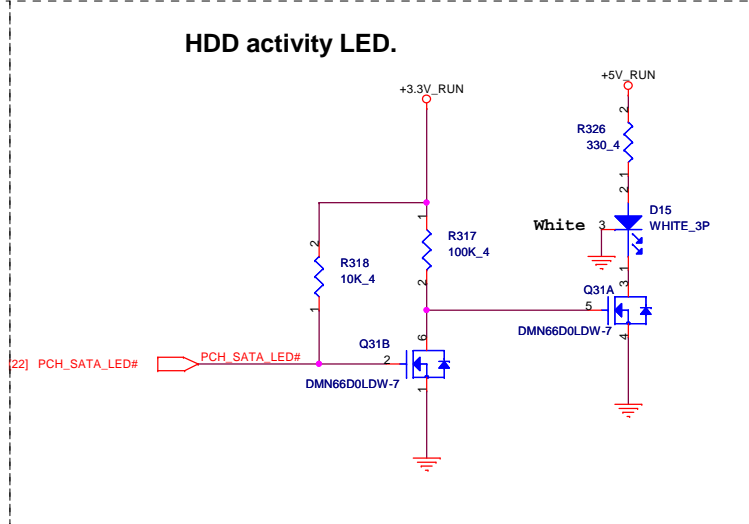
**Bluetooth / WLAN on/off LED**

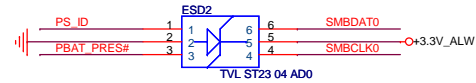
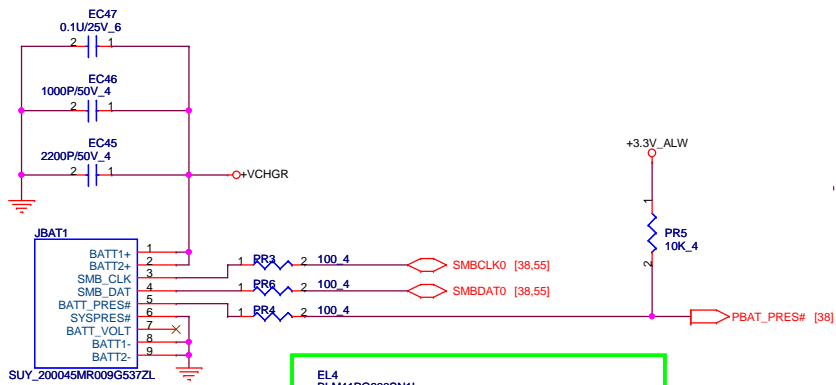


**Battery**

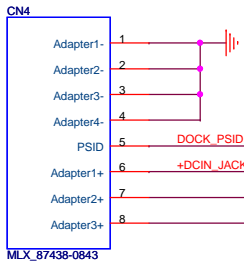
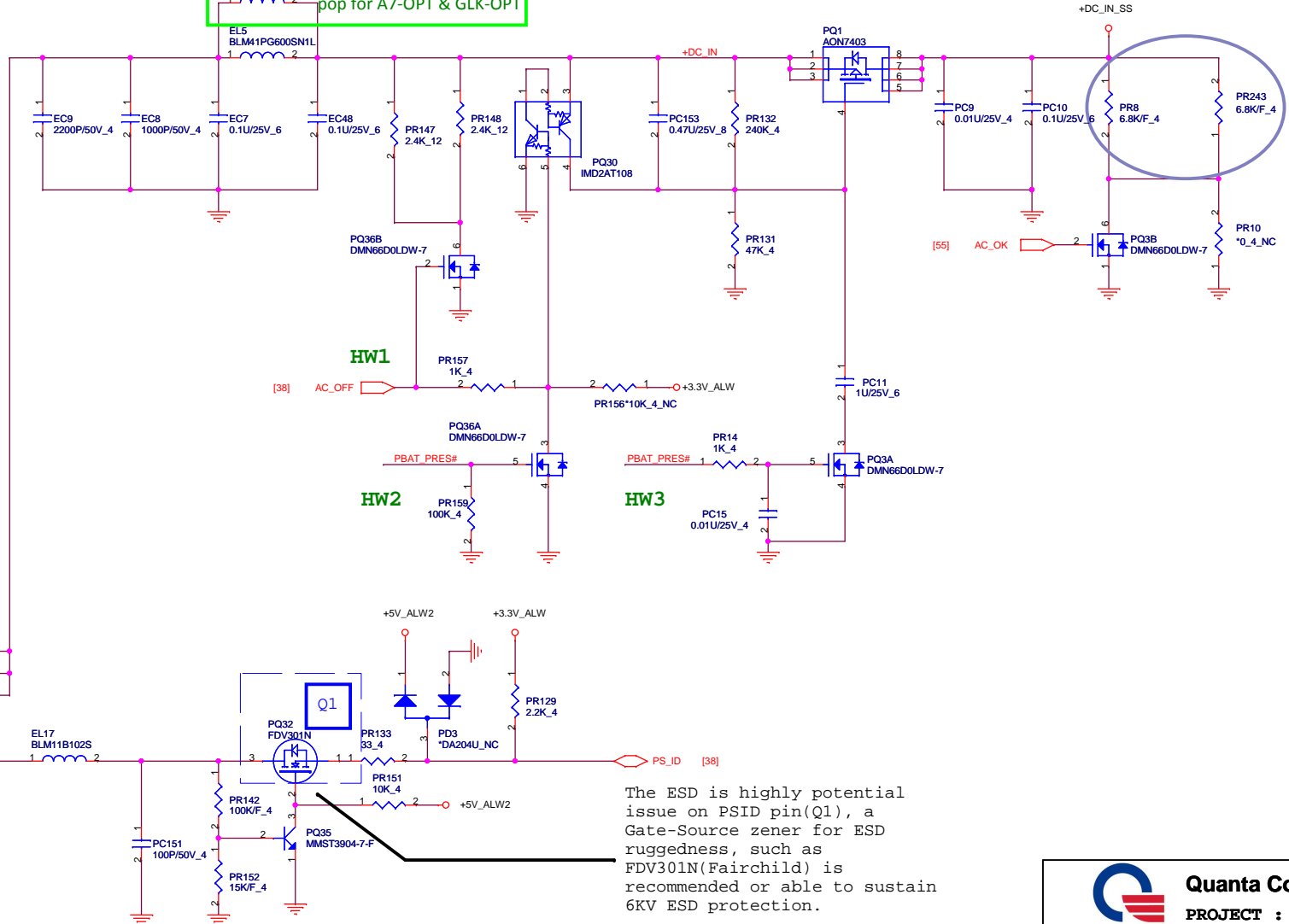


**HDD activity LED.**



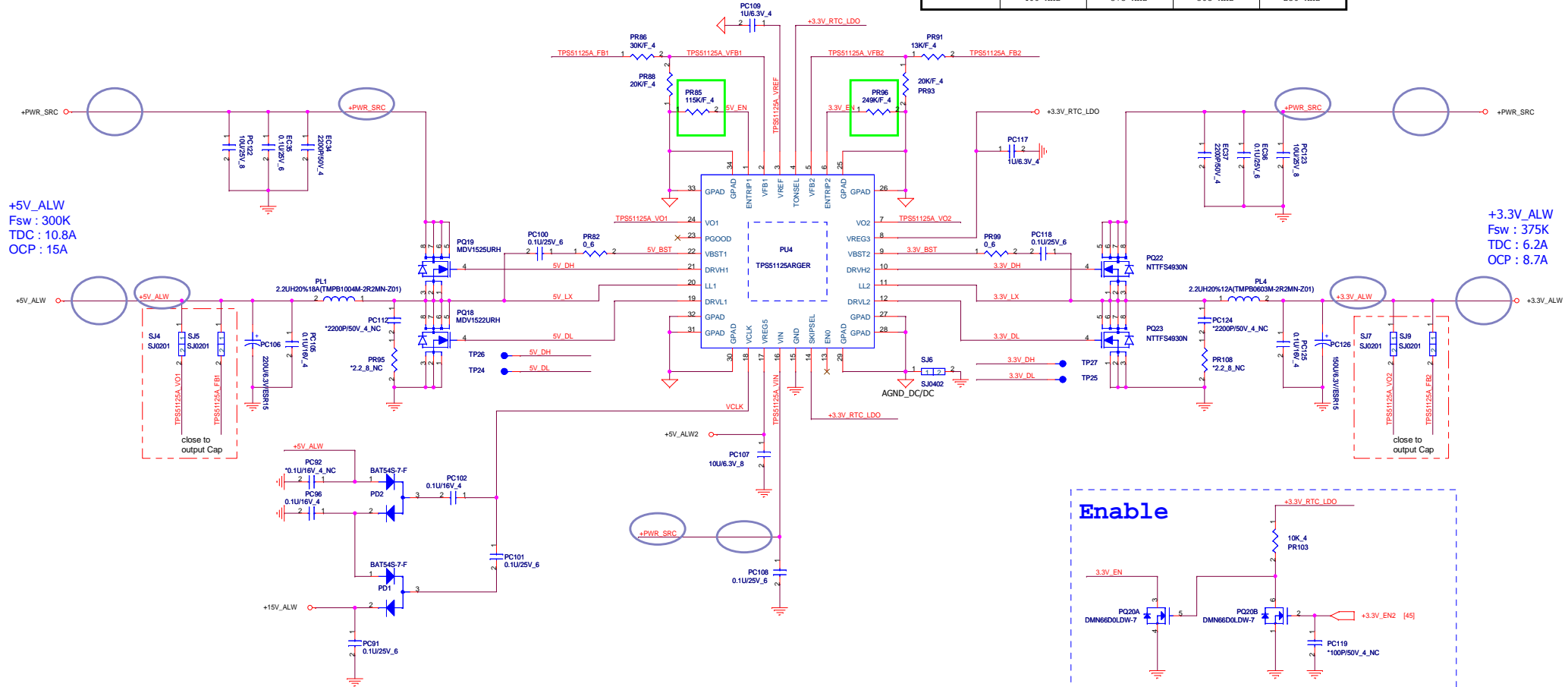


EL4 BLM41PG600SN1L  
EL5 BLM41PG600SN1L  
pop for A7-OPT & GLK-OPT



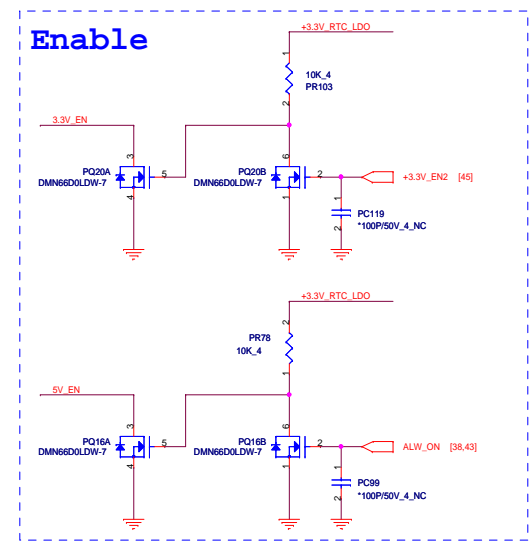
The ESD is highly potential issue on PSID pin(Q1), a Gate-Source zener for ESD ruggedness, such as FDV301N(Fairchild) is recommended or able to sustain 6KV ESD protection.

TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz



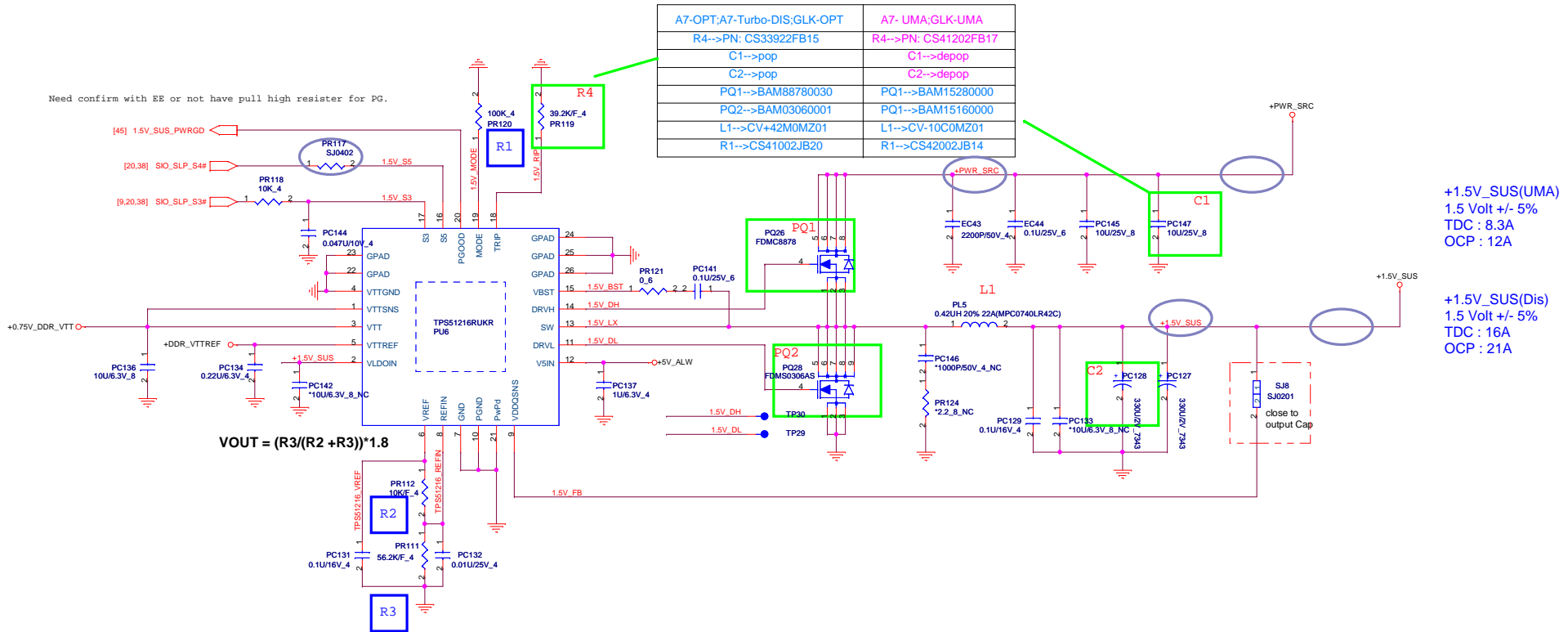
+5V\_ALW  
Fsw : 300K  
TDC : 10.8A  
OCP : 15A

+3.3V\_ALW  
Fsw : 375K  
TDC : 6.2A  
OCP : 8.7A





Need confirm with EE or not have pull high resistor for PG.



$$V_{OUT} = (R3/(R2 + R3)) * 1.8$$

A7-OPT;A7-Turbo-DIS;GLK-OPT	A7- UMA;GLK-UMA
R4-->PN: CS33922FB15	R4-->PN: CS41202FB17
C1-->pop	C1-->depop
C2-->pop	C2-->depop
PQ1-->BAM88780030	PQ1-->BAM15280000
PQ2-->BAM03060001	PQ1-->BAM15160000
L1-->CV+42M0MZ01	L1-->CV-10COMZ01
R1-->CS41002JB20	R1-->CS42002JB14

+1.5V\_SUS(UMA)  
1.5 Volt +/- 5%  
TDC : 8.3A  
OCP : 12A

+1.5V\_SUS(Dis)  
1.5 Volt +/- 5%  
TDC : 16A  
OCP : 21A

MODE Selection			
	Resistance between MODE and GND	Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz
R1	68K_4	CS36802JB12	300k Hz Non-tracking
R1	47K_4	CS34702JB21	400k Hz Discharge

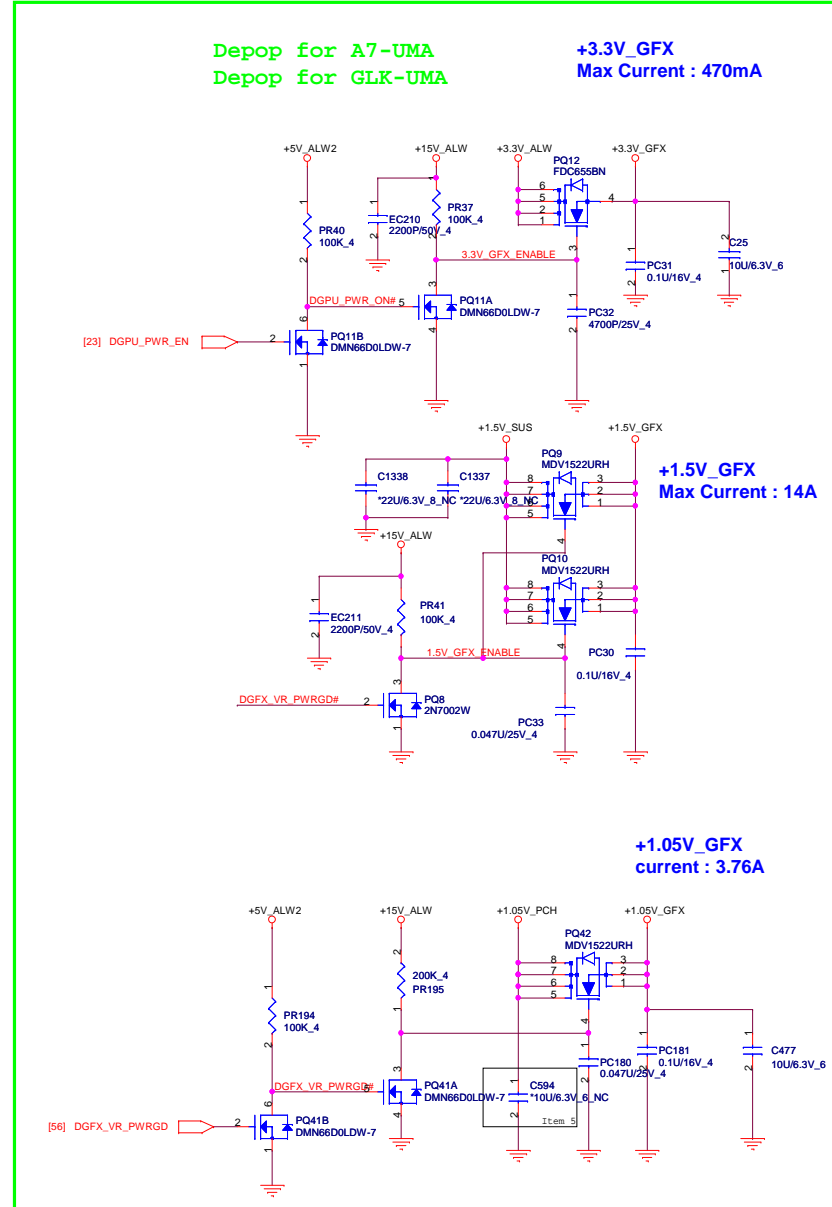
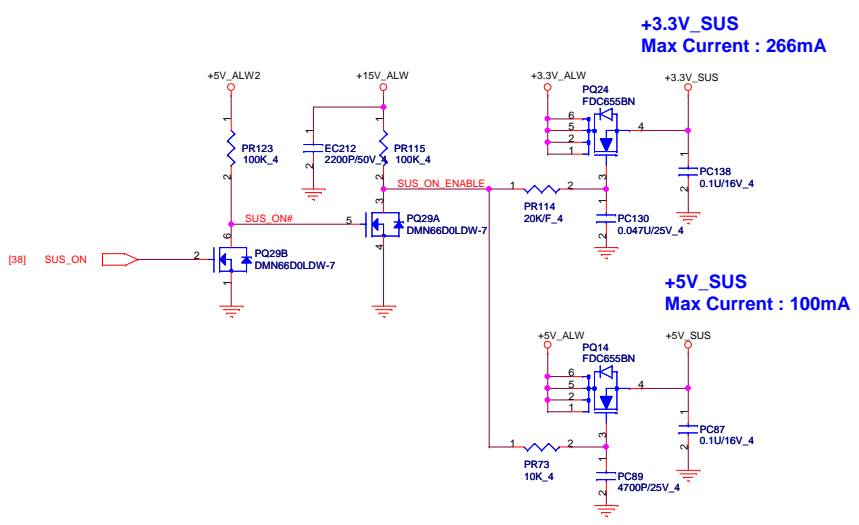
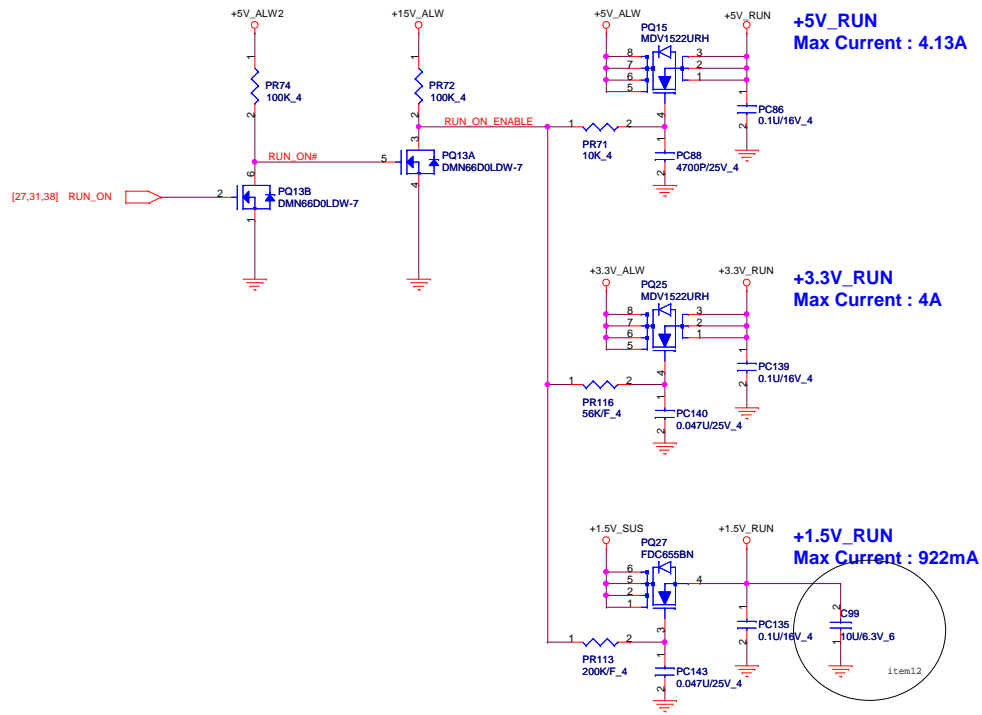
Outputs Management by S3, S5 control

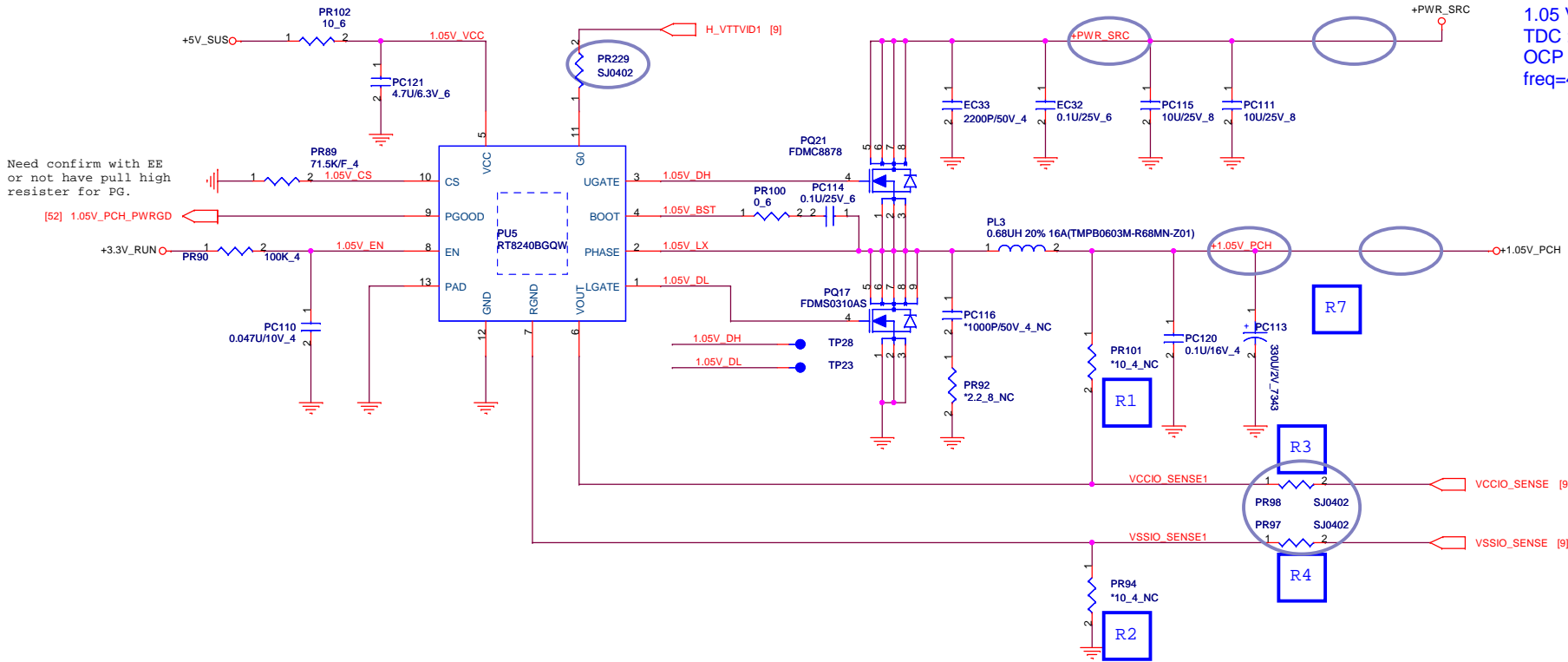
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

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PROJECT : R09

Size | Document Number | Rev  
**1.5\_SUS/0.75\_DDR\_VTT (TPS51216RUKR)** | 1A

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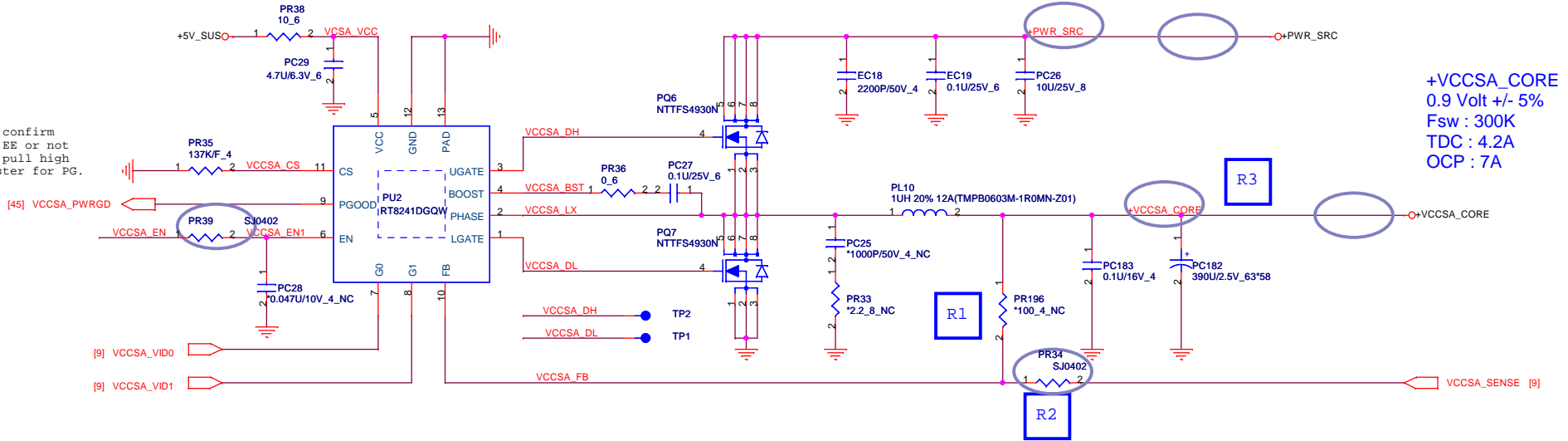
Need confirm with EE or not have pull high resistor for PG.

[52] 1.05V\_PCH\_PWRGD

+1.0V\_VCCIO  
 1.05 Volt DC +/- 2%  
 TDC : 13.4A  
 OCP : 18.5A  
 freq=400k

For EA test	
R1	10_4
R2	10_4
R3	NC
R4	NC
R5	NC
R6	NC
R7	NC

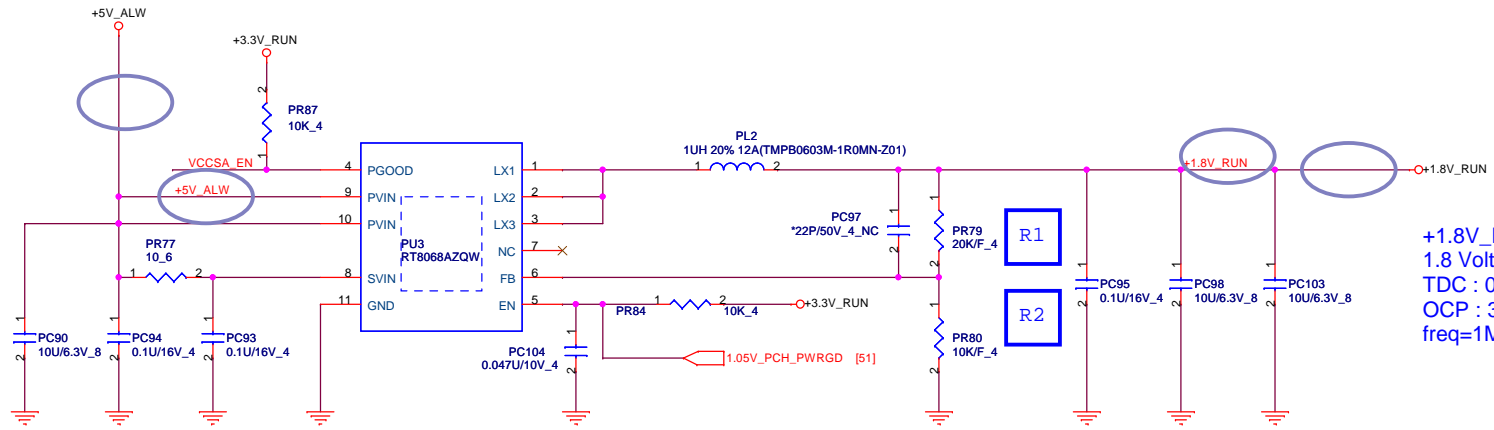
Need confirm with EE or not have pull high resistor for PG.



+VCCSA\_CORE  
0.9 Volt +/- 5%  
Fsw : 300K  
TDC : 4.2A  
OCP : 7A

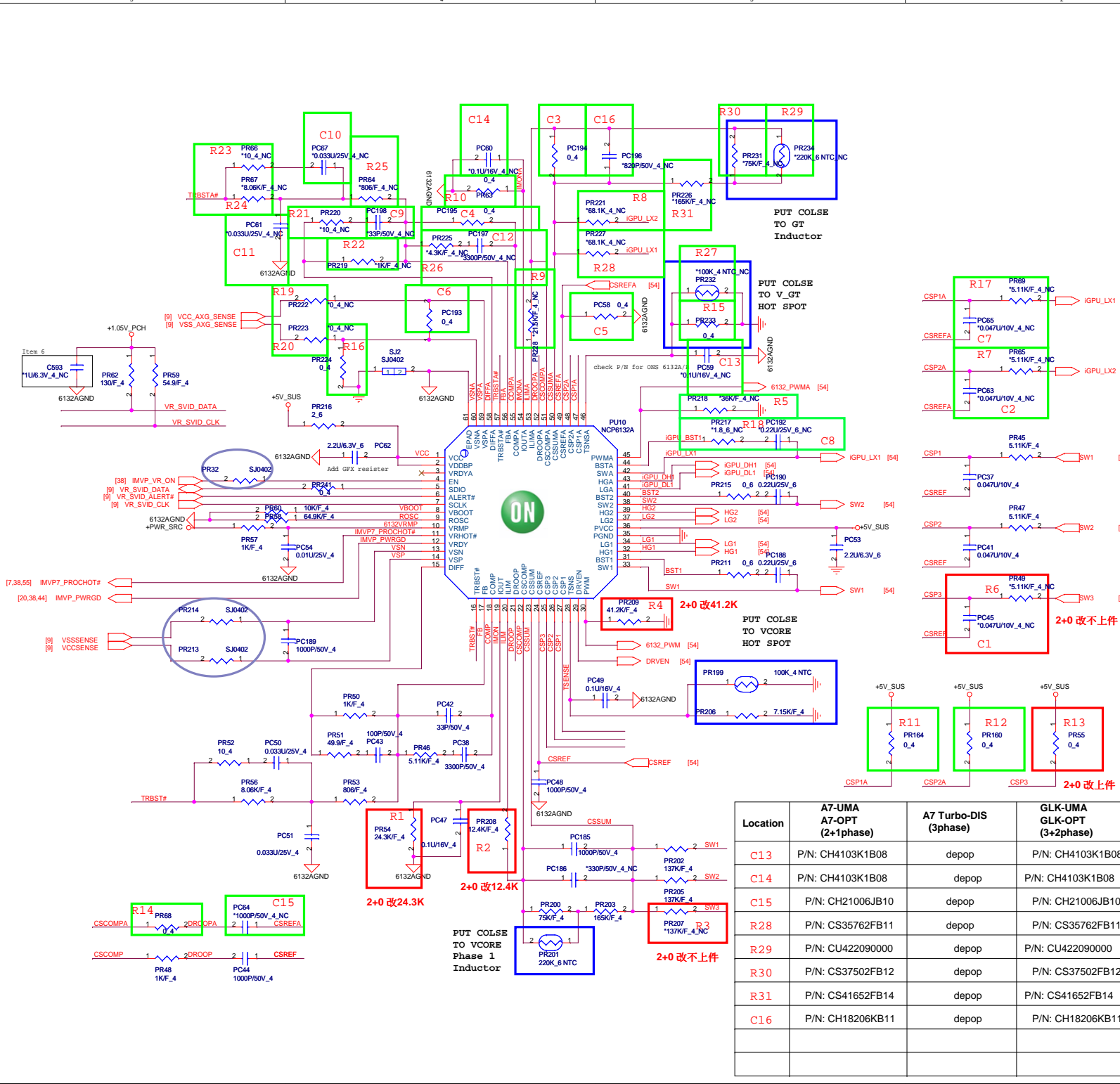
VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V

For EA test	
R1	100_4
R2	NC
R3	NC
R4	NC



+1.8V\_RUN  
1.8 Volt +/- 5%  
TDC : 0.869A  
OCP : 3.5A  
freq=1M

$$VOUT = 0.6(1+R1/R2)$$



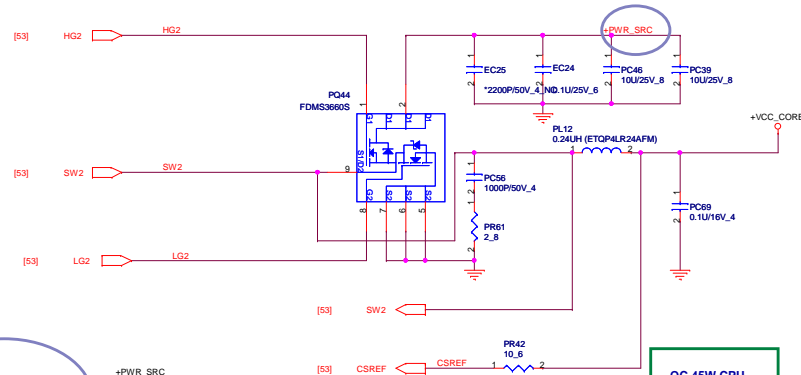
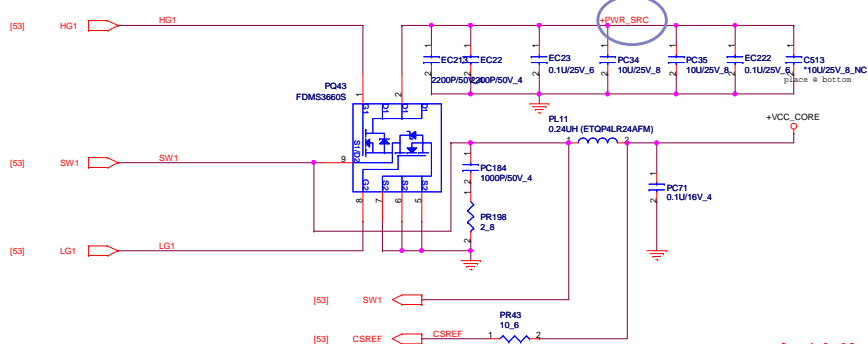
Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
R1	P/N: CS32432FB01	P/N: CS32372FB05	P/N: CS32372FB05
R2	P/N: CS31242FB05	P/N: CS32102FB14	P/N: CS32102FB14
R3	depop	P/N: CS41302FB01	P/N: CS41302FB01
R4	P/N: CS34122FB19	P/N: CS37322FB14	P/N: CS37322FB14
R5	P/N: CS32552FB03	depop	P/N: CS33602FB07
R6	depop	P/N: CS25112FB15	P/N: CS25112FB15
C1	depop	P/N: CH34702KB10	P/N: CH34702KB10
R7	depop	depop	P/N: CS25112FB15
C2	depop	depop	P/N: CH34702KB10
R8	depop	depop	P/N: CS35762FB11
R9	P/N: CS31582FB12	depop	P/N: CS32152B00
R10	P/N: CS32432FB01	P/N: CS00002JB38	P/N: CS32402FB15
R11	depop	P/N: CS00002JB38	depop
R12	P/N: CS00002JB38	P/N: CS00002JB38	depop
R13	P/N: CS00002JB38	depop	depop
C3	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
C4	P/N: CH01006JB08	P/N: CS00002JB38	P/N: CH01006JB08
C5	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R14	P/N: CS15102FB19	P/N: CS00002JB38	P/N: CS15102FB19
C6	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R15	P/N: CS28252FB15	P/N: CS00002JB38	P/N: CS28252FB15
R16	depop	P/N: CS00002JB38	depop
R17	P/N: CS25112FB15	depop	P/N: CS25112FB15
C7	P/N: CH34702KB10	depop	P/N: CH34702KB10
R18	P/N: CS00003J951	depop	P/N: CS00003J951
C8	P/N: CH4224K9904	depop	P/N: CH4224K9904
R19	P/N: CS00002JB38	depop	P/N: CS00002JB38
R20	P/N: CS00002JB38	depop	P/N: CS00002JB38
R21	P/N: CS01002JB22	depop	P/N: CS01002JB22
R22	P/N: CS21002FB24	depop	P/N: CS21002FB24
C9	P/N: CH03306JB04	depop	P/N: CH03306JB04
R23	P/N: CS01002JB22	depop	P/N: CS01002JB22
R24	P/N: CS22002FB19	depop	P/N: CS22002FB19
C10	P/N: CH16806KB17	depop	P/N: CH16806KB17
C11	P/N: CH24704KB19	depop	P/N: CH24704KB19
R25	P/N: CS31072FB10	depop	P/N: CS31072FB10
R26	P/N: CS24302FB07	depop	P/N: CS24302FB07
C12	P/N: CH23306JB16	depop	P/N: CH23306JB16
R27	P/N: CU4100B0000	depop	P/N: CU4100B0000
C13	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C14	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C15	P/N: CH21006JB10	depop	P/N: CH21006JB10
R28	P/N: CS35762FB11	depop	P/N: CS35762FB11
R29	P/N: CU422090000	depop	P/N: CU422090000
R30	P/N: CS37502FB12	depop	P/N: CS37502FB12
R31	P/N: CS41652FB14	depop	P/N: CS41652FB14
C16	P/N: CH18206KB11	depop	P/N: CH18206KB11

Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
C13	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C14	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C15	P/N: CH21006JB10	depop	P/N: CH21006JB10
R28	P/N: CS35762FB11	depop	P/N: CS35762FB11
R29	P/N: CU422090000	depop	P/N: CU422090000
R30	P/N: CS37502FB12	depop	P/N: CS37502FB12
R31	P/N: CS41652FB14	depop	P/N: CS41652FB14
C16	P/N: CH18206KB11	depop	P/N: CH18206KB11

**Quanta Computer Inc.**  
PROJECT : R09

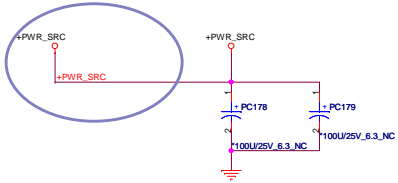
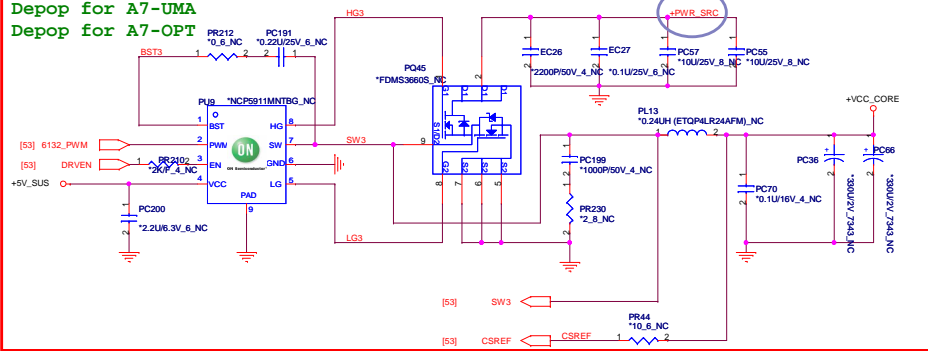
Size	Document Number	Rev
	<b>CPU_CORE (NCP6132)</b>	1A
Date:	Monday, March 05, 2012	Sheet 53 of 57

# CPU Power



2+0 改不上件

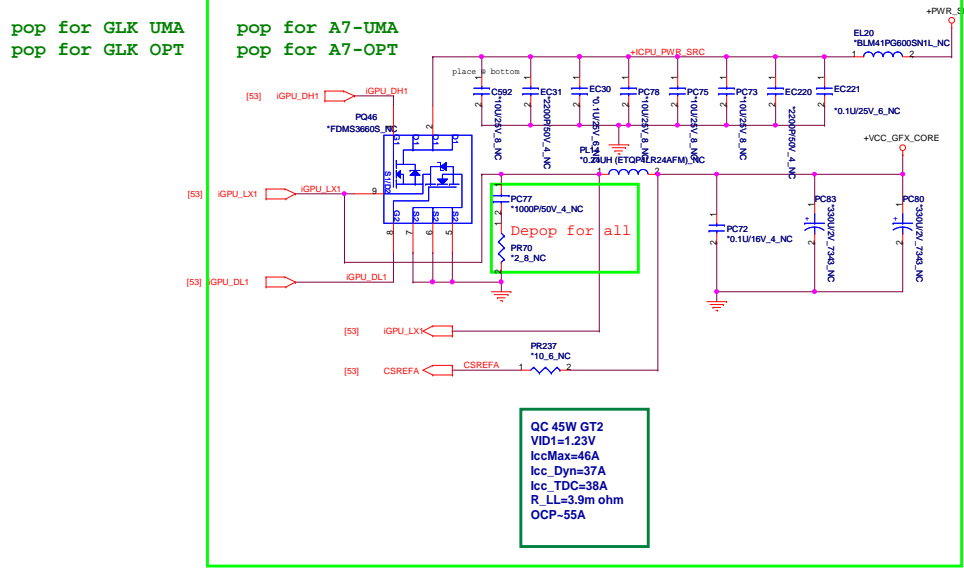
Depop for A7-UMA  
Depop for A7-OPT



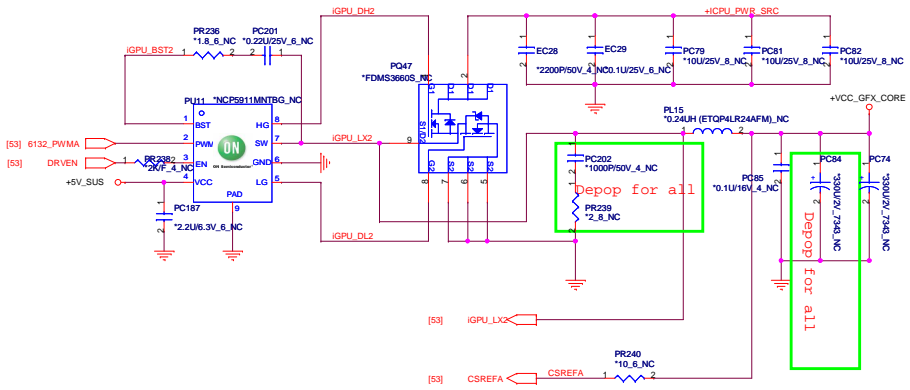
QC 45W CPU  
VID1=0.9V  
IccMax=94A  
Icc\_Dyn=66A  
Icc\_TDC=52A  
R\_LL=1.9m ohm  
OCP=110A

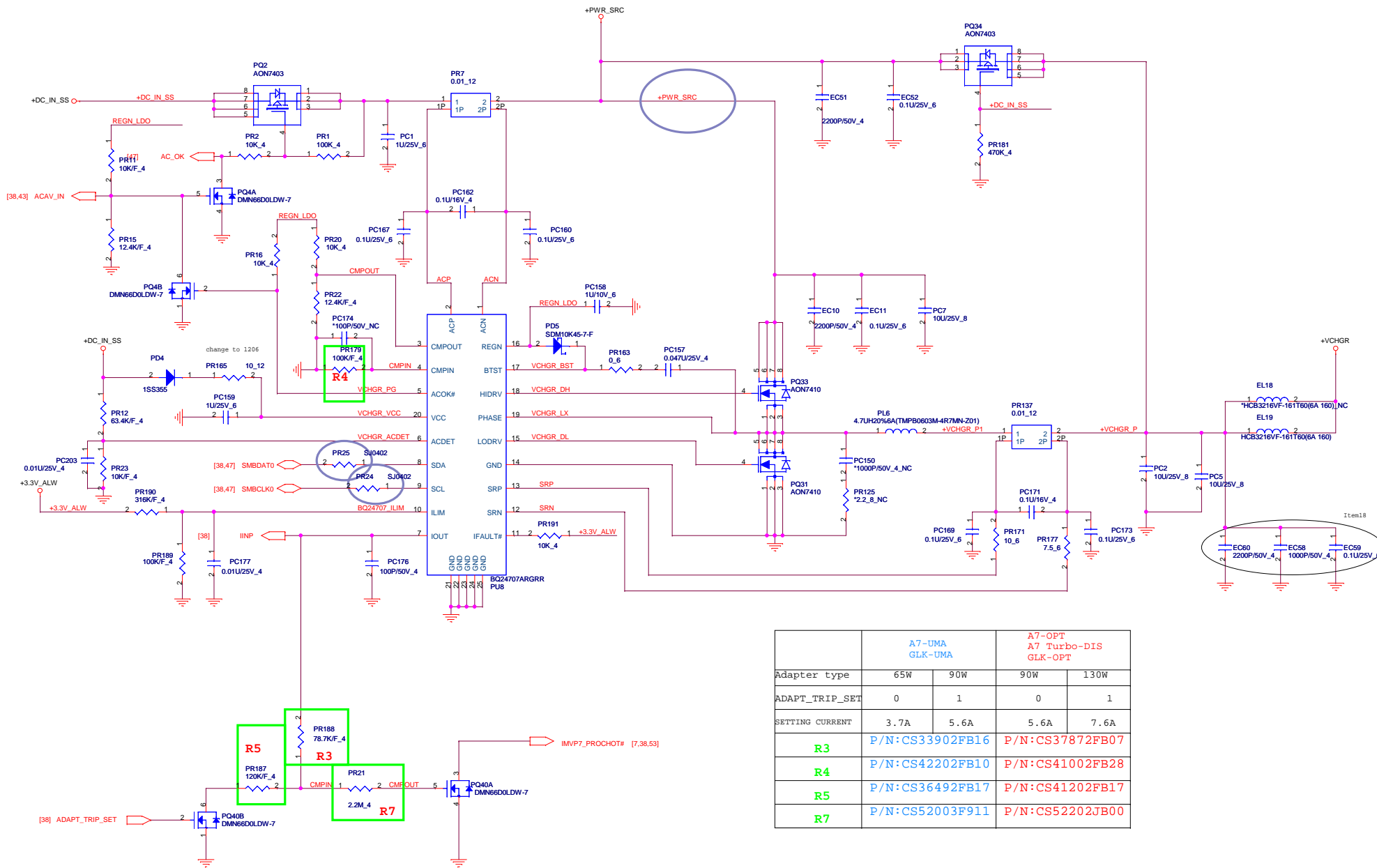
pop for GLK UMA  
pop for GLK OPT

pop for A7-UMA  
pop for A7-OPT



QC 45W GT2  
VID1=1.23V  
IccMax=46A  
Icc\_Dyn=37A  
Icc\_TDC=38A  
R\_LL=3.9m ohm  
OCP=55A





	A7-UMA GLK-UMA	A7-OPT A7 Turbo-DIS GLK-OPT		
Adapter type	65W	90W	90W	130W
ADAPT_TRIP_SET	0	1	0	1
SETTING CURRENT	3.7A	5.6A	5.6A	7.6A
R3	P/N:CS33902FB16	P/N:CS37872FB07		
R4	P/N:CS42202FB10	P/N:CS41002FB28		
R5	P/N:CS36492FB17	P/N:CS41202FB17		
R7	P/N:CS52003F911	P/N:CS52202JB00		

Depop for A7-UMA  
Depop for GLK-UMA

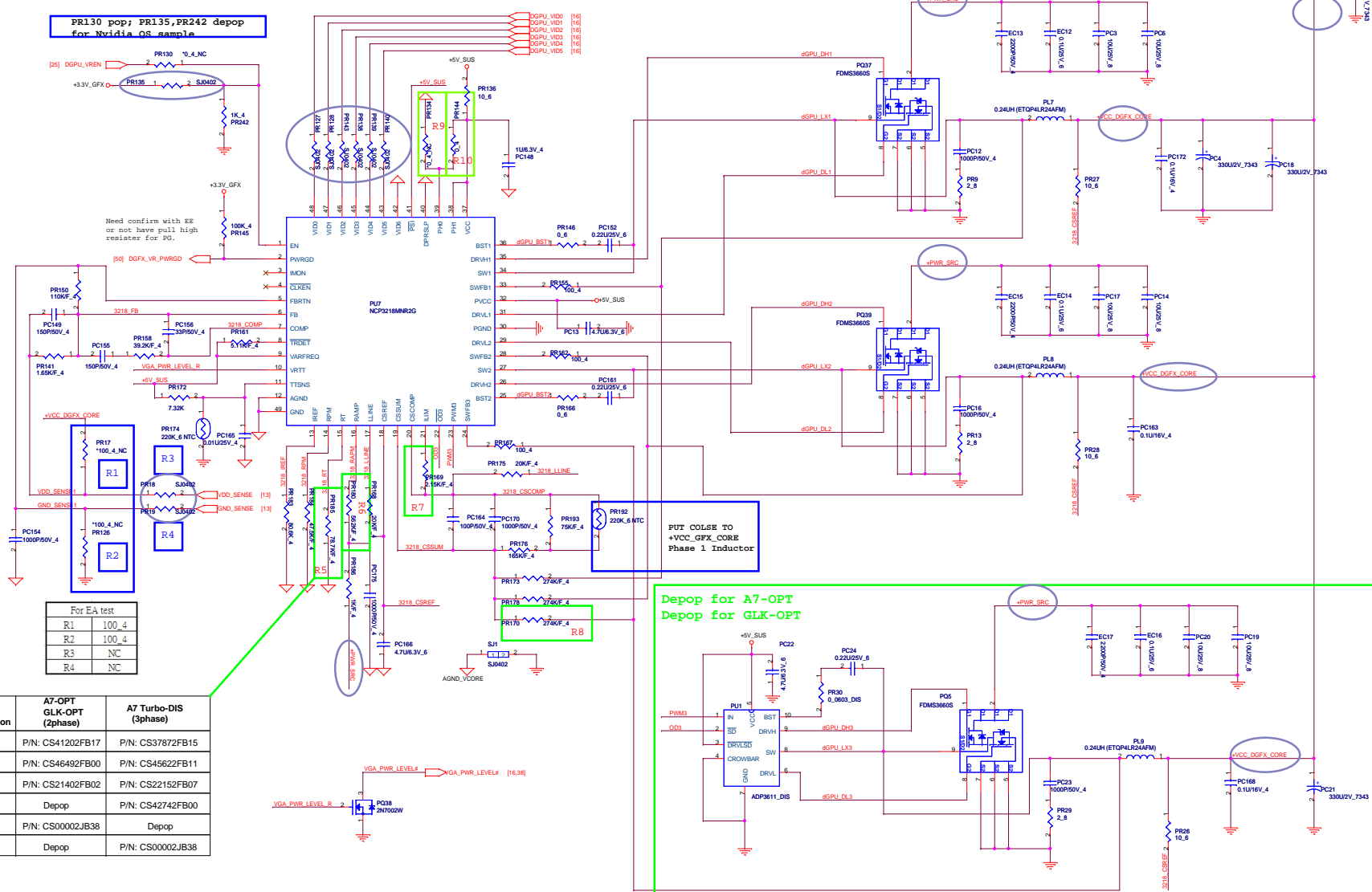
**N13XXX2**

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

**N13XXX1**

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

+VCC\_GFX\_CORE  
Fs=400K  
Dis =30A  
Turbo =42A  
Dis OC=42A  
Turbo OC=60A



PR130 pop; PR135, PR242 depop for Nvidia OS sample

Need confirm with EE or not have pull high resistor for PG.

Depop for A7-OPT  
Depop for GLK-OPT

For EA test

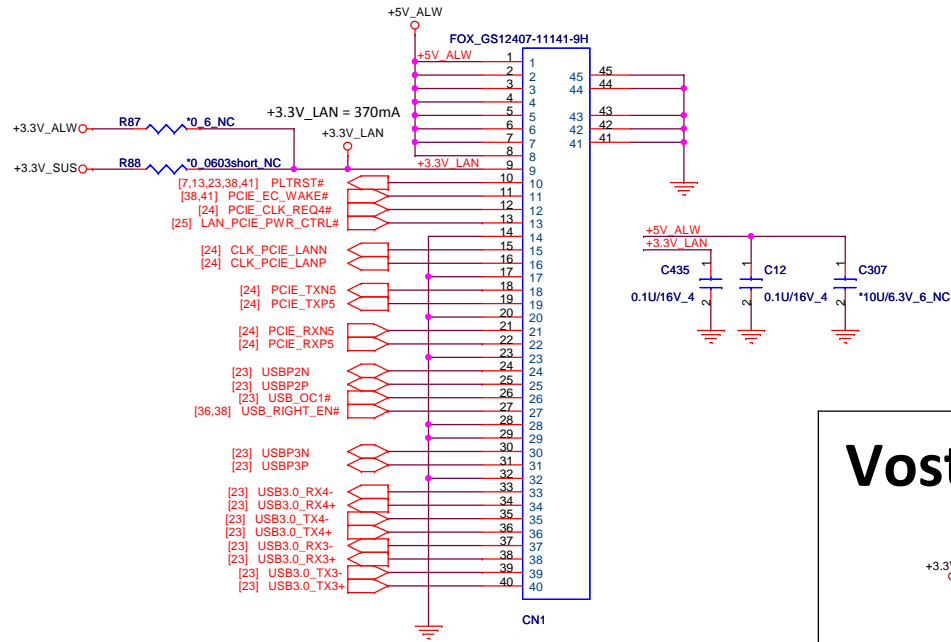
R1	100_4
R2	100_4
R3	NC
R4	NC

Location	A7-OPT GLK-OPT (2phase)	A7 Turbo-DIS (3phase)
R5	P/N: CS41202FB17	P/N: CS3782FB15
R6	P/N: CS46492FB00	P/N: CS45622FB11
R7	P/N: CS21402FB02	P/N: CS22152FB07
R8	Depop	P/N: CS42742FB00
R9	P/N: CS00002JB38	Depop
R10	Depop	P/N: CS00002JB38



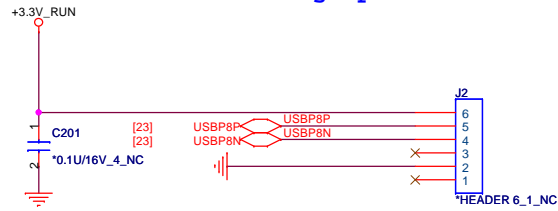
# DB CONNECTOR

## RJ45 + USB 3.0 \* 2



## Vostro - NA

### Fingerprint



### Power button board

