

# R33 INTEL UMA/DISCRETE SYSTEM DIAGRAM

01

**+3V/+5V S5**  
PG.35

**+1.05V\_VTT**  
PG.38

**CPU Core**  
PG.40~41

**DDR3**  
PG.37

**VCCSA**  
PG.36

**Charge**  
PG.34

**Dis-Charge**  
PG.39

**+VGACORE**  
PG.42

**+1.0V\_VGA**  
PG.43

**SODIMM1**  
Max. 4GB  
PG.12

**SODIMM2**  
Max. 4GB  
PG.13

**INTEL IVY**  
37.5mm X 37.5mm  
989pin PGA  
TDP 35W  
PG.2~5

**AMD Thames XT**  
29mm X 29mm  
TDP 25W  
PG.14~20

**VRAM**  
128Mx16x8,128bit  
PG.21~22

**HDD**  
PG.32

**ODD**  
PG.32

**INTEL PCH Panther Point**  
PG.6~11

**USB3.0 Ports X2**  
PG.28

**Webcam**  
PG.23

**PCI-E x 1**

LANE2 LANE1

**LAN**  
RTL8105EH  
10/100  
PG.29

**WLAN BT COMBO**  
PG.33

USB 2.0  
PORT10

**PCI-E x 1**

LANE3

**Accelerometer**  
PG.33

**Card Reader**  
RTS5229  
PG.26

**KBC**  
EnE KB3930QF A2  
PG.30

SMBUS LPC

**KB** PG.31

**TP** PG.31

**ROM** PG.30

**FAN** PG.32

**AUDIO CODEC**  
IDT 92HD87  
ICT  
PG.27

**Speaker**  
PG.27

**HP/MIC**  
PG.28

**Analog MIC**  
PG.28

**HDMI**  
PG.25

**CRT**  
PG.24

**LVDS**  
PG.23

**Stackup**

TOP

GND

IN1

IN2

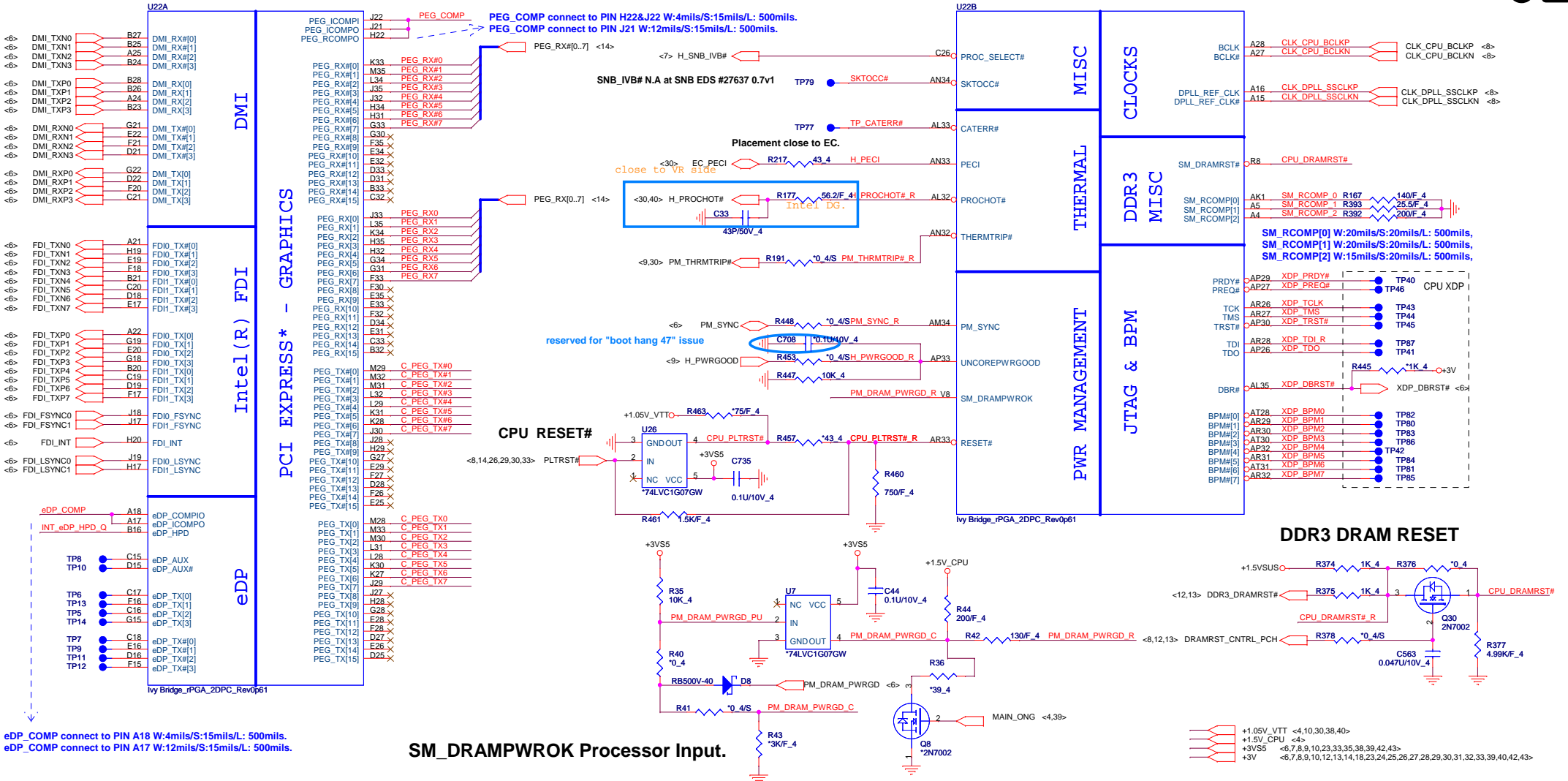
VCC

BOT



PROJECT : R33  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
BLOCK DIAGRAM		
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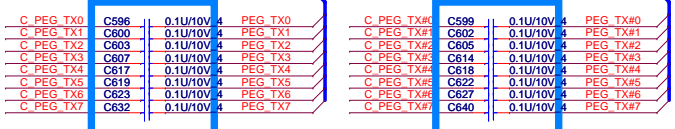


eDP\_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.  
eDP\_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

SM\_DRAMPWROK Processor Input.

**FDI disable (DIS only stuff)**

**PEG x16 disable (UMA only remove)**

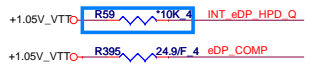


FDI\_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

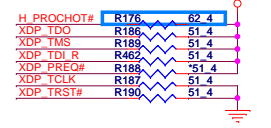
**DP & PEG Compensation**



eDP\_ICOMPIO and ICOMPIO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG\_ICOMPI and RCOMPIO signals should be routed within 500 mils typical impedance = 43 mohms PEG\_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

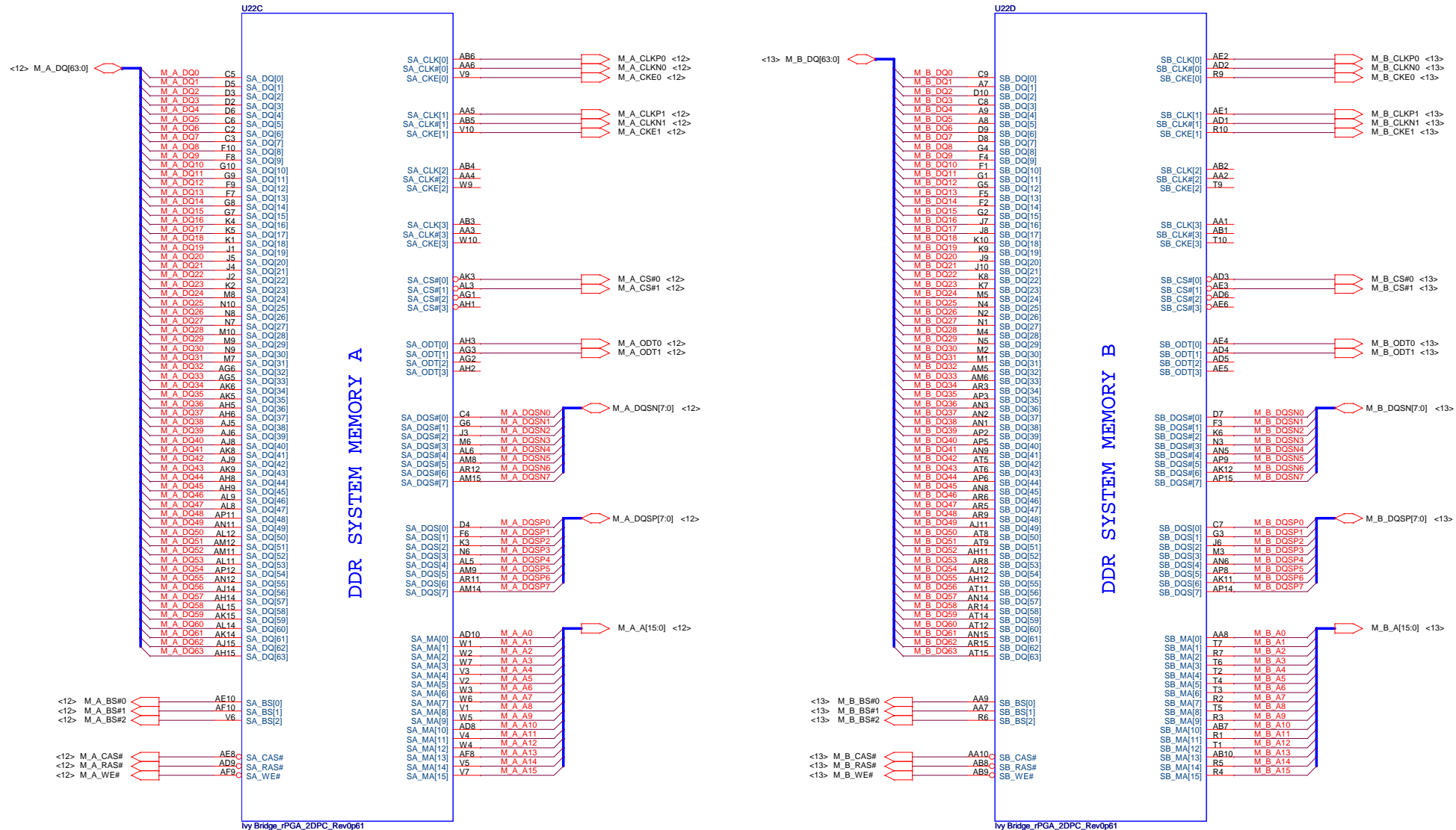
**Processor pull-up (CPU)**



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**Quanta Computer Inc.**

Size Custom	Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
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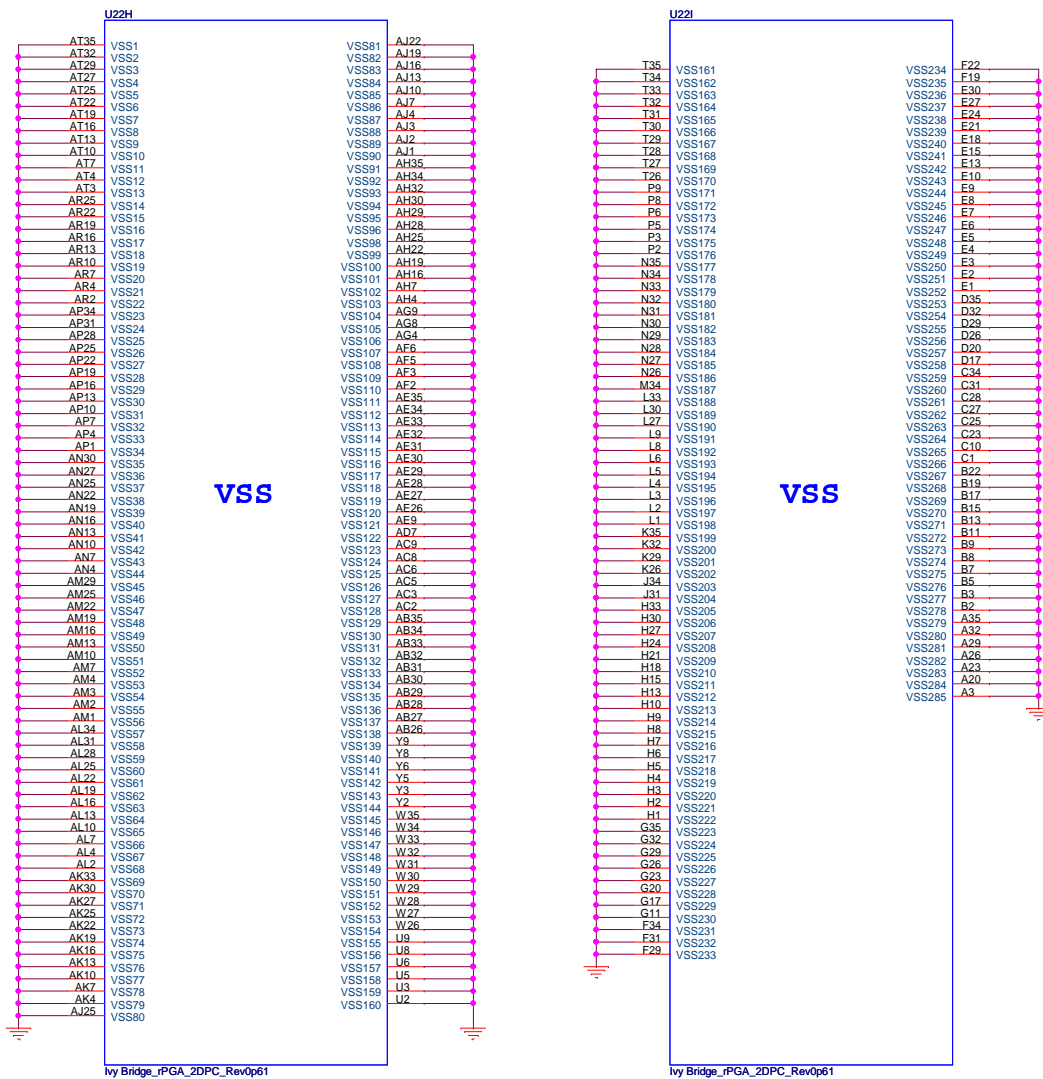
# Ivy Bridge Processor (DDR3)



	<b>PROJECT : R33</b>		Rev 1A
	Quanta Computer Inc.		
	Document Number	SNB 2/4 (DDR3 I/F)	
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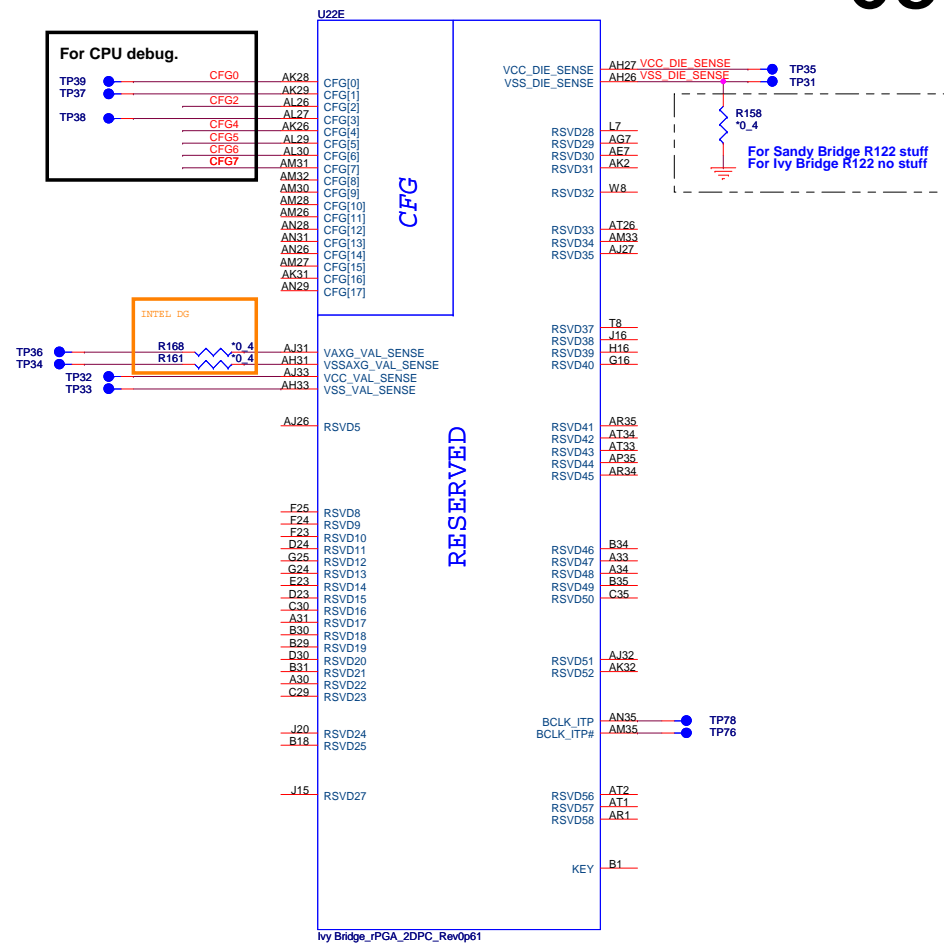


# Ivy Bridge Processor (GND)



# Ivy Bridge Processor (RESERVED, CFG)

05

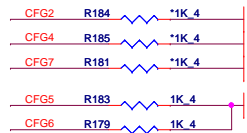


For rPGA socket, RSVD59 pin should be left NC.

## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



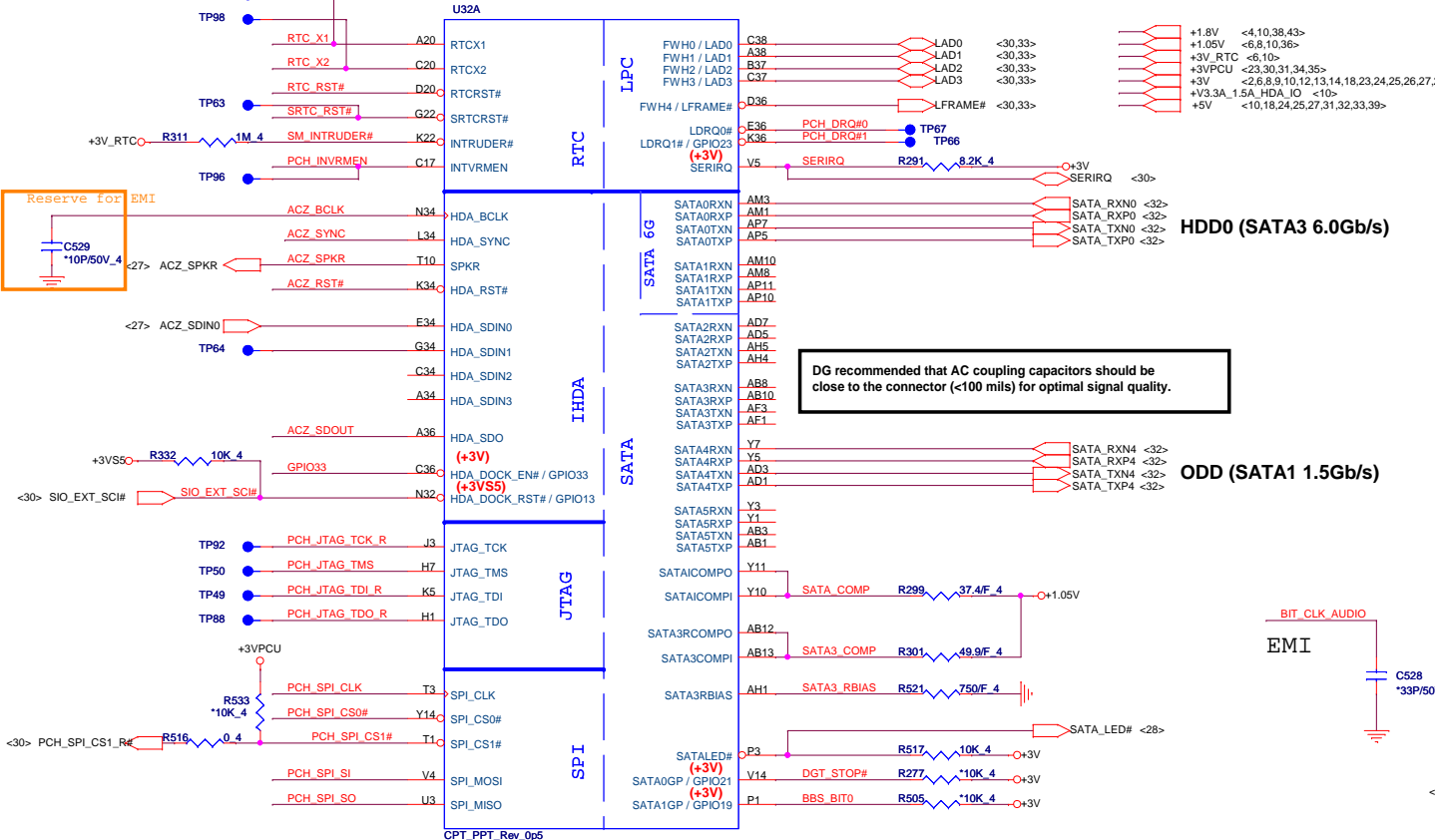
**CFG[6:5] (PCIe Port Bifurcation Straps)**  
 11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

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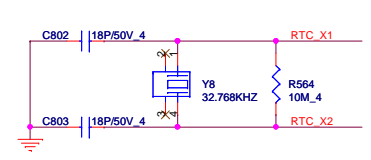
Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
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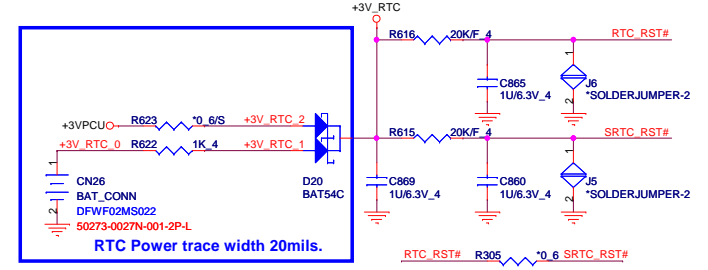
### Cougar Point/Panther Point (HDA,JTAG,SATA)



### RTC Clock 32.768KHz



### RTC Circuitry(RTC)

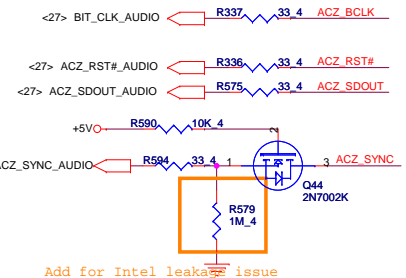


### HDD0 (SATA3 6.0Gb/s)

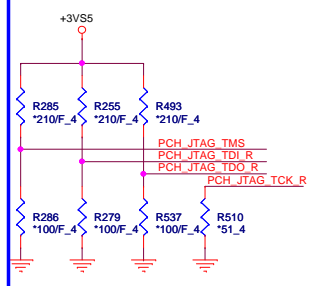
### ODD (SATA1 1.5Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

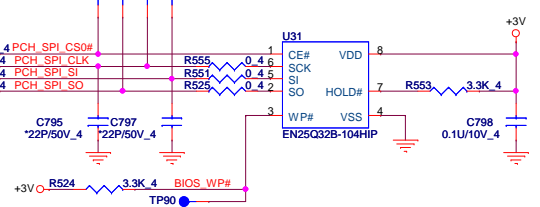
### HDA Bus(CLG)



### PCH JTAG Debug(CLG)



### PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZNOQ02 (EN25Q32B-104HIP)
Max	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
Socket		DFHS08FS023

### PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R500 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 *1K 4 R585 *10K 4 +3V PCI_GNT3# <8>
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	R572 0 4 GPIO33 1 2 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R534 *1K 4 R585 *1K 4 BBS_BIT0
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK		BBS_BIT1 <8>
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R547 *1K 4 NV_ALE <8>
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R528 *2.2K 4 R546 *1K 4 NV_CLE <9> H_SNB_IVB# <2> gandy/ivy bridge
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VSS R334 *1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overriden	<30> GPIO33_E ACZ_SDOUT R573 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R492 *1K 4 PLL_ODVR_EN <9>
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPL_SI R292 *1K 4 +3V

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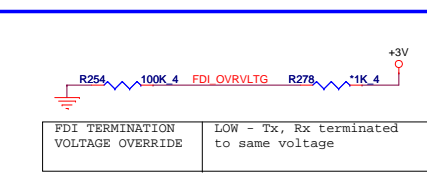
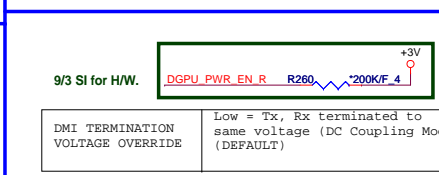
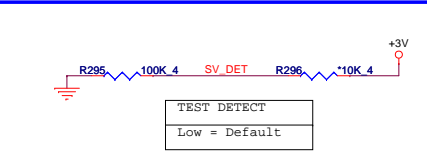
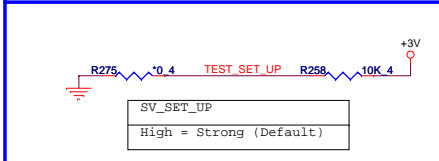
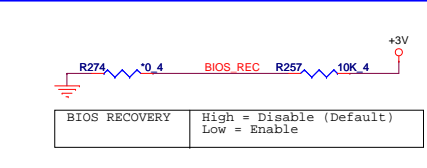
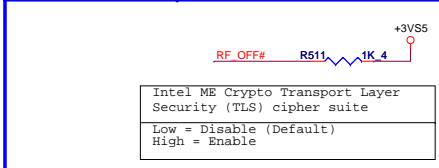
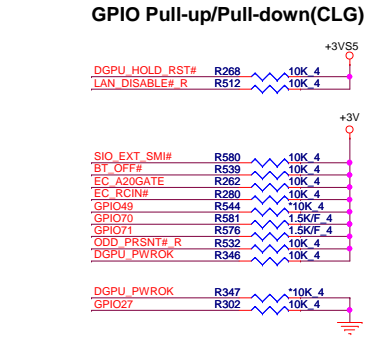
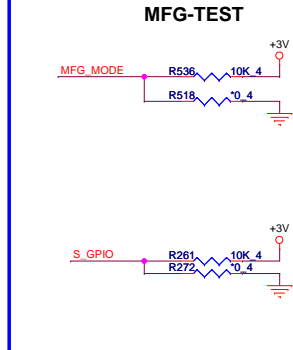
Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
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# Cougar Point/Panther Point (GPIO,VSS\_NCTF,RSVD)

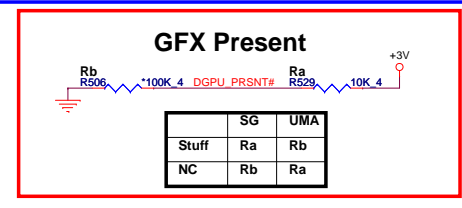
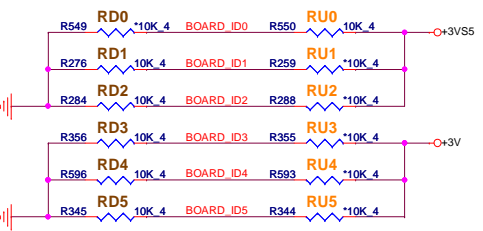
Clock Gen Power OK (CLG)



## BOARD ID SETTING

- <8> BOARD\_ID0 BOARD\_ID0
- <8> BOARD\_ID1 BOARD\_ID1
- <8> BOARD\_ID2 BOARD\_ID2
- <8> BOARD\_ID3 BOARD\_ID3

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R33 UMA	0	0	0	0	0	0
R33 DIS	0	0	0	0	0	1
	0	0	0	0	1	1
	0	0	0	1	1	1
	0	0	0	0	0	0



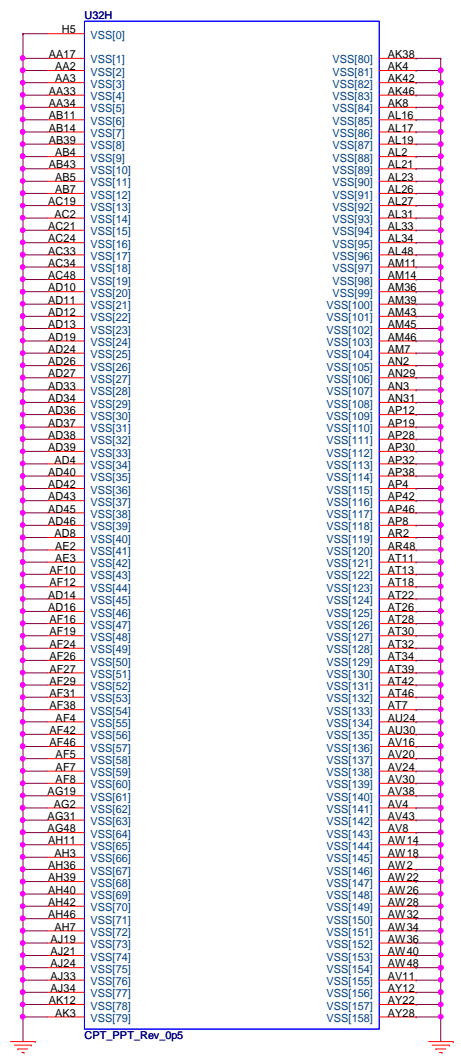
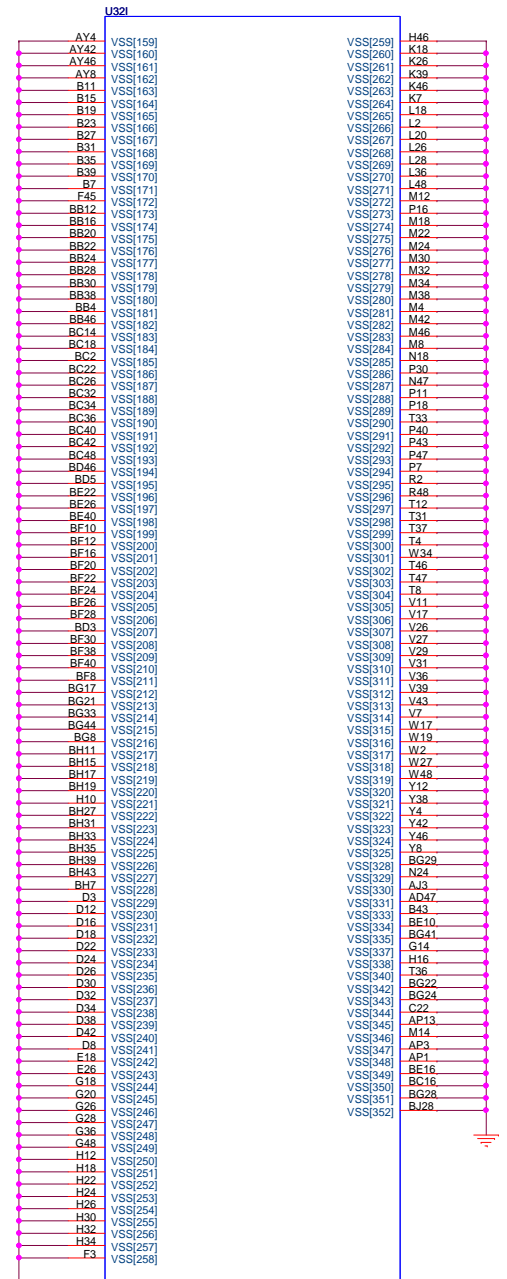
**PROJECT : R33**  
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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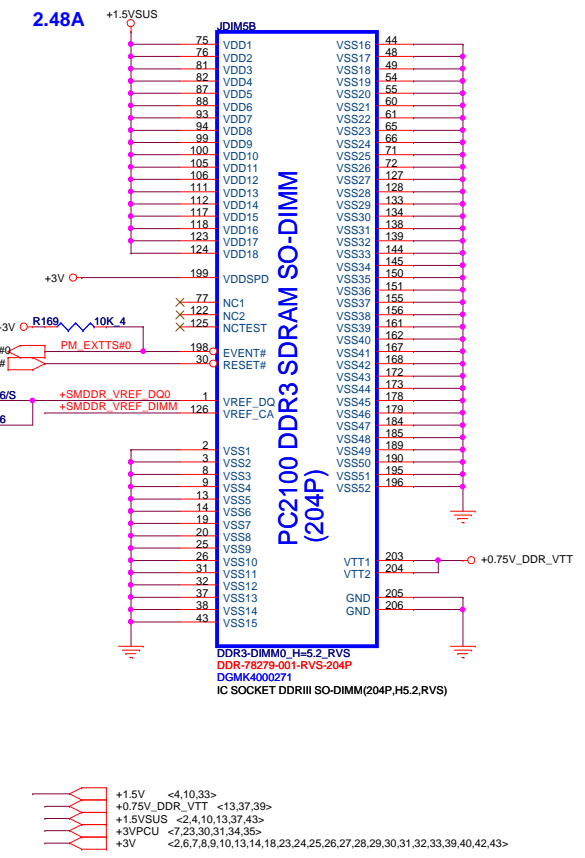
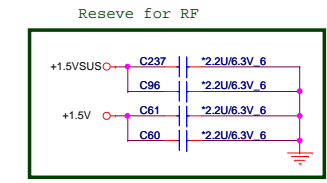
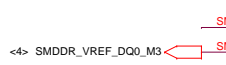
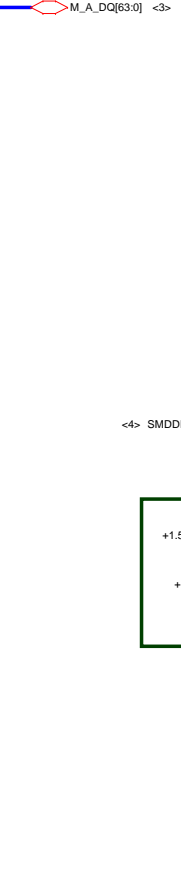
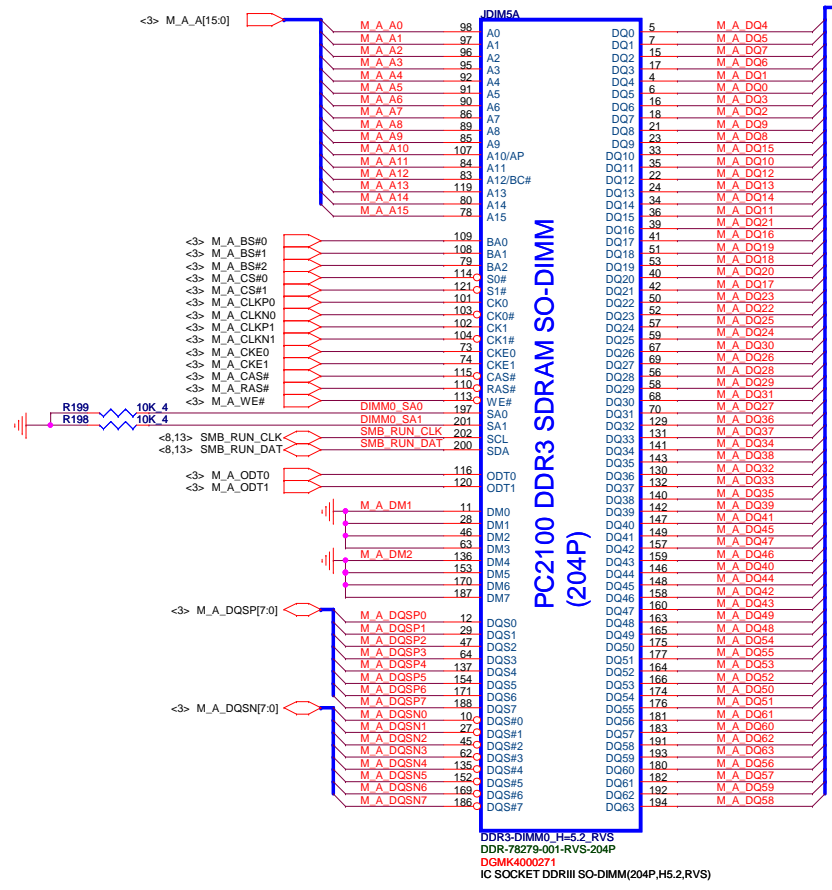


Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)



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	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	
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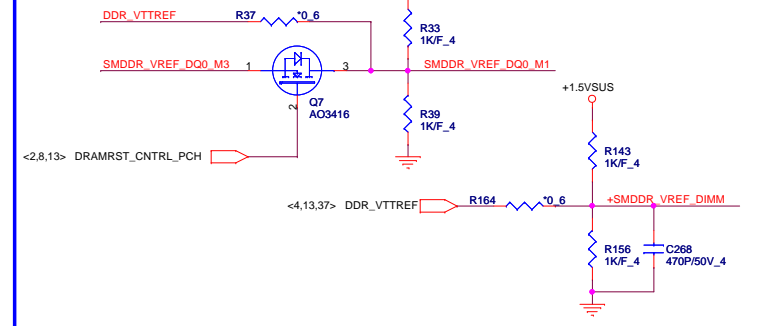
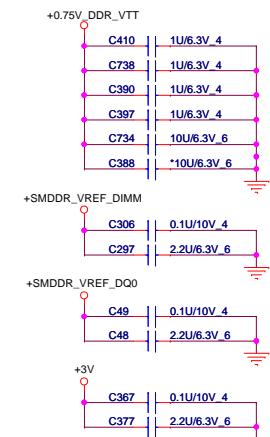
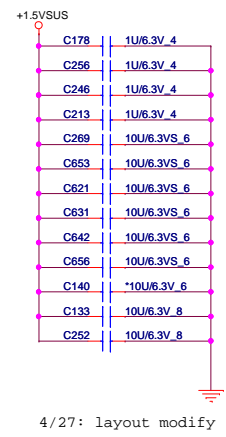


VREF DQ0 M2 Solution

Place these Caps near So-Dimm0.

VREF DQ0 M1 Solution

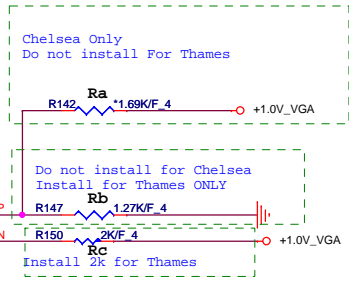
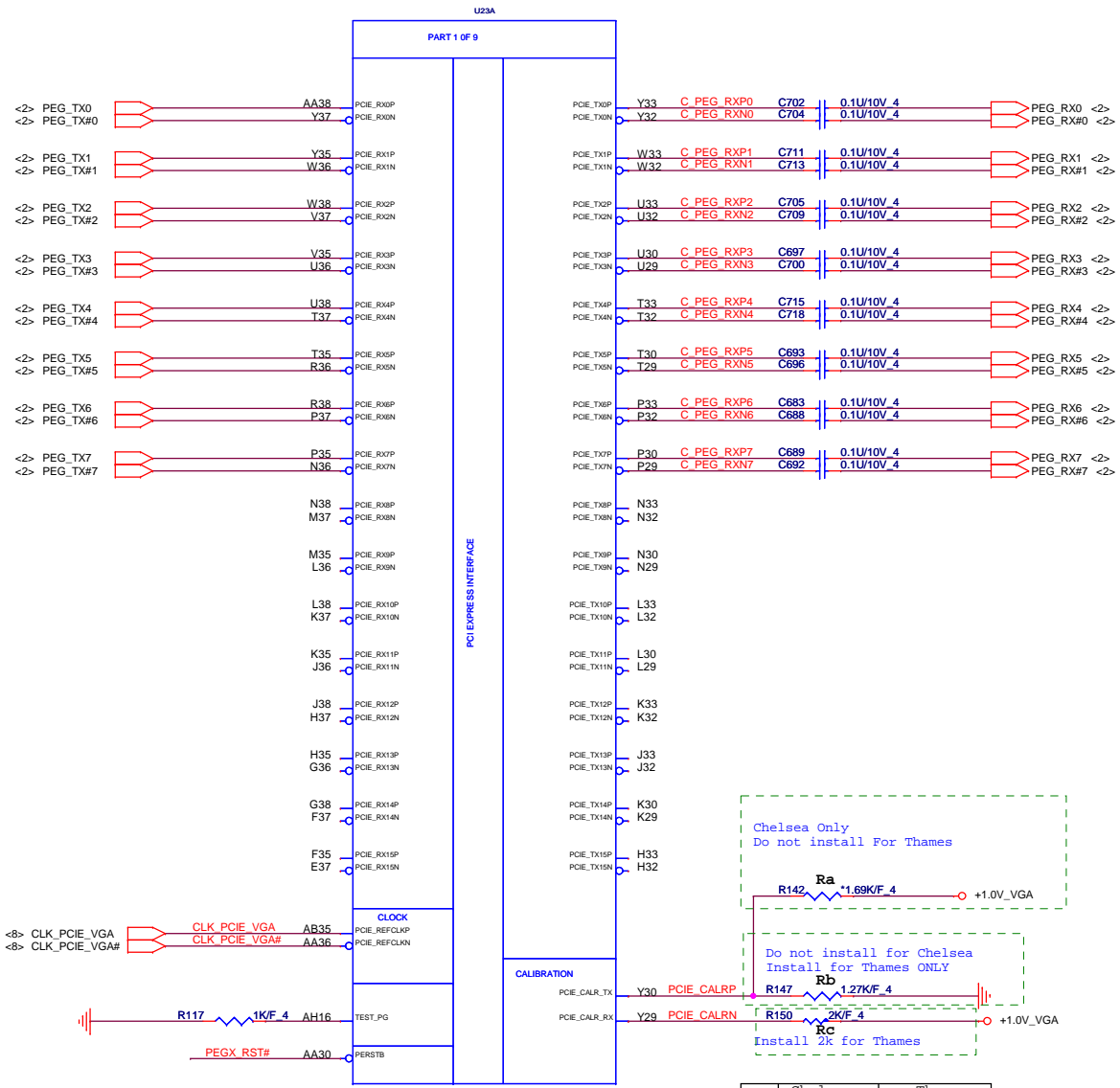
del M2 solution



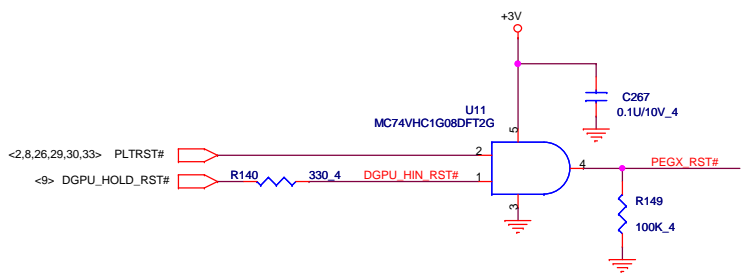
4/27: layout modify

	<b>PROJECT : R33</b>		Rev 1A
	Quanta Computer Inc.		
	Document Number	DDR3 DIMM0-RVS (5.2H)	
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	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K



<16,18,19,43> +1.0V\_VGA

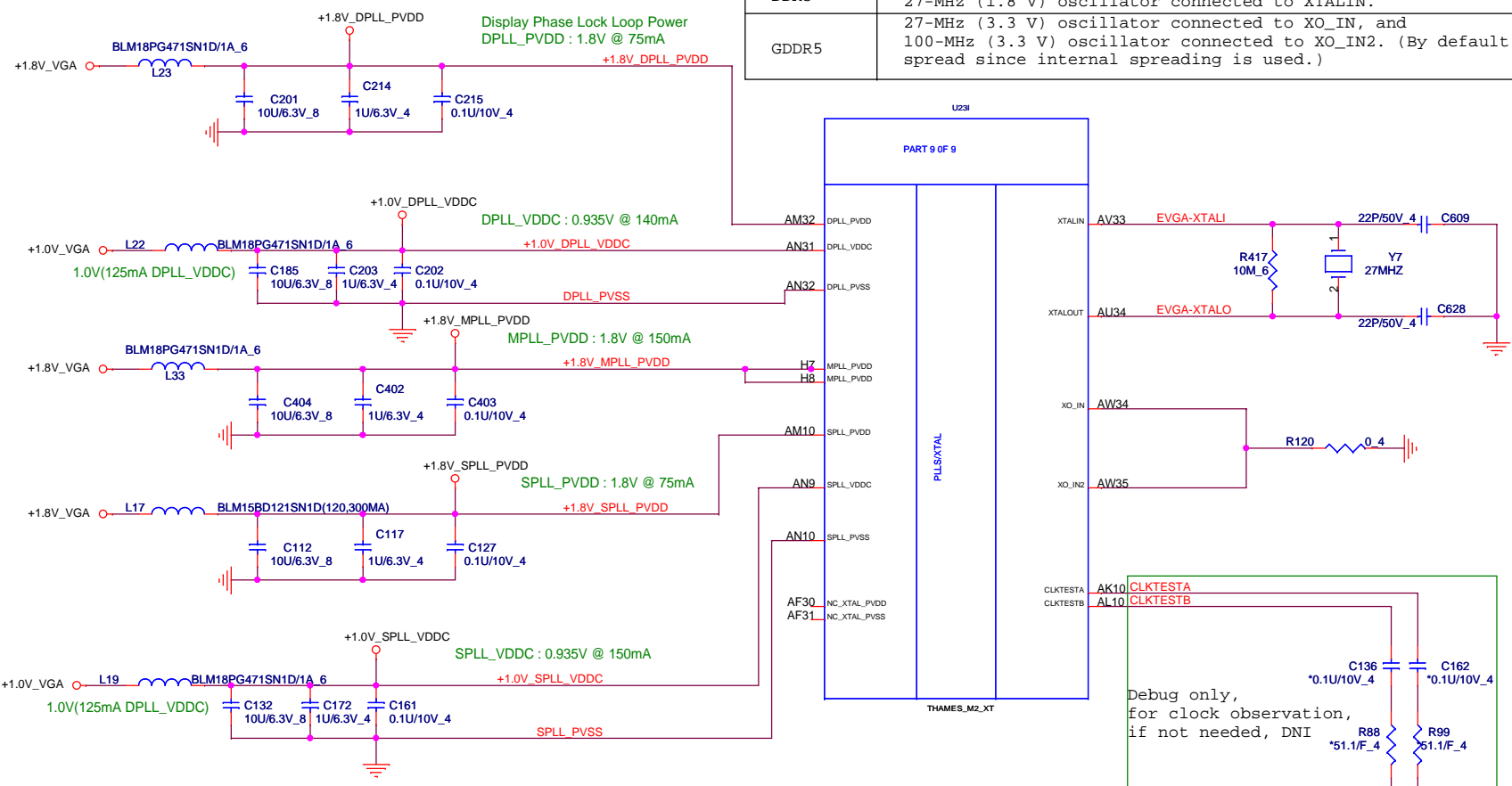




**PROJECT : R33**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>THAMES_PCIE_Interface</b>	Rev 1A
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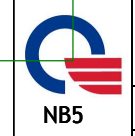
Memory Type	
DDR3	27-MHz ( $\pm 30$ ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



<14,18,19,43> +1.0V\_VGA  +1.0V\_VGA  
 <15,18,19,43> +1.8V\_VGA  +1.8V\_VGA

Debug only,  
 for clock observation,  
 if not needed, DNI

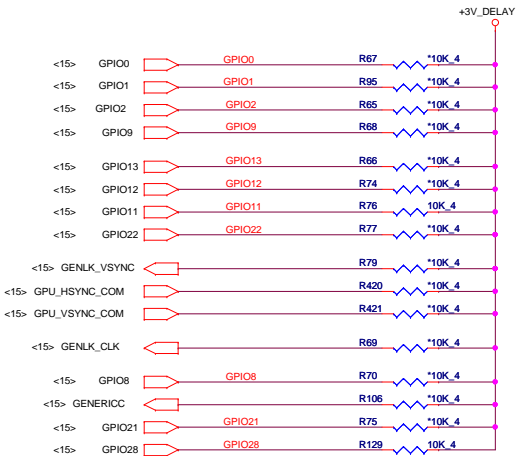
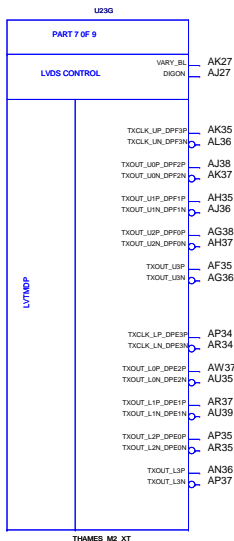
route 50ohms  
 single-ended/  
 100ohms diff and keep short



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**Quanta Computer Inc.**

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CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS  
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

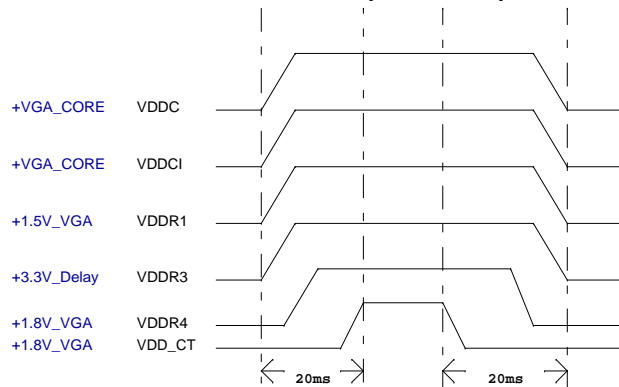
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% TX output swing 1: Full TX output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Mbit, M25P05A (ST) 101 - 1Mbit, V25P05A (ST) 101 - 4Mbit, V25P30 (ST) 101 - 8Mbit, V25P80 (ST) 101 - 512Kbit Pm25LV612 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

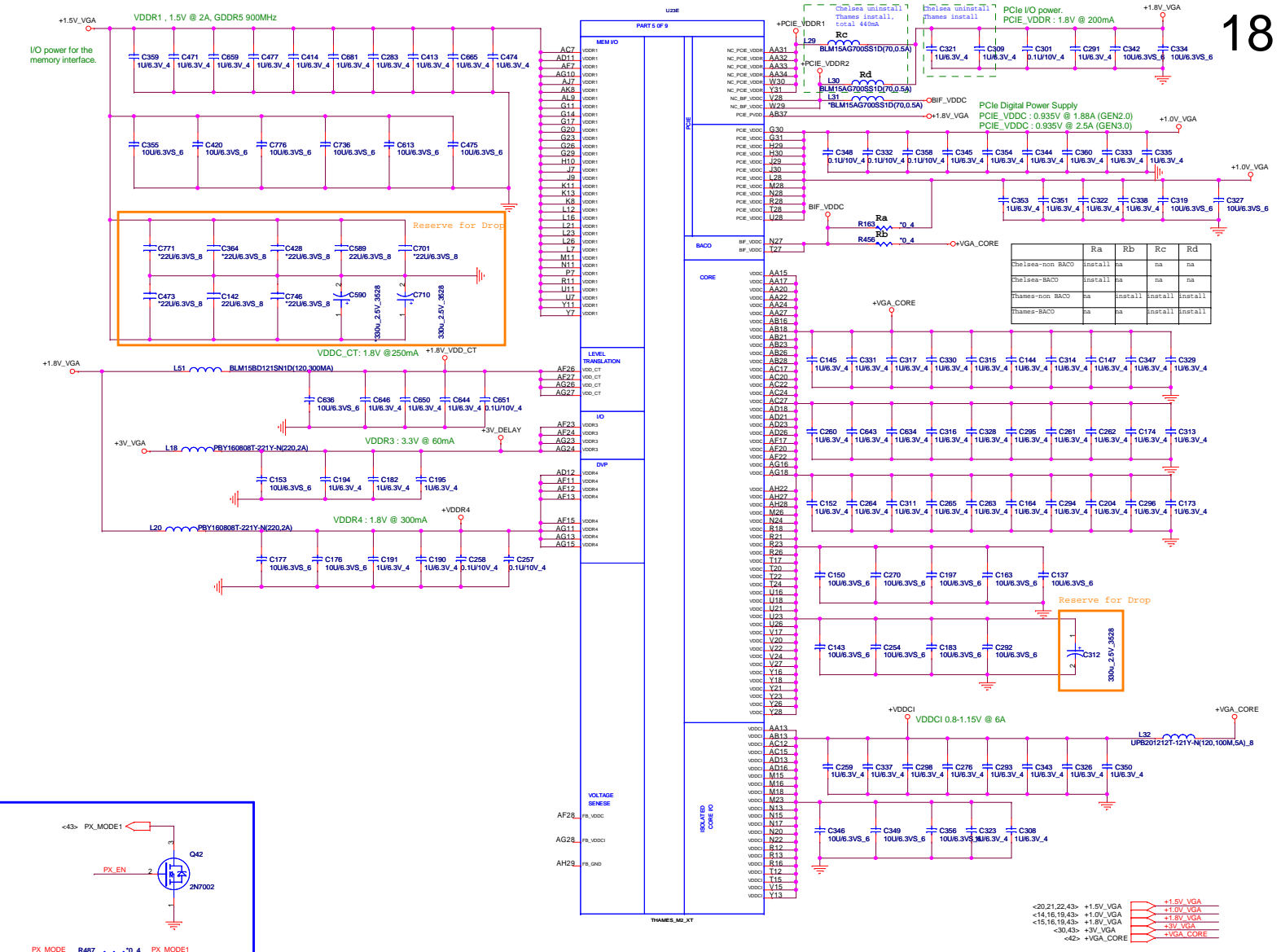
Power Up/Down Sequence



**PROJECT : R33**  
**Quanta Computer Inc.**

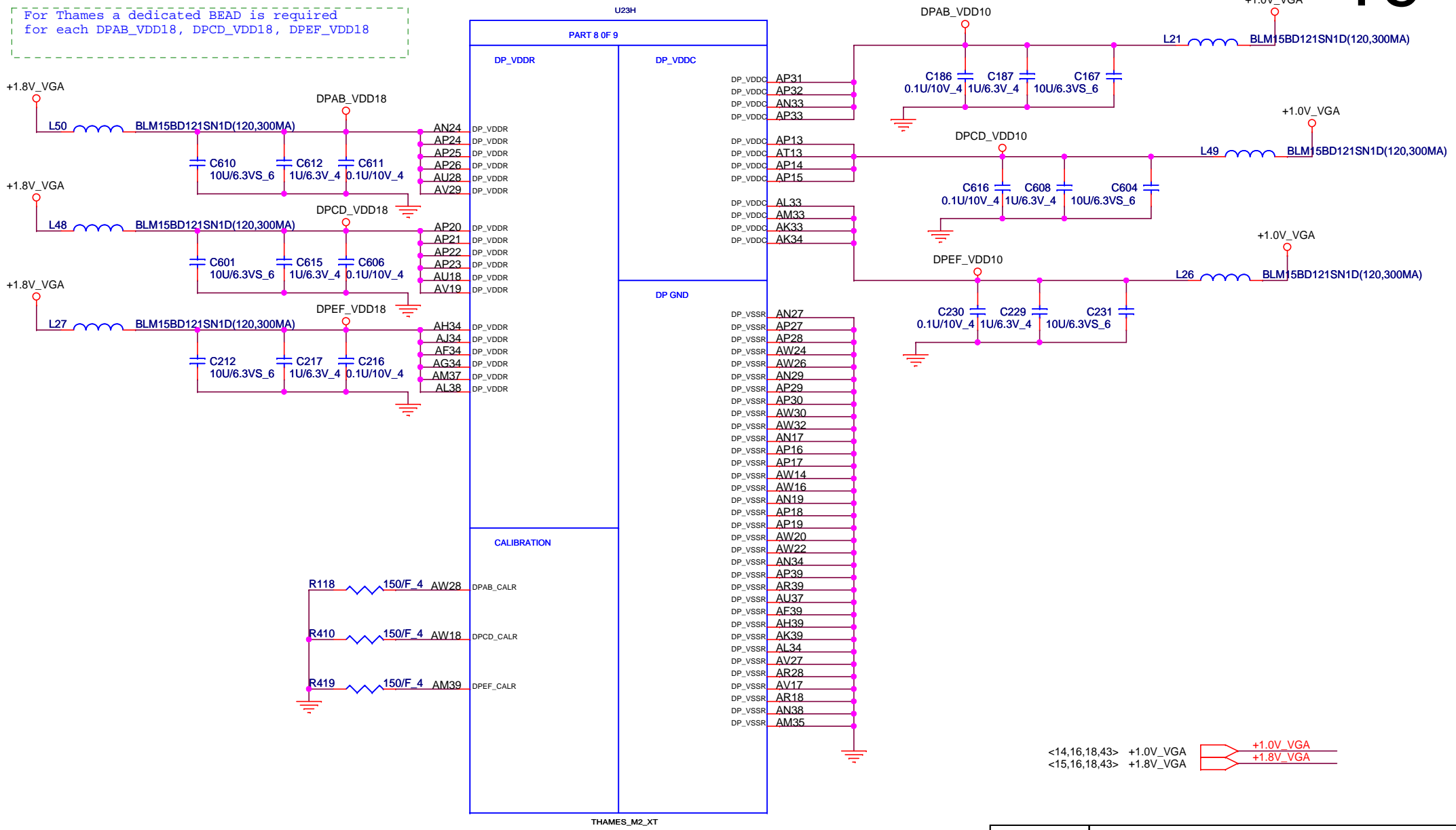
NB5

Size Custom	Document Number THAMES_LVDS / STRAP	Rev 1A
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For Thames a dedicated BEAD is required for each DPAB\_VDD18, DPCD\_VDD18, DPEF\_VDD18

For Thames a dedicated BEAD is required for each DPAB\_VDD10, DPCD\_VDD10, DPEF\_VDD10

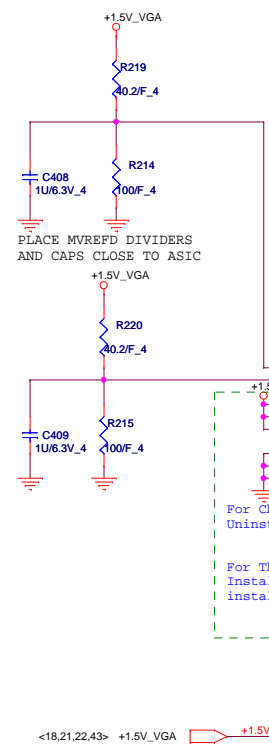
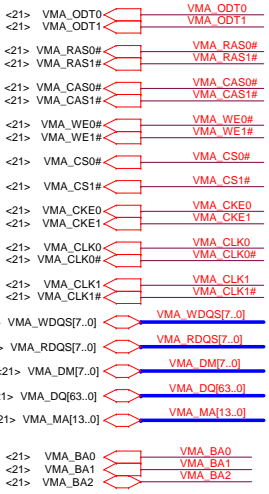


<14,16,18,43> +1.0V\_VGA  
 <15,16,18,43> +1.8V\_VGA



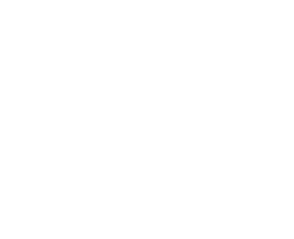
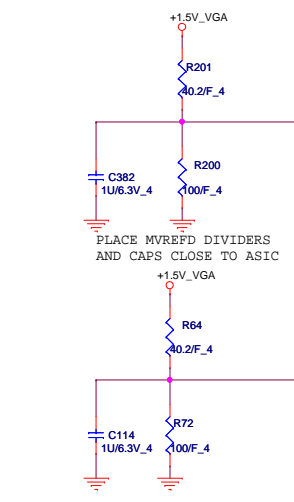
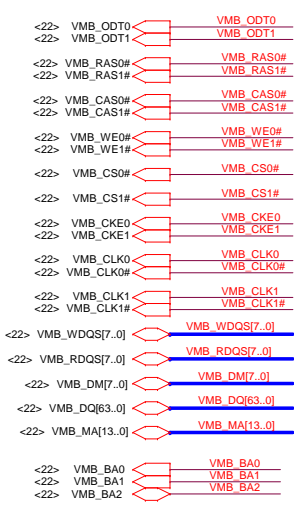
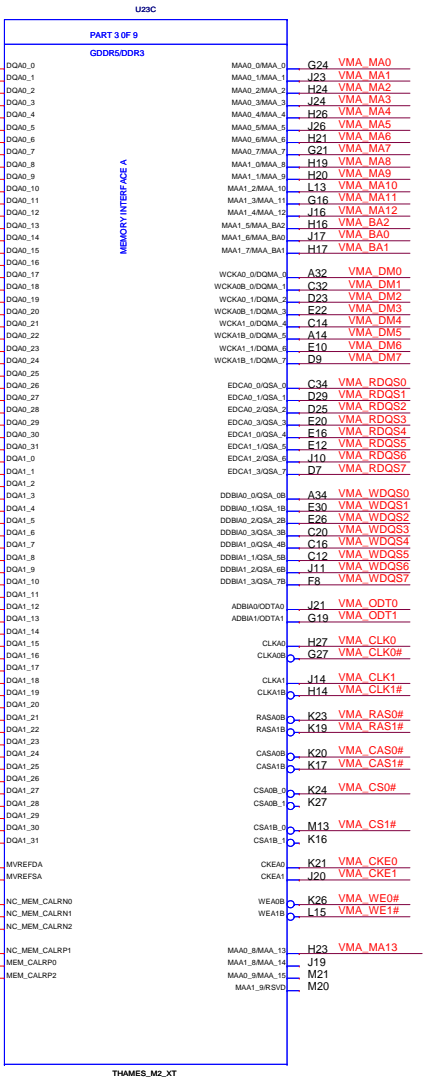
**PROJECT : R33**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>THAMES_DP Powers</b>	Rev 1A
Date: Wednesday, August 31, 2011		
Sheet 19 of 43		

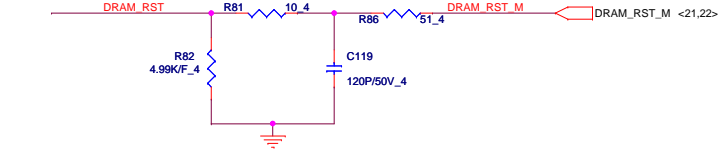
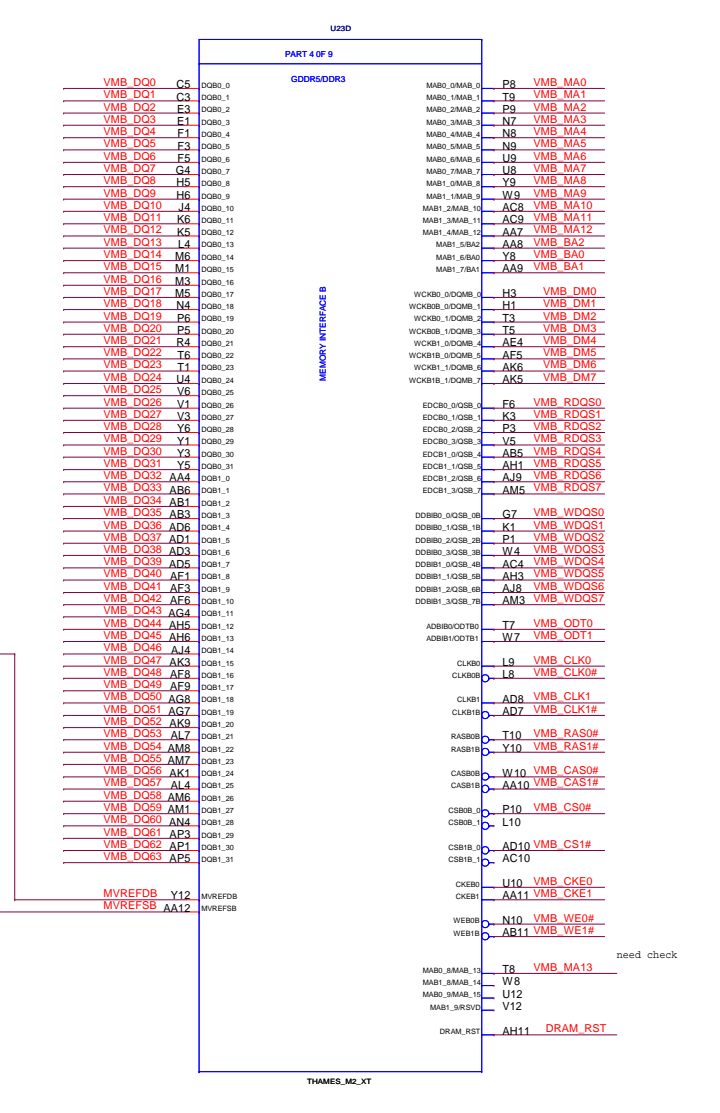


For Chelsea,  
Uninstall Ra, Rb, Rc and Rd

For Thames  
Install Ra, Rb, Rc and Rd  
install 240 Ohm for Re AND Rf



<18,21,22,43> +1.5V\_VGA



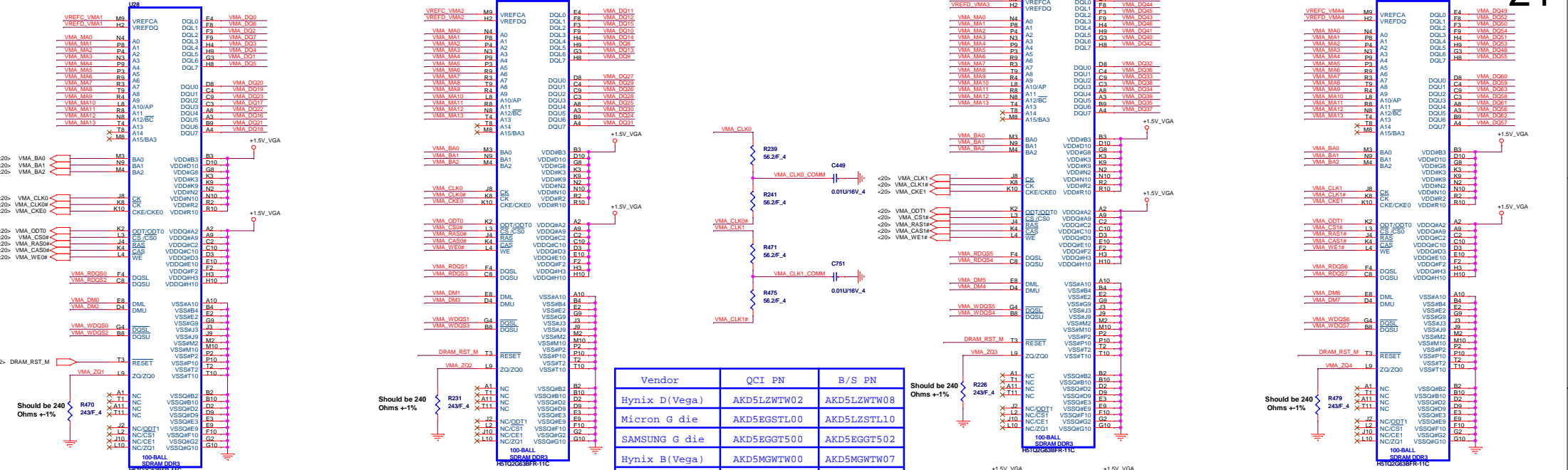
need check

**PROJECT : R33**  
**Quanta Computer Inc.**

Size: Custom  
Document Number: **THAMES\_MEM\_Interface**  
Date: Wednesday, August 31, 2011 | Sheet 20 of 43

Rev: 1A

# CHANNEL A: 256MB/512MB DDR3



Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

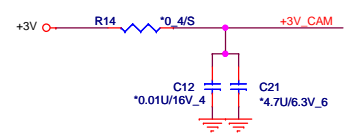
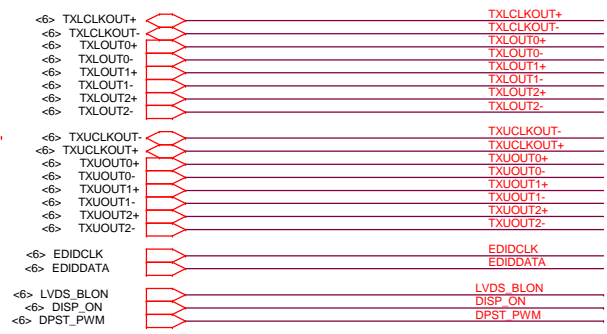
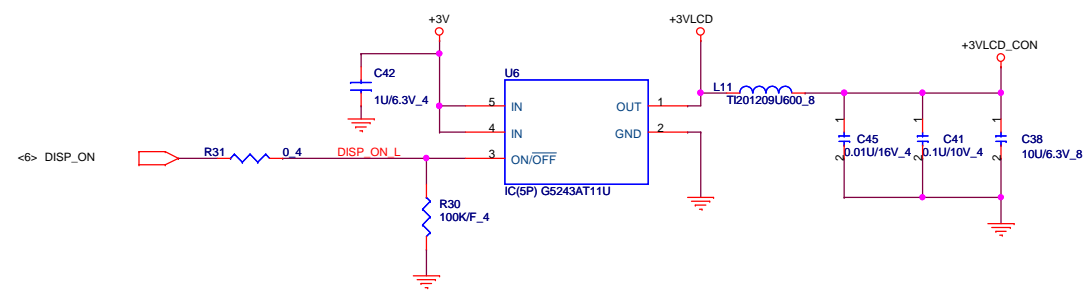
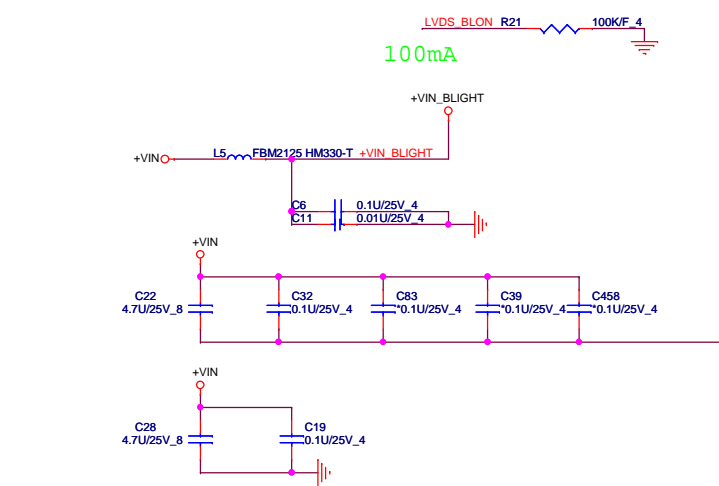
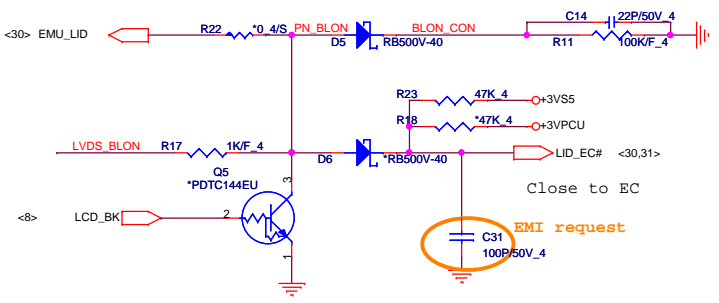
**PROJECT : R33**  
**Quantia Computer Inc.**

Site Custom    Document Number **VRAM-A (DDR3 BGA96)**    Rev 3A

Date: Wednesday, August 31, 2011    Sheet 21 of 43



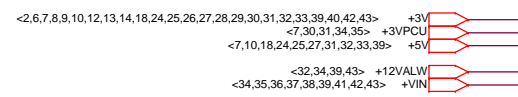
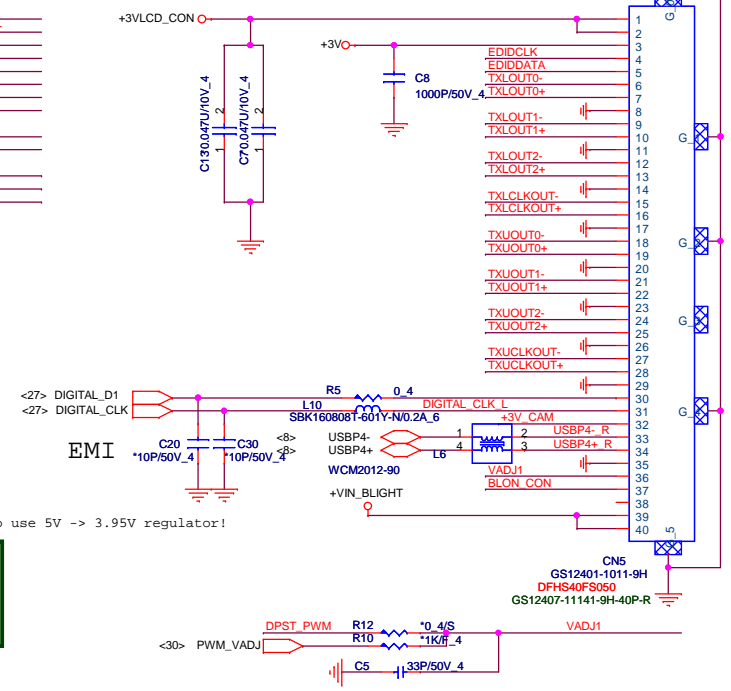
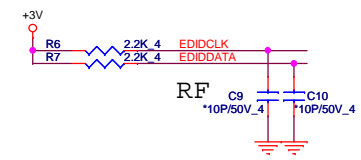
# LID Switch



Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L6 location

- USBP4- R8 \*0.4 USBP4- R
- USBP4+ R9 \*0.4 USBP4+ R

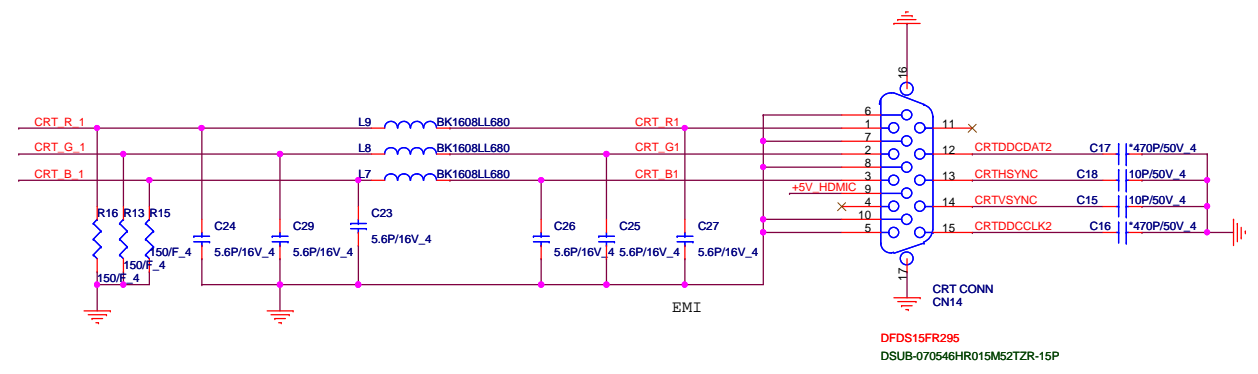


**PROJECT : R33**  
**Quanta Computer Inc.**

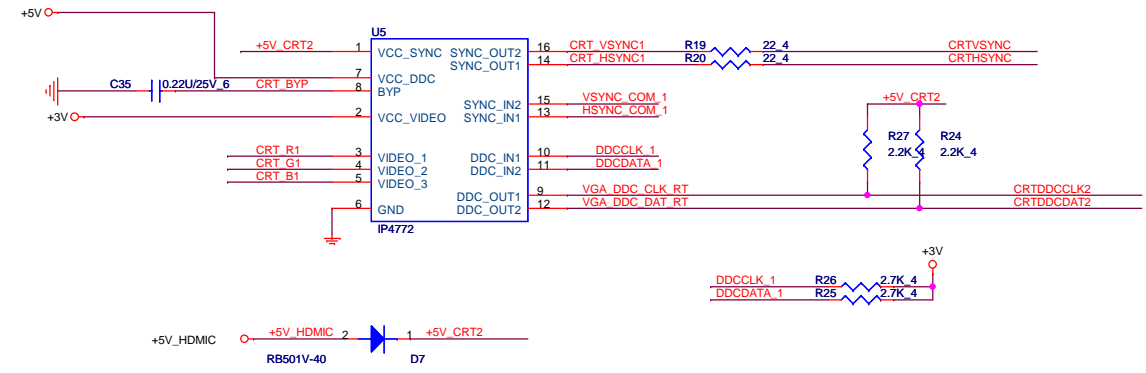
Size Custom Document Number LCD CONN/LID/CAM Rev 1A

Date: Wednesday, August 31, 2011 11:43 AM

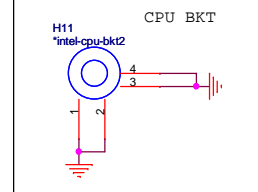
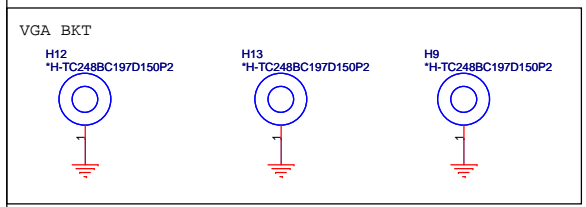
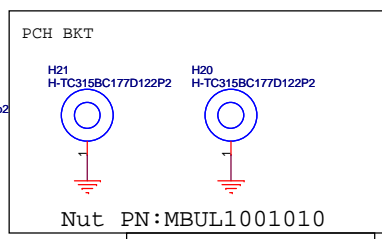
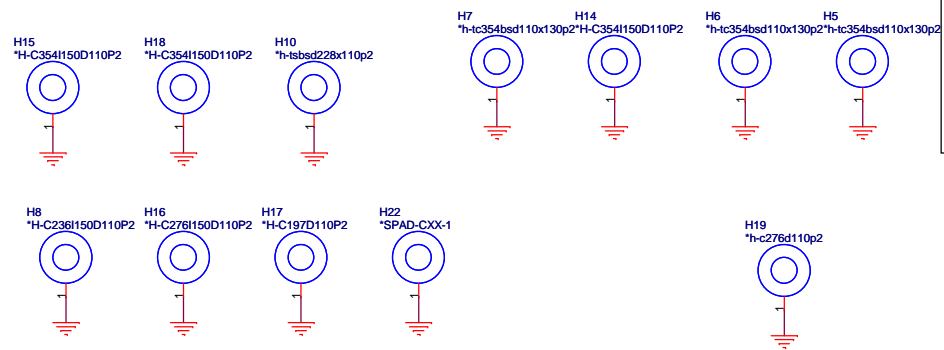
CRT PORT



- <6> CRT\_R
  - <6> CRT\_G
  - <6> CRT\_B
  - <6> HSYNC\_COM
  - <6> VSYNC\_COM
  - <6> DDCCLK
  - <6> DDCDATA
- CRT\_R\_1
  - CRT\_G\_1
  - CRT\_B\_1
  - HSYNC\_COM\_1
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  - DDCCLK\_1
  - DDCDATA\_1



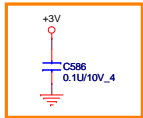
HOLE



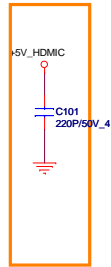
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	Size Custom	Document Number <b>CRT_Hole</b>
Date: Wednesday, August 24, 2011   Sheet 24 of 43		



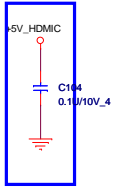
EMI request



Add for EMI



EMI request

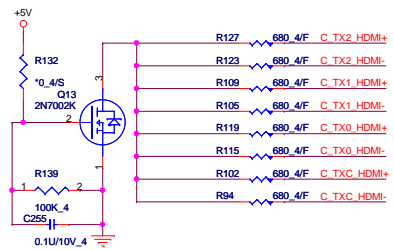
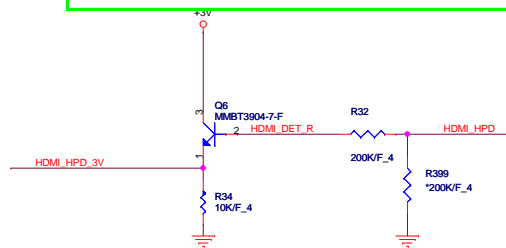
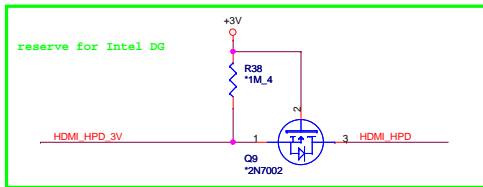
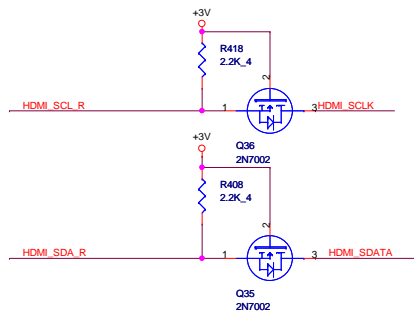


close to HDMI conn

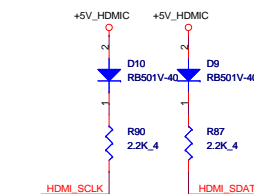
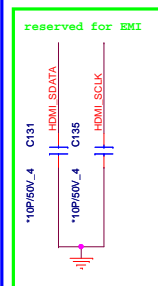
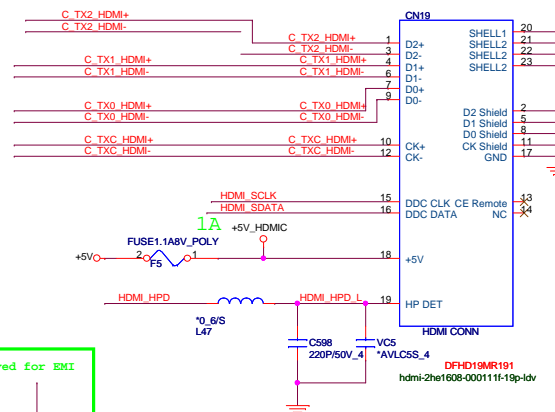
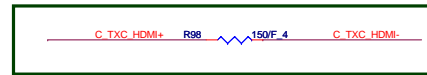
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<6>	IN_DO#	IN_DO#	C180	0.1u/10V_4	C TX0 HDMI-
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<6>	IN_D1	IN_D1	C169	0.1u/10V_4	C TX1 HDMI+
<6>	IN_D2#	IN_D2#	C200	0.1u/10V_4	C TX2 HDMI-
<6>	IN_D2	IN_D2	C210	0.1u/10V_4	C TX2 HDMI+



DISCRETE HDMI I2C SELECT  
Close to HDMI Connector



EMI request



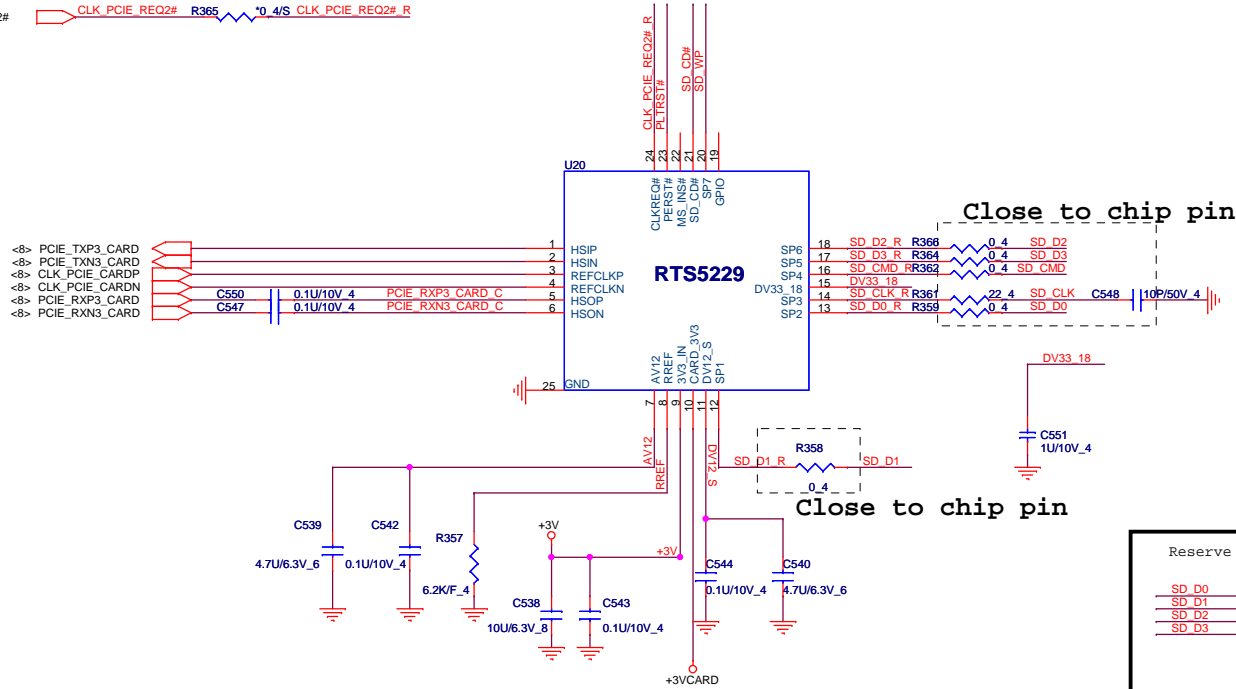
**PROJECT : R33**  
**Quanta Computer Inc.**

Size Custom Document Number **HDMI CONN** Sheet 25 of 43

Date: Wednesday, August 24, 2011

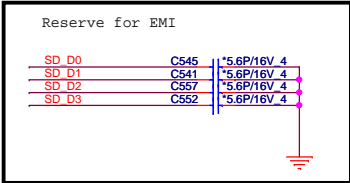
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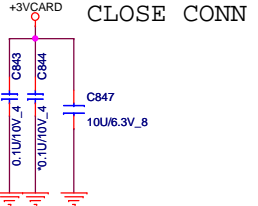
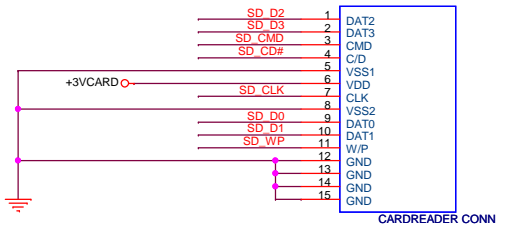



Close to chip pin

Close to chip pin

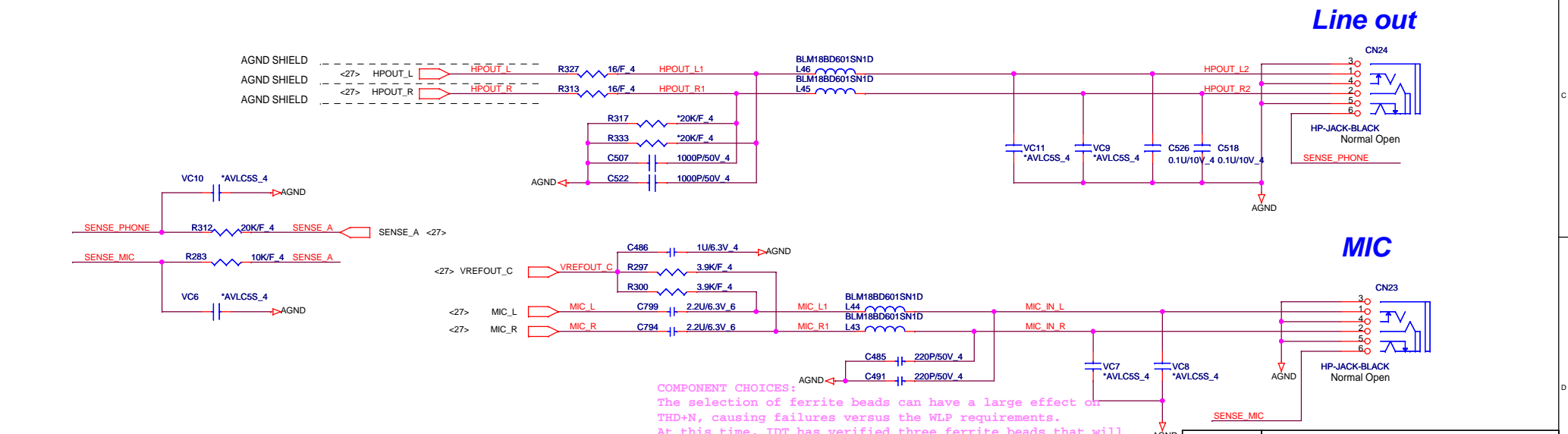
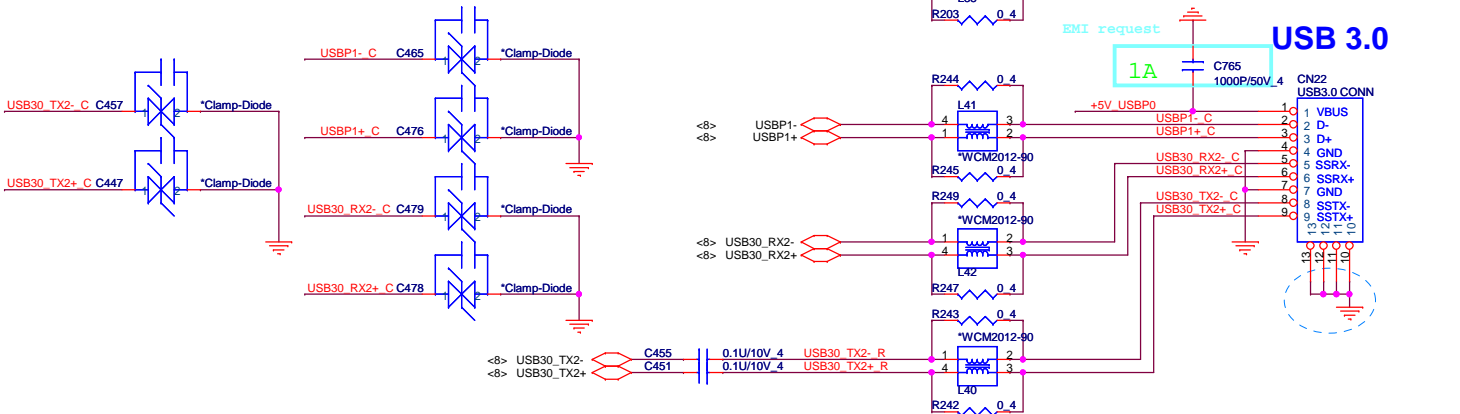
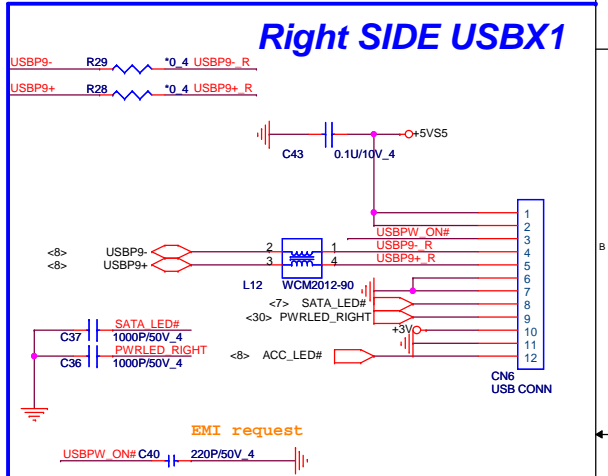
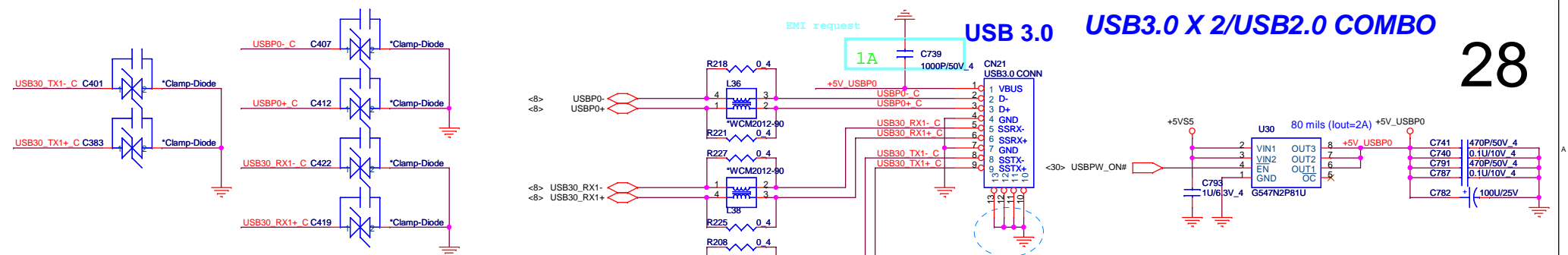


### SD / MMC CARD READER




	<b>PROJECT : R33</b> Quanta Computer Inc.	
	Size Custom Document Number <b>RTS5229 &amp; CR SOCKET</b>	Rev 1A
Date: Thursday, August 25, 2011		Sheet 26 of 43





**COMPONENT CHOICES:**  
 The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements. At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:  
 Murata: BLM18BD601SN1  
 TDK: MMZ1608Y601BTA  
 Taiyo Yuden: LF BK 1608HM601-T

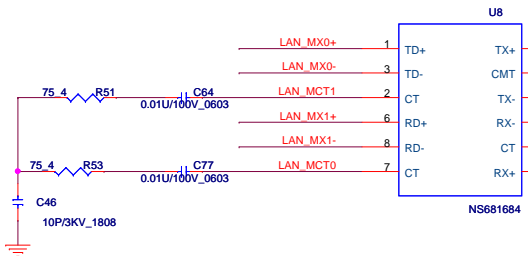
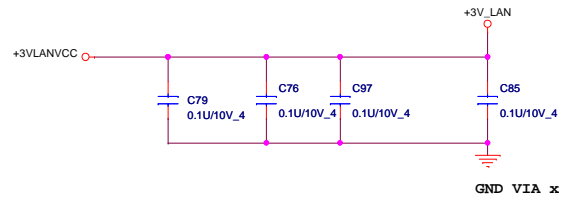
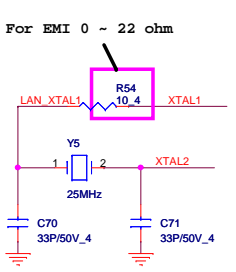


**NB5**

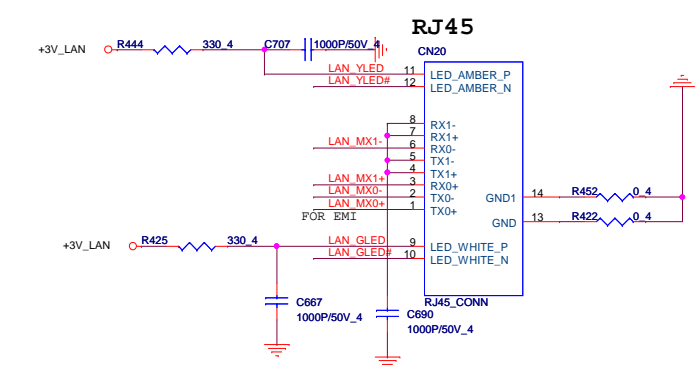
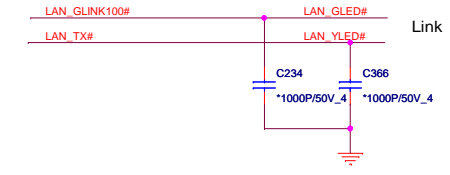
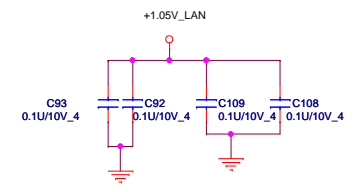
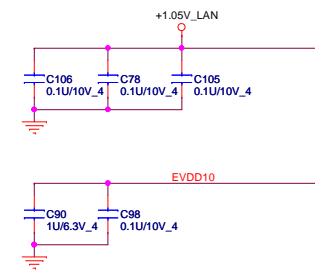
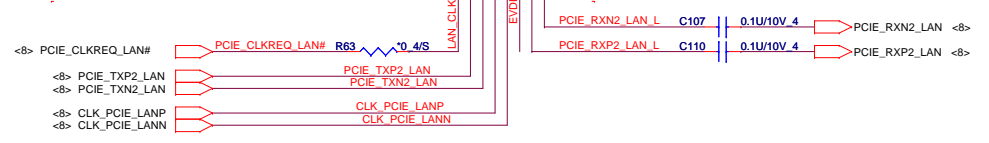
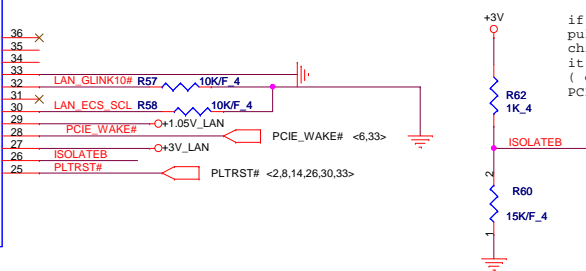
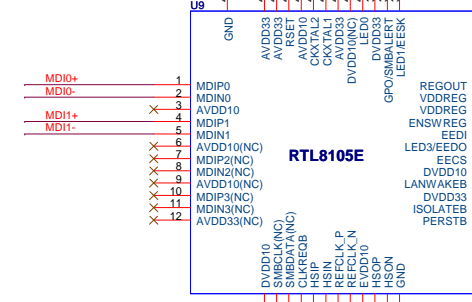
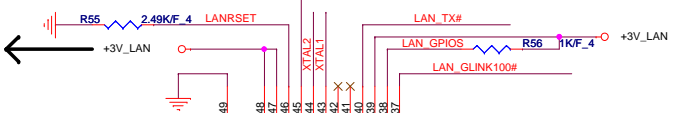
**PROJECT : R33**  
 Quanta Computer Inc.

Rev 1A

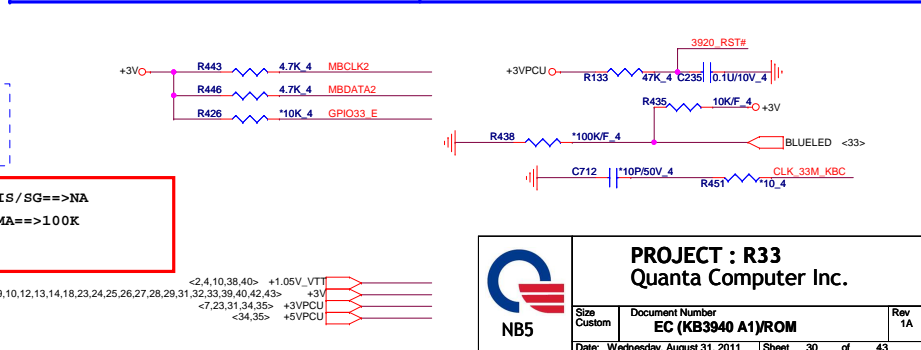
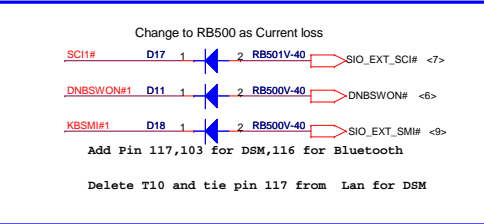
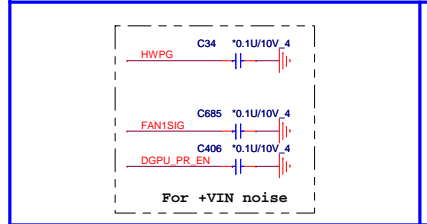
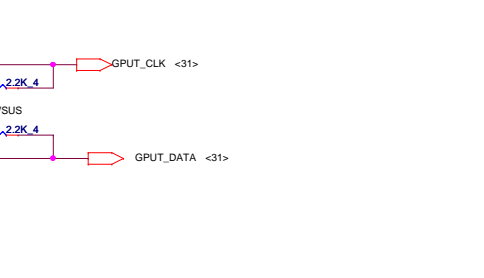
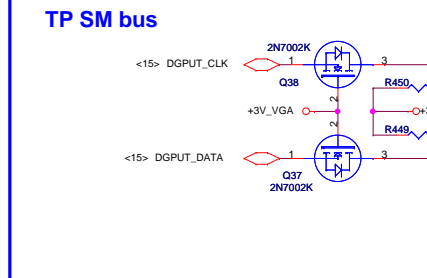
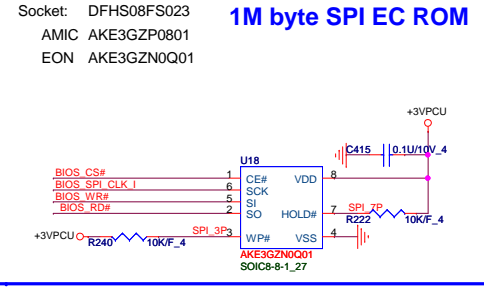
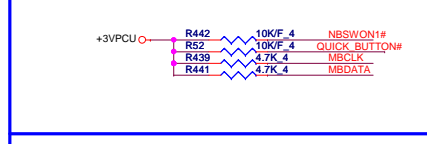
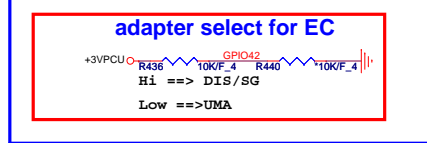
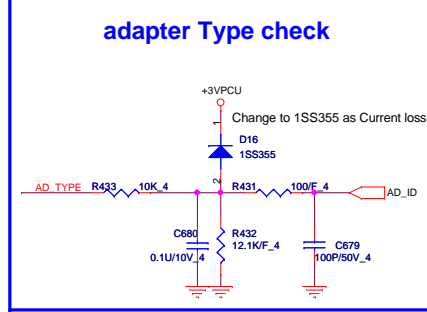
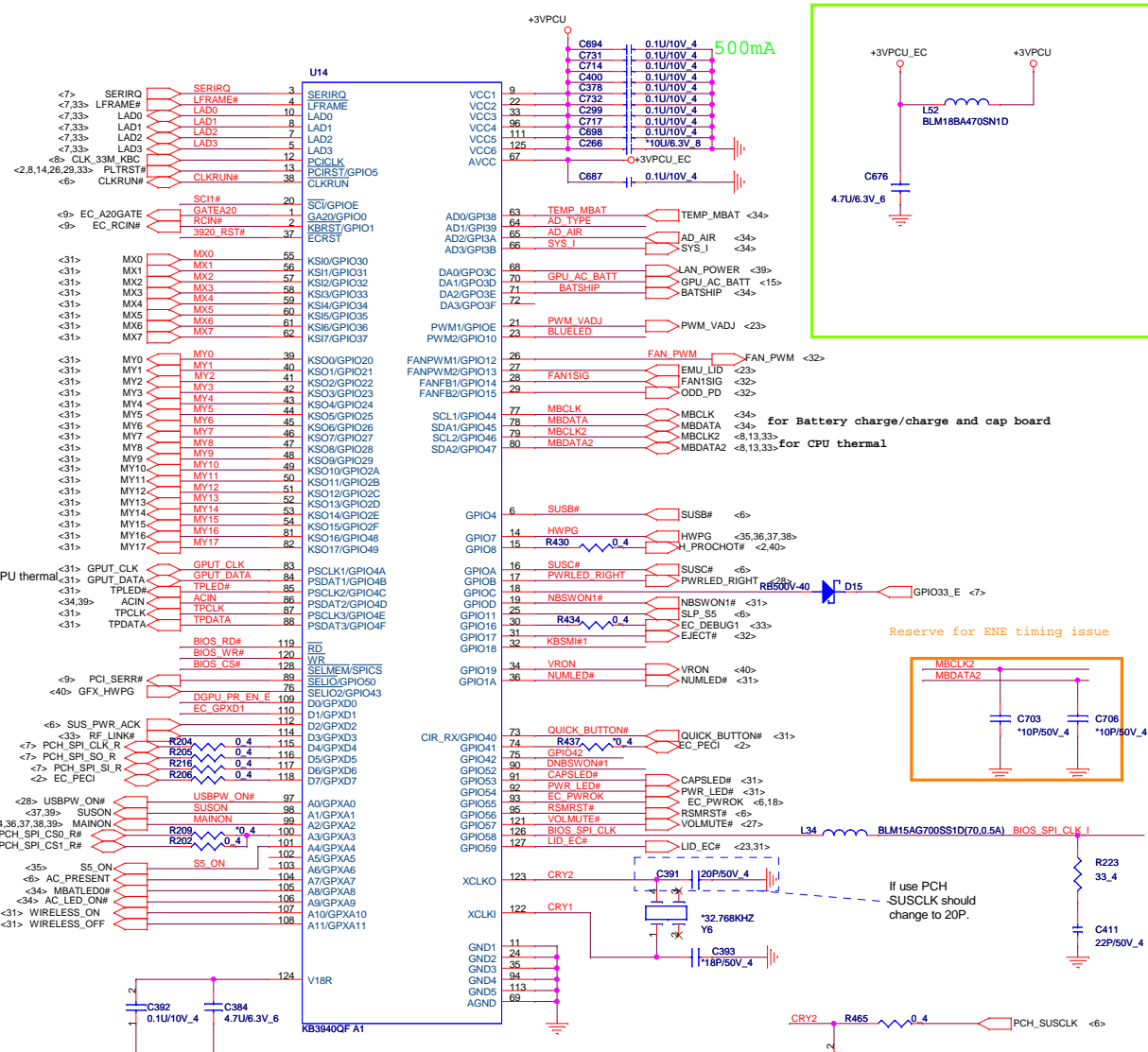
Size Custom	Document Number <b>USB/BT/Audio Jack</b>	Date: Monday, August 29, 2011
Sheet 28 of 43		

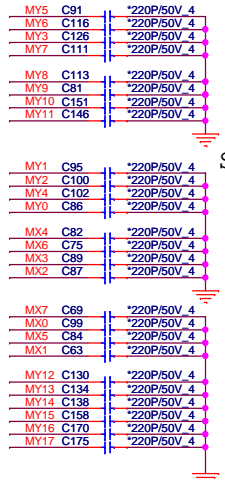


GND VIA x 9 Pcs

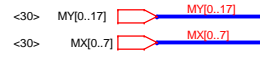
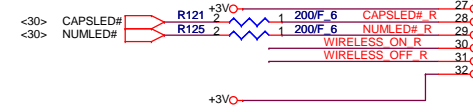


	<b>PROJECT : R33</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number <b>RTL 8105E/RJ45</b>
Date: Wednesday, August 24, 2011   Sheet 29 of 43		

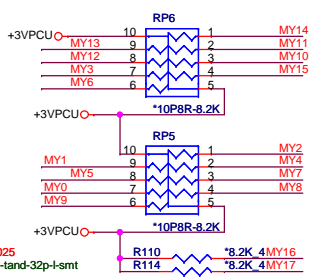




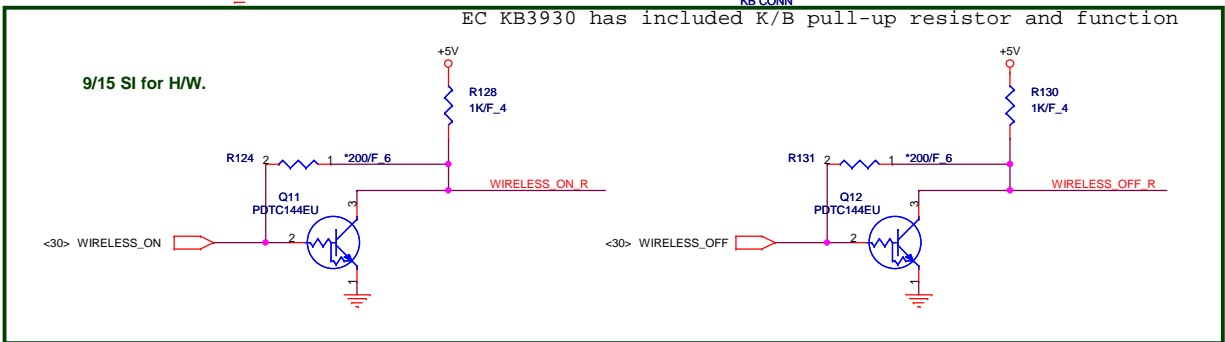
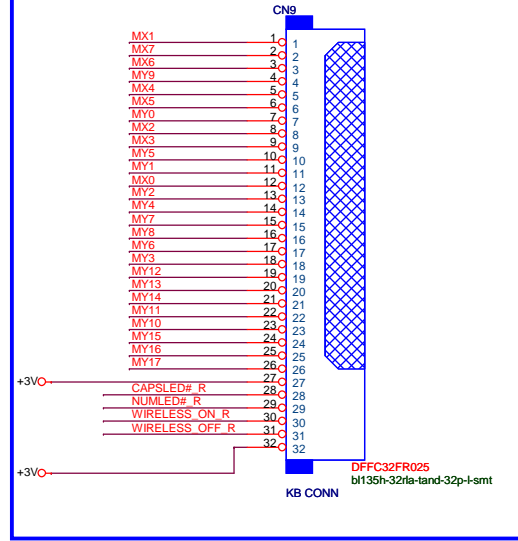
SI un-install



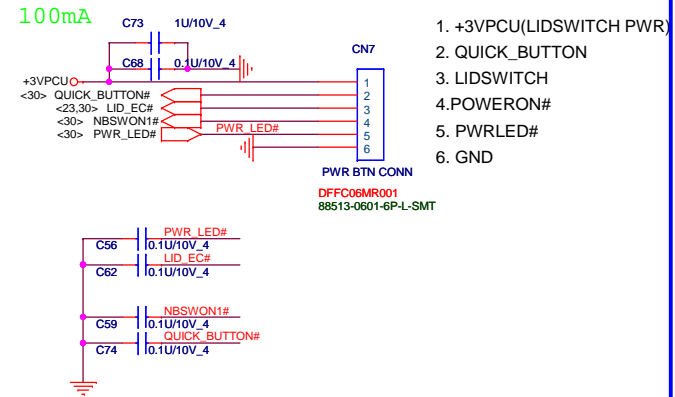
KEYBOARD PULL-UP



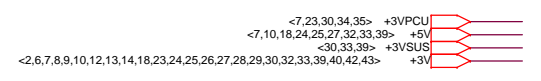
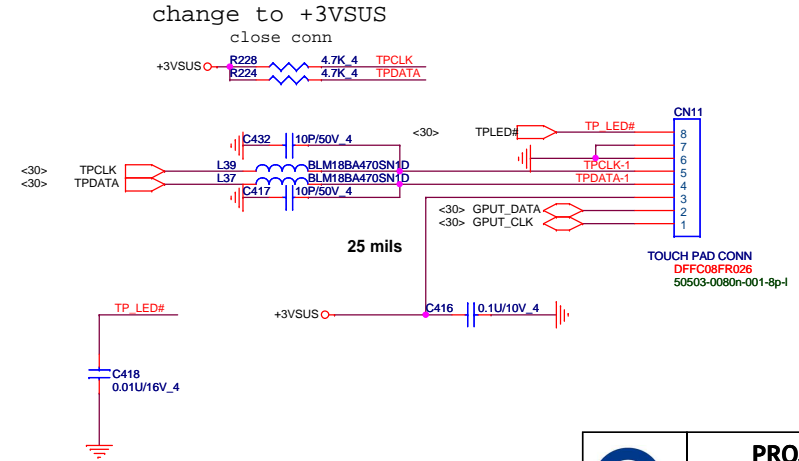
KEYBOARD Con.  
Co-layout for 17" only



POWER BUTTON CONNECT



TOUCH PAD Con.



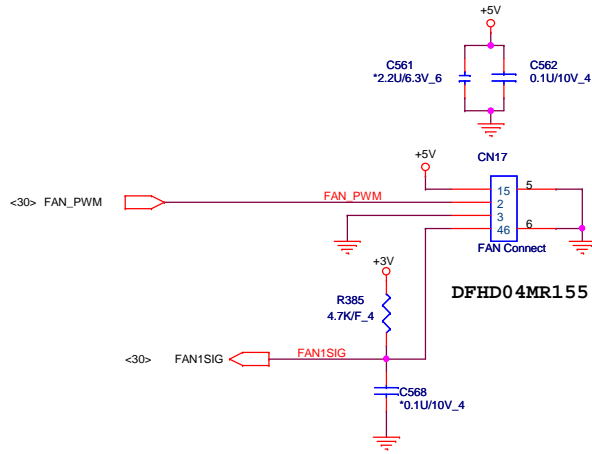
**PROJECT : R33**  
**Quanta Computer Inc.**

Size Custom Document Number  
**LED/KB/SW/TP**

Date: Wednesday, August 24, 2011 1:58pm 31 of 43

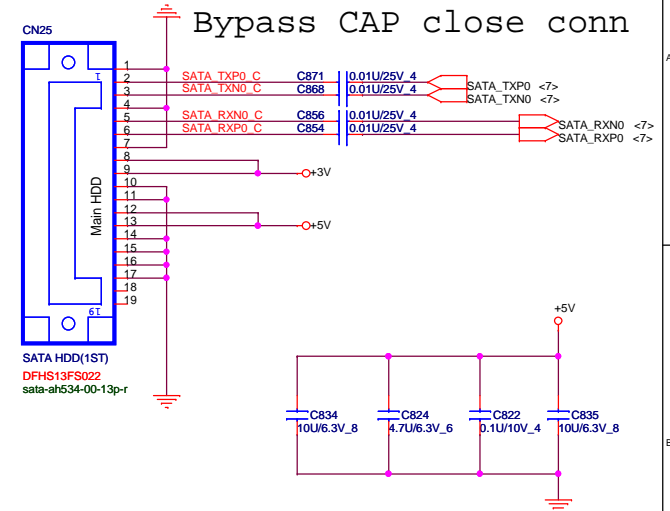
Rev 1A

# CPU FAN

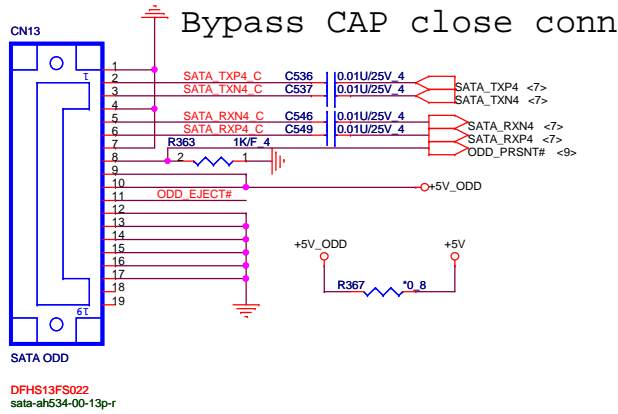


# SATA HDD CONNECTOR

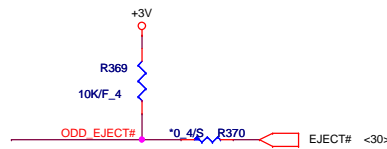
32



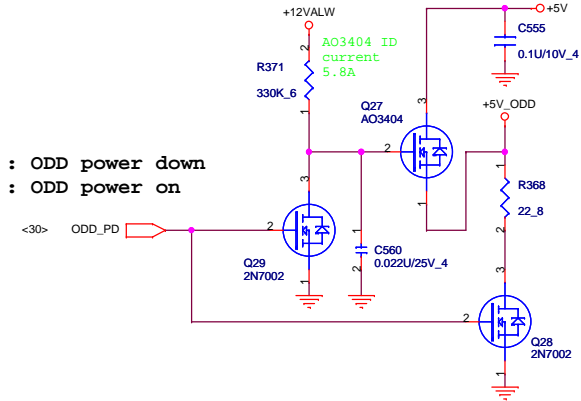
# SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



High : ODD power down  
Low : ODD power on

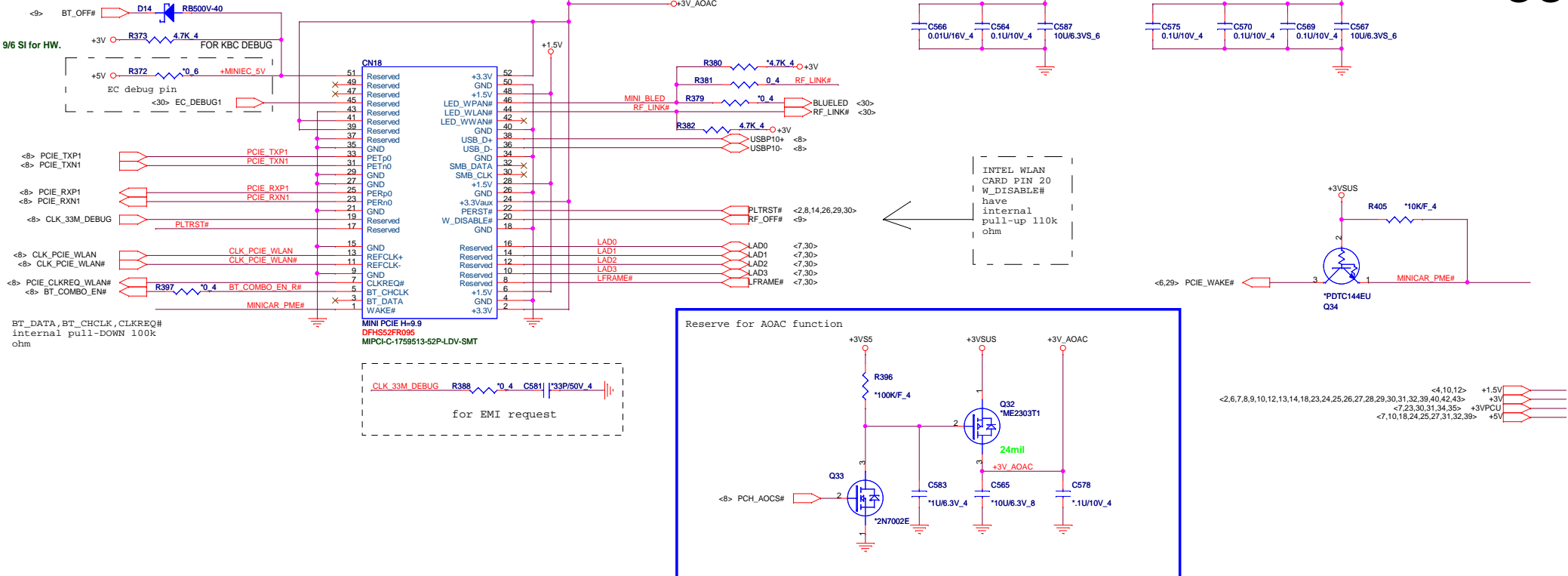


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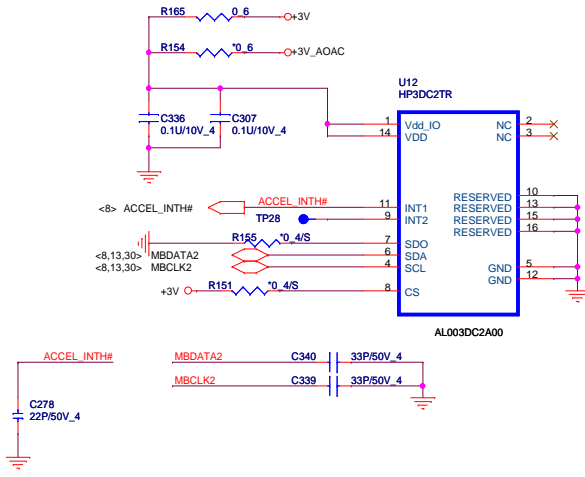
Size Custom	Document Number HDD/ODD/FAN	Rev 1A
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# Mini PCI-E Card 1 WLAN



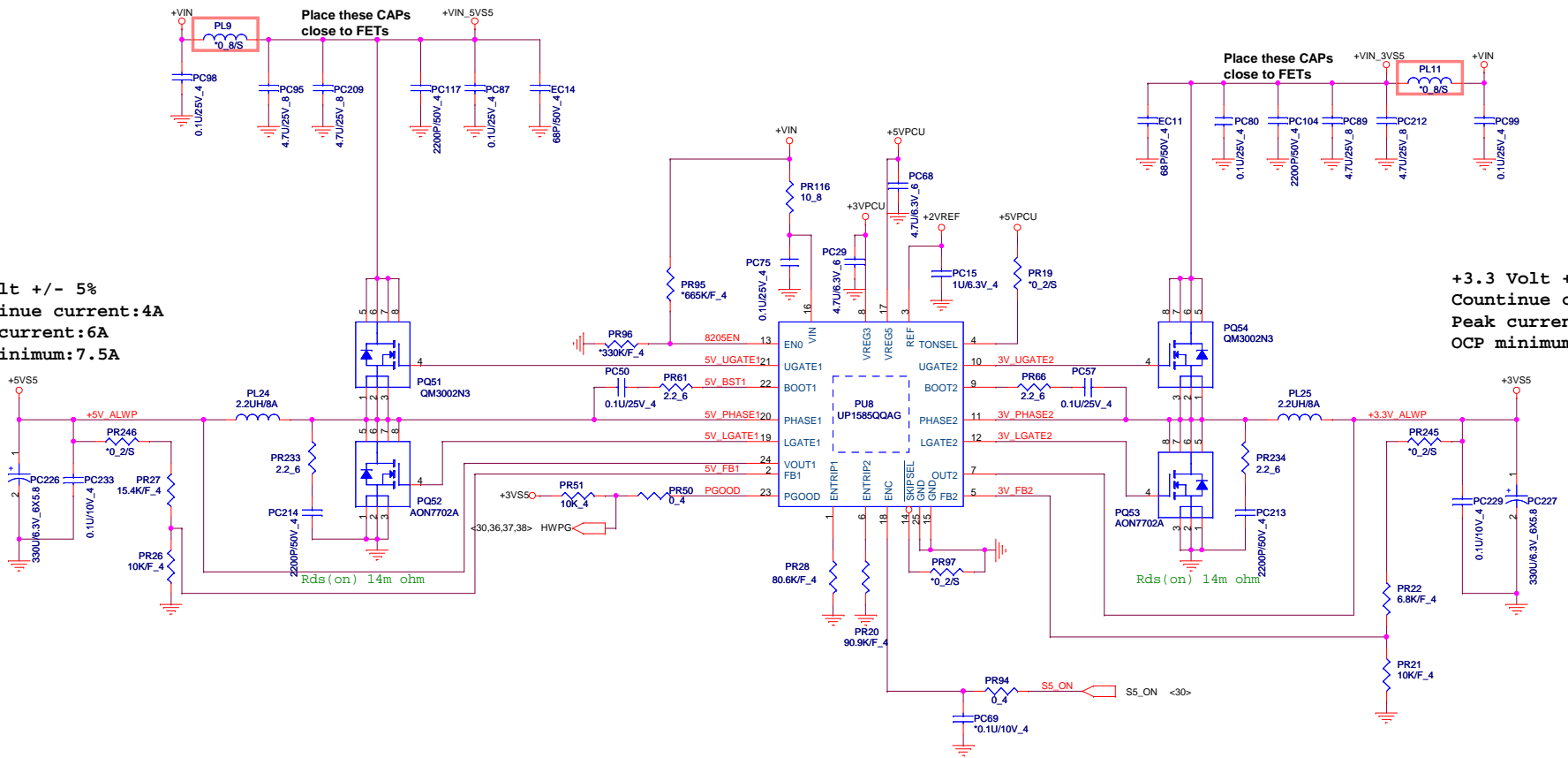
# Accelerometer Sensor



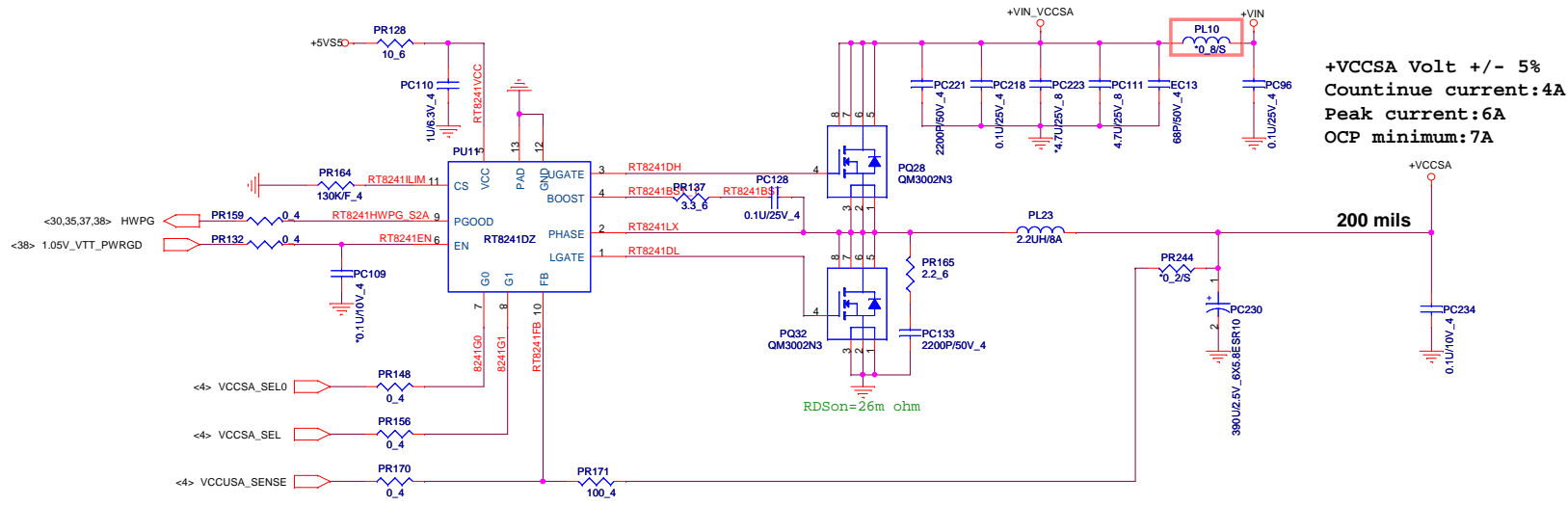


**+5 Volt +/- 5%**  
**Countinue current:4A**  
**Peak current:6A**  
**OCP minimum:7.5A**

**+3.3 Volt +/- 5%**  
**Countinue current:4A**  
**Peak current:6A**  
**OCP minimum:7.5A**

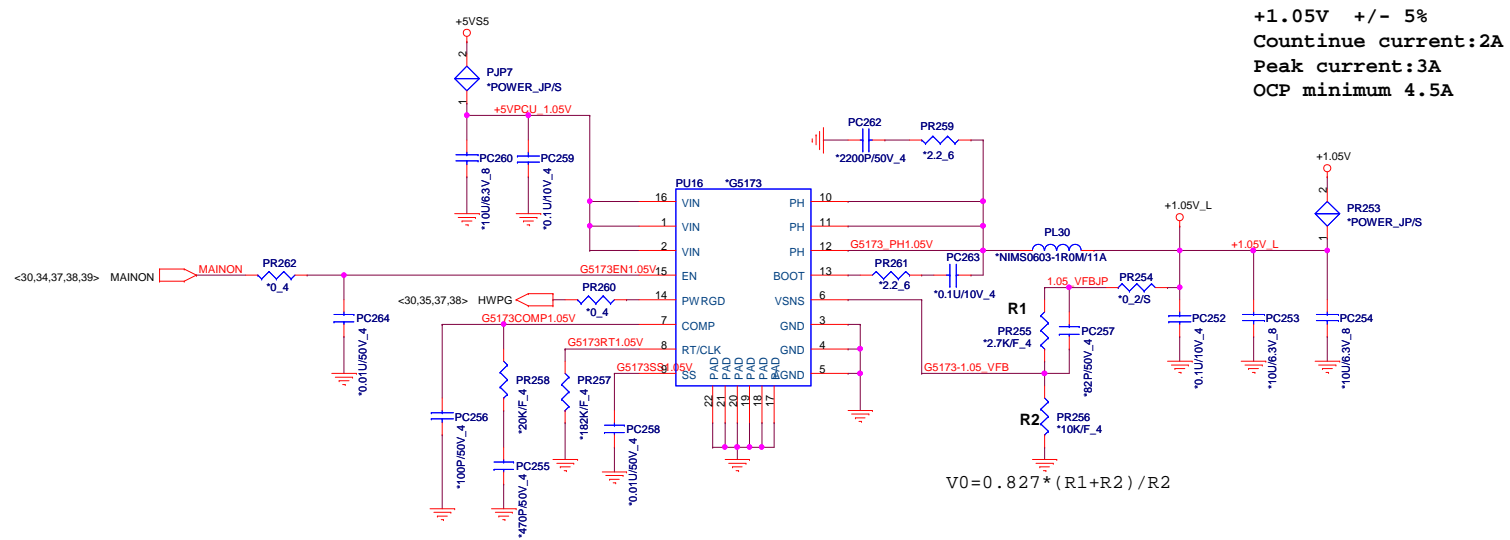


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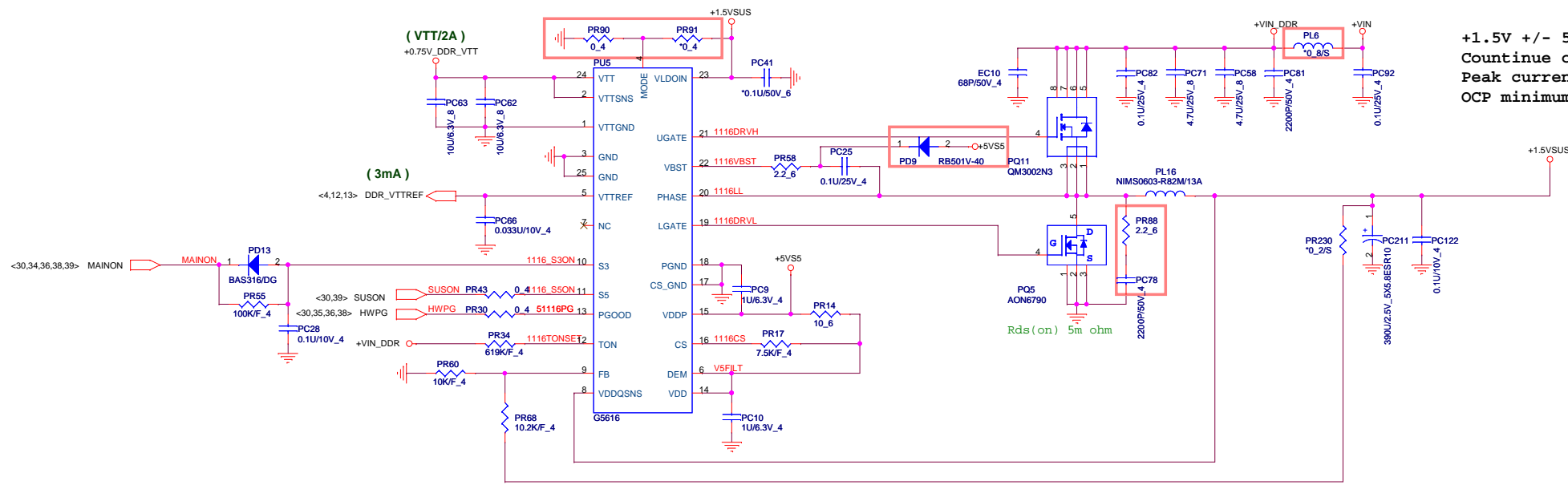


**CPU system agent voltage slew rate of 0.5 -10 mV/μs**


H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.80V (SV-RT8241DZGQW) 0.85V (LV-RT8241EZGQW)
1	0	0.725V
1	1	0.675V

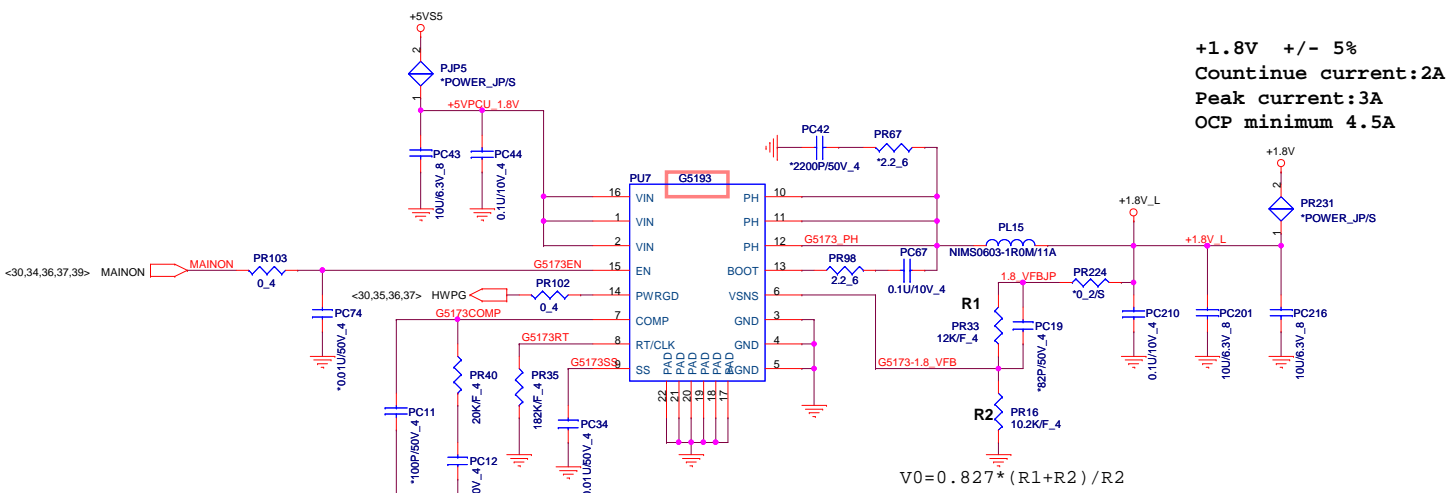
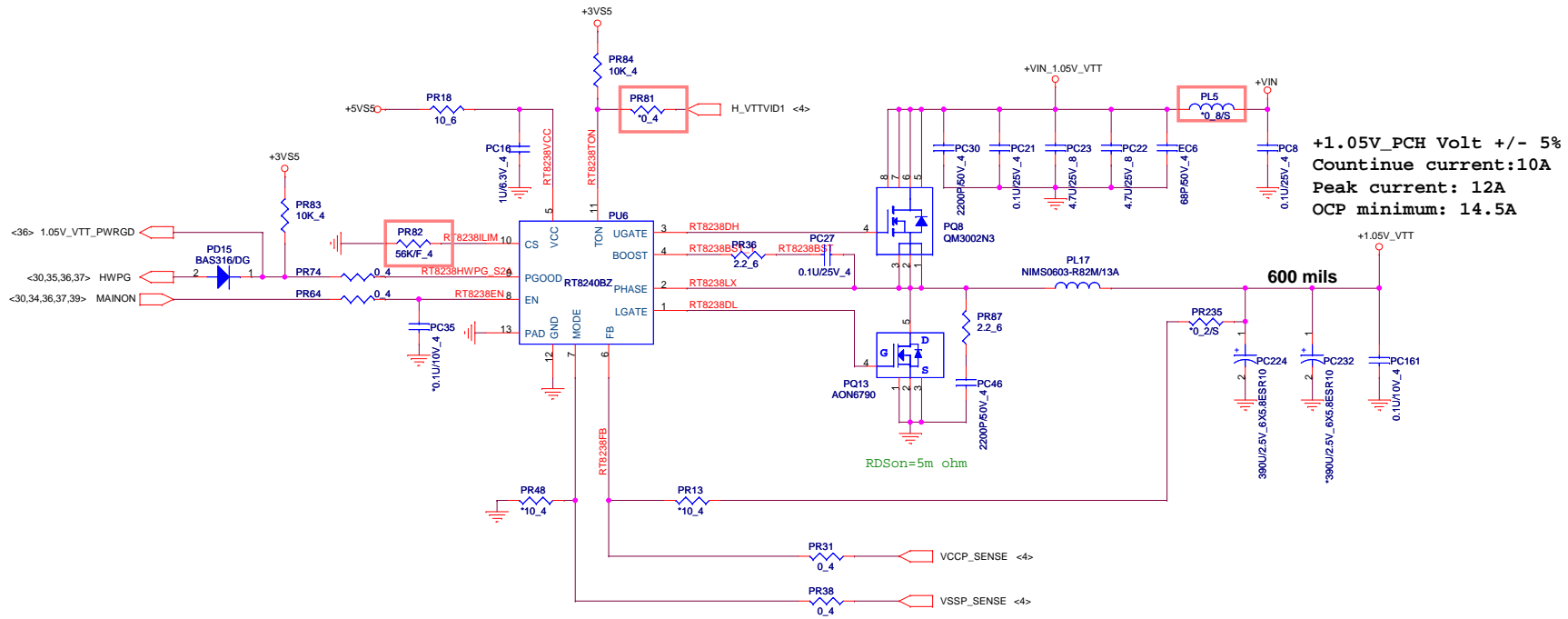


	<b>PROJECT : R33</b>		Date: Monday, August 29, 2011
	Quanta Computer Inc.		
	Size Custom Document Number VCCSA (RT8241EZ) Date:	Rev 1A Sheet 36 of 43	

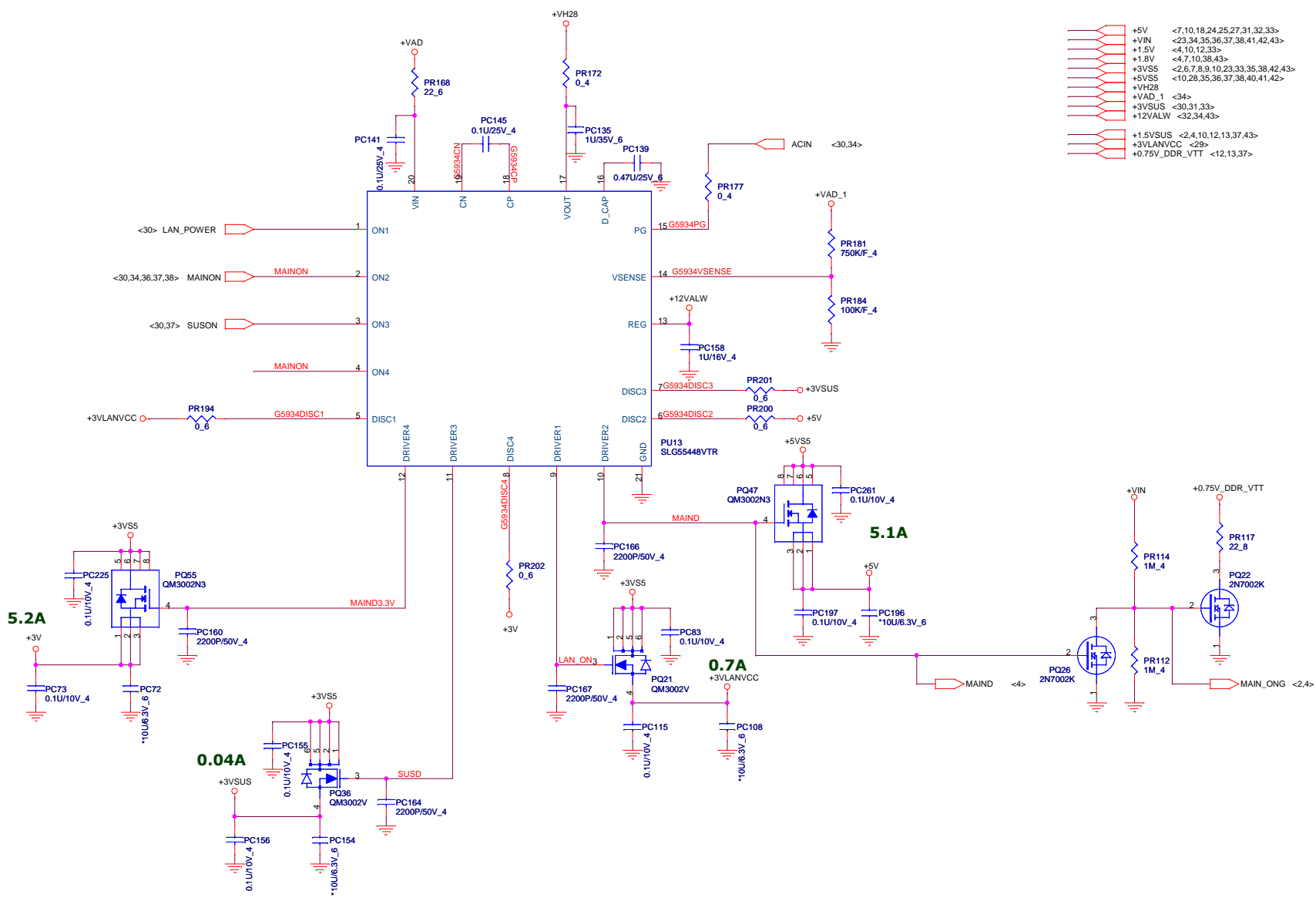


+1.5V +/- 5%  
 Countinue current:10A  
 Peak current:12A  
 OCP minimum 15A


	<b>PROJECT : R33</b> Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	<b>DDRIII(RT8207LGQW)</b>	1A
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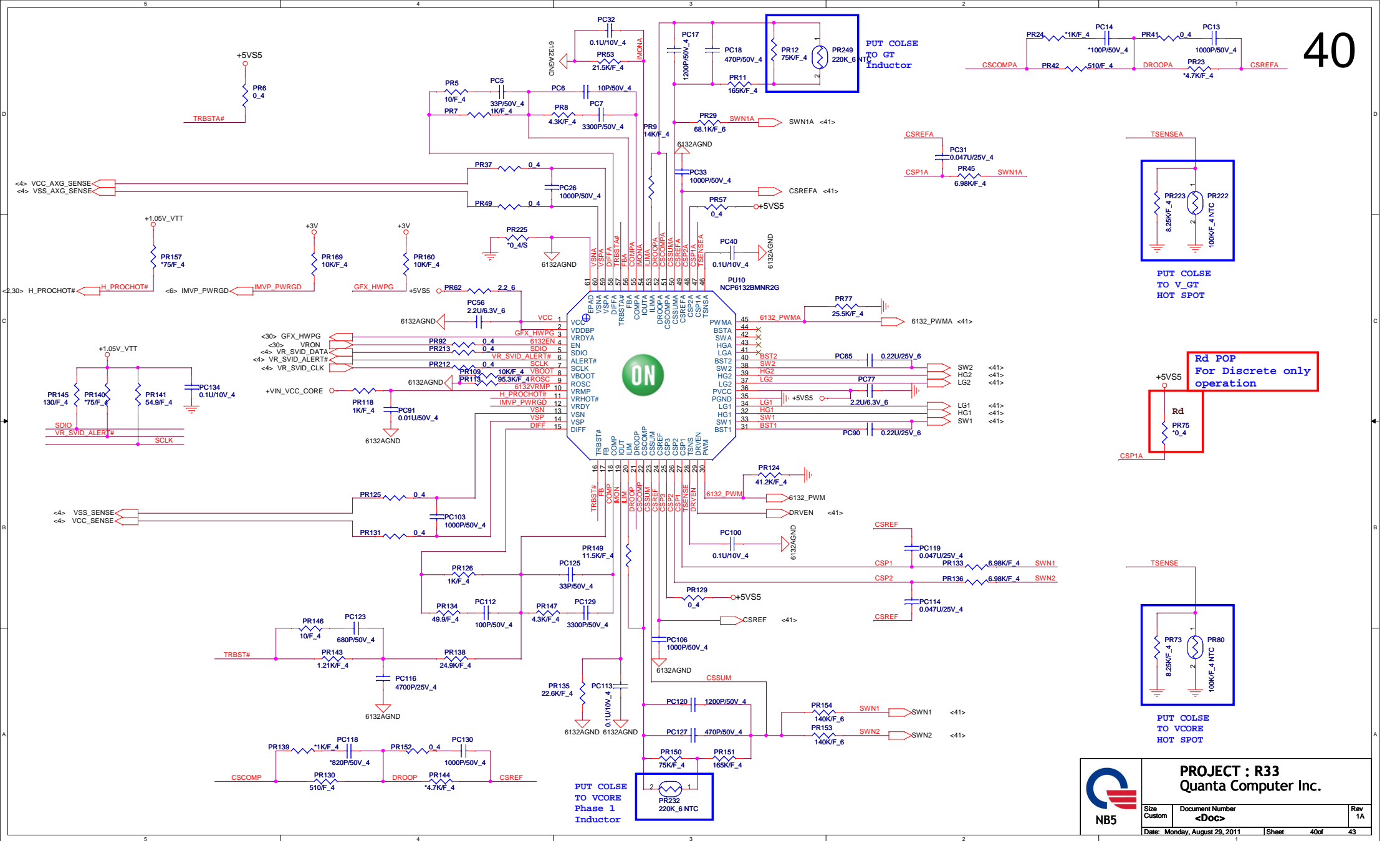


	<b>PROJECT : R33</b>		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number <b>1.0V(RT8228BZ)/1.8V(G5173)</b>	
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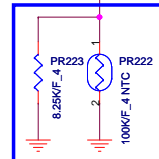


- +5V <7,10,18,24,25,27,31,32,33>
- +VIN <23,34,35,36,37,38,41,42,43>
- +1.5V <4,10,12,33>
- +1.8V <4,7,10,38,43>
- +3VS5 <2,6,7,8,9,10,23,33,35,38,42,43>
- +5VS5 <10,28,35,36,37,38,40,41,42>
- +VH28
- +VAD\_1 <34>
- +3VSUS <30,31,33>
- +12VALW <32,34,43>
- +1.5VSUS <2,4,10,12,13,37,43>
- +3VLAVCC <29>
- +0.75V\_DDR\_VTT <12,13,37>

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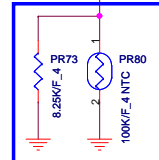
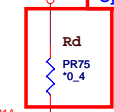


PUT COLSE  
TO GT  
Inductor



PUT COLSE  
TO V\_GT  
HOT SPOT

Rd POP  
For Discrete only  
operation



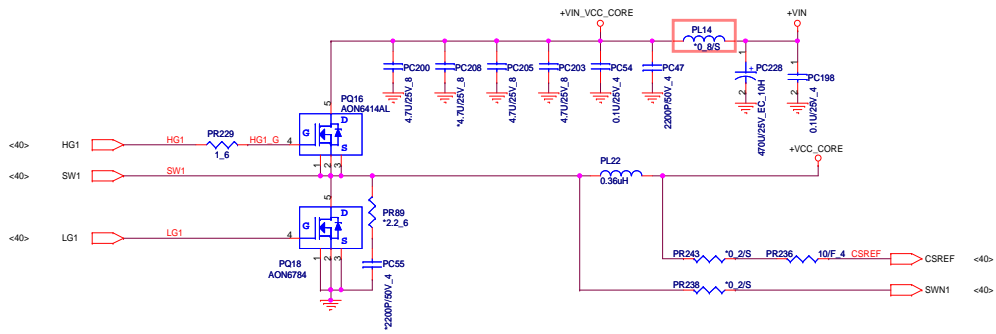
PUT COLSE  
TO VCORE  
HOT SPOT

PUT COLSE  
TO VCORE  
Phase 1  
Inductor

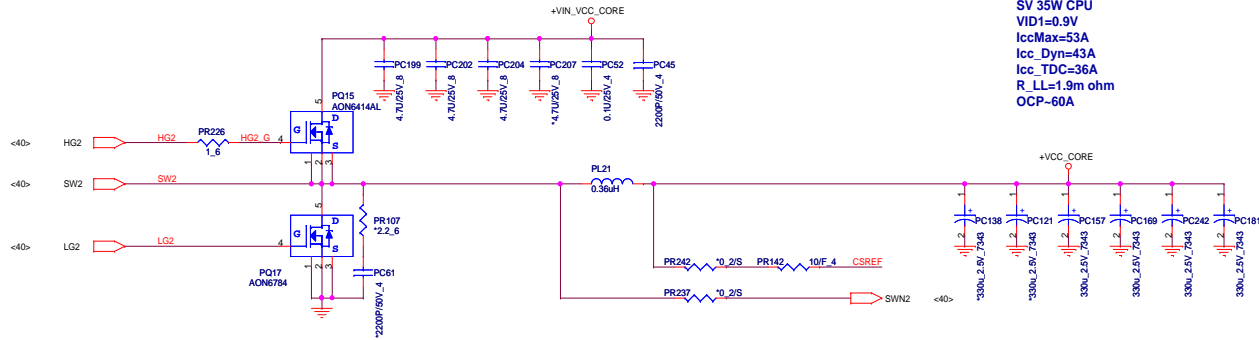


	<b>PROJECT : R33</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <Doc>	Rev 1A
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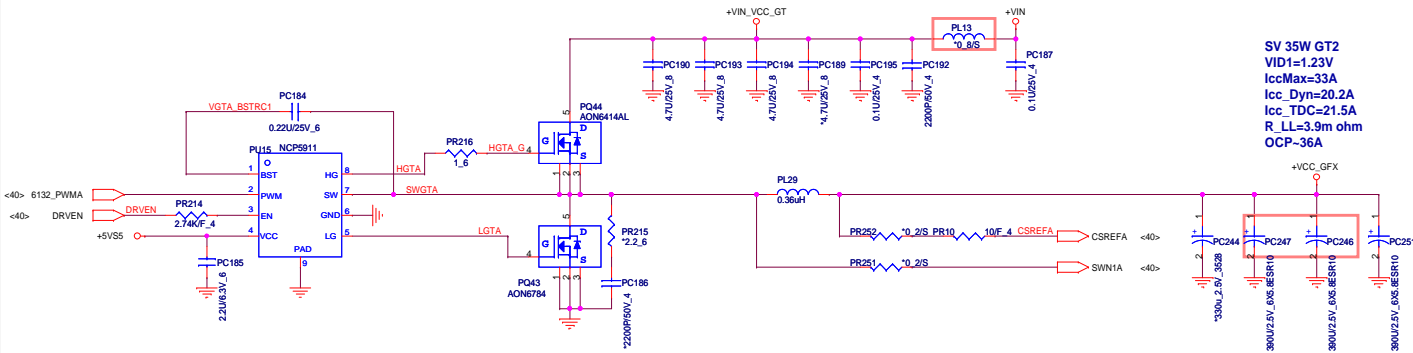


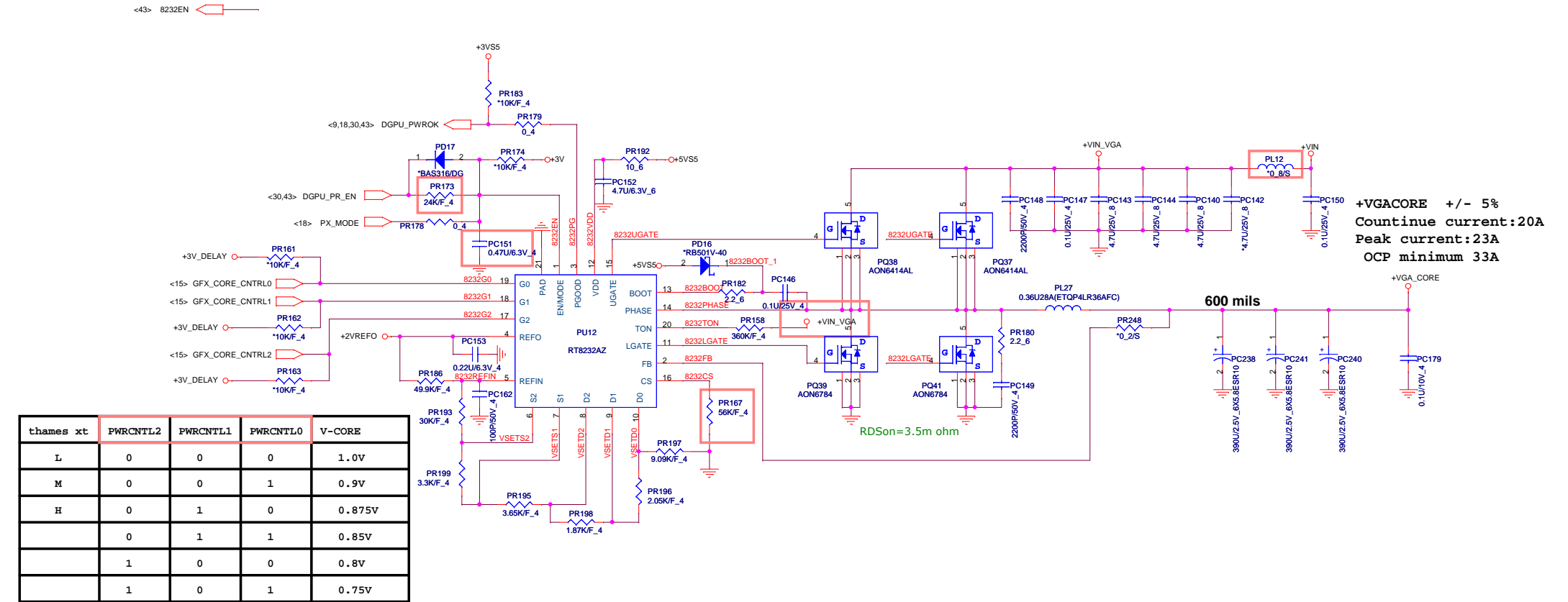


SV 35W CPU  
 VID1=0.9V  
 IccMax=53A  
 Icc\_Dyn=43A  
 Icc\_TDC=36A  
 R\_LL=1.9m ohm  
 OCP=60A



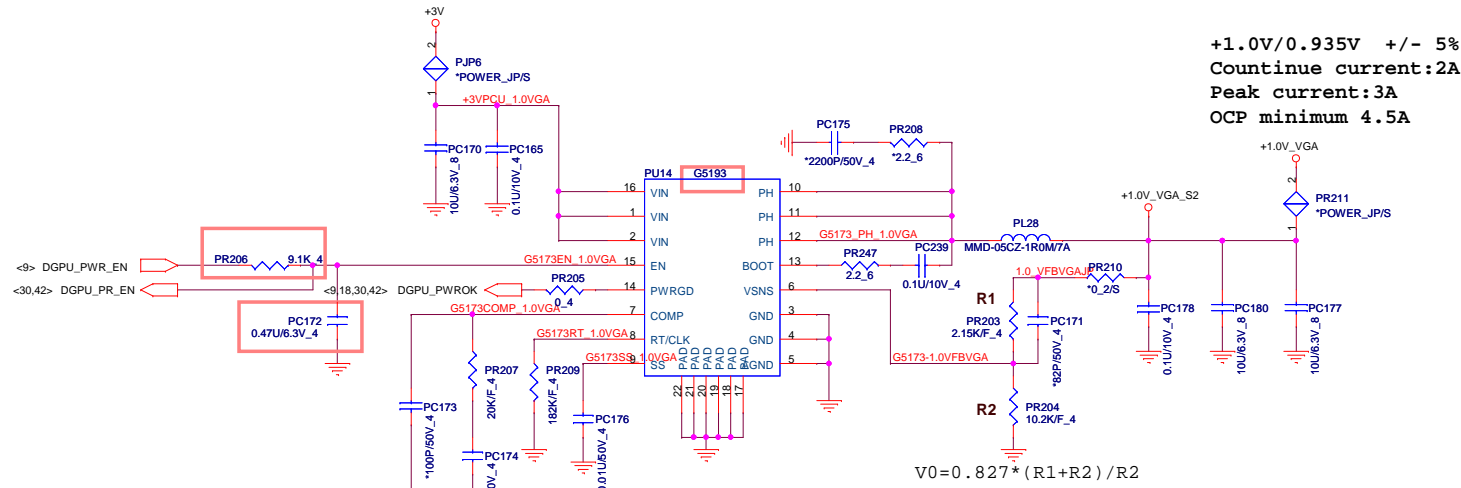
SV 35W GT2  
 VID1=1.23V  
 IccMax=33A  
 Icc\_Dyn=20.2A  
 Icc\_TDC=21.5A  
 R\_LL=3.9m ohm  
 OCP=36A



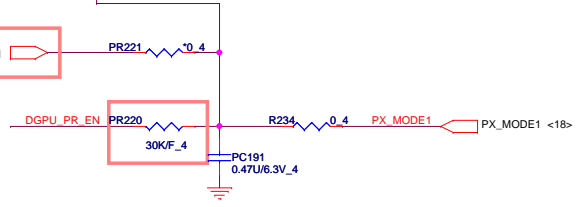
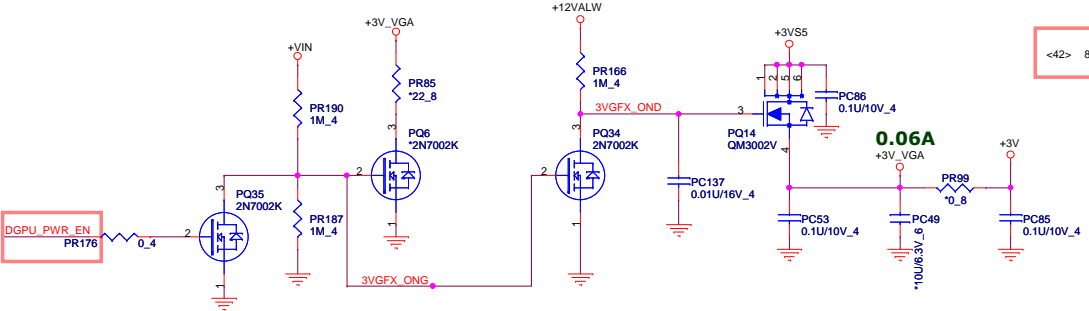
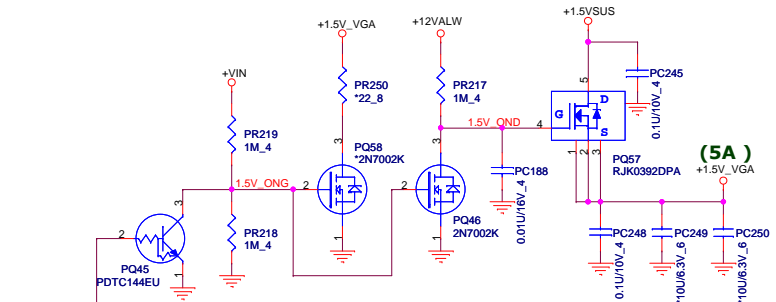
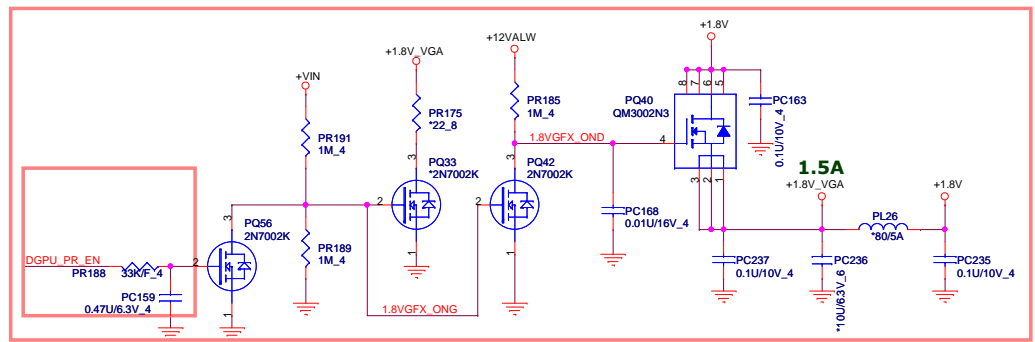


thames xt	PWRCNTL2	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

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- +3V <2,6,7,8,9,10,12,13,14,18,23,24,25,27,28,29,30,31,32,33,39,40,42>
- +VIN <23,34,35,36,37,38,39,41,42>
- +1.8V <4,7,10,38>
- +3V/SS <2,6,7,8,9,10,23,33,35,38,39,42>
- +5VSS <10,23,35,36,37,38,39,40,41,42>
- +3V\_VGA <18>
- +12VALW <32,34,39>
- +1.5V/SUS <2,4,10,12,13,37>
- +1.5V\_VGA <18,20,21,22>
- +1.8V\_VGA <15,16,18,19>
- +3V\_DELAY <15,17,18,42>
- +VGA\_CORE <18,42>



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**Quanta Computer Inc.**

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