

# PRAHA (SRI)

CPU : **Intel Merom (800MHz)**  
 Chip Set : RS600ME & SB600  
 Remarks : Mobility Platform

Model Name : PRAHA  
 PBA Name : MAIN  
 PCB Code : TPT : BA41-00791A  
                   GCE : BA41-00792A  
                   NAN : BA41-00811A  
 Dev. Step : MP1.0 (8-Layer)  
 Revision : 1.0  
 T.R. Date : 2007.07.02

DRAW	CHECK	APPROVAL

■ **Owner : SEC Mobile R & D**      **Signature :**      **X**

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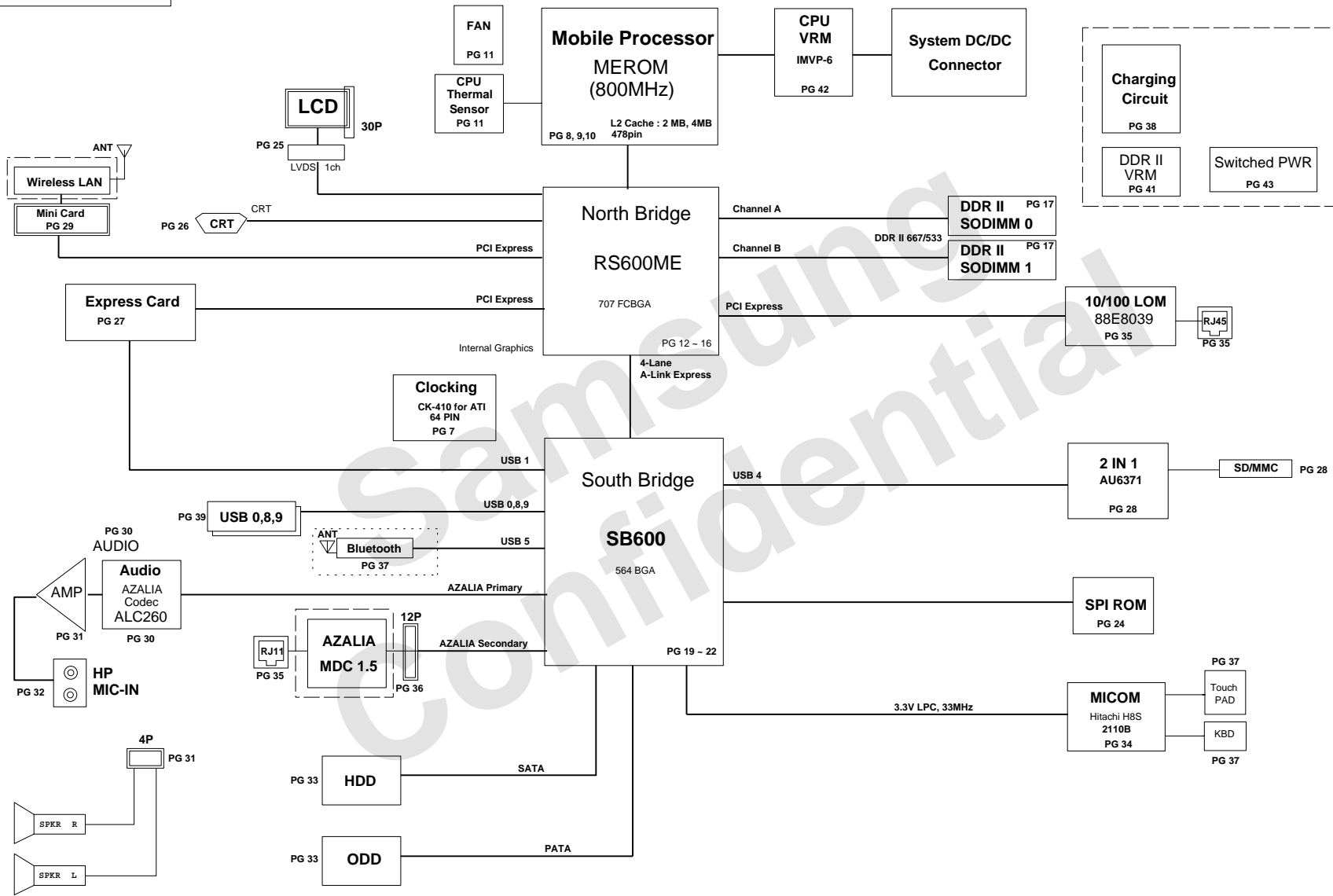
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**USE ICT PORT**

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	COVER	PART NO.	
APPROVAL	SJ PARK	REV	1.0		BA41-00791A	
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	1 OF 47	

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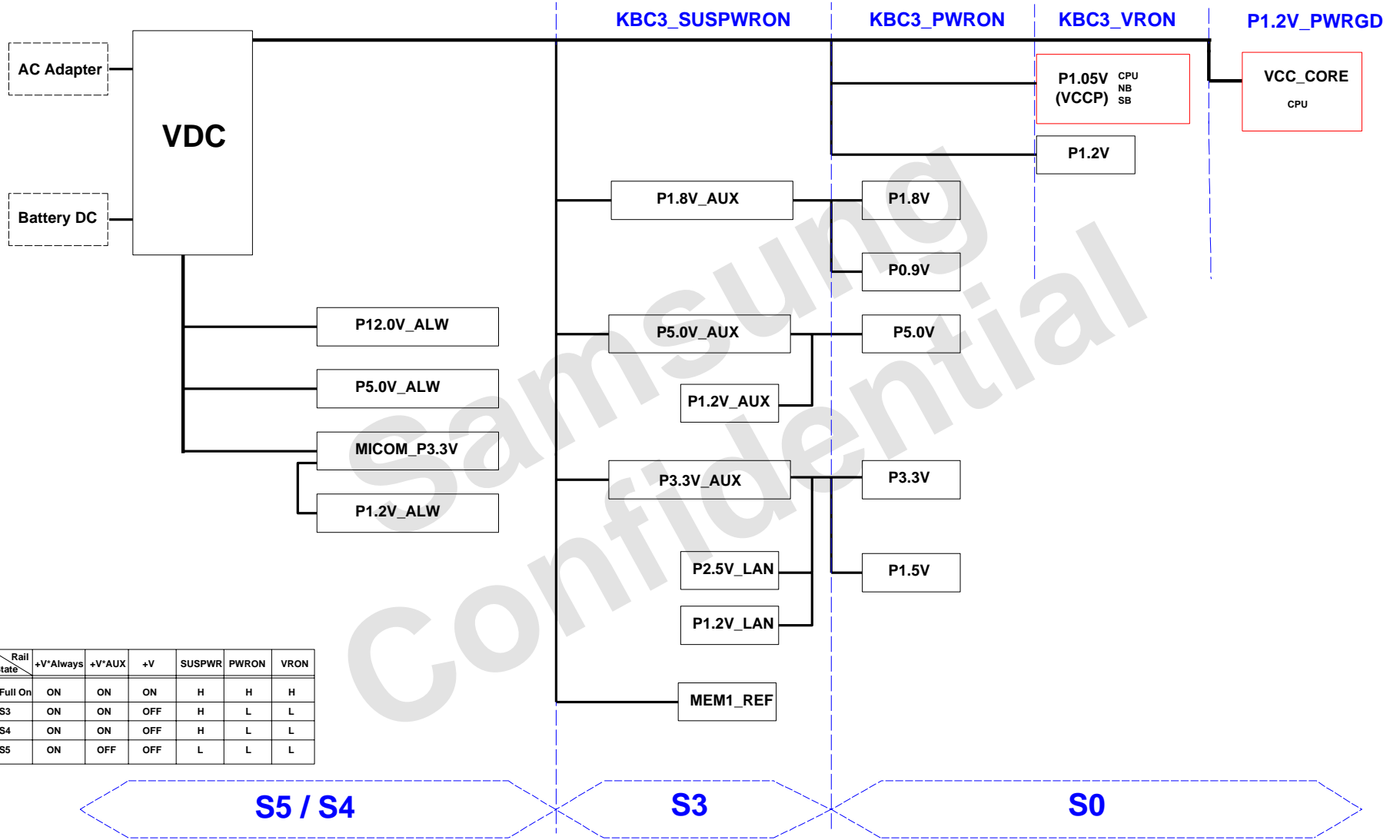
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DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	OPERATION BLOCK DIAGRAM	PART NO.	BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	2	OF 47

# Power Diagram

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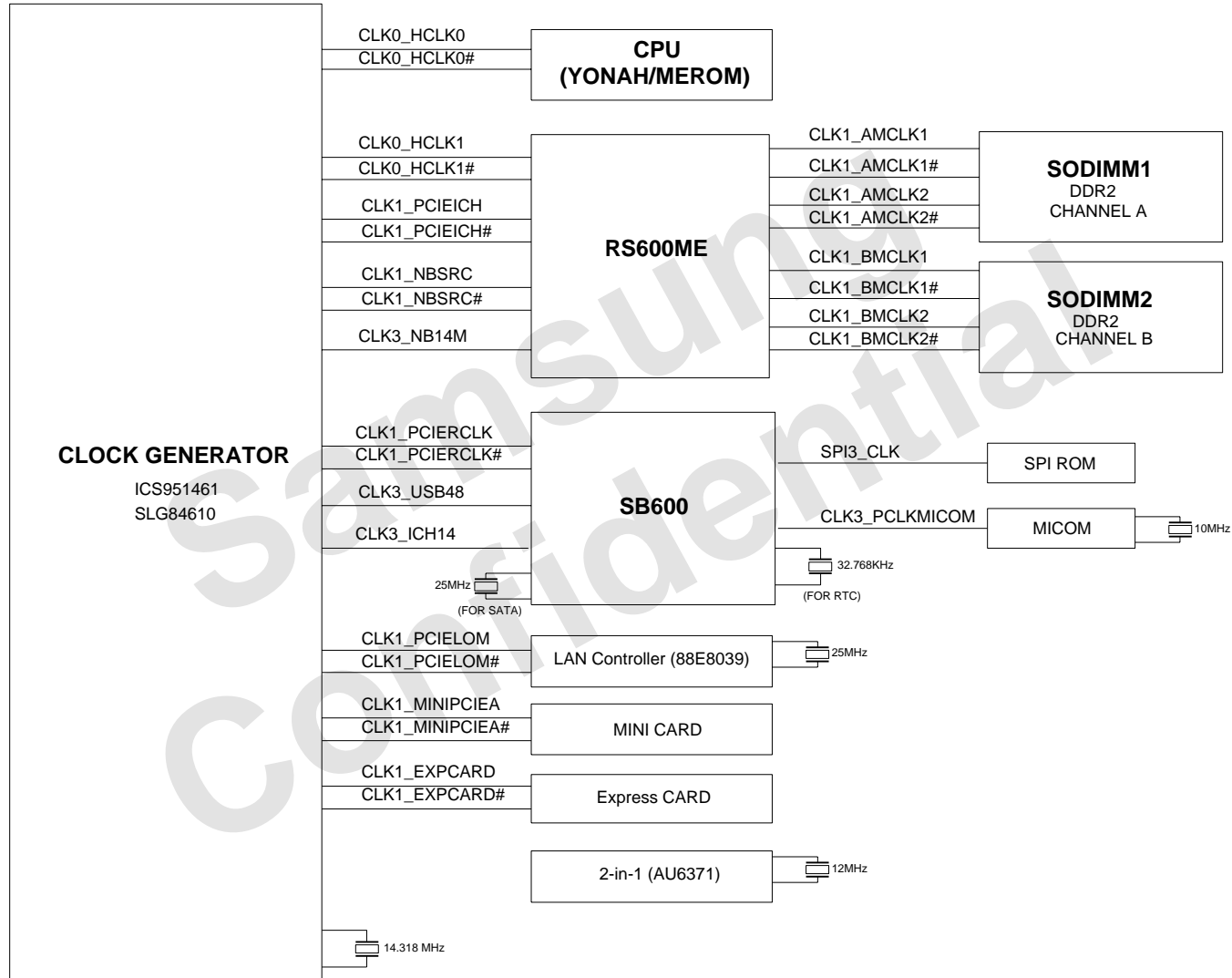


Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN	POWER DIAGRAM	
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
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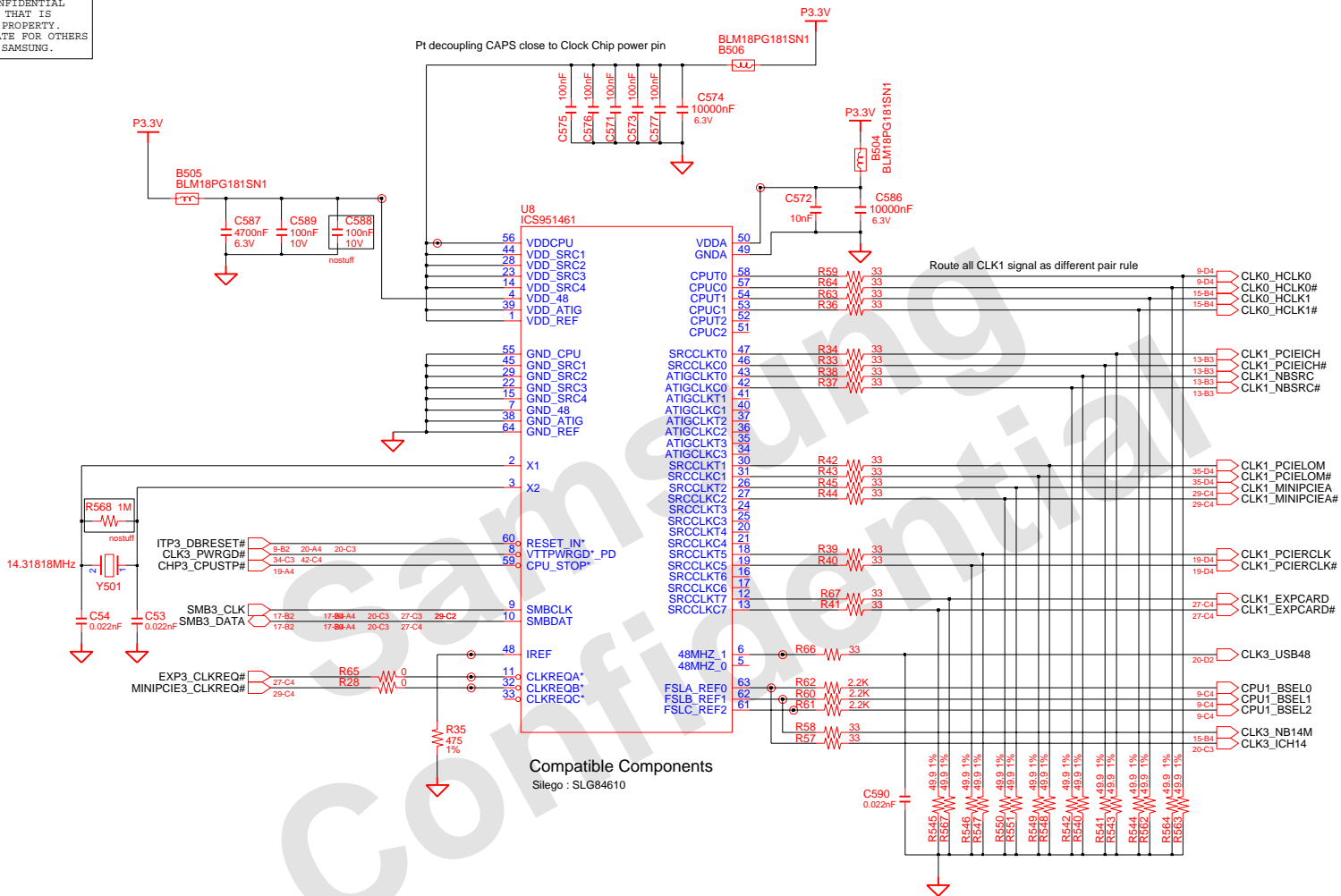


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) CLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 5 OF 47
MODULE CODE						



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**Compatible Components**  
Silogo : SLG84610

Place all the series termination resistor as close as Clock Chip as possible

FSA, FSB, FSC of Clock chip are low threshold inputs  
 $V_{ih\_fs\_min} = 0.7V$   
 $V_{il\_fs\_max} = 0.35V$

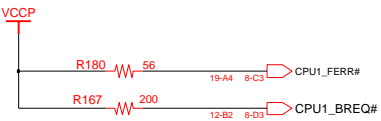
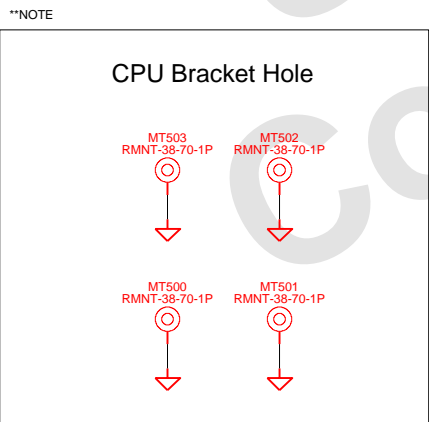
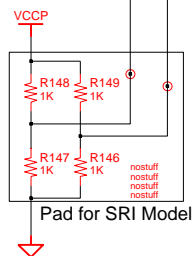
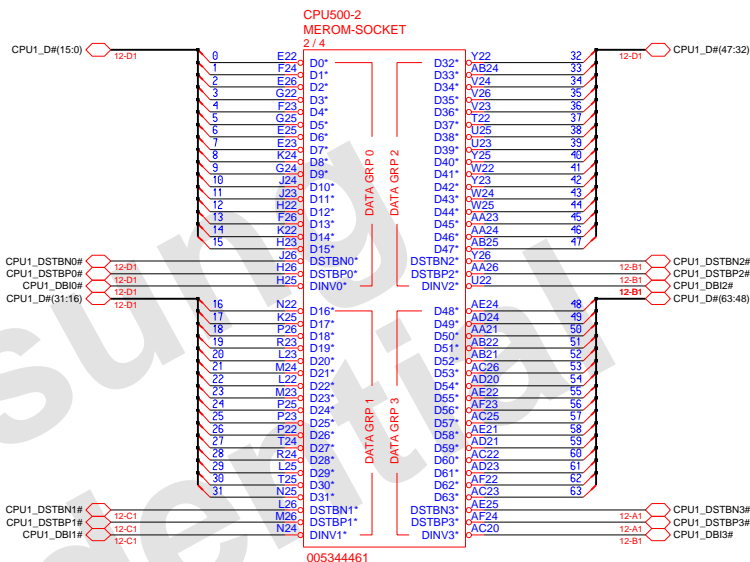
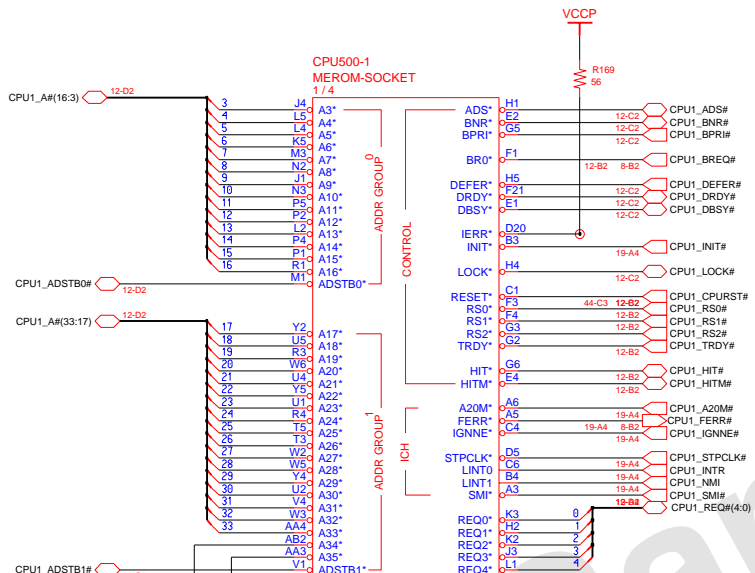
CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

Merom 800MHz  
 Celeron 533MHz  
 Merom 667MHz

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		CLOCK GENERATOR	PART NO. BA41-00791A
MODULE CODE		LAST EDIT				

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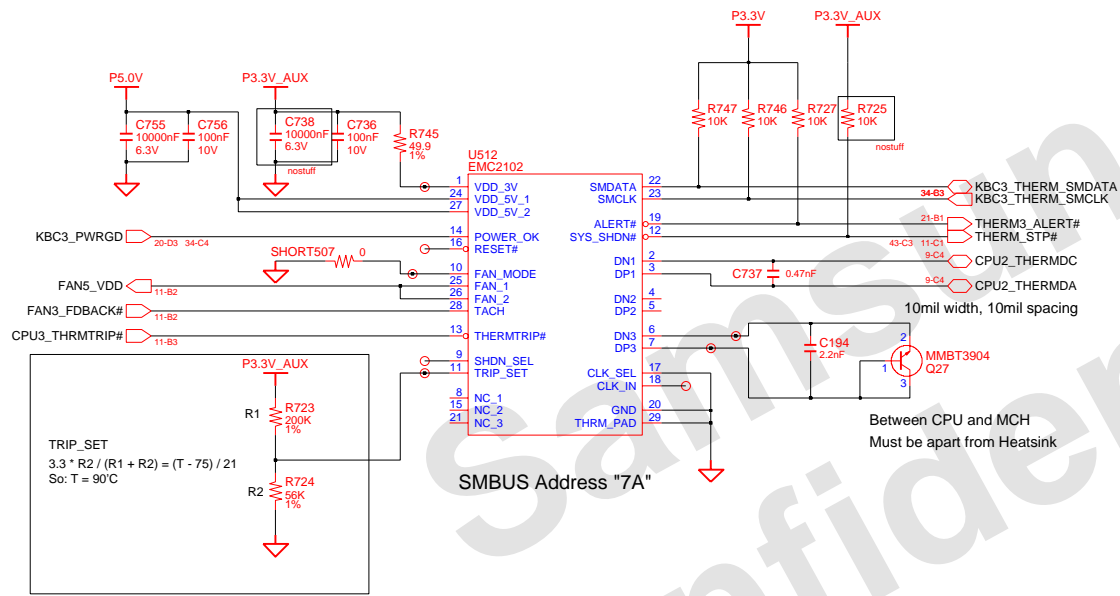
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MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 8 OF 47		





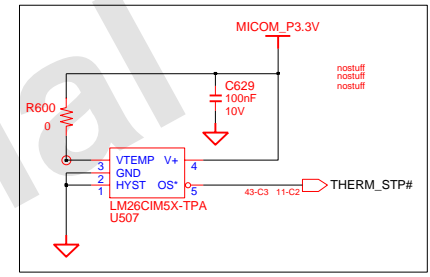


# Thermal Monitor

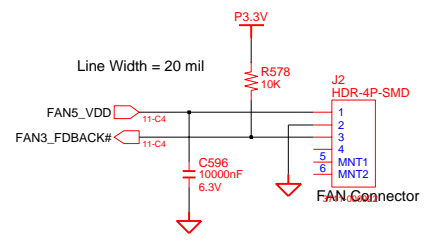
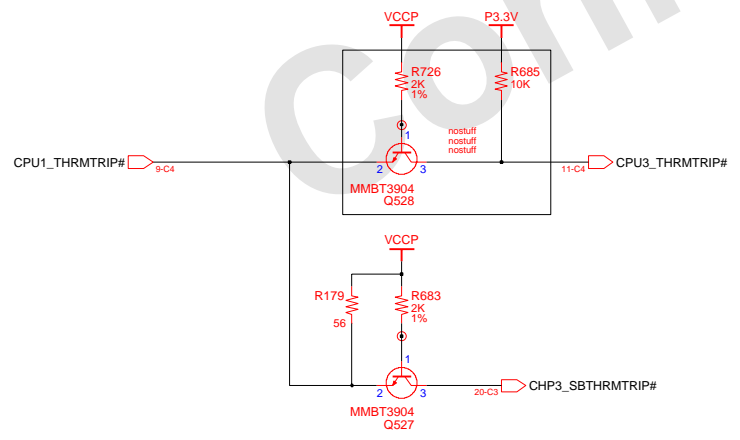


- Refer To Thermal Sensor Layout Guidelines.
- Place the Thermal Sensor close to a remote diode.
  - Keep traces away from high voltage (+12V bus)
  - Keep traces away from fast data buses and CRT signal.
  - Use recommended trace widths and spacings (10mil)
  - Place a ground plane under the traces.
  - Use guard traces flanking DXP and DXN and connecting to GND

## OTP (NOSTUFF)

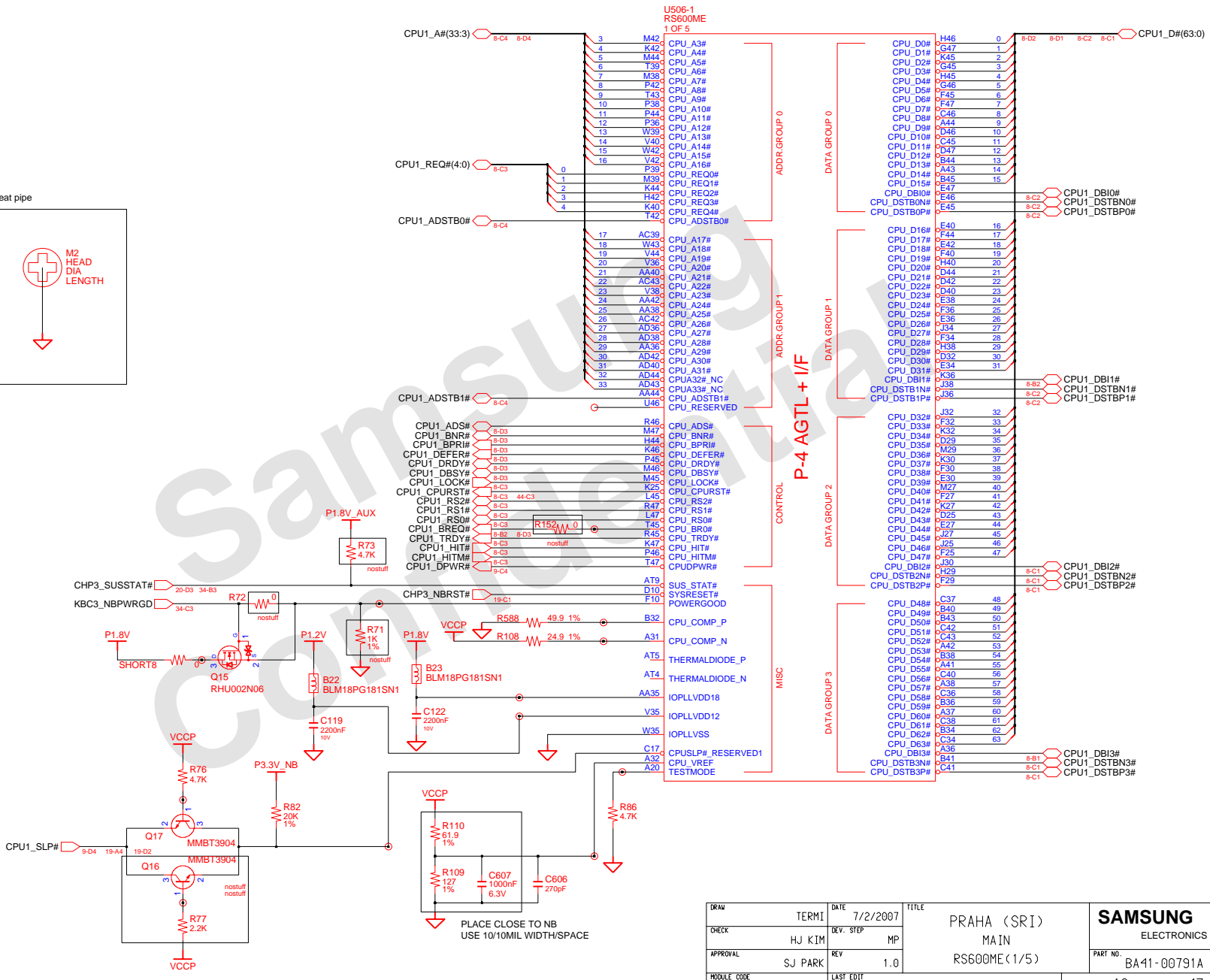
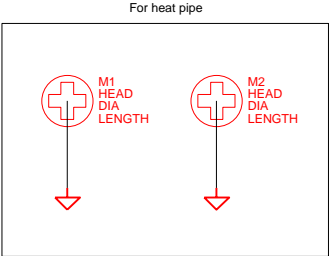


## FAN Control



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	THERMAL SENSOR/FAN CNTRL		PART NO. BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	11	OF 47

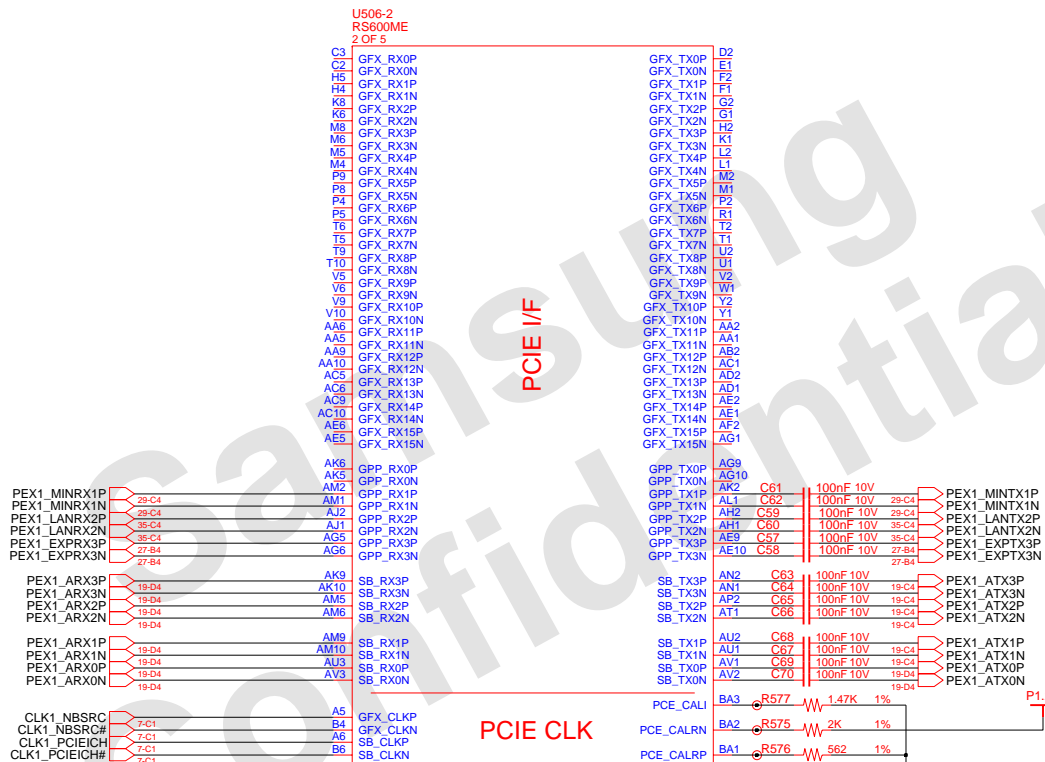
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CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		RSG00ME(1/5)	PART NO. BA41-00791A
MODULE CODE		LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	12	OF 47

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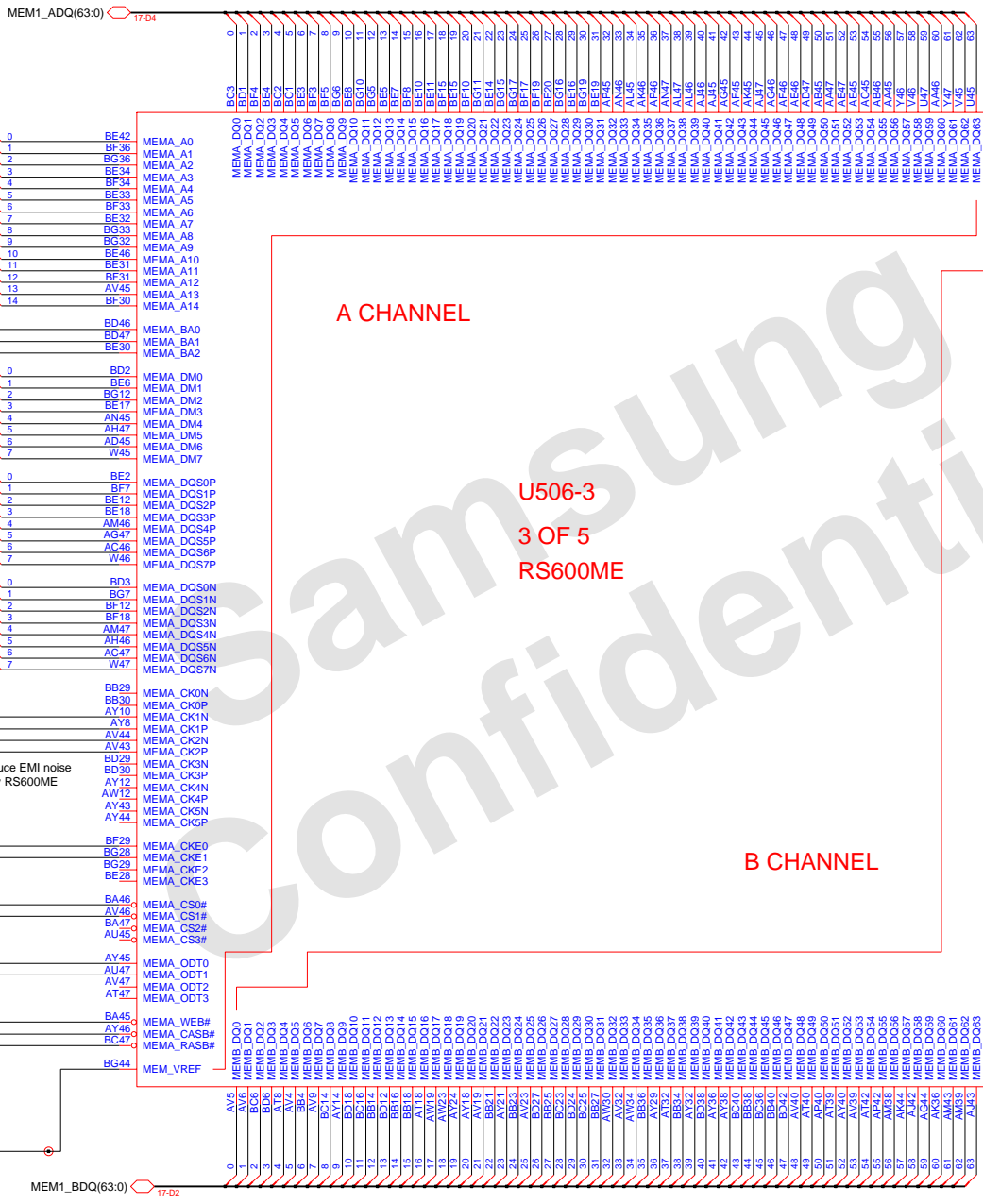
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PEX1_MIN	Mini Card I/F
PEX1_LAN	LOM I/F
PEX1_EXP	Express Card I/F

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	RS600ME(2/5)		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
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**A CHANNEL**

**B CHANNEL**

MEM1\_AMA(14:0) 17-D4 18-C4

MEM1\_ABS0 17-C4 18-C4  
 MEM1\_ABS1 17-C4 18-C4  
 MEM1\_ABS2 17-C4 18-C4  
 MEM1\_ADM(7:0) 17-B4

MEM1\_ADQS(7:0) 17-B4

MEM1\_AQS(7:0) 17-A4

CLK1\_AMCLK1# 17-C4

CLK1\_AMCLK1# 17-C4  
 CLK1\_AMCLK2# 17-C4

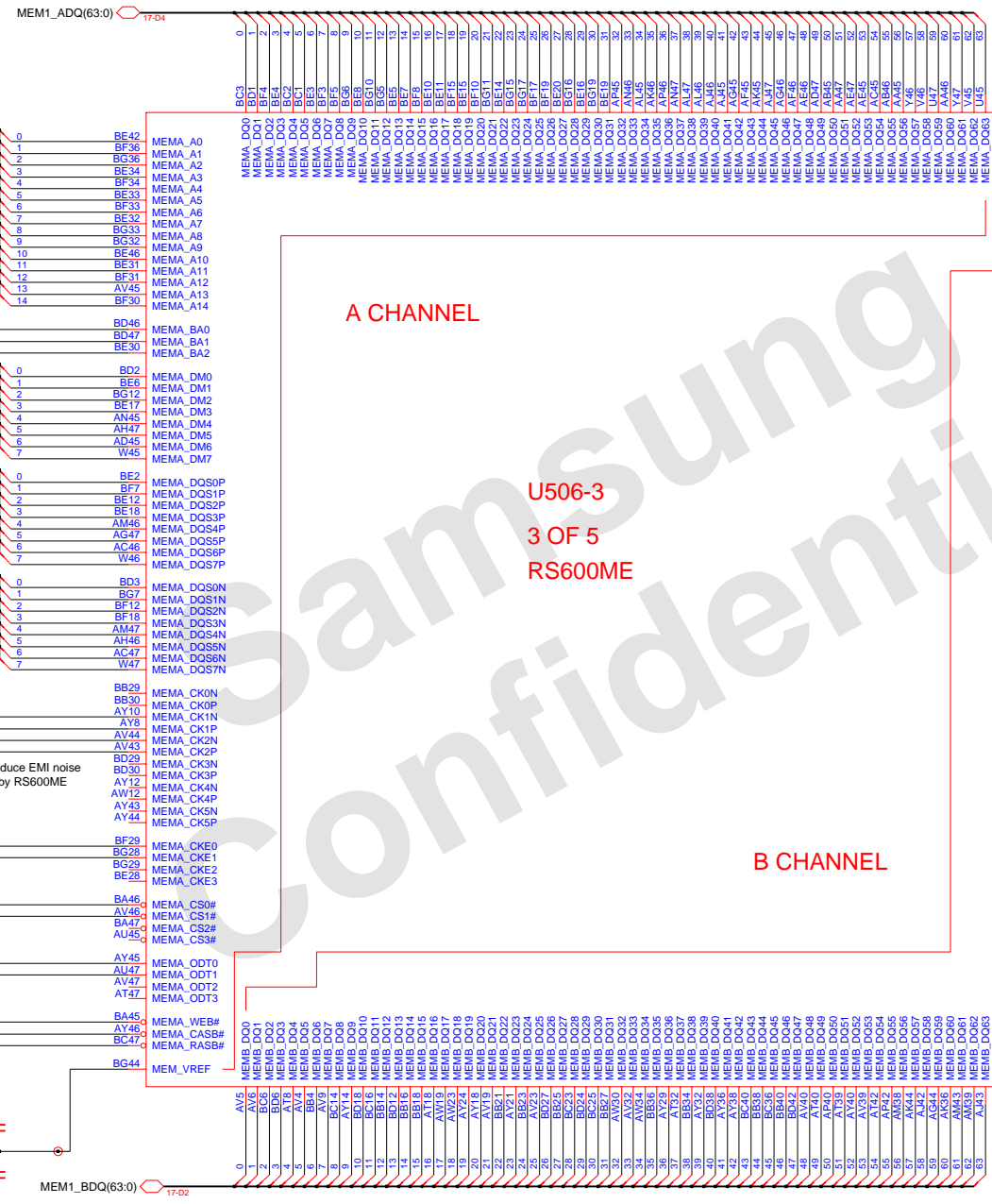
CLK1\_AMCLK2# 17-C4

MEM1\_ACKE0 17-C4 18-D4  
 MEM1\_ACKE1 17-C4 18-D4

MEM1\_ACS0# 17-C4 18-D4  
 MEM1\_ACS1# 17-C4 18-D4

MEM1\_AODT0 17-B4 18-D4  
 MEM1\_AODT1 17-B4 18-D4

MEM1\_AWE# 17-B4 18-C4  
 MEM1\_ARAS# 17-C4 18-C4  
 MEM1\_REF



MEM1\_BMA(14:0) 18-C3 17-D2

MEM1\_BBS0 18-C3 17-C2  
 MEM1\_BBS1 18-C3 17-C2  
 MEM1\_BBS2 18-C3 17-C2  
 MEM1\_BDM(7:0) 17-B2

MEM1\_BDOS(7:0) 17-B2

MEM1\_BDOS#(7:0) 17-A2

CLK1\_BMCLK1# 17-C2  
 CLK1\_BMCLK1 17-C2  
 CLK1\_BMCLK2# 17-C2

CLK1\_BMCLK2# 17-C2

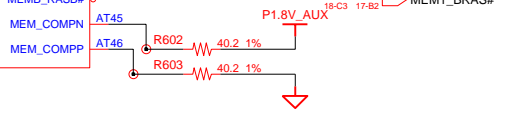
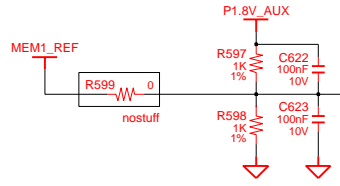
MEM1\_BCKE0 18-D3 17-C2  
 MEM1\_BCKE1 18-D3 17-C2

MEM1\_BCS0# 18-D3 17-C2  
 MEM1\_BCS1# 18-D3 17-C2

MEM1\_BODT0 18-D3 17-B2  
 MEM1\_BODT1 18-D3 17-B2

MEM1\_BWE# 18-C3 17-B2  
 MEM1\_BAS# 18-C3 17-C2  
 MEM1\_BRAS# 18-C3 17-B2

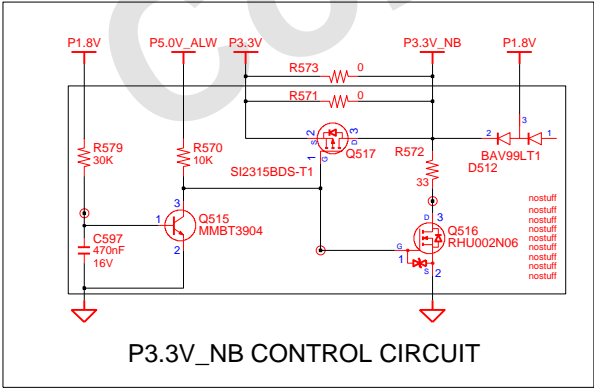
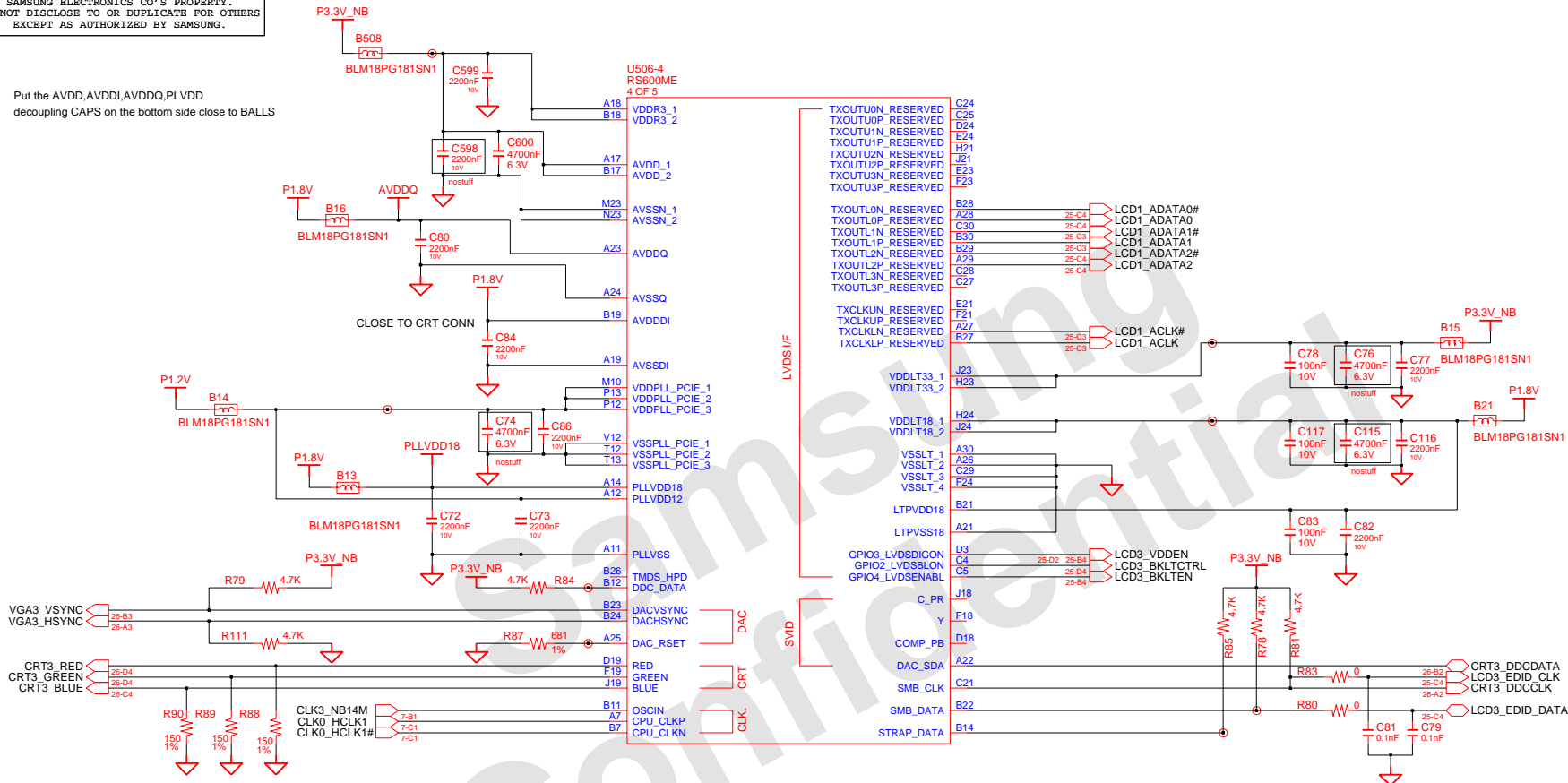
MEM\_COMPN AT45  
 MEM\_COMPP AT46



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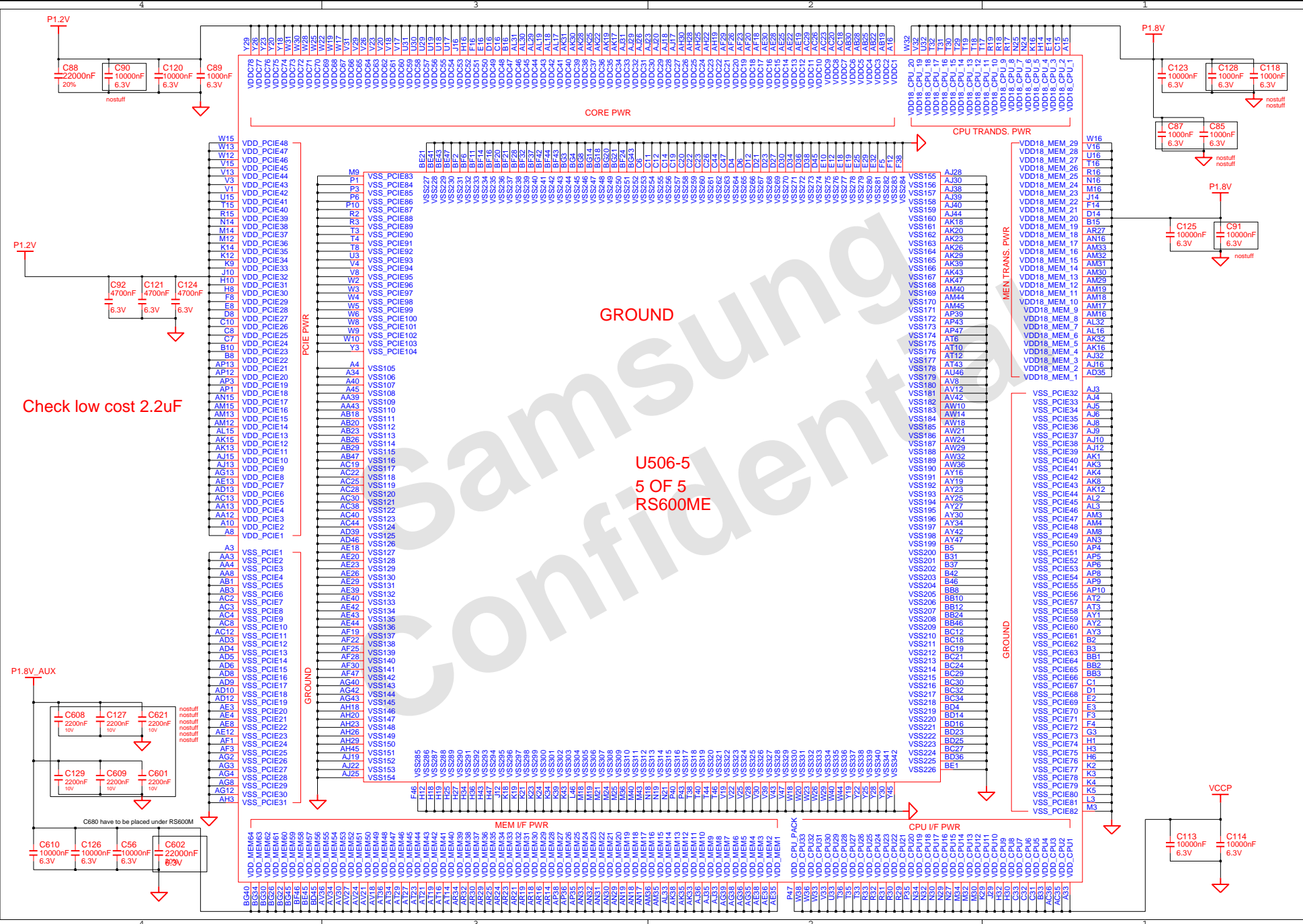
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Put the AVDD, AVDDI, AVDDQ, PLVDD decoupling CAPS on the bottom side close to BALLS



STRAP DEFINITIONS FOR THE RS6000	
STRAP PIN	DESCRIPTION
DACHSYN	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYN	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS6000
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

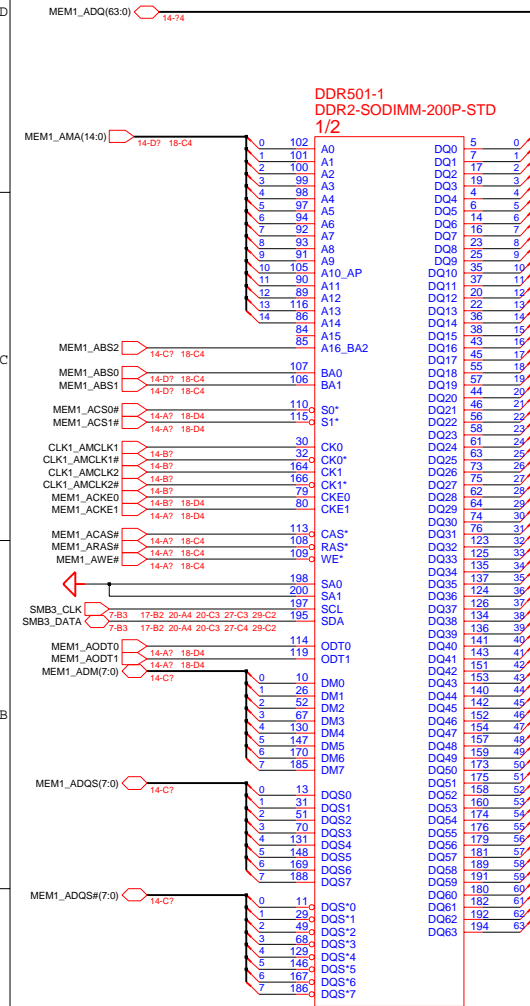
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MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	15	OF 47





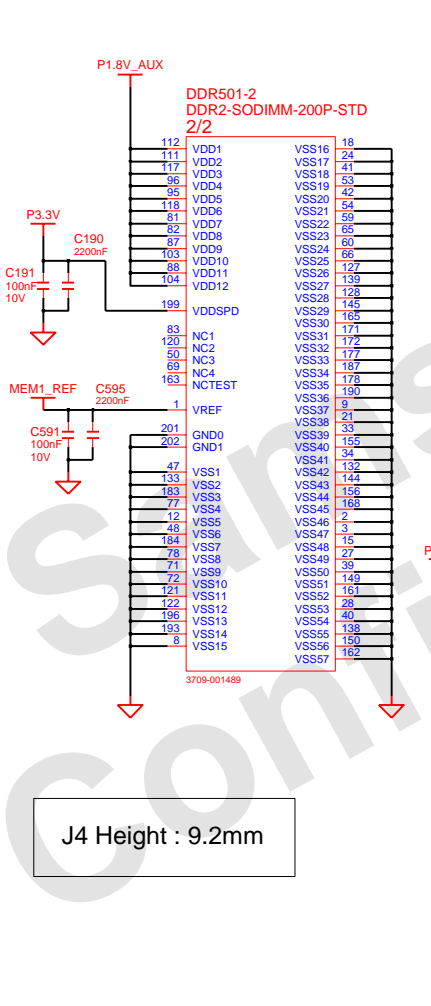
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DDR501-1  
DDR2-SODIMM-200P-STD  
1/2

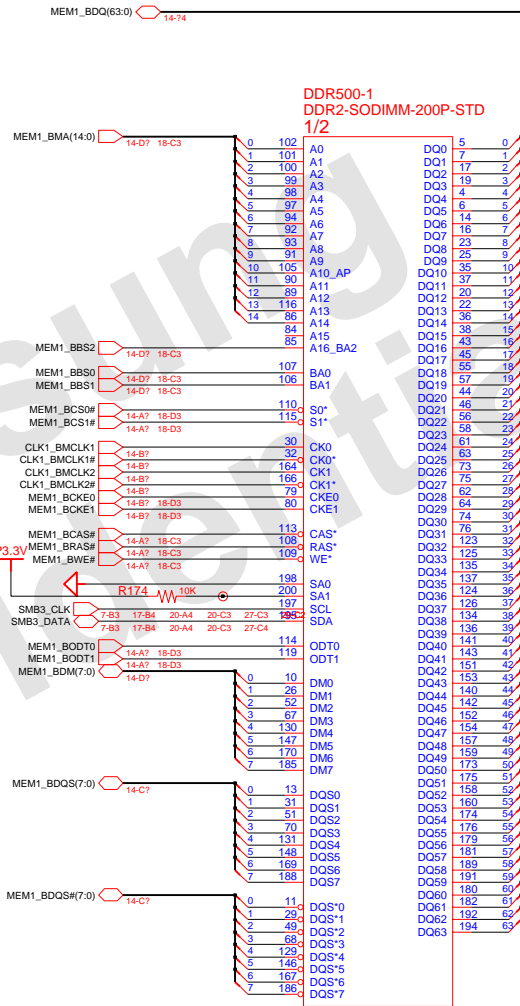
3709-001489



DDR501-2  
DDR2-SODIMM-200P-STD  
2/2

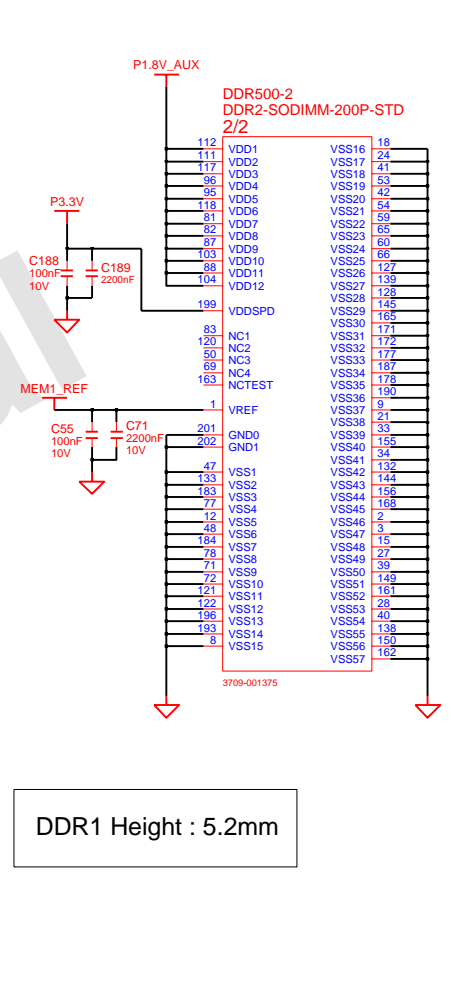
J4 Height : 9.2mm

3709-001489



DDR500-1  
DDR2-SODIMM-200P-STD  
1/2

3709-001375



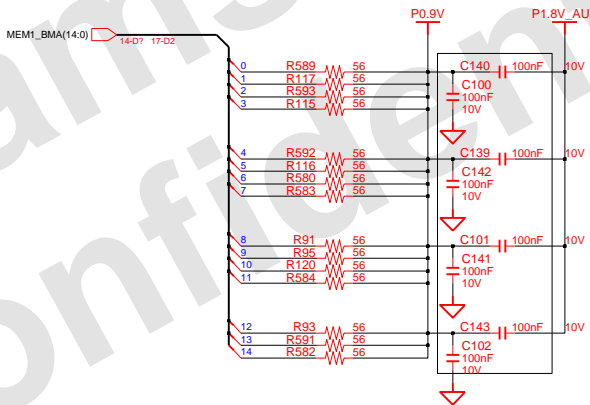
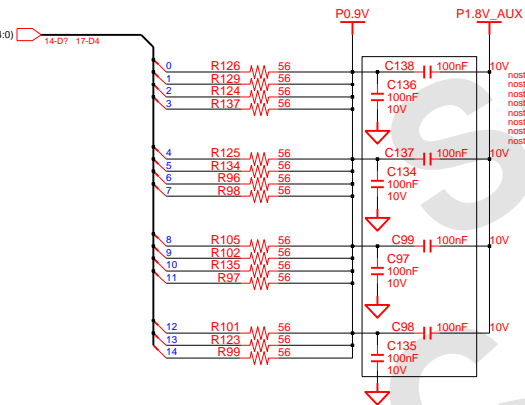
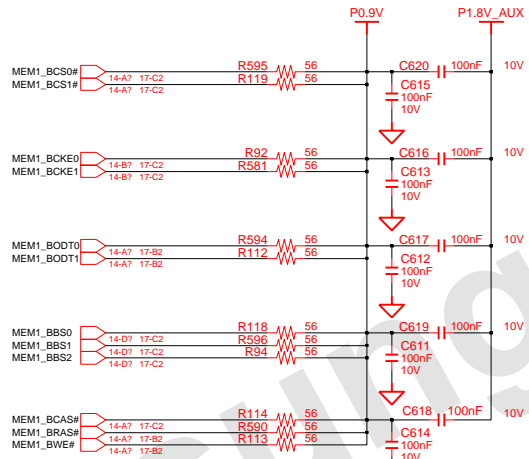
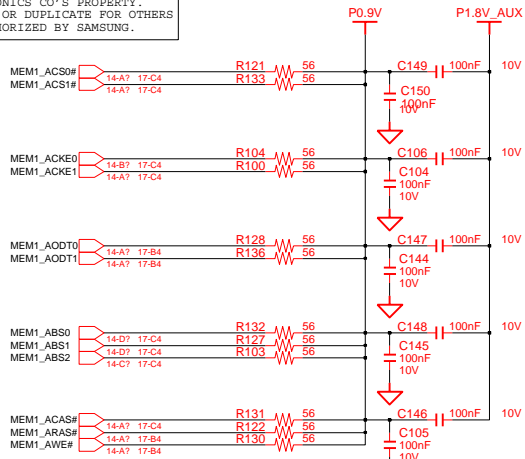
DDR500-2  
DDR2-SODIMM-200P-STD  
2/2

DDR1 Height : 5.2mm

3709-001375

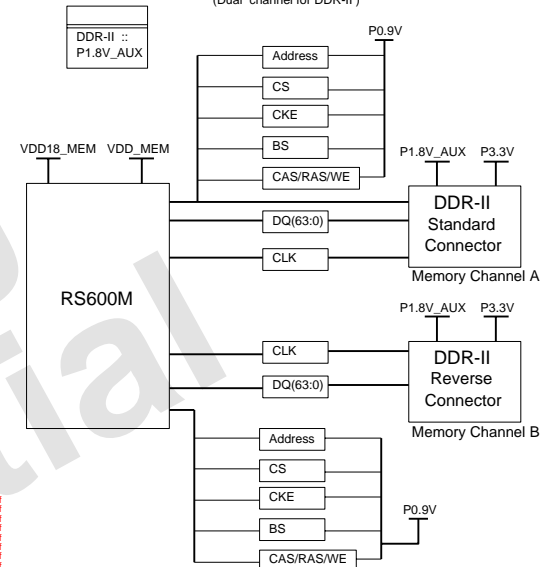
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CHECK	HJ KIM	DEV. STEP	MP	MAIN		
APPROVAL	SJ PARK	REV	1.0	DDR2 - SODIMM		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	17	OF 47

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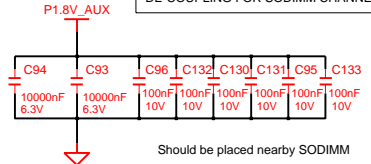


### Memory Topology

(Dual channel for DDR-II)

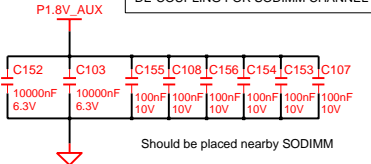


#### DE-COUPLING FOR SODIMM CHANNEL A



Should be placed nearby SODIMM

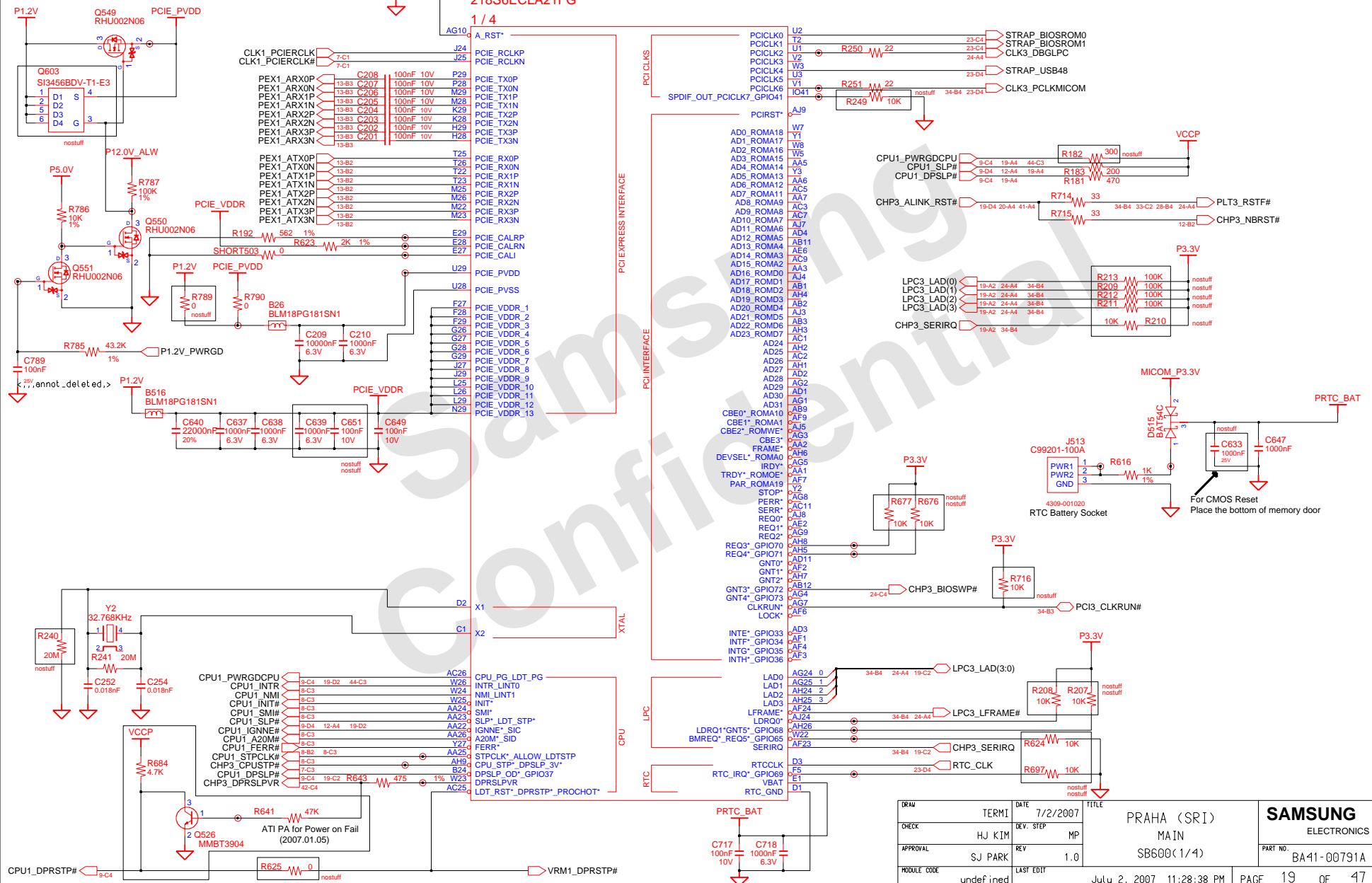
#### DE-COUPLING FOR SODIMM CHANNEL B



Should be placed nearby SODIMM

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	DDR2 - TERMINATION		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	18	OF 47

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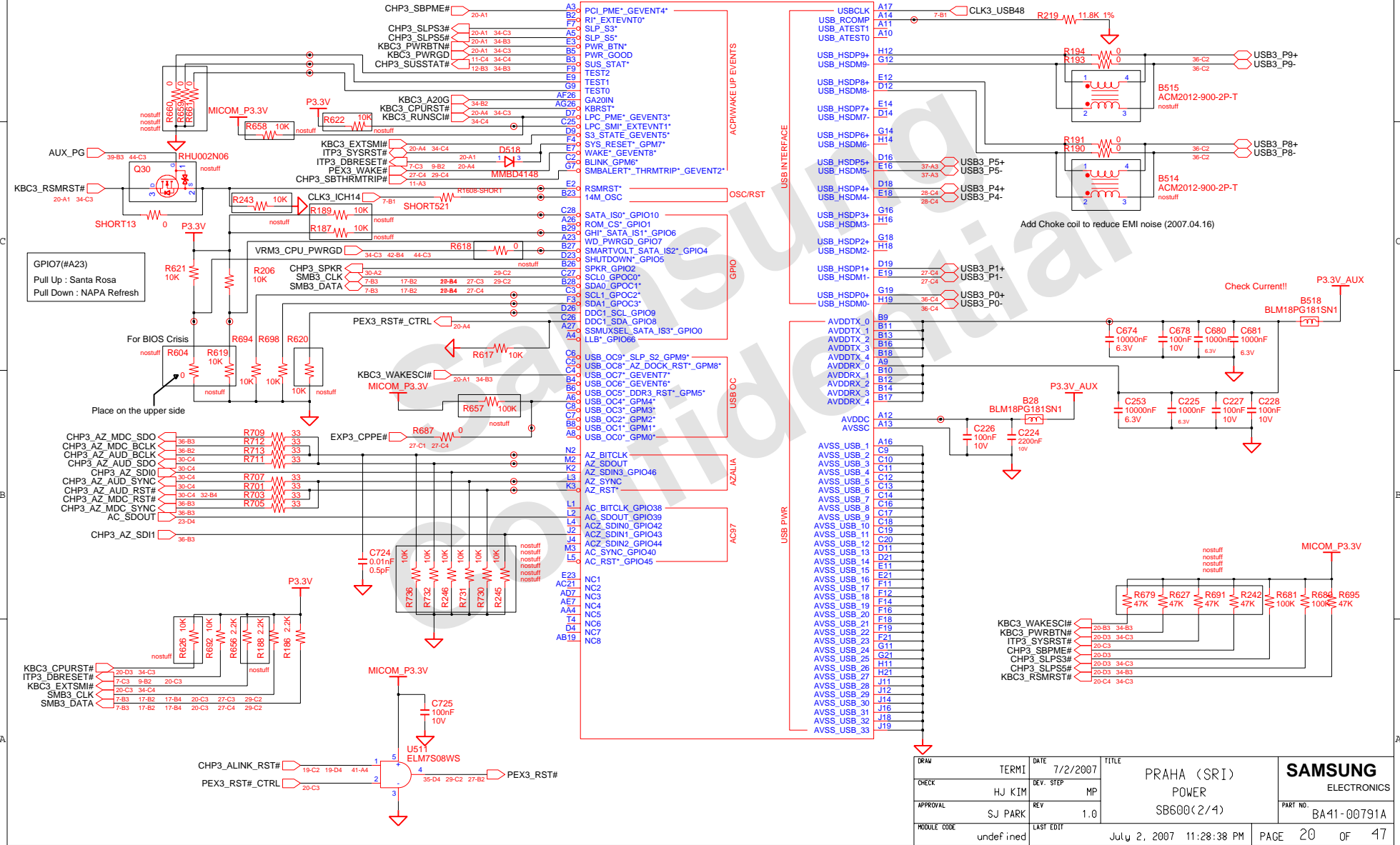
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APPROVAL	SJ PARK	REV	1.0	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 19 OF 47

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USB Port 0 : Left side USB Port
USB Port 1 : Express Card
USB Port 4 : 2-in-1 Memory Card
USB Port 5 : Bluetooth I/F
USB Port 8, 9 : Rear side USB Port

U11-2
218S6ECLA21FG
2 / 4



GPIO7(#A23)
Pull Up : Santa Rosa
Pull Down : NAPA Refresh

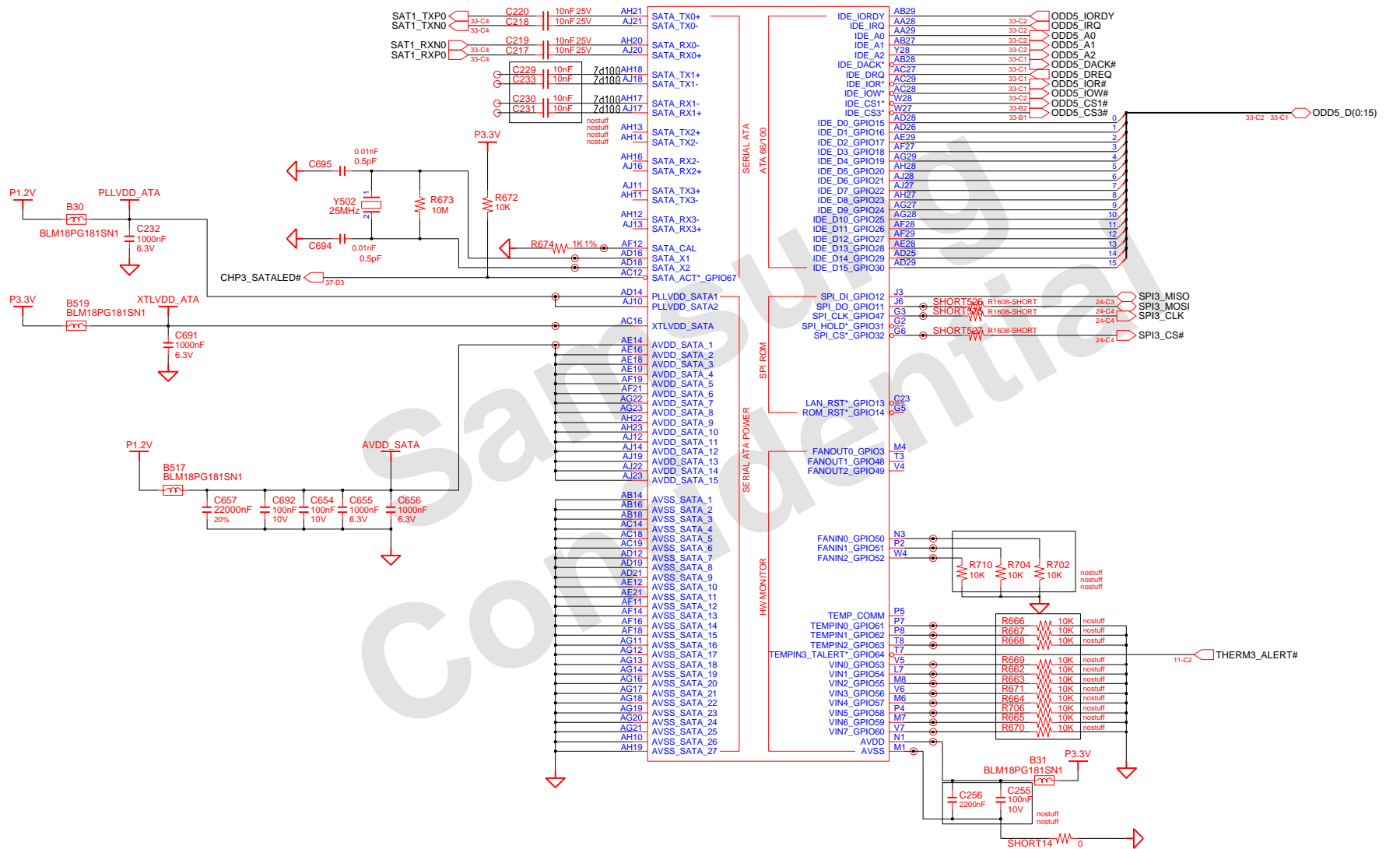
Add Choke coil to reduce EMI noise (2007.04.16)

Check Current!!!

Table with columns: DRAW, CHECK, APPROVAL, MODULE CODE, TERMI, DEV. STEP, REV, LAST EDIT, DATE, TITLE, PRAHA (SRI) POWER SB600(2/4), SAMSUNG ELECTRONICS, PART NO. BA41-00791A, PAGE 20 OF 47

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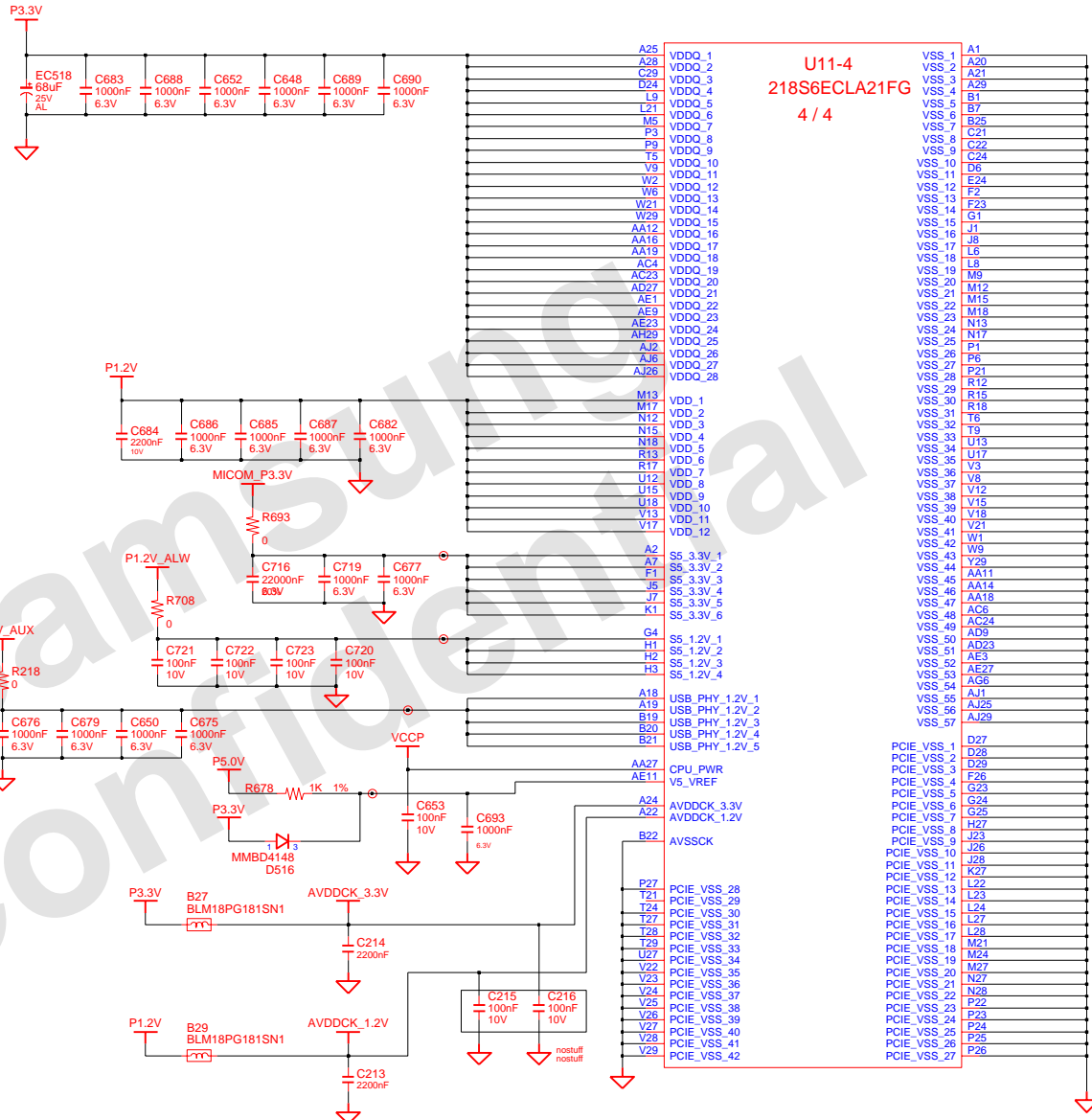
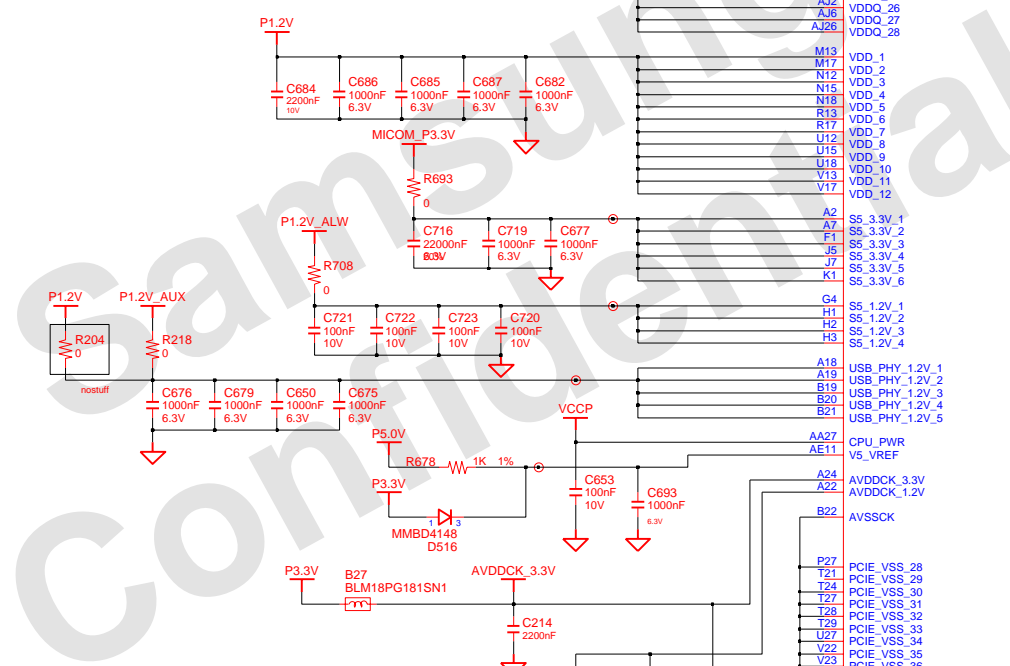
U11-3  
 218S6ECLA21FG  
 3 / 4



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		SB600(3/4)	PART NO.
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	21	OF 47

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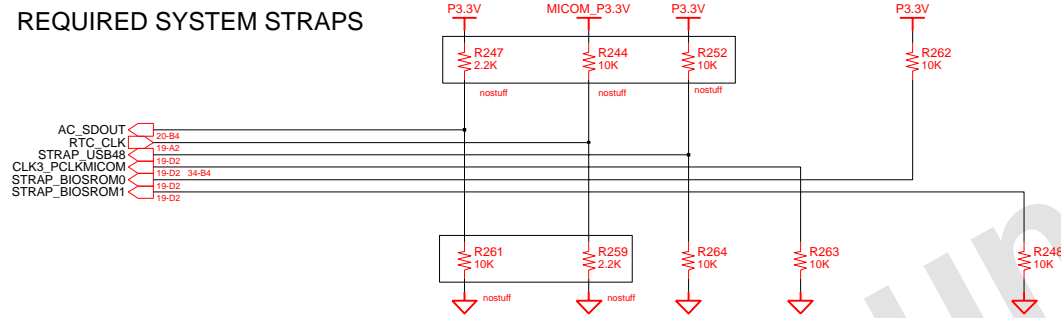
A25	VDDQ_1	VSS_1	A1
A26	VDDQ_2	VSS_2	A20
C28	VDDQ_3	VSS_3	A21
B24	VDDQ_4	VSS_4	A29
L9	VDDQ_5	VSS_5	B1
L21	VDDQ_6	VSS_6	B7
M5	VDDQ_7	VSS_7	B25
P3	VDDQ_8	VSS_8	C21
P9	VDDQ_9	VSS_9	C22
T5	VDDQ_10	VSS_10	C24
V9	VDDQ_11	VSS_11	D6
W2	VDDQ_12	VSS_12	F24
W6	VDDQ_13	VSS_13	F2
W21	VDDQ_14	VSS_14	F23
W29	VDDQ_15	VSS_15	G1
AA12	VDDQ_16	VSS_16	J1
AA16	VDDQ_17	VSS_17	J8
AA19	VDDQ_18	VSS_18	L6
AC4	VDDQ_19	VSS_19	L8
AC23	VDDQ_20	VSS_20	M9
AE27	VDDQ_21	VSS_21	M12
AE11	VDDQ_22	VSS_22	M15
AE9	VDDQ_23	VSS_23	M18
AE23	VDDQ_24	VSS_24	N13
AH29	VDDQ_25	VSS_25	N17
AJ2	VDDQ_26	VSS_26	P1
AJ6	VDDQ_27	VSS_27	P6
AJ26	VDDQ_28	VSS_28	P21
M13	VDD_1	VSS_29	R12
M17	VDD_2	VSS_30	R15
N12	VDD_3	VSS_31	R18
N15	VDD_4	VSS_32	T6
N18	VDD_5	VSS_33	T9
R13	VDD_6	VSS_34	U13
R17	VDD_7	VSS_35	U17
U12	VDD_8	VSS_36	V8
U15	VDD_9	VSS_37	V12
U18	VDD_10	VSS_38	V15
V13	VDD_11	VSS_39	V18
V17	VDD_12	VSS_40	V21
A2	S5_3.3V_1	VSS_41	W1
A7	S5_3.3V_2	VSS_42	W9
F1	S5_3.3V_3	VSS_43	Y29
J5	S5_3.3V_4	VSS_44	AA11
J7	S5_3.3V_5	VSS_45	AA14
K1	S5_3.3V_6	VSS_46	AA18
G4	S5_1.2V_1	VSS_47	AC6
H1	S5_1.2V_2	VSS_48	AC24
H2	S5_1.2V_3	VSS_49	AD9
H3	S5_1.2V_4	VSS_50	AD23
A18	USB_PHY_1.2V_1	VSS_51	AE3
A19	USB_PHY_1.2V_2	VSS_52	AE7
B19	USB_PHY_1.2V_3	VSS_53	AG6
B20	USB_PHY_1.2V_4	VSS_54	AJ1
B21	USB_PHY_1.2V_5	VSS_55	AJ25
AA27	CPU_PWR	VSS_56	AJ29
AE11	V5_VREF	VSS_57	D27
A24	AVDDCK_3.3V	PCIE_VSS_1	D28
A22	AVDDCK_1.2V	PCIE_VSS_2	D29
B22	AVSSCK	PCIE_VSS_3	F26
P27	PCIE_VSS_28	PCIE_VSS_4	G23
T21	PCIE_VSS_29	PCIE_VSS_5	G24
T24	PCIE_VSS_30	PCIE_VSS_6	G25
T27	PCIE_VSS_31	PCIE_VSS_7	H27
T28	PCIE_VSS_32	PCIE_VSS_8	J23
T29	PCIE_VSS_33	PCIE_VSS_9	J26
U27	PCIE_VSS_34	PCIE_VSS_10	K27
V22	PCIE_VSS_35	PCIE_VSS_11	K27
V23	PCIE_VSS_36	PCIE_VSS_12	L22
V24	PCIE_VSS_37	PCIE_VSS_13	L23
V25	PCIE_VSS_38	PCIE_VSS_14	L23
V26	PCIE_VSS_39	PCIE_VSS_15	L24
V27	PCIE_VSS_40	PCIE_VSS_16	L27
V28	PCIE_VSS_41	PCIE_VSS_17	L28
V29	PCIE_VSS_42	PCIE_VSS_18	M21
		PCIE_VSS_19	M24
		PCIE_VSS_20	M27
		PCIE_VSS_21	N27
		PCIE_VSS_22	N28
		PCIE_VSS_23	P22
		PCIE_VSS_24	P24
		PCIE_VSS_25	P25
		PCIE_VSS_26	P26

U11-4  
218S6ECLA21FG  
4 / 4

DRAW	TERMI	DATE	TITLE	PRAHA (SRI) MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	7/2/2007	MP		
APPROVAL	SJ PARK	REV	1.0	SB600(4/4)	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	22 OF 47

SB600 HAS AN INTERNAL PD FOR AC\_SDOUT  
 SB600 HAS AN INTERNAL PU FOR RTC\_CLK

**REQUIRED SYSTEM STRAPS**



	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0	PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM	
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	L, H = LPC ROM L, L = FWH ROM	

**DEBUG STRAPS**

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

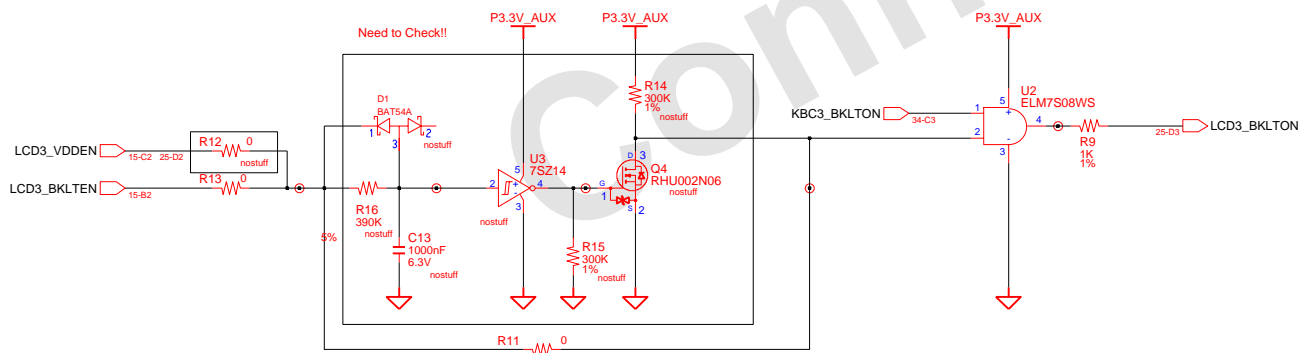
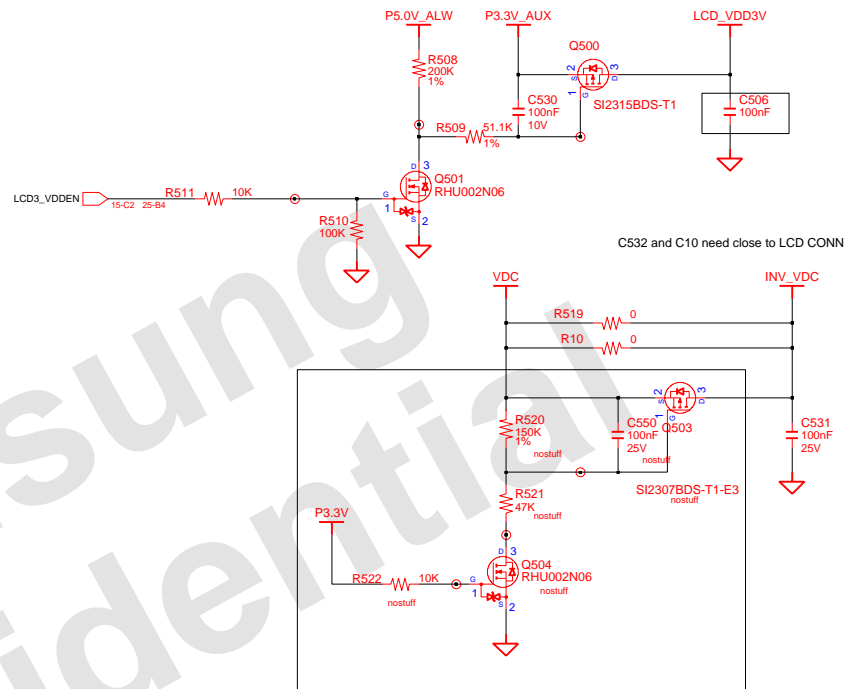
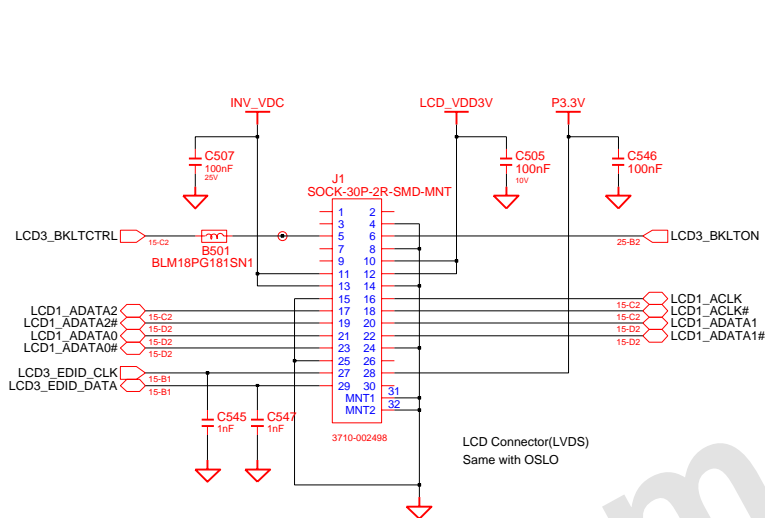
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	STRAPS		PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	23	OF 47





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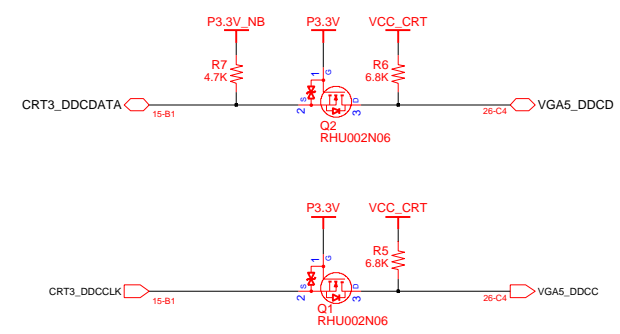
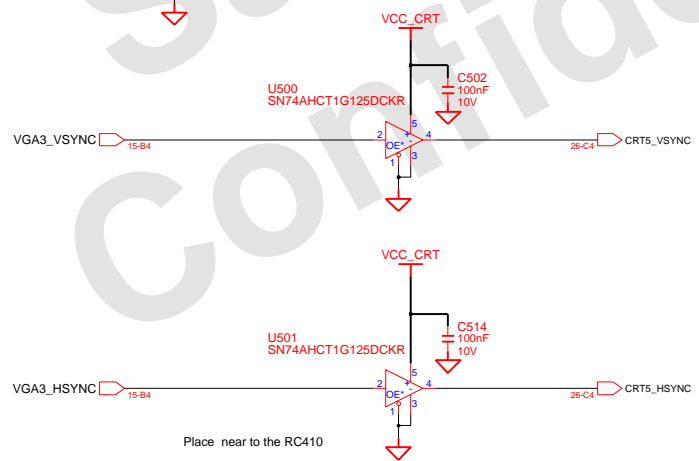
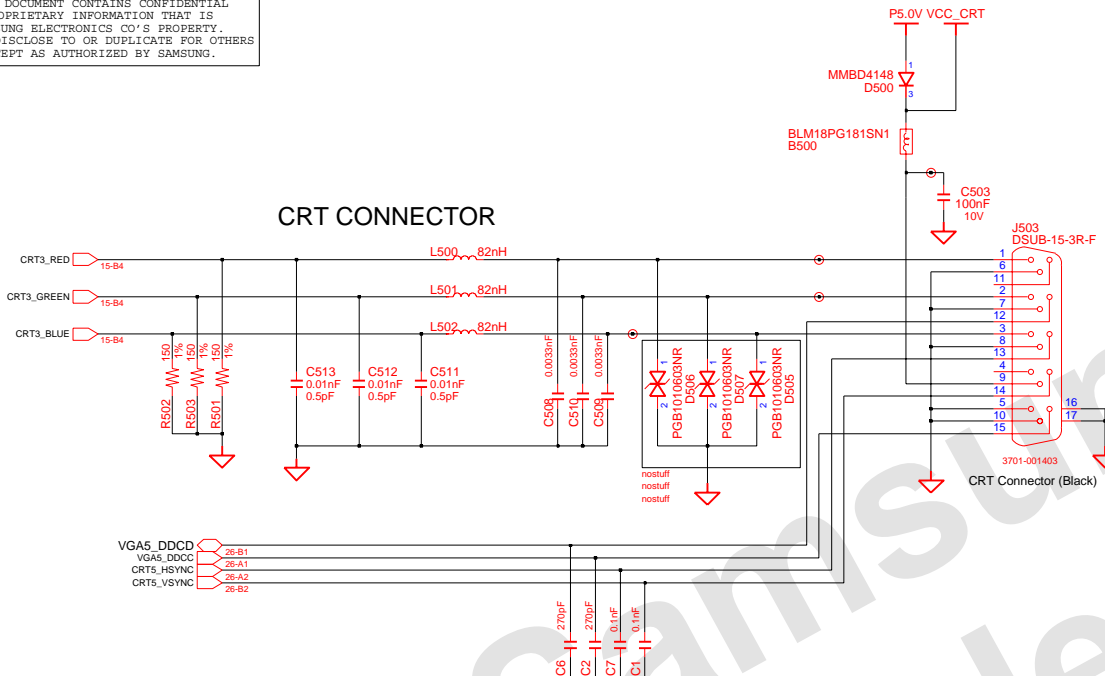
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DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) LCD Connector & SPREAD SPECTRUM	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	PART NO.		
APPROVAL	SJ PARK	REV	1.0	July 2, 2007 11:28:38 PM		BA41-00791A
MODULE CODE	undefined	LAST EDIT		PAGE	25	OF 47

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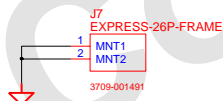
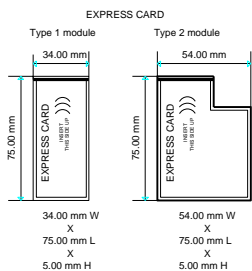
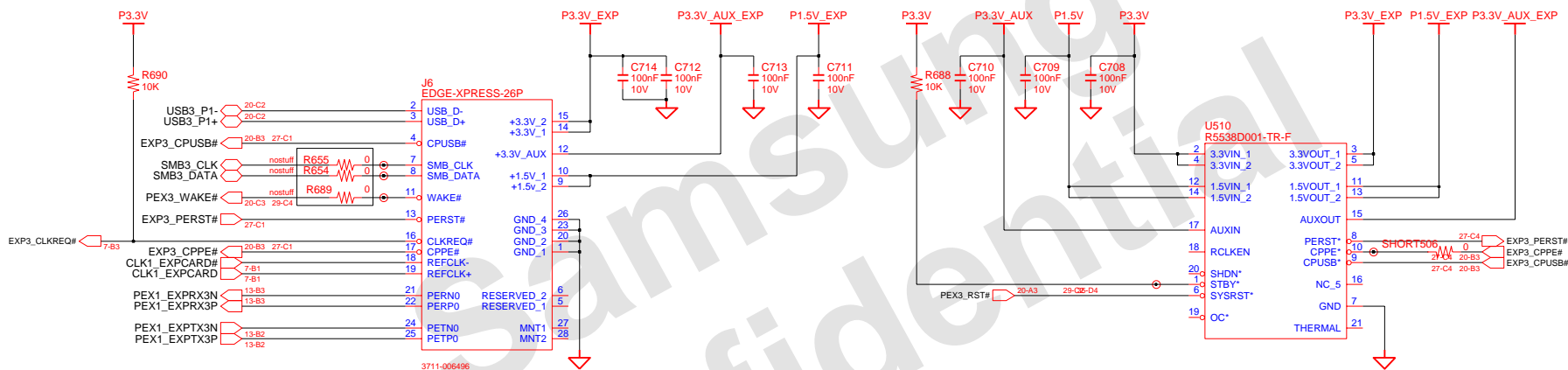
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DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		CRT	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			PAGE 26 OF 47

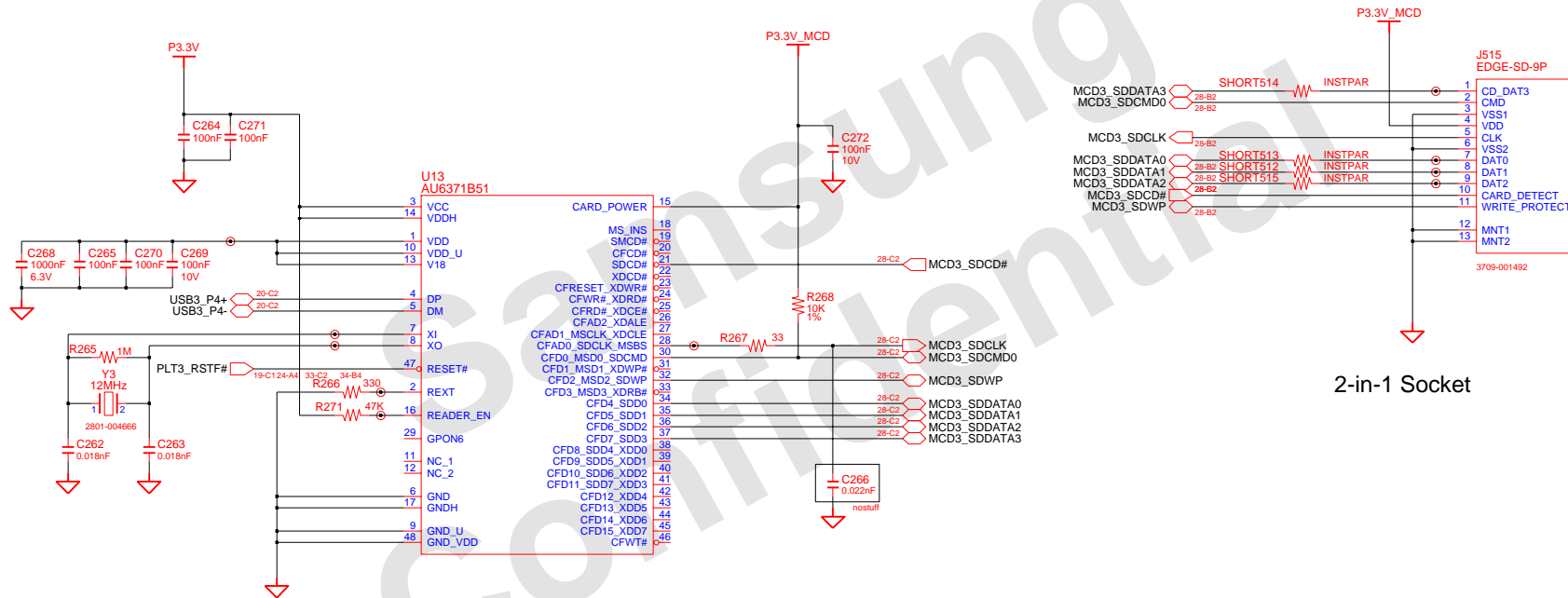
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DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	EXPRESS CARD	PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	27	OF 47

2 IN 1 CARD

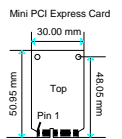
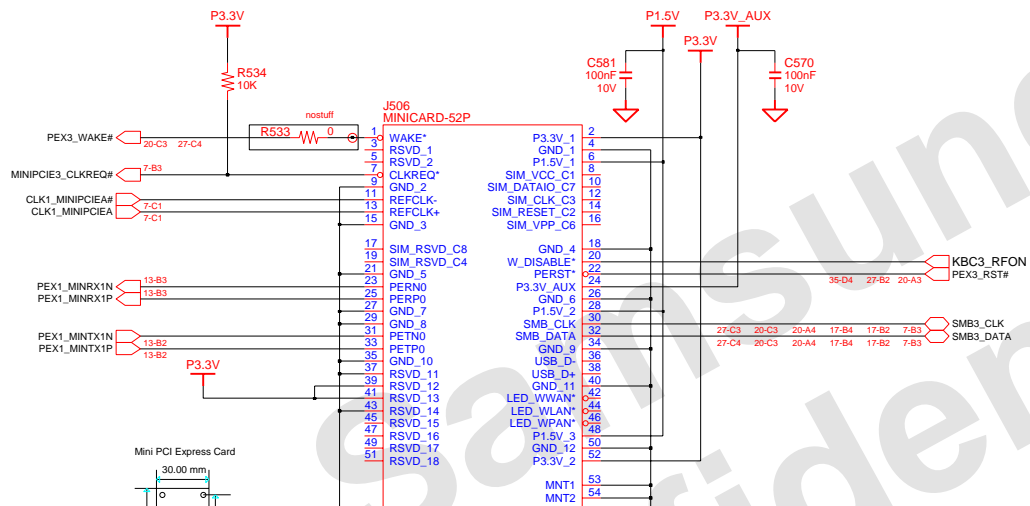


2-in-1 Socket

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0	2 in 1 Socket		PART NO.
MODULE CODE	LAST EDIT		July 2, 2007 11:28:38 PM		PAGE	28 OF 47

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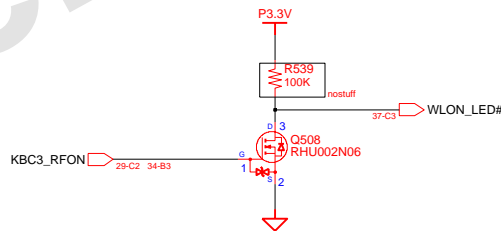
Odd Pins : Top side  
 Even Pins : Bottom Side

**7mm Height  
 Mini PCI Express**

PCI Express Mini Card ElectroMechanical Spec. 1.0



**4.5mm Height  
 For MiniCard**



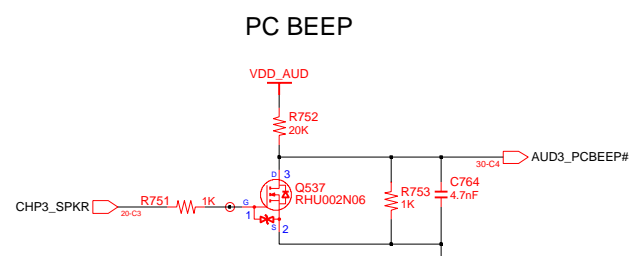
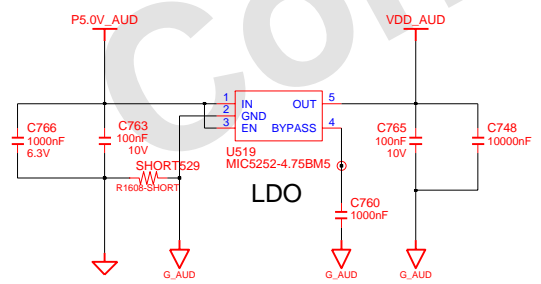
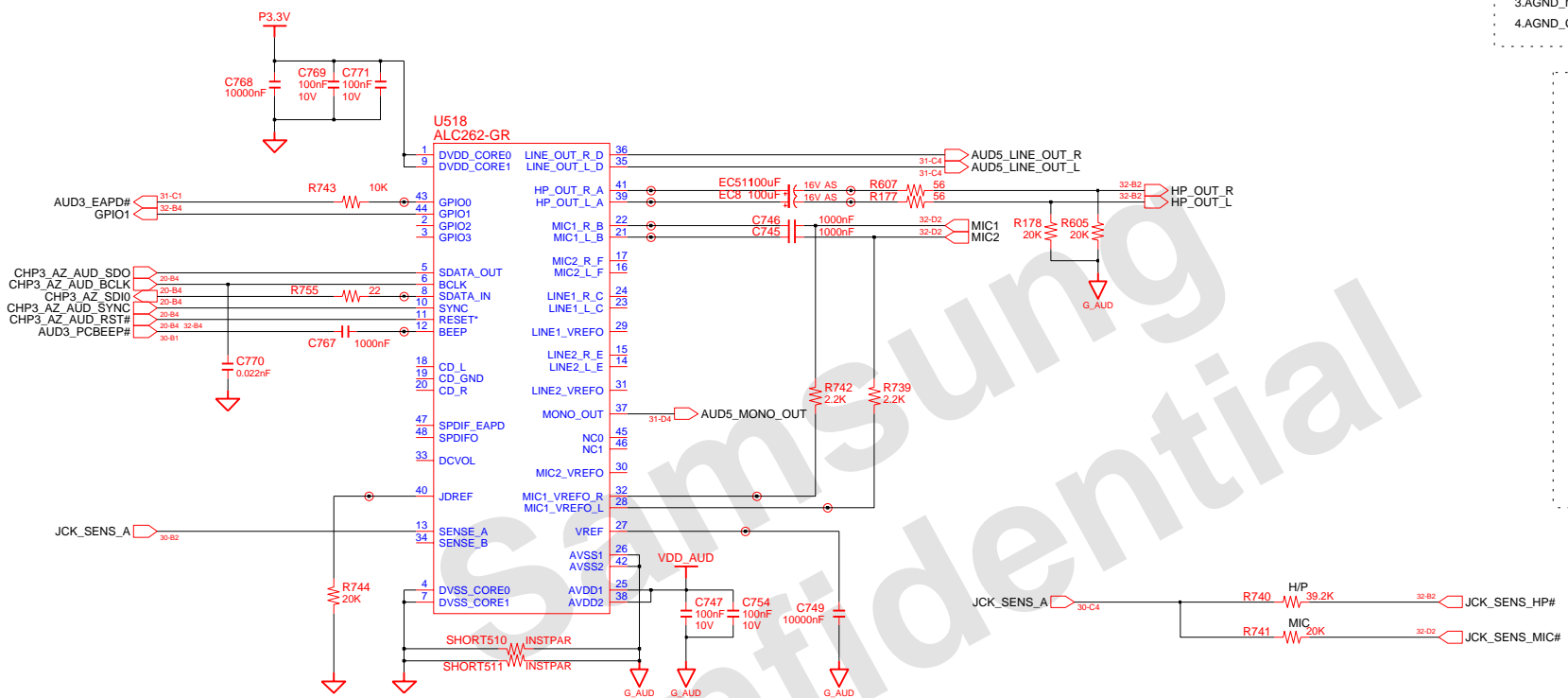
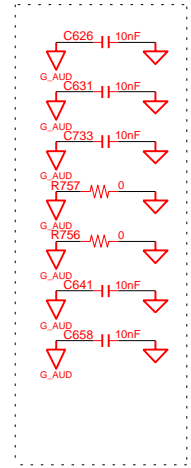
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN MINI CARD	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	29	OF 47
					PART NO.	BA41-00791A

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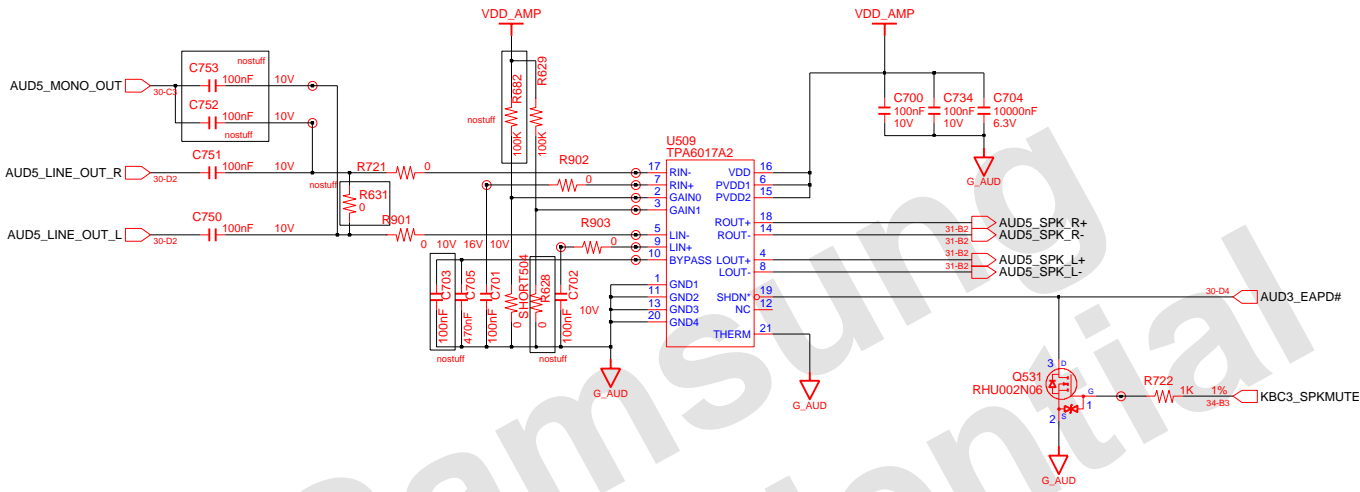
- 1.AGND\_AUD IS AUDIO GROUND
- 2.GND IS DIGITAL GROUND
- 3.AGND\_MIC IS MIC GROUND
- 4.AGND\_CHS IS CHASS GROUND

ALL TYPE IS 1608

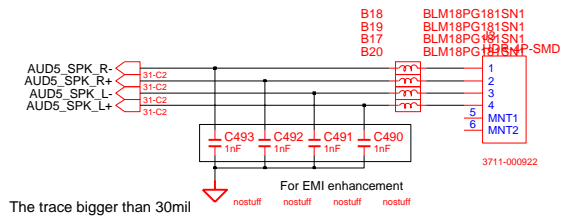
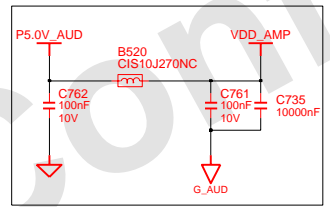


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN AUDIO CODEC	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	30	OF 47

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**AMP\_VDD INTERNAL STEREO SPEAKERS**

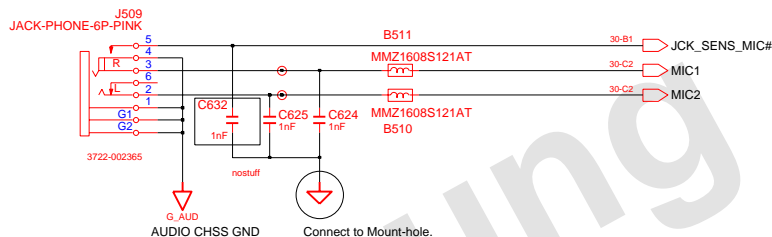


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN LIMITER & AMP	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	31	OF 47

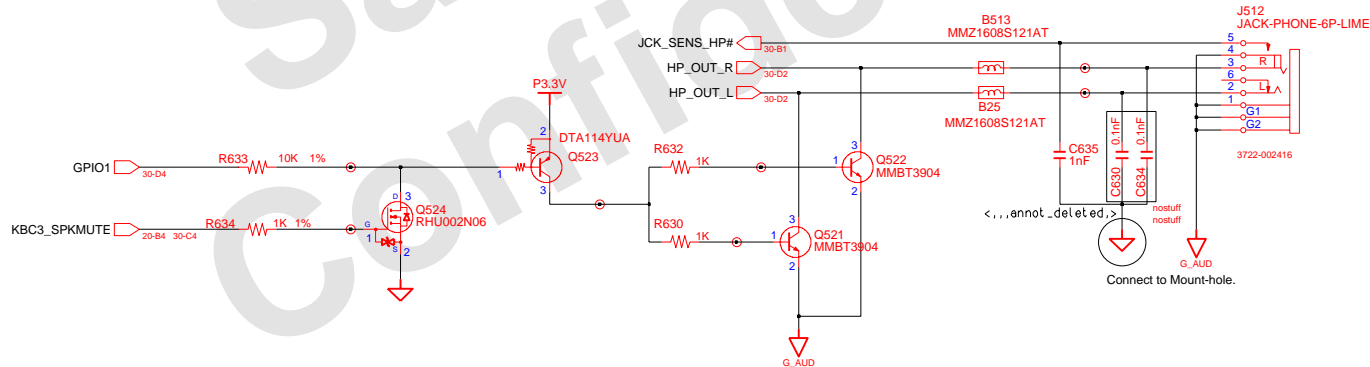
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**MIC JACK**



**HEADPHONE**



The traces led to Audio Jacks have the width over 10mil

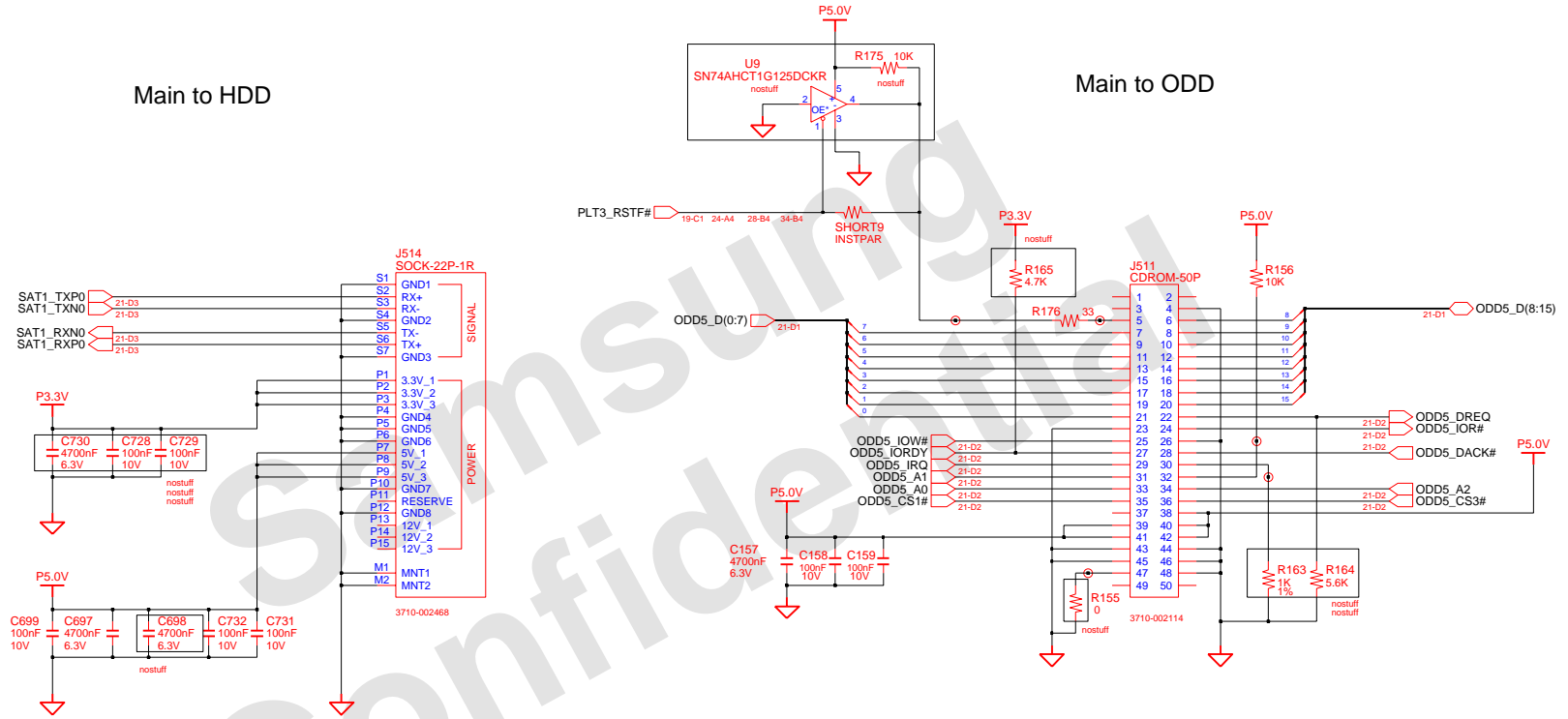
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		MIC & HEADPHONE	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	32	OF 47



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Main to HDD

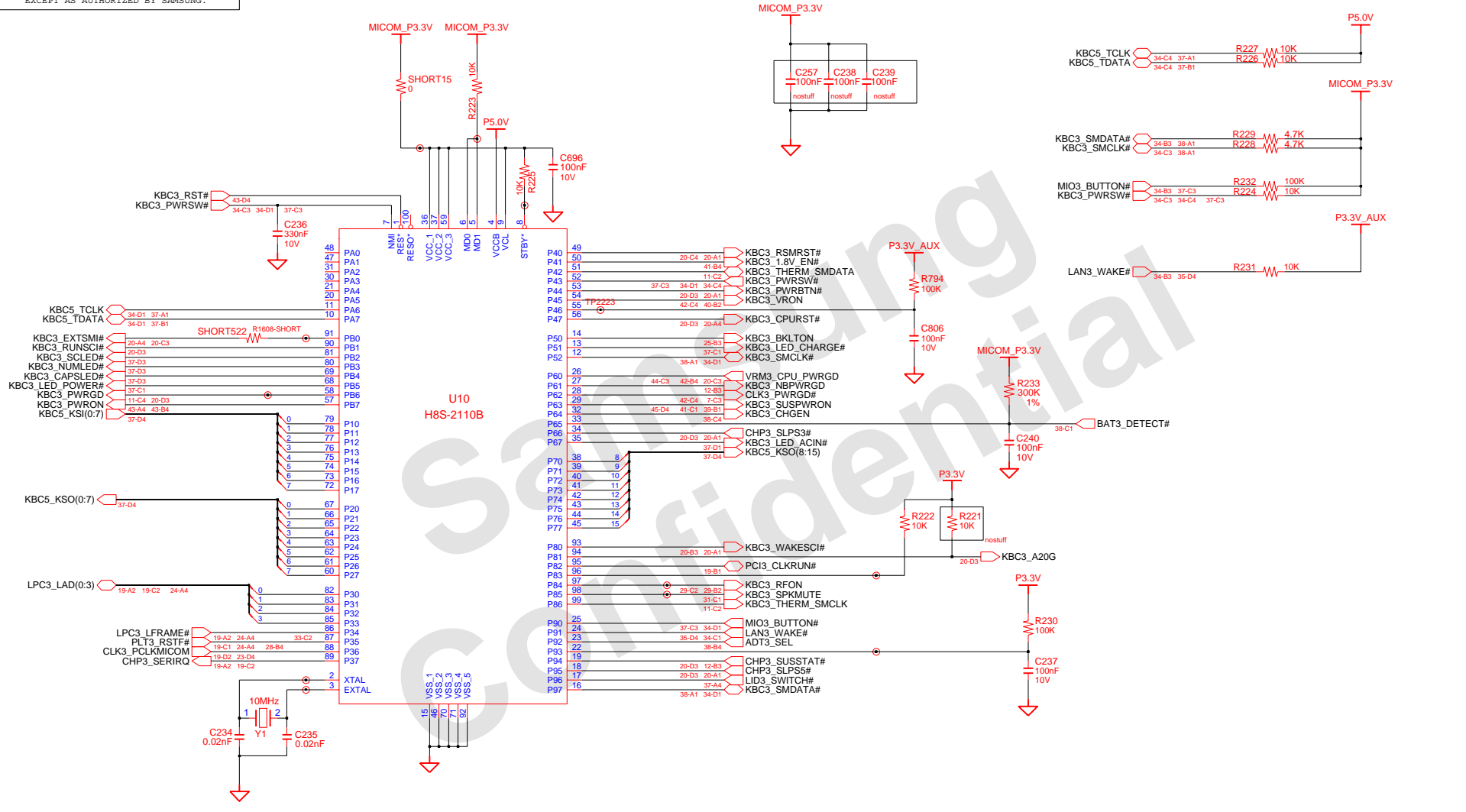
Main to ODD



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER HDD & ODD	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	33	OF 47

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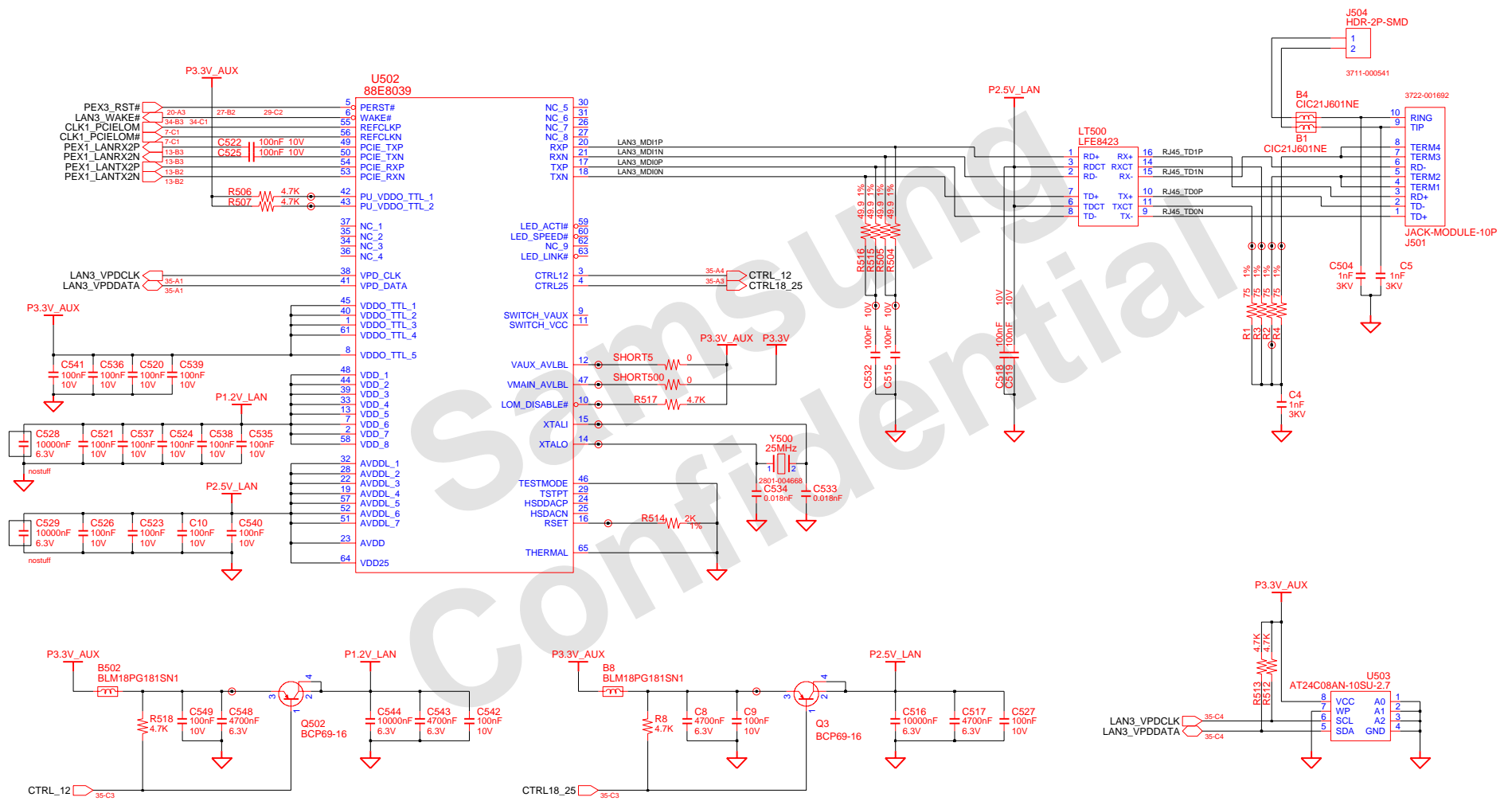


**MICOM Crisis Update**  
 Condition: P90=P91=P92=High(MICOM\_P3V)  
 MD0=MD1=Low(0V)  
 Serial Port: P84 & P85

The removed signal compared from 144pin

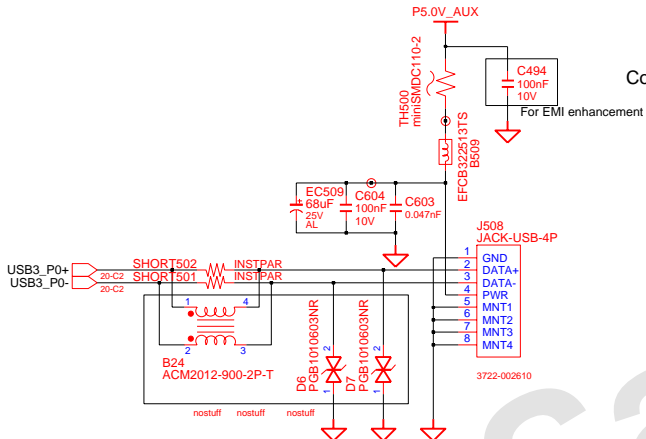
- KBC5\_CAL\_THRM\*
- THRM\_ALERT\*
- LCD3\_BKLTEN
- FAN3\_FDBACK\*
- THERM\_STP\*

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		POWER	
APPROVAL	SJ PARK	REV	1.0		MICOM	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	34	OF 47



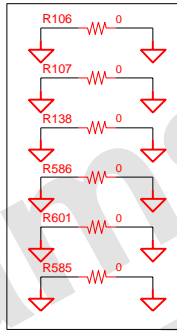
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MAIN LAN		
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	35	OF 47

## Side USB Connector



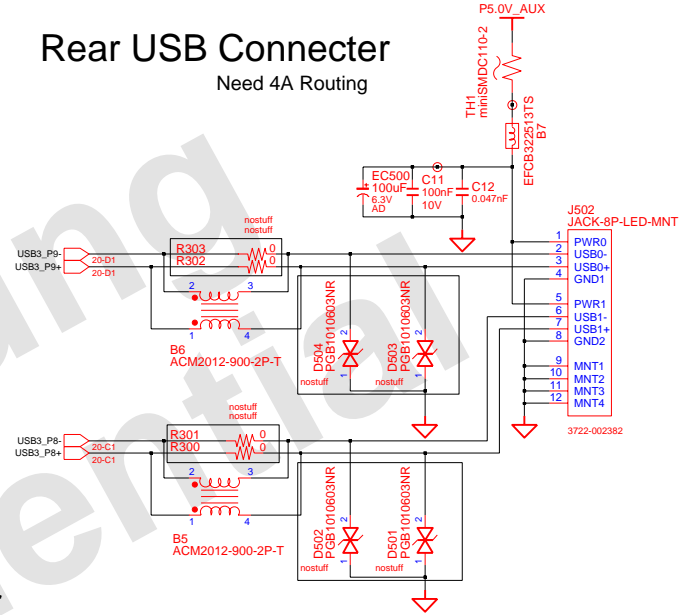
Connect left side USB GND with CPU GND

Top : 3EA Bottom : 3EA

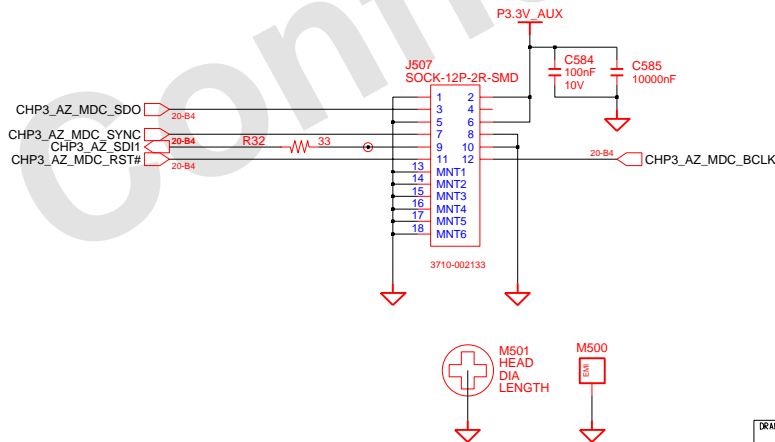


## Rear USB Connector

Need 4A Routing



## MDC Connector

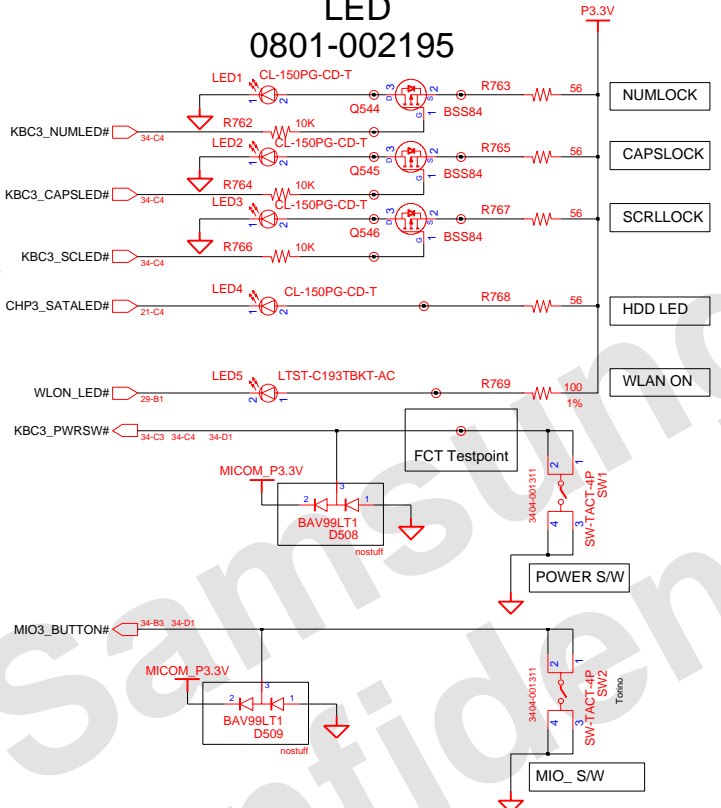
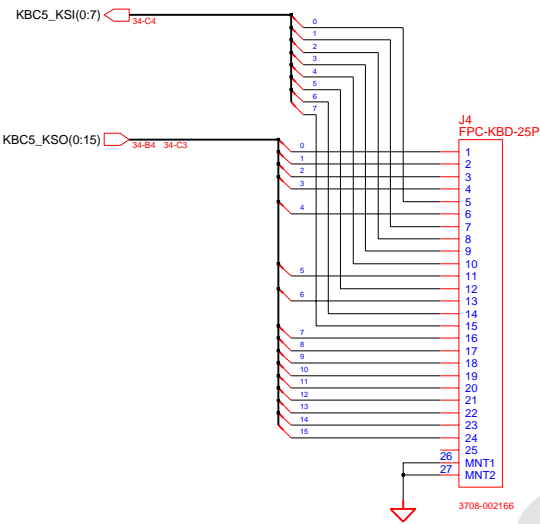


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	USB PORT & MDC Conn.		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	36	OF 47

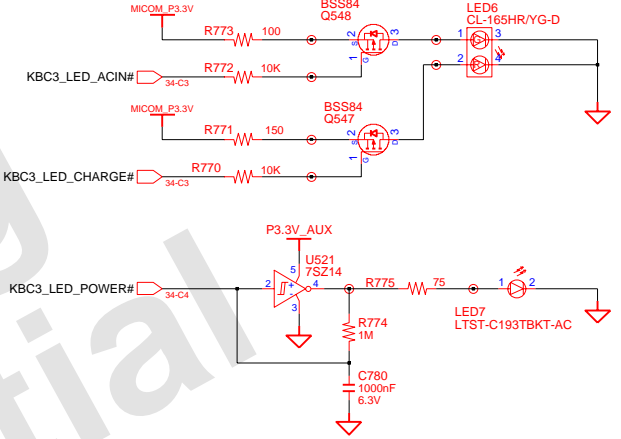
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# LED 0801-002195

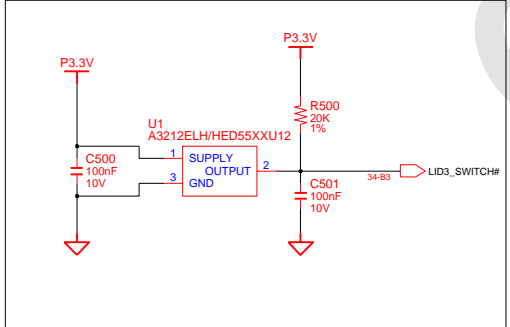
## KEYBOARD



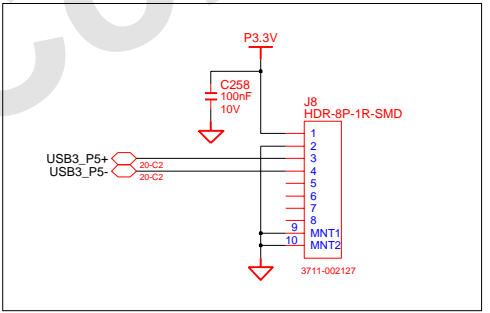
## ADAPTERIN/CHARGING LED



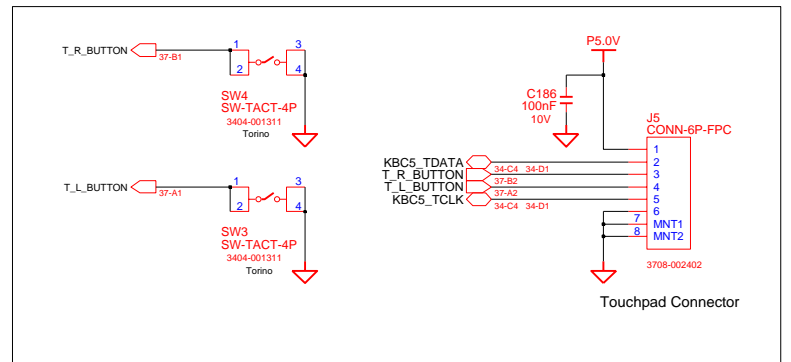
## LID SWITCH



## Bluetooth Interface Factory Option



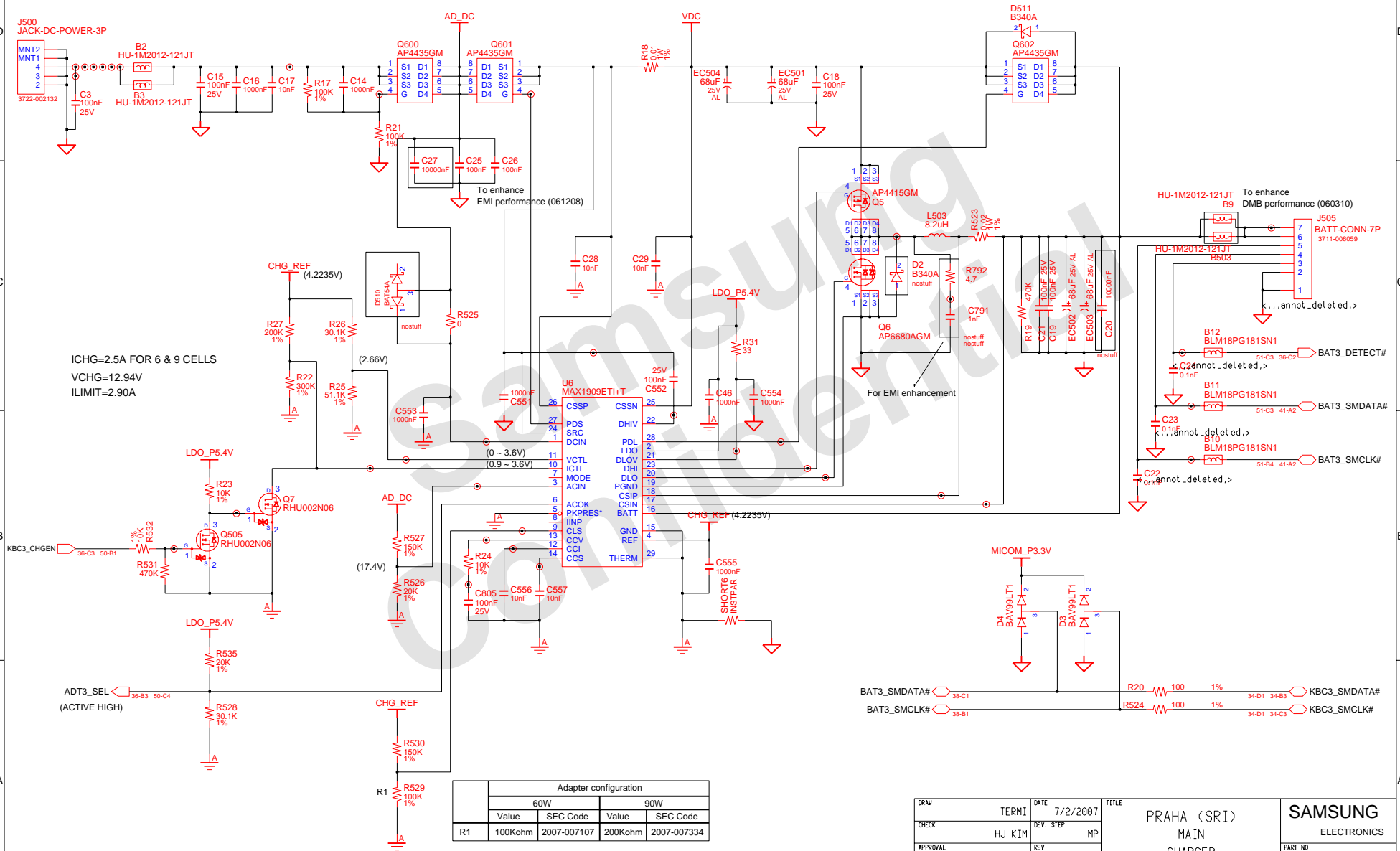
## TOUCHPAD



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	LED & BLUETOOTH	PART NO.	
APPROVAL	SJ PARK	REV	1.0	TOUCHPAD & KBD & LID S/W	BA41-00791A	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	37	OF 47

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# CHARGER & POWER MANAGEMENT



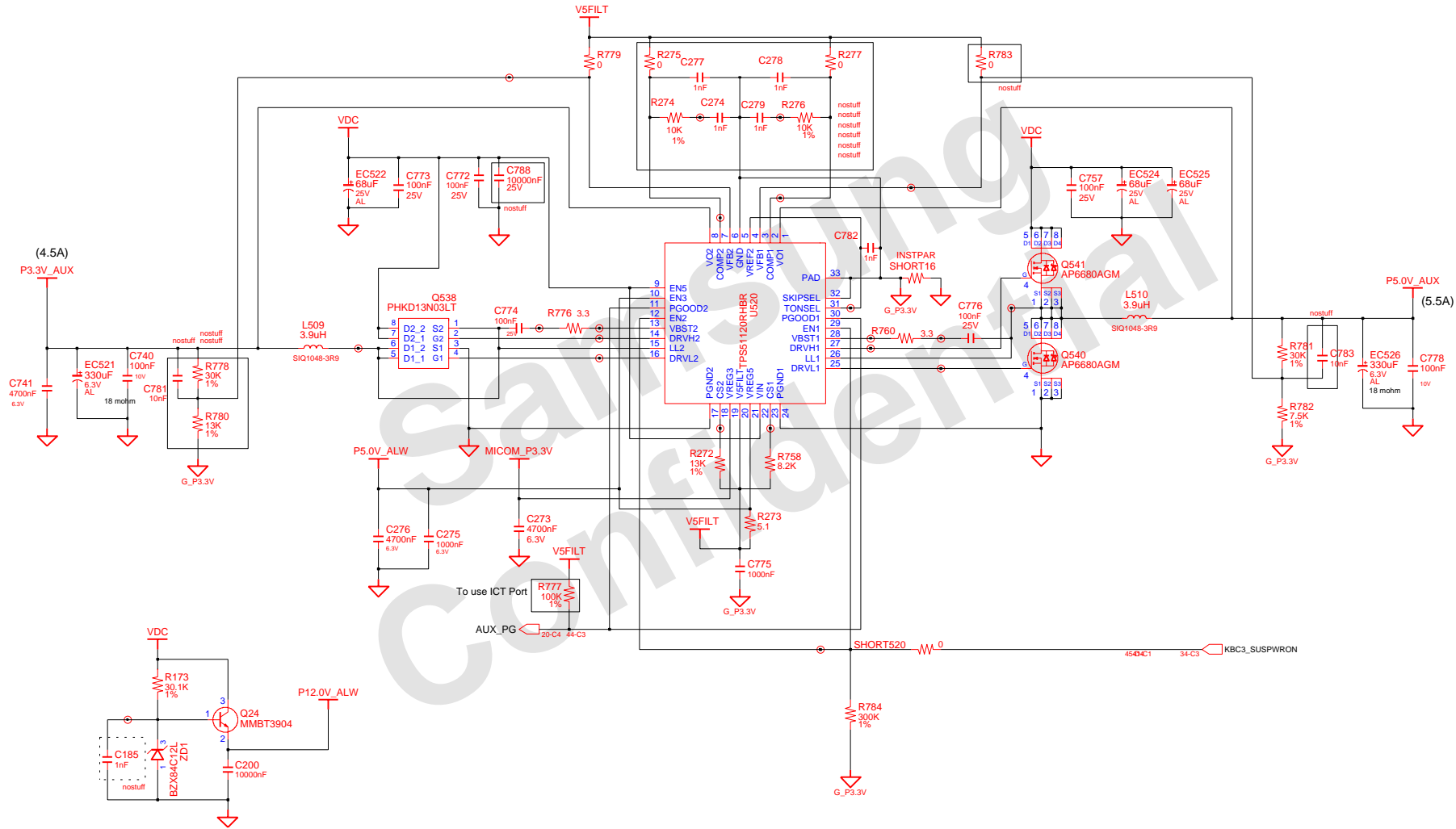
ICHG=2.5A FOR 6 & 9 CELLS  
 VCHG=12.94V  
 ILIMIT=2.90A

Adapter configuration			
60W		90W	
Value	SEC Code	Value	SEC Code
R1	100Kohm	200Kohm	2007-007334

GRW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00791A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	38 OF 47	

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# P3.3V\_AUX & P5V\_AUX

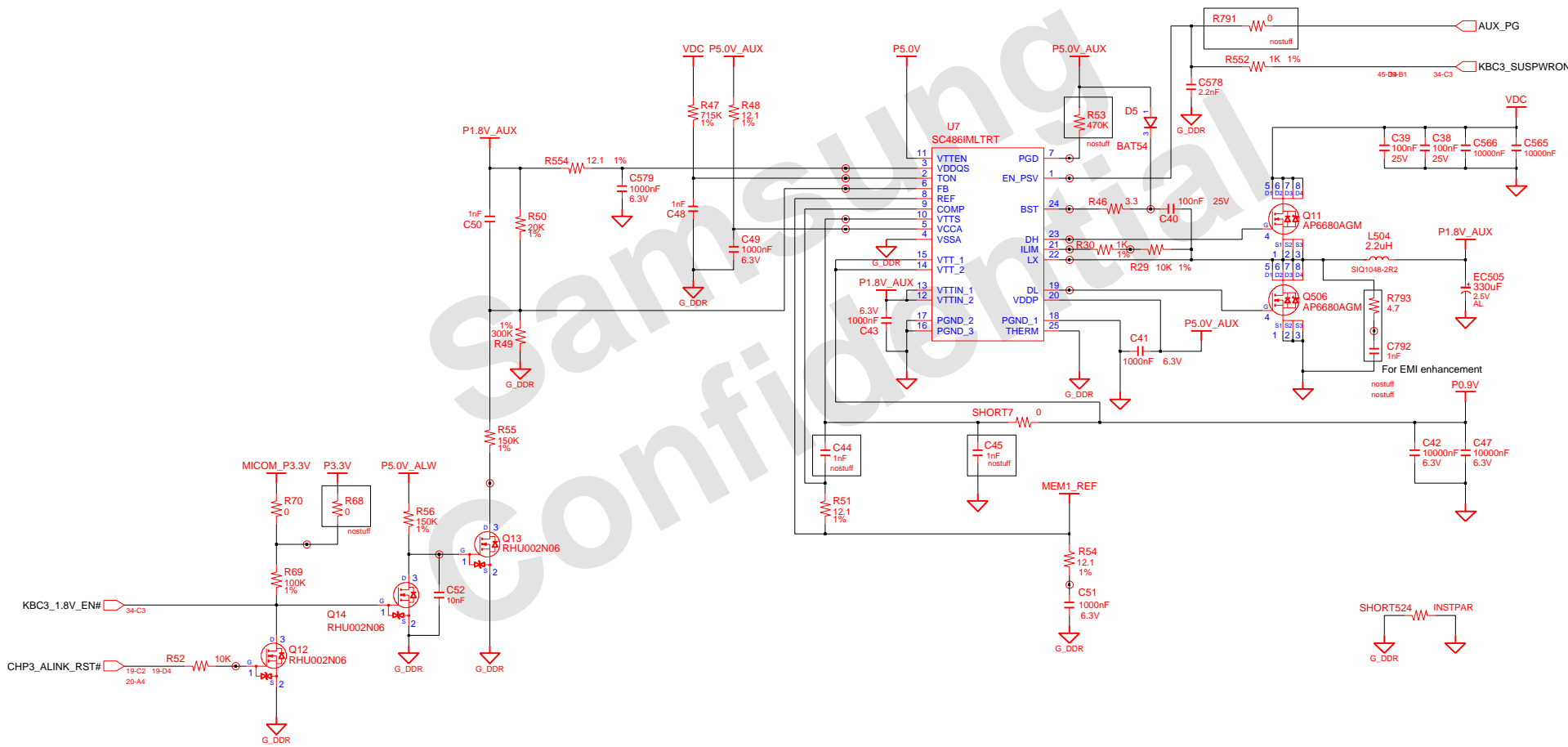


DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) POWER P3.3V_AUX & P5V_AUX	SAMSUNG ELECTRONICS	
CHECK	HJ KIM	REV. STEP	MP				
APPROVAL	SJ PARK	REV	1.0			PART NO.	
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	39	OF	17





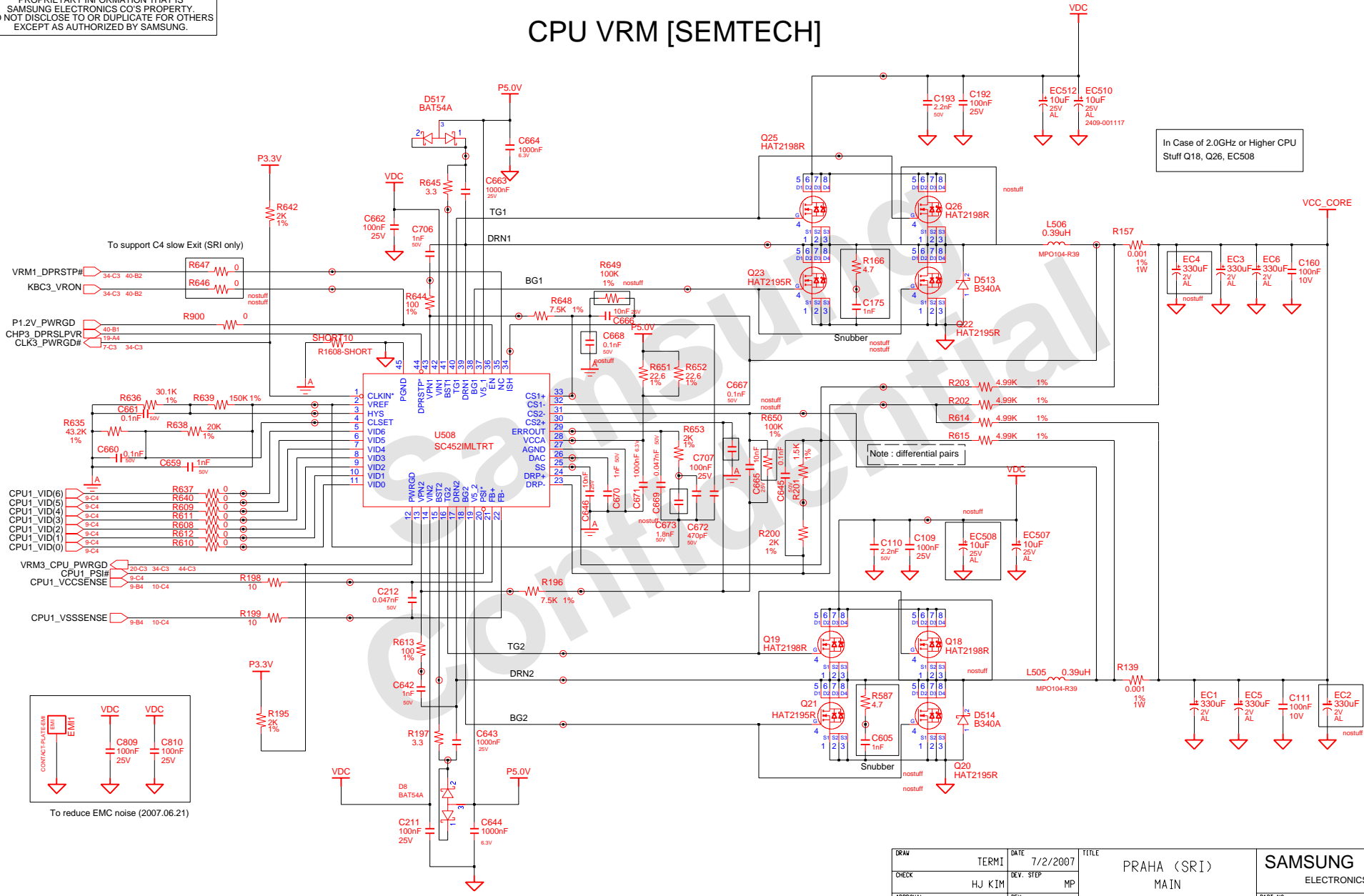
# DDR2 Power



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP		MAIN	
APPROVAL	SJ PARK	REV	1.0		DDR2 POWER	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	41	OF 47

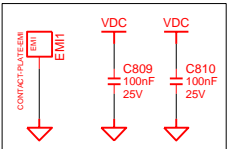
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# CPU VRM [SEMTECH]



In Case of 2.0GHz or Higher CPU  
 Stuff Q18, Q26, EC508

Note : differential pairs

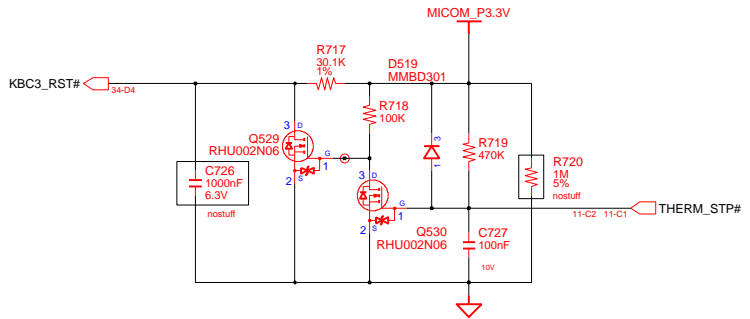


To reduce EMC noise (2007.06.21)

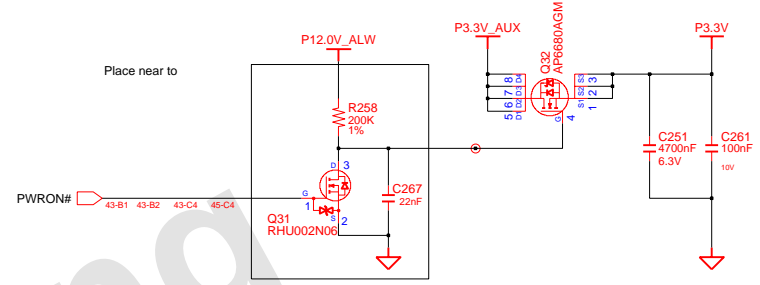
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN CPU VRM	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE 42 OF 47		
					PART NO.	BA41-00791A

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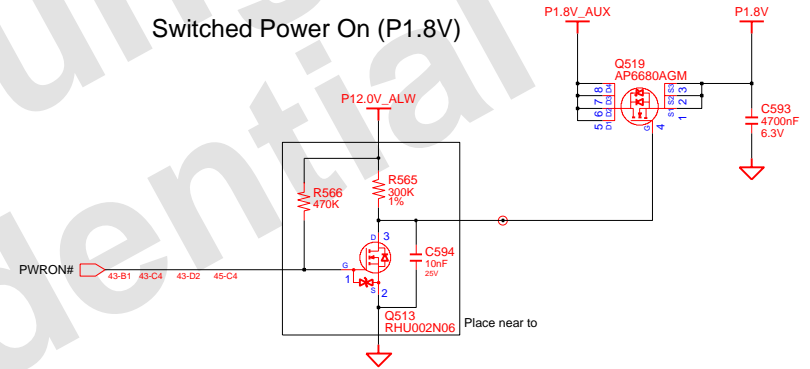
### MICOM RESET



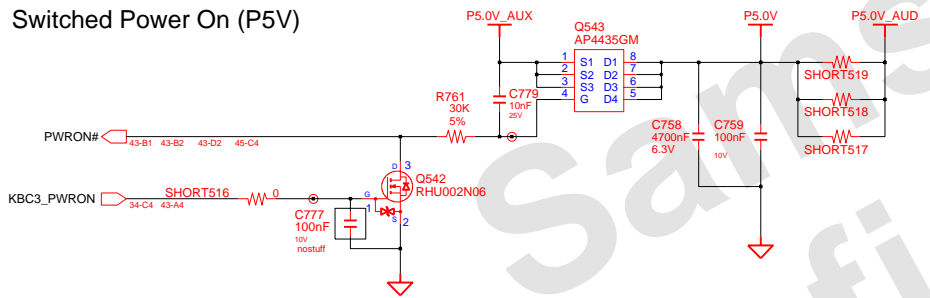
### Switched Power On (P3.3V)



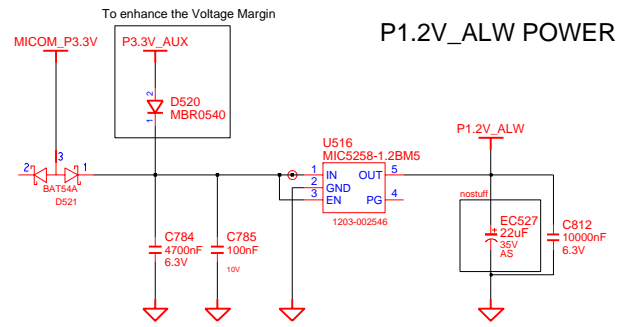
### Switched Power On (P1.8V)



### Switched Power On (P5V)



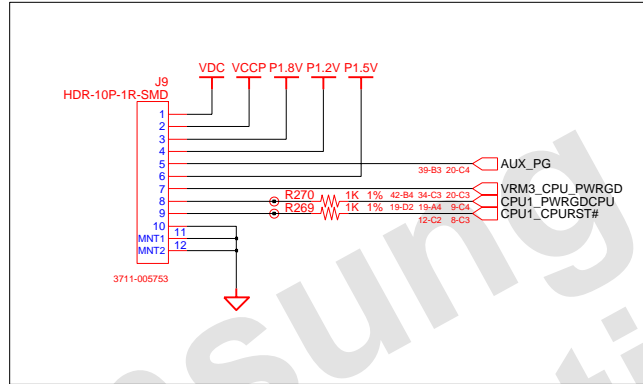
### P1.2V\_ALW POWER



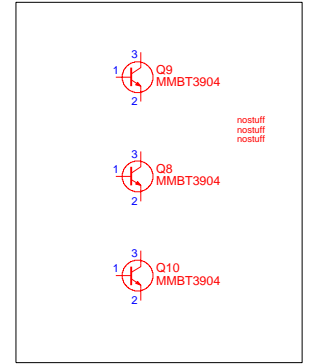
DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAIN	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	MICOM & SWITCHED POWER		
APPROVAL	SJ PARK	REV	1.0		PART NO.	BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	43	OF 47

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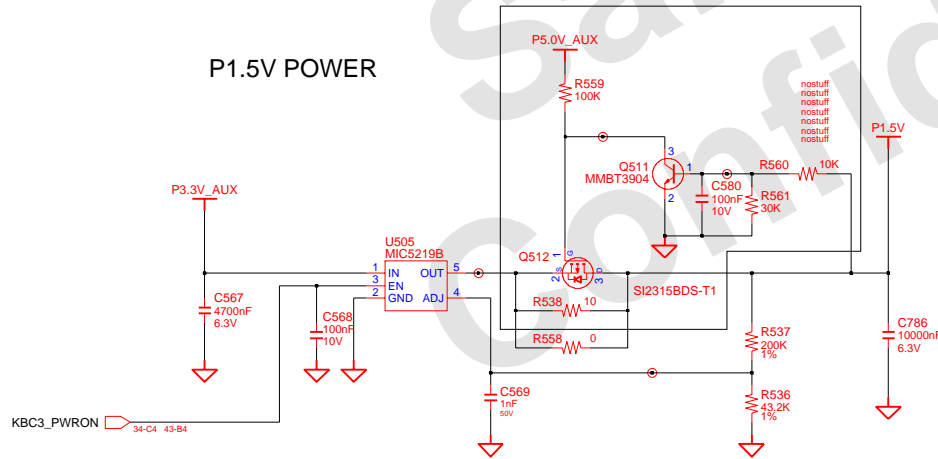
### ICT PORT



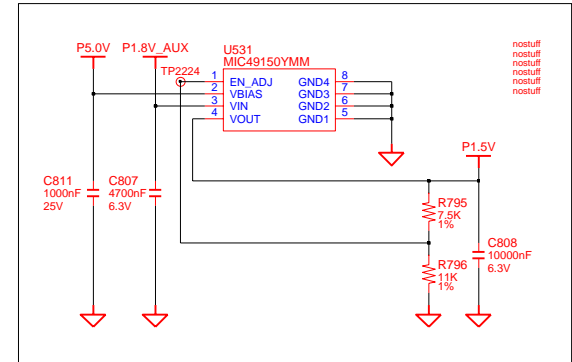
### For Debugging



### P1.5V POWER



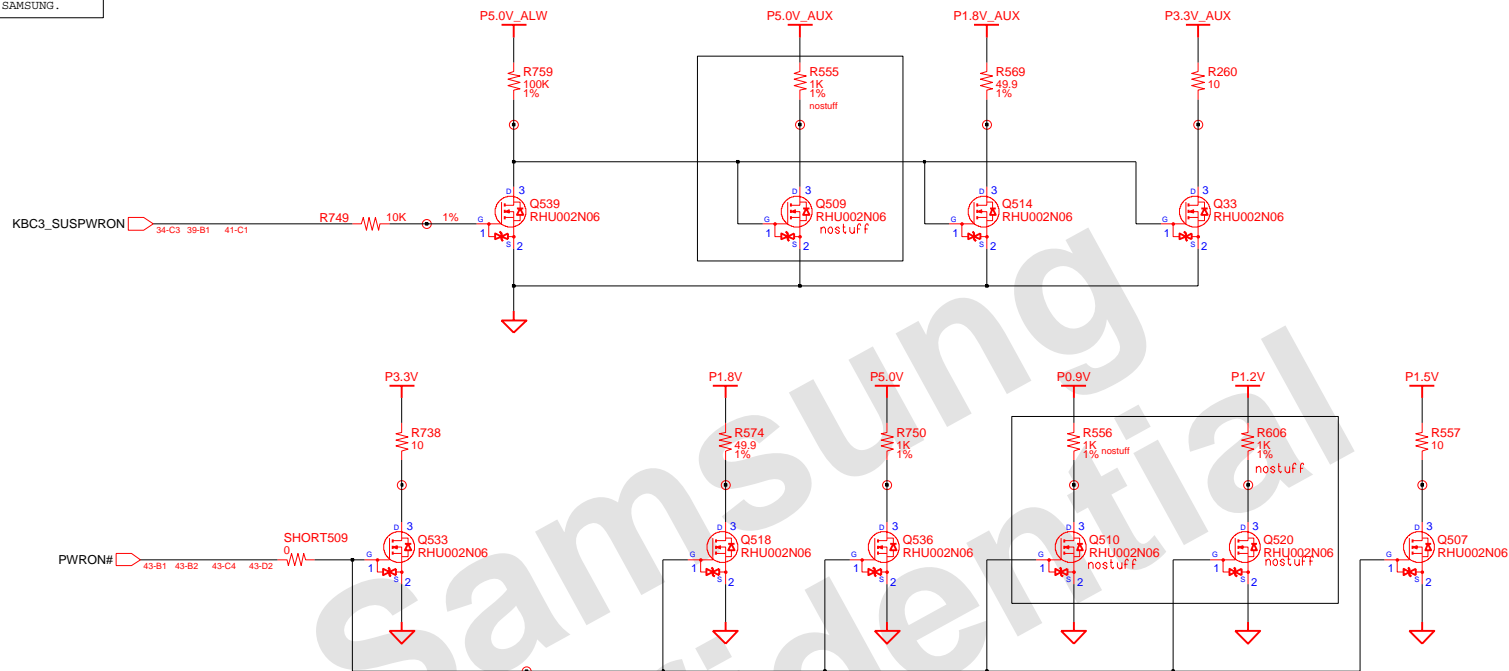
### To make up PCI Express 1.5V rail current margin (nostuff)



GRAM	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	SAMSUNG ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		ICT PORT	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM		PAGE 44	OF 47

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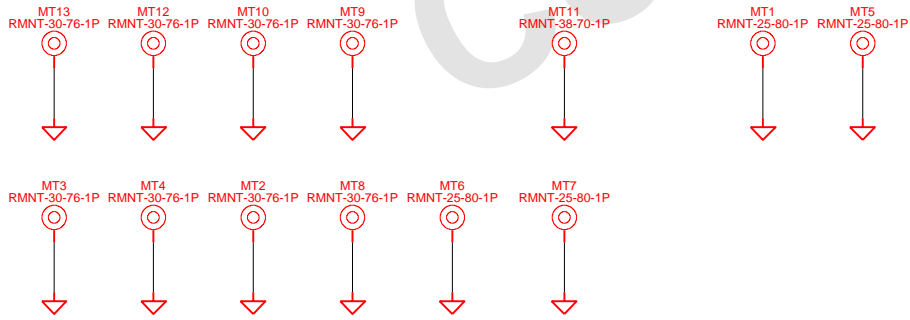
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**System**

**Board**

Located in lower left corner of PCB



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI) MAINBD	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP	POWER DRAW & MNT HOLE		
APPROVAL	SJ PARK	REV	1.0	PART NO. BA41-00791A		PAGE 45 OF 47
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM			

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REV1  
 1 O  
 2 O O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0		TP	PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	46	OF 47

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○AC\_SDOUT  
 ○AD3\_SEL  
 ○AUD3\_EAPD#  
 ○AUD3\_PCBEPP#  
 ○AUD5\_LINE\_OUT\_L  
 ○AUD5\_LINE\_OUT\_R  
 ○AUD5\_MONO\_OUT  
 ○AUD5\_SPK\_L+  
 ○AUD5\_SPK\_L-  
 ○AUD5\_SPK\_R+  
 ○AUD5\_SPK\_R-  
 ○AUX\_PG  
 ○BAT3\_DETECT#  
 ○BAT3\_SMCLK#  
 ○BAT3\_SMDATA#  
 ○CHP3\_ALINK\_RST#  
 ○CHP3\_AZ\_AUD\_BCLK  
 ○CHP3\_AZ\_AUD\_RST#  
 ○CHP3\_AZ\_AUD\_SDO  
 ○CHP3\_AZ\_AUD\_SYNC  
 ○CHP3\_AZ\_MDC\_BCLK  
 ○CHP3\_AZ\_MDC\_RST#  
 ○CHP3\_AZ\_MDC\_SDO  
 ○CHP3\_AZ\_MDC\_SYNC  
 ○CHP3\_AZ\_SDIO  
 ○CHP3\_AZ\_SDIO1  
 ○CHP3\_BIOSWP#  
 ○CHP3\_DPRSPLPWR  
 ○CHP3\_NBRST#  
 ○CHP3\_SATALED#  
 ○CHP3\_SBPME#  
 ○CHP3\_SBTMRTRIP#  
 ○CHP3\_SERIRO  
 ○CHP3\_SLP3#  
 ○CHP3\_SLP35#  
 ○CHP3\_SPKR  
 ○CHP3\_SUSSTAT#  
 ○CPU1\_A20M#  
 ○CPU1\_ADS#  
  
 ○CPU1\_BNR#  
 ○CPU1\_BPRI#  
 ○CPU1\_BREQ#  
 ○CPU1\_BSEL0  
 ○CPU1\_BSEL1  
 ○CPU1\_BSEL2  
 ○CPU1\_CPURST#  
 ○CLK3\_DBGCLPC  
 ○CLK3\_IQH14  
 ○CLK3\_NB14M  
 ○CLK3\_PCLKMICOM  
 ○CLK3\_PWRGD#  
 ○CLK3\_USB48  
  
 ○CPU1\_DBSY#  
 ○CPU1\_DEFR#  
 ○CPU1\_DPRS1P#  
 ○CPU1\_DPSLP#  
 ○CPU1\_DPWR#  
 ○CPU1\_DRDY#

○CPU1\_FERR#  
 ○CPU1\_HIT#  
 ○CPU1\_HITM#  
 ○CPU1\_IGNNE#  
 ○CPU1\_INIT#  
 ○CPU1\_INTR#  
 ○CPU1\_LOCK#  
 ○CPU1\_NMI#  
 ○CPU1\_PSI#  
 ○CPU1\_PWRGDCCPU  
  
 ○CPU1\_RS0#  
 ○CPU1\_RS1#  
 ○CPU1\_RS2#  
 ○CPU1\_SLP#  
 ○CPU1\_SMI#  
 ○CPU1\_TCK  
 ○CPU1\_TDI  
 ○CPU1\_THRMTRIP#  
 ○CPU1\_TMS  
 ○CPU1\_TRDY#  
 ○CPU1\_TRST#  
 ○CPU1\_VCCSENSE  
 ○CPU1\_VID(0)  
 ○CPU1\_VID(1)  
 ○CPU1\_VID(2)  
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 ○CPU1\_VID(4)  
 ○CPU1\_VID(5)  
 ○CPU1\_VID(6)  
 ○CPU1\_VSSSENSE  
 ○CPU2\_THERMIDA  
 ○CPU2\_THERMDC  
 ○CPU3\_THRMTRIP#  
 ○CRT3\_BLUE  
 ○CRT3\_DDCCLK  
 ○CRT3\_DODDATA  
 ○CRT3\_GREEN  
 ○CRT3\_RED  
 ○CRT5\_HSYNC  
 ○CRT5\_VSYNC  
 ○CTRL18\_25  
 ○CTRL12  
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 ○EXP3\_CPPPE#

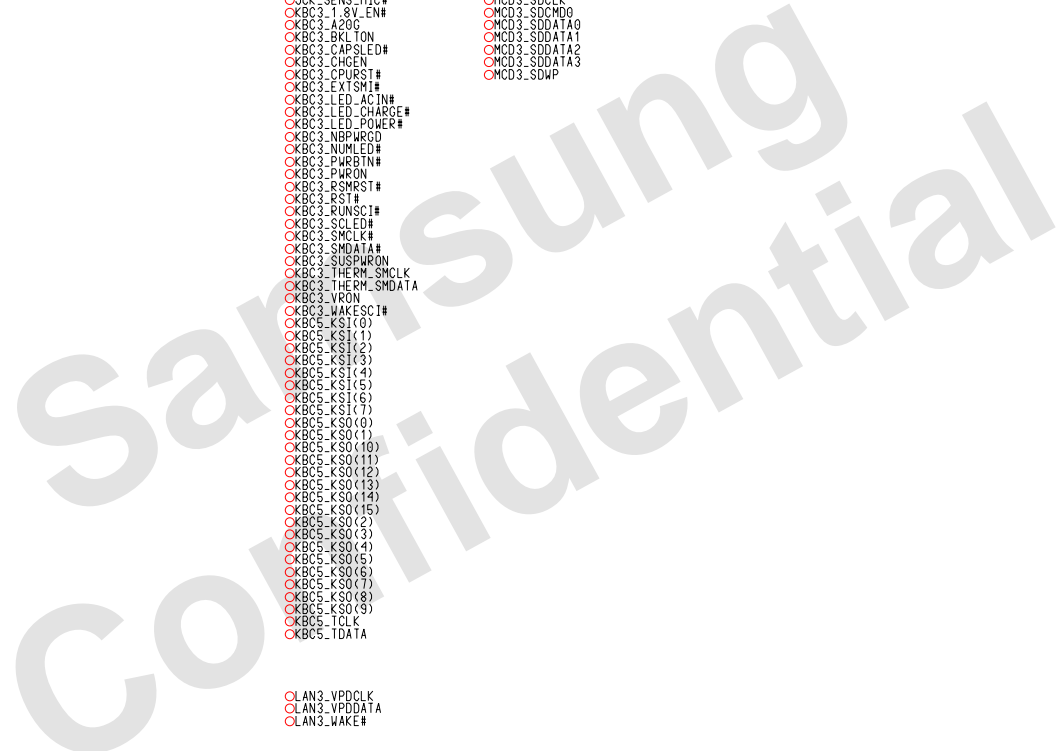
○EXP3\_CPUSB#  
 ○EXP3\_PPERST#  
 ○CPU1\_HITM#  
 ○FANS\_FBEEP#  
 ○FANS\_VDD  
 ○GPIO1  
 ○HP\_OUT\_L  
 ○HP\_OUT\_R  
 ○ITP3\_DBRESET#  
 ○ITP3\_SYSRST#  
 ○JCK\_SENS\_A  
 ○JCK\_SENS\_HP#  
 ○JCK\_SENS\_MIC#  
 ○KBC3\_18V\_EN#  
 ○KBC3\_A20G  
 ○KBC3\_BKLTON  
 ○KBC3\_CAPSLED#  
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 ○KBC3\_CPURST#  
 ○KBC3\_EXTSMI#  
 ○KBC3\_LED\_ACIN#  
 ○KBC3\_LED\_CHARGE#  
 ○KBC3\_LED\_POWER#  
 ○KBC3\_NBPWRGD  
 ○KBC3\_NUMLED#  
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 ○KBC3\_PWRON  
 ○KBC3\_SMRST#  
 ○KBC3\_RST#  
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 ○KBC3\_SCLE#  
 ○KBC3\_SMCLK#  
 ○KBC3\_SMDATA#  
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 ○KBC3\_THERM\_SMCLK  
 ○KBC3\_THERM\_SMDATA  
 ○KBC3\_VIRON  
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 ○KBC5\_KSI(1)  
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 ○KBC5\_KSO(8)  
 ○KBC5\_KSO(9)  
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 ○KBC5\_TDATA

○LAN3\_VPDCLK  
 ○LAN3\_VPDDATA  
 ○LAN3\_WAKE#

○LCD3\_BKLCTRL  
 ○LCD3\_BKLTON

○LCD3\_BKLTON  
 ○LCD3\_EDID\_CLK  
 ○LCD3\_EDID\_DATA  
 ○CD3\_VDDEN  
 ○ID3\_SWITCH#  
 ○PC3\_LAD(0)  
 ○PC3\_LAD(1)  
 ○PC3\_LAD(2)  
 ○PC3\_LAD(3)  
 ○PC3\_LFRAME#  
 ○MCD3\_SDCD#  
 ○MCD3\_SDCLK  
 ○MCD3\_SDCMDQ  
 ○MCD3\_SDDATA0  
 ○MCD3\_SDDATA1  
 ○MCD3\_SDDATA2  
 ○MCD3\_SDDATA3  
 ○MCD3\_SDWP

○MIC1  
 ○MIC2  
 ○MINIPCIE3\_CLKREQ#  
 ○MIO3\_BUTTON#



DRAW	TERMI	DATE	7/2/2007	TITLE	PRAHA (SRI)	<b>SAMSUNG</b> ELECTRONICS
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			PART NO. BA41-00791A
MODULE CODE	undefined	LAST EDIT	July 2, 2007 11:28:38 PM	PAGE	47	OF 47

