Thurman UMA Schematics Document

uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

2007-11-19

REV : -1 (DELL:A00)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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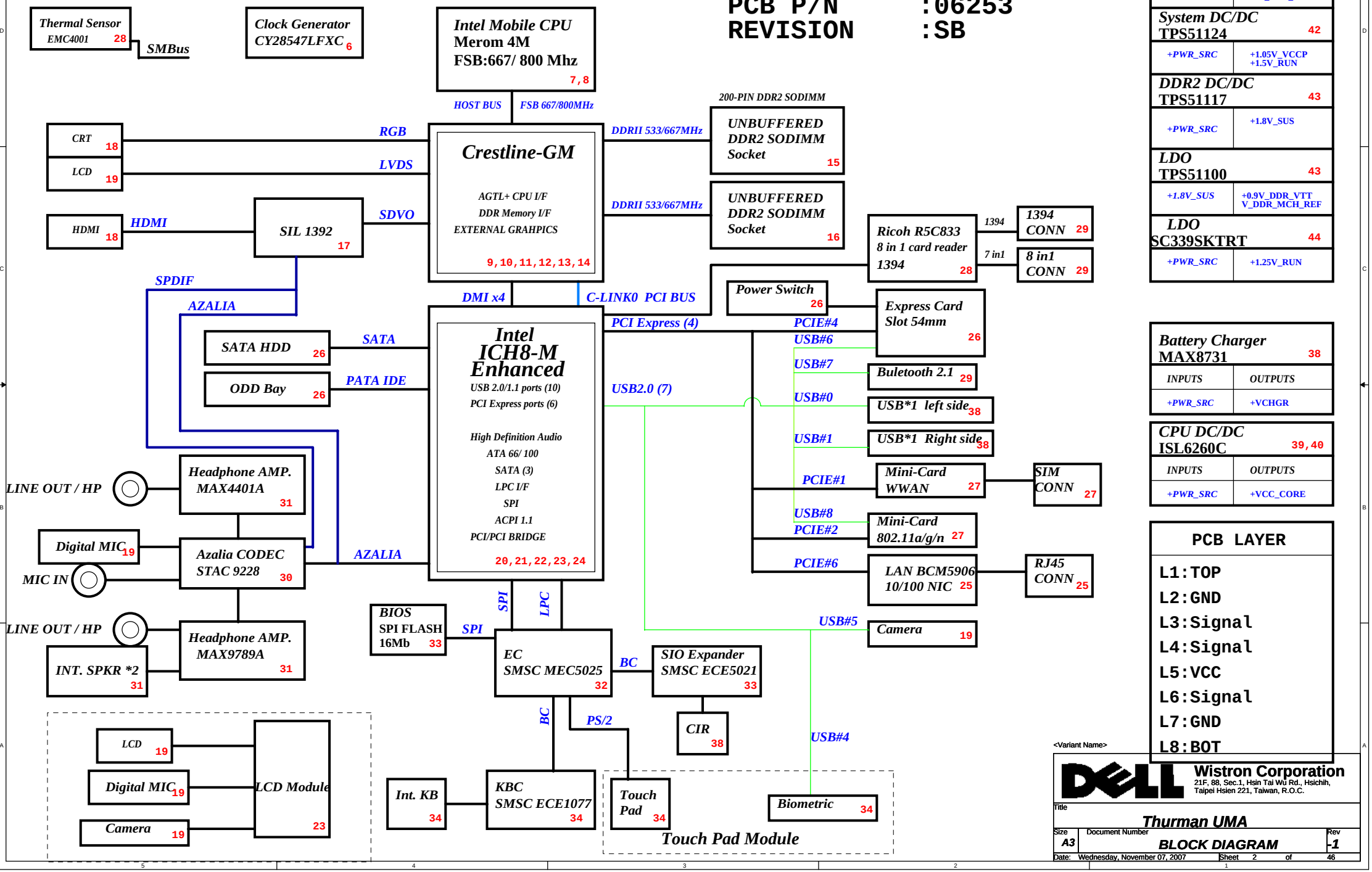
Title	Thurman UMA	
Size: A3	Document Number: COVER PAGE	Rev: -1
Date: Friday, January 18, 2008	Sheet 1 of 46	

Thurman UMA Block Diagram

Project code:91.4C301.001
PCB P/N :06253
REVISION :SB



System DC/DC TPS51120 41	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO

System DC/DC TPS51124 42	
+PWR_SRC	+1.05V_VCCP +1.5V_RUN

DDR2 DC/DC TPS51117 43	
+PWR_SRC	+1.8V_SUS

LDO TPS51100 43	
+1.8V_SUS	+0.9V_DDR_VTT V_DDR_MCH_REF

LDO SC339SKTRT 44	
+PWR_SRC	+1.25V_RUN

Battery Charger MAX8731 38	
INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 39,40	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

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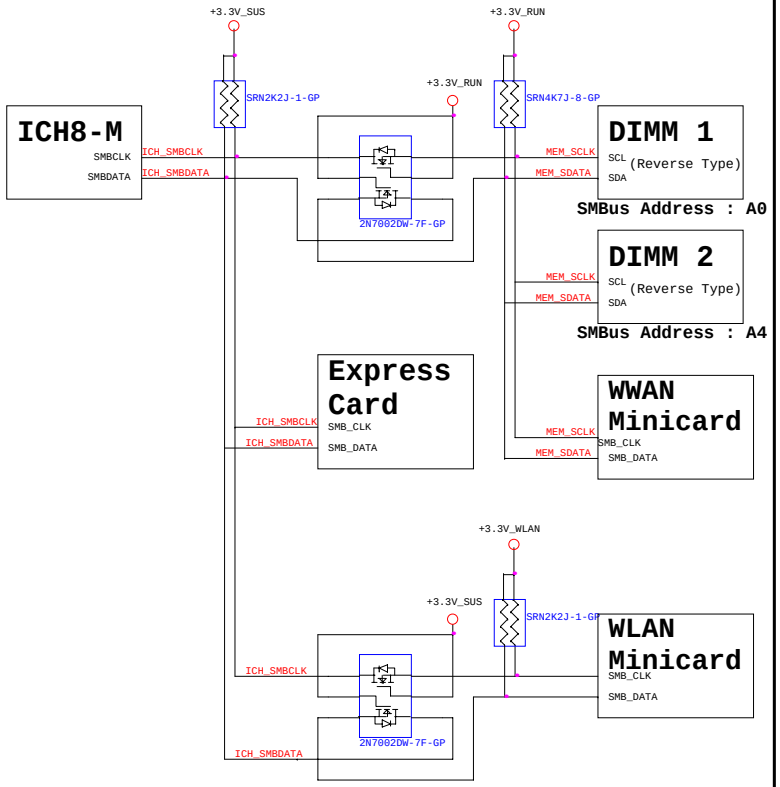
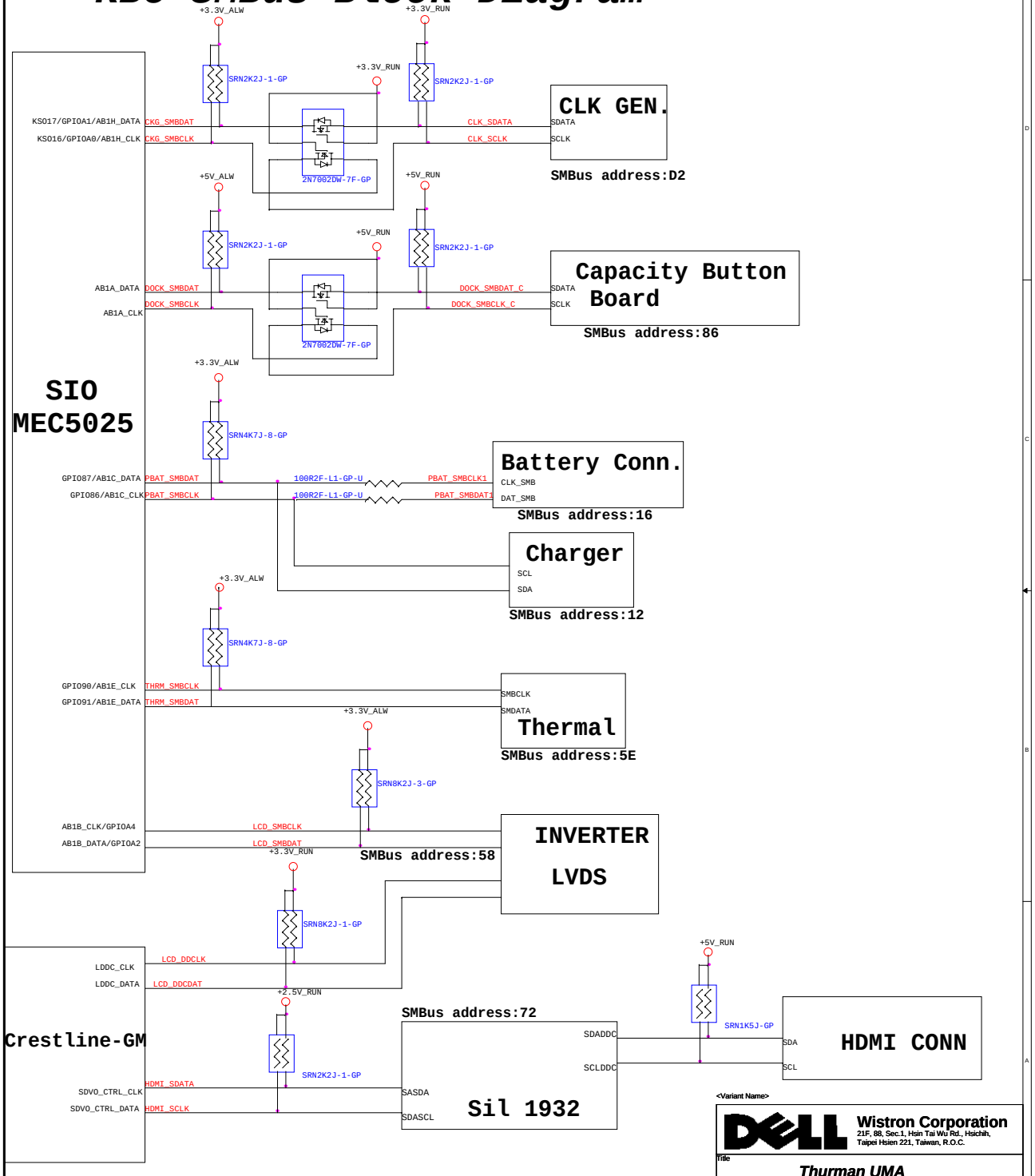
Size: A3 | Document Number: BLOCK DIAGRAM | Rev: -1
Date: Wednesday, November 07, 2007 | Sheet 2 of 46

ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



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Size	Document Number	Rev
C	SMBus Block Diagram	-1

Date: Wednesday, November 07, 2007 Sheet 3 of 46

CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD	tp3	AZ_DOUT_ICH	Description
0	0		RSVD
0	1		Enter XOR Chain
1	0		Normal Operation(default)
1	1		Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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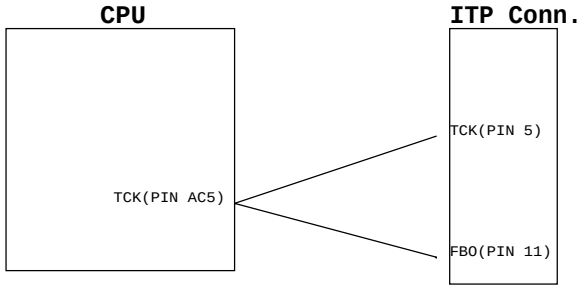
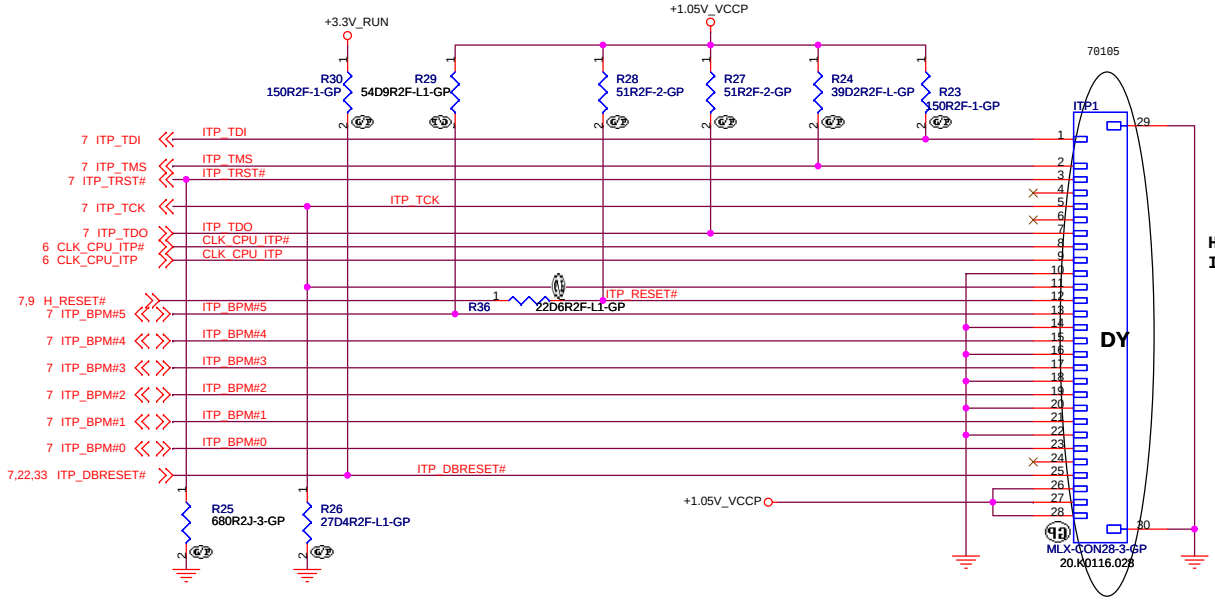
Size: A3 | Document Number: Table of Content | Rev: -1

Date: Wednesday, November 07, 2007 | Sheet 4 of 46





H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max)

+1.05VRUN use Decoupling Capacitor close
ITP connector 100 mil (max)

ITP Debug Conn.

<Variant Name>

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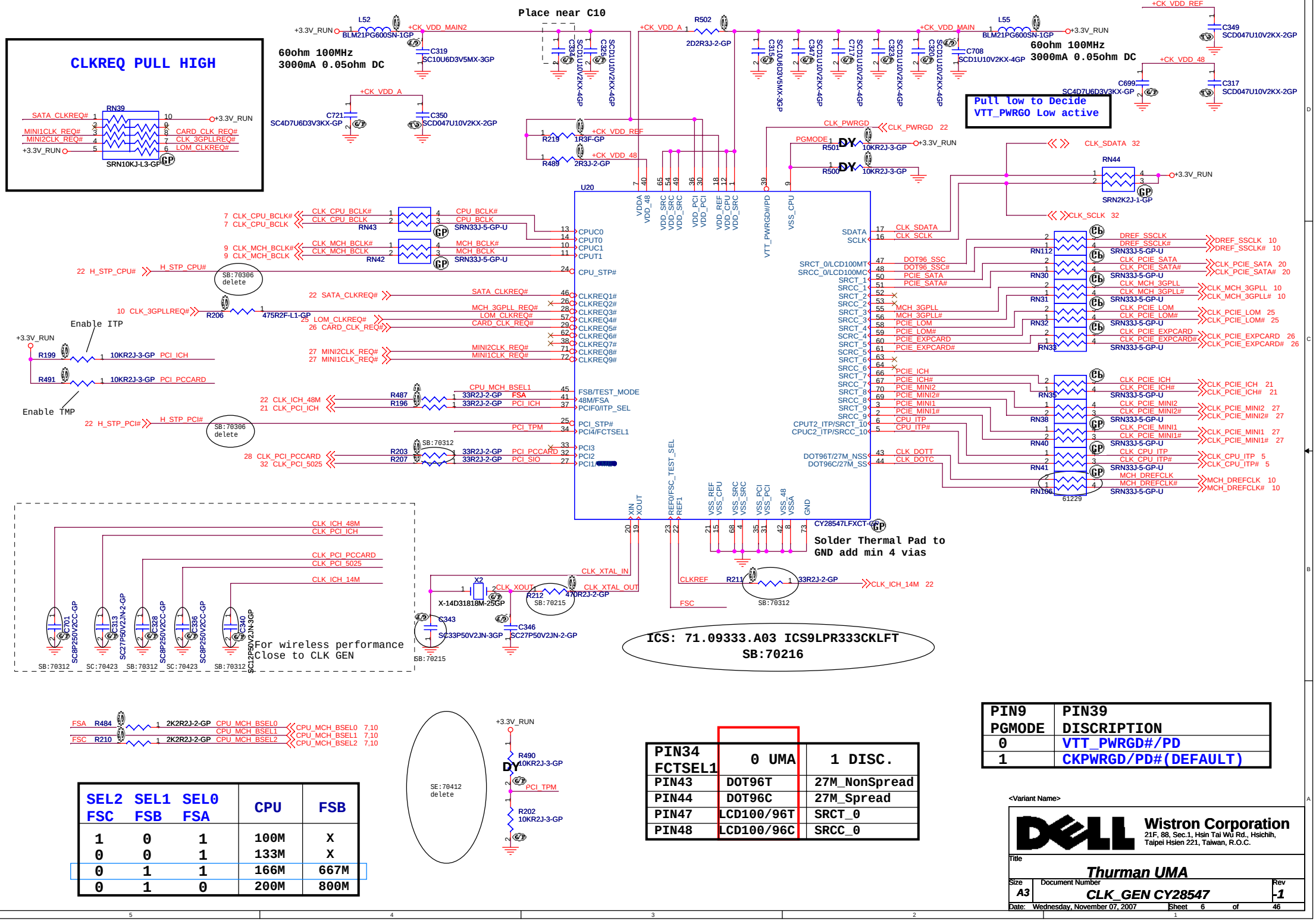
Size: *A3*	Document Number: *ITP Debug*	Rev: *-1*
Date: Wednesday, November 07, 2007	Sheet 5 of 46	



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PIN34 FCTSEL1	0 UMA	1 DISC.
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

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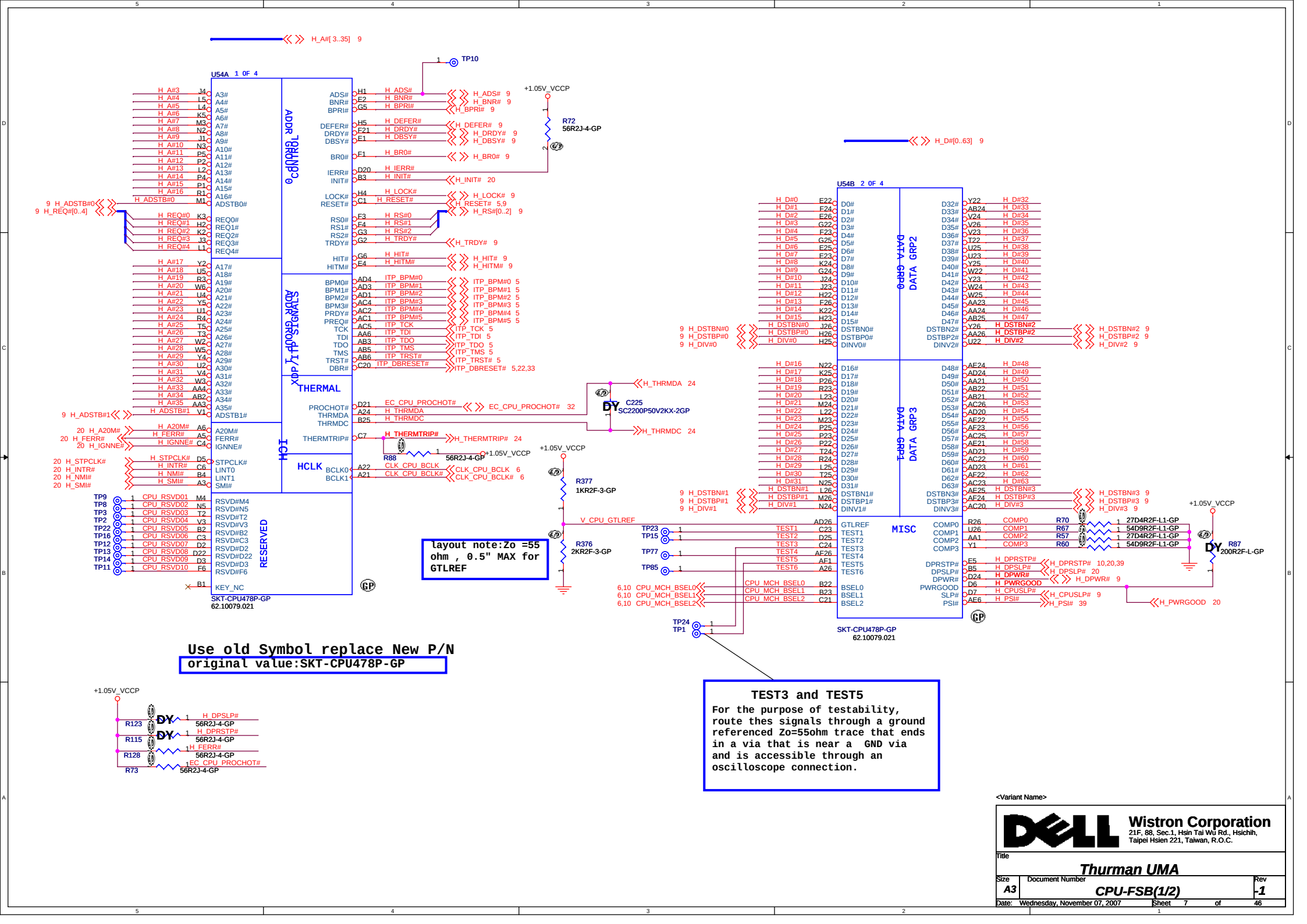
Size	Document Number	Rev
A3	CLK_GEN CY28547	-1

Date: Wednesday, November 07, 2007 Sheet 6 of 46


H_A#[3..35] 9
TP10
U54A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
ASYNC GTL SIGNALS
THERMAL
HCLK
RESERVED
ITCH
A3# A4# A5# A6# A7# A8# A9# A10# A11# A12# A13# A14# A15# A16# ADSTB0#
REQ0# REQ1# REQ2# REQ3# REQ4#
A17# A18# A19# A20# A21# A22# A23# A24# A25# A26# A27# A28# A29# A30# A31# A32# A33# A34# A35# ADSTB1#
A20M# FERR# IGNNE#
STPCLK# LINT0 LINT1 SMI#
RSVD#M4 RSVD#N5 RSVD#T2 RSVD#V3 RSVD#B2 RSVD#C3 RSVD#D2 RSVD#D22 RSVD#D3 RSVD#F6
KEY_NC
ADS# BNR# BPRI#
DEFER# DRDY# DBSY#
BR0#
IERR# INIT#
LOCK# RESET#
RS0# RS1# RS2# TRDY#
HIT# HITM#
BPM0# BPM1# BPM2# BPM3# PRDY# PREQ#
TCK TDI TDO TMS TRST# DBR#
PROCHOT# THRMDA THRMDC
THERMTRIP#
BCLK0 BCLK1
SKT-CPU478P-GP
62.10079.021
H_ADS# H_BNR# H_BPRI#
H_DEFER# H_DRDY# H_DBSY#
H_BR0#
H_IERR# H_INIT#
H_LOCK# H_RESET#
H_RS#0 H_RS#1 H_RS#2 H_TRDY#
H_HIT# H_HITM#
ITP_BPM#0 ITP_BPM#1 ITP_BPM#2 ITP_BPM#3 ITP_BPM#4 ITP_BPM#5
ITP_TCK ITP_TDI ITP_TDO ITP_TMS ITP_TRST# ITP_DBRESET#
EC_CPU_PROCHOT#
H_THRMDA H_THRMDC
H_THERMTRIP#
CLK_CPU_BCLK CLK_CPU_BCLK#
+1.05V_VCCP
R72 56R2J-4-GP
R88 56R2J-4-GP
R377 1KR2F-3-GP
R376 2KR2F-3-GP
C225 SC2200P50V2KX-2GP
DY
V_CPU_GTLREF
layout note:Zo =55 ohm , 0.5" MAX for GTLREF
H_D#[0..63] 9
U54B 2 OF 4
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
D0# D1# D2# D3# D4# D5# D6# D7# D8# D9# D10# D11# D12# D13# D14# D15# DSTBN0# DSTBP0# DINV0#
D16# D17# D18# D19# D20# D21# D22# D23# D24# D25# D26# D27# D28# D29# D30# D31# DSTBN1# DSTBP1# DINV1#
D32# D33# D34# D35# D36# D37# D38# D39# D40# D41# D42# D43# D44# D45# D46# D47# DSTBN2# DSTBP2# DINV2#
D48# D49# D50# D51# D52# D53# D54# D55# D56# D57# D58# D59# D60# D61# D62# D63# DSTBN3# DSTBP3# DINV3#
GTLREF TEST1 TEST2 TEST3 TEST4 TEST5 TEST6 BSEL0 BSEL1 BSEL2
COMP0 COMP1 COMP2 COMP3 DPRSTP# DPSLP# DPWR# PWRGOOD SLP# PSI#
SKT-CPU478P-GP
62.10079.021
H_DSTBN#0 H_DSTBP#0 H_DIV#0
H_DSTBN#1 H_DSTBP#1 H_DIV#1
H_DSTBN#2 H_DSTBP#2 H_DIV#2
H_DSTBN#3 H_DSTBP#3 H_DIV#3
H_DPRSTP# H_DPSLP# H_DPWR# H_PWRGOOD H_CPUSLP# H_PSI#
CPU_MCH_BSEL0 CPU_MCH_BSEL1 CPU_MCH_BSEL2
27D4R2F-L1-GP 54D9R2F-L1-GP
R87 200R2F-L-GP
TP9 CPU_RSVD01
TP8 CPU_RSVD02
TP3 CPU_RSVD03
TP2 CPU_RSVD04
TP22 CPU_RSVD05
TP16 CPU_RSVD06
TP12 CPU_RSVD07
TP13 CPU_RSVD08
TP14 CPU_RSVD09
TP11 CPU_RSVD10
TP23 TP15 TP77 TP85 TP24 TP1
Use old Symbol replace New P/N
original value:SKT-CPU478P-GP
TEST3 and TEST5
For the purpose of testability, route thes signals through a ground referenced Zo=55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
R123 R115 R128 R73
H_DPSLP# H_DPRSTP# H_FERR# EC_CPU_PROCHOT#
56R2J-4-GP
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Title
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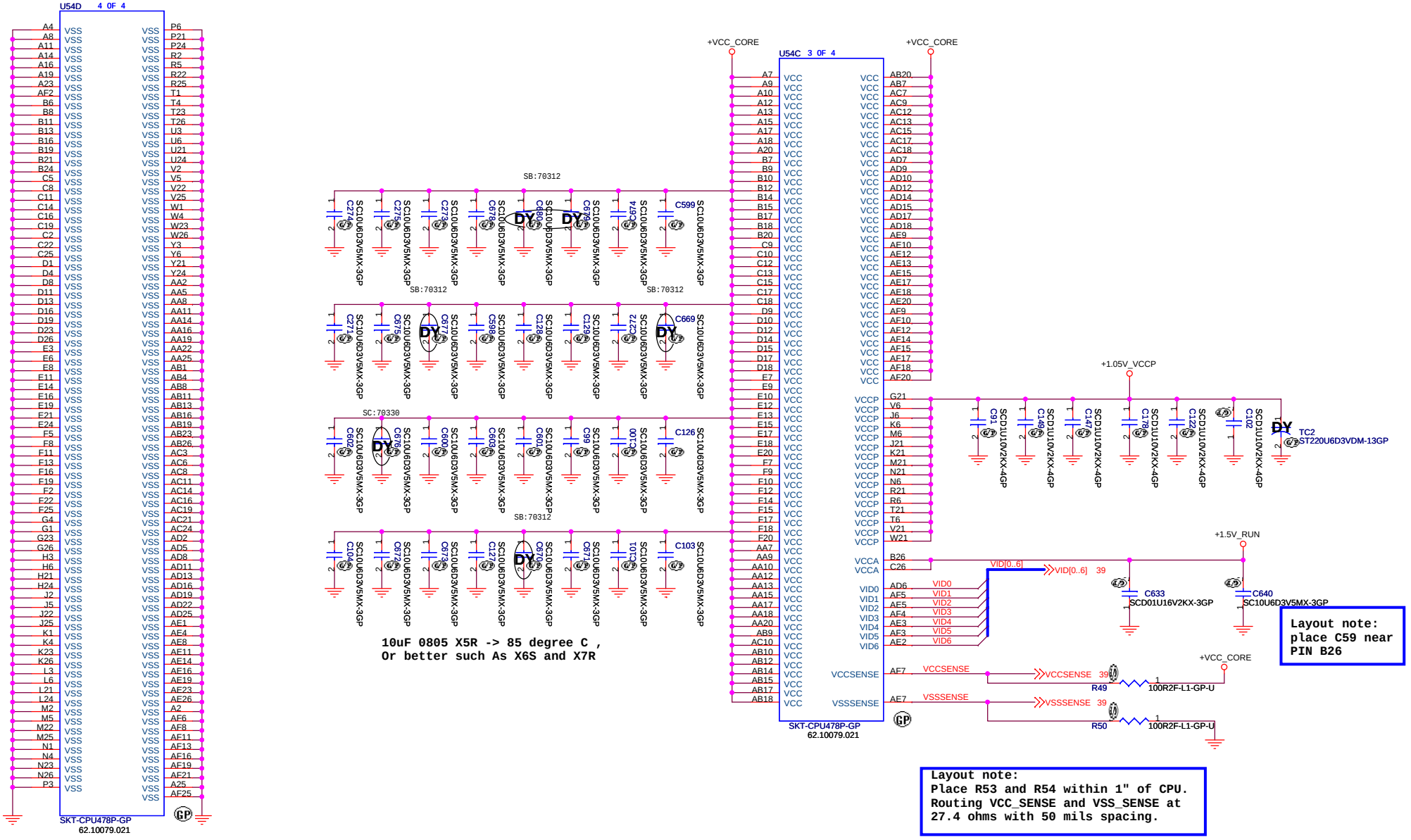
Size A3
Document Number CPU-FSB(1/2)
Rev -1
Date: Wednesday, November 07, 2007
Sheet 7 of 46



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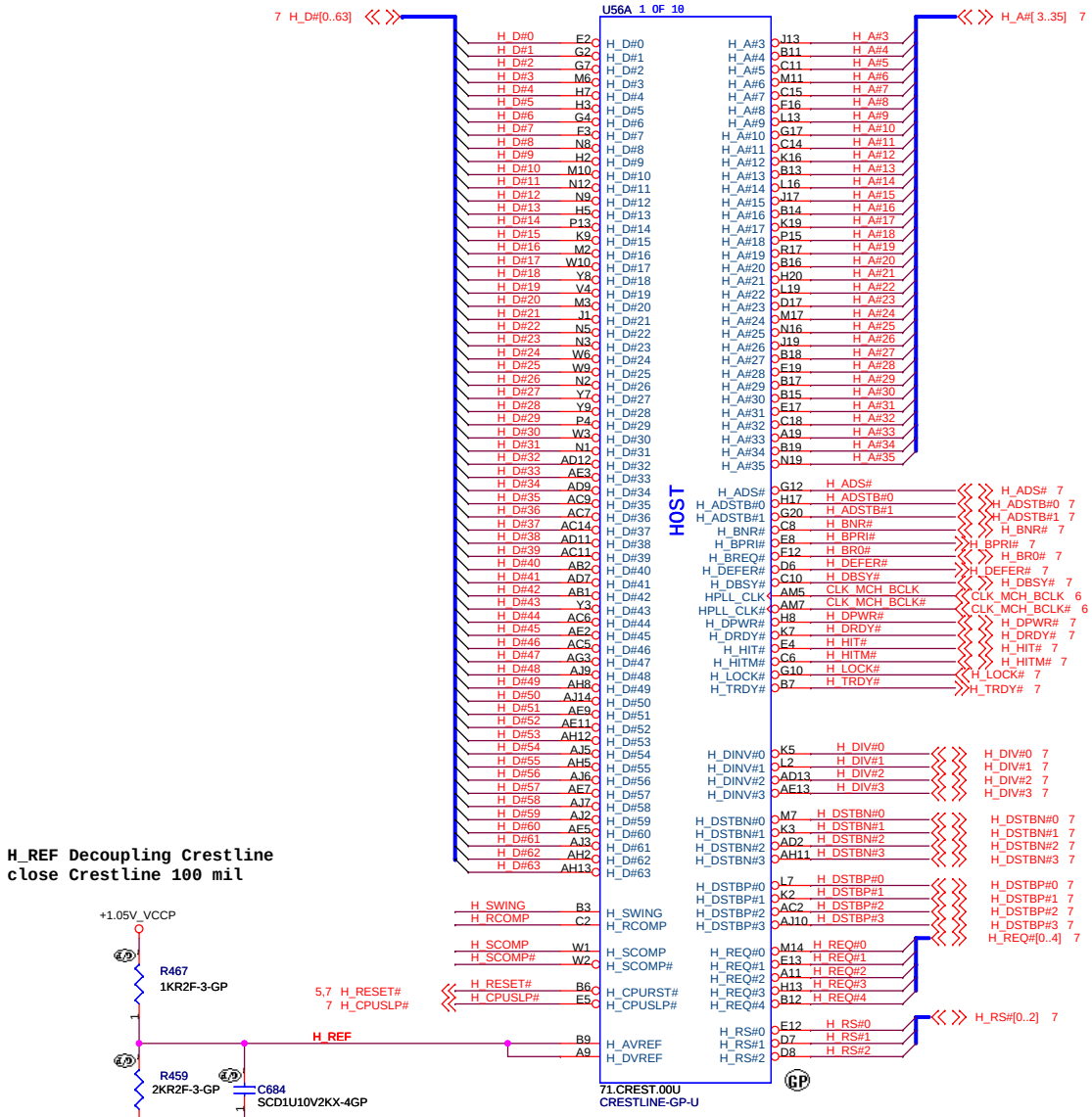
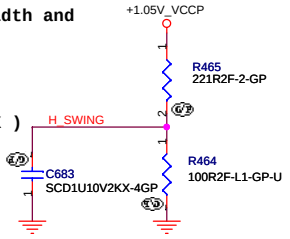
Date: Wednesday, November 07, 2007	Sheet 8 of 46	



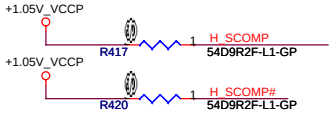
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close Caliistoga 500 mil (MAX)

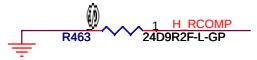
From Schematic Design Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors and Capacitors close Caliistoga 500 mil (MAX) Zo=55ohms



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



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Size	Document Number	Rev
A3	GMCH-FSB LIBC (1/6)	-1

Date: Wednesday, November 07, 2007 Sheet 9 of 46

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
	CFG[2..0] FSB Select
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

Layout Note:
MCH_CLVREF ~= 0.350V
Width/Spacing = 12/12

CLOSE PIN BL15 BK14

U56B 2 OF 10

RSVD
DDR MUXING
CLK
CFG
DMI
GRAPHICS VID
PM
ME
NC
MISC

CRESTLINE-GP-U 71.CREST.00U

<Variant Name>

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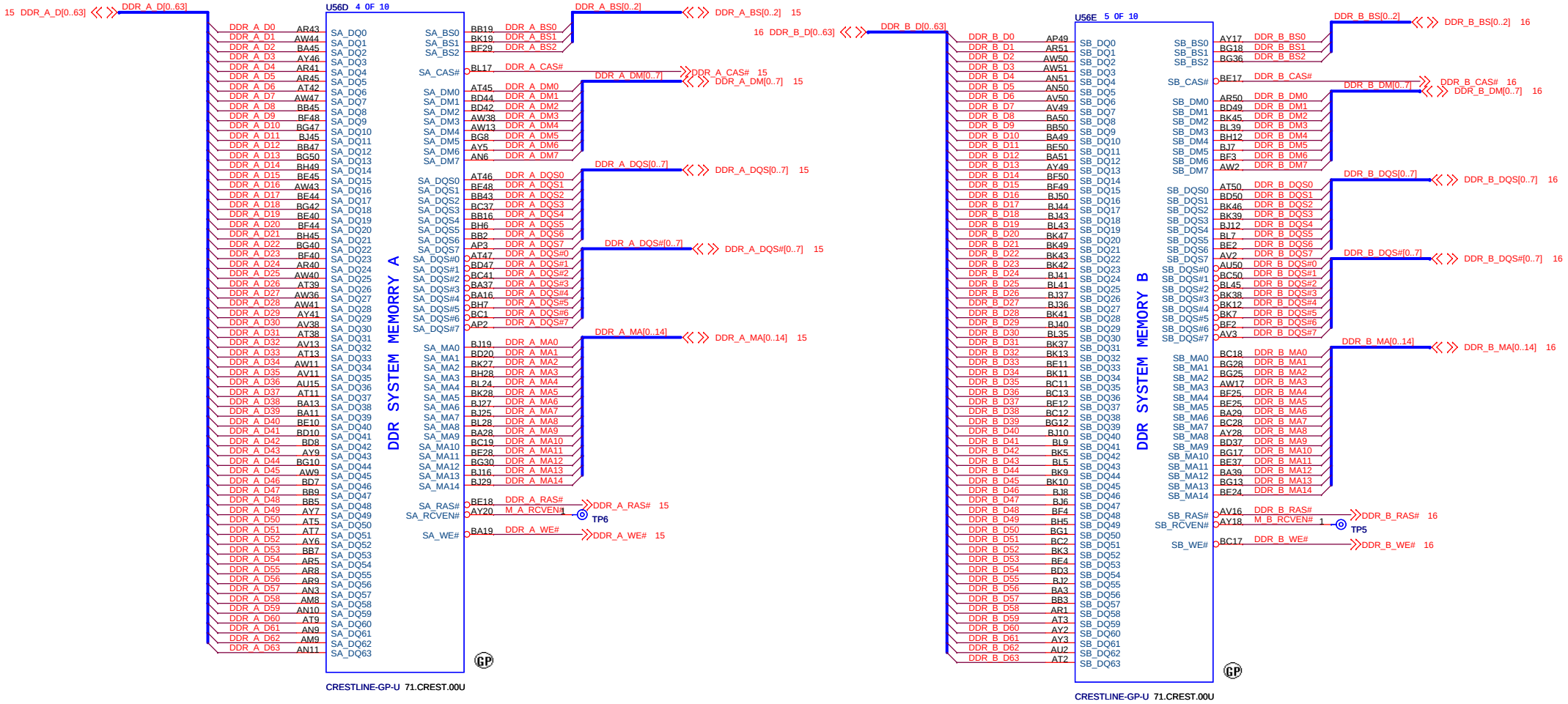
Date: Wednesday, November 07, 2007 | Sheet 10 of 46



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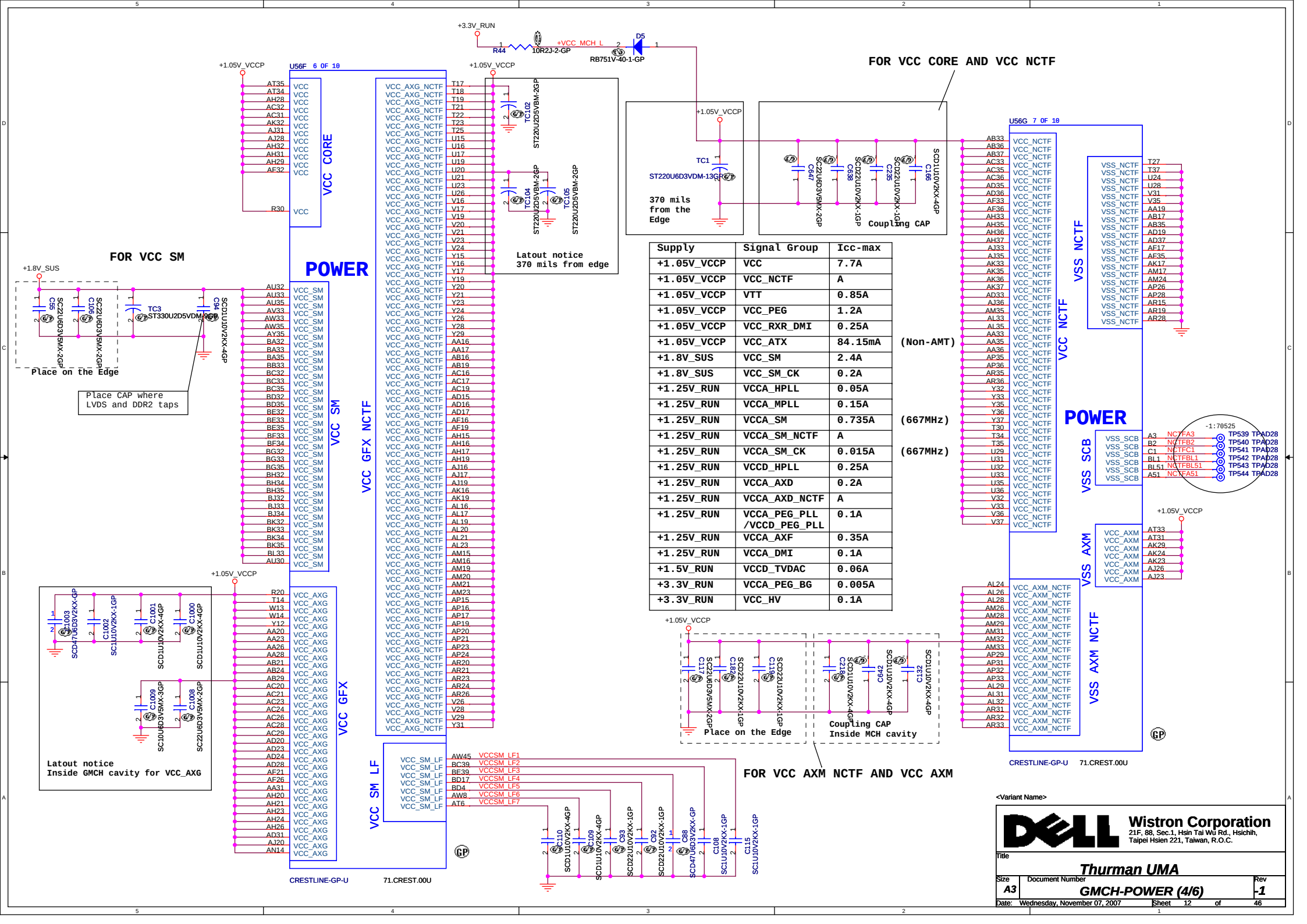
Title: ***Thurman UMA***

Size	Document Number	Rev
A3	GMCH-DDR (3/6)	-1

Date: Wednesday, November 07, 2007 Sheet 11 of 46



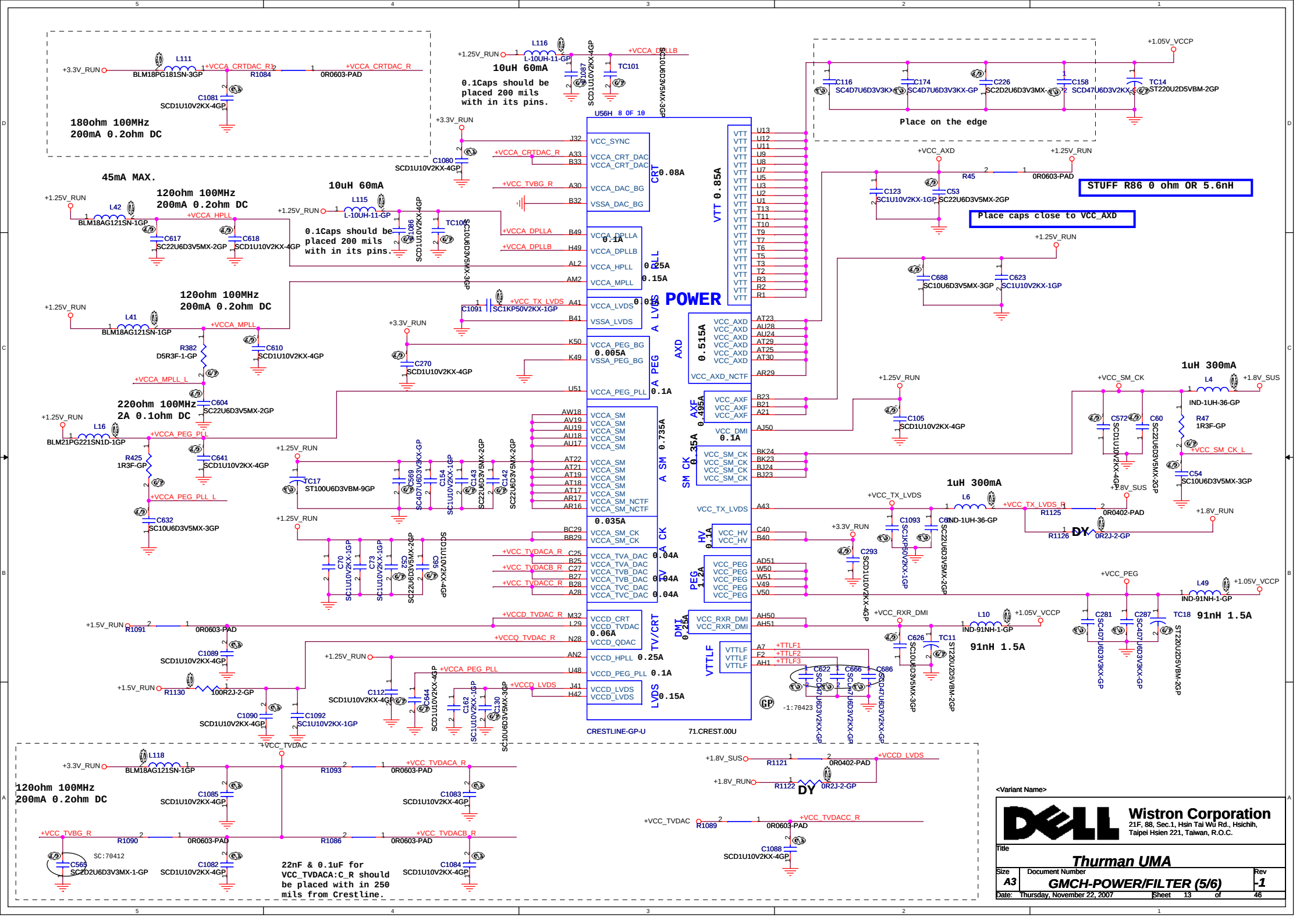
Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	7.7A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

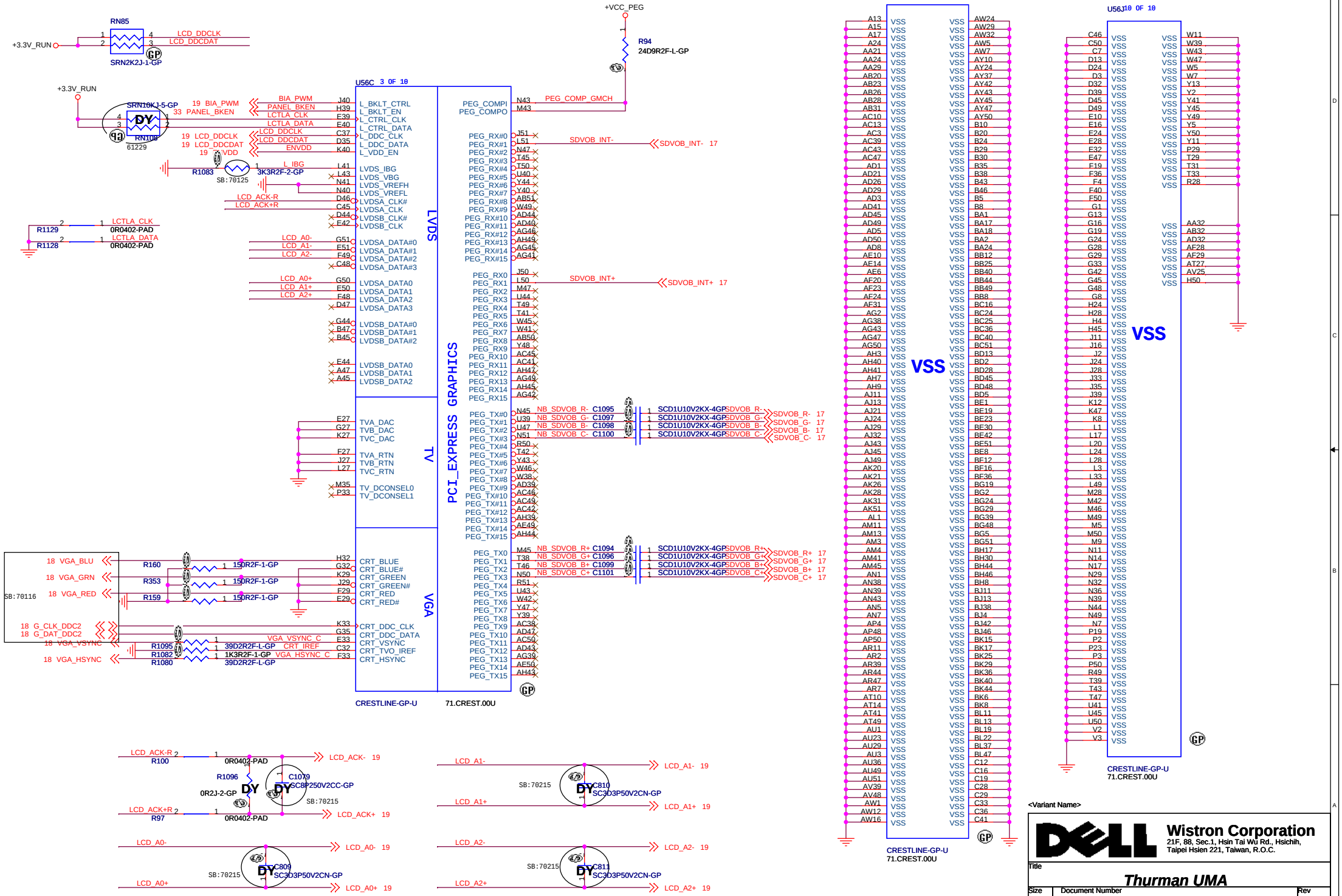
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

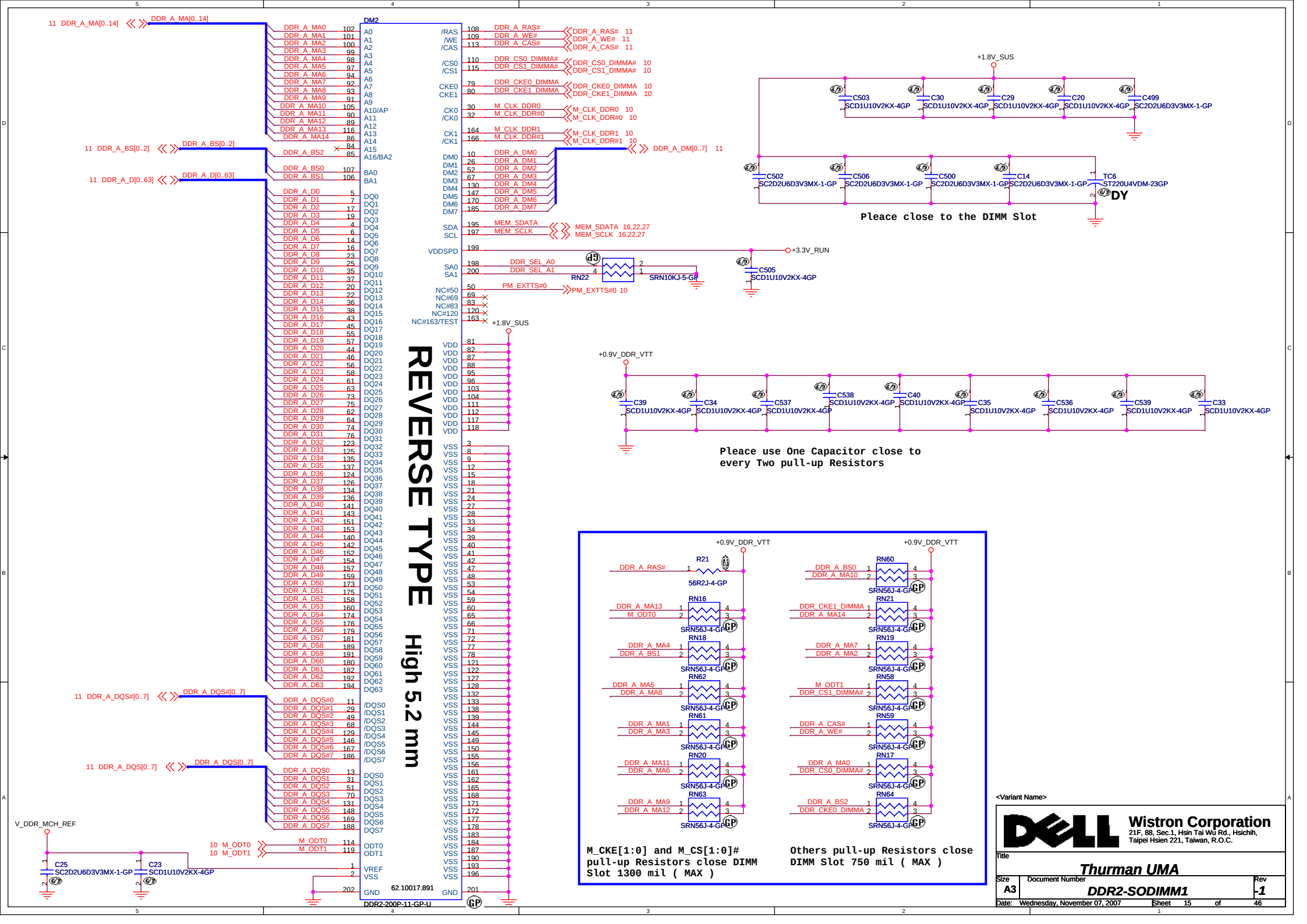
Title: Thurman UMA

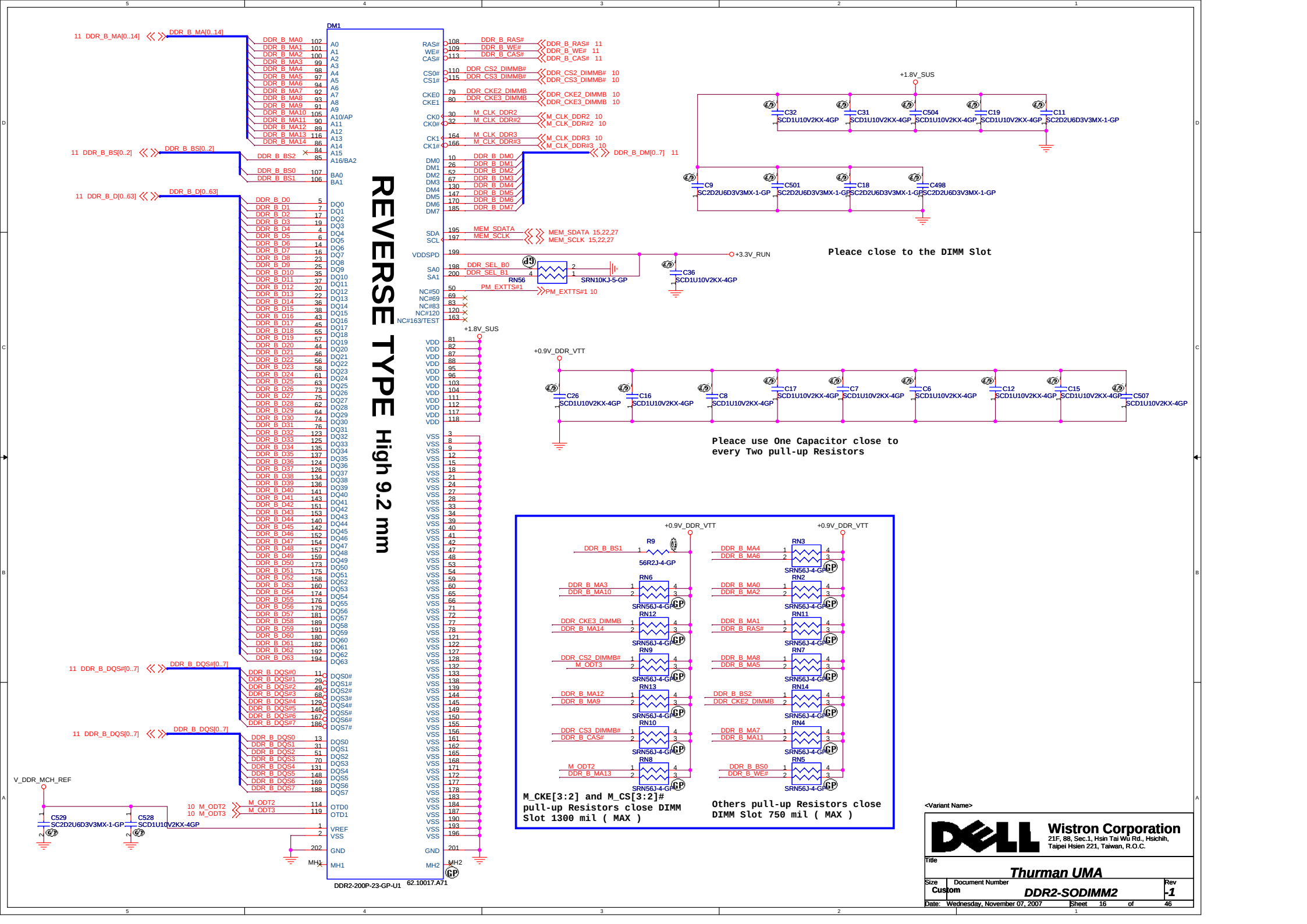
Size: A3 | Document Number: GMCH-POWER (4/6) | Rev: -1

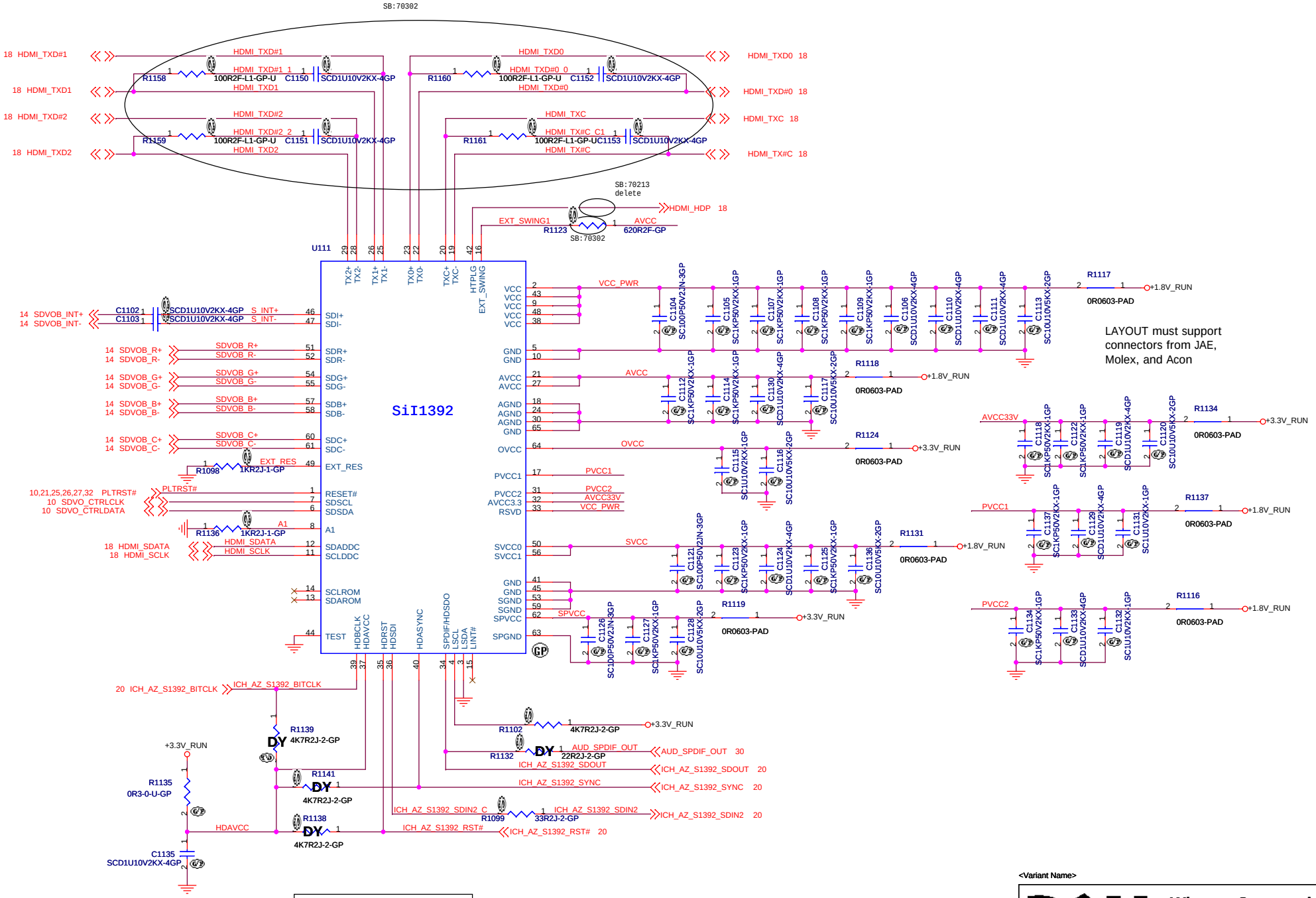
Date: Wednesday, November 07, 2007 | Sheet 12 of 46


180ohm 100MHz
200mA 0.2ohm DC
10uH 60mA
0.1Caps should be placed 200 mils with in its pins.
45mA MAX.
120ohm 100MHz
200mA 0.2ohm DC
220ohm 100MHz
2A 0.1ohm DC
U56H 8 OF 10
CRESTLINE-GP-U
71.CREST.00U
POWER
Place on the edge
STUFF R86 0 ohm OR 5.6nH
Place caps close to VCC_AXD
1uH 300mA
91nH 1.5A
DY
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Thurman UMA
GMCH-POWER/FILTER (5/6)
Size A3
Rev -1
Date: Thursday, November 22, 2007
Sheet 13 of 46


RN85
SRN2K2J-1-GP
+3.3V_RUN
LCD_DDCLK
LCD_DDCDAT
+VCC_PEG
R94
24D9R2F-L-GP
U56C 3 OF 10
CRESTLINE-GP-U
71.CREST.00U
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TVB_RTN
TVC_RTN
TV_DCONSEL0
TV_DCONSEL1
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_VSYNC
CRT_TVO_IREF
CRT_HSYNC
PEG_COMPI
PEG_COMPO
PEG_COMP_GMCH
SDVOB_INT-
SDVOB_INT+
SCD1U10V2KX-4GP
U56I 9 OF 10
U56J 10 OF 10
VSS
CRESTLINE-GP-U
71.CREST.00U
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size A3
Document Number
GMCH-GND/LVDA/VGA (6/6)
Rev -1
Date: Wednesday, November 07, 2007
Sheet 14 of 46

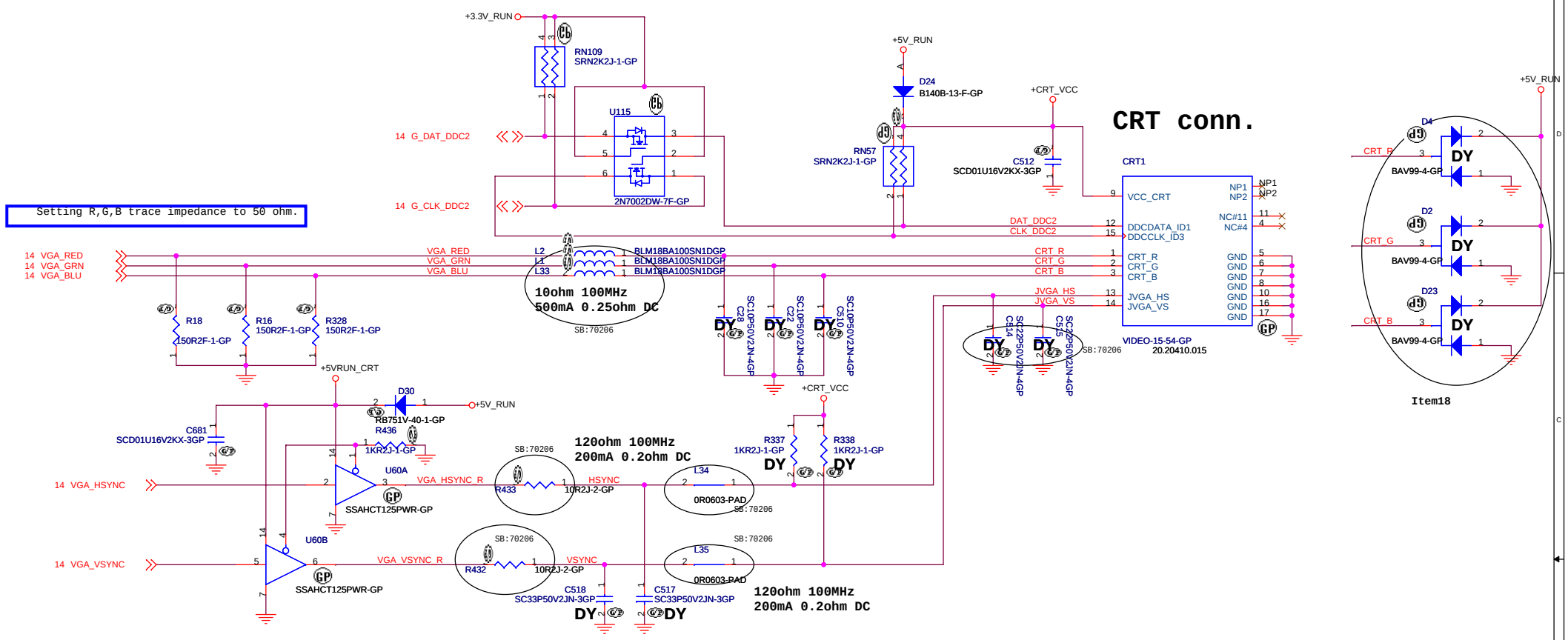

DM2
DDR2-200P-11-GP-U
62.10017.891
REVERSE TYPE
High 5.2 mm
11 DDR_A_MA[0..14]
DDR_A_MA[0..14]
11 DDR_A_BS[0..2]
DDR_A_BS[0..2]
11 DDR_A_D[0..63]
DDR_A_D[0..63]
11 DDR_A_DQS#[0..7]
DDR_A_DQS#[0..7]
11 DDR_A_DQS[0..7]
DDR_A_DQS[0..7]
V_DDR_MCH_REF
C25 SC2D2U6D3V3MX-1-GP
C23 SCD1U10V2KX-4GP
10 M_ODT0
10 M_ODT1
DDR_A_RAS# 11
DDR_A_WE# 11
DDR_A_CAS# 11
DDR_CS0_DIMMA# 10
DDR_CS1_DIMMA# 10
DDR_CKE0_DIMMA 10
DDR_CKE1_DIMMA 10
M_CLK_DDR0 10
M_CLK_DDR#0 10
M_CLK_DDR1 10
M_CLK_DDR#1 10
DDR_A_DM[0..7] 11
MEM_SDATA 16,22,27
MEM_SCLK 16,22,27
+3.3V_RUN
DDR_SEL_A0
DDR_SEL_A1
RN22 SRN10KJ-5-GP
C505 SCD1U10V2KX-4GP
PM_EXTTS#0
PM_EXTTS#0 10
+1.8V_SUS
+0.9V_DDR_VTT
C503 SCD1U10V2KX-4GP
C30 SCD1U10V2KX-4GP
C29 SCD1U10V2KX-4GP
C20 SCD1U10V2KX-4GP
C499 SC2D2U6D3V3MX-1-GP
C502 SC2D2U6D3V3MX-1-GP
C506 SC2D2U6D3V3MX-1-GP
C500 SC2D2U6D3V3MX-1-GP
C14 SC2D2U6D3V3MX-1-GP
TC6 ST220U4VDM-23GP
DY
Please close to the DIMM Slot
C39 SCD1U10V2KX-4GP
C34 SCD1U10V2KX-4GP
C537 SCD1U10V2KX-4GP
C538 SCD1U10V2KX-4GP
C40 SCD1U10V2KX-4GP
C35 SCD1U10V2KX-4GP
C536 SCD1U10V2KX-4GP
C539 SCD1U10V2KX-4GP
C33 SCD1U10V2KX-4GP
Please use One Capacitor close to
every Two pull-up Resistors
R21 56R2J-4-GP
RN16 SRN56J-4-GP
RN18 SRN56J-4-GP
RN62 SRN56J-4-GP
RN61 SRN56J-4-GP
RN20 SRN56J-4-GP
RN63 SRN56J-4-GP
RN60 SRN56J-4-GP
RN21 SRN56J-4-GP
RN19 SRN56J-4-GP
RN58 SRN56J-4-GP
RN59 SRN56J-4-GP
RN17 SRN56J-4-GP
RN64 SRN56J-4-GP
M_CKE[1:0] and M_CS[1:0]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)
Others pull-up Resistors close
DIMM Slot 750 mil (MAX)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size A3
Document Number DDR2-SODIMM1
Rev -1
Date: Wednesday, November 07, 2007
Sheet 15 of 46


REVERSE TYPE High 9.2 mm
DM1
DDR2-200P-23-GP-U1
62.10017.A71
11 DDR_B_MA[0..14]
DDR_B_MA[0..14]
11 DDR_B_BS[0..2]
DDR_B_BS[0..2]
11 DDR_B_D[0..63]
DDR_B_D[0..63]
11 DDR_B_DQS#[0..7]
DDR_B_DQS#[0..7]
11 DDR_B_DQS[0..7]
DDR_B_DQS[0..7]
DDR_B_DM[0..7] 11
V_DDR_MCH_REF
C529 SC2D2U6D3V3MX-1-GP
C528 SCD1U10V2KX-4GP
10 M_ODT2
10 M_ODT3
+1.8V_SUS
+0.9V_DDR_VTT
+3.3V_RUN
RN56 SRN10KJ-5-GP
C36 SCD1U10V2KX-4GP
C32 SCD1U10V2KX-4GP
C31 SCD1U10V2KX-4GP
C504 SCD1U10V2KX-4GP
C19 SCD1U10V2KX-4GP
C11 SC2D2U6D3V3MX-1-GP
C9 SC2D2U6D3V3MX-1-GP
C501 SC2D2U6D3V3MX-1-GP
C18 SC2D2U6D3V3MX-1-GP
C498 SC2D2U6D3V3MX-1-GP
Please close to the DIMM Slot
C26 SCD1U10V2KX-4GP
C16 SCD1U10V2KX-4GP
C8 SCD1U10V2KX-4GP
C17 SCD1U10V2KX-4GP
C7 SCD1U10V2KX-4GP
C6 SCD1U10V2KX-4GP
C12 SCD1U10V2KX-4GP
C15 SCD1U10V2KX-4GP
C507 SCD1U10V2KX-4GP
Please use One Capacitor close to every Two pull-up Resistors
R9 56R2J-4-GP
RN6 SRN56J-4-GP
RN12 SRN56J-4-GP
RN9 SRN56J-4-GP
RN13 SRN56J-4-GP
RN10 SRN56J-4-GP
RN8 SRN56J-4-GP
RN3 SRN56J-4-GP
RN2 SRN56J-4-GP
RN11 SRN56J-4-GP
RN7 SRN56J-4-GP
RN14 SRN56J-4-GP
RN4 SRN56J-4-GP
RN5 SRN56J-4-GP
M_CKE[3:2] and M_CS[3:2]# pull-up Resistors close DIMM Slot 1300 mil (MAX)
Others pull-up Resistors close DIMM Slot 750 mil (MAX)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size Custom
Document Number DDR2-SODIMM2
Rev -1
Date: Wednesday, November 07, 2007
Sheet 16 of 46

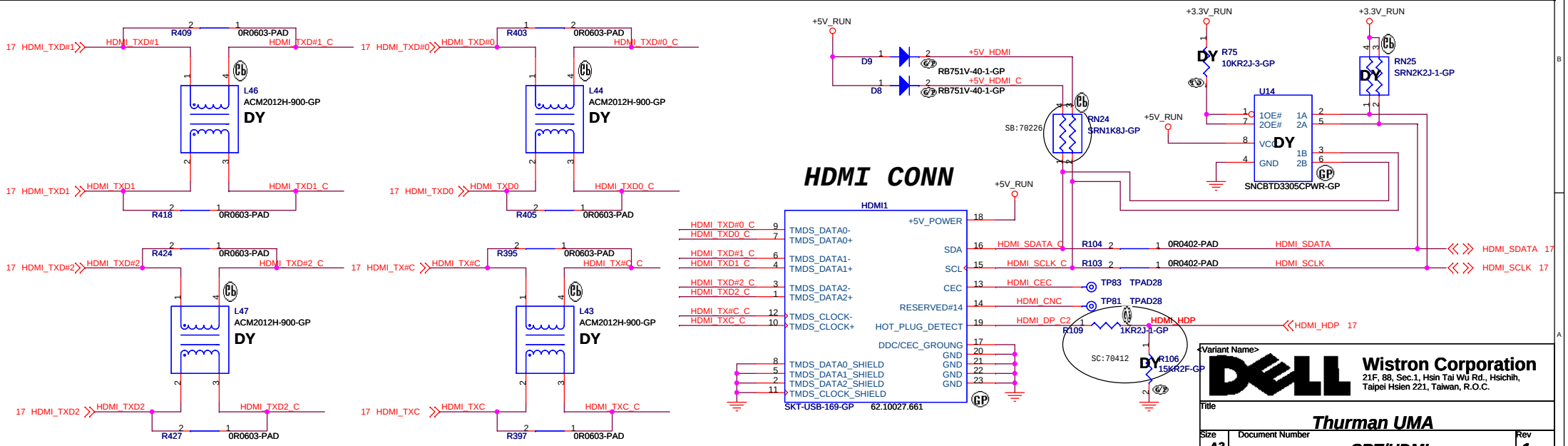

SB:70302
HDMI_TXD#1
HDMI_TXD1
HDMI_TXD#2
HDMI_TXD2
HDMI_TXD0
HDMI_TXD#0
HDMI_TXC
HDMI_TX#C
R1158
R1159
R1160
R1161
100R2F-L1-GP-U
100R2F-L1-GP-UC1153
C1150
C1151
C1152
SCD1U10V2KX-4GP
SB:70213
delete
HDMI_HDP
EXT_SWING1
R1123
620R2F-GP
U111
SiI1392
TX2+
TX2-
TX1+
TX1-
TX0+
TX0-
TXC+
TXC-
HTPLG
EXT_SWING
SDI+
SDI-
SDR+
SDR-
SDG+
SDG-
SDB+
SDB-
SDC+
SDC-
EXT_RES
RESET#
SDSCL
SDSDA
A1
SDADDC
SCLDDC
SCLROM
SDAROM
TEST
HDBCLK
HDAVCC
HDRST
HDSDI
HDASYNC
SPDIF/HDSDO
LSCL
LSDA
LINT#
VCC
GND
AVCC
AGND
OVCC
PVCC1
PVCC2
AVCC33
VCC_PWR
RSVD
SVCC0
SVCC1
SGND
SPVCC
SPGND
SDVOB_INT+
SDVOB_INT-
SDVOB_R+
SDVOB_R-
SDVOB_G+
SDVOB_G-
SDVOB_B+
SDVOB_B-
SDVOB_C+
SDVOB_C-
PLTRST#
SDVO_CTRLCLK
SDVO_CTRLDATA
HDMI_SDATA
HDMI_SCLK
ICH_AZ_S1392_BITCLK
ICH_AZ_S1392_SDOUT
ICH_AZ_S1392_SYNC
ICH_AZ_S1392_SDIN2
ICH_AZ_S1392_RST#
AUD_SPDIF_OUT
HDAVCC
+3.3V_RUN
+1.8V_RUN
R1098
R1102
R1117
R1118
R1119
R1124
R1131
R1134
R1136
R1137
R1138
R1139
R1141
R1099
R1132
R1135
R1116
C1135
1KR2J-1-GP
4K7R2J-2-GP
33R2J-2-GP
22R2J-2-GP
0R3-0-U-GP
0R0603-PAD
LAYOUT must support connectors from JAE, Molex, and Acon
SPDIF: Stuff
R1123,R1113,R1115,R1117
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size
A3
Document Number
Sil 1932
Rev
-1
Date: Wednesday, November 07, 2007
Sheet 17 of 46

CRT conn.

Setting R,G,B trace impedance to 50 ohm.



HDMI CONN



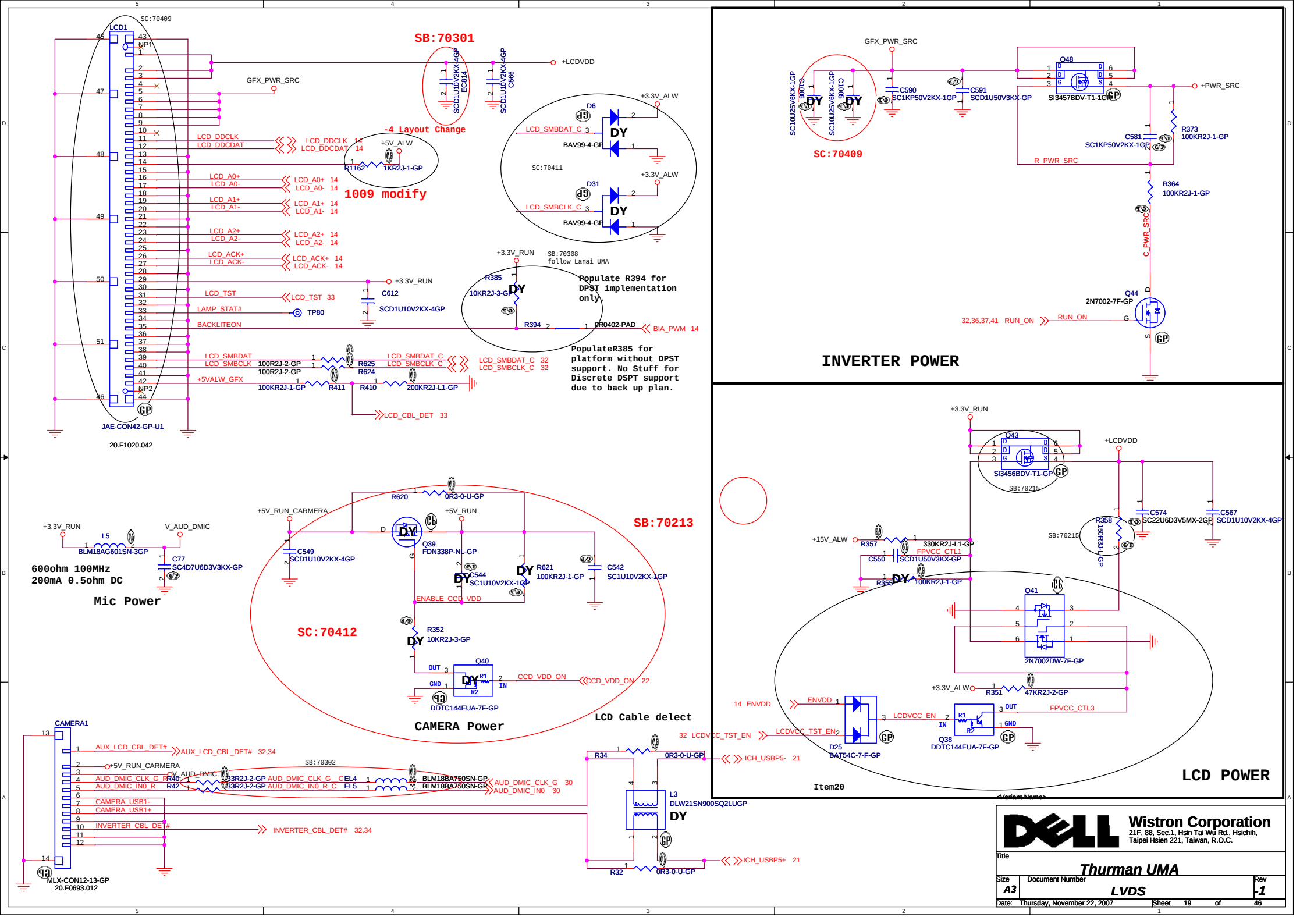
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: Thurman UMA

Size	Document Number	Rev
A3	CRT/HDMI	-1

Date: Wednesday, November 07, 2007 Sheet 18 of 46

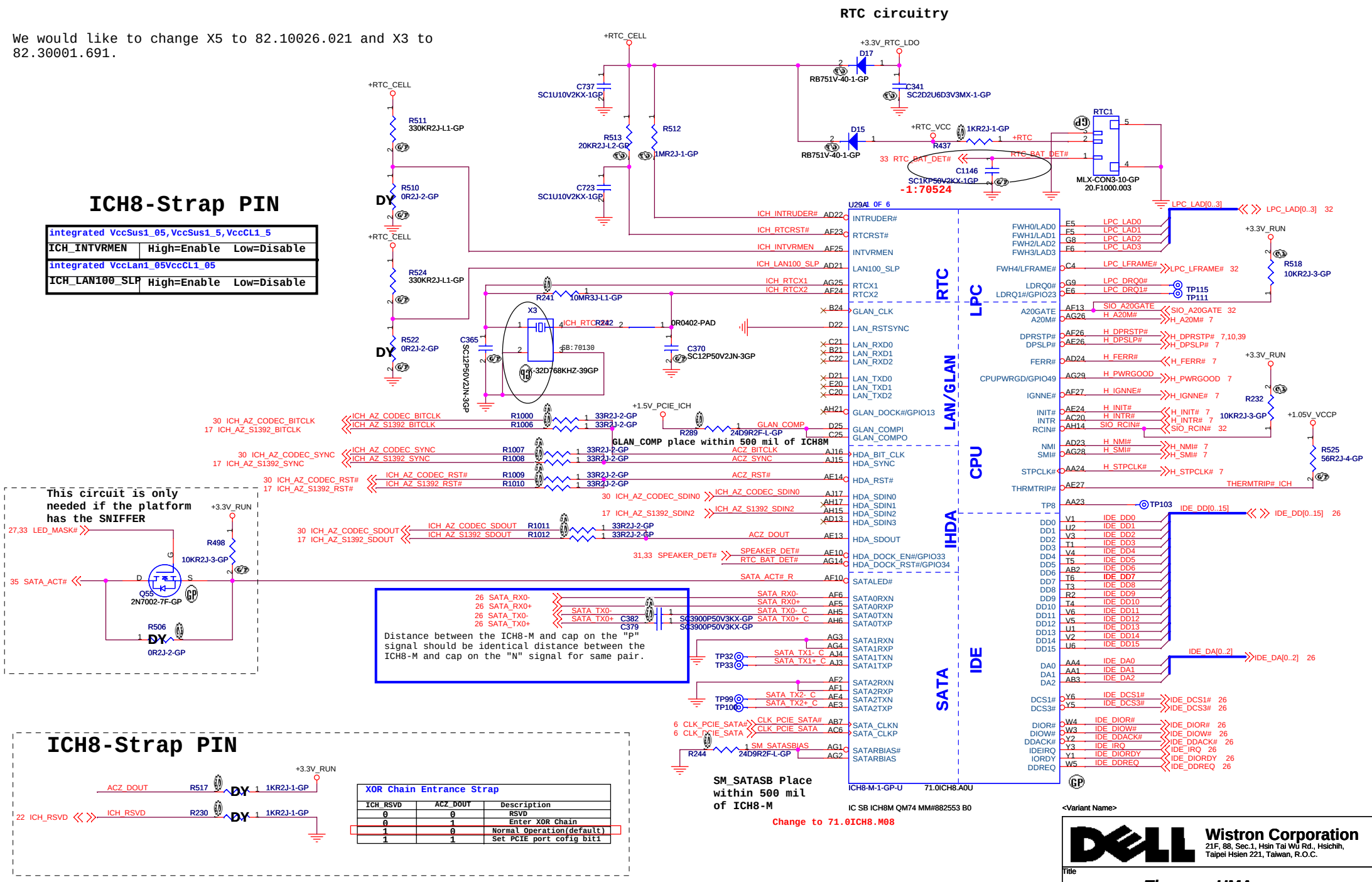

SB:70301
SC:70409
LCD1
JAE-CON42-GP-U1
20.F1020.042
GFX_PWR_SRC
+LCDVDD
SCD1U10V2KX-4GP
EC614
C566
-4 Layout Change
1009 modify
LCD_DDCLK
LCD_DDCDAT
+5V_ALW
R1162
1KR2J-1-GP
LCD_A0+
LCD_A0-
LCD_A1+
LCD_A1-
LCD_A2+
LCD_A2-
LCD_ACK+
LCD_ACK-
LCD_TST
LAMP_STAT#
TP80
BACKLITEON
+3.3V_RUN
C612
SCD1U10V2KX-4GP
+3.3V_ALW
D6
BAV99-4-GP
LCD_SMBDAT_C
D31
LCD_SMBCLK_C
SC:70411
SB:70308
follow Lanai UMA
R385
10KR2J-3-GP
R394
0R0402-PAD
BIA_PWM
Populate R394 for DPST implementation only.
PopulateR385 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.
LCD_SMBDAT
LCD_SMBCLK
100R2J-2-GP
R625
R624
R411
R410
200KR2J-L1-GP
+5VALW_GFX
LCD_CBL_DET
SC:70409
C590
SC1KP50V2KX-1GP
C591
SCD1U50V3KX-GP
Q48
SI3457BDV-T1-1GP
+PWR_SRC
C581
SC1KP50V2KX-1GP
R373
100KR2J-1-GP
R_PWR_SRC
R364
100KR2J-1-GP
C_PWR_SRC
Q44
2N7002-7F-GP
RUN_ON
INVERTER POWER
Q43
SI3456BDV-T1-GP
SB:70215
C574
SC22U6D3V5MX-2GP
C567
SCD1U10V2KX-4GP
R358
150R3-L-GP
+15V_ALW
R357
330KR2J-L1-GP
FPVCC_CTL1
C550
SCD1U50V3KX-GP
R355
100KR2J-1-GP
Q41
2N7002DW-7F-GP
+3.3V_ALW
R351
47KR2J-2-GP
FPVCC_CTL3
ENVDD
LCDVCC_EN
LCDVCC_TST_EN
D25
BAT54C-7-F-GP
Q38
DDTC144EUA-7F-GP
LCD POWER
Item20
SB:70213
SC:70412
+5V_RUN_CARMERA
+5V_RUN
R620
0R3-0-U-GP
C549
SCD1U10V2KX-4GP
Q39
FDN338P-NL-GP
C544
SC1U10V2KX-1GP
R621
100KR2J-1-GP
C542
SC1U10V2KX-1GP
ENABLE_CCD_VDD
R352
10KR2J-3-GP
Q40
DDTC144EUA-7F-GP
CCD_VDD_ON
CAMERA Power
L5
BLM18AG601SN-3GP
V_AUD_DMIC
C77
SC4D7U6D3V3KX-GP
600ohm 100MHz
200mA 0.5ohm DC
Mic Power
LCD Cable delect
CAMERA1
MLX-CON12-13-GP
20.F0693.012
AUX_LCD_CBL_DET#
AUX_LCD_CBL_DET# 32,34
SB:70302
AUD_DMIC_CLK_G
AUD_DMIC_IN0_R
33R2J-2-GP
BLM18BA750SN-GP
AUD_DMIC_CLK_G 30
AUD_DMIC_IN0 30
CAMERA_USB1-
CAMERA_USB1+
INVERTER_CBL_DET#
INVERTER_CBL_DET# 32,34
R34
0R3-0-U-GP
ICH_USBP5-
L3
DLW21SN900SQ2LUGP
ICH_USBP5+
R32
0R3-0-U-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size
A3
Document Number
LVDS
Rev
-1
Date: Thursday, November 22, 2007
Sheet 19 of 46

We would like to change X5 to 82.10026.021 and X3 to 82.30001.691.

RTC circuitry

ICH8-Strap PIN

integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable



ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

PCI_GNT#0 R582 1KR2J-1-GP
ICH_SPI_CS1# R R292 DY 1KR2J-1-GP
PCI_GNT#3 R581 DY 1KR2J-1-GP

PCI I/F PULL HIGH

RP4 SRN8K2J-2-GP-U
PCI_SERR# PCI_TRDY# PCI_IRDY# PCI_PLOCK# +3.3V_RUN
PCI_STOP# PCI_DEVSEL# PCI_FRAME# PCI_REQ#1 +3.3V_RUN

RP5 SRN8K2J-2-GP-U
22 USB_IDE# +3.3V_RUN
PCI_PIRQB# PCI_REQ#0 PCI_PIRQC# USB_IDE#
SB_WPAN_PCIE_RST# PCI_PIRQA# PCI_PIRQD# PCI_PERR# +3.3V_RUN

BIOS should not enable the internal GPIO pull up

+3.3V_RUN RN52 SRN10KJ-5-GP
SB_WLAN_PCIE_RST# SB_NB_PCIE_RST#

R295 20KR3J-1-GP SB_WWAN_PCIE_RST#
RN53 SRN100KJ-6-GP
SB_NB_PCIE_RST# SB_WLAN_PCIE_RST#
R296 20KR3J-1-GP SB_LOM_PCIE_RST#

R611 15R2J-GP ICH_SPI_CS0# +3.3V_ALW
U80 74LVC1G08GW-1-GP
R612 DY 15R2J-GP 33 SPI_CS0# SPI_CS0# R
R597 SIO_SPI_CS# 32
R291 15R2J-GP 32 ICH_EC_SPI_CLK ICH_EC_SPI_CLK_R
R290 15R2J-GP 32 ICH_EC_SPI_DO 32 ICH_EC_SPI_DIN
ICH_EC_SPI_CS# ICH_EC_SPI_DO_R ICH_EC_SPI_DIN

PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN

RN67 SRN10KJ-5-GP +3.3V_SUS
USB_OC5# USB_OC4#

RP1 SRN10KJ-L3-GP +3.3V_SUS
USB_OC6# USB_OC9# USB_OC7# USB_OC0#
USB_OC1# USB_OC2# USB_OC3# USB_OC8#

Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

PCI Interface Routing

Add Buffers as need for Loading and Fanout concerns

28 PCI_AD[0..31] PCI_AD[0..31]

U29C 3 0F 6

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 GNT3#/GPIO55 REQ3#/GPIO54
PCI_REQ#0 PCI_GNT#0 PCI_REQ#1 PCI_GNT#1 SB_WWAN_PCIE_RST# PCI_GNT#2 PCI_GNT#3 SB_LOM_PCIE_RST#
PCI_REQ#1 28 PCI_GNT#1 28 SB_WWAN_PCIE_RST# 27 TP114 SB_LOM_PCIE_RST# 25

C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C_BE#0 PCI_C_BE#1 PCI_C_BE#2 PCI_C_BE#3
PCI_C_BE#[0..3] PCI_C_BE#[0..3] 28

IRDY# PAR PCIRST# DEVSEL# PERR# FRAME# PLOCK# SERR# STOP# TRDY#
PCI_IRDY# PCI_PAR PCI_RST# G PCI_DEVSEL# PCI_PERR# PCI_FRAME# PCI_PLOCK# PCI_SERR# PCI_STOP# PCI_TRDY#
PCI_IRDY# 28 PCI_PAR 28 PCI_DEVSEL# 28 PCI_PERR# 28 PCI_FRAME# 28 TP124 PCI_SERR# 28 PCI_STOP# 28 PCI_TRDY# 28

PLTRST# PCICLK PME#
PCI_PLTRST# CLK_PCI_ICH ICH_PME#
CLK_PCI_ICH 6 ICH_PME# 33

R281 33R2J-GP PCI_RST# 28

+3.3V_SUS 16mA
U28 SNLVC1G08DCKRG4-GP
C404 SCD1U10V2KX-4GP
R260 33R2J-GP PLT_RST# S PLTRST# 10,17,25,26,27,32
R261 DY 0R2J-GP

Interrupt I/F

SB:70302
PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
SB_WPAN_PCIE_RST# SB_WLAN_PCIE_RST# SB_NB_PCIE_RST# PCIE_MCARD2_DET#
SB_WPAN_PCIE_RST# 27 SB_WLAN_PCIE_RST# 27 SB_NB_PCIE_RST# 10 PCIE_MCARD2_DET# 27
28 PCI_PIRQC# 28 PCI_PIRQD#

ICH8-M-1-GP-U 71.0ICH8.A0U
IC SB ICH8M QM74 MM#882553 B0

CLK_ICH_14M EMI Mode Place close to ICH8-M

CLK_PCI_ICH R294 10R2J-2-GP DY CLK_ICHPCI C462 SC8P250V2CC-GP DY
EMI

U29B 2 OF 6

MiniCard WWAN

PCIE_RX1- PCIE_RX1+ PCIE_TX1- PCIE_TX1+ C409 C407 SCD1U10V2KX-4GP PCIE_TXN1_C PCIE_TXP1_C
27 PCIE_RX1- 27 PCIE_RX1+ 27 PCIE_TX1- 27 PCIE_TX1+
PERN1 PERP1 PETN1 PETP1 P27 P26 N29 N28

MiniCard WLAN

PCIE_RX2- PCIE_RX2+ PCIE_TX2- PCIE_TX2+ C416 C414 SCD1U10V2KX-4GP PCIE_TXN2_C PCIE_TXP2_C
27 PCIE_RX2- 27 PCIE_RX2+ 27 PCIE_TX2- 27 PCIE_TX2+
PERN2 PERP2 PETN2 PETP2 M27 M26 L29 L28

Express Card

PCIE_RX4- PCIE_RX4+ PCIE_TX4- PCIE_TX4+ C429 C425 SCD1U10V2KX-4GP PCIE_TXN3_C PCIE_TXP3_C
26 PCIE_RX4- 26 PCIE_RX4+ 26 PCIE_TX4- 26 PCIE_TX4+
PERN4 PERP4 PETN4 PETP4 H27 H26 G29 G28
PERN3 PERP3 PETN3 PETP3 K27 K26 J29 J28
PERN5 PERP5 PETN5 PETP5 F27 F26 E29 E28

LAN

PCIE_RX6- PCIE_RX6+ PCIE_TX6- PCIE_TX6+ C433 C432 SCD1U10V2KX-4GP PCIE_TXN4_C PCIE_TXP4_C
25 PCIE_RX6- 25 PCIE_RX6+ 25 PCIE_TX6- 25 PCIE_TX6+
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP D27 D26 C29 C28

SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO B23 E22 D23 F21

USB_OC0# USB_OC1# USB_OC2# USB_OC3# USB_OC4# USB_OC5# USB_OC6# USB_OC7# USB_OC8# USB_OC9#
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#
38 USB_OC0# 38 USB_OC1# AJ19 AG16 AG15 AE15 AF15 AG17 AD12 AJ18 AD14 AH18

PCI-Express

DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI_MTX_IRX_N0 DMI_MTX_IRX_P0 DMI_MRX_ITX_N0 DMI_MRX_ITX_P0
DMI_MTX_IRX_N0 10 DMI_MTX_IRX_P0 10 DMI_MRX_ITX_N0 10 DMI_MRX_ITX_P0 10
V27 V26 U29 U28

DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI_MTX_IRX_N1 DMI_MTX_IRX_P1 DMI_MRX_ITX_N1 DMI_MRX_ITX_P1
DMI_MTX_IRX_N1 10 DMI_MTX_IRX_P1 10 DMI_MRX_ITX_N1 10 DMI_MRX_ITX_P1 10
Y27 Y26 W29 W28

DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI_MTX_IRX_N2 DMI_MTX_IRX_P2 DMI_MRX_ITX_N2 DMI_MRX_ITX_P2
DMI_MTX_IRX_N2 10 DMI_MTX_IRX_P2 10 DMI_MRX_ITX_N2 10 DMI_MRX_ITX_P2 10
AB26 AB25 AA29 AA28

DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_MTX_IRX_N3 DMI_MTX_IRX_P3 DMI_MRX_ITX_N3 DMI_MRX_ITX_P3
DMI_MTX_IRX_N3 10 DMI_MTX_IRX_P3 10 DMI_MRX_ITX_N3 10 DMI_MRX_ITX_P3 10
AD27 AD26 AC29 AC28

DMI_CLKN DMI_CLKP
CLK_PCIE_ICH# CLK_PCIE_ICH
CLK_PCIE_ICH# 6 CLK_PCIE_ICH 6
T26 T25

DMI_ZCOMP DMI_IRCOMP
DMI_COMP R246 24D9R2F-L-GP
Y23 Y24
+1.5V_PCIE_ICH

Direct Media Interface

SPI

USB

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P
ICH_USBP0- ICH_USBP0+ ICH_USBP1- ICH_USBP1+ ICH_USBP4- ICH_USBP4+ ICH_USBP5- ICH_USBP5+ ICH_USBP6- ICH_USBP6+ ICH_USBP7- ICH_USBP7+ ICH_USBP9- ICH_USBP9+
ICH_USBP0- 38 ICH_USBP0+ 38 ICH_USBP1- 38 ICH_USBP1+ 38
ICH_USBP4- 34 ICH_USBP4+ 34 ICH_USBP5- 19 ICH_USBP5+ 19 ICH_USBP6- 26 ICH_USBP6+ 26 ICH_USBP7- 29 ICH_USBP7+ 29
ICH_USBP9- 27 ICH_USBP9+ 27
G3 G2 H5 H4 H2 H1 J3 J2 K5 K4 K2 K1 L3 L2 M5 M4 M2 M1 N3 N2

USBRBIAS USBRBIAS
USBRBIAS R272 22D6R2F-L1-GP
F2 F3

ICH8-M-1-GP-U 71.0ICH8.A0U
IC SB ICH8M QM74 MM#882553 B0

USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%

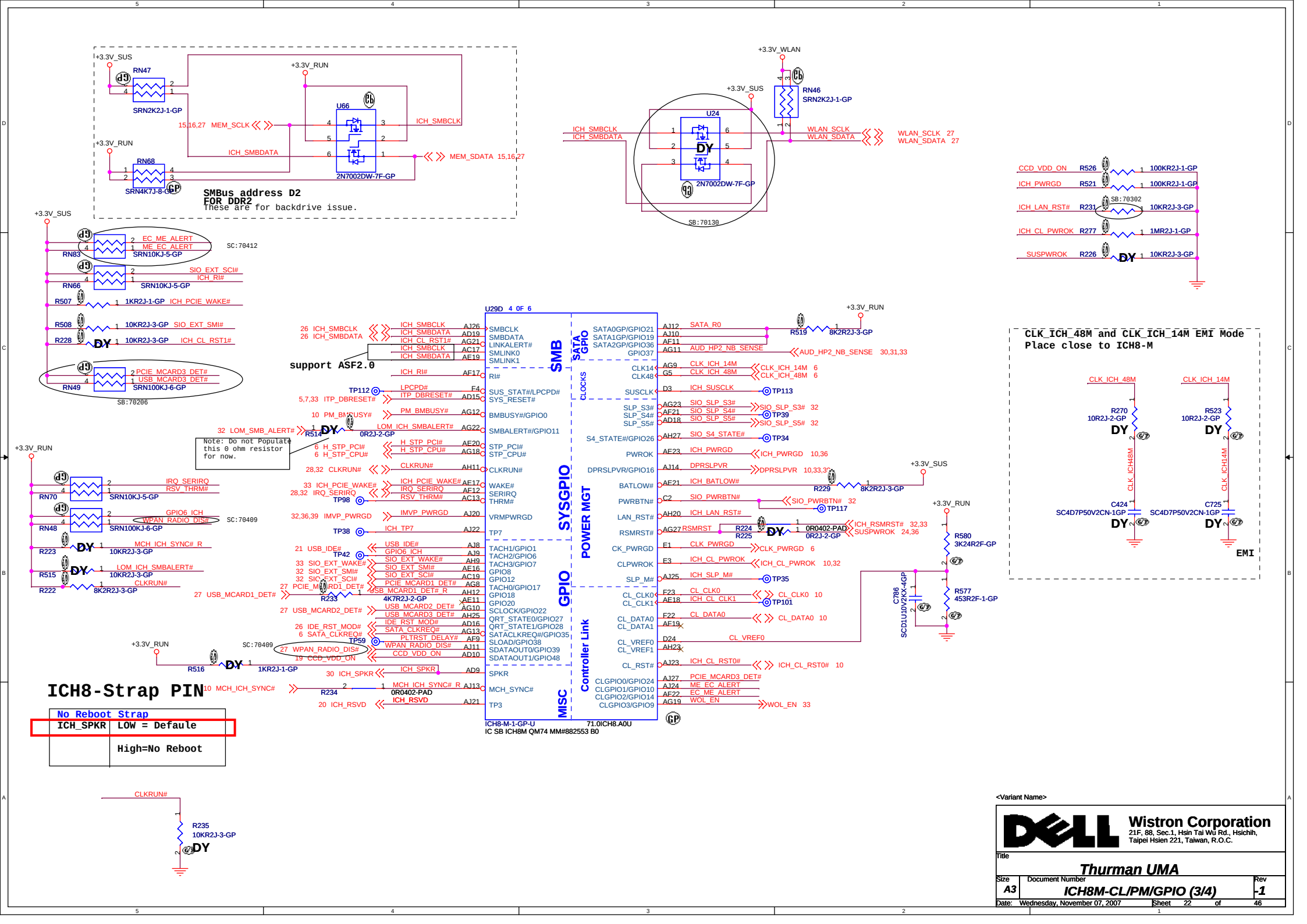
DMI_COMP R158 place within 500 mil of ICH8M

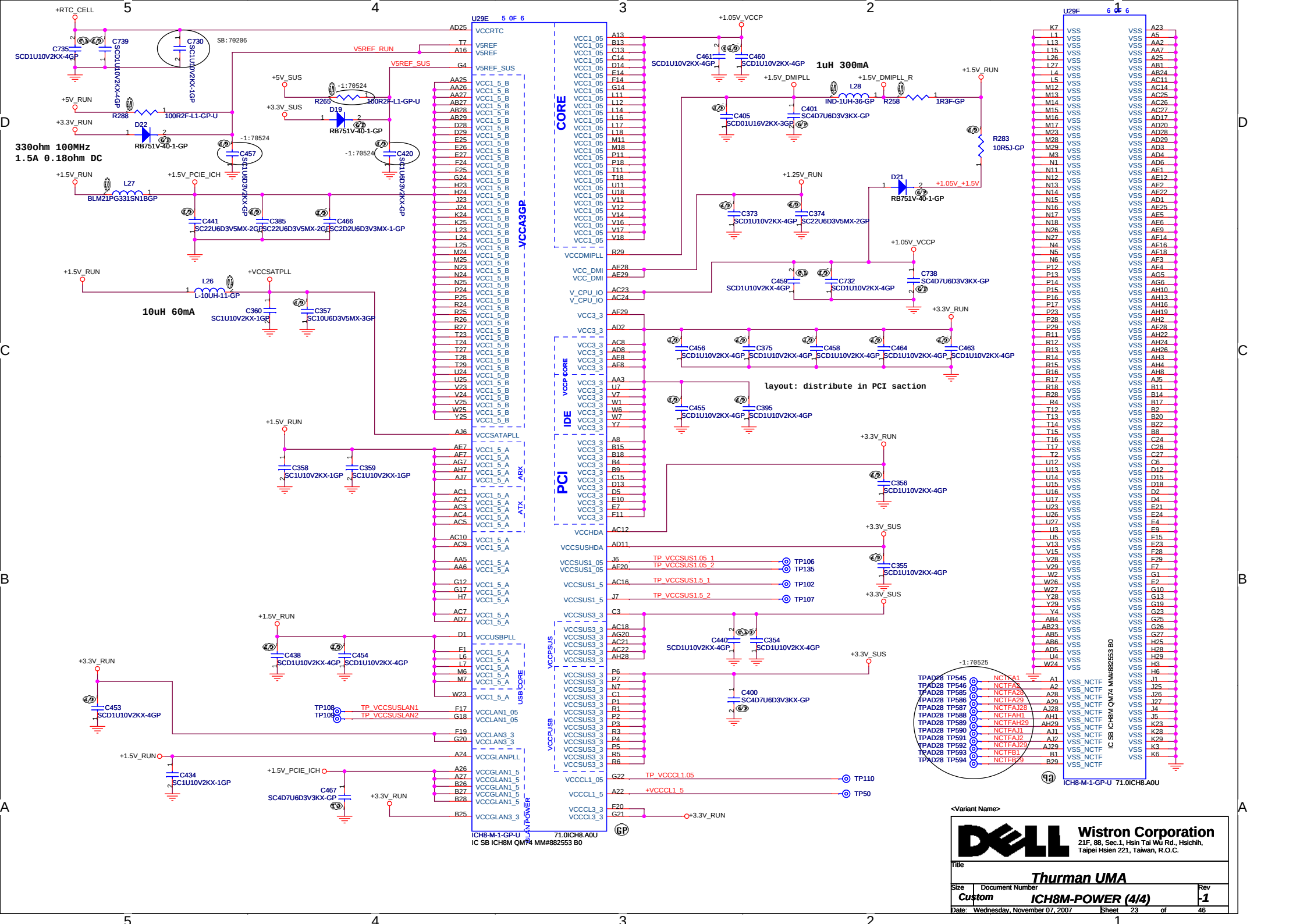
USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	MINI Card WLAN
USB9	

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA
Size: A3 | Document Number: ICH8M-PCIE/USB/SPI/DMI (2/4) | Rev: -1
Date: Thursday, November 22, 2007 | Sheet 21 of 46


SMBus address D2
FOR DDR2
These are for backdrive issue.
support ASF2.0
Note: Do not Populate this 0 ohm resistor for now.
CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M
ICH8-Strap PIN
No Reboot Strap
ICH_SPKR LOW = Defaule
High=No Reboot
ICH8-M-1-GP-U
IC SB ICH8M QM74 MM#882553 B0
71.0ICH8.A0U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Thurman UMA
ICH8M-CL/PM/GPIO (3/4)
Wednesday, November 07, 2007



Variant Name	<Variant Name>
Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thurman UMA
Size	Custom
Document Number	ICH8M-POWER (4/4)
Rev	-1
Date	Wednesday, November 07, 2007
Sheet	23 of 46

SSID = THERMAL

C276 Please Close to Guardian

Place near the bottom SODIMM CONN

REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil

Place inside CPU socket

C300 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

REM_DIODE4_N and REM_DIODE4_P routing Trace width and Spacing use 10 / 10 mil

Thermal sensor for Mini Card should be placed TOP Side under WWAN CARD

C295 Please close to Guardian

C260 Please Close to Guardian

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

U16

EMC4001-HZH-1GP

Version B: 74.04001.A73

Note :

VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C

should be placed BOT DIMM

pull up on SIO

C916, C459, C472 Please Close to Guardian

CPU THERMALTRIP

MCH THERMALTRIP

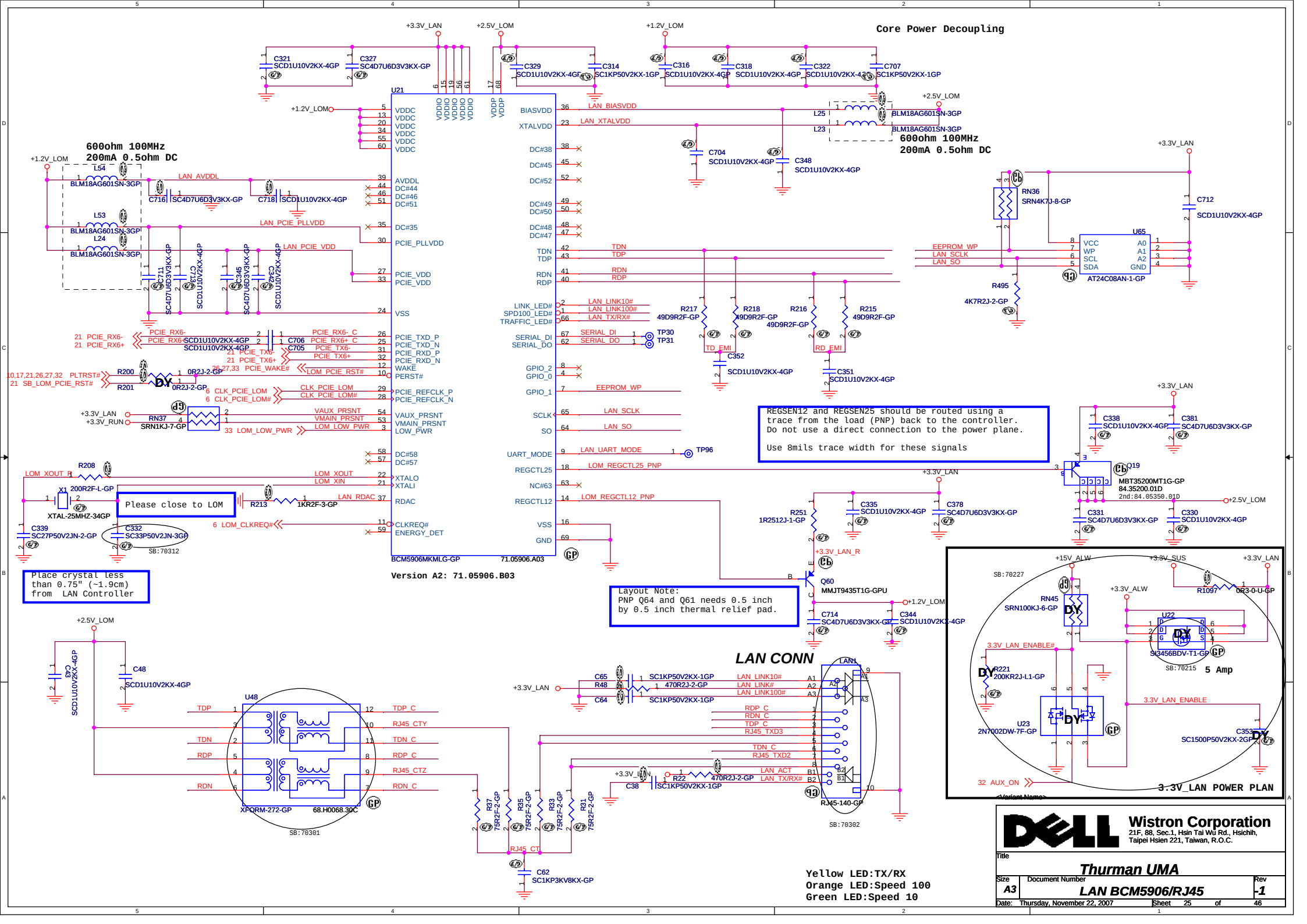
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

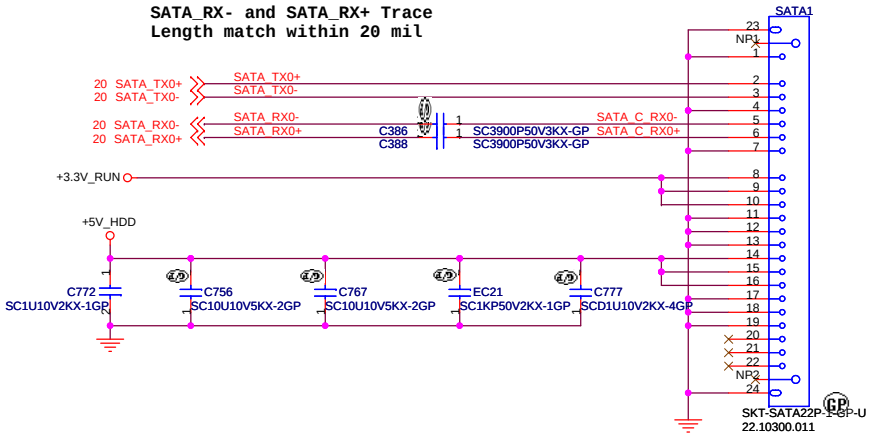
Size	Document Number	Rev
A3	FAN/EMC4001	-1

Date: Wednesday, November 07, 2007 Sheet 24 of 46

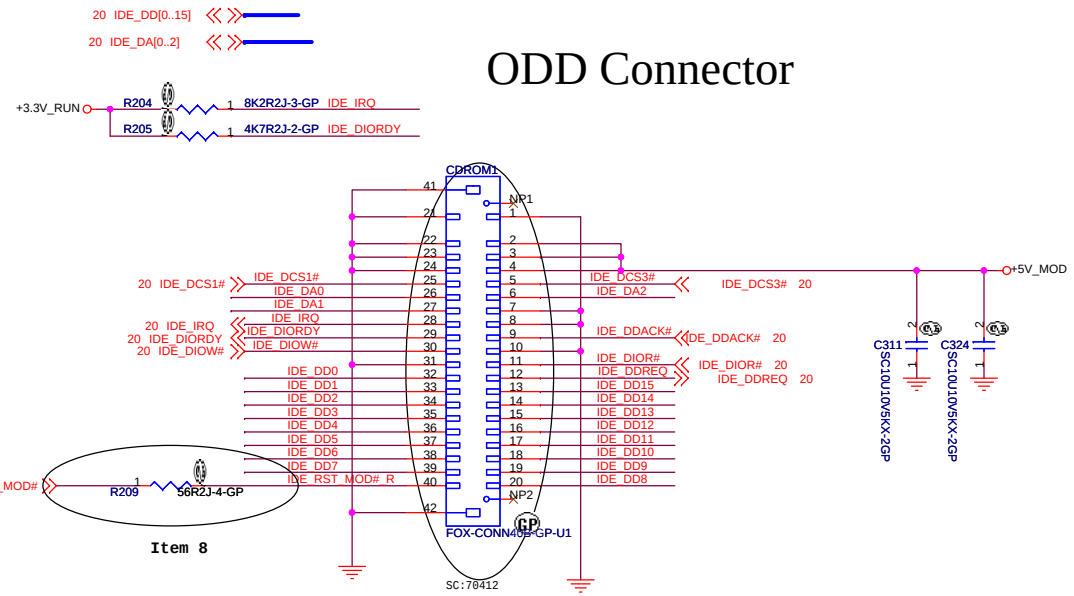

Core Power Decoupling
600ohm 100MHz
200mA 0.5ohm DC
600ohm 100MHz
200mA 0.5ohm DC
U21
BCM5906MKMLG-GP
71.05906.A03
Version A2: 71.05906.B03
REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.
Use 8mils trace width for these signals
Please close to LOM
Place crystal less than 0.75" (~1.9cm) from LAN Controller
Layout Note: PNP Q64 and Q61 needs 0.5 inch by 0.5 inch thermal relief pad.
LAN CONN
U48
XFORM-272-GP
68.H0068.30C
RJ45-140-GP
3.3V_LAN POWER PLAN
5 Amp
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Thurman UMA
LAN BCM5906/RJ45
Size A3
Rev -1
Date: Thursday, November 22, 2007
Sheet 25 of 46

SSID = IDE & SATA

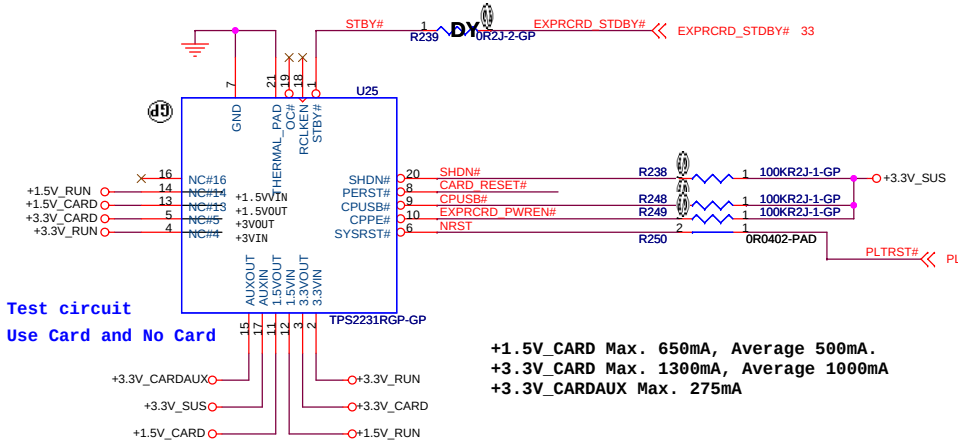
SATA HDD Connector

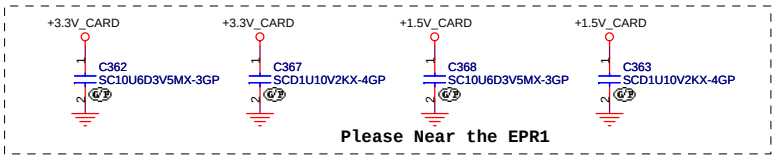


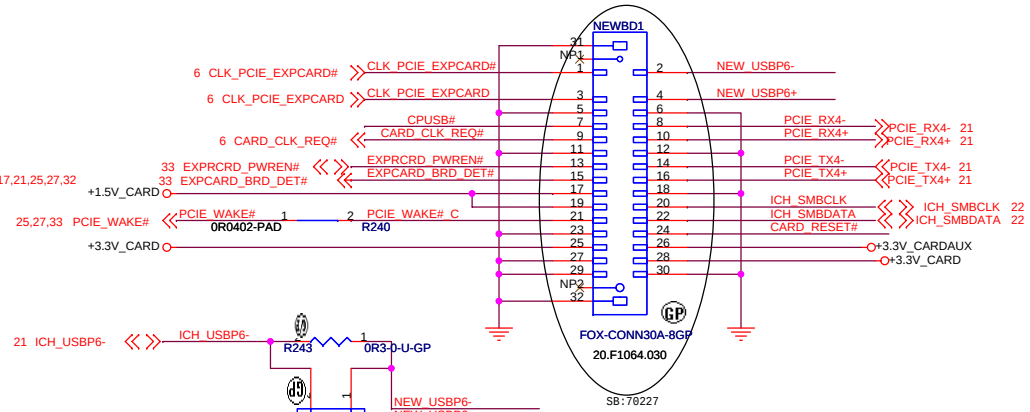
ODD Connector

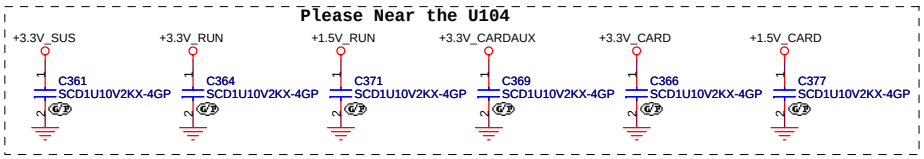


Express Card









<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thurman UMA*

Size	Document Number	Rev
A3	HDD/ODD/TO EXPRESS BD CONN	-1

Date: Wednesday, November 07, 2007 Sheet 26 of 46

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

DEBUG PINS

MiniCard WLAN connector

MiniCard WWAN connector

Prevent backdrive when WoW is enabled.

C587 Please Near the MINICARD1/Pin24

C337 Please Near the MINICARD2/Pin24

This circuit is only needed if the platform has the SNIFFER

For Debug card used only.

Layout note: Place caps EC10-EC14 close Mini Card connector.

Layout note: Place caps EC87,EC88 close SIM Card connector.

SB:070301

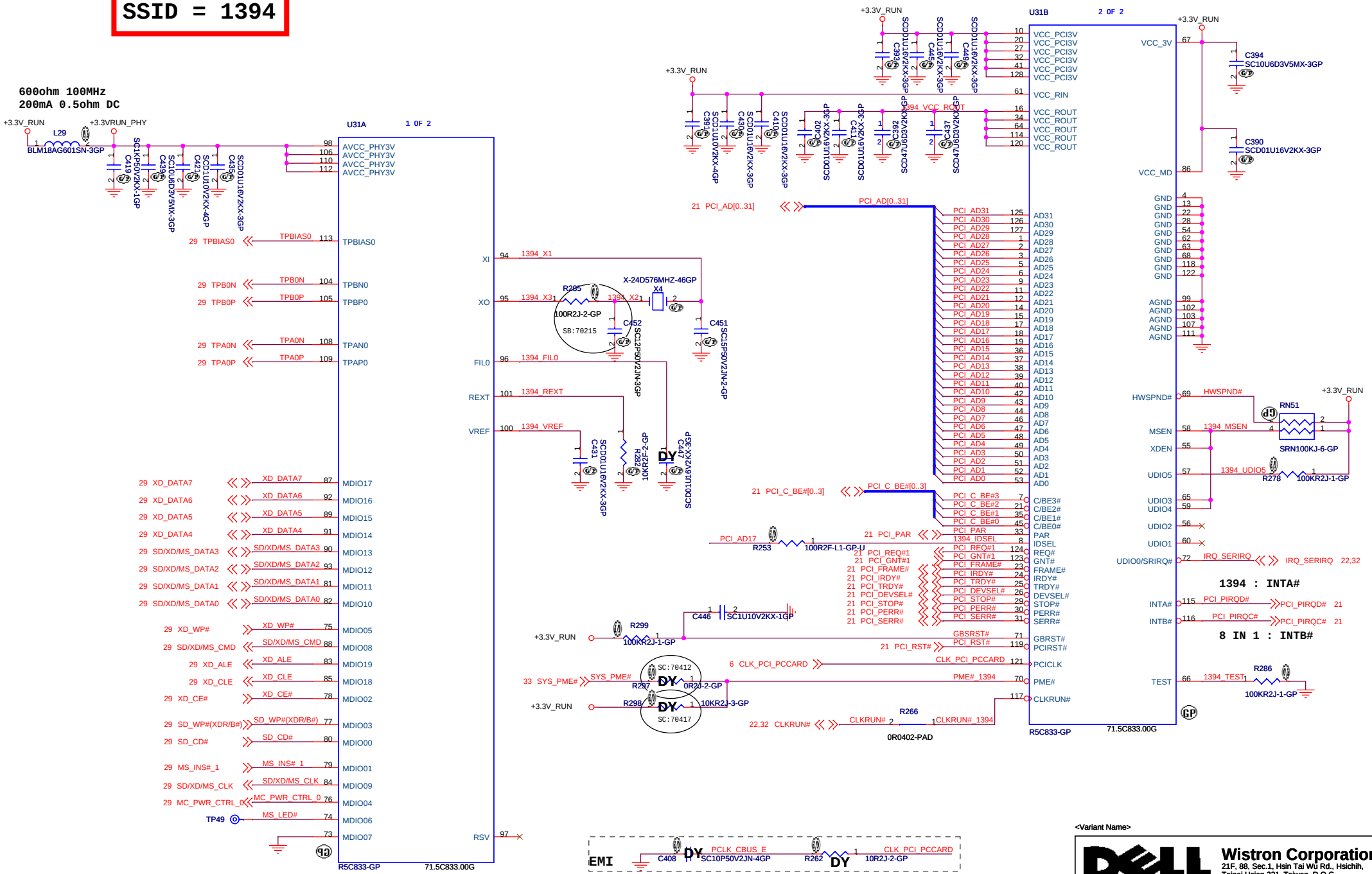
SC:70409

Close WLAN1

Variant Name	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thurman UMA
Size	A3
Document Number	MINICARD/WLAN/WWAN
Rev	-1
Date:	Wednesday, November 07, 2007
Sheet	27 of 46

SSID = 1394

600ohm 100MHz
200mA 0.5ohm DC

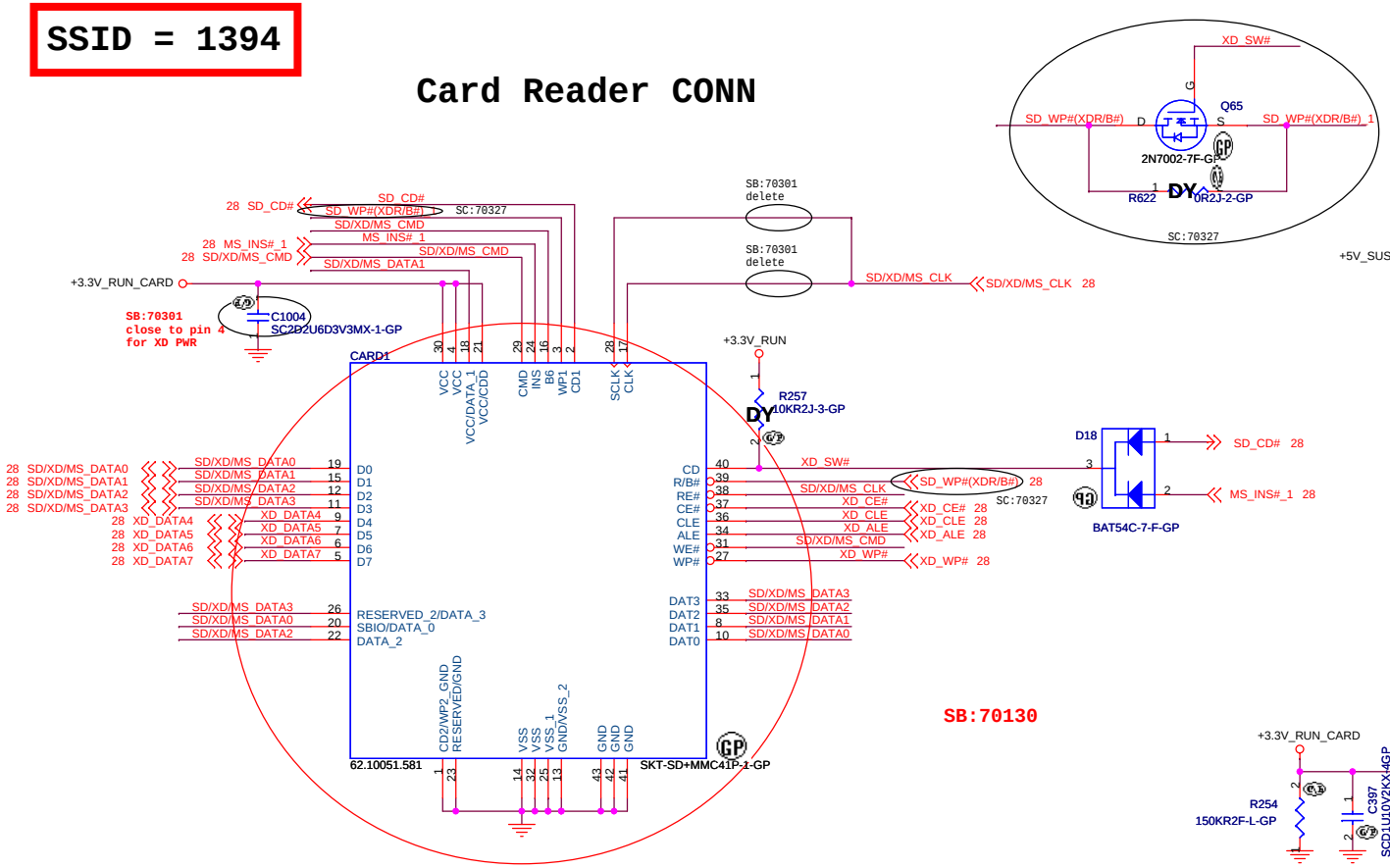


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

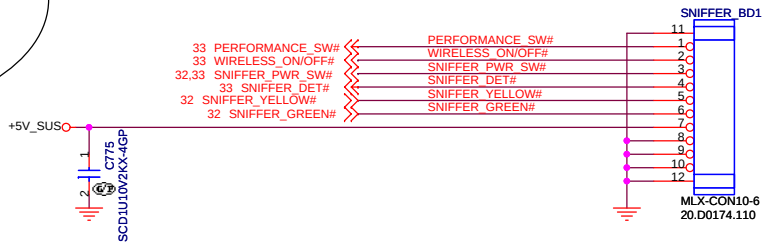
Title: Thurman UMA
Size: A3 | Document Number: 1394 R5C833 | Rev: -1
Date: Wednesday, November 07, 2007 | Sheet 28 of 46

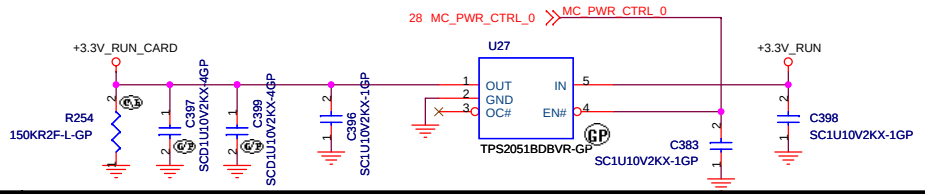
SSID = 1394

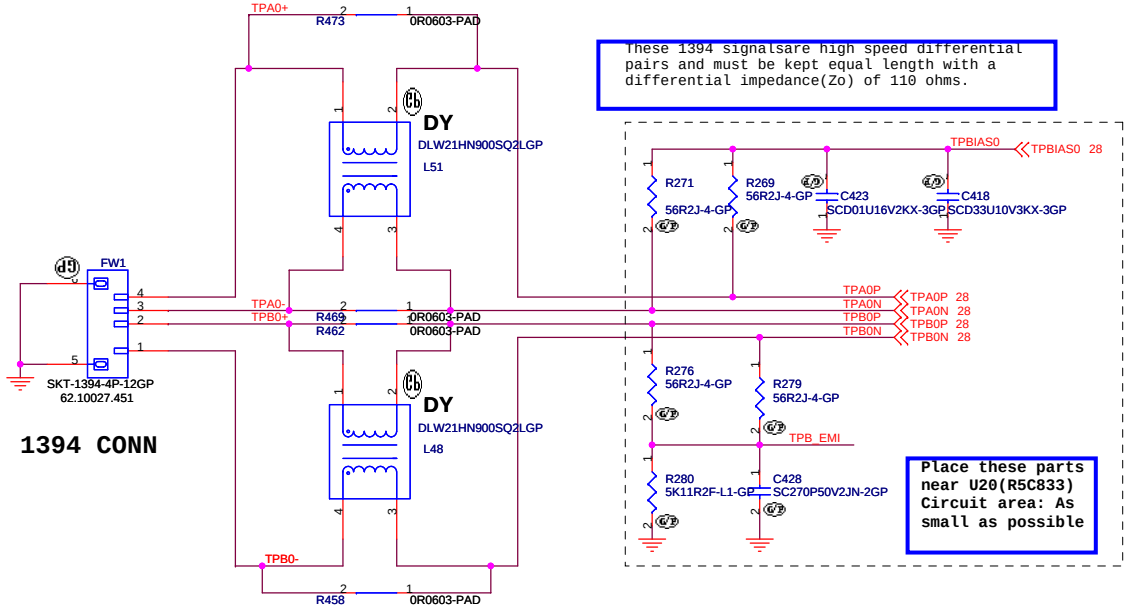
Card Reader CONN



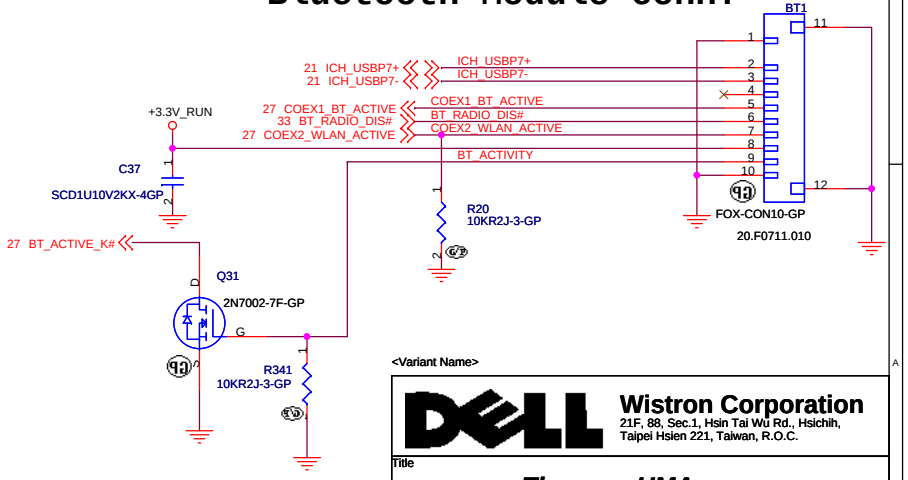
SNIFFER BOARD CONN







Bluetooth Module conn.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thurman UMA*

Size	Document Number	Rev
A3	8in1 /1394/SNIFFER BD CON/BT	-1

Date: Wednesday, November 07, 2007 Sheet 29 of 46

60ohm 100MHz
3000mA 0.05ohm DC

+3.3V_RUN
L60
BLM21PG600SN1-GP
+3V_RUN_DVDD_CORE
C783 SCD1U10V2KX-4GP
C450 SCD1U10V2KX-4GP
C791 SC1U10V2KX-1GP

U76
STAC9228X5TAEB4X-GP

DVDD_CORE
DVDD_CORE
DVDD
R284 100KR2J-1-GP
+3V_RUN_DVDD_CORE3
C448 SC1KP50V2KX-1GP

BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
20 ICH_AZ_CODEC_BITCLK
20 ICH_AZ_CODEC_SDIN0
20 ICH_AZ_CODEC_SDOUT
20 ICH_AZ_CODEC_SYNC
20 ICH_AZ_CODEC_RST#
R583 33R2J-2-GP
SB_AZ_CODEC_SDIN0_R

+3.3V_RUN
U36
74LVC1G125DC-GP
19 AUD_DMIC_CLK_G
AUD_DMIC_CLK_G
R306 0R2J-2-GP
AUD_DMIC_CLK

19 AUD_DMIC_IN0
31 AUD_EAPD#
AUD_DMIC_IN0
AUD_EAPD#
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
R584 4K7R2J-2-GP
11/06
17 AUD_SPDIF_OUT
AUD_SPDIF_OUT
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT

DVSS1
DVSS2

+VDDA
C770 SCD1U10V2KX-4GP
C436 SC1U10V2KX-1GP

AVDD1
AVDD2

SENSE_A
SENSE_B
AUD_SENSE_A
AUD_SENSE_B

PORT_A_L
PORT_A_R
VREFOUT_A
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_HP1_OUT_L 31
AUD_HP1_OUT_R 31
TO Audio OP

PORT_B_L
PORT_B_R
VREFOUT_B

PORT_C_L
PORT_C_R
VREFOUT_C
TO Audio OP

PORT_D_L
PORT_D_R
VREFOUT_D
AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_LINE_OUT_L 31
AUD_LINE_OUT_R 31

PORTE_L
PORTE_R
VREFOUT_E
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_B

PORTF_L
PORTF_R
VREFOUT_F
AUD_HP2_OUT_L 31
AUD_HP2_OUT_R 31

PORTG_L
PORTG_R

PORTH_L
PORTH_R

CD_L
CD_GND
CD_R

PC_BEEP
AUD_PC_BEEP

CAP2
VREFFILT
AUD_CAP2
AUD_VREFFLT
C760 SC10U10V5KX-2GP
C761 SC10U10V5KX-2GP

AVSS1
AVSS2

PC BEEP

C780 SCD1U10V2KX-4GP
AUD_BEEP
R302 20KR2J-L2-GP
AUD_SYS_BEEP
R587 10KR2J-3-GP
SB:70302

+VDDA
U33
74AHC1G86GW-GP
From SB
ICH_SPKR 22
BEEP 32
From EC

XOR gate

PORT C : LEAVE NC
IF NO INTERNAL MICS.

Port A---> HP1
Port E---> ext Mic
Port D---> Speaker
Port F---> HP2

+VDDA
R569 5K1R2F-2-GP
R573 39K2R2F-L-GP
C778 SC1KP50V2KX-1GP
HP1_NB_SENSE
Q64 2N7002-7F-GP
AUD_HP1_NB_SENSE 31,33
R300 5K1R2F-2-GP
R316 39K2R2F-L-GP
SB:70106
R313 20KR2J-L2-GP
C758 SC1KP50V2KX-1GP
MIC_SWITCH
AUD_HP2_NB_SENSE 22,31,33
Q24 2N7002DW-7F-GP
HP2_NB_SENSE
AUD_MIC_SWITCH

Change R352 to 2.67K
1% for AD1984

If SENSE_A total length
> 6" change C to 0.1uF

Azalia I/F EMI

ICH_AZ_CODEC_SDOUT
R578 47R2J-2-GP
ICH_AZ_CODEC_SDOUT1
C787 SCD1U10V2KX-4GP

Azalia I/F EMI

ICH_AZ_CODEC_BITCLK
R579 47R2J-2-GP
ICH_AZ_CODEC_BITCLK1
C788 SCD1U10V2KX-4GP

MIC IN

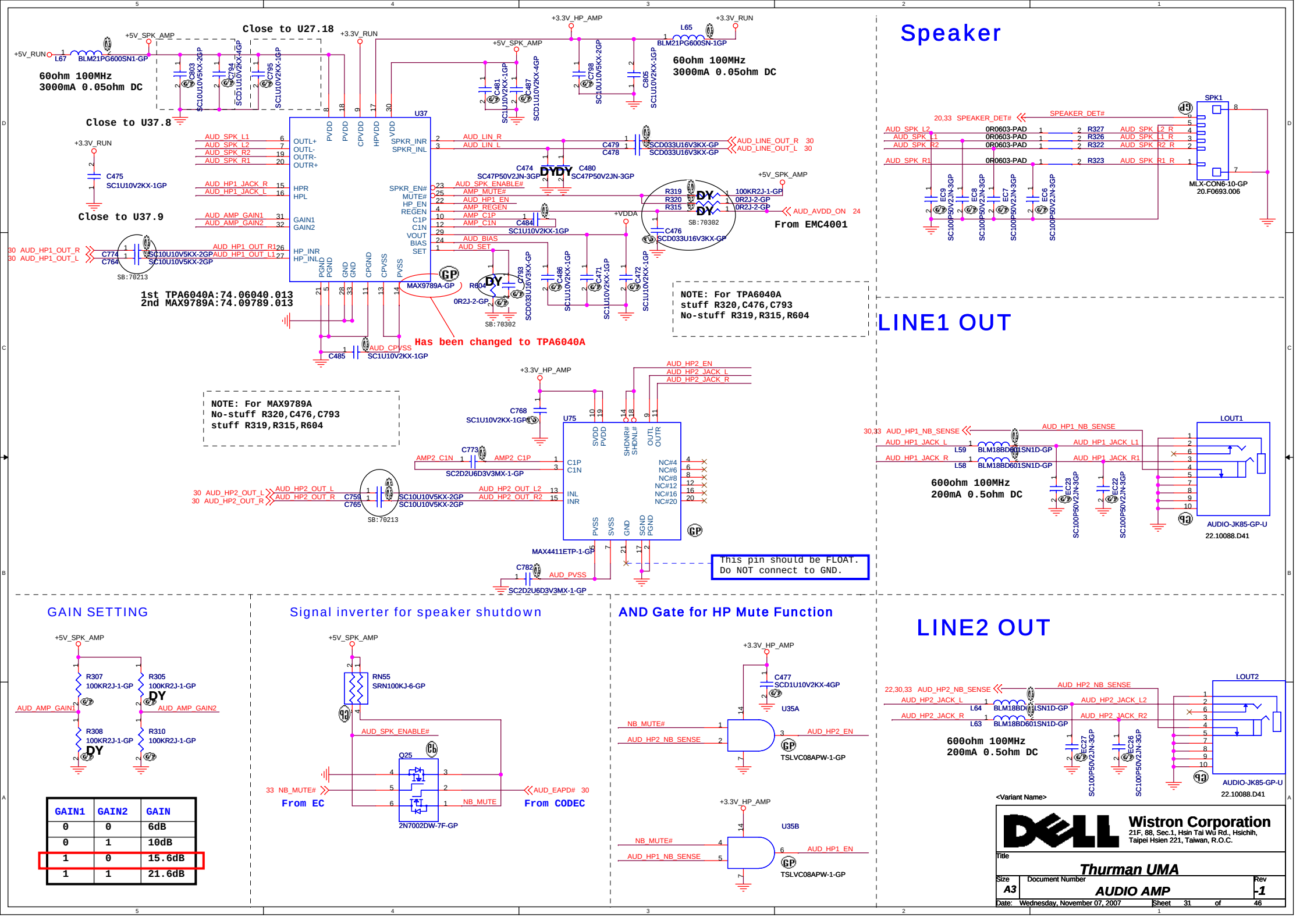
AUD_VREFOUT_B
R576 4K7R2J-2-GP
R599 4K7R2J-2-GP
C790 SC10U10V5KX-2GP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
C785 SC1U6D3V3KX-1GP
C789 SC1U6D3V3KX-1GP
MIC_IN_L_2
MIC_IN_R_2
R586
R594
-1:70524
MIC_IN_L_3
MIC_IN_R_3
0R0402-PAD
BLM18BD601SN1D-GP
L62
L61
MIC_IN_L_C
MIC_IN_R_C
+3.3V_RUN
R602 100KR2J-1-GP
AUD_MIC_SWITCH
MIC1
EC25 SC100P50V2JN-3GP
EC24 SC100P50V2JN-3GP
AUDIO-JK85-GP-U
22.10088.D41

600ohm 100MHz
200mA 0.5ohm DC

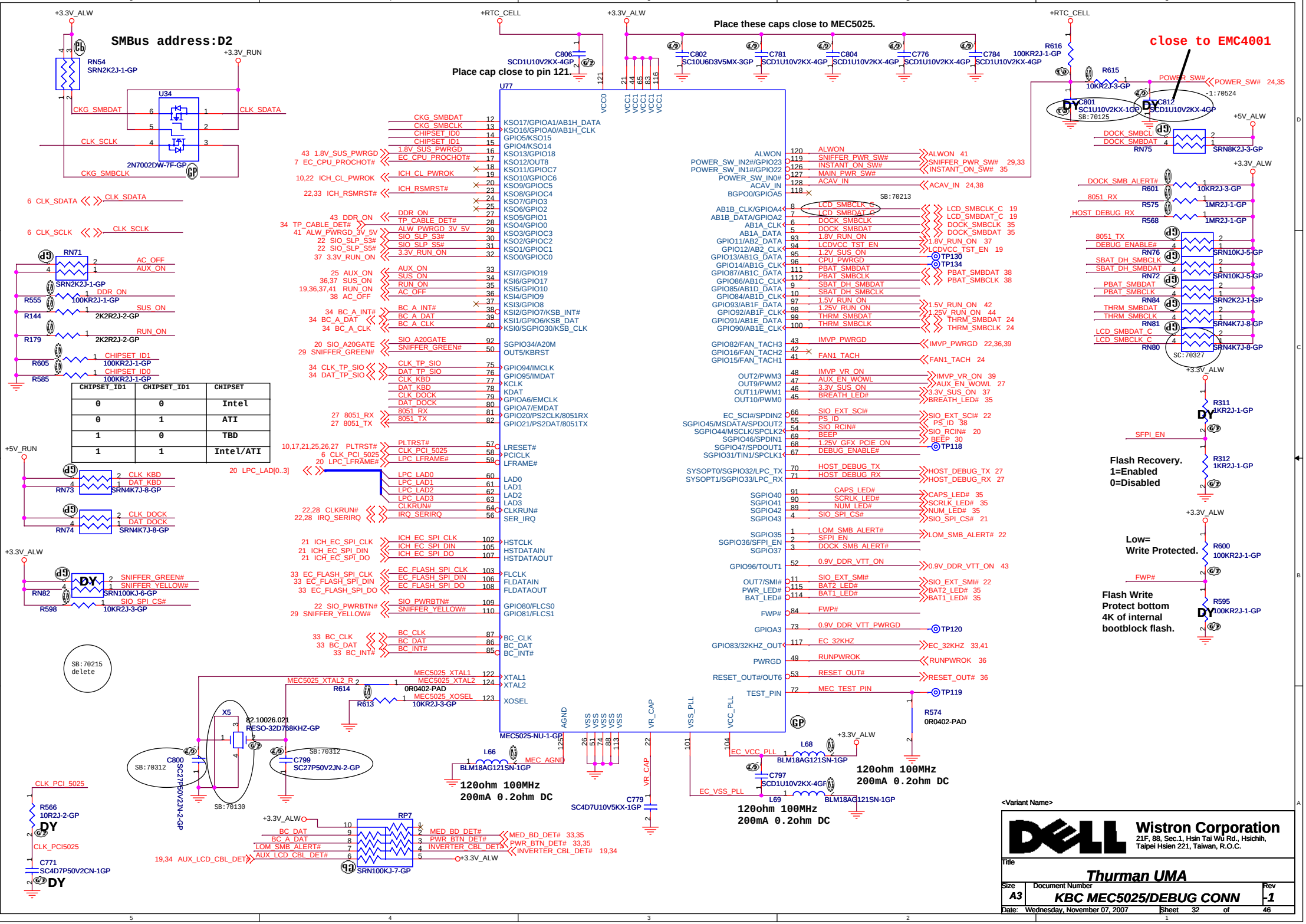
<Variant Name>

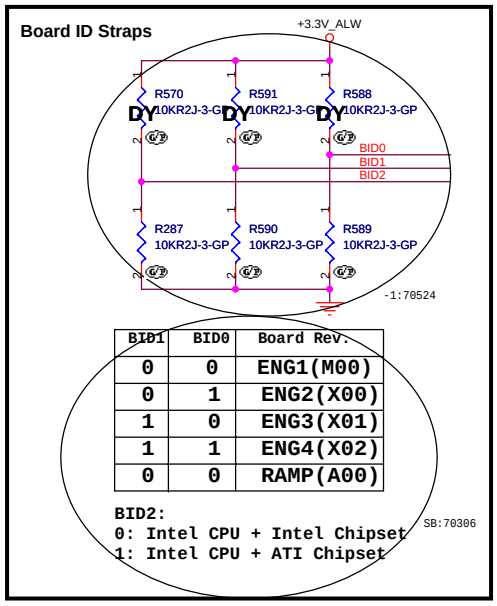
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA
Size: A3
Document Number: CODEC STAC9228
Rev: -1
Date: Thursday, November 22, 2007
Sheet 30 of 46

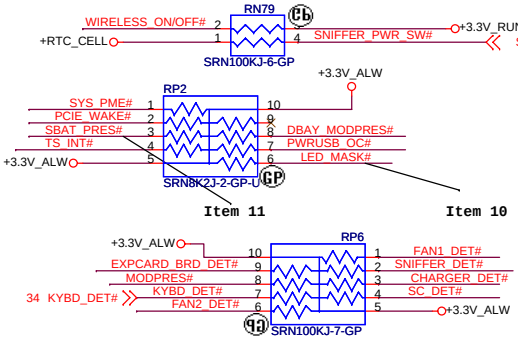


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

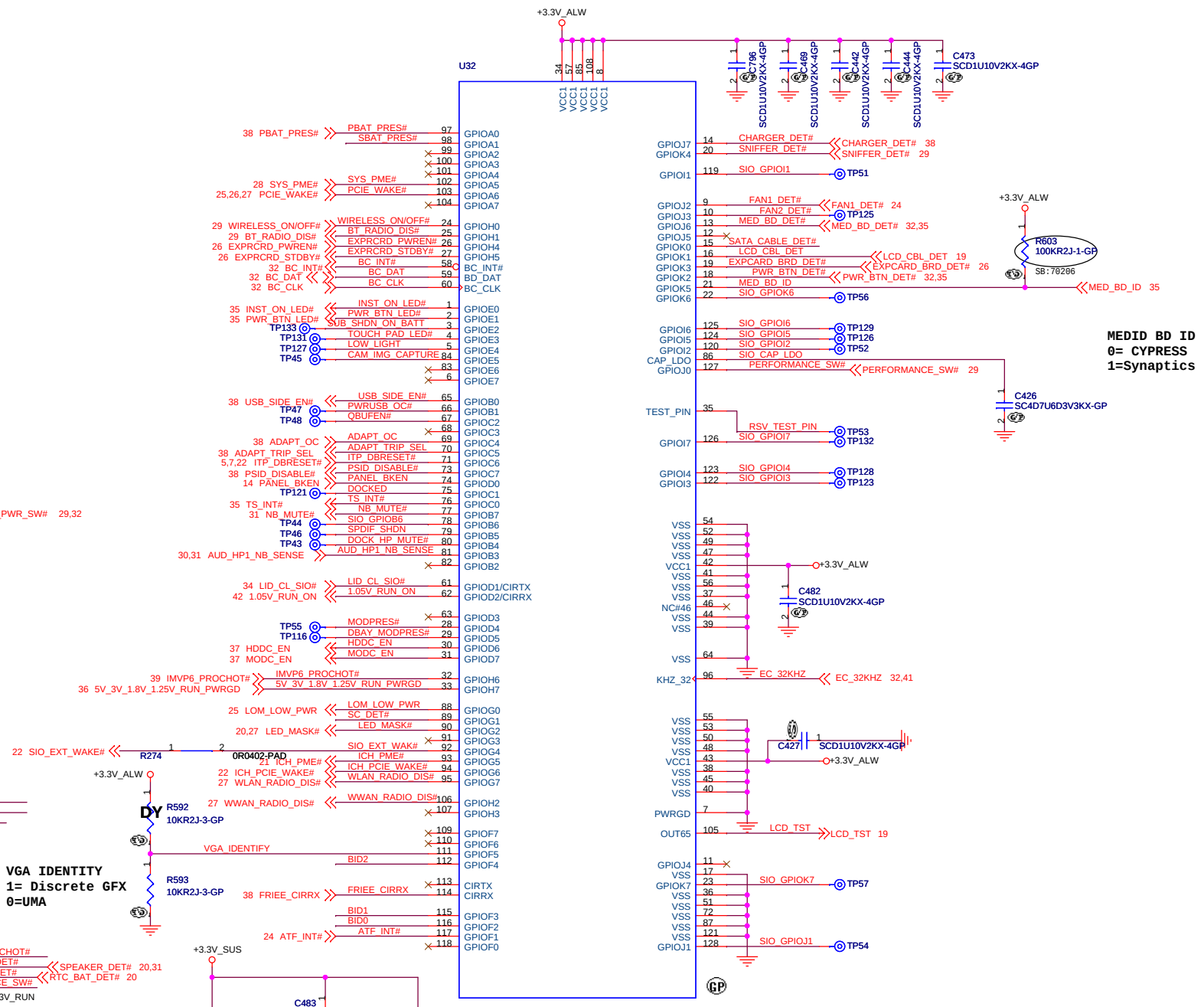

SMBus address:D2
Place these caps close to MEC5025.
Place cap close to pin 121.
close to EMC4001
U77
MEC5025-NU-1-GP
2N7002DW-7F-GP
SRN2K2J-1-GP
SRN4K7J-8-GP
SRN100KJ-6-GP
SRN100KJ-7-GP
SRN8K2J-3-GP
SRN10K2J-5-GP
SRN2K2J-1-GP
SRN4K7J-8-GP
SRN4K7J-8-GP
SC:70327
SB:70213
SB:70125
SB:70312
SB:70130
SB:70215
delete
CHIPSET_ID1 | CHIPSET_ID1 | CHIPSET
0 | 0 | Intel
0 | 1 | ATI
1 | 0 | TBD
1 | 1 | Intel/ATI
Flash Recovery.
1=Enabled
0=Disabled
Low=
Write Protected.
Flash Write
Protect bottom
4K of internal
bootblock flash.
120ohm 100MHz
200mA 0.2ohm DC
120ohm 100MHz
200mA 0.2ohm DC
120ohm 100MHz
200mA 0.2ohm DC
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size A3
Document Number
KBC MEC5025/DEBUG CONN
Rev -1
Date: Wednesday, November 07, 2007
Sheet 32 of 46



BID1	BID0	Board Rev.
0	0	ENG1(M00)
0	1	ENG2(X00)
1	0	ENG3(X01)
1	1	ENG4(X02)
0	0	RAMP(A00)

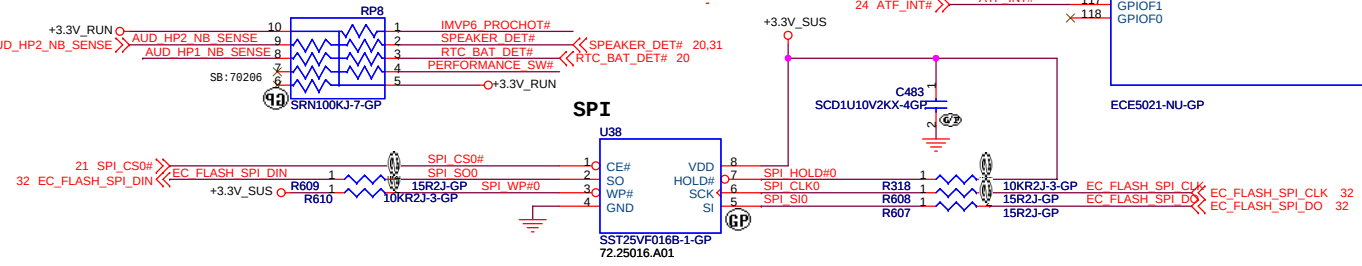


VGA IDENTITY
1= Discrete GFX
0=UMA



MEDID BD ID
0= CYPRESS
1=Synaptics

SPI



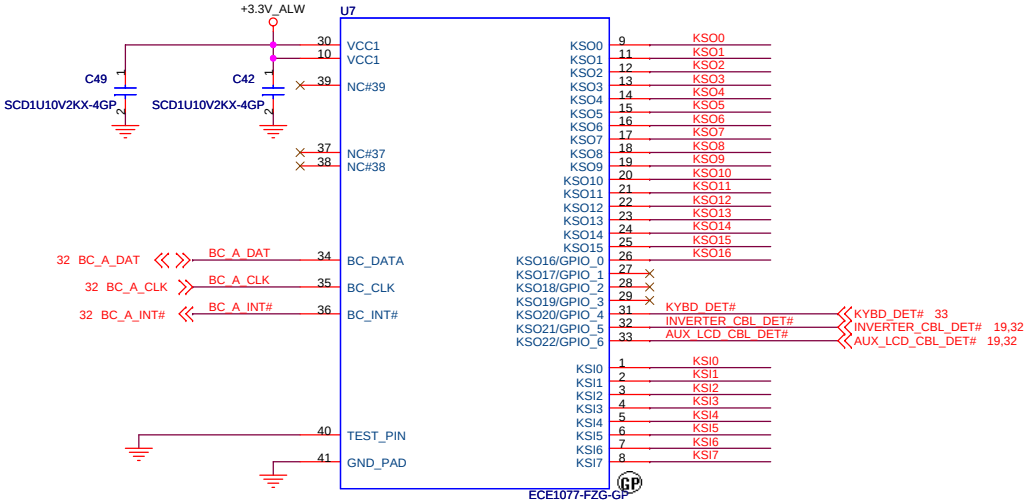
<Variant Name>

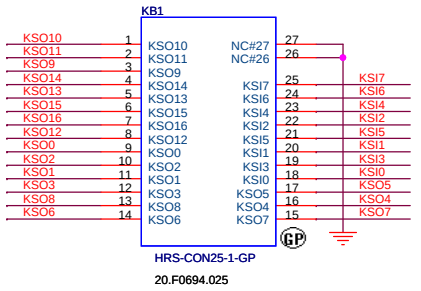
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

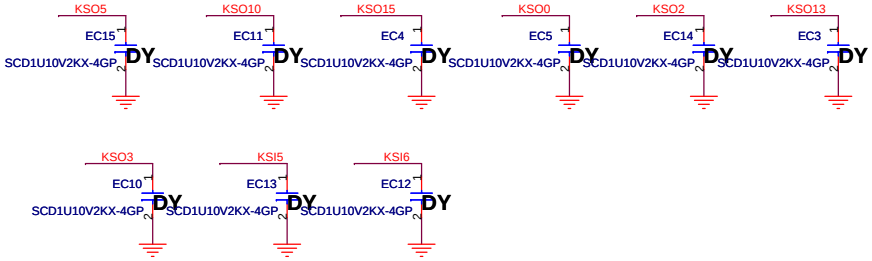
Title: Thurman UMA

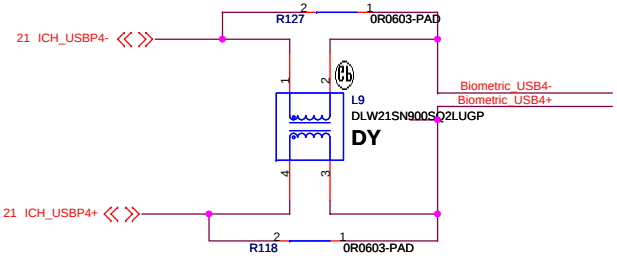
Size	Document Number	Rev
A3	SIO ECE5011/SPI ROM	-1

Date: Wednesday, November 07, 2007 Sheet 33 of 46

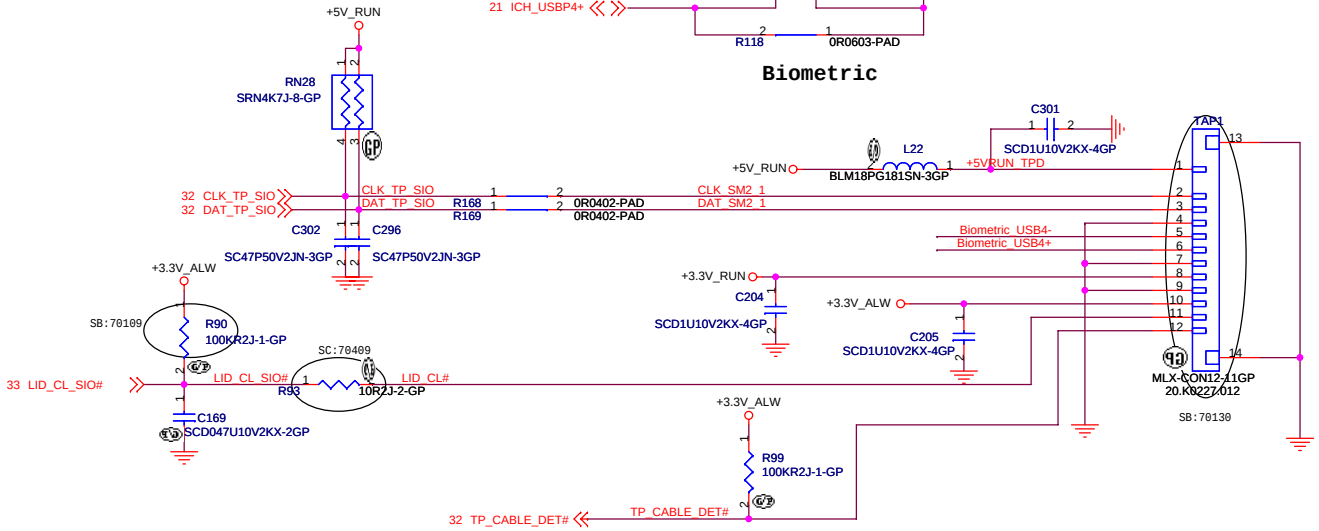








Biometric



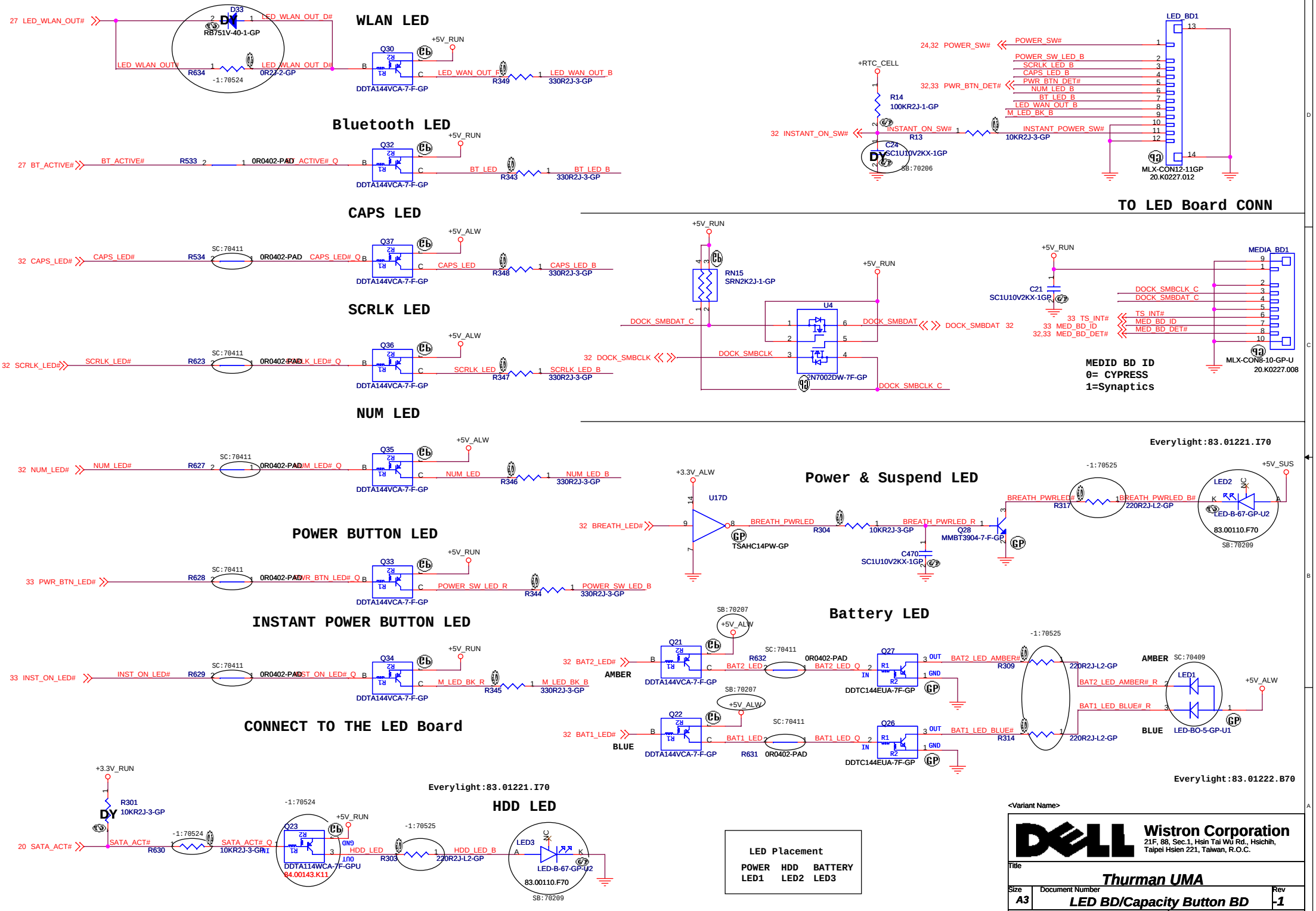
<variant_name>

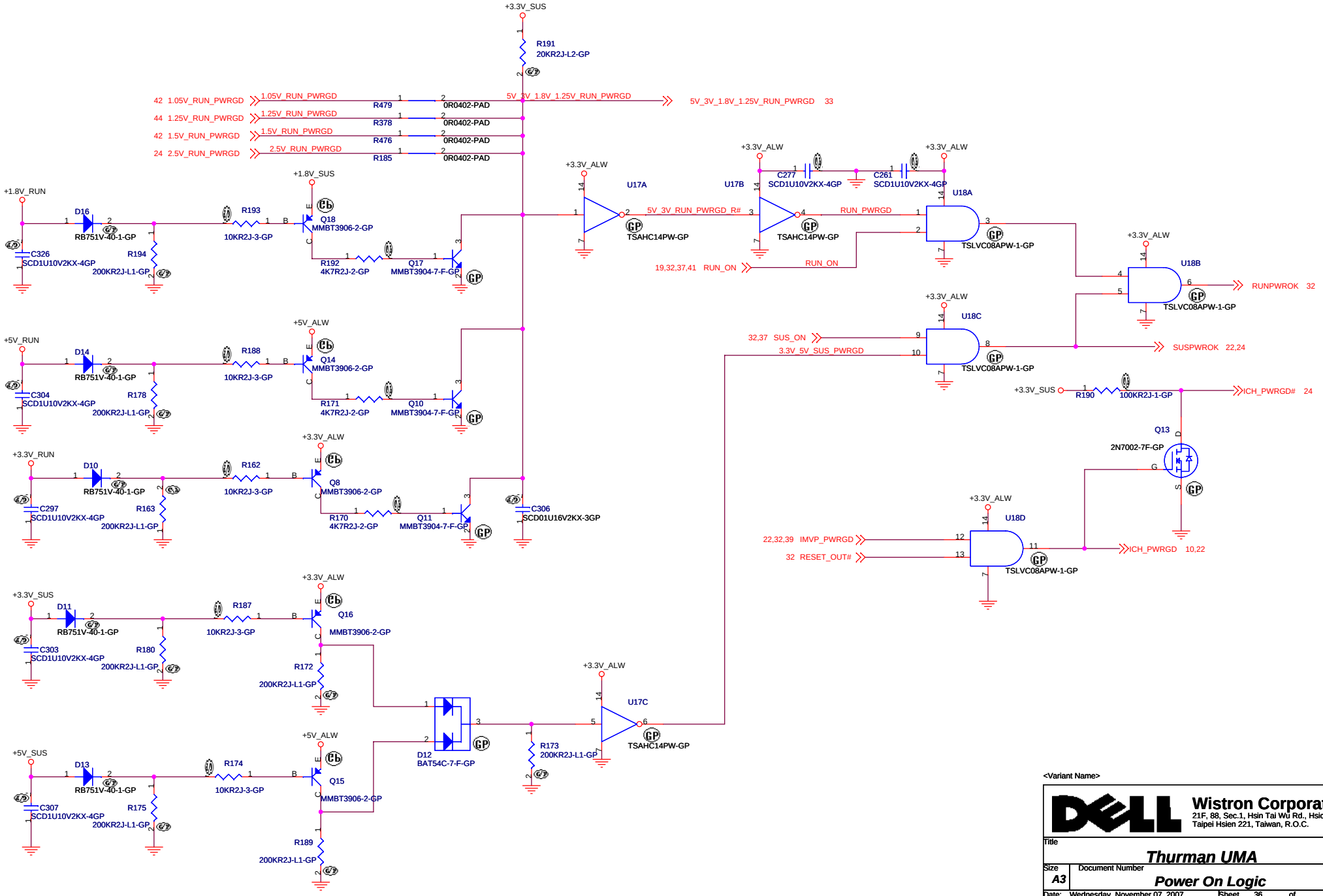
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

Size	Document Number	Rev
A3	SIO ECE1077/KB CONN/TP	-1

Date: Wednesday, November 07, 2007 Sheet 34 of 46


WLAN LED
Bluetooth LED
CAPS LED
SCRLK LED
NUM LED
POWER BUTTON LED
INSTANT POWER BUTTON LED
CONNECT TO THE LED Board
HDD LED
TO LED Board CONN
Power & Suspend LED
Battery LED
MEDID BD ID
0= CYPRESS
1=Synaptics
LED Placement
POWER LED1
HDD LED2
BATTERY LED3
Everylight:83.01221.I70
Everylight:83.01222.B70
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Thurman UMA
LED BD/Capacity Button BD
Size A3
Rev -1
Date: Wednesday, November 07, 2007
Sheet 35 of 46



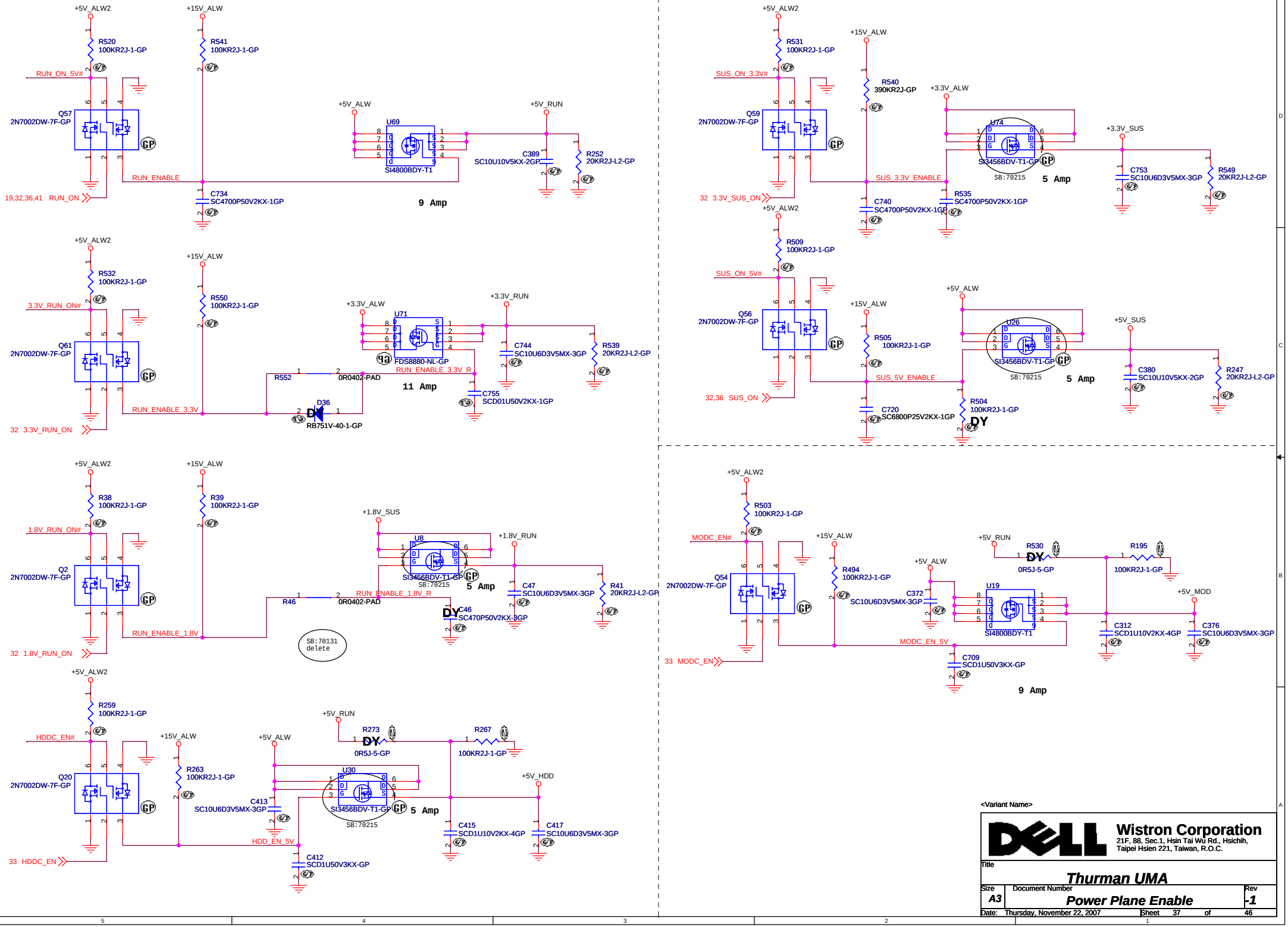
<Variant Name>

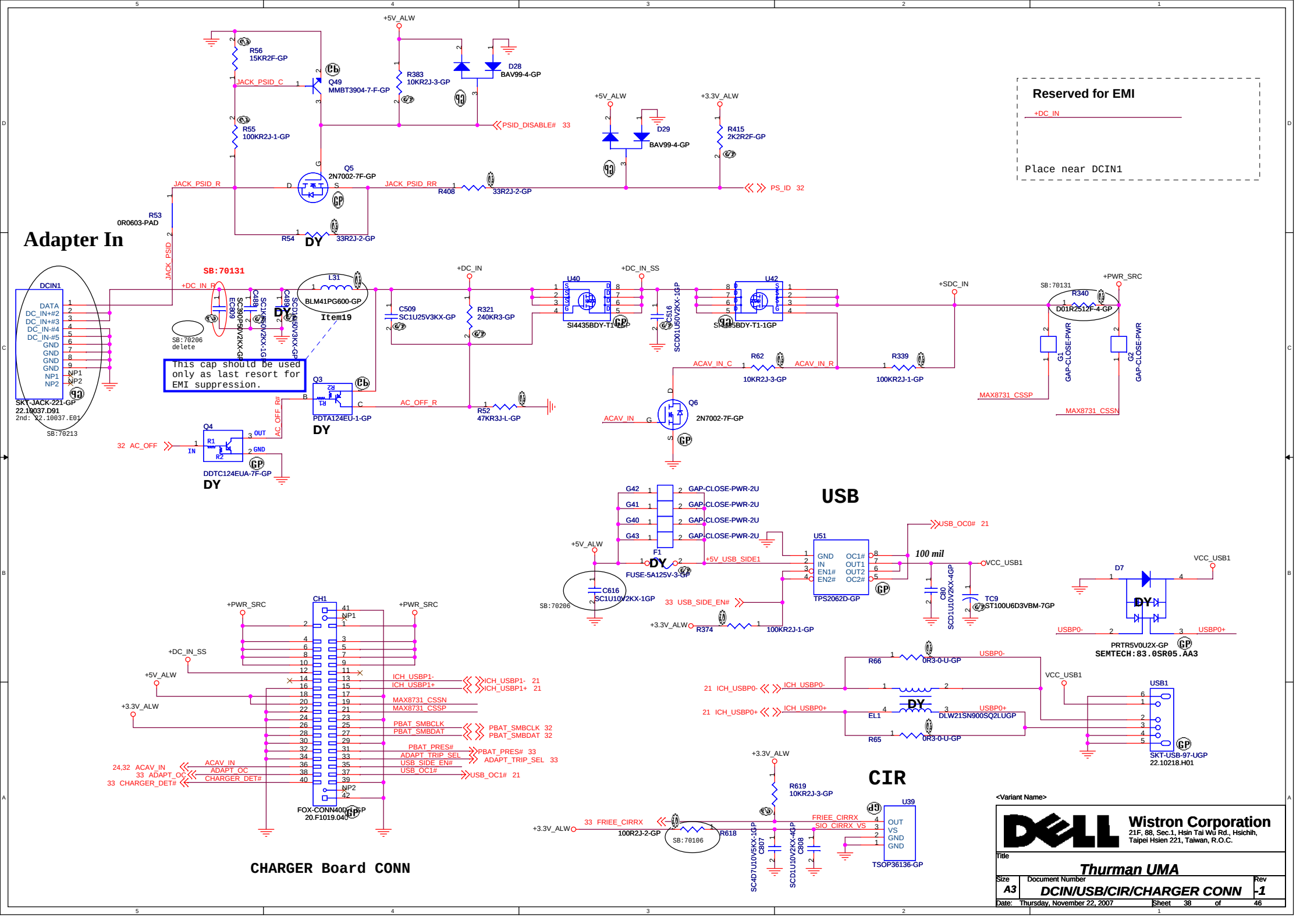
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thurman UMA**

Size	Document Number	Rev
A3	Power On Logic	-1

Date: Wednesday, November 07, 2007 Sheet 36 of 46


+5V_ALW2
+15V_ALW
R520 100KR2J-1-GP
R541 100KR2J-1-GP
RUN_ON_5V#
Q57 2N7002DW-7F-GP
RUN_ENABLE
19,32,36,41 RUN_ON
C734 SC4700P50V2KX-1GP
+5V_ALW
U69
SI4800BDY-T1
+5V_RUN
C389 SC10U10V5KX-2GP
R252 20KR2J-L2-GP
9 Amp
+5V_ALW2
+15V_ALW
R532 100KR2J-1-GP
R550 100KR2J-1-GP
3.3V_RUN_ON#
Q61 2N7002DW-7F-GP
RUN_ENABLE_3.3V
32 3.3V_RUN_ON
+3.3V_ALW
U71
FDS8880-NL-GP
+3.3V_RUN
R552 0R0402-PAD
RUN_ENABLE_3.3V_R
D36 RB751V-40-1-GP
C744 SC10U6D3V5MX-3GP
C755 SCD01U50V2KX-1GP
R539 20KR2J-L2-GP
11 Amp
+5V_ALW2
+15V_ALW
R38 100KR2J-1-GP
R39 100KR2J-1-GP
1.8V_RUN_ON#
Q2 2N7002DW-7F-GP
RUN_ENABLE_1.8V
32 1.8V_RUN_ON
+1.8V_SUS
U8
SI3456BDV-T1-GP
SB:70215
+1.8V_RUN
R46 0R0402-PAD
RUN_ENABLE_1.8V_R
C47 SC10U6D3V5MX-3GP
DY C46 SC470P50V2KX-3GP
R41 20KR2J-L2-GP
5 Amp
SB:70131 delete
+5V_ALW2
+15V_ALW
R259 100KR2J-1-GP
R263 100KR2J-1-GP
HDDC_EN#
Q20 2N7002DW-7F-GP
HDD_EN_5V
33 HDDC_EN
+5V_RUN
R273 DY 0R5J-5-GP
R267 100KR2J-1-GP
+5V_ALW
U30
SI3456BDV-T1-GP
SB:70215
+5V_HDD
C413 SC10U6D3V5MX-3GP
C412 SCD1U50V3KX-GP
C415 SCD1U10V2KX-4GP
C417 SC10U6D3V5MX-3GP
5 Amp
+5V_ALW2
+15V_ALW
R531 100KR2J-1-GP
R540 390KR2J-GP
SUS_ON_3.3V#
Q59 2N7002DW-7F-GP
SUS_3.3V_ENABLE
32 3.3V_SUS_ON
+3.3V_ALW
U74
SI3456BDV-T1-GP
SB:70215
+3.3V_SUS
C740 SC4700P50V2KX-1GP
R535 SC4700P50V2KX-1GP
C753 SC10U6D3V5MX-3GP
R549 20KR2J-L2-GP
5 Amp
+5V_ALW2
+15V_ALW
R509 100KR2J-1-GP
R505 100KR2J-1-GP
SUS_ON_5V#
Q56 2N7002DW-7F-GP
SUS_5V_ENABLE
32,36 SUS_ON
+5V_ALW
U26
SI3456BDV-T1-GP
SB:70215
+5V_SUS
C720 SC6800P25V2KX-1GP
R504 100KR2J-1-GP
DY
C380 SC10U10V5KX-2GP
R247 20KR2J-L2-GP
5 Amp
+5V_ALW2
R503 100KR2J-1-GP
MODC_EN#
Q54 2N7002DW-7F-GP
33 MODC_EN
+15V_ALW
R494 100KR2J-1-GP
MODC_EN_5V
+5V_ALW
C372 SC10U6D3V5MX-3GP
+5V_RUN
R530 DY 0R5J-5-GP
R195 100KR2J-1-GP
U19
SI4800BDY-T1
+5V_MOD
C709 SCD1U50V3KX-GP
C312 SCD1U10V2KX-4GP
C376 SC10U6D3V5MX-3GP
9 Amp
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size A3
Document Number
Power Plane Enable
Rev -1
Date: Thursday, November 22, 2007
Sheet 37 of 46


Adapter In
Reserved for EMI
+DC_IN
Place near DCIN1
R56 15KR2F-GP
Q49 MMBT3904-7-F-GP
R383 10KR2J-3-GP
D28 BAV99-4-GP
R55 100KR2J-1-GP
Q5 2N7002-7F-GP
R53 0R0603-PAD
R54 33R2J-2-GP
R408 33R2J-2-GP
D29 BAV99-4-GP
R415 2K2R2F-GP
PSID_DISABLE# 33
PS_ID 32
JACK_PSID_R
JACK_PSID_RR
JACK_PSID
DCIN1
SKT-JACK-221-GP
22.10037.D91
SB:70213
SB:70131
SB:70206 delete
This cap should be used only as last resort for EMI suppression.
L31 BLM41PG600-GP
Item19
C509 SC1U25V3KX-GP
R321 240KR3-GP
U40 SI4435BDY-T1-GP
U42 SI4435BDY-T1-GP
C516 SCD01U50V2KX-1GP
+DC_IN_SS
+SDC_IN
+PWR_SRC
R340 D01R2512F-4-GP
GAP-CLOSE-PWR
MAX8731_CSSP
MAX8731_CSSN
ACAV_IN_C
ACAV_IN_R
R62 10KR2J-3-GP
R339 100KR2J-1-GP
ACAV_IN
Q6 2N7002-7F-GP
Q3 PDTA124EU-1-GP
R52 47KR3J-L-GP
AC_OFF_R
Q4 DDTC124EUA-7F-GP
32 AC_OFF
DY
USB
G42 G41 G40 G43 GAP-CLOSE-PWR-2U
F1 FUSE-5A125V-3-GP
+5V_USB_SIDE1
U51 TPS2062D-GP
USB_OC0# 21
100 mil
VCC_USB1
TC9 ST100U6D3VBM-7GP
C616 SC1U10V2KX-1GP
33 USB_SIDE_EN#
R374 100KR2J-1-GP
D7 PRTR5V0U2X-GP
SEMTECH:83.0SR05.AA3
USBP0-
USBP0+
R66 0R3-0-U-GP
R65 0R3-0-U-GP
EL1 DLW21SN900SQ2LUGP
ICH_USBP0-
ICH_USBP0+
USB1 SKT-USB-97-UGP
22.10218.H01
CH1 FOX-CONN40D-GP
20.F1019.040
ICH_USBP1-
ICH_USBP1+
MAX8731_CSSN
MAX8731_CSSP
PBAT_SMBCLK
PBAT_SMBDAT
PBAT_PRES#
ADAPT_TRIP_SEL
USB_SIDE_EN#
USB_OC1#
ACAV_IN
ADAPT_OC
CHARGER_DET#
CHARGER Board CONN
CIR
R619 10KR2J-3-GP
R618 100R2J-2-GP
U39 TSOP36136-GP
FRIEE_CIRRX
SIO_CIRRX_VS
SC4D7U10V5KX-1GP C807
SCD1U10V2KX-4GP C808
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size A3
Document Number DCIN/USB/CIR/CHARGER CONN
Rev -1
Date: Thursday, November 22, 2007
Sheet 38 of 46

Thermal Design = 35.2A
Peak Current [Ipeak]= 44A
OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEFSX0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37

Item 14

-4 Layout Change

071113 Modify TC6

071018 add TC22

SB:70131

SB:70215

SB:70301

SB:70302

SB:70312

SB:70301 delete

SB:70215 del C72

EMI request

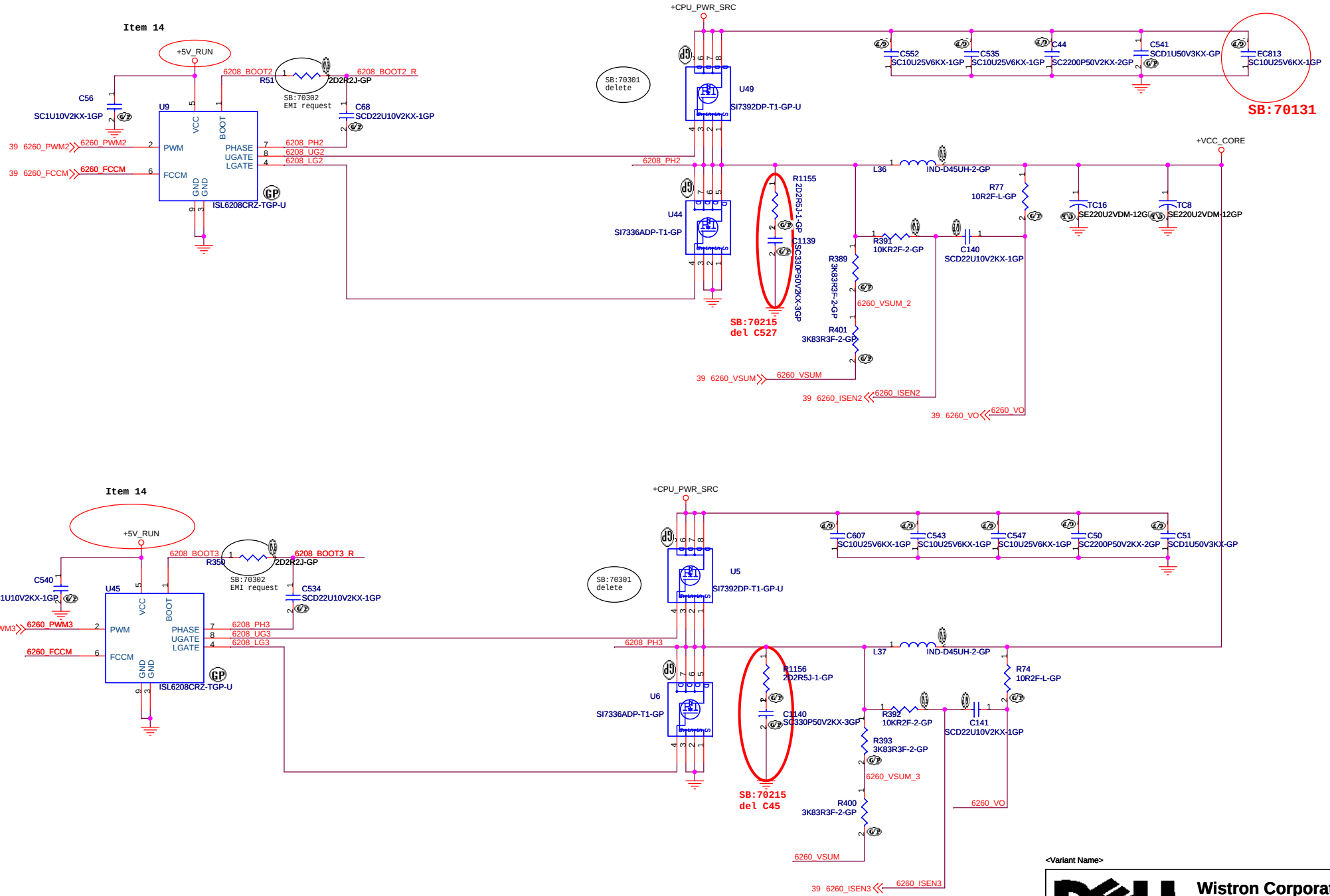
<Variant Name>

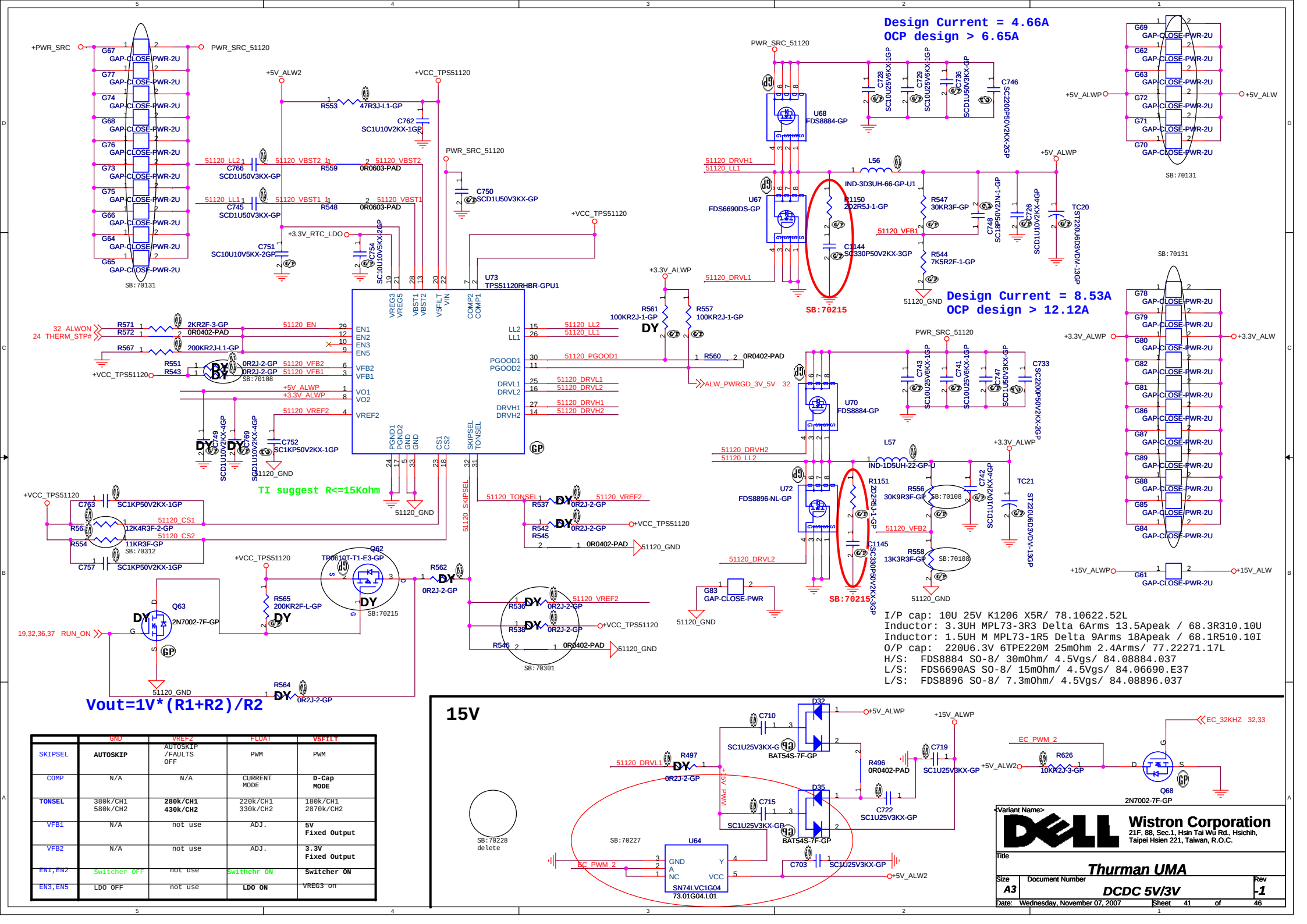
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

Size: A3 | Document Number: CPU Core-01 | Rev: -1

Date: Thursday, November 22, 2007 | Sheet 39 of 46


Item 14
+5V_RUN
6208_BOOT2
R51
2D2R2J-GP
6208_BOOT2_R
SB:70302
EMI request
C56
SC1U10V2KX-1GP
C68
SCD22U10V2KX-1GP
U9
VCC
BOOT
PWM
PHASE
UGATE
LGATE
FCCM
GND
GND
ISL6208CRZ-TGP-U
39 6260_PWM2
6260_PWM2
39 6260_FCCM
6260_FCCM
6208_PH2
6208_UG2
6208_LG2
+CPU_PWR_SRC
SB:70301
delete
U49
SI7392DP-T1-GP-U
C552
SC10U25V6KX-1GP
C535
SC10U25V6KX-1GP
C44
SC2200P50V2KX-2GP
C541
SCD1U50V3KX-GP
EC813
SC10U25V6KX-1GP
SB:70131
+VCC_CORE
U44
SI7336ADP-T1-GP
R1155
2D2R5J-1-GP
C1139
SC330P50V2KX-3GP
SB:70215
del C527
L36
IND-D45UH-2-GP
R77
10R2F-L-GP
TC16
SE220U2VDM-12GP
TC8
SE220U2VDM-12GP
R391
10KR2F-2-GP
C140
SCD22U10V2KX-1GP
R389
3K83R3F-2-GP
6260_VSUM_2
R401
3K83R3F-2-GP
39 6260_VSUM
6260_VSUM
39 6260_ISEN2
6260_ISEN2
39 6260_VO
6260_VO
Item 14
+5V_RUN
6208_BOOT3
R350
2D2R2J-GP
6208_BOOT3_R
SB:70302
EMI request
C540
SC1U10V2KX-1GP
C534
SCD22U10V2KX-1GP
U45
VCC
BOOT
PWM
PHASE
UGATE
LGATE
FCCM
GND
GND
ISL6208CRZ-TGP-U
39 6260_PWM3
6260_PWM3
6260_FCCM
6208_PH3
6208_UG3
6208_LG3
+CPU_PWR_SRC
SB:70301
delete
U5
SI7392DP-T1-GP-U
C607
SC10U25V6KX-1GP
C543
SC10U25V6KX-1GP
C547
SC10U25V6KX-1GP
C50
SC2200P50V2KX-2GP
C51
SCD1U50V3KX-GP
U6
SI7336ADP-T1-GP
R1156
2D2R5J-1-GP
C1140
SC330P50V2KX-3GP
SB:70215
del C45
L37
IND-D45UH-2-GP
R74
10R2F-L-GP
R392
10KR2F-2-GP
C141
SCD22U10V2KX-1GP
R393
3K83R3F-2-GP
6260_VSUM_3
R400
3K83R3F-2-GP
6260_VSUM
39 6260_ISEN3
6260_ISEN3
6260_VO
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size
A3
Document Number
CPU Core-02
Rev
-1
Date: Wednesday, November 07, 2007
Sheet 40 of 46



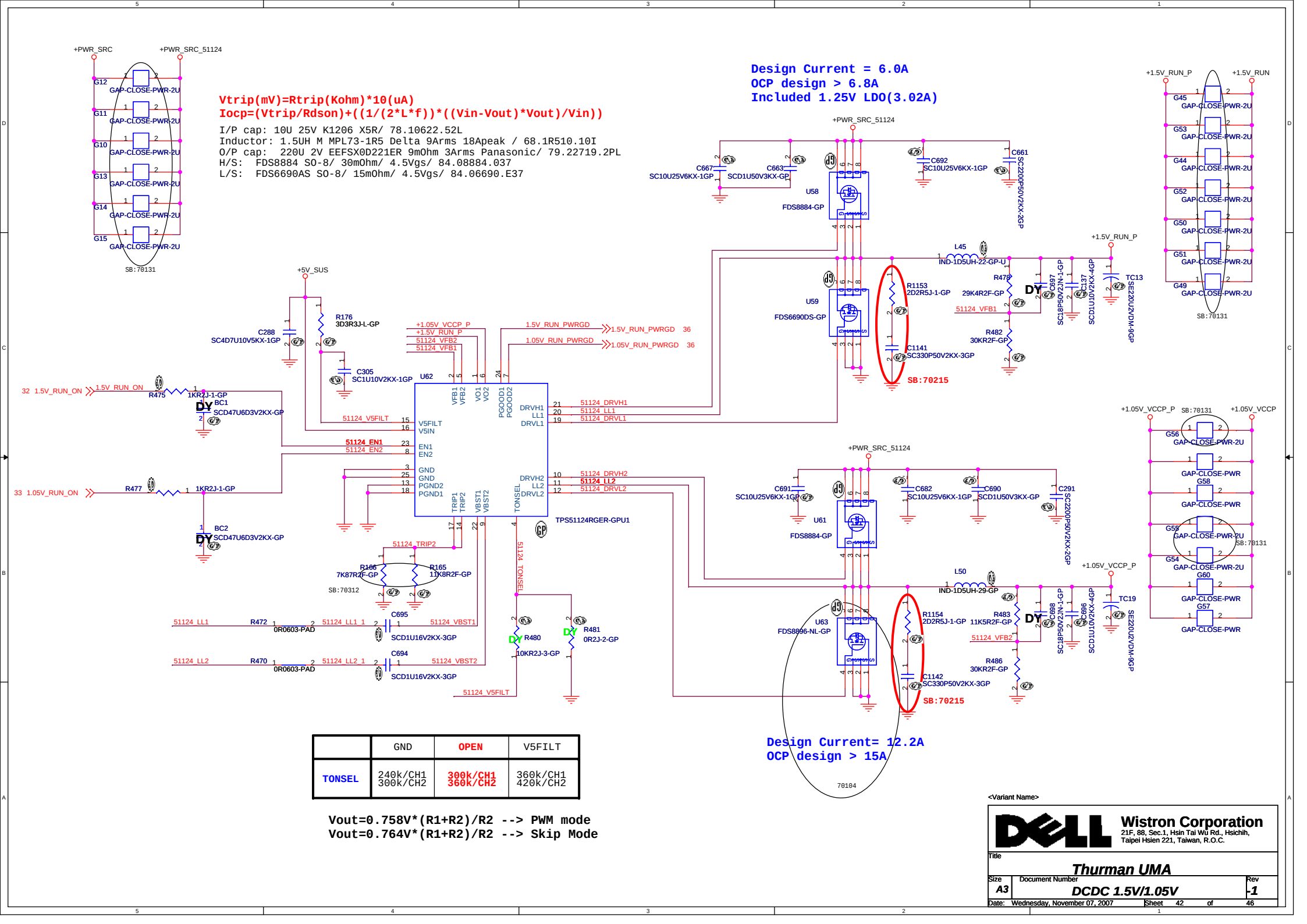
	GND	VREF2	FLOAT	VSFILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 ON

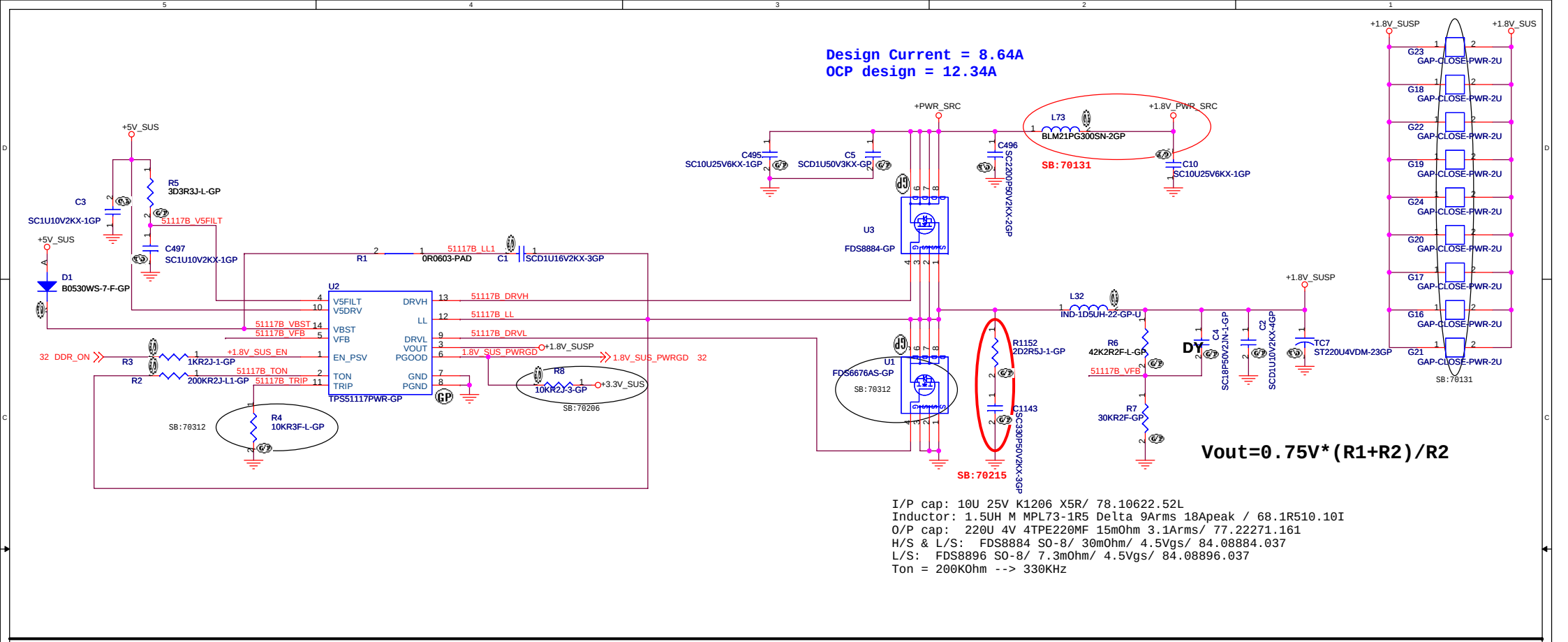
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

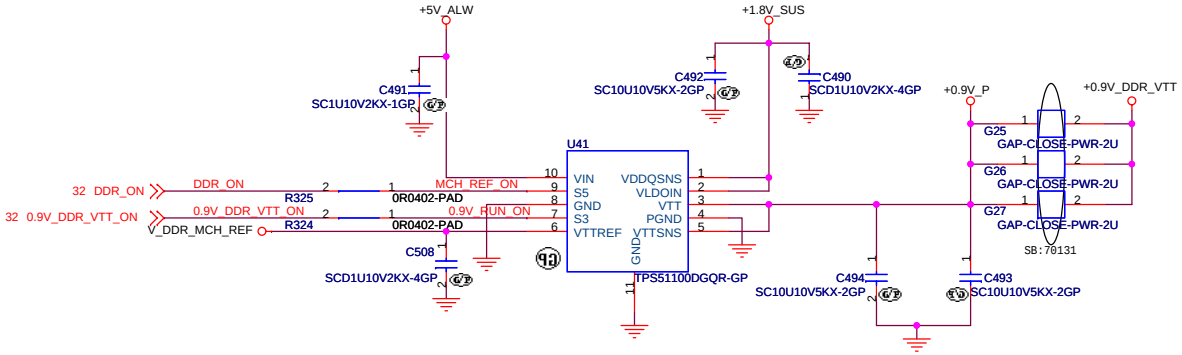
Size: A3 | Document Number: DCDC 5V/3V | Rev: -1

Date: Wednesday, November 07, 2007 | Sheet 41 of 46


+PWR_SRC
+PWR_SRC_51124
G12 GAP-CLOSE-PWR-2U
G11 GAP-CLOSE-PWR-2U
G10 GAP-CLOSE-PWR-2U
G13 GAP-CLOSE-PWR-2U
G14 GAP-CLOSE-PWR-2U
G15 GAP-CLOSE-PWR-2U
SB:70131
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37
Design Current = 6.0A
OCP design > 6.8A
Included 1.25V LDO(3.02A)
+PWR_SRC_51124
C667 SC10U25V6KX-1GP
C663 SCD1U50V3KX-GP
U58 FDS8884-GP
C692 SC10U25V6KX-1GP
C661 SC2200P50V2KX-2GP
+1.5V_RUN_P
+1.5V_RUN
G45 GAP-CLOSE-PWR-2U
G53 GAP-CLOSE-PWR-2U
G44 GAP-CLOSE-PWR-2U
G52 GAP-CLOSE-PWR-2U
G50 GAP-CLOSE-PWR-2U
G51 GAP-CLOSE-PWR-2U
G49 GAP-CLOSE-PWR-2U
SB:70131
L45 IND-1D5UH-22-GP-U
U59 FDS6690DS-GP
R1153 2D2R5J-1-GP
R479 29K4R2F-GP
DY
C697 SC18P50V2JN-1-GP
C137 SCD1U10V2KX-4GP
TC13 SE220U2VDM-9GP
R482 30KR2F-GP
C1141 SC330P50V2KX-3GP
SB:70215
+5V_SUS
R176 3D3R3J-L-GP
C288 SC4D7U10V5KX-1GP
C305 SC1U10V2KX-1GP
+1.05V_VCCP_P
+1.5V_RUN_P
51124_VFB2
51124_VFB1
1.5V_RUN_PWRGD
1.05V_RUN_PWRGD
32 1.5V_RUN_ON
R475 1KR2J-1-GP
BC1 SCD47U6D3V2KX-GP
51124_V5FILT
51124_EN1
51124_EN2
U62
VFB1 VFB2 VO1 VO2 PGOOD1 PGOOD2
V5FILT VSIN EN1 EN2 GND GND PGND2 PGND1
DRVH1 LL1 DRVL1 DRVH2 LL2 DRVL2 TONSEL TRIP1 TRIP2 VBST1 VBST2
TPS51124RGER-GPU1
51124_DRVH1
51124_LL1
51124_DRVL1
51124_DRVH2
51124_LL2
51124_DRVL2
33 1.05V_RUN_ON
R477 1KR2J-1-GP
BC2 SCD47U6D3V2KX-GP
51124_TRIP2
R166 7K87R2F-GP
R165 11K8R2F-GP
SB:70312
C695 SCD1U16V2KX-3GP
C694 SCD1U16V2KX-3GP
R472 0R0603-PAD
R470 0R0603-PAD
51124_LL1_1
51124_LL2_1
51124_VBST1
51124_VBST2
51124_TONSEL
R480 10KR2J-3-GP
R481 0R2J-2-GP
51124_V5FILT
+PWR_SRC_51124
C691 SC10U25V6KX-1GP
C682 SC10U25V6KX-1GP
C690 SCD1U50V3KX-GP
C291 SC2200P50V2KX-2GP
U61 FDS8884-GP
+1.05V_VCCP_P
+1.05V_VCCP
G56 GAP-CLOSE-PWR-2U
G58 GAP-CLOSE-PWR
G55 GAP-CLOSE-PWR-2U
G54 GAP-CLOSE-PWR-2U
G60 GAP-CLOSE-PWR
G57 GAP-CLOSE-PWR
SB:70131
L50 IND-1D5UH-29-GP
U63 FDS8896-NL-GP
R1154 2D2R5J-1-GP
R483 11K5R2F-GP
C698 SC18P50V2JN-1-GP
C696 SCD1U10V2KX-4GP
TC19 SE220U2VDM-9GP
R486 30KR2F-GP
C1142 SC330P50V2KX-3GP
SB:70215
Design Current= 12.2A
OCP design > 15A
70104
GND 240k/CH1 300k/CH2
OPEN 300k/CH1 360k/CH2
V5FILT 360k/CH1 420k/CH2
TONSEL
Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thurman UMA
Size A3
Document Number
DCDC 1.5V/1.05V
Rev -1
Date: Wednesday, November 07, 2007
Sheet 42 of 46



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHz



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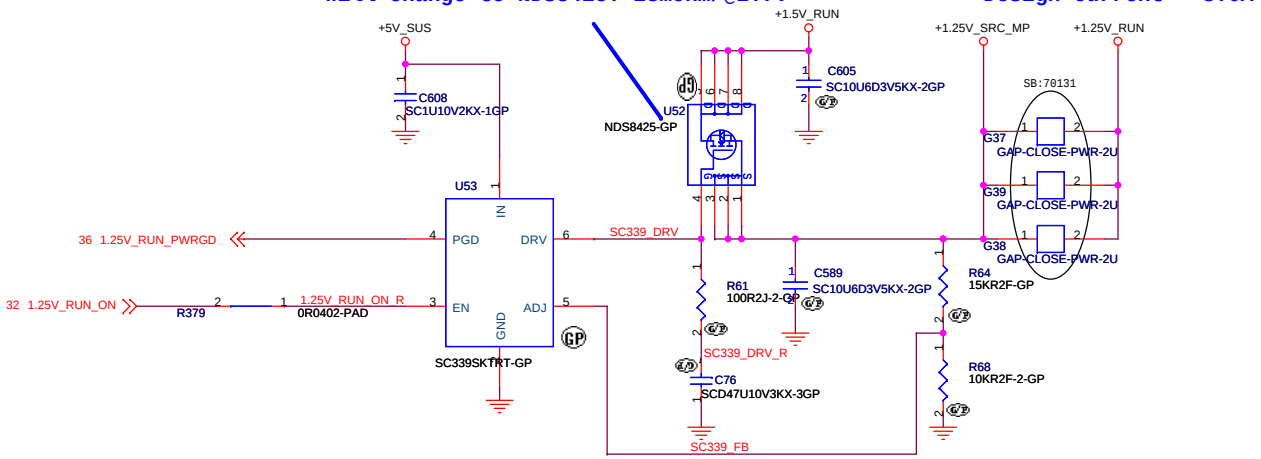
Title	Thurman UMA	
Size: A3	Document Number: DCDC 1.8V/0.9V	Rev: -1
Date: Wednesday, November 07, 2007	Sheet 43 of 46	

Will Change to NDS8425. 28mOhm/@2.7V

Design Current = 3.0A



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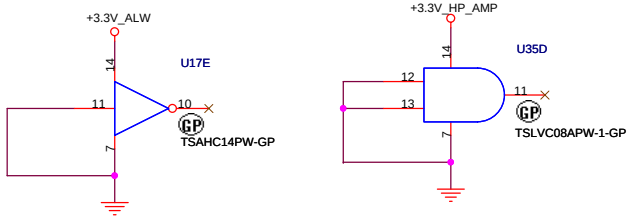
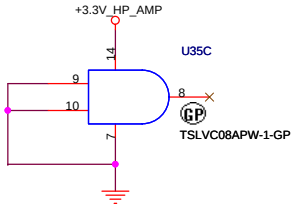
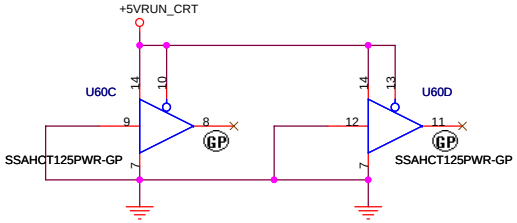
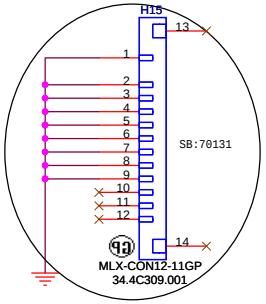
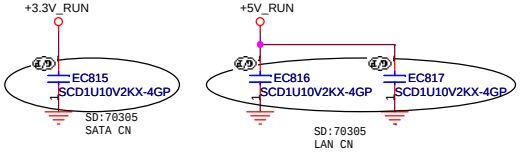
Size: *A3*	Document Number: *DCDC 1.25V*	Rev: *-1*
Date: Wednesday, November 07, 2007	Sheet 44 of 46	











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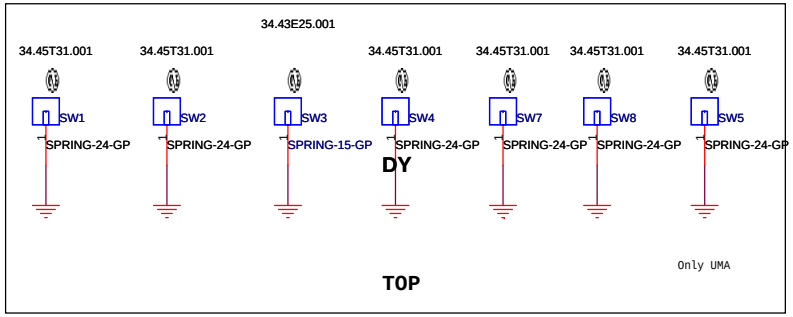
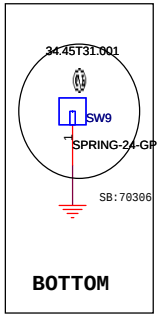
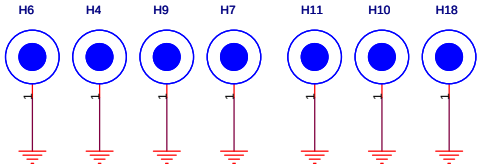
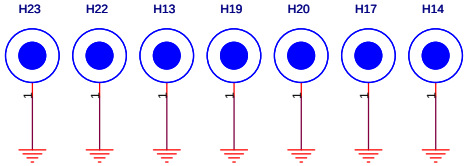
SW9 - 34.49Q02.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001









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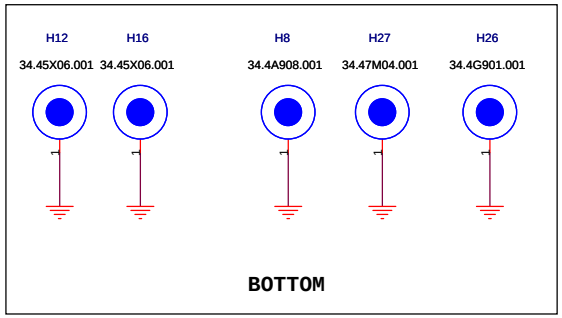
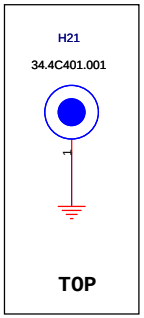
H27: 34.47M04.001
H26: 34.4G901.001
H21: 34.4C401.001





<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thurman UMA

Size: A3 | Document Number: EMI&MISC | Rev: -1

Date: Thursday, November 22, 2007 | Sheet 45 of 46

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/11/24		1				EE
		2				EE
		3				EE
		4				EE
		5				EE
		6				EE
		7				EE
		8				EE
		9				EE
		10				EE
		11				EE
		12				EE
		13				EE
		14				EE
		15				EE
		16				Power team
		17				EE
		18				EE
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		23				
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		25				
		26				

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thurman UMA*

Size: A3 | Document Number: *HISTORY* | Rev: -1

Date: Wednesday, November 07, 2007 | Sheet 46 of 46