DATA SHEET

SPIF225A

USB and eSATA to Serial-ATA Bridge

JAN. 25, 2007

Version 1.1

Table of Contents

PAGE

USB 2.0 TO SERIAL-ATA HOST BRIDGE

1.GENERAL DESCRIPTION

The SunplusIT SPIF225A is a single-chip solution for USB to Serial-ATA(SATA) host bridge. It has a USB high-speed device port and a SATA 1.5G host port. It received standard Mass Storage Device Class (MSDC) SCSI command from USB host and translate into ATA/ATAPI command to SATA device. The maximum throughput can goes up to 30MB/sec.

2.FEATURES

SPIF225A has many special features that can provide our customers to make their end products unique. Some of these features require an I2C interface serial Non Volatile Memory (NVM) while some of them require specify driver or new mask ROM.

2.1. Overall Feature

- Data transfer throughput at 30MB/sec.
- Available in 64-pin TQFP package with ePad[1].
- Embedded Memory, USB PHY and SATA PHY have isolated BIST.
- Full scan for high production test coverage
- Support multi GPIOs for customize.
- Support Pass Through ATA command with LBA48 bit and Port Multiplier feature
- Support multi-I2C device. [2]
- Support Serial ATA Port Multiplier
- Pass Microsoft™ WHQL certification.
- Support Window 98/ME/2K/XP, Linux , Mac 10 OS platform

2.2. USB Features

- Compliant with USB 2.0 specifications and pass USB certification.
- Support USB high speed (480Mbps) and full speed transfer rate (12Mbps).
- Support Mass Storage Device Class bulk only transfer.
- Support USB vendor command (Control Endpoint) and SCSI vendor command.
- Support USB host controller for UHCI, OHCI, EHCI mode.

2.3. Serial-ATA Features

- Compliant with Serial-ATA 1.0A specifications
- Support Serial-ATA generation 1 transfer rate of 1.5Gb/s
- Support spread spectrum in receiver
- Support Serial-ATA power saving mode: Partial and Slumber mode.
- Support SerialATA PHY Hi-Z enable and disable feature.[3]
- Support SerialATA Port Multiplier with command base.

2.4. Application Examples

- USB External HDD, Enclosures, Mobil Rack, Docking Station

3.REFERENCES

For more details information about USB and SATA technology, please refer to the following industry specifications:

- Serial-ATA / High Speed Serialized ATA Attachment specification, Revision 1.0A.
- Universal Serial Bus Specification Revision 2.0.
- Serial ATA Port Multiplier specification, Reversion 1.2.

[1] For e-Pad of SPIF225A, please always connect e-Pad to the ground of application board.

[2] About I2C device program guide, please check with your agent to get the relative document.

[3] Serial ATA Hi-Z mode could be only used SATA I 1.5GHZ.

4.BLOCK DIAGRAM

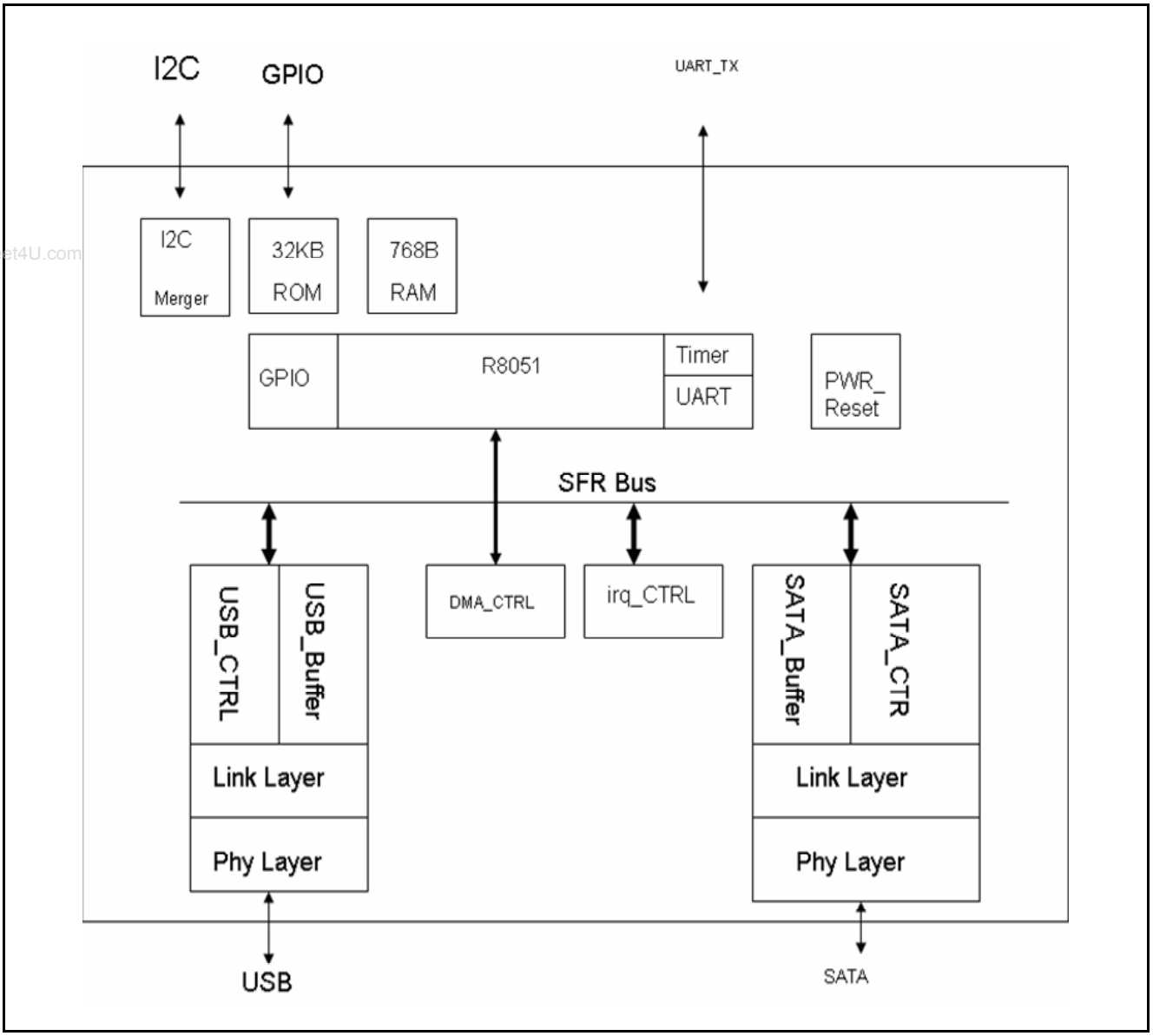


Fig 4-1: SPIF225A Functional Blocks Diagram

5.SIGNAL DESCRIPTIONS

5.1. Pin Descriptions

Table 5-1: Pin Types

Pin Type	Pin Description
I/O	Bi-directional Pin
I	Input Pin
O	Output Pin
T	Tri-state Output Pin
A	Analog pin
USB	USB D+ D-
SATA	SATA TX+ TX- RX+ RX-

5.2. Pin Diagram

5.2.1. TQFP64

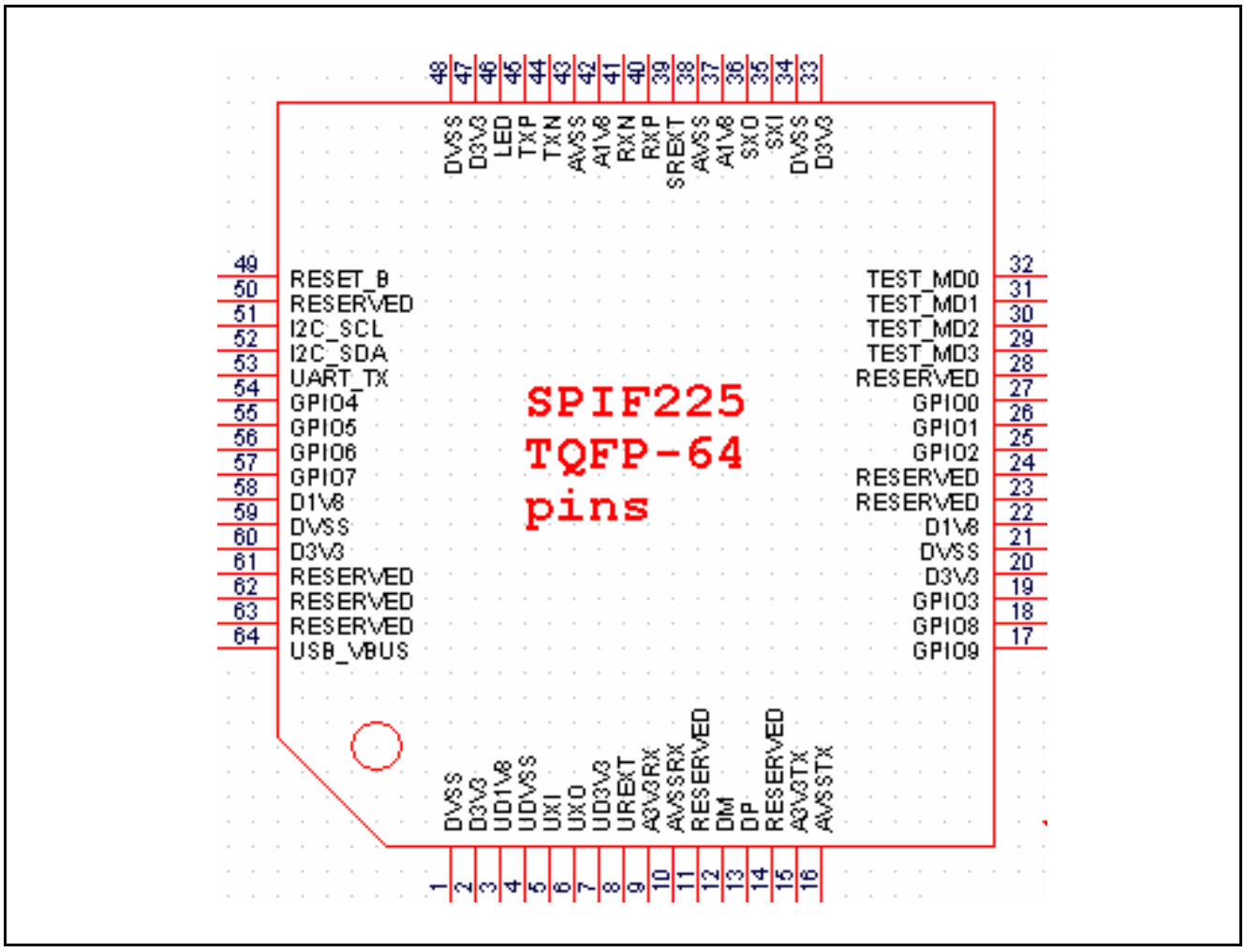
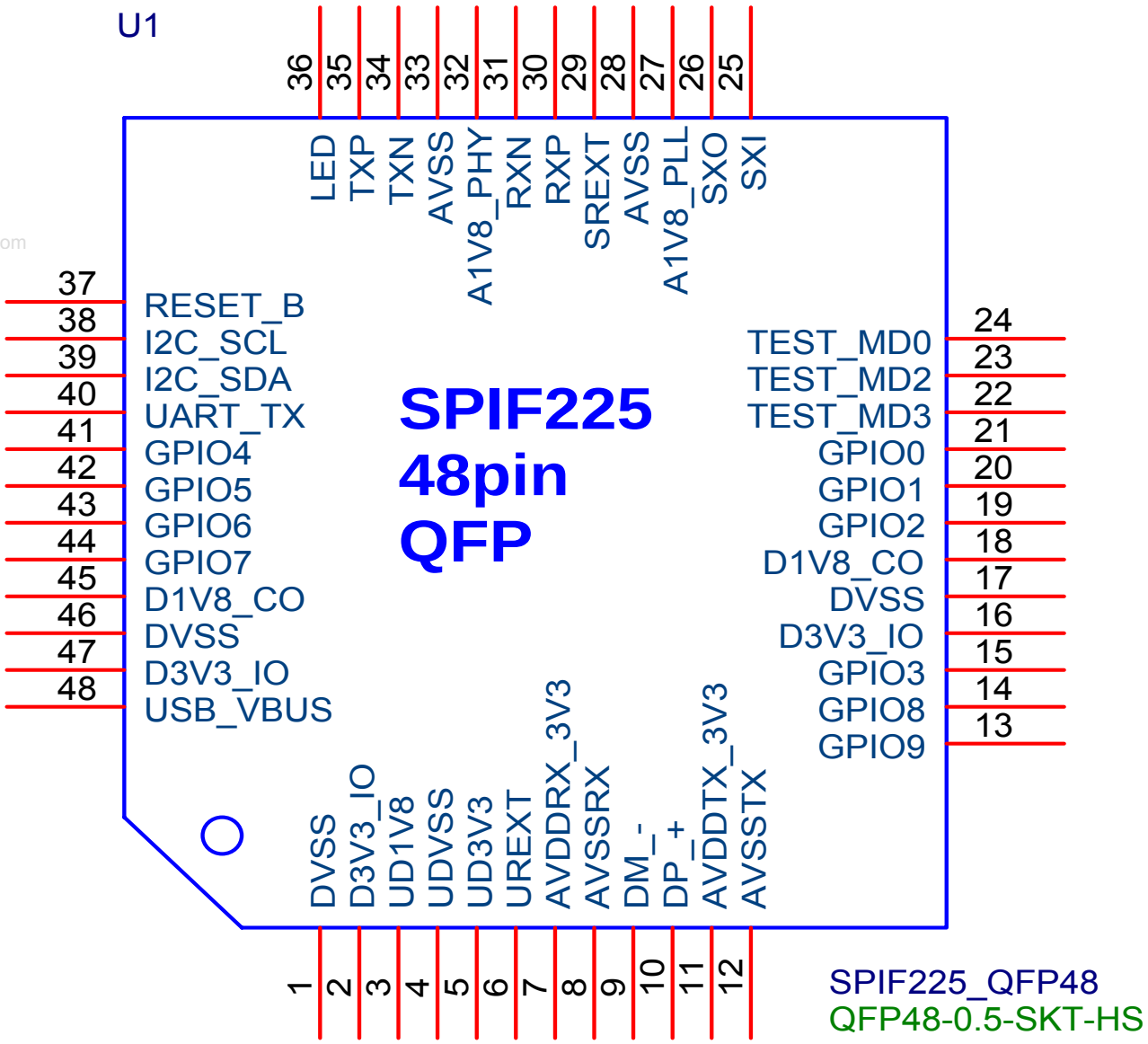


Figure 5-1 SPIF225A Pin Diagram

5.2.2. LQFP48



5.3. Pin Listing

5.3.1. TQFP 64:

Table 5-2: SPIF225A Pin Listing

Pin	Mnemonic	Type	Pin Description
1	DVSS	GND	Digital Ground
2	D3V3	PWR	Digital 3.3V Power
3	UD1V8	PWR	USB Digital 1.8V Power
4	UDVSS	GND	USB Digital Ground
5	UXI	I	USB Crystal Oscillator Input / External Clock Input
6	UXO	O	USB Crystal Oscillator Output
7	UD3V3	PWR	USB Crystal 3.3V Power
8	UREXT	A	USB External Resistor 12Kohm
9	A3V3RX	PWR	USB Analog Ground for PHY RX
10	AVSSRX	GND	USB Analog Power for PHY RX
11	Reserve		No connection
12	DM	USB	USB High Speed D-
13	DP	USB	USB High Speed D+
14	Reserve	USB	No connection
15	A3V3TX	PWR	USB Analog power for PHY TX
16	AVSSTX	GND	USB Analog Ground for PHY TX
17	GPIO9		General Purpose IO 9
18	GPIO8		General Purpose IO 8
19	GPIO3	I	SATA PHY Hi-Z control 0 : SATA PHY Hi-Z 1: SATA PHY enable
20	D3V3	PWR	Digital 3.3V Power
21	DVSS	GND	Digital Ground
22	D1V8	PWR	Digital 1.8V Power
23	Reserve		No connect
24	Reserve		No connect
25	GPIO2	I/O	General purpose IO 2
26	GPIO1	I/O	General purpose IO 1
27	GPIO0	I	General purpose IO 0
28	Reserve		No connect
29	TEST_MD3	I	Test Mode Selection Bit 3
30	TEST_MD2	I	Test Mode Selection Bit 2
31	TEST_MD1	I	Test Mode Selection Bit 1
32	TEST_MD0	I	Test Mode Selection Bit 0
33	D3V3	PWR	Digital 3.3V Power
34	DVSS	GND	Digital Ground
35	SXI	I	SATA Crystal Oscillator Input / External Clock Input
36	SXO	O	SATA Crystal Oscillator Output
37	A1V8	PWR	SATA 1.8V Analog Power
38	AVSS	GND	SATA Analog Ground
39	SREXT	A	SATA External Reference Resistor Input
40	RXP	SATA	SATA Differential Receive +ve
41	RXN	SATA	SATA Differential Receive –ve
42	A1V8	PWR	SATA 1.8V Analog Power

Pin	Mnemonic	Type	Pin Description
43	AVSS	GND	SATA Analog Ground
44	TXN	SATA	SATA Differential Transmit –ve
45	TXP	SATA	SATA Differential Transmit +ve
46	LED	T	HDD active LED output
47	D3V3	PWR	Digital 3.3V Power
48	DVSS	GND	Digital Ground
49	RESET_B	I	Low Active Reset
50	Reserve		No connect
51	I2C_SCL	I/O	I2C Clock
52	I2C_SDA	I/O	I2C Data
53	UART_TX	O	UART TX
54	GPIO4	I/O	General purpose 4
55	GPIO5	I/O	General purpose 5
56	GPIO6	I/O	General purpose 6
57	GPIO7	I/O	General purpose 7
58	D1V8	PWR	Digital 1.8V Power
59	DVSS	GND	Digital Ground
60	D3V3	PWR	Digital 3.3V Power
61	Reserve		Reserve
62	Reserve		Reserve
63	Reserve		Reserve
64	USB_VBUS	I	USB VBUS

5.3.2. LQFP48:

Pin	Mnemonic	Type	Pin Description
1	DVSS	GND	Digital Ground
2	D3V3_IO	PWR	3.3V Power
3	UD1V8	PWR	USB Digital 1.8V Power
4	UDVSS	GND	USB Digital Ground
5	UD3V3	PWR	USB Crystal 3.3V Power
6	UREXT	A	USB External Resistor 12Kohm
7	AVDDRX_3V3	Power	USB Analog Power for PHY RX
8	AVSSRX	GND	USB Analog Ground for PHY RX
9	DM	USB	USB High Speed D-
10	DP	USB	USB High Speed D+
11	AVDDTX_3V3	PWR	USB Analog power for PHY TX
12	AVSSTX	GND	USB Analog Ground for PHY TX
13	GPIO9		General Purpose IO 9
14	GPIO8		General Purpose IO 8
15	GPIO3	I	SATA PHY Hi-Z control 0 : SATA PHY Hi-Z 1: SATA PHY enable
16	D3V3-IO	PWR	Digital 3.3V Power
17	DVSS	GND	Digital Ground
18	D1V8_CO	PWR	Digital 1.8V Power
19	GPIO2	I/O	General purpose IO 2
20	GPIO1	I/O	General purpose IO 1

Pin	Mnemonic	Type	Pin Description
21	GPIO0	I	General purpose IO 0
22	TEST_MD3	I	Test Mode Selection Bit 3
23	TEST_MD2	I	Test Mode Selection Bit 2
24	TEST_MD0	I	Test Mode Selection Bit 0
25	SXI	I	SATA Crystal Oscillator Input / External Clock Input
26	SXO	O	SATA Crystal Oscillator Output
27	A1V8_PLL	PWR	SATA 1.8V Analog Power
28	AVSS	GND	SATA Analog Ground
29	SREXT	I	SATA External Reference Resistor Input
30	RXP	SATA	SATA Differential Receive +ve
31	RXN	SATA	SATA Differential Receive –ve
32	A1V8_PHY	PWR	SATA 1.8V Analog Power
33	AVSS	GND	SATA Analog Ground
34	TXN	SATA	SATA Differential Transmit –ve
35	TXP	SATA	SATA Differential Transmit +ve
36	LED	T	HDD active LED output
37	RESET_B	I	Low Active Reset
38	I2C_SCL	I/O	I2C Clock
39	I2C_SDA	I/O	I2C Data
40	UART_TX	O	UART TX
41	GPIO4	I/O	General purpose 4
42	GPIO5	I/O	General purpose 5
43	GPIO6	I/O	General purpose 6
44	GPIO7	I/O	General purpose 7
45	D1V8_CO	PWR	Digital 1.8V Power
46	DVSS	GND	Digital Ground
47	D3V3_IO	PWR	Digital 3.3V Power
48	USB_VBUS	I	USB VBUS

6. FUNCTIONAL DESCRIPTIONS

6.1. Power Management

SPIF225A support both USB and SATA power management mechanism.

If SATA device initial a partial/slumber request, SPIF225A will decide whether accept or not depend on current USB status. If USB host is not access SATA device, SPIF225A might let SATA device goes into partial/slumber mode and stop its SATA connection.

If USB host try to access SATA device when SATA device is power down, SPIF225A will issue a comm reset OOB signal to wake up device and re-establish the SATA connection.

If USB host suspend SPIF225A, SPIF225A will send partial/slumber request to power down SATA device before goes into suspend. SPIF225A will also wait up SATA device when it is wake up by the USB host.

6.1.1. USB Suspend Power Management Mode

USB host will periodically sending SOF packet in constant timing interval. If device haven't received any USB bus activity for more than 3ms, it will have to try to pull up D+ through 1.5K Ohm resistor to detect whether host want to reset or suspend the device. If suspend, device will have to power down as much logic as possible because device must not consume more than 500μA from VBUS during suspend.
When host try to wake up device drive a Resume-K (DM high, DP low) to wake up device. If device try to initialize the connection, it will also drive a Resume-K to host.

6.1.2. SATA Partial Power Management Mode

Partial mode may be initiated by software through the SMisc register (bit 0). By setting the bit, the software causes PMREQ_P primitives (Power Management REQuest – Partial) to be sent to the Serial ATA device, which will respond with either a PMACK or PMNAK. If a PMACK is received the Partial mode is entered; A PMNAK is ignored; the request remains asserted.

The Serial ATA device may initiate partial mode. This is indicated by the reception of PMREQ_P primitives from the device. Software enables the acknowledgement of this request by setting the IPM value in the SControl register to '00x1' If enabled, a PMACK will be sent to the device; if not enabled, a PMNAK will be sent. When the request is received and its acknowledgement is enabled, Partial mode is entered.

Partial mode status is reported in both the SStatus register ('0010' in the IPM field) and the SMisc register (bit 4).

Partial mode is cleared by setting the ComWake bit in the Smisc register. This will send a COMWAKE signal to the device through the Serial ATA link to initiate a Partial to On sequence. Partial mode can also be cleared through receipt of OOB signals from the device.

6.1.3. SATA Slumber Power Management Mode

Slumber mode may be initiated by software through the SMisc register (bit 1). By setting the bit, software causes PMREQ_S primitives to be sent to the Serial ATA device, which will respond with either a PMACK or PMNAK. If a PMACK is received the Slumber mode is entered. A PMNAK is ignored; the request remains asserted.

The Serial ATA device may initiate slumber mode. This is indicated by the reception of PMREQ_S primitives. Software enables the acknowledgement of this request by setting the IPM value in the SControl register to '001x'. If enabled, a PMACK will be sent to the device; if not enabled, a PMNAK will be sent. When the request is received and its acknowledgement is enabled, Slumber mode is entered.

Slumber mode status is reported in both the SStatus register ('0110' in the IPM field) and the SMisc register (bit 5).

Slumber mode is cleared by setting the ComWake bit in the Smisc register. This will send a COMWAKE signal to the device through the Serial ATA link to initiate a Slumber to On sequence. Slumber mode can also be cleared through receipt of OOB signals from the device.

6.2. Hot-Plug Support

SPIF225A support both SATA and USB hot-plug feature.

6.2.1. USB Hot-Plug Support

USB device uses VBUS status to detect if it is plug into a host. When it does, it will raise it D+ and host will detect device present and start building up communication channel. Device also uses VBUS falling to detect if it has been unplug from host and will reset all its status to wait for another plug-in action.

For full-speed device, it will raise pull up resistor at D+ to create an IDLE-J situation. If the device is unplugged or want to create software disconnect situation by take out pull up resistor, host will detect D+D- is changing from IDLE-J to SE0 and recognize as device unplugged.

For high-speed device, host will keep sending SOF packet in idle situation. Because both host and device has 45ohm pull down termination resistor, the voltage level is normal. If device unplugged or want to create software disconnect situation by take out its pull down resistor, the voltage level is twice as normal voltage because equivalent resistor is increased.

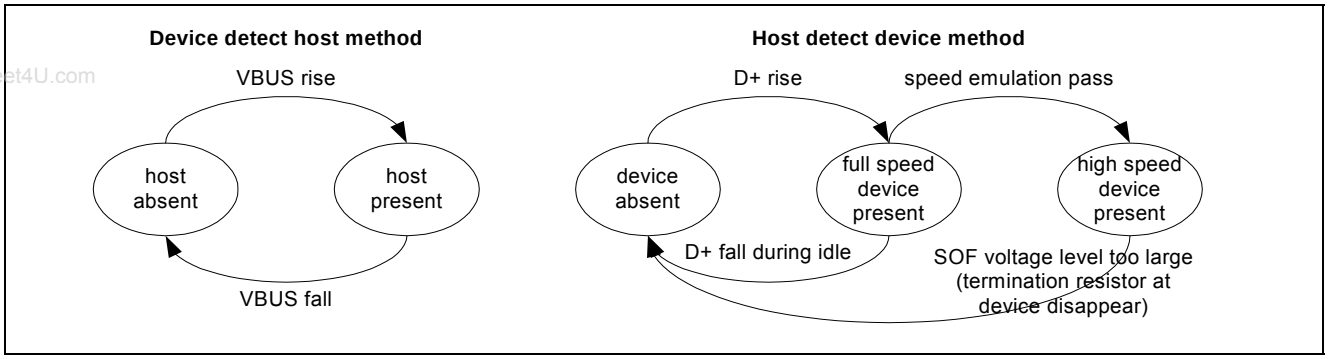


Fig 6-1: USB Hot Plug Mechanism

6.2.2. SATA Hot-Plug Support

SATA use differential signal squelch level to detect if host/device is present. Host will keep sending (can be disable to reduce power consumption) OOB signal to let device detect its present. If a device received host OOB signal, it will also return OOB signal to let host detect its present and communication channel is established.

If any site is unplug or create a software disconnect situation by stop it transmitter from sending differential signal, the other site will sense the differential signal disappear and know the other site is unplugged.

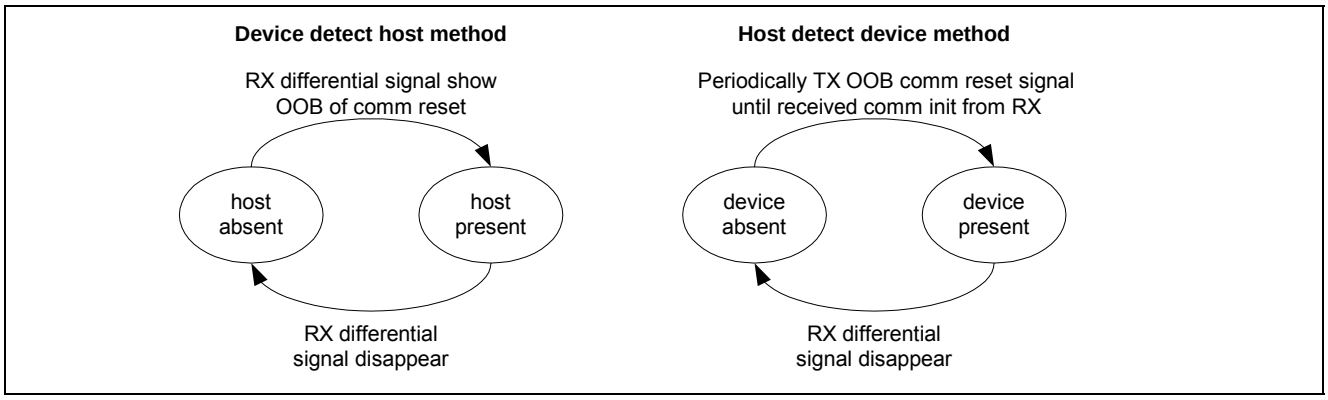


Fig 6-2: SATA Hot Plug Mechanism

6.2.3. SPIF225A Hot-Plug Support

SPIF216A can perform software USB disconnect function by taking out 45ohm termination in high speed or taking out 1.5K pull up resistor on DP in full speed. All SATA device connection status will all reflect on USB site. For example, if SPIF216A is plugged into USB host without SATA device connection. SPIF216 will perform USB software disconnection and users will not see any USB device plugged in information. If SATA device is plugged in later, SPIF216 will restart its USB connection procedure and users will see a new USB device plugged in. If SATA device is suddenly unplugged, SPIF216A will also perform USB software disconnection to show users an USB device is unplugged.

7.ELECTRICAL SPECIFICATIONS

7.1. Power Requirement

7-1: Total Power Dissipation (Typical corner, T_A =25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I_{IO}	Absolute digital I/O pad power supply	3.3V	1.0	4.5	6.0	mA
I_{CORE}	Absolute digital core power supply	1.8V	8-	18	25	mA
I_{AUSB}	Absolute analog power supply for USB PHY	3.3V	0	25-	30	mA
I_{ASATA}	Absolute analog power supply for SATA PHY	1.8V	64-	68	80	mA

Note: Max total power < 432mW

7.2. Absolute Maximum Ratings

Table 7-2: Absolute Maximum Ratings (Typical corner, 25℃)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{IO}	Absolute digital I/O pad power supply voltage	3.0	3.3-	3.6	V
V_{CORE}	Absolute digital power supply	1.71	1.8-	1.89	V
V_{AUSB}	Absolute analog power supply voltage for USB PHY	3.0	3.3	3.6	V
V_{ASATA}	Absolute analog power supply voltage for SATA PHY	1.71	1.8	1.89	V
T_{STR}	Absolute storage temperature	-40		125	℃

7.3. Recommended/Typical Operating Conditions

Table 7-3: Recommended/Typical Operating Conditions

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CORE}	Operating digital power supply voltage	1.71	1.8	1.89	V
V_{IO}	Operating digital I/O pad supply voltage	3.0	3.3	3.6	V
V_{AUSB}	Operating analog power supply voltage for USB PHY	3.0	3.3	3.6	V
V_{ASATA}	Operating analog power supply voltage for SATA PHY	1.71	1.8	1.89	V
T_{STR}	Operating temperature	0	25	70	℃

7.4. DC Characteristics

Table 7-4: DC Characteristics

(Testing condition: V_{CORE} =1.8V V_{AUSB}, = 3.3V, V_{ASATA} = 1.8V T_a =25^{0}C, Unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{IL}	Input low voltage		-0.3	-	0.8	V
V_{IH}	Input high voltage		2.0	-	3.9	V
V_{TH}	Threshold point		1.45	1.59	1.77	V
V_T^+	Schmitt trig. Low to High threshold point		1.47	1.50	1.50	V
V_T^-	Schmitt trig. high to low threshold point		0.90	0.94	0.96	V
I_I	Input leakage current		-	-	±10	µA
I_{OZ}	Tri-state output leakage current		-	-	±10	µA

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R_{PU}	Pull-up resistor		46	70	114	KΩ
R_{PD}	Pull-down resistor		30	58	129	KΩ
V_{OL}	Output low voltage	I_{OL} (min)	-	-	0.4	V
V_{OH}	Output high voltage	I_{OH} (min)	2.4	-	-	V
I_{OL}	Low level output current					mA
I_{OH}	High level output current					mA

Note: Above information are TSMC standard IO PADs specifications. SPIF225A haven't decided which type of IOs to be used.

7.5. USB Interface DC Characteristics

Table 7-5: USB DC Characteristics (Typical corner, 25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Input Levels for Full-Speed						
V_{IH}	Single Ended High (driven)		2.0	-		V
V_{IHZ}	Single Ended High (floating)		2.7	-	3.6	V
V_{IL}	Single Ended Low		-	-	0.8	V
V_{DI}	Differential input | (D+) - (D-) | sensitivity		0.2	-	-	V
V_{CM}	Differential common mode range		0.8	-	2.5	V
Input Levels for High-Speed						
V_{HSSQ}	HS differential squelch threshold		100	-	150	mV
V_{HSDSC}	HS differential disconnect threshold		525	-	625	mV
V_{HSCM}	HS data common mode voltage range		-50	-	500	mV
Output Levels for Full-Speed						
V_{OL}	Low		0.0	-	0.3	V
V_{OH}	High		2.8	-	3.6	V
V_{OSE1}	SE1		0.8	-	-	V
V_{CRS}	Signal crossover voltage		1.3	-	2.0	V
Output Levels for High-Speed						
V_{HSOI}	HS Idle level		-10	-	10	mV
V_{HSOH}	HS data signaling high		360	-	440	mV
V_{HSOL}	HS data signaling low		-10	-	10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		-900	-	-500	mV

Note: Above information same as USB specification Rev.2.0 Chapter 7.3.2

7.6. USB Interface Timing Specification

Table 7-6: USB Electrical Characteristics (Typical corner, 3.3V/1.8V, 25^0)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Full Speed Driver Characteristics						
T_{FR}	Rise time		4.0	-	20	ns
T_{FF}	Fall time		4.0	-	20	ns

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
T_{FRFM}	Differential rise fall time matching		90	-	111.11	%
$T_{FDRATHS}$	Full Speed data rate (HS capable)		11.994	-	12.006	Mbps
High Speed Driver Characteristics						
T_{HSR}	Rise time		500	-	-	ps
T_{HSF}	Fall time		500	-	-	ps
T_{HSDRAT}	High Speed data rate		479.760	-	480.240	Mbps

Note: Above information same as USB specification Rev.2.0 Chapter 7.3.2

7.7. USB Reference Clock Input Requirements

Table 7-7: USB Reference Clock Input Requirements (Typical corner, 3.3V/1.8V, 25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R_{UEXT}	REXT		-	12.47	-	Kohm
F_{UREF}	REFCLK frequency	12MHz	-500	-	+500	ppm
T_{UREFRF}	REFCLK rise and fall time	20% ~ 80%	-	-	4.0	ns
T_{UREFD}	REFCLK duty cycle	20% ~ 80%	40	-	60	%

7.8. SATA Interface DC Characteristics

Table 7-8: SATA DC Characteristics (Typical corner, 1.8V, 25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CM,DD}$	Common mode voltage	DC to DC	200	250	450	mV
$V_{CM,AD}$	Common mode voltage	AC to DC	0	-	2.0	mV
$V_{CM,DA}$	Common mode voltage	DC to AC	0	-	2.0	mV
$V_{diff,tx}$	TX+/TX- differential peak-to-peak voltage swing		400	500	600	mV_{p-p}
$V_{diff,rx}$	RX+/RX- differential peak-to-peak voltage swing		325	400	600	mV_{p-p}
V_{sqth}	Squelch differential detector threshold		50	100	200	mV_{p-p}
$Z_{diff,tx}$	TX differential pair impedance	TDR differential mode 100ps edge 20~80%	85	100	115	Ohm
$Z_{diff,rx}$	RX differential pair impedance	TDR differential mode 100ps edge 20~80%	85	100	115	Ohm
$Z_{SE,tx}$	TX single-ended impedance	TDR 100ps edge 20~80%	40	-	-	Ohm
$Z_{SE,rx}$	RX single-ended impedance	TDR 100ps edge 20~80%	40	-	-	Ohm
$C_{ACcoupling}$	Coupling capacitance for AC coupled TX and RX pairs		-	-	12	nF

Note: Above information same as SATA specification Rev. 1.0a Chapter 6.6.1

7.9. SATA Interface Timing Specification

Table 7-9: SATA Electrical Characteristics (Typical corner, 1.8V, 25℃)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
T_{UI}	Unit interval (bit rate)	1.5G +- 350ppm	666.43	-	670.12	ps
T_{rise}	Rise time at transmitter	20% ~ 80%	0.15	0.3	0.41	UI
T_{fall}	Fall time at transmitter	20% ~ 80%	0.15	0.3	0.41	UI
T_{skew}	Differential skew at transmitter		-	-	20	ps
$F_{skew,DC}$	Tx DC clock frequency skew	Exclude 0~5000ppm SSC down spread AC modulation	-350	-	+350	ppm
$F_{skew,AC}$	Tx AC clock frequency skew		-5000	-	+0	ppm
$T_{comreset,H}$	COMRESET/COMINIT detector ON threshold spacing		304	320	336	ns
$T_{comreset,L}$	COMRESET/COMINIT detector OFF threshold spacing		175	-	525	ns
$T_{comwake,H}$	COMWAKE detector ON threshold spacing		101.3	106.7	112	ns
$T_{comwake,L}$	COMWAKE detector OFF threshold spacing		55	-	175	ns
$T_{comwake,S}$	COMWAKE transmit spacing		103.5	106.7	109.9	ns
UI_{OOB}	OOB data period		646.67	-	686.67	ps

Note: Above information same as SATA specification Rev. 1.0a Chapter 6.6.1

7.10. SATA Reference Clock Input Requirements

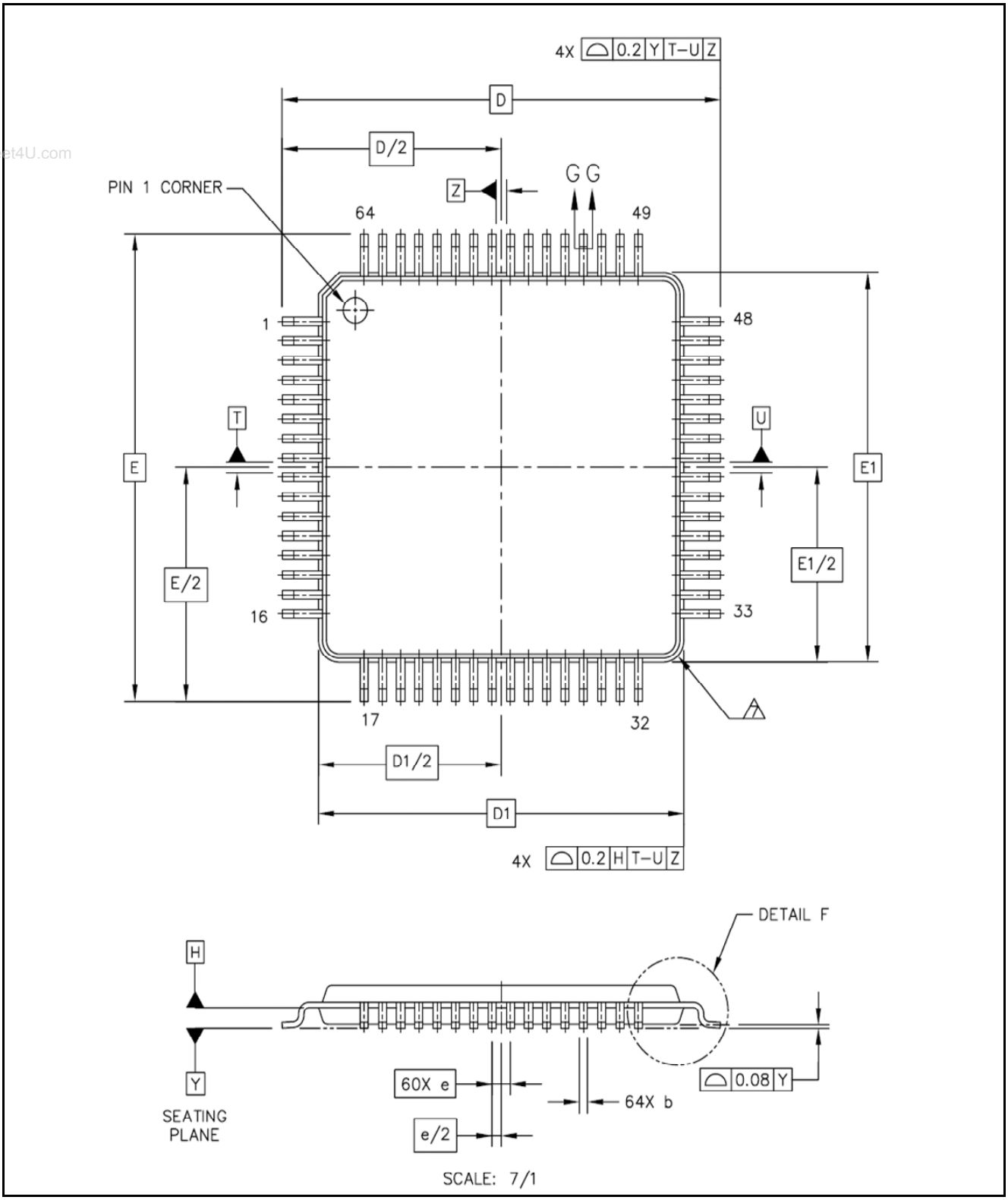
Table 7-10: CLKI Reference Clock Input Requirements (Typical corner, 1.8V, 25℃)

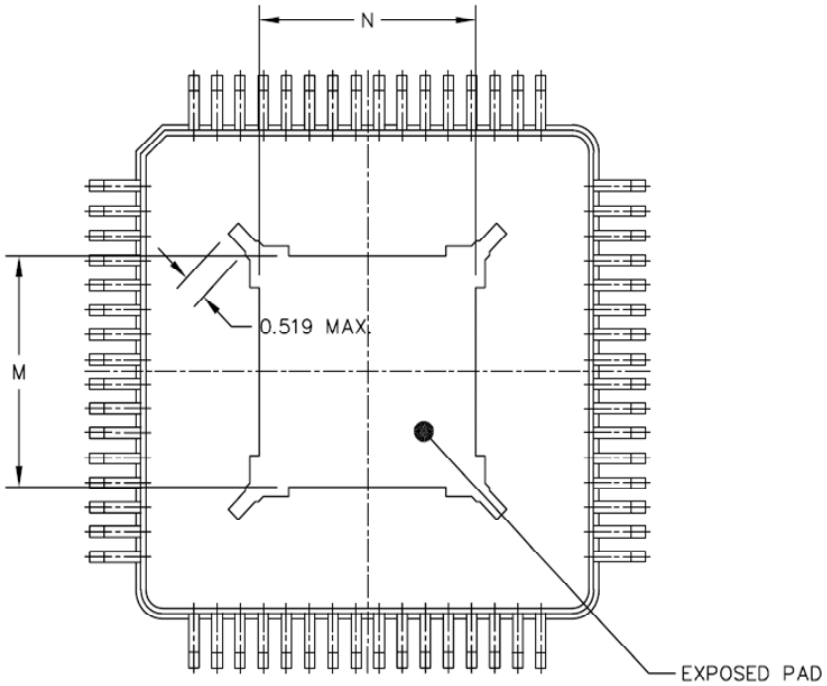
Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R_{SEXT}	Nominal frequency	REXT = 1k 1%	-	25	-	Ohm
F_{SREF}	CLKI frequency tolerance		-350	-	+350	ppm
T_{SREFRF}	Rise and fall time at CLKI	25MHz reference clock, 20% ~ 80%	-	-	4.0	ns
T_{SREFD}	CLKI duty cycle	20% ~ 80%	40	-	60	%

8.PACKAGE/PAD LOCATIONS

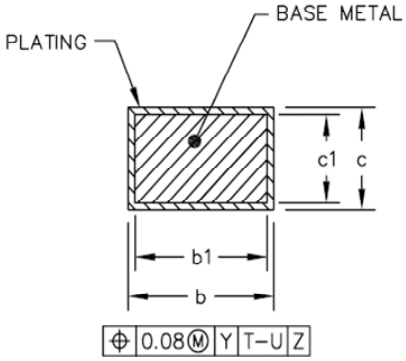
8.1. Package Information

8.1.1. TQFP64:

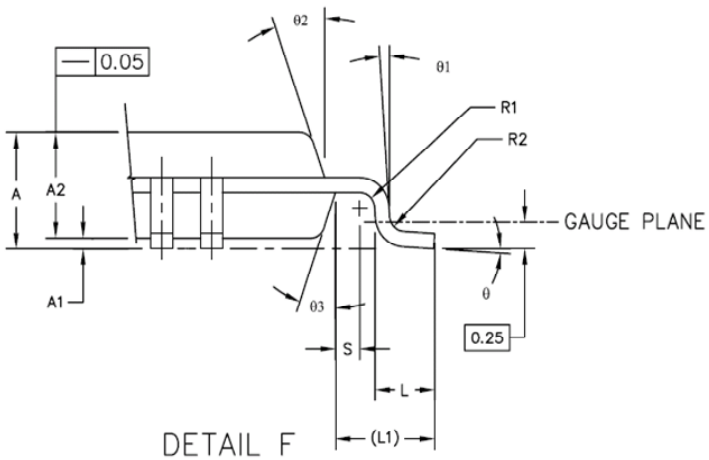




BOTTOM VIEW
SCALE: 7/1



SECTION G–G
SCALE: 100/1

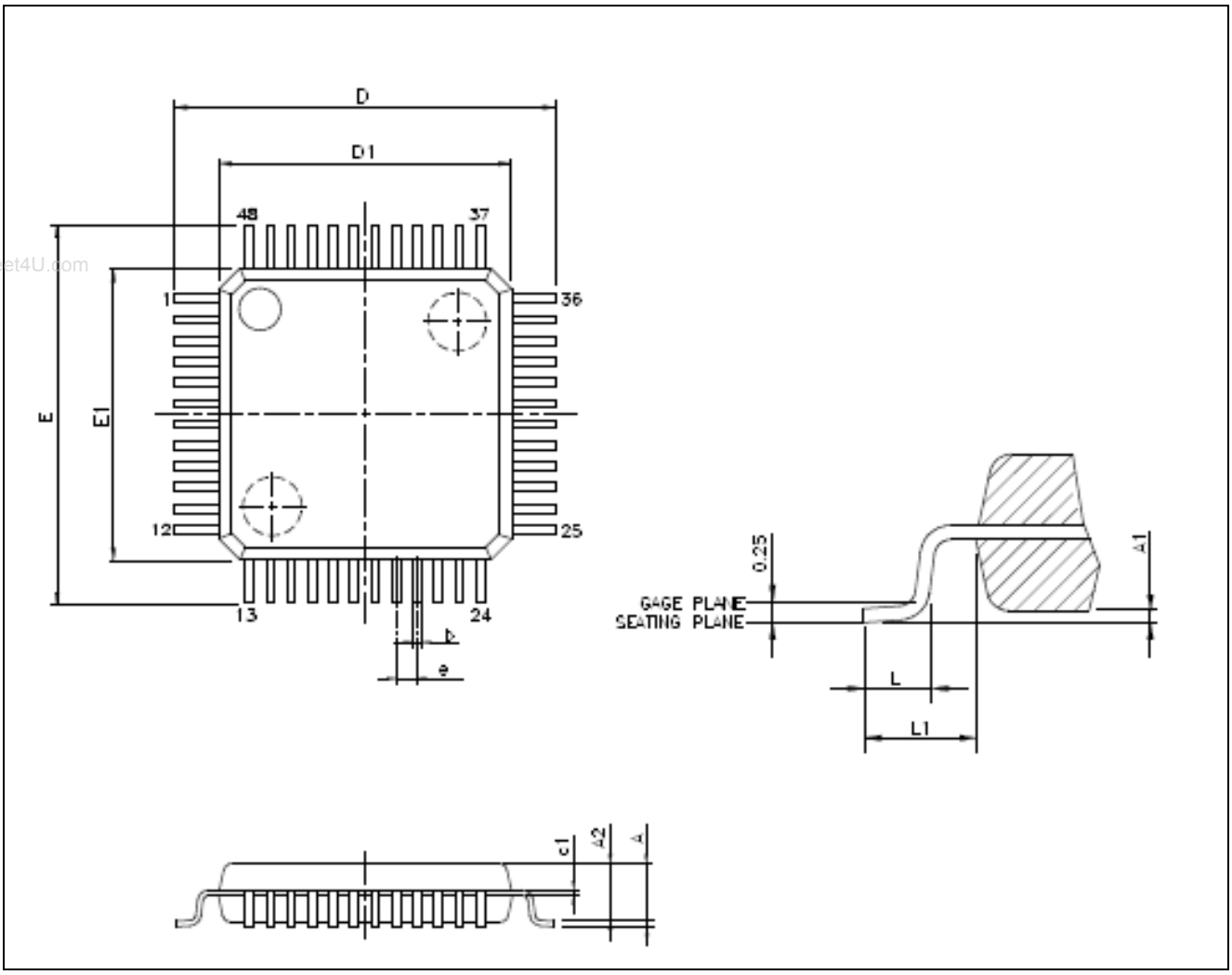


DETAIL F
SCALE: 15/1

DIM	MIN		MAX	DIM	MIN		MAX
A	---		1.2	L1		1 REF	
A1	0.05		0.15	R1	0.08		---
A2	0.95	1	1.05	R2	0.08		0.2
b	0.17	0.22	0.27	S	0.2		---
b1	0.17	0.2	0.23	θ	0°	3.5°	7°
c	0.09		0.2	θ1	0°		---
c1	0.09		0.16	θ2	11°	12°	13°
D		12 BSC		θ3	11°	12°	13°
D1		10 BSC		M	4.58	4.68	4.78
e		0.5 BSC		N	4.58	4.68	4.78
E		12 BSC					
E1		10 BSC					
L	0.45	0.6	0.75				

Fig 8-1: SPIF225A in TQFP-64 package
◎E-Pad dimension could be changed without notice.

8.1.2. LQFP48:



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1.JEDEC OUTLINE:MS-026 BBC

2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

8.2. Ordering Information

Product Number	Package Type
SPIF225A - HF021	Green Package form – TQFP 64*
SPIF225A - HL231	Green Package form – LQFP 48

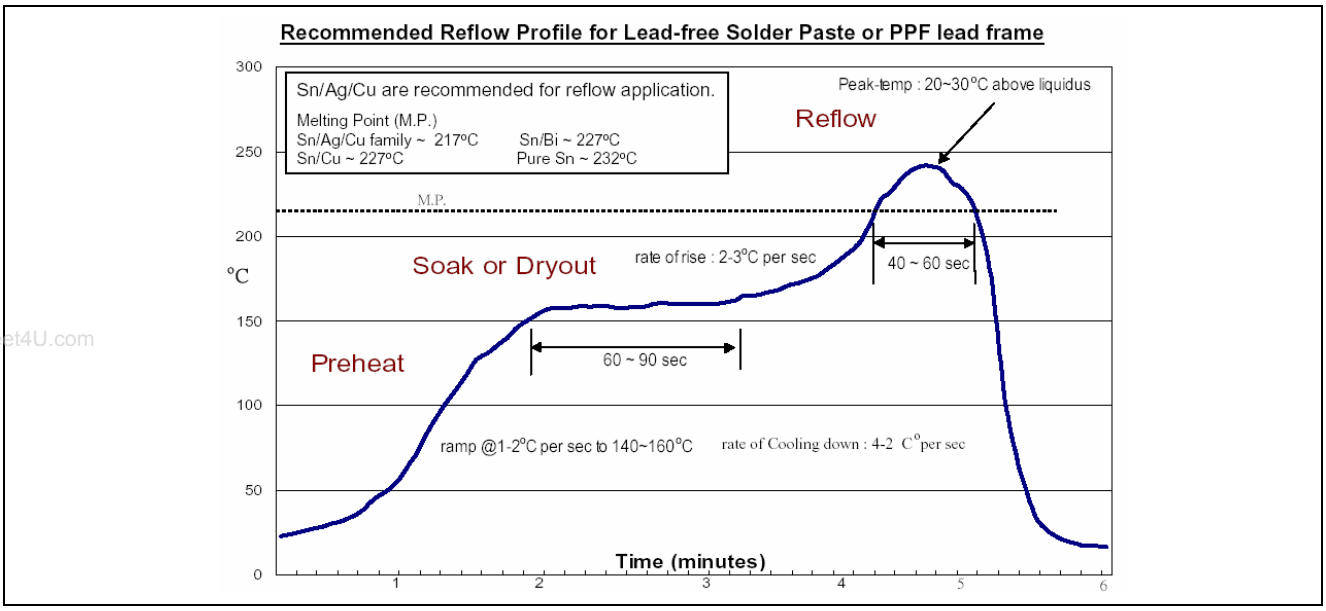
8.3. Storage Condition and Period for Package

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
TQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes
LQFP	LEVEL 3	255 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JESD22-A112, or the "CAUTION Note" on dry pack bag.

8.4. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of SUNPLUSIT leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF(Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.



9.DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by Sunplus Innovation Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. SUNPLUSIT makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, SUNPLUSIT MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. SUNPLUSIT reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by SUNPLUSIT for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

10. REVISION HISTORY

Date	Revision #	Description	Page
JUL. 11, 2006	0.1	Original	19
OCT, 12, 2006	1.0	Modify 1.8V power range	11
JAN, 25, 2007	1.1	Add LQFP48 package pin assignment, package information, and order information	9,10,20,21