Table 24. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
M30	VCC	Power/Other	
N1	PWRGOOD	Power/Other	Input
N2	IGNNE#	Asynch CMOS	Input
N3	VSS	Power/Other	
N4	RESERVED		
N5	RESERVED		
N6	VSS	Power/Other	
N7	VSS	Power/Other	
N8	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VCC	Power/Other	
N25	VCC	Power/Other	
N26	VCC	Power/Other	
N27	VCC	Power/Other	
N28	VCC	Power/Other	
N29	VCC	Power/Other	
N30	VCC	Power/Other	
P1	TESTHI11	Power/Other	Input
P2	SMI#	Asynch CMOS	Input
P3	INIT#	Asynch CMOS	Input
P4	VSS	Power/Other	
P5	RESERVED		
P6	A04#	Source Synch	Input/Output
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P23	VSS	Power/Other	
P24	VSS	Power/Other	
P25	VSS	Power/Other	
P26	VSS	Power/Other	
P27	VSS	Power/Other	
P28	VSS	Power/Other	
P29	VSS	Power/Other	
P30	VSS	Power/Other	
R1	COMP3	Power/Other	Input
R2	VSS	Power/Other	
R3	FERR#/PBE#	Asynch CMOS	Output
R4	A08#	Source Synch	Input/Output
R5	VSS	Power/Other	
R6	ADSTB0#	Source Synch	Input/Output

Table 24. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
R7	VSS	Power/Other	
R8	VCC	Power/Other	
R23	VSS	Power/Other	
R24	VSS	Power/Other	
R25	VSS	Power/Other	
R26	VSS	Power/Other	
R27	VSS	Power/Other	
R28	VSS	Power/Other	
R29	VSS	Power/Other	
R30	VSS	Power/Other	
T1	COMP1	Power/Other	Input
T2	FC4	Power/Other	
T3	VSS	Power/Other	
T4	A11#	Source Synch	Input/Output
T5	A09#	Source Synch	Input/Output
T6	VSS	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
T23	VCC	Power/Other	
T24	VCC	Power/Other	
T25	VCC	Power/Other	
T26	VCC	Power/Other	
T27	VCC	Power/Other	
T28	VCC	Power/Other	
T29	VCC	Power/Other	
T30	VCC	Power/Other	
U1	FC28	Power/Other	
U2	FC29	Power/Other	
U3	FC30	Power/Other	
U4	A13#	Source Synch	Input/Output
U5	A12#	Source Synch	Input/Output
U6	A10#	Source Synch	Input/Output
U7	VSS	Power/Other	
U8	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VCC	Power/Other	
U25	VCC	Power/Other	
U26	VCC	Power/Other	
U27	VCC	Power/Other	