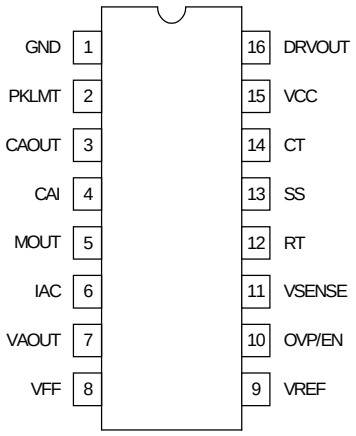
UCC2817, UCC2818, UCC3817, UCC3818
BiCMOS POWER FACTOR PREREGULATOR

SLUS395A - FEBRUARY 2000 - REVISED APRIL 2000

- Controls Boost Preregulator to Near-Unity Power Factor
- Limits Line Distortion
- World Wide Line Operation
- Over-Voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-Forward Line Regulation
- Leading Edge Modulation
- 150 μA Typical Start-Up Current
- Low Power BiCMOS Operation
- 12 V to 17 V Operation

SOIC-16, DIL-16 (TOP VIEW)
D, DW, and N PACKAGES



description

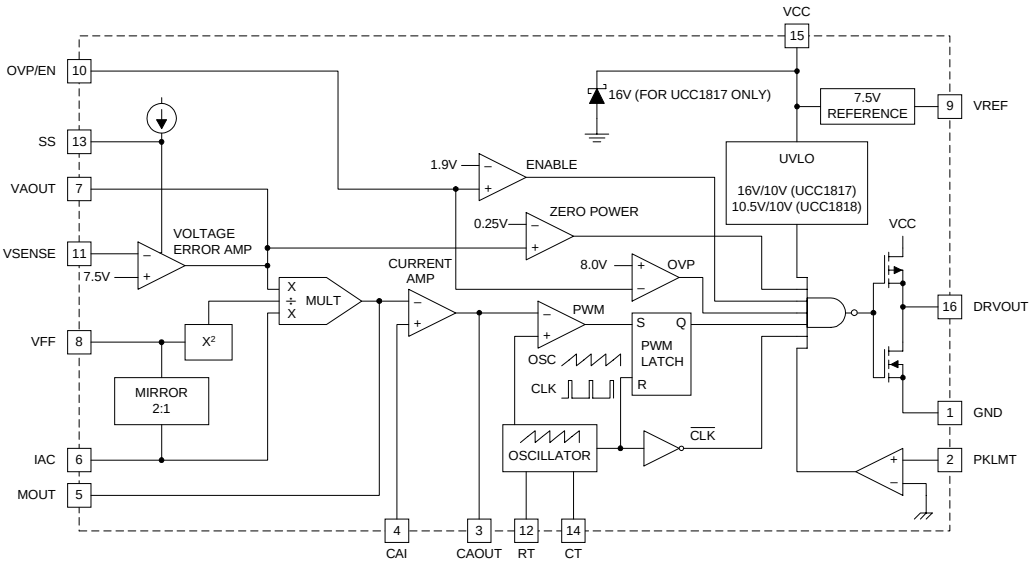
The UCC2817, UCC2818, UCC3817, and UCC3818 provide all the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the ac input line current waveform to correspond to that of the ac input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Unitrode's BiCMOS process, the UCC2817/UCC2818 offers new features such as lower start-up current, lower power dissipation, over-voltage protection, a shunt UVLO detect circuitry, a leading-edge modulation technique to reduce ripple current in the bulk capacitor and an improved, low-offset (±2 mV) current amplifier to reduce distortion at light load conditions.

UCC2817 offers an on-chip shunt regulator with low start-up current, suitable for applications utilizing a bootstrap supply. UCC2818 is intended for applications with a fixed supply (VCC).

Available in the 16-pin D, DW, and N packages.

block diagram



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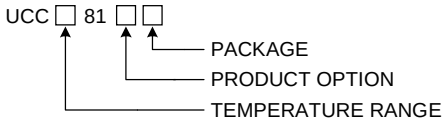
absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply Voltage VCC . . . . . 18 V
Gate Drive Current, Continuous . . . . . 0.2 A
Gate Drive Current, 50% Duty Cycle . . . . . 1 A
Input Voltage, CAI, MOUT . . . . . 8 V
Input Voltage, PKLMT . . . . . 5 V
Input Voltage, VSENSE, OVP/EN . . . . . 10 V
Input Current, RT, IAC, PKLMT . . . . . 10 mA
Maximum Negative Voltage, DRVOUT, PKLMT, MOUT . . . . . –0.5 V
Power Dissipation . . . . . 1 W

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ORDERING INFORMATON



electrical characteristics (unless otherwise noted), these specifications hold for T_A = 0°C to 70°C for the UCC3817 and T_A = –40°C to 85°C for the UCC2817, $T_A = T_J$. VCC = 12 V, R_T = 22 kΩ, C_T = 330 pF

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply current, off	VCC = (VCC turn-on threshold –0.3 V)		150	300	μA
Supply current, on	VCC = 12 V, No load on DRVOUT	2	4	6	mA
UVLO Section					
VCC turn-on threshold (UCCx817)		15.4	16	16.6	V
UVLO hysteresis (UCCx817)		5.8	6.3		V
Maximum shunt voltage (UCCx817)	I_{VCC} = 10 mA	15.4	17	17.5	V
VCC turn-on threshold (UCCx818)		9.7	10.2	10.8	V
VCC turn-off threshold (UCCx818)		9.4	9.7		V
UVLO hysteresis (UCCx818)		0.3	0.5		V
Voltage Amplifier Section					
Input voltage	T_A = 0°C to 70°C	7.387	7.5	7.613	V
	T_A = –40°C to 85°C	7.369	7.5	7.631	V
V_{SENSE} bias current	VSENSE = VREF, VAOUT = 2.5 V		50	200	nA
Open loop gain	VAOUT = 2 V to 5 V	50	90		dB
V_{OUT} high	I_L = –150 μA	5.3	5.5	5.6	V
V_{OUT} low	I_L = 150 μA	0	50	150	mV
Over Voltage Protection and Enable Section					
Over voltage reference		VREF 0.48	VREF 0.50	VREF 0.52	V
Hysteresis			500		mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.1	0.2		V

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PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Current Amplifier Section							
Input offset voltage	V_{CM} = 0 V,	V_{CAOUT} = 3 V		-2	0	2	mV
Input bias current	V_{CM} = 0 V,	V_{CAOUT} = 3 V			-50	-100	nA
Input offset current	V_{CM} = 0 V,	V_{CAOUT} = 3 V			25	100	nA
Open loop gain	V_{CM} = 0 V,	V_{CAOUT} = 2 V to 5 V			90		dB
CMRR	V_{CM} = 0 V to 1.5 V,	V_{CAOUT} = 3 V		60	80		dB
V_{OUT} high	I_L = -120 µA			5.6	6.3	6.8	V
V_{OUT} low	I_L = 1 mA			0.1	0.2	0.5	V
Gain bandwidth product	see note 1				2.5		MHz
Voltage Reference Section							
Input voltage	T_A = 0°C to 70°C			7.387	7.5	7.613	V
	T_A = -40°C to 85°C			7.369	7.5	7.631	V
Load regulation	I_{REF} = 1 mA to 2 mA			0	3	10	mV
Line regulation	VCC = 10.8 V to 15 V see note 2			0	20	50	mV
Short circuit current	V_{REF} = 0 V			-20	-25		mA
Oscillator Section							
Initial accuracy	T_A = 25°C			85	100	115	kHz
Voltage stability	VCC = 10.8 V to 15 V			-1		1	%
Total variation	Line, Temp			80		120	kHz
Ramp peak voltage				4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)				3.5	4	4.5	V
Peak Current Limit Section							
PKLMT reference voltage				-15		15	mV
PKLMT propogation delay				150	350	500	ns
Multiplier Section							
High line, low power	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 1.25 V	0	-6	-20	µA
High line, high power	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 5 V	-75	-90	-110	µA
Low line, low power	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 1.25 V	-10	-19	-50	µA
Low line, high power	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 5 V	-260	-300	-360	µA
IAC limited	I_{AC} = 150 µA,	V_{FF} = 1.3 V,	VAOUT = 5 V	-250	-300	-400	µA
Gain constant (K)	I_{AC} = 300 µA,	V_{FF} = 3 V,	VAOUT = 2.5 V	0.5	1	1.5	1/V
Zero current	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 0.25 V		0	-2	µA
	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 0.25 V		0	-2	µA
	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 0.5 V		0	-3	µA
Power limit	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 5 V	-360	-420	-500	µW
Feed-Forward Section							
VFF output current	I_{AC} = 300 µA			-140	-150	-160	µA
Soft Start Section							
SS charge current				-6	-10	-16	µA

NOTE 1: Ensured by design, not 100% tested.

NOTE 2: Reference variation for V_{CC} < 10.8 V is shown in Figure 8.

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver Section					
Pull up resistance	I_O = –100 mA		7	12	Ω
Pull down resistance	I_O = 100 mA		3	10	Ω
Output rise time	C_L = 1 nF, R_L = 10 Ω		25	50	ns
Output fall time	C_L = 1 nF, R_L = 10 Ω		10	50	ns
Maximum duty cycle		93	95	100	%
Zero Power Section					
Zero power comparator threshold	Measured on VAOUT	0.20	0.33	0.50	V

pin descriptions

CAI: (current amplifier non-inverting input) This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: (current amplifier output) This is the output of a wide bandwidth op amp that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct current.

CT: (oscillator timing capacitor) A capacitor from CT to GND will set the PWM oscillator frequency according to:

$$f = \left(\frac{0.725}{RT \times CT}\right)$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: (gate drive) The output drive for the PFC stage is a totem pole MOSFET gate driver on DRVOUT. Use a series gate resistor of at least 5 Ω to prevent interaction between the gate impedance and the DRVOUT output driver that might cause the DRVOUT to overshoot excessively. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

GND: (ground) All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1-μF or larger ceramic capacitor.

IAC: (input AC current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. Recommended maximum I_{IAC} is 500 μA.

MOUT: (multiplier output and current amplifier inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier is limited to $\left(2 \times I_{IAC}\right)$. The multiplier output current is given by the equation:

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^2 \times K}$$

Where $K = \frac{1}{V}$ is the multiplier gain constant.

OVP/EN: (over-voltage/enable) A window comparator input that disables the output driver if the boost output is 5% above nominal or will disable both the PFC output driver and reset SS if pulled below 1.9 V (typ).

pin descriptions (continued)

PKLMT: (PFC peak current limit) The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 kΩ and 100 kΩ is recommended.

SS: (soft start) V_{SS} is at ground for V_{VCC} low conditions. When enabled, SS will charge an external capacitor with a current source. This voltage will be used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a V_{VCC} dropout the OVP/EN is forced below 1.9 V (typ), SS will quickly discharge to disable the PWM.

Note: In an open-loop test circuit grounding the SS pin will not ensure 0% duty cycle. Please see application section for details.

VAOUT: (voltage amplifier output) This is the output of the op amp that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices will be inhibited unless V_{VCC} exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

VFF: (feed-forward signal) RMS signal generated at this pin by mirroring I_{IAC} into a single pole external filter.

$$R_{VFF} = \frac{V_{VFF(max)}}{\frac{I_{IAC(max)}}{2\sqrt{2}}} \times 0.9$$

VSENSE: (voltage amplifier inverting input) This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 10 mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1-μF or larger ceramic capacitor for best stability.

APPLICATION INFORMATION

The UCC3817 is a BiCMOS average current mode boost controller for high power factor, high efficiency preregulator power supplies. Figure 1 shows the UCC3817 in a 250-W PFC preregulator circuit. Off-line switching power converters normally have an input current that is not sinusoidal. The input current waveform will have high harmonic content because current is drawn in pulses at the peaks of the input voltage waveform. An active power factor correction circuit programs the input current to follow the line voltage, forcing the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between the current and voltage waveforms. Power factor can be defined in terms of the phase angle between two sinusoidal waveforms of the same frequency:

$$PF = \cos\Theta$$

Therefore, a purely resistive load would have a power factor of 1. In practice, power factors of 0.999 with THD (total harmonic distortion) less than 3% are possible with a well-designed circuit. Following guidelines are provided to design PFC boost converters using the UCC3817.

APPLICATION INFORMATION

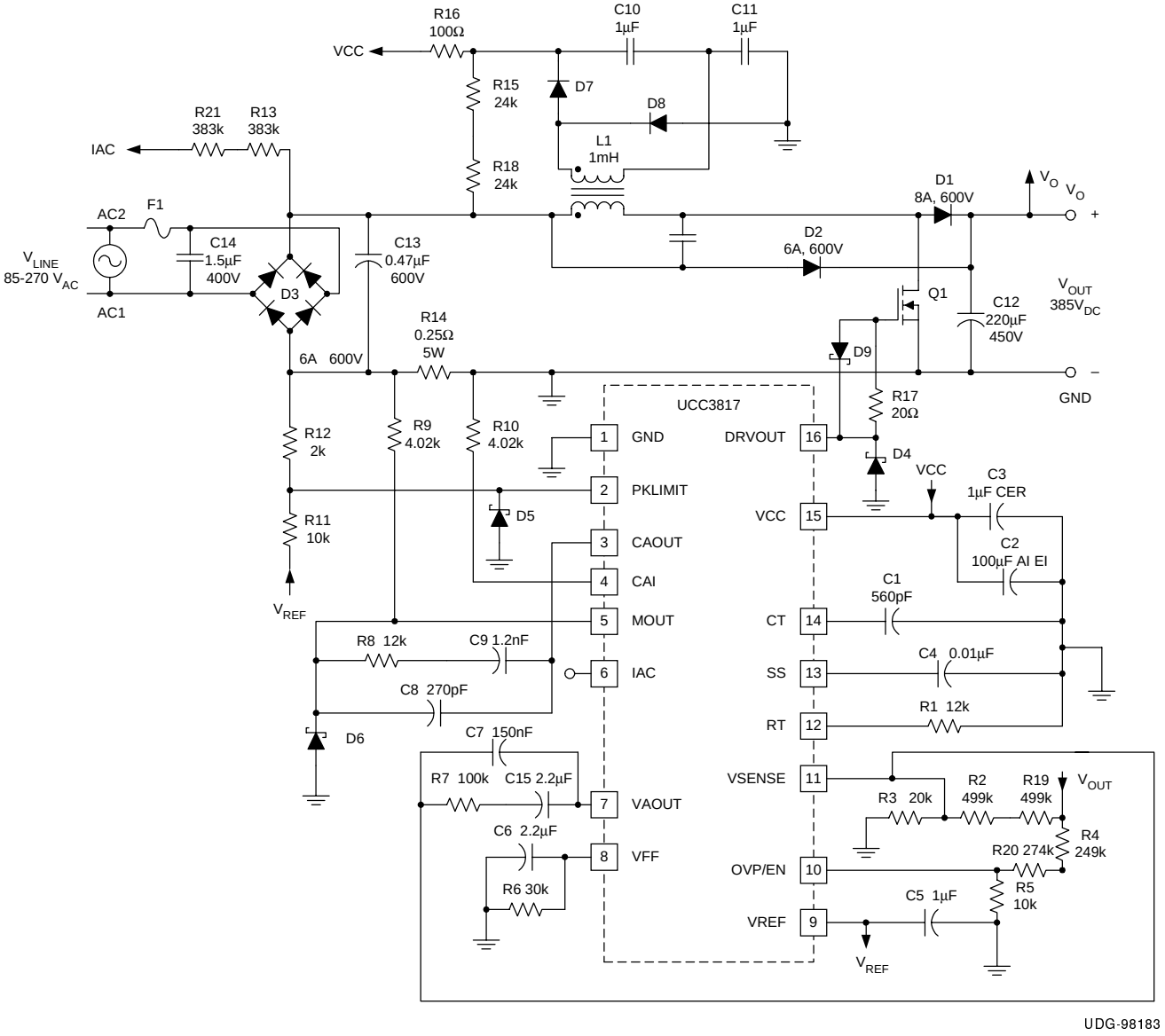

Figure 1. Typical Application Circuit

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APPLICATION INFORMATION

power stage

L_{BOOST} : The boost inductor value is determined by:

$$L_{BOOST} = \frac{\left(V_{IN(min)} \times D\right)}{(\Delta I \times fs)}$$

Where D is the duty cycle, ΔI is the inductor ripple current and f_S is the switching frequency. For the example circuit a switching frequency of 100 kHz, a ripple current of 875 mA, a maximum duty cycle of 0.688 and a minimum input voltage of 85 V_{RMS} gives us a boost inductor value of about 1 mH. The values used in this equation are at the peak of low line, where the inductor current and its ripple are at a maximum.

C_{OUT} : Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the hold-up time required for supporting the load after input ac voltage is removed. Hold-up is the amount of time that the output stays in regulation after the input has been removed. For this circuit, the desired hold-up time is approximately 16 ms. Expressing the capacitor value in terms of output power, output voltage, and hold-up time gives the equation:

$$C_{OUT} = \frac{\left(2 \times P_{OUT} \times \Delta t\right)}{\left(V_{OUT}^2 - V_{OUT(min)}^2\right)}$$

In practice the calculated minimum capacitor value may be inadequate because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often necessitates the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed can be determined by dividing the maximum specified output ripple voltage by the inductor ripple current. In this design hold-up time was the dominant determining factor and a 220-μF, 450-V capacitor was chosen for the output voltage level of 385 VDC at 250 W.

power switch selection

As in any power supply design, tradeoffs between performance, cost and size have to be made. When selecting a power switch it can be useful to calculate the total power dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, C_{OSS} loss and turn-on and turn-off losses:

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times fs$$

$$P_{COSS} = \frac{1}{2} \times C_{OSS} \times V^2_{OFF} \times fs$$

$$P_{ON} + P_{OFF} = \frac{1}{2} \times V_{OFF} \times I_L \times \left(t_{ON} + t_{OFF}\right) \times fs$$

where Q_{GATE} is the total gate charge, V_{GATE} is the gate drive voltage, f_S is the clock frequency, C_{OSS} is the drain source capacitance of the MOSFET, t_{ON} and t_{OFF} are the switching times (estimated using device parameters R_{GATE}, Q_{GD} and V_{TH}) and V_{OFF} is the voltage across the switch during the off time, in this case $V_{OFF} = V_{OUT}$.

Conduction loss is calculated as the product of the $R_{DS(on)}$ of the switch (at the worst case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \times K \times I^2_{RMS}$$

where K is the temperature factor found in the manufacturer's $R_{DS(on)}$ vs. junction temperature curves.

APPLICATION INFORMATION

power switch selection (continued)

Calculating these losses and plotting against frequency gives a curve which enables the designer to determine either which manufacturer's device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. In this example the switch was chosen as the best trade off between performance, availability and cost. An excellent review of this procedure can be found in the Unitrode Power Supply Design Seminar SEM1200, Topic 6, Design Review: 140 W, *[Multiple Output High Density DC/DC Converter]*.

soft start

The soft start circuitry is used to prevent overshoot of the output voltage during start up. This is accomplished by bringing up the voltage amplifier's output (V_{VAOUT}) slowly which will allow for the PWM duty cycle to increase slowly. Please use the following equation to select a capacitor for the soft start pin.

In this example T_{DELAY} is equal to 5 ms which would yield a C_{SS} of approximately 7 nf.

$$C_{SS} = \frac{10\ \mu A \times T_{DELAY}}{7.5\ V}$$

In an open loop test circuit shorting the soft start pin to ground does not guarantee 0% duty cycle. This is due to the current amplifiers input offset voltage which could force the current amplifier output high or low depending on the polarity of the offset voltage. However, in the typical application there is sufficient amount of inrush and bias current to overcome the current amplifiers offset voltage.

multiplier

The output of the multiplier of the UCC3817 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high power factor operation. As such, the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are VAOUT, the voltage amplifier error signal, I_{IAC}, a representation of the input rectified ac line voltage, and an input voltage feedforward signal, V_{VFF}. The output of the multiplier, I_{MOUT}, can be expressed:

$$I_{MOUT} = I_{IAC} \times \frac{\left(V_{VAOUT} - 1\right)}{V \times K \times V_{VFF}^{2}}$$

where K is a constant typically equal to $\frac{1}{V}$.

The I_{IAC} signal is obtained through a high value resistor connected between the rectified ac line and the IAC pin of the UCC3817. This resistor is sized to give the maximum I_{IAC} current at high line. For this device the maximum I_{IAC} current is about 500 μA. A higher current than this can drive the multiplier out of its linear range. A smaller current level will be functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85 VAC to 265 VAC gives a resistor value of 750 kΩ. Because of voltage rating constraints of standard 1/4 W resistors, use a combination of lower value resistors connected in series to give the 750 kΩ value and distribute the high voltage across two or more resistors.

The current through the I_{IAC} resistor is mirrored internally to the VFF pin where it is filtered to produce a voltage feedforward signal proportional to line voltage and free of a 120 Hz ripple component. This second harmonic ripple component at the VFF pin is one of the major contributors to harmonic distortion in the system, so adequate filtering is crucial. Refer to Unitrode Power Supply Design Seminar, SEM-700 Topic 7, *[Optimizing the Design of a High Power Factor Preregulator.]* Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is:

$\frac{1.5\%}{66\%}$ or 0.022

APPLICATION INFORMATION

multiplier (continued)

A ripple frequency (f_R) of 120 Hz and an attenuation of 0.022 gives us a single pole filter with:

$$fp = 120\ Hz \times 0.022 = 2.6\ Hz$$

The range of this input to the multiplier should be 0.5 V to 5.5 V over the line input range. Therefore the filter resistor should be sized accordingly. Maximum I_{IAC} current is 500 μA, mirrored 2:1 to VFF becomes 250 μA. The dc output is 90% of the RMS value of this half sine wave, or 159 μA. So the filter resistor should be equal to the voltage swing of the input to the multiplier divided by the dc current or:

$$\frac{5\ V}{159\ \mu A} = 31.44\ k\Omega$$

Select 30 kΩ for a standard value. Solving for the capacitor value:

$$C_{VFF} = \frac{1}{2\,\pi(30\ K)(2.6\ Hz)} \approx 2.2\ \mu F$$

This results in a single pole filter, which will adequately attenuate the harmonic distortion and also meet the dc requirement of the proper voltage swing across line conditions.

The R_{MOUT} resistor is sized to match the maximum current through the sense resistor to the maximum multiplier current. The maximum multiplier current, or $I_{MOUT(max)}$, can be determined by the equation:

$$I_{MOUT(max)} = \frac{I_{IAC}@V_{IN(min)} \times \left(V_{VAOUT(max)} - 1V\right)}{K \times V_{VFF}^{2}\ (min)}$$

$I_{MOUT(max)}$ for this design is approximately 315 μA. The R_{MOUT} resistor can then be determined by:

$$R_{MOUT} = \frac{V_{RSENSE}}{I_{MOUT(max)}}$$

In this example R_{MOUT} is equal to 3.91 kΩ.

voltage loop

The second major source of harmonic distortion is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier and appears as a 3rd harmonic ripple at the input to the multiplier. The voltage loop must be compensated not just for stability but also to attenuate the contribution of this ripple to the total harmonic distortion of the system. (refer to Figure 2).

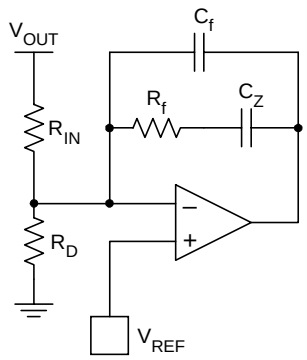

Figure 2. Voltage Amplifier Configuration

APPLICATION INFORMATION

voltage loop (continued)

The gain of the voltage amplifier, G_{VA}, can be determined by first calculating the amount of ripple present on the output capacitor. The peak value of the second harmonic voltage is given by the equation:

$$V_{OPK} = \frac{P_{IN}}{\left(2\pi \times f_R \times C_{OUT} \times V_{OUT}\right)}$$

In this example V_{OPK} is equal to 3.91 V. Assuming an allowable contribution of 0.75% (1.5% peak to peak) from the voltage loop to the total harmonic distortion budget we set the gain equal to:

$$G_{VA} = \frac{\left(\Delta V_{VAOUT}\right)(0.015)}{V_{OPK}}$$

where ΔV_{VAOUT} is the effective output voltage range of the error amplifier (5 V for the UCC3817). The network needed to realize this filter is comprised of an input resistor, R_{IN}, and feedback components C_f, C_Z, and R_f. The value of R_{IN} is already determined because of its function as one half of a resistor divider from V_{OUT} feeding back to the voltage amplifier for output voltage regulation. In this case the value was chosen to be 1 MΩ. This high value was chosen to reduce power dissipation in the resistor. In practice, the resistor value would be realized by the use of two 500-kΩ resistors in series because of the voltage rating constraints of most standard 1/4-W resistors. The value of C_f is determined by the equation:

$$C_f = \frac{1}{\left(2\pi \times f_R \times G_{VA} \times R_{IN}\right)}$$

In this example C_f equals 150 nF. Resistor R_f sets the dc gain of the error amplifier and thus determines the frequency of the pole of the error amplifier. The location of the pole can be found by setting the gain of the loop equation to one and solving for the crossover frequency. The frequency, expressed in terms of input power, can be calculated by the equation:

$$f_{VI}^2 = \frac{P_{IN}}{\left((2\pi)^2 \times \Delta V_{VAOUT} \times V_{OUT} \times R_{IN} \times C_{OUT} \times C_f\right)}$$

f_{VI} for this converter is 10 Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM1000, Topic 1, *[A 250-kHz, 500-W Power Factor Correction Circuit Employing Zero Voltage Transitions]*.

Solving for R_f becomes:

$$R_f = \frac{1}{\left(2\pi \times f_{VI} \times C_f\right)}$$

or R_f equals 100 kΩ.

Due to the low output impedance of the voltage amplifier capacitor C_Z was added in series with R_F to reduce loading on the voltage divider. To ensure the voltage loop crossed over at f_{VI}, C_Z was selected to add a zero at a 10th of f_{VI}. For this design a 2.2-μF capacitor was chosen for C_Z. The following equation can be used to calculate C_Z.

$$C_Z = \frac{1}{2 \times \pi \times \frac{f_{VI}}{10} \times R_f}$$

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APPLICATION INFORMATION

current loop

The gain of the power stage is:

$$G_{ID}(s) = \frac{\left(V_{OUT} \times R_{SENSE}\right)}{\left(s \times L_{BOOST} \times V_P\right)}$$

R_{SENSE} has been chosen to give the desired differential voltage for the current sense amp at the desired current limit point. In this example a current limit of 4 A and a reasonable differential voltage to the current amp of 1 V gives a R_{SENSE} value of 0.25 Ω. V_P in this equation is the voltage swing of the oscillator ramp, 4 V for the UCC3817. Setting the crossover frequency of the system to 1/10th of the switching frequency, or 10 kHz, requires a power stage gain at that frequency of 0.383. In order for the system to have a gain of 1 at the crossover frequency, the current amplifier needs to have a gain of $1/G_{PS}$ at that frequency. G_{EA}, the current amp gain is then:

$$G_{EA} = \frac{1}{G_{ID}} = \frac{1}{0.383} = 2.611$$

R_I is the R_{MOUT} resistor, previously calculated to be 3.9 kΩ. (refer to Figure 3). The gain of the current amp is R_f/R_I, so multiplying R_I by G_{EA} gives the value of R_f, in this case approximately 12 kΩ. Setting a zero at the crossover frequency and a pole at half the switching frequency completes the current loop compensation.

$$C_Z = \frac{1}{2 \times \pi \times R_f \times f_C}$$

$$C_P = \frac{1}{2 \times \pi \times R_f \times \frac{f_s}{2}}$$

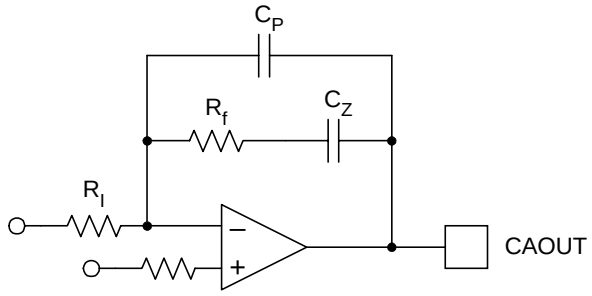

Figure 3. Current Loop Compensation

The UCC3817 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous Unitrode PFC controllers improves noise immunity in the current amplifier. It also adds a phase inversion into the control loop. The UCC3817 takes advantage of this phase inversion to implement leading-edge duty cycle modulation. Synchronizing a boost PFC controller to a downstream dc to dc controller reduces the ripple current seen by the bulk capacitor between stages, reducing capacitor size and cost and reducing EMI. This is explained in greater detail in a following section. The UCC3817 current amplifier configuration is shown in Figure 4.

APPLICATION INFORMATION

current loop (continued)

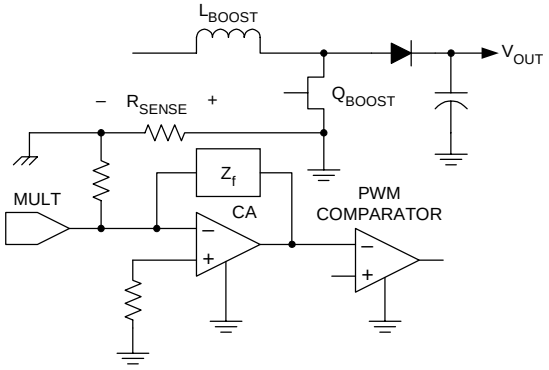

Figure 4. UCC3817 Current Amplifier Configuration

start up

The UCC3818 version of the device is intended to have VCC connected to a 12 V supply voltage. The UCC3817 has an internal shunt regulator enabling the device to be powered from bootstrap circuitry as shown in the typical application circuit of Figure 1. The current drawn by the UCC3817 during under-voltage lockout, or start up current, is typically 150 μA. Once VCC is above the UVLO threshold, the device is enabled and will draw 4 mA typically. A resistor connected between the rectified ac line voltage and the VCC pin provides current to the shunt regulator during power-up. Once the circuit is operational the bootstrap winding of the inductor will provide the VCC voltage. Sizing of the start-up resistor is determined by the start-up time requirement of the system design.

$$I_C = C\frac{\Delta V}{\Delta t}$$

$$R = \frac{V_{RMS} \times (0.9)}{I_C}$$

Where I_C is the charge current, C is the total capacitance at the VCC pin, ΔV is the UVLO threshold and t is the allowed start-up time.

Assuming a 1 second allowed start-up time, a 16-V UVLO threshold, and a total VCC capacitance of 100 μF, a resistor value of 51 kΩ is required at a low line input voltage of 85 V_{RMS}. The IC start-up current is sufficiently small as to be ignored in sizing the start-up resistor.

capacitor ripple reduction

For a power system where the PFC boost converter is followed by a dc-dc converter stage, there are benefits to synchronizing the two converters. In addition to the usual advantages such as noise reduction and stability, proper synchronization can significantly reduce the ripple currents in the boost circuit's output capacitor. Figure 5 helps illustrate the impact of proper synchronization by showing a PFC boost converter together with the simplified input stage of a forward converter. The capacitor current during a single switching cycle depends on the status of the switches Q1 and Q2 and is shown in Figure 6. It can be seen that with a synchronization scheme that maintains conventional trailing edge modulation on both converters, the capacitor current ripple is highest. The greatest ripple current cancellation is attained when the overlap of Q1 off-time and Q2 on-time is maximized. One method of achieving this is to synchronize the turn-on of the boost diode (D1) with the turn-on of Q2. This approach implies that the boost converter's leading edge is pulse width modulated while the forward converter is modulated with traditional trailing edge PWM. The UCC3817 is designed as a leading edge

APPLICATION INFORMATION

capacitor ripple reduction (continued)

modulator with easy synchronization to the downstream converter to facilitate this advantage. Table 1 compares the $I_{CB(rms)}$ for D1/Q2 synchronization as offered by UCC3817 vs. the $I_{CB(rms)}$ for the other extreme of synchronizing the turn-on of Q1 and Q2 for a 200-W power system with a V_{BST} of 385 V.

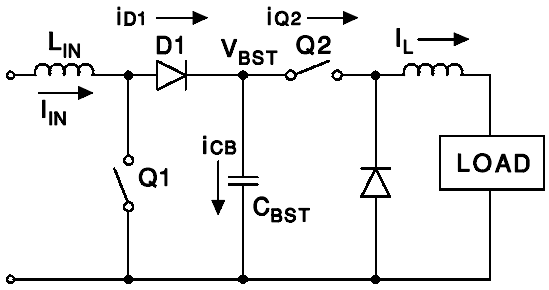

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Figure 5. Simplified Representation of a 2-Stage PFC Power Supply

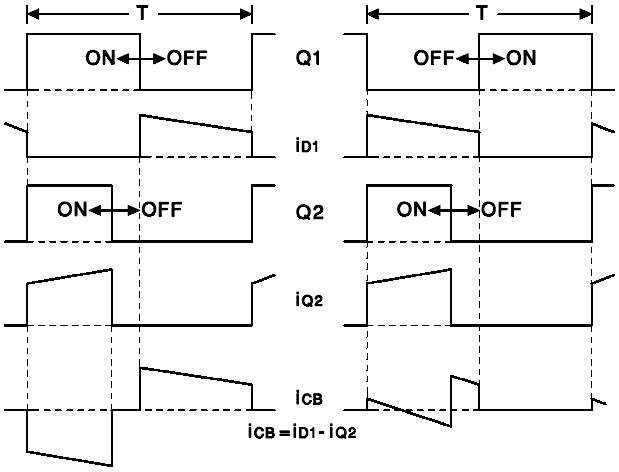

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Figure 6. Timing Waveforms for Synchronization Scheme

Table 1. Effects of Synchronization on Boost Capacitor Current

	V_{IN} = 85 V		V_{IN} = 120 V		V_{IN} = 240 V	
D(Q2)	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2
0.35	1.491 A	0.835 A	1.341 A	0.663 A	1.024 A	0.731 A
0.45	1.432 A	0.93 A	1.276 A	0.664 A	0.897 A	0.614 A

Table 1 illustrates that the boost capacitor ripple current can be reduced by about 50% at nominal line and about 30% at high line with the synchronization scheme facilitated by the UCC3817. The output capacitance value can be significantly reduced if its choice is dictated by ripple current or the capacitor life can be increased as a result. In cost sensitive designs where hold-up time is not critical, this is a significant advantage.

APPLICATION INFORMATION (continued)

capacitor ripple reduction (continued)

An alternative method of synchronization to achieve the same ripple reduction is possible. In this method, the turn-on of Q1 is synchronized to the turn-off of Q2. While this method yields almost identical ripple reduction and maintains trailing edge modulation on both converters, the synchronization is much more difficult to achieve and the circuit can become susceptible to noise as the synchronizing edge itself is being modulated.

MULTIPLIER CONSTANT POWER PERFORMANCE

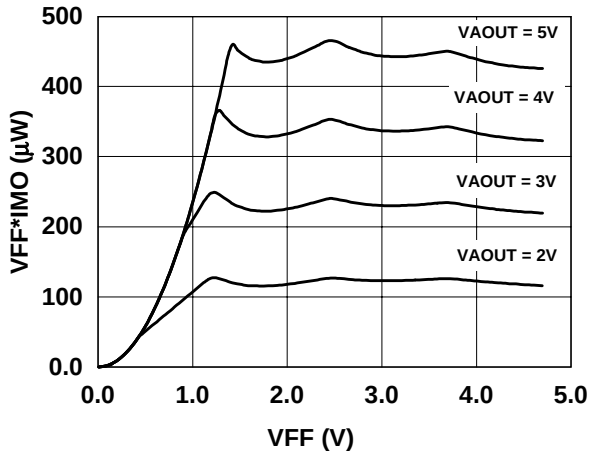

Figure 7

REFERENCE VS. INPUT VOLTAGE

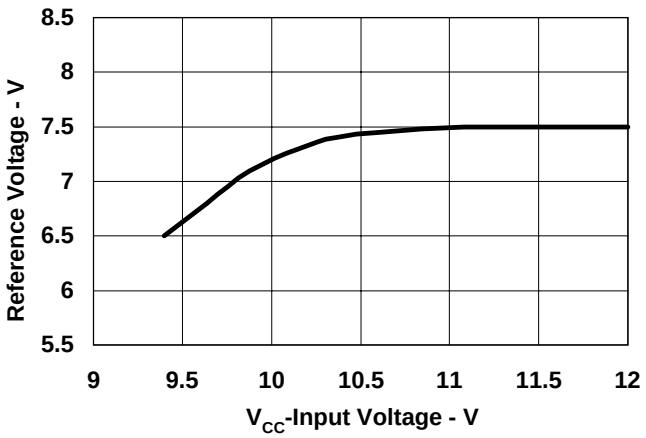

Figure 8

MULTIPLIER GAIN (K) vs. VAOUT

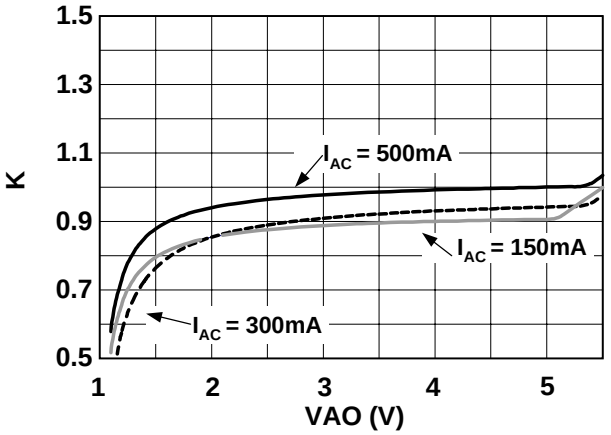

Figure 9

MULTIPLIER OUTPUT CURRENT (I_{MOUT}) vs. VAOUT

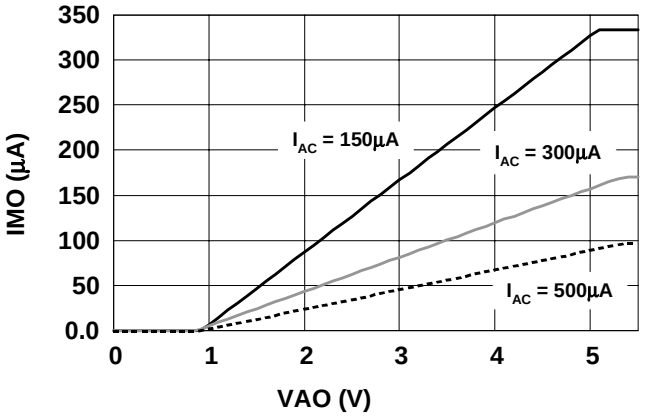

Figure 10

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