Multi-Phase Synchronous-Rectified Buck Controller for Next Generation CPU Core Power

General Description

The uP1608P/Q is a multi-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high-performance Intel microprocessors. It integrates a 8-bit DAC that supports Intel VR10/VR11 and AMD K8-M2 tables to set the output voltage between 0.5V and 1.6V.

The uP1608P provides programmable 3/4 phase operation and uP1608Q provides 1/2 phase operation. uP1608P/Q integrates 3/2 bootstrapped drivers that support 12V + 12V driving capability. 4 phase operation is enabled by a logic level PWM output, achieving optimal balance between cost and flexibility. It also supports dynamic phase selection by PS1/2 pins. Operation with phase reduction at light load conditions achieves high efficiency over a wide range of output current.

The uP1608P/Q includes programmable droop slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient.

Other features include accurate and reliable short-circuit protection, adjustable over current protection, and a delayed power OK output. This uP1608P is available in VQFN6x6-48L package and uP1608Q is available in VQFN5x5-40L package.

Ordering Information

Order Number	Package	Top Marking	Remark
uP1608PQGK	VQFN6x6-48L	uP1608PK	3/4 Phase Operation
uP1608QQGJ	VQFN5x5-40L	uP1608QJ	1/2 Phase Operation

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

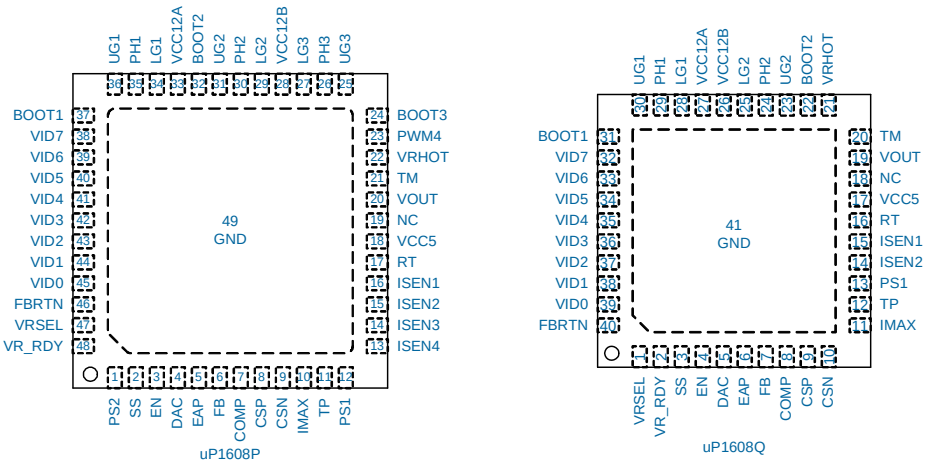
Features

- **Selectable Phase Number Operation**
  - **uP1608P : 3/4 Phase**
  - **uP1608Q : 1/2 Phase**
- **8-bit DAC, Supporting Intel VR10/VR11 and AMD K8-M2 CPUs**
- **Programmable Dynamic Power Saving Mode Operation**
- **Simple Single-Loop Voltage-Mode Control**
- **Integrated 12V Bootstrapped Drivers with Internal Bootstrap Diode**
- **Lossless $R_{DS(ON)}$ Current Sensing for Current Balance**
- **Adjustable Operation Frequency form 100kHz to 1MHz Per Phase**
- **External Compensation**
- **Adjustable Over Current Protection**
- **Adjustable Soft Start**
- **VR_HOT and VR_RDY Indication**
- **VQFN6x6-48L(uP1608P) and VQFN5x5-40L (uP1608Q) Packages**
- **RoHS Compliant and Halogen Free**

Applications

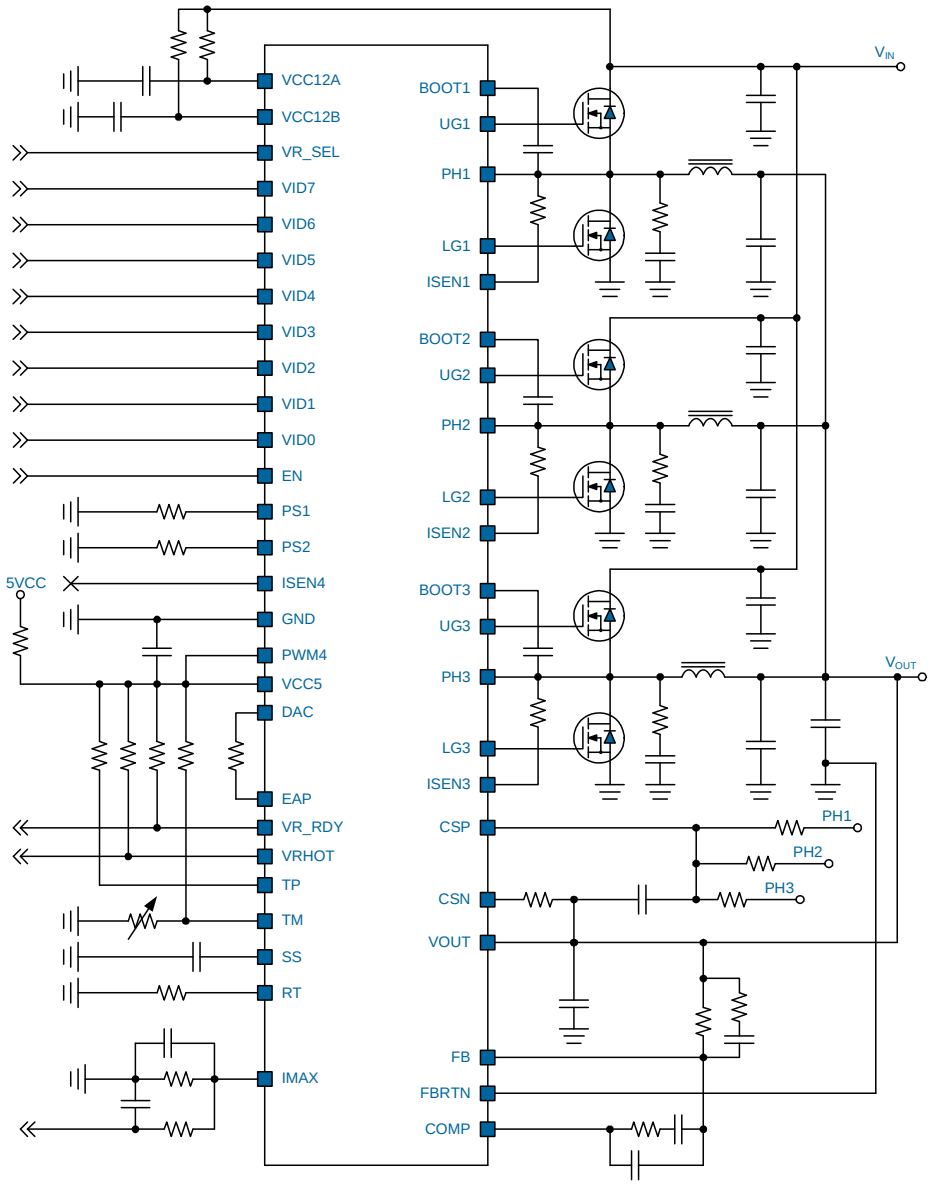
- **Desktop PC Core Power Supplies**
- **Middle/High End Graphic Cards**
- **Low Output Voltage, High Power Density DC/DC Converters**
- **Voltage Regulator Modules**

Pin Configuration



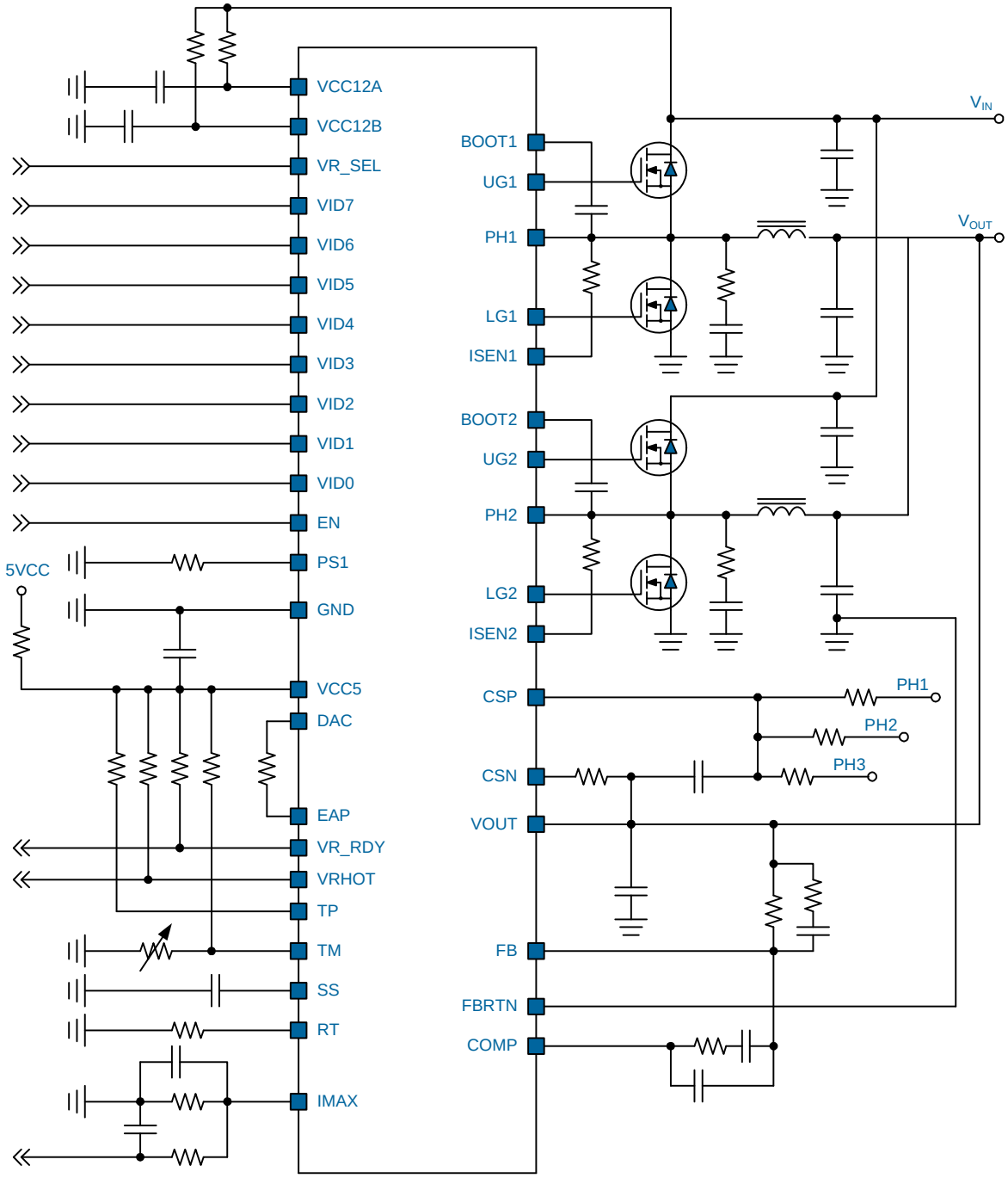
Typical Application Circuit

uP1608P-for 3 phase



Typical Application Circuit

uP1608Q-for 2 phase



Functional Pin Description

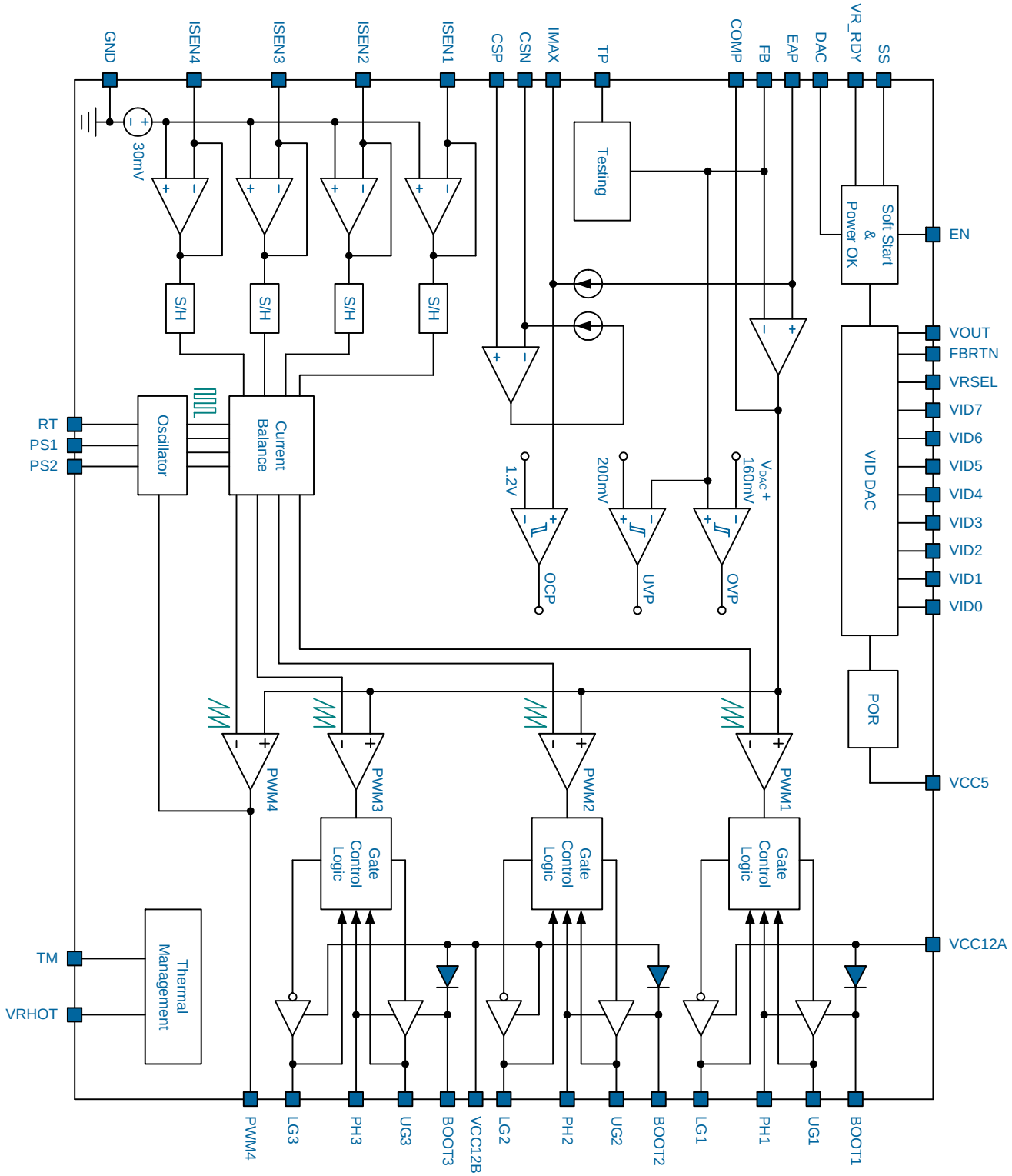
Pin No.		Name	Pin Function
PQGK	QQGJ		
1	NA	PS2	**Power Saving Mode Setting Input 2.** Connect a resistor from this pin to GND to set the phase reduction threshold level.
2	3	SS	**Soft Start.** Connect a capacitor from this pin to GND to set the soft start time.
3	4	EN	**Chip Enable.** Pulling this pin lower than 0.4V shuts down the device**.**
4	5	DAC	**DAC Output.** Output of the internal DAC. Connect a resistor form this pin to EAP to set the load line slope.
5	6	EAP	**Non-Inverting Input of the Error Amplifier.** Connect a resistor from this pin to DAC to set the load line slope.
6	7	FB	**Feedback Pin.** This pin is the inverting input of the error amplifier.
7	8	COMP	**Compensation Output.** This pin is the output of the error amplifier
8	9	CSP	**Positive Input of the Current Sensing GM Amplifier.**
9	10	CSN	**Negative Input of the Current Sensing GM Amplifier.**
10	11	IMAX	**Output Current Indication.** Connect a resistor from this pin to GND to set the over current protection level.
11	12	TP	**Test Pin.** Reserved for internal testing purpose.
12	13	PS1	**Power Saving Mode Setting Input 1.** Connect a resistor from this pin to ground to set the phase reduction threshold level.
13	NA	ISEN4	**Current Sensing for Phase 4.**
14	NA	ISEN3	**Current Sensing for Phase 3.**
15	14	ISEN2	**Current Sensing for Phase 2.**
16	15	ISEN1	**Current Sensing for Phase 1.**
17	16	RT	**Switching Frequency Programming.** Connect a resistor from this pin to GND to set the switching frequency.
18	17	VCC5	**5V Supply Input.** This pin receives a 5V voltage source to power the control circuit. Connect this pin to ATX 5VCC.
19	18	NC	**Not Connected.**
20	19	VOUT	**Output Voltage Sensing.**
21	20	TM	**Thermal Monitoring.** Connect NTC network to this pin for thermal monitoring.
22	21	VRHOT	**VR HOT Output.**
23	NA	PWM4	**PWM Output of Phase 4.** Connect this pin to input pin of the companion gate driver, such as uP6281. Connect this pin to VCC5 for 3 phase operation.
24	NA	BOOT3	**BOOT for Phase 3.** Connect a capacitor from this pin to PH3 to form a bootstrap circuit for upper gate driver of the phase 3.

Functional Pin Description

Pin No.		Name	Pin Function
PQGK	QQGJ		
25	NA	UG3	**Upper Gate Driver for Phase 3.** Connect this pin to the gate of phase 3 upper MOSFET.
26	NA	PH3	**Phase Pin for Phase 3.** This pin is the return path of upper gate driver for phase 3. Connect a capacitor from this pin to BOOT3 to form a bootstrap circuit for upper gate driver of the phase 3.
27	NA	LG3	**Lower Gate Driver for Phase 3.** Connect this pin to the gate of phase 3 lower MOSFET.
28	26	VCC12B	**Supply Input.** This pin supplies current for gate drivers and control circuits.
29	25	LG2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
30	24	PH2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase 2.
31	23	UG2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET.
32	22	BOOT2	**BOOT for Phase 2.** Connect a capacitor from this pin to PH2 to form a bootstrap circuit for upper gate driver of the phase 2.
33	27	VCC12A	**Supply Input.** This pin supplies current for gate drivers and control circuits.
34	28	LG1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
35	29	PH1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
36	30	UG1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
37	31	BOOT1	**BOOT for Phase 1.** Connect a capacitor from this pin to PH1 to form a bootstrap circuit for upper gate driver of the phase 1.
38	32	VID7	**Bit 7 of DAC Input.** Pull this pin to VCC5 for AMD K8-M2 VID table.
39	33	VID6	**Bit 6 of DAC Input.**
40	34	VID5	**Bit 5 of DAC Input.**
41	35	VID4	**Bit 4 of DAC Input.**
42	36	VID3	**Bit 3 of DAC Input.**
43	37	VID2	**Bit 2 of DAC Input.**
44	38	VID1	**Bit 1 of DAC Input.**
45	39	VID0	**Bit 0 of DAC Input.**
46	40	FBRTN	**Return for the DAC Circuit.** Connect this pin to the point where output voltage is to be regulated.
47	1	VRSEL	**VID Table Selection.** Connect this pin to VCC5 for VR11.X VID table, and to GND for VR10.X VID table.
48	2	VR_RDY	**VR Ready Indication.**
Exposed Pad GND			**Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

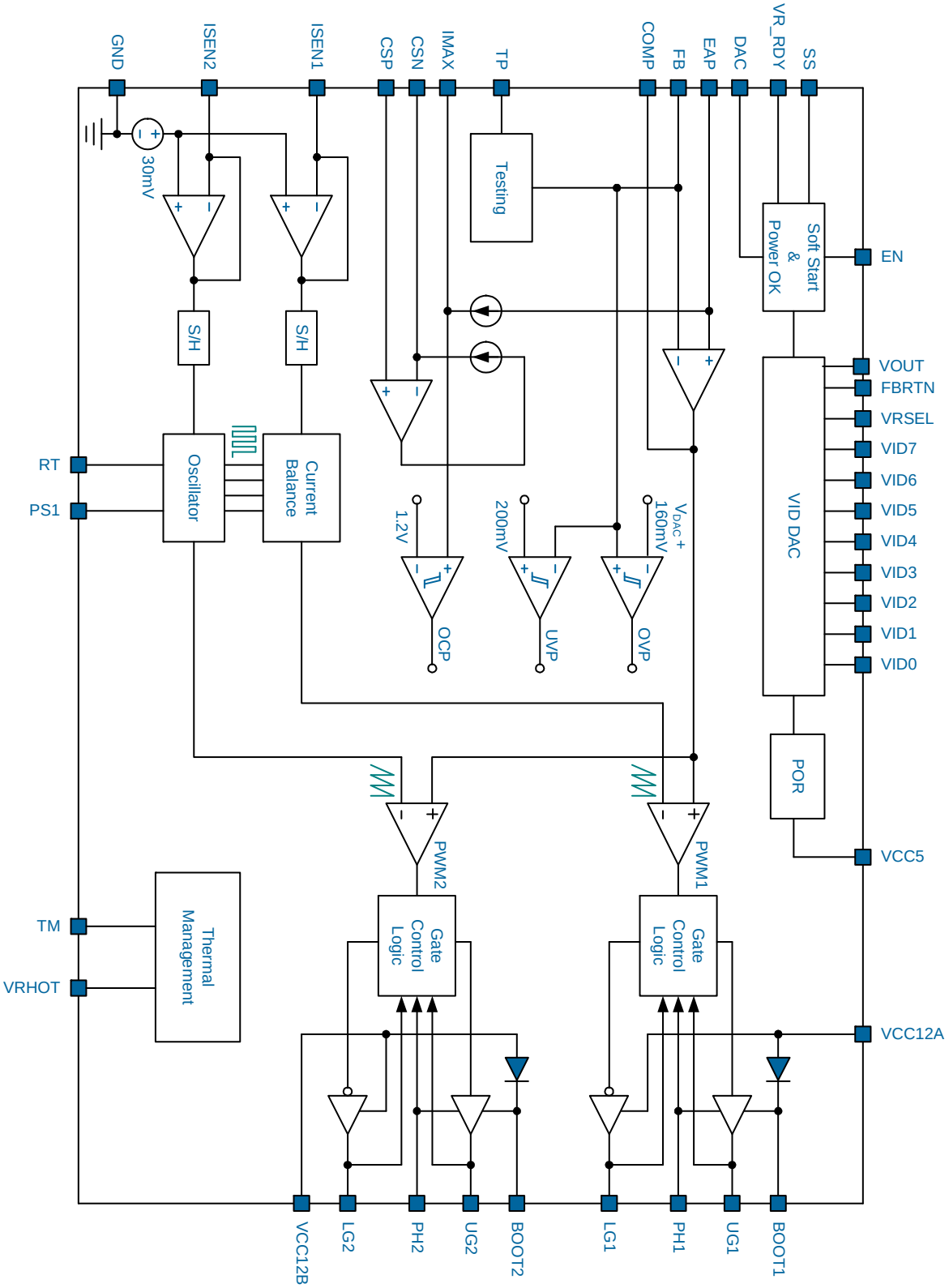
Functional Block Diagram

uP1608P



Functional Block Diagram

uP1608Q



Functional Description

The uP1608P/Q is a multi-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high-performance Intel microprocessors. It integrates a 8-bit DAC that supports Intel VR10/VR11 and AMD K8-M2 tables to set the output voltage between 0.375V and 1.6V.

The uP1608P provides programmable 3/4 phase operation and uP1608Q provides 1/2 phase operation. uP1608P/Q integrates 3/2 bootstrapped drivers that support 12V + 12V driving capability. 4 phase operation is enabled by a logic level PWM output, achieving optimal balance between cost and flexibility. It also supports dynamic phase selection by PS1/2 pins. Operation with phase reduction at light load conditions achieves high efficiency over a wide range of output current.

The uP1608P/Q includes programmable droop slope functions to adjust the output voltage as a function of the load current, optimally positioning it for a system transient.

Other features include accurate and reliable short-circuit protection, adjustable over current protection, and a delayed power OK output. This uP1608P is available in VQFN6x6-48L package and uP1608Q is available in VQFN5x5-40L package.

Supply Input and Power on Reset

The uP1608P/Q receives supply input from VCC12A/B pins to provide current to gate drivers. RC filters are required for locally bypassing the supply input pins. Since only the VCC12A pin is monitored for power on reset, **make sure the VCC12A/B pins are connected to the same voltage source externally.** The POR level is typically 9.5V at VCC12A rising.

The VCC5 pin receives a well-decoupled 5V voltage source to power the internal control circuit. Place a minimum 1uF ceramic capacitor physically near the VCC5 pin for locally bypassing the VCC5 voltage. The VCC5 voltage is continuously monitored for power on reset. The POR level is typical 4.1V at VCC5 rising.

Operation Phase Selection

The uP1608P supports 3/4 phase operation. PWM4 status are checked at POR for operation phase selection. Connect PWM4 to VCC5 for 3-phase operation for uP1608P. Let the unused current sensing pin ISEN4 float when selecting 3-phase operation. (*See the related section for Dynamic Phase Reduction.*)

VID Table Selection

The uP1608P/Q supports Intel VR10/VR11 and AMD K8-M2 VID tables. Pulling the VRSEL pin lower than 0.4V selects VR10 table as shown in Table 1 while pulling the VRSEL pin higher than 0.8V select the VR11 table as shown in Table 2. Pulling the VID7 pin to VCC5 selects AMD k8-M2 table.

Oscillation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency with 4 phase operation (uP1608P) and 1/2 phase operation (uP1608Q) as:

$$f_{OSC} = 300\left(\frac{24k\Omega}{R_{RT}(k\Omega)}\right)^{0.92} \quad (kHz)$$

Figure 1 shows the relationship between oscillation frequency and R_{RT}.

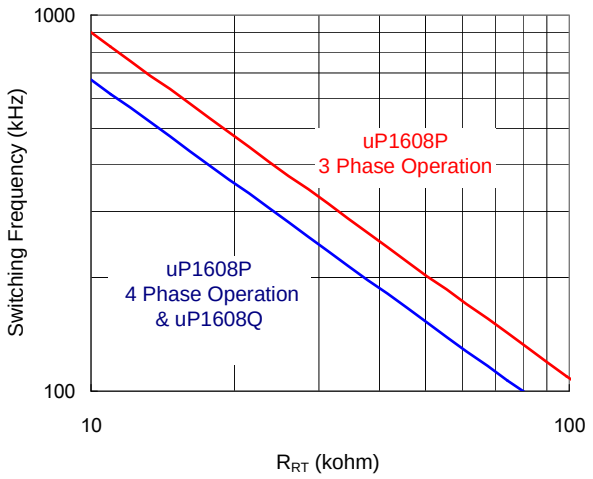


Figure 1. Switching Frequency vs. R_{RT}

When 3 phase operation(uP1608P), the oscillation frequency vs. R_{RT} relationship is revised as:

$$f_{OSC} = 300\left(\frac{33k\Omega}{R_{RT}(k\Omega)}\right)^{0.92} \quad (kHz)$$

Output Current Sensing

Figure 2 illustrates the output current sensing block of the uP1608P/Q. The voltage V_{CS} across the current sensing capacitor C_{CS} can be expressed as:

$V_{CS} = I_{OUT} \times DCR/P$

if the following condition is true.

$P \times L / DCR = R_{CSP} \times C_{CS}$

where P is the phase number of operation (P = 2 for two phase operation, P = 3 for three phase operation, and P = 4 for four phase operation), L is the output inductor of the buck converter, DCR is the parasitic resistance of the inductor, R_{CSP} and C_{CS} are the external RC network for current sensing.

The GM amplifier will source a current I_{AVG} to the CSN pin

Functional Description

Table 1. VR11 VID Table (VRSEL = VCC5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750

Table 1. VR11 VID Table (Cont.) (VRSEL = VCC5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625

Table 1. VR11 VID Table (Cont.) (VRSEL = VCC5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88850
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500

Table 1. VR11 VID Table (Cont.) (VRSEL = VCC5)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

Functional Description

Table 1. VRD10 + VID6 VID Table (VRSEL = GND)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875

Table 1. VRD10 + VID6 VID Table (Cont.) (VRSEL = GND)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625

Functional Description

Table 1. VRD10 + VID6 VID Table (Cont.) (VRSEL = GND)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	Voltage
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.89750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

Table 3. AMD K8-M2 VID Table (Cont.) (VID7 = VCC5)

VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0..7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125

Table 3. AMD K8-M2 VID Table (Cont.) (VID7 = VCC5)

VID5	VID4	VID3	VID2	VID1	VID0	Voltage
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4626
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

to let its inputs virtually short circuit.

$I_{AVG} \times R_{CSN} = V_{CS}$

Therefore the output current signal I_{AVG} can be expressed as:

$$I_{AVG} = \frac{I_{OUT} \times DCR}{P \times R_{CSN}}$$

The output current signal I_{AVG} is used as droop turning and output over current protection. Please see the related section for details.

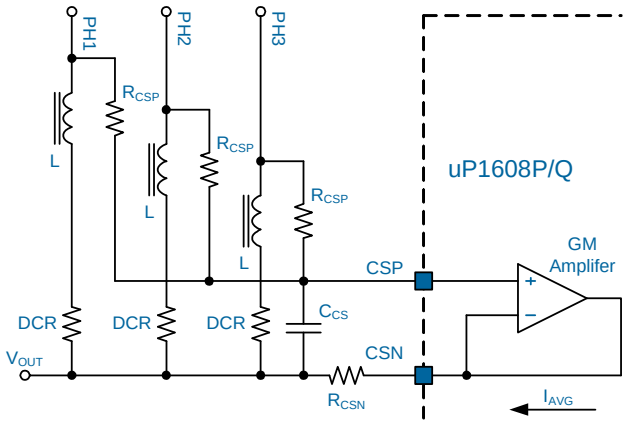


Figure 2. Output Current Sensing of uP1608P/Q.

Voltage Control Loop

Figure 3 illustrates the voltage control loop of the uP1608P/Q. FB and EAP are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage V_{COMP} and the duty cycle of buck converter to force FB voltage V_{FB} follows V_{EAP}.

As shown in Figure 3, V_{DAC} is output of the internal VID table. The slew rate of V_{DAC} is limited by the capacitor connected to SS pin during soft start and VID on the fly transition. The sensed current signal is mirrored to the EAP pin and creates voltage at EAP pin as:

$V_{EAP} = V_{DAC} - K \times R_{DRP} \times I_{AVG}$

where V_{DAC} is a slew rate limited voltage source, I_{AVG} is a current source proportional to output current, K is the current mirror gain (uP1608P: K = 3 for three phase operation, K = 4 for four phase operation; uP1608Q: K=4 for 1/2 phase operation) and R_{DRP} is an external resistor for adjusting load line slope.

Note that the constant P and K are only dependent of the power stage topology. They are programmed by the PWM4 configuration. Dynamic phase reduction will not affect the value of P and K.

Functional Description

Therefore, the output voltage will be:

$$V_{OUT} = V_{DAC} - \frac{K \times R_{DRP} \times I_{OUT} \times DCR}{P \times R_{CSN}}$$

Please see the related section for details.

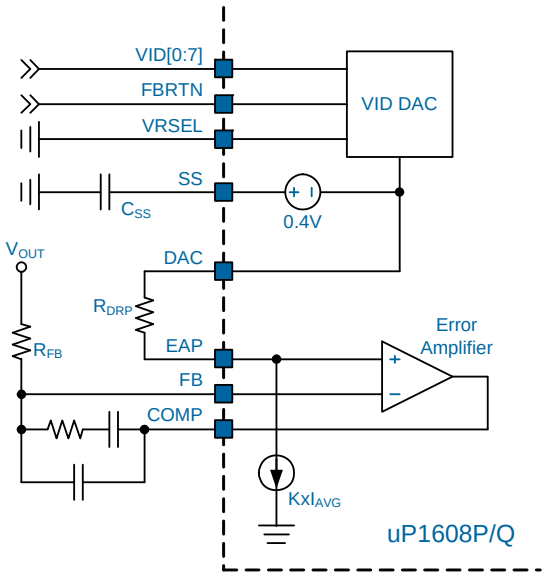


Figure 3. Voltage Control Loop.

Soft Start and Power OK

Figure 4 illustrates typical VR11.1 compliant soft start cycle of uP1608P/Q. A capacitor C_{SS} connected to SS pin is used to adjust the soft start cycle.

A limited current source I_{SS} is used to charge/discharge C_{SS} when VID changes. Since V_{DAC} is 0.8V higher than V_{SS}, this limit the slew rate of V_{SS} and V_{DAC} during soft start and VID on the fly period. This consequently limits the output voltage ramp up/down slew rate.

The uP1608P/Q is POR and enabled at T0. There is a 900us time delay (T0 ~ T1) before the current source I_{SS} begins charging the C_{SS}. The DAC voltage V_{DAC} and output voltage V_{OUT} is kept zero during (T0 ~ T2). The V_{DAC} and V_{OUT} ramps up to boot up voltage V_{BOOT} during time delay TD2. The uP1608P/Q inserts a time delay TD3 for the VID to get valid. The V_{DAC} and V_{OUT} ramps to its target value according to VID status during TD4. The uP1608P/Q asserts soft start end and set VR_RDY to high impedance status at T6.

Before time delay TD6 ends, the I_{SS} is limited to 10uA. After that, the I_{SS} is limited to 160uA. Consequently, critical time periods are calculated as:

(T2 - T1) = 0.8V x C_{SS} / 10uA

TD1 = T2 - T0 = 900us + 0.8V x C_{SS} / 10uA

TD2 = V_{BOOT} x C_{SS} / 10uA = 1.1V x C_{SS} / 10uA

TD4 = |V_{VID} - V_{BOOT}| x C_{SS} / 10uA

TD5 = 900us - TD4

Time Delay (T1 - T0) = 900us, TD3 = 900us are fixed delay and can not be adjusted externally.

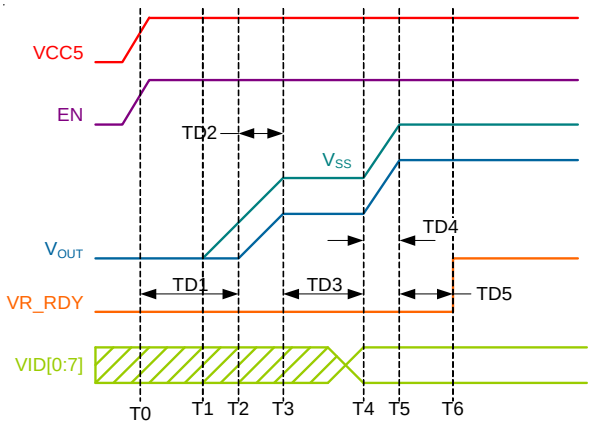


Figure 4. Soft Start Cycle of uP1608P/Q.

Channel Current Sensing

The uP1608P/Q extracts phase currents for current balance and over current protection by parasitic on-resistance of the lower switches when turn on as shown in Figure 6. The ISEN1/2/3/4 pins sense the corresponding phase current when the low side MOSFETs are turned on.

$$I_{SENX} = ((I_{PHX} \times R_{DS(ON)}) + V_{DC}) / R_{SENX}$$

where I_{SENX} is the sampled and held phase current signal, I_{PHX} is phase current, $R_{DS(ON)}$ is the on-resistance of the low side MOSFETs, and V_{DC} is 30mV offset voltage for the current balance circuit. The current balance circuit increases the duty cycle of the phase whose phase current is smaller than others and decrease the duty cycle of the phase whose phase current is larger than others.

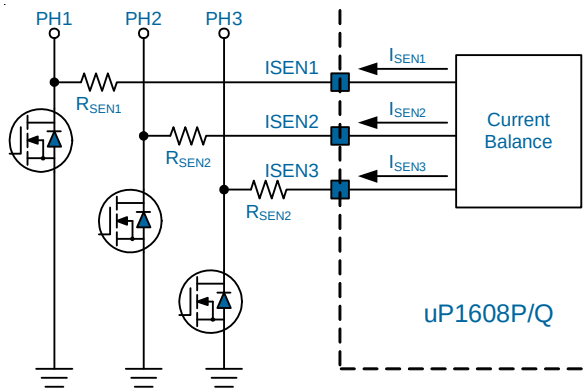


Figure 6. Phase Current Sensing and Current Balance.

Functional Description

Select R_{SENX} to set the current balance gain. A rule of thumb is to keep I_{SENX} = 30uA at rated output current.

Output Over Current Protection

I_{AVG} is mirrored and injected to the IMAX pin and create a voltage V_{IMAX} at IMAX pin.

$$V_{IMAX} = K \times R_{IMAX} \times I_{AVG} = \frac{K \times R_{IMAX} \times I_{OUT} \times DCR}{P \times R_{CSN}}$$

where K is the current mirror gain (uP1608P: K = 3 for three phase operation, K = 4 for four phase operation; uP1608Q: K = 4 for 1/2 phase operation). The over current protection is activated and shuts down the uP1608P/Q if the IMAX voltage is higher than 1.2V.

Output Over Voltage Protection

The OVP is activated and turns on the low side MOSFETs if (V_{FB} - V_{DAC}) > 160mV

The uP1608P/Q turns on the lower gate drivers when OVP is detected. The over voltage protection is latch-off and can only be reset by POR or toggling the EN pin.

Under Voltage Protection

The under voltage protection is activated if FB voltage V_{FB} is lower than 200mV. The uP1608P/Q turns off both higher and lower gate drivers when UVP is tetected. The under voltage protection is latch-off and can only be reset by POR or toggling the EN pin.

Power Saving Mode and Automatic Phase Reduction

The uP1608P/Q sources a 10uA current source out of PS1 and PS2 pins. Connecting resistors R_{PS1} and R_{PS2} at PS1 and PS2 pins creates voltage levels V_{PS1} and V_{PS2} for power saving mode operation.

V_{PS1} = 10uA x R_{PS1}

V_{PS2} = 10uA x R_{PS2}

Table 3 shows the operation phase of uP1608P/Q according to V_{IMAX}, V_{PS1}, V_{PS2} and PWM4 status. Take PWM4 = VCC5, V_{PS1} = 0.2V, V_{PS2} = 0.3V and V_{IMAX} = 0.25V for example, the uP1608P/Q turns off phase 2 and operates the converter in 2-phase. Note that the uP1608P/Q do not reset the clock sequence during dynamic phase reduction. Phase 1 and phase 3 still has 240° phase shift.

The automatic phase reduction reduces the switching and conduction losses at light load condition and enables high efficiency over a wide range of output current.

R_{PS2} > R_{PS1} and V_{PS2} > 0.22V are required when programming the phase-reduction threshold level.

Do not let PS1 > 0.8V and PS2 < 0.07V simutantaneously as it will lead to unknown status.

Table 3. Operation Phase Selection.

uP1608P		
3 Phase Configuration, PWM4 connect to VCC5		
Forced 1 Phase Operation	PS2 < 0.07V PS1 < 0.8V	1 Phase (1)
Forced 3 Phase Operation	PS1 > 0.8V PS2 > 0.22V	3 Phase (1, 2,3)
Auto PSI Mode	PS1 < V_{IMAX} PS2 < V_{IMAX}	3 Phase (1, 2,3)
	PS1 < V_{IMAX} PS2 > V_{IMAX}	2 Phase (1, 3)
	PS1 > V_{IMAX} PS2 > V_{IMAX}	1 Phase (1)
	PS1 > V_{IMAX} PS2 < V_{IMAX}	2 Phase (1, 2)
4 Phase Configuration, PWM4 connect to pre-driver		
Forced 1 Phase Operation	PS2 < 0.07V PS1 < 0.8V	1 Phase (1)
Forced 4 Phase Operation	PS1 > 0.8V PS2 > 0.22V	4 Phase (1, 2, 3, 4)
Auto PSI Mode	PS1 < V_{IMAX} PS2 < V_{IMAX}	4 Phase (1, 2, 3, 4)
	PS1 < V_{IMAX} PS2 > V_{IMAX}	2 Phase (1, 3)
	PS1 > V_{IMAX} PS2 > V_{IMAX}	1 Phase (1)
	PS1 > V_{IMAX} PS2 < V_{IMAX}	3 Phase (1, 2, 4)
uP1608Q		
Forced 2 Phase Operation	PS1 > 0.8V	2 Phase (1, 2)
Auto PSI Mode	PS1 > V_{IMAX} 1 Phase (1) PS1 < V_{IMAX} 2 Phase	2 Phase (1, 2)

Temperature Monitoring

The uP1608P/Q monitors the converter temperature at TM pin as shown if Figure 7. VR_HOT is activated if V_{TM} < 28% of VCC5 and sets the VR_HOT pin high impedance. VR_HOT is pulled low if V_{TM} > 33% of VCC5.

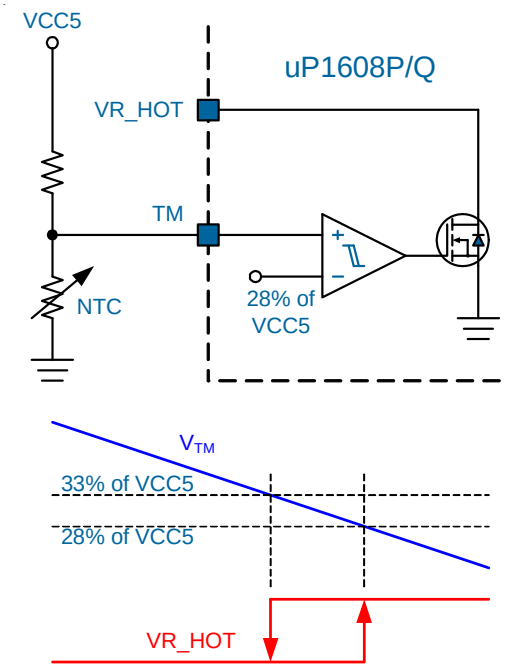


Figure 7. Temperature Monitoring of uP1608P/Q.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC12A/B ---------- -0.3V to +15V
BOOTx to PHx ---------- -0.3V to +15V
PHx to GND
- DC ---------- -0.7V to 15V
- < 200ns ---------- -8V to 30V

BOOTx to GND
- DC ---------- -0.3V to VCC12A/B + 15V
- < 200ns ---------- -0.3V to 42V

UGx to PHx
- DC---------- -0.3V to (BOOTx - PHx +0.3V)
- <200ns ---------- -5V to (BOOTx - PHx + 0.3V)

LGx to GND
- DC ---------- -0.3V to + (VCC12A/B + 0.3V)
- <200ns ---------- -5V to VCC12A/B + 0.3V

Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- VQFN6x6 - 48L θ_{JA} ---------- 35°C/W
- VQFN5x5 - 40L θ_{JA} ---------- 36°C/W
- VQFN6x6 - 48L θ_{JC} ---------- 3°C/W
- VQFN5x5 - 40L θ_{JC} ---------- 3°C/W

Power Dissipation, P_D @ T_A = 25°C
- VQFN6x6 - 48L ---------- 2.86W
- VQFN5x5 - 40L ---------- 2.78W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +150°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, $V_{CC12A/B}$ ---------- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC12 = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC12}		10.8	12.0	13.2	V
Supply Current	I_{CC12}	UGx and LGx Open; Switching	2	4	7	mA
Supply Input Voltage	V_{CC5}		4.5	5.0	5.5	V
Supply Current	I_{CC5}		2	4	6	mA
VCC12A POR Threshold	$V_{CC12RTH}$	V_{CC12A} Rising.	8.5	9.5	10.5	V
VCC12A POR Hysteresis	$V_{CC12HYS}$		0.7	1.0	1.3	V
VCC5 POR Threshold			3.7	4.1	4.4	V
VCC5 POR Hysteresis			0.35	0.50	0.65	V
Soft Start						
Soft Start Current	I_{SS}	V_{SS} = 0V	9.1	10.4	11.7	uA
VID on the Fly Maximum Current	I_{SS}		140	165	190	uA
Feedback Return						
Leakage of FBRTN			--	--	200	uA
Thermal Management						
VR_HOT Threshold Level			26	28	30	$\%V_{CC5}$
VR_HOR Hysteresis			2	5	7	$\%V_{CC5}$
Enable Control						
Logic Low Threshold	V_{IL}		--	--	0.4	V
Logic High Threshold	V_{IH}		0.8	--	--	V
Oscillator						
Switching Frequency	f_{OSC}	R_{RT} = 24kΩ, for 4 phase operation (uP1608P)	270	300	330	kHz
		R_{RT} = 33kΩ, for 3 phase operation (uP1608P)	270	300	330	kHz
		R_{RT} = 24kΩ, for 1/2 phase operation (uP1608Q)	270	300	330	kHz
Adjustable Frequency Range			100	--	1000	kHz
Ramp Amplitude		Guaranteed by Design	3.5	4	4.5	V
Maximum Duty		3 Phase Operation (uP1608P) Guaranteed by Design	80	87	95	%
		4 Phase Operation (uP1608P) Guaranteed by Design	85	90	95	
		1/2 Phase Operation (uP1608Q) Guaranteed by Design	85	90	95	
RT Pin Voltage	V_{RT}		0.95	1.00	1.05	V

Electrical Characteristics

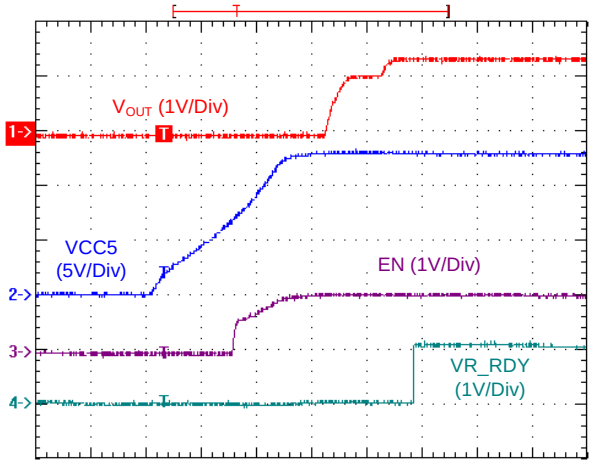
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage and DAC						
DAC Accuracy	V_{FB}	0.5V to 0.8V	-10	--	10	mV
		0.8V to 1.0V	-8	--	8	
		1.0V to 1.6V	-0.5	--	0.5	%
DAC Input Logic Low Threshold	V_{IL}		--	--	0.4	V
DAC Input Logic High Threshold	V_{IH}		0.8	--	--	V
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF.	30	--	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	1400	1800	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	300	360	--	uA
Current Sense						
Maximum Sourcing Current			100	--	--	uA
Input Offset Voltage			-1	0	1	mV
IMAX Current Mirror Accuracy		I_{IMAX}/I_{AVG}, 3 phase operation (uP6108P)	279	300	321	%
		I_{IMAX}/I_{AVG}, 4 phase operation (uP6108P)	372	400	428	%
		I_{IMAX}/I_{AVG}, 1/2 phase operation (uP6108Q)	372	400	428	%
Droop Current Mirror Accuracy		I_{DRP}/I_{AVG}, 3 phase operation (uP6108P)	279	300	321	%
		I_{DRP}/I_{AVG}, 4 phase operation (uP6108P)	372	400	428	%
		$I_{DRP/}I_{AVG}$, 1/2 phase operation (uP6108Q)	372	400	428	%
I_{SENx} Voltage	V_{DC}	R_{SENx} = 1kΩ	25	33	45	mV
Power Saving Mode						
PS1/PS2 Soucing Current	I_{PSX}	R_{PS1} = R_{PS2} = 47k	9	10	11	uA
V_{PS2} Exit Force 1 Phase		T_A = 25°C	--	--	180	mV
		T_A = 125°C	--	--	190	mV
V_{PS1} Force Full Phase			0.77	0.80	0.83	V
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	2	4	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	1	2	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	2	4	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.8	1.6	Ω
Dead Time	T_{DT}		--	30	--	ns

Electrical Characteristics

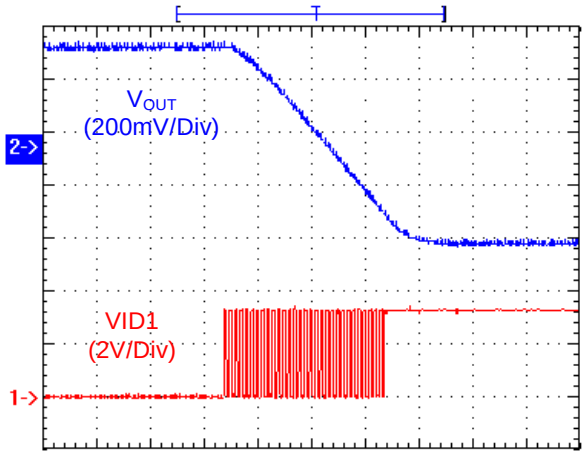
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection						
Total Curren Protection Threshold	V_{IMAX}		1.1	1.2	1.3	V
Total Curren Protection Threshold Delay Time			5	--	30	us
FB Over Voltage Protection		V_{FB} - V_{DAC}	130	160	190	mV
FB Over Voltage Protection Delay Time			80	--	150	us
FB Under Voltage Protection	V_{FB}		150	200	250	mV
FB Under Voltage Protection Delay Time			1	--	5	us
Over Temperature Protection Threshold		Guaranteed by Design	145	160	175	^{O}C
Over Temperature Protection Hysteresis			5	20	35	^{O}C
Output Pin Capability						
VRHOT Sinking Capability	V_{HOT}	I_{HOT} = 4mA.	--	0.05	0.2	V
VR_RDY Sinking Capability	V_{RDY}	I_{RDY} = 4mA.	--	0.05	0.2	V

Typical Operation Characteristics

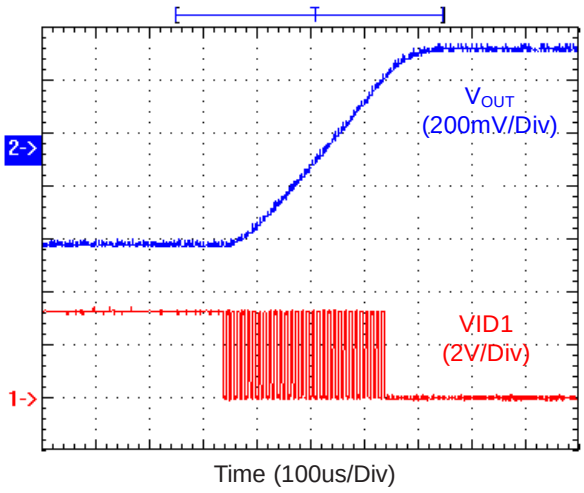
Power On Sequence



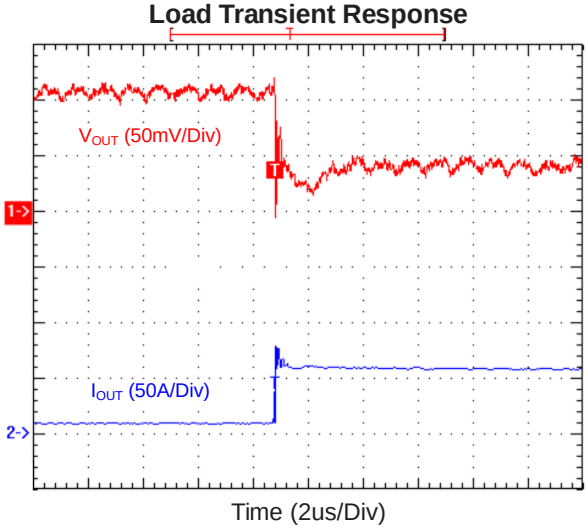
DVID Falling



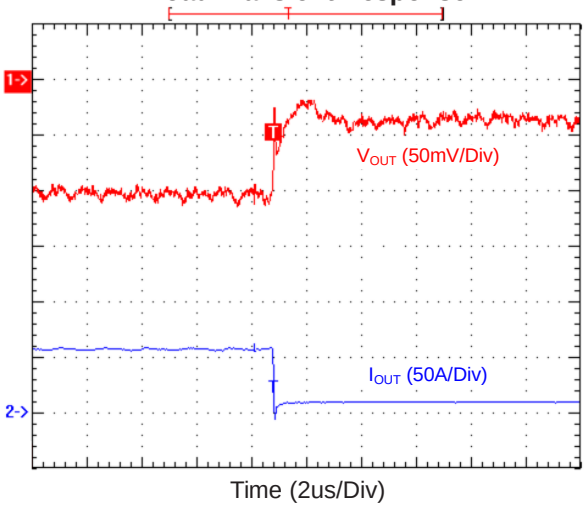
DVID Rising



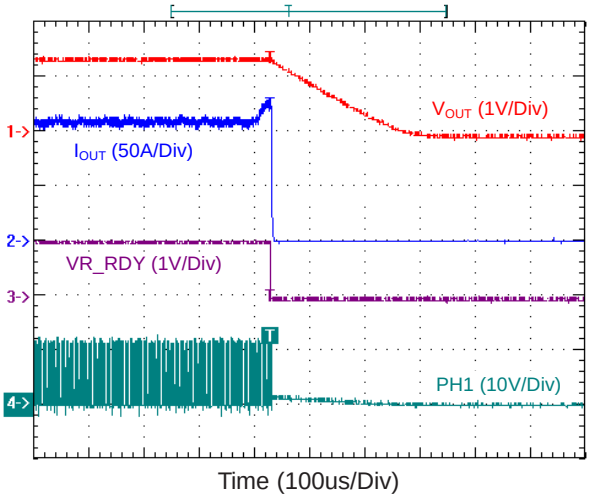
Load Transient Response



Load Transient Response



Over Current Protection



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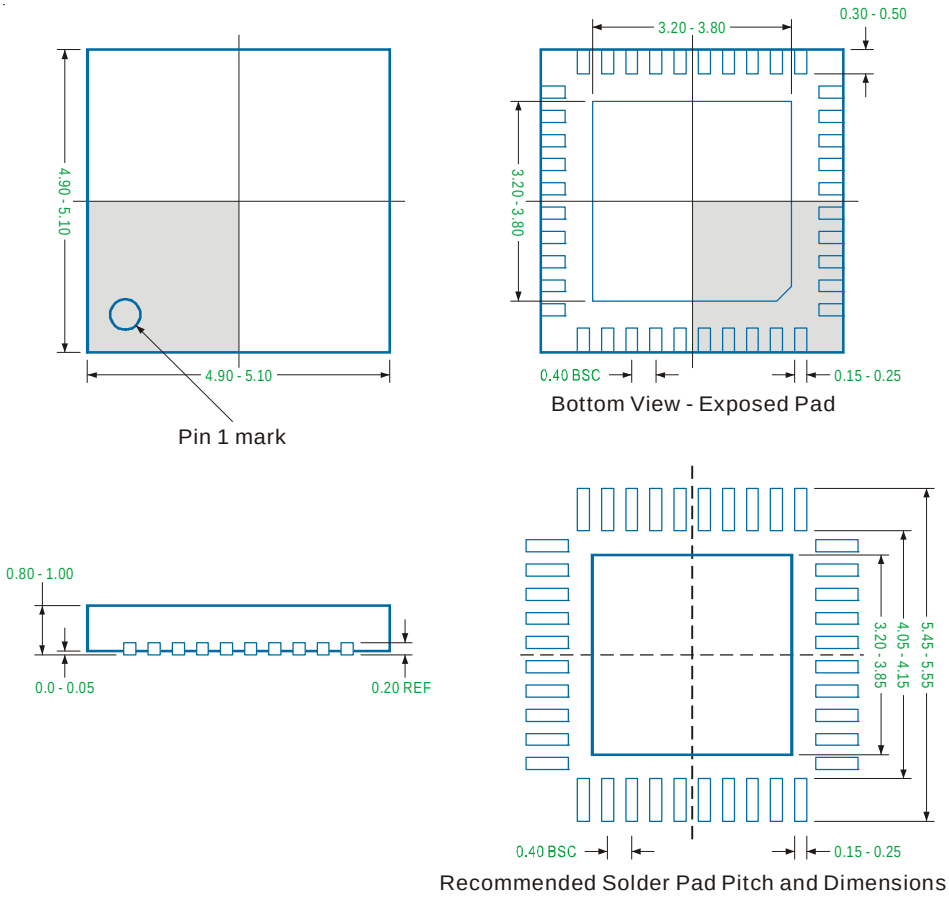
Package Information

VQFN5x5 - 40L Package

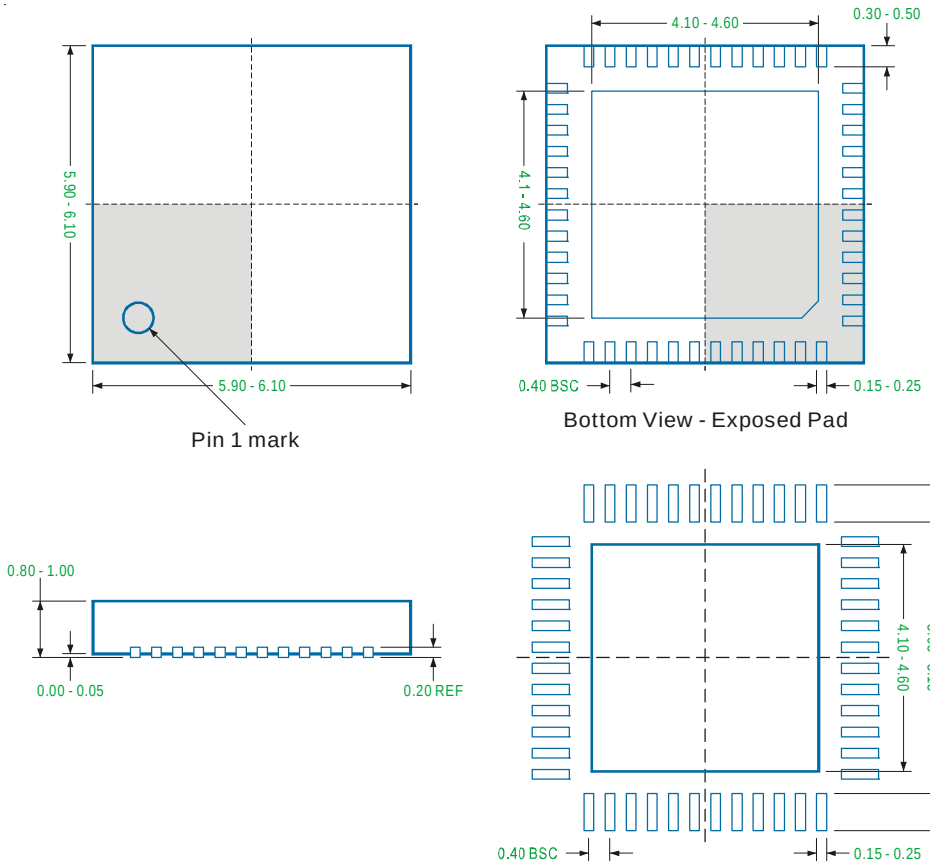


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

VQFN6x6 - 48L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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