Compact Dual-Phase Synchronous-Rectified Buck Controller

General Description

The uP6201A/B is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current thanks to its embedded bootstrapped drivers that support 12V + 12V driving capability. The uP6201A/B features configurable gate driving voltage for maximum efficiency and optimal performance. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to internal 0.6V or external reference voltage from 0.4V to 2.5V. The uP6201A/B adopts DCR current sensing technique for channel current balance, over current protection, droop control, and output current indication. The uP6201A/B offers a regulated 5V voltage with 20mA output current capability for other peripheral circuitry.

A MODE pin programs single- or two- phase operation making the uP6201A/B ideally suitable for dual power input applications like PCIE interfaced graphic cards.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation function, quick response to step load transient, and power OK. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes to QFN4x4-24L package.

Ordering Information

Order Number	Package Type	Remark
uP6201AQ	QFN 4x4-24L	Wtih Droop Function
uP6201BQ	QFN 4x4-24L	Without Droop Function

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

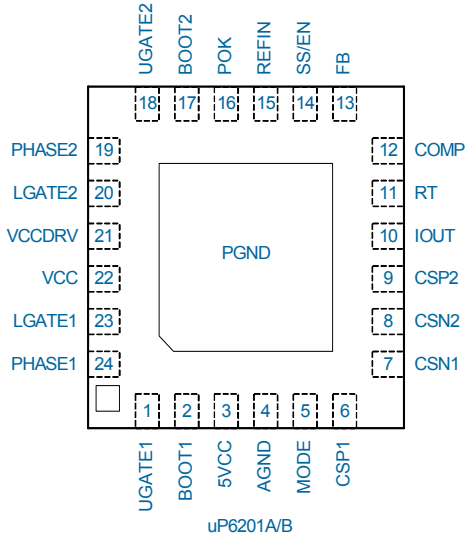
Features

- Operate with 4.5V ~13.2V Supply Voltage
- Selectable External or Internal 0.6V Reference
- Support Single- and Two- Phase Operation
- 5VCC with 20mA Output Current Capability
- ±2.0% Over Line Voltage and Temperature
- Simple Single-Loop Voltage-Mode Control
- 12V Bootstrapped Drivers with Internal Bootstrap Diode
- DCR Current Sensing
- Adjustable Operation Frequency form 50kHz to 1MHz Per Phase
- External Compensation
- Adjustable Over Current Protection and Output Current Indication
- External Reference
- Adjustable Soft Start
- QFN4x4-24L Package
- RoHS Compliant and 100% Lead (Pb)-Free

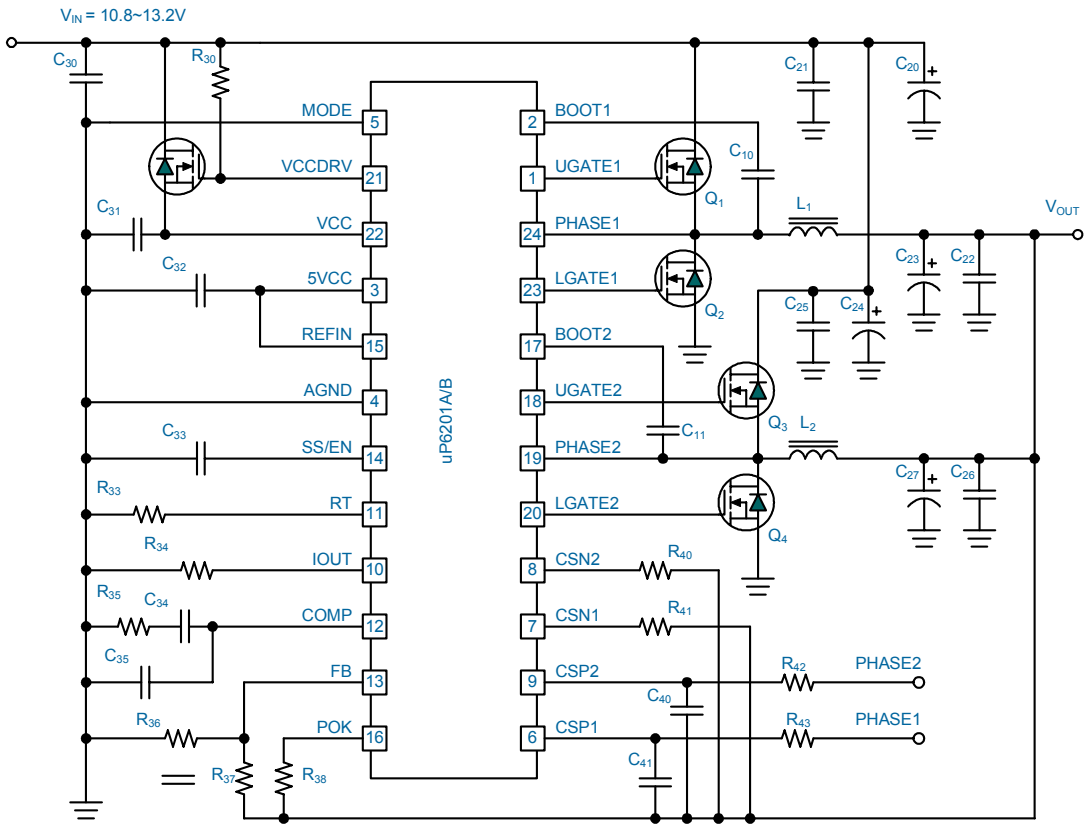
Applications

- Middle-High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules

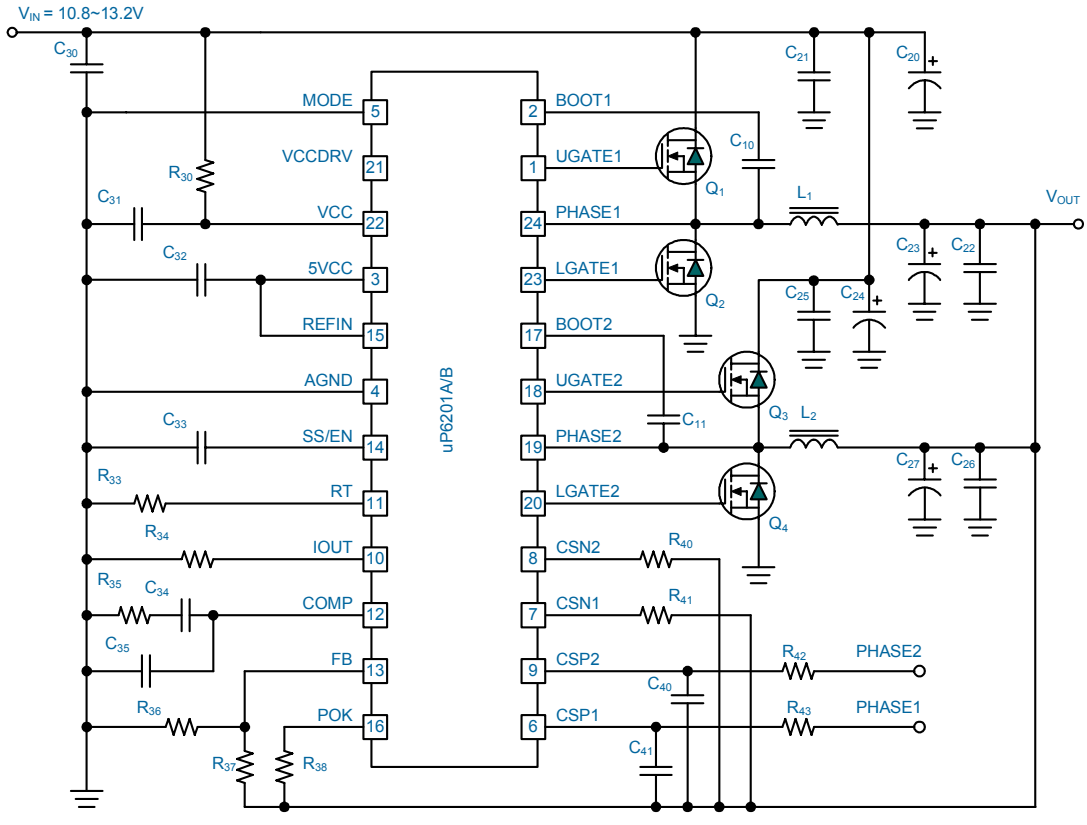
Pin Configuration



Typical Application Circuit

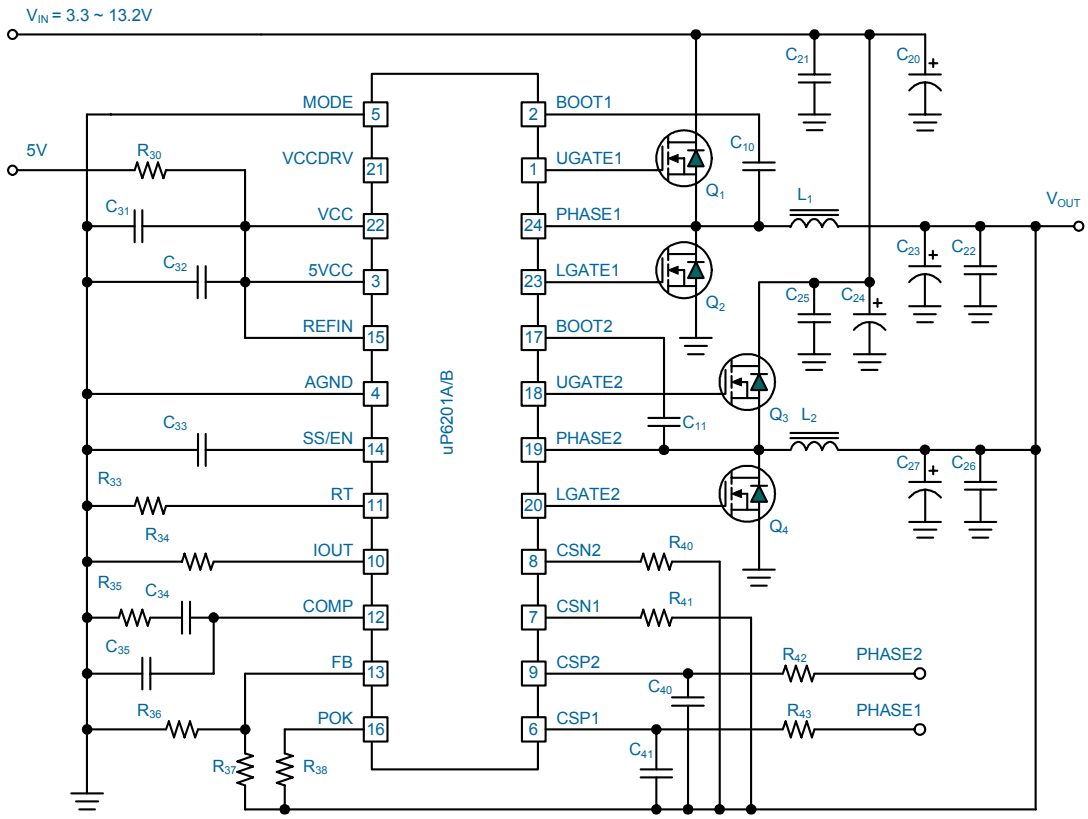


A. 9V Drive Using External Regulator



B. 12V Drive

Typical Application Circuit



C. 5V Drive

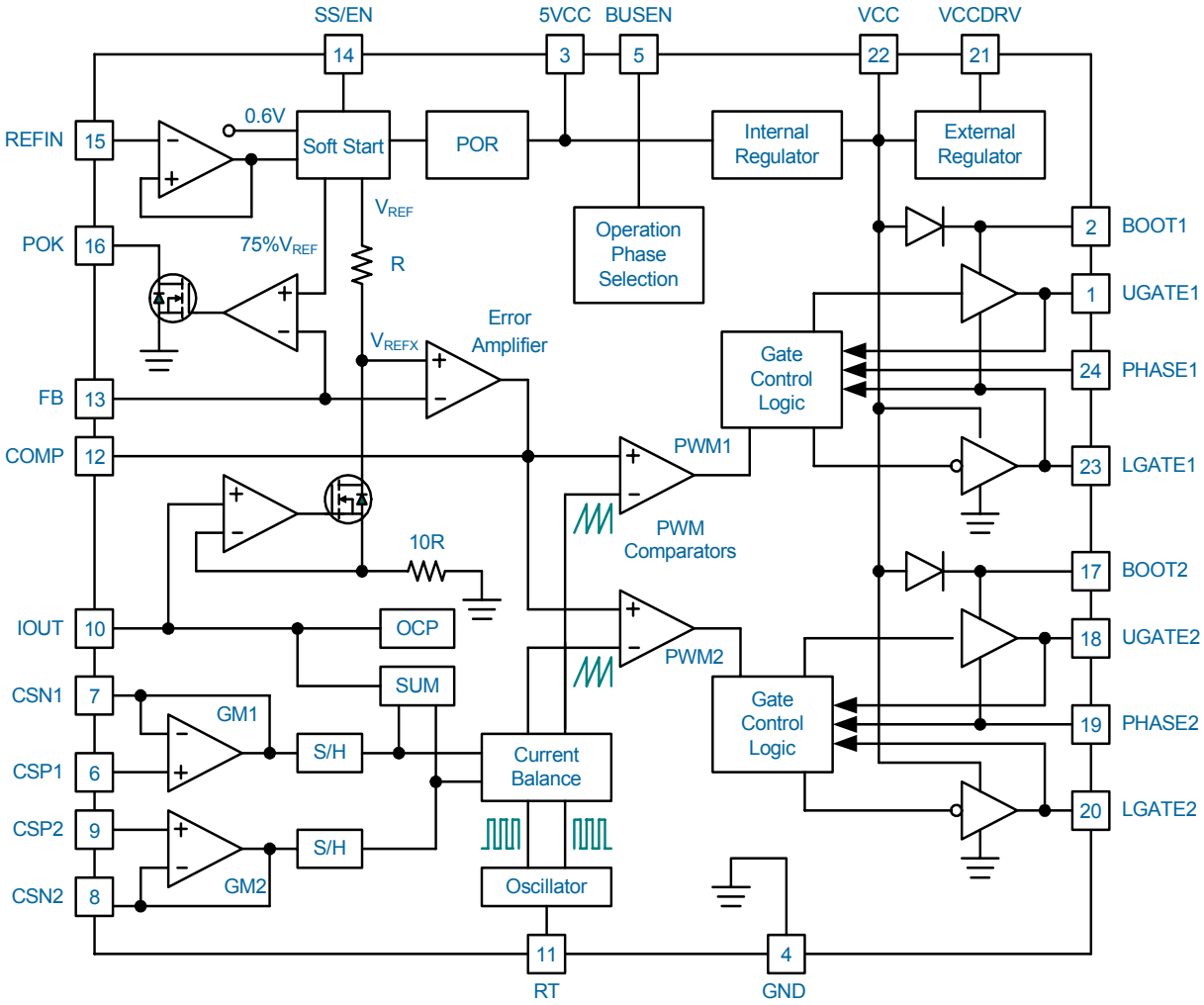
Functional Pin Description

No.	Pin Name	Pin Function
1	UGATE1	**Upper Gate Driver Output for Channel 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
2	BOOT1	**Bootstrap Supply** for the floating upper gate driver of channel 1. Connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
3	5VCC	**Internal Regulator Output.** This is the output pin of linear regulator for internal bias and external usage. The output current capability is 20mA.
4	AGND	**Signal Ground for the IC.** All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
5	MODE	**Operation Phase Selection.** Pulling this pin lower than 0.4V sets two-phase operation. Pulling this pin higher than 1.4V sets single-phase operation and disables phase2. Once operated in single-phase mode, the operation mode is latched. It is required to toggle SS/EN or 5VCC pin to reset the IC.
6	CSP1	**Positive Input of Current Sensing GM1.** This pin companied with CSN1 senses the inductor current of channel 1 through an RC network.
7	CSN1	**Negative Input of Current Sensing GM1.** This pin companied with CSP1 senses the inductor current of channel 1 through an RC network.
8	CSN2	**Negative Input of Current Sensing GM2.** This pin companied with CSP2 senses the inductor current of channel 2 through an RC network.
9	CSP2	**Positive Input of Current Sensing GM2.** This pin companied with CSN2 senses the inductor current of channel 2 through an RC network.
10	IOUT	**Output Current Indication.** This pin indicates the output current level. Connect this pin with resistor to ground to set the coefficient of the output current indication. The resistor also decide the output impedance of droop control (uP6201A Only)
11	RT	**Operation Frequency Setting.** Connecting a resistor between this pin and AGND to set the operation frequency.
12	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
13	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to AGND is used to set the regulation voltage. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
14	SS/EN	**Soft Start Output.** Connect a capacitor from this pin to AGND to set the soft start interval. Pulling low this pin down to 0.5V shuts down the uP6201A/B.
15	REFIN	**External Reference Input.** This is input pin of external reference voltage. If external reference voltage is not available, connect this pin to 5VCC for internal 0.6V reference.
16	POK	**Power OK Indication.** POK is an open drain output used to indicate the status of the voltages on SS pin and FB pin. POK will go high impedance if V_{FB}> 075% of reference voltage after soft start ends.

Functional Pin Description

No.	Pin Name	Pin Function
17	BOOT2	**Bootstrap Supply** for the floating upper gate driver of channel 2. Connect the bootstrap capacitor between BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
18	UGATE2	**Upper Gate Driver Output for Channel 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
19	PHASE2	**Switch Node for Channel 2.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
20	LGATE2	**Lower Gate Driver Output for Channel 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
21	VCCDRV	**Driver for External Linear Regulator.** This pin is the drive output for that external linear regulator. Connect this pin to the base/gate of NPN/NMOS transistor as the pass element.
22	VCC	**Supply Voltage.** This pin along with VCCDRV pin and external pass element provides a regulated 8V bias supply for the uP6201A/B, the lower gate drivers, and the bootstrap circuit for upper drivers. This pin can receive a well-decoupled 4.5~13.2V supply voltage alone if the VCCDRV pin is left open. Ensure that this pin is bypassed by a ceramic capacitor next to the IC.
23	LGATE1	**Lower Gate Driver Output for Channel 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
24	PHASE1	**Switch Node for Channel 1.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
Exposed Pad	PGND	**Power Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Block Diagram



uP6201A

Functional Description

The uP6201A/B is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current thanks to its embedded bootstrapped drivers that support 12V + 12V driving capability. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to internal 0.6V or external reference voltage from 0.4V to 2.5V. The uP6201A/B adopts DCR current sensing technique for channel current balance, over current protection, droop control, and output current indication. The uP6201A/B offers 5VCC with 20mA output current capability for other peripheral circuitry.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include internal soft start, adjustable operation function, quick response to step load transient, power OK and external reference input. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes QFN 4x4_24L package.

External VCC and Internal 5VCC Regulator

The uP6201A/B provides flexible gate driving voltage for maximum efficiency and optimal performance. The VCC pin powers the uP6201A/B control circuit, the lower gate drivers and the bootstrap circuit for the higher gate drivers. A linear regulator regulates V_{CC} at 9V as shown in Figure 1. Connect VCCDRV pin to the base/gate of the external NPN/NMOS transistor and VCC pin to the emitter/source to form a linear regulator. Ensure that the ceramic bypass capacitor is placed next to the IC.

An internal linear regulator regulates VCC input to a 5VCC voltage for internal control logic circuit if VCC is higher than 7V. This linear regulator is designed to support up to 20mA output current for peripheral circuits. Place an 1uF ceramic capacitor next to the 5VCC pin to decouple this voltage.

Figure 2 shows the application where 12V gate voltage is used. When VCCDRV is left open, VCC pin can receive a well decoupled supply input of 4.5~13.2V. However, if V_{IN} is lower than 5.5V, the dropout voltage of the internal regulator may cause 5VCC too low for normal operation. Tie 5VCC to VCC directly for the applications where VCC is under 5.5V as shown in Figure 3.

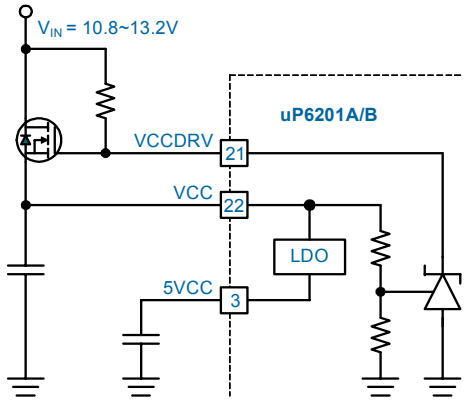


Figure 1. 9V Drive Application

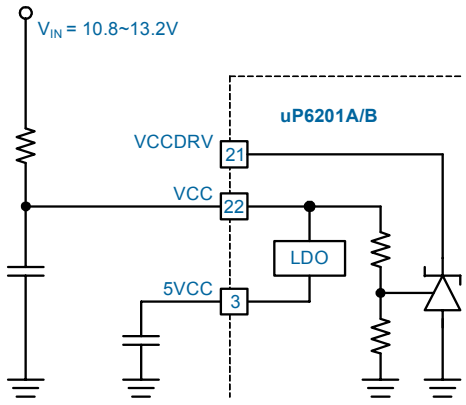


Figure 2. 12V Drive Application

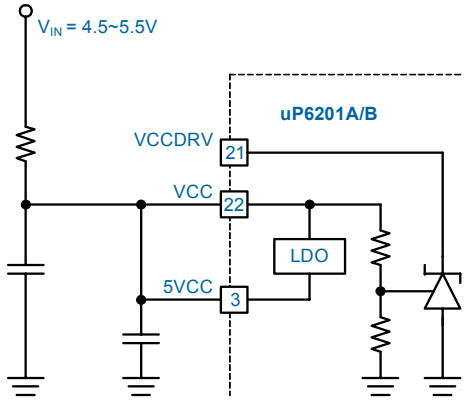


Figure 3. 5V Drive Application

Bootstrap diodes are embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required. The uP6201A/B integrates MOSFET gate drives that are powered from the VCC pin and support 12V+12V driving capability. Converters that consist of uP6201A feature high efficiency without special consideration on the selection of MOSFETs.

Functional Description

Note that the built-in bootstrapping diode is not a Schottky diode having higher forward bias voltage. When using 5V driving voltage, external Schottky diode is recommended for bootstrapping diode.

Power On Reset and Initialization

The uP6201A/B continuously monitors 5VCC for power on reset (POR) to ensure the supply voltage is high enough for normal operation of the device. The POR threshold level is typically 4.2V at 5VCC rising.

Operation Phase Selection

The uP6201A/B supports single- or two- phase operation. Pulling the MODE pin lower than 0.4V sets two-phase operation. Pulling the MODE pin higher than 1.4V sets single-operation. Once operated in single-phase mode, the operation phase is latched and can only be reset by toggle 5VCC or SS/EN pin. This feature is important for PCIE interfaced graphic cards where neither bus power nor external power is capable of delivering full load current.

Configure the converter as shown in Figure 4. Power the phase 1 converter by PCIE bus power and power the phase 2 converter by external power. If the external power code is not plugged into the socket, the External Power Detection will set MODE pin high and the uP6201A/B operates in single phase mode. The uP6201A/B could provides limited current to GPU for required operation when external power is not plugged.

Two-phase operation will making the phase 2 converter acts like an boost converter if the external power is not available, boosting the output voltage to the input voltage. The relationship between input voltage and output voltage is governed by conventional boost converter equation. Offset of the current balance function may make the duty cycle of phase 2 converter smaller than that of phase 1 converter. This results in external power higher than 15V that may damage the input capacitors and other devices. Figure 4 configuration turns off phase 2 converter when the external power is not available, thus eliminates the possibility of over voltage on input capacitors and other devices of the phase 2 converter.

Note that when operated in single phase, the rated current is reduced to one half of normal level. Continuous demanding high current may damage the converter.

Reference Voltage Selection

The uP6201A/B features selectable internal or external reference voltage. The REFIN voltage level is checked at POR to select the desired reference voltage. Internal 0.6V reference voltage is selected if $V_{REFIN} > V_{CC5} - 0.8V$ at POR, otherwise external reference voltage is selected. Once selected, the reference source is fixed and can only be programmed at next POR.

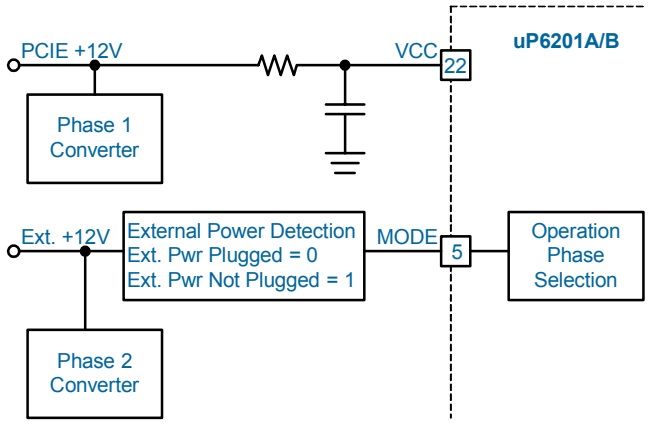


Figure 4. Single/Two Phase Operation

Tie REFIN voltage to 5VCC to select internal reference when POR. If the external reference voltage is higher than 2.5V before POR, it may cause uP6201A/B to select internal 0.6V reference voltage and should be avoided.

Oscillation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency as:

$$f_{OSC} = \frac{10000}{R_{RT}(k\Omega)} \quad (kHz)$$

Figure 5 shows the relationship between oscillation frequency and R_{RT}.

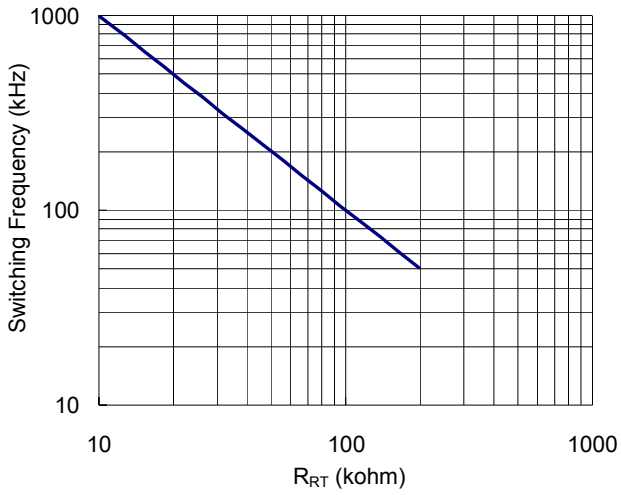


Figure 5. Switching Frequency vs. R_{RT}.

Soft Start and Power OK

Once POR releases, the uP6201A/B initiates its soft start cycle. Figure 6 shows the softstart cycle with external reference voltage. A 10uA current charges the soft start capacitor C_{SS} making its voltage V_{SS} linearly ramp up. The V_{SS} clamps reference voltage V_{REF} with a MOSFET threshold voltage at non-inverting input of the error amplifier. Accordingly, the output voltage will softly ramp up and draw minimum inrush current from the power bus.

The uP6201A/B features pre-bias start-up capability. If the output voltage is pre-biased with a voltage, say V_{BIAS}, that accordingly makes V_{FB} higher than reference voltage ramping V_{REF}. The error amplifier keeps V_{COMP} lower than the valley of the sawtooth waveform and makes PWM comparators output low until the ramping V_{REF} catches up the feedback voltage. The uP6201A/B keeps both upper and lower MOSFETs off until the first pulse takes place.

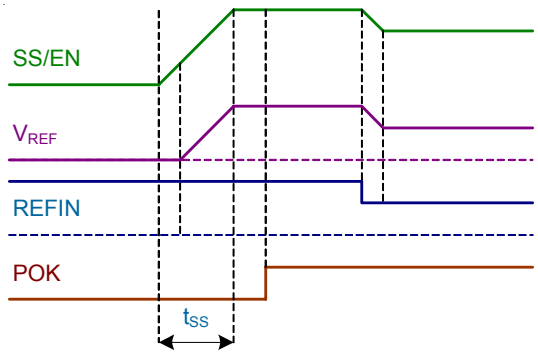


Figure 6. Timing Diagram of Soft Start Interval.

The uP6201A/B claims soft start end when V_{REF} catches up V_{REFIN} and set POK to high impedance output if no fault conditions are detected. The total soft start time with external reference voltage is about

$$t_{SS} = \frac{C_{SS}(V_{REFIN} + 0.8V)}{10uA}$$

where 0.8V accounts for the delay time caused by the MOSFET threshold voltage. When internal 0.6V reference voltage is used, simply take V_{REFIN} = 0.6V into the above equation.

When external reference voltage changes, the slew rate of V_{REF} is also limited by the soft start mechanism. Consequently, this results in a smooth output voltage transition during external reference voltage change. The soft start also acts as the timer during OCP and UVP as described in the later sections.

Channel Current Sensing

The uP6201A/B extracts phase currents by parasitic DCR of the inductors for channel current balancing, droop tuning, and over current detecting. An RC network is paralleled to the inductor for current sensing as shown in Figure 7 where DCR is the parasitic resistance. The V_C across the capacitor equals to $V_{DCR} = I_L$ x DCR across the DCR of the inductor if the time constants match: RC = L/DCR.

The GM amplifier will source a current source $I_{CSN} = V_C / R_{CSN}$ to virtually short its two inputs. Consequently I_{CSN} is sampled and held as:

$$I_{CSN} = \frac{DCR \times I_L}{R_{CSN}}$$

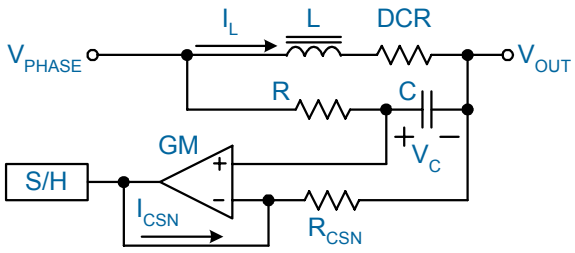


Figure 7. DCR Current Sensing Scheme

The sourcing capability of the GM amplifier is 100uA. It is recommended to scale $\boldsymbol{I_{CSN} = 30uA}$ at rated inductor current. Take a 60A converter for example. Assume DCR = 2mΩ, select the sense resistor according to

$$R_{CSN} = \frac{30A \times 2m\Omega}{30uA} = 2.0k\Omega$$

Current Balance

The uP6201A/B fine tunes the duty cycle of each channel for current balance according to the sensed inductor current signals. If the current of channel 1 is smaller than the current of channel 2, the uP6201A/B increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice verse.

Over Current Protection

The sensed current signals are monitored for over current protection. The uP6201A/B features both total current OCP and phase current OCP. If I_{CSN1} or I_{CSN2} is higher than 80uA, the phase current OCP is activated. If $I_{CSN1} + I_{SCN2}$ is higher than 120uA, total current OCP is activated.

The uP6201A/B features hiccup and shutdown mode OCP. If OCP takes place after soft start end, the uP6201A/B turns off both upper and lower MOSFETs and discharges the C_{SS} with a constant current of 10uA. When V_{SS} touches down 0.4V, the uP6201A/B initiates another soft start cycle. The uP6201A/B shuts down after 4 times hiccups. If the OCP takes place during soft start cycle, the uP6201A/B turns off both upper and lower MOSFETs but keeps charging the C_{SS} with a constant current of 10uA until the soft start end.

Functional Description

The shutdown status can only be reset by POR function. Figure 8, and Figure 9 illustrate the OCP behaviors during soft start and after soft start end respectively.

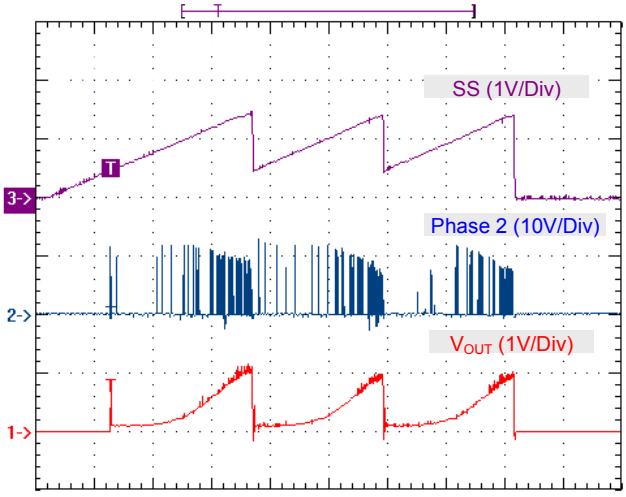


Figure 8. OCP during Soft Start

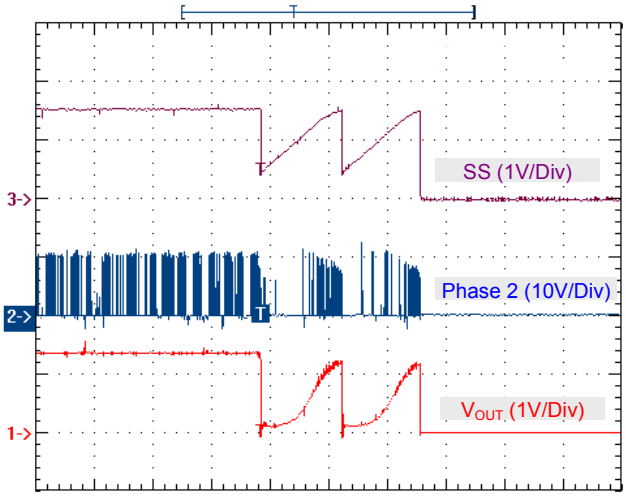


Figure 9. OCP after Soft Start End.

Output Current Indication

The sensed current signals are summed and injected into the IOUT pin for output current indication. A resistor R_{IOUT} connected to this pin scales the voltage V_{IOUT} proportional to the output current:

$$V_{IOUT} = \frac{DCR \times I_{OUT}}{2 \times R_{CSN}} \times R_{IOUT}$$

Droop Tuning (uP6201A Only)

The IOUT pin also adjusts the load line for droop control as shown in Figure 10. The V_{REF} is the internal 0.6V or external reference voltage as described in the relative sections. The V_{REFX} is the real reference voltage at the non-inverting input of the error amplifier. The two well-matched Rs share the same current and see same voltage drop that is exactly V_{IOUT}. Consequently,

$$V_{REFX} = V_{REF} - \frac{V_{IOUT}}{10}$$

$$V_{REFX} = V_{REF} - \frac{DCR \times I_{OUT}}{2 \times R_{CSN}} \times \frac{R_{IOUT}}{10}$$

Finally,

$$V_{OUT} = \frac{R1+R2}{R2} \times V_{REF} - \frac{DCR \times R_{IOUT} \times (R1+R2)}{2 \times R_{CSN} \times R2} \times \frac{I_{OUT}}{10}$$

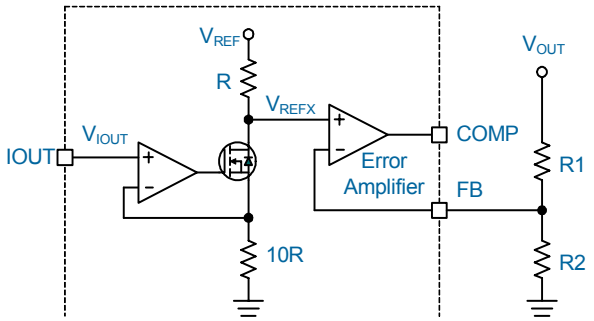


Figure 10. Load Line Setting

Absolute Maximum Rating

Supply Input Voltage, VCC (Note 1) ---------- -0.3V to +15V
VCCDRV ---------- -0.3V to +15V
PHASE to GND
DC ---------- -0.3V to 15V
< 200ns ---------- -5V to 30V
BOOT to PHASE ---------- 15V
BOOT to GND
DC ---------- -0.3V to PHASE +15V
< 200ns ---------- -0.3V to 42V
Input, Output or I/O Voltage ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
QFN4x4-24L θ_{JA} ---------- 40°C/W
Power Dissipation, P_D @ T_A = 25°C
QFN4x4-24L ---------- 2.5W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- +4.5V to +5.5V or 5.5V to 13.2V

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Voltage	V_{CC}		4.5	--	13.2	V
Supply Current	I_{CC}	UGATE and LGATE Open; V_{CC} = 12V, Switching	--	5	--	mA
Quiescent Supply Current	I_{CC_Q}	V_{FB} = 0.7V, No Switching, I_{CC5} = 0mA	--	4	--	mA
Regulated Supply Voltage	V_{CC}	V_{IN} = 12V, V_{FB} = 0.7 V, No Switching, I_{CC5} = 0mA	8	9	10	V
VCCDRV Sink Capability	I_{VCCDRV}	V_{IN} = 12V	4	--	--	mA
5VCC and Power On Reset						
5VCC Accuracy	V_{CC5}	V_{CC} = 12V, V_{FB} = 0.7 V, No Switching, I_{CC5} = 0mA	4.9	5.2	5.4	V
5VCC Maximum Output Current	I_{CC5_MAX}	V_{CC} = 12V, V_{FB} = 0.7 V, No Switching	20	--	--	mA
5VCC Tolerance	V_{CC5}	V_{CC} = 6.5V~13.2V, I_{CC5} = 0 ~ 20mA	4.5	--	5.5	V
POR Threshold	V_{CC5RTH}		--	4.0	4.4	V
POR Hysteresis	V_{CC5HYS}		--	0.2	--	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Soft Start						
Soft Start Current	I_{SS}	V_{CC} = 12V	8	10	12	uA
Re-Soft Start Threshold Level	V_{SS_HICCUP}		--	0.5	--	V
Operation Phase Selection						
MODE Rising Threshold Level	V_{MODE}	V_{CC} = 12V	1.4	--	--	V
MODE Falling Threshold Level	V_{MODE}	V_{CC} = 12V	--	--	0.4	V
MODE Pin Deglitch Time		From MODE = high to channel 2 disabled	2	6	10	us
Oscillator						
Free Running Frequency	f_{OSC}	R_{RT} = 33k	270	300	330	kHz
Frequency Variation			-10	--	10	%
Frequency Range			50	--	1000	kHz
Maximum Duty Cycle			85	90	95	%
Minimum Duty Cycle			--	0	--	%
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	2.5	--	V_{P-P}
Reference Voltage						
Nominal Feedback Voltage	V_{FB}	V_{CC} = 12V, V_{COMP} = 1.6V, V_{REFIN} = V_{CC5}, using internal 0.6V reference voltage	0.591	0.6	0.609	V
REFIN Range	V_{REFIN}		0	--	2.5	V
VREFIN Offset		$\lvert V_{REFIN} - V_{FB} \rvert$, V_{CC} = 12V, No Load, V_{REFIN} = 0.4~2.5V	--	--	10	mV
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	60	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	6	10	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	1200	1700	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	220	280	--	uA
Current Sense						
Maximum Sorcing Current	I_{CSN_MAX}		100	--	--	uA
GM Amplifier Offset	V_{OFFSET}	V_{CSP} = 0.8V, Connect a resistor R_{CSN} = 20kΩ from CSN to GND	-5	0	5	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Gate Driver (V_{CC} = 12V)						
Upper Gate Source	I_{UG_SRC}	V_{BOOT} - V_{PHASE} = 12V, V_{BOOT} - V_{UGATE} = 6V	--	-1.5	--	A
Upper Gate Sink	I_{UG_SNK}	V_{BOOT} - V_{PHASE} = 12V, V_{BOOT} - V_{UGATE} = 6V	--	2	--	A
Upper Gate Source	R_{UG_SRC}	V_{BOOT} - V_{PHASE} = 12V, V_{BOOT} - V_{UGATE} = 1V	--	3	6	Ω
Upper Gate Sink	R_{UG_SNK}	V_{UGATE} - V_{PHASE} = 1V	--	2	4	Ω
Lower Gate Source	I_{LG_SRC}	V_{CC} - V_{LGATE} = 6V	--	-1.5	--	A
Lower Gate Sink	I_{LG_SNK}	V_{LGATE} = 6V	--	2	--	A
Lower Gate Source	R_{LG_SRC}	V_{CC} - V_{LGATE} = 1V	--	3	6	Ω
Lower Gate Sink	R_{LG_SNK}	V_{LGATE} = 1V	--	2	4	Ω
PHASE Falling to LGATE Rising Delay		V_{CC} = 12V; V_{PHASE} < 1.2V to V_{LGATE} > 1.2V	--	30	--	ns
LGATE Falling to UGATE Rising Delay		V_{CC} = 12V; V_{LGATE} < 1.2V to (V_{UGATE} - V_{PHASE}) > 1.2V	--	30	--	ns
Dead Time	T_{DT}		--	30	--	ns
Minimum On Time		Pulse Width Static Operating		100	150	ns
Gate Driver (V_{CC} = 9V)						
Upper Gate Source	R_{UG_SRC}	V_{BOOT} - V_{PHASE} = 9V, V_{BOOT} - V_{UGATE} = 1V	--	3.3	6.6	Ω
Upper Gate Sink	R_{UG_SNK}	V_{UGATE} - V_{PHASE} = 1V	--	2.2	4.4	Ω
Lower Gate Source	R_{LG_SRC}	V_{CC} - V_{LGATE} = 1V	--	3.3	6.6	Ω
Lower Gate Sink	R_{LG_SNK}	V_{LGATE} = 1V	--	2.2	4.4	Ω
Protection						
Phase Over Current Protection Level	I_{CSN_OCP}	I_{CSN1} or I_{CSN2}	--	80	--	uA
Total Over Current Protection	I_{SUM_OCP}	I_{SUM} = I_{CSN1} + I_{CSN2}	--	120	--	uA
Over Temperature Protection			--	150	--	°C
Over Temperature Hysteresis			--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

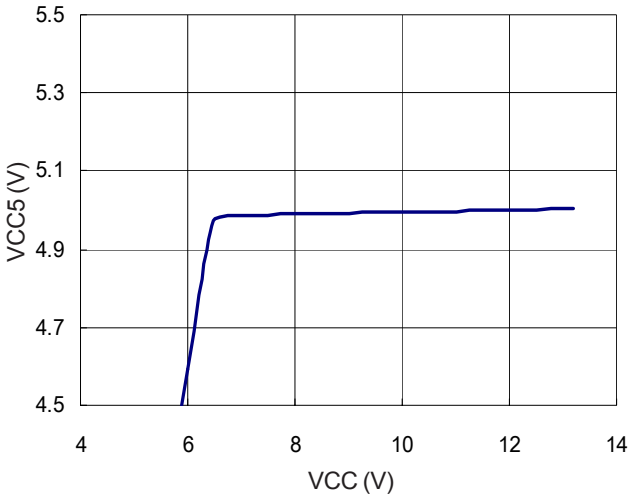
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

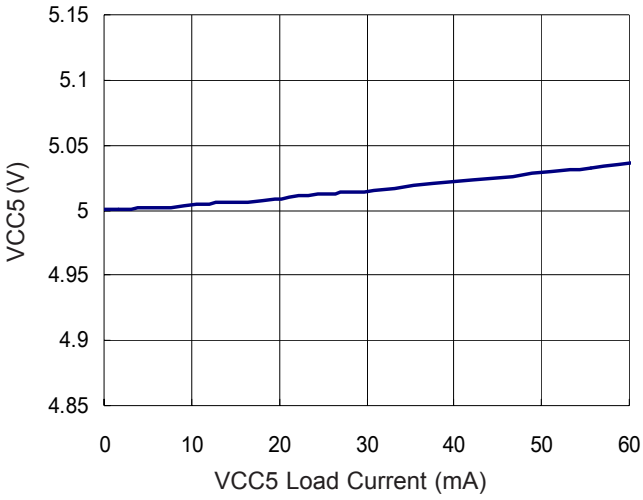
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

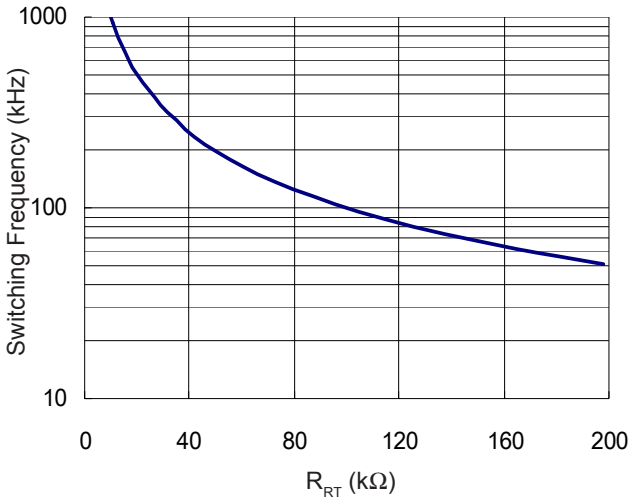
VCC5 Line Regulation



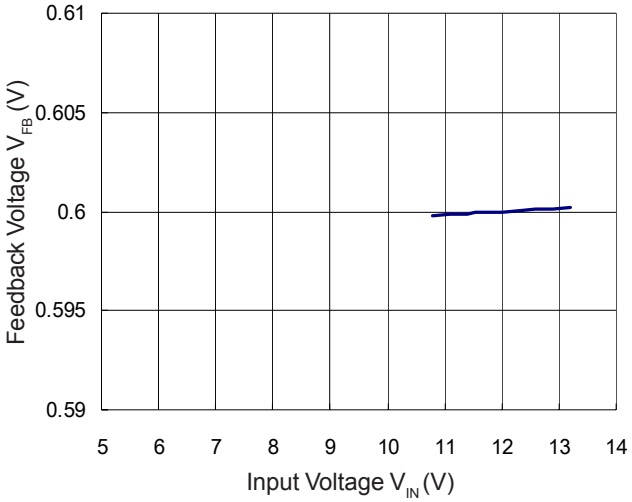
VCC5 Load Regulation



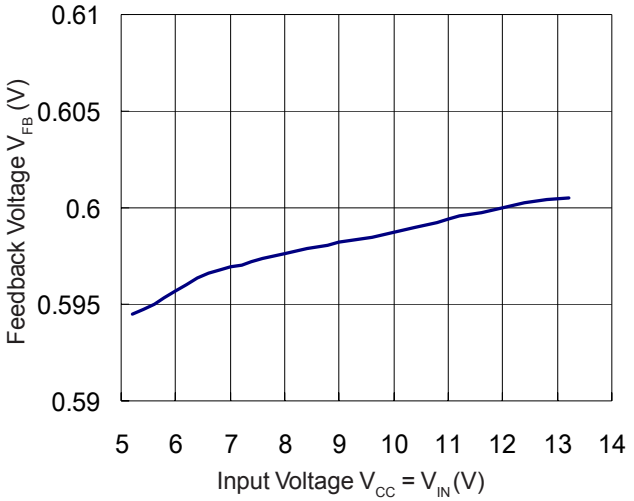
Switching Frequency vs. R_{RT}



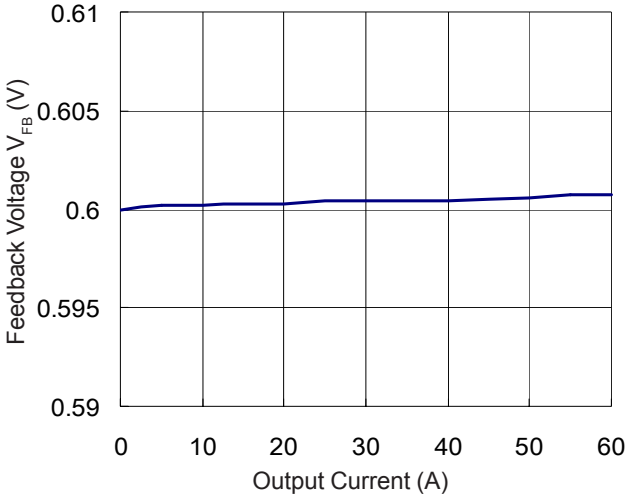
Output Voltage Line Regulation (V_{CC} = 9V)



Output Voltage Line Regulation (V_{CC} = V_{IN})

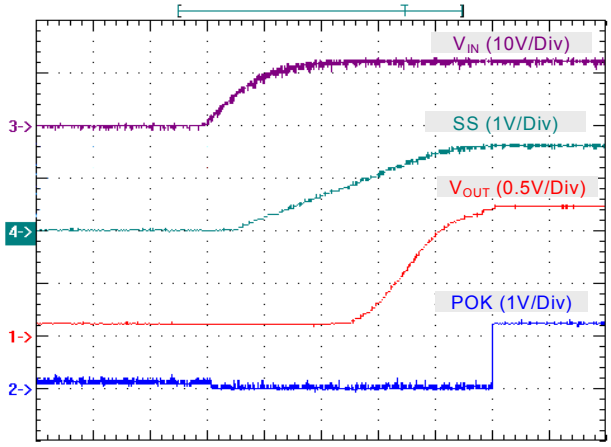


Output Voltage Load Regulation



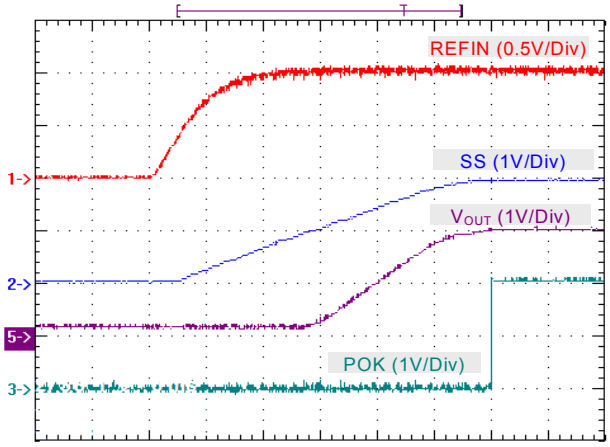
Typical Operation Characteristics

Power On



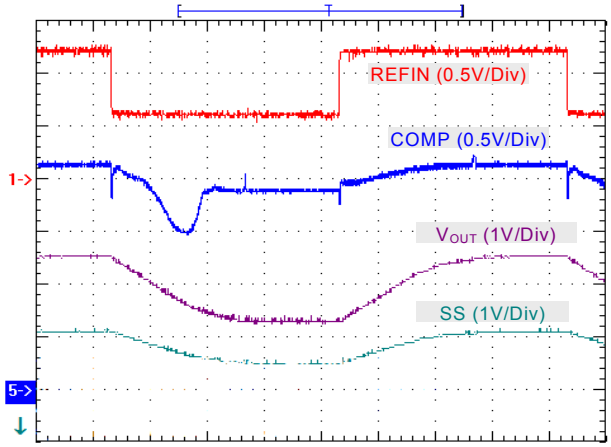
Time (5ms/Div)

Turn On by REFIN



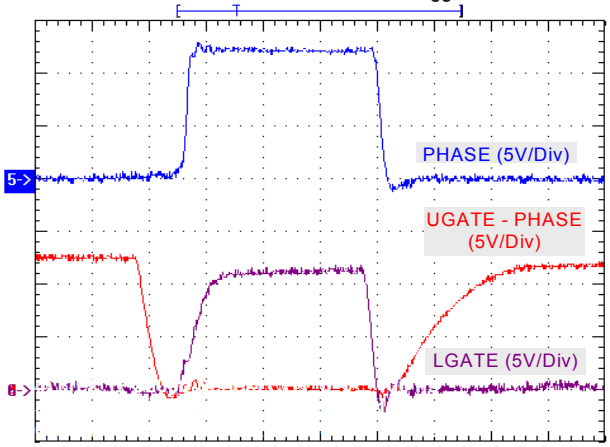
Time (5ms/Div)

Reference Input Step Change



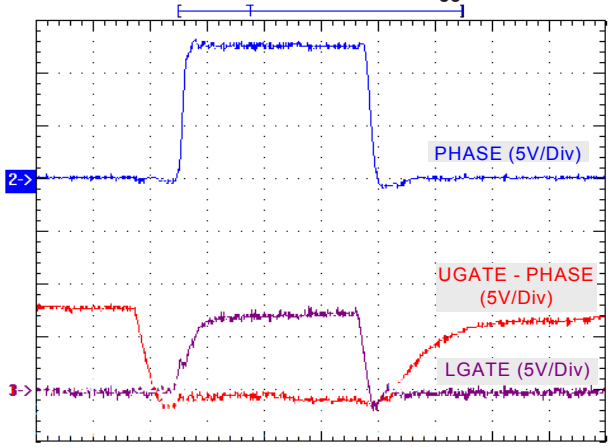
Time (250us/Div)
I_{OUT} = 5A

Switching Waveforms (V_{CC} = 12V)



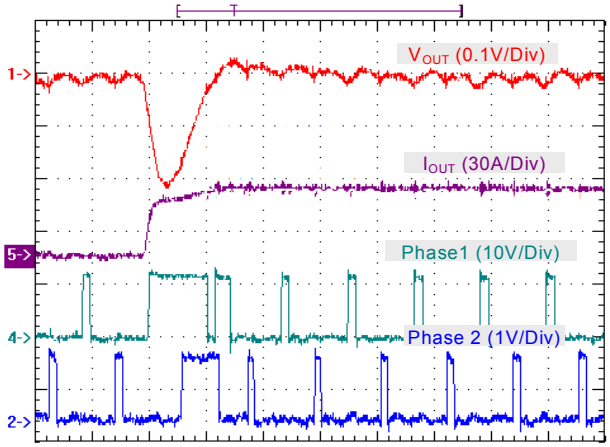
Time (100ns/Div)
V_{CC} = 12V, 20MHz bandwidth limited

Switching Waveforms (V_{CC} = 9V)



Time (100ns/Div)
V_{CC} = 8V, 20MHz bandwidth limited

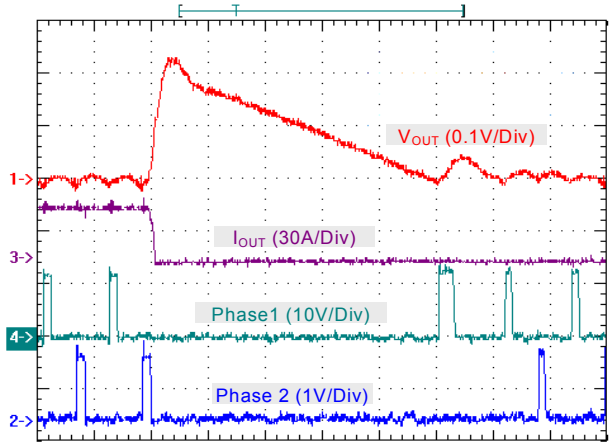
Load Transient Response



Time (2.5us/Div)
I_{OUT} = 0A to 40A

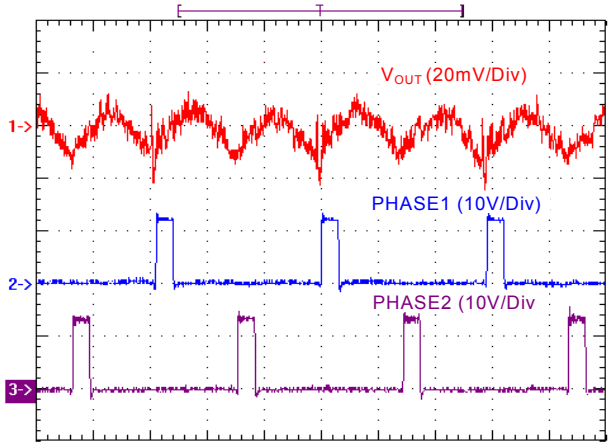
Typical Operation Characteristics

Load Transient Response



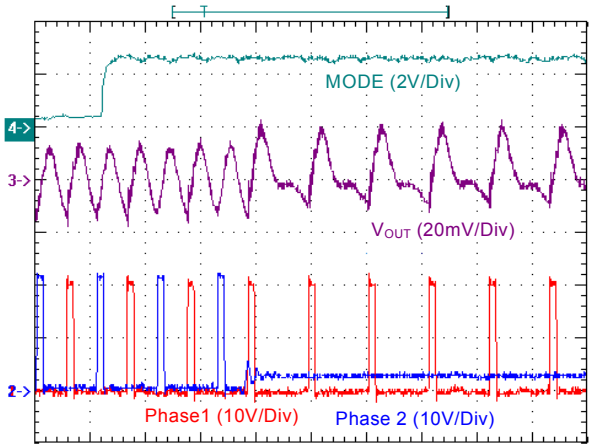
Time 2.5s/Div
I_{OUT} = 40A to 0A

Steady State Operation



Time (1us/Div)
V_{IN} = 12V, V_{OUT} = 1.2V

Two To Single Phase Operation



Time 2.5us/Div

Application Information

Component Selection Guidelines

The selection of external component is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its capability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Power MOSFET Selection

The uP6201A/B requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is supplied by VCC pin that receives 4.5V~13.2V supply voltage. When operating with a 7~13.2V power supply for VCC, a wide variety of NMOSFETs can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 7V. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the uP6201A/B may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 40ns or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP6201A/B is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}} ; D_{LOW} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LOW} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LOW}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the upper MOSFET includes an additional term for switching losses, which are largest at high input voltages. The lower MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are mainly dissipated by the uP6201A/B and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_{G\_C} = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS\_UP}) \times f_{OSC}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LOW} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP6201A/B, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor selection usually is based on the considerations of inductance, rated current, size requirements and DC resistance (DCR).

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} V_{OUT} (1 - \frac{V_{OUT}}{V_{IN}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 20% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

Application Information

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Input Capacitor Selection

The synchronous-rectified Buck converter draws pulsed current with sharp edges from the input capacitor, resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(REMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The equivalent ripple current into the output capacitor is half of the inductor ripple current while the equivalent frequency is double of phase operation frequency due to two phase operation The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} = \frac{\Delta I_L}{2}\left(ESR + \frac{1}{16 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PHASE node is low. When the upper

MOSFET turns on, the PHASE node rises to V_{IN} and the BOOT pin rises to approximately V_{IN} + V_{CC}. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.47µF to 1µF, X5R or X7R dielectric capacitor is adequate.

Feedback Loop Compensation

Figure 11 highlights the voltage-mode control loop for a synchronous-rectified buck converter consisting of uP6201A/B. The control loop includes a compensator and a modulator, where the modulator consists of the PWM comparator, the power stage amplifier and the output filter; the compensator consists of the error amplifier and compensating network. A well-designed feedback loop tightly regulates the output voltage (V_{OUT}) to the reference voltage V_{REF} with fast response to load/line transient and good stability. The goal of the compensation network is to provide and the highest 0dB crossing frequency and adequate phase margin (greater than 45 degrees). It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

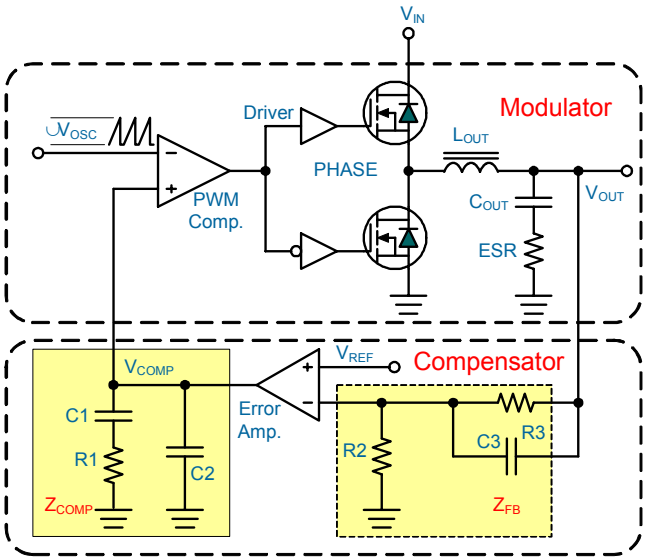


Figure 10. Voltage-Mode Control Loop of uP6201A/B.

Modulator Break Frequency Equations

The error amplifier output (V_{COMP}) is compared with the oscillator (OSC) sawtooth waveform to provide a pulse-width modulated (PWM) waveform with an amplitude of V_{IN} at the PHASE node. The PWM waveform is smoothed by the output filter (L_{OUT} and C_{OUT}). The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC Gain and the output filter (L_{OUT} and C_{OUT}), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as:

$$F_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitor. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements as described in the later sections. The ESR zero of the output capacitor expressed as:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

Figure 12 illustrates frequency response of a typical modulator using uP6201A/B.

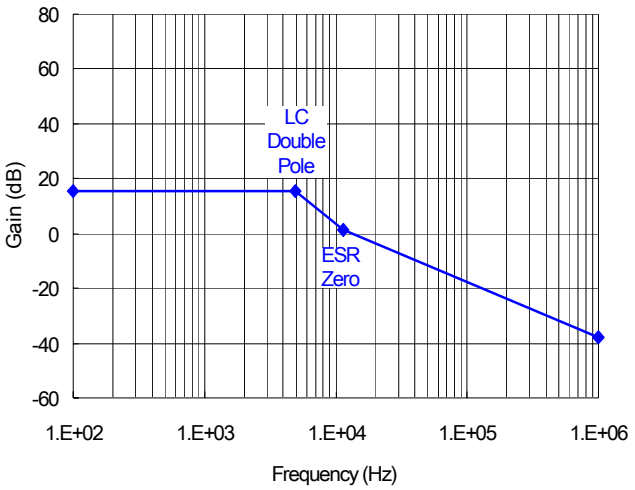


Figure 12. Frequency Response of Modulator.

2) Compensator Frequency Equations

The uP6201A/B adopts an operational transconductance amplifier (OTA) as the error amplifier as shown in Figure 13.

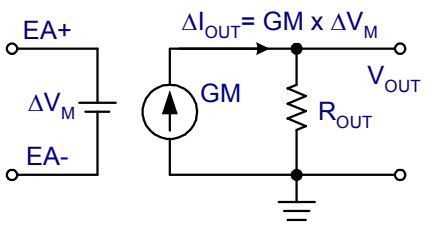


Figure 13. Operational Transconductance Amplifier.

The ***transconductance*** is defined as:

Application Information

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}$$

ΔV_M = (EA+) - (EA-); ΔI_{OUT} = E/A output current.

Figure 14 illustrates a type II compensation network using OTA. The compensation network consists of the error amplifier and the impedance networks Z_{FB} and Z_{COMP}.

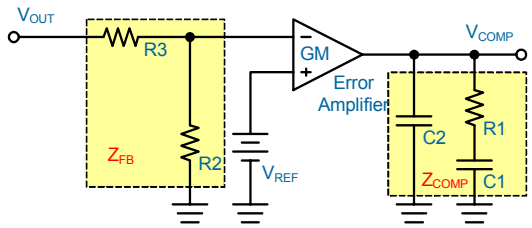


Figure 14. Type II Compensation Network Using OTA.

The compensator transfer function is the small-signal transfer function of V_{COMP}/V_{OUT}. This function is dominated by a Mid-Band Gain and compensation network Z_{COMP}, with a pole at F_{P1} and a zero at F_{Z1}. The Mid-Band Gain of the compensation is expressed as:

$$Mid\_Band\_Gain = \frac{R2}{R2 \times R3} \times R1 \times GM$$

The equations below relate the compensation network's pole and zero to the components (R1, C1, and C2) in Figure 15.

$$F_{P1} = \frac{1}{2\pi \times R1 \times (\frac{C1 \times C2}{C1 + C2})}; \quad F_{Z1} = \frac{1}{2\pi \times R1 \times C1}$$

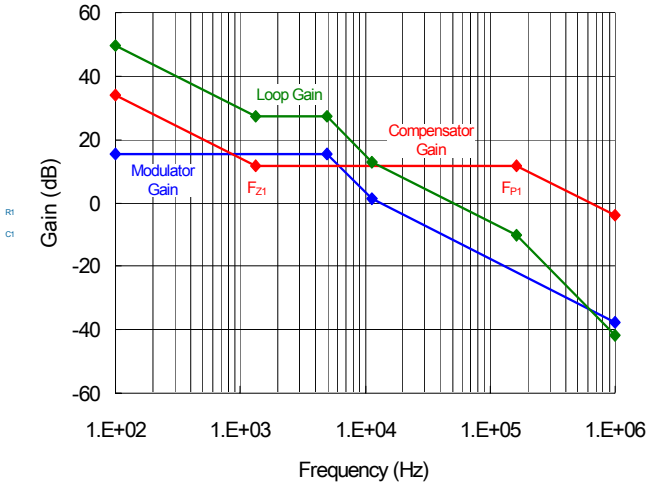


Figure 15. Frequency Response of Type II Compensation.

Figure 16 shows the DC-DC converter's gain vs. frequency. Careful design of Z_{COMP} and Z_{FB} provides tight regulation and fast response to load/line transient with good stability. Follow the guidelines for locating the poles and zeros of the compensation network.

1. Pick Mid-Band Gain (R1) for desired converter bandwidth.
2. Place Zero (C1) below LC double pole (~20% P_{LC}).
3. Place Pole (C2) at half the switching frequency.
4. Check gain against error amplifier open loop gain.
5. Estimate phase margin - repeat if necessary.

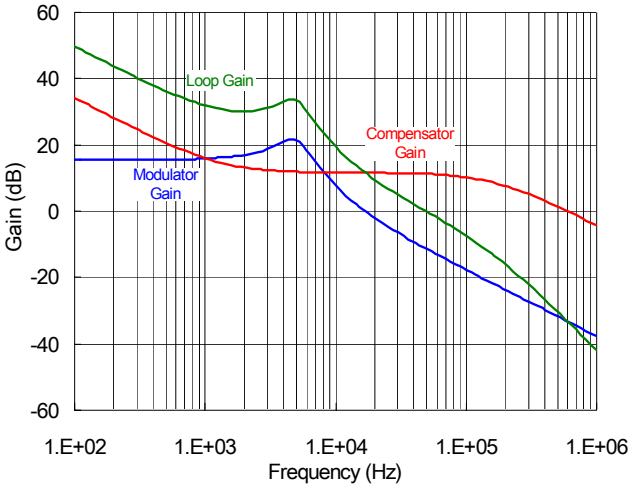


Figure16. Frequency Response of Type II Compensation.

Design Example

As a design example, take a power supply with the following specifications:

V_{IN} = 10.8V to 13.2V (12V nominal), V_{OUT} = 1.2V ±5%, $I_{OUT(MAX)}$ = 40A, f_{OSC} = 300kHz, ΔV_{OUT} = 20mV, bandwidth = 60kHz.

1.) Power Component Selection

First, choose the inductor for about 20% ripple current at the maximum V_{IN}:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

$$\Delta I_L = 40A \times 20\% = \frac{1}{300kHz \times L_{OUT}} \times 1.2V \times (1 - \frac{1.2V}{13.2V})$$

$$L_{OUT} = 0.45\,uH$$

Selecting a standard value of 0.47uH results in a maximum ripple current of 7.7A. The ripple current into output capacitors is 3.9A.

Choose two 1000uF capacitors with 10mΩ ESR in parallel to yield equivalent ESR = 5mΩ. The output ripple voltage is about 20mV accordingly. An optional 22uF ceramic output capacitor is recommended to minimize the effect of ESL in the output ripple.

The modulator DC gain and break frequencies are calculated

as:

$$DC\ Gain = 20 \times \log(\frac{V_{IN}}{\Delta V_{OSC}}) = 20 \times \log(\frac{12}{2.5}) = 13.6dB$$

$$F_{LC} = \frac{1}{2\pi\sqrt{0.47 \times 10^{-6} \times 2000 \times 10^{-6}}} = 5.2kHz$$

$$F_{ESR} = \frac{1}{2\pi \times 5 \times 10^{-3} \times 2000 \times 10^{-6}} = 16kHz$$

2.) Compensation

Select R2 = R3 = 10kΩ to set output voltage as 1.2V. R2 and R3 do not affect the compensation, 1kΩ ~ 10kΩ is adequate for the application.

The modulator gain at zero-crossing frequency (60kHz) is calculated as -17.4dB. This demands a compensator with mid-band gain as 17.4dB. Select R1 as:

$$R1 = \frac{10^{(17.4/20)} \times V_{OUT}}{GM \times V_{REF}} = 8.7k\Omega$$

Select C1 = 13nF to place F_{Z1} = 1.4kHz, about one fifth of the LC double pole.

Select C2 = 68pF to place F_{P1} = 270kHz, about half of the equivalent switching frequency.

Figure 17 shows the result loop gain vs. frequency relation.

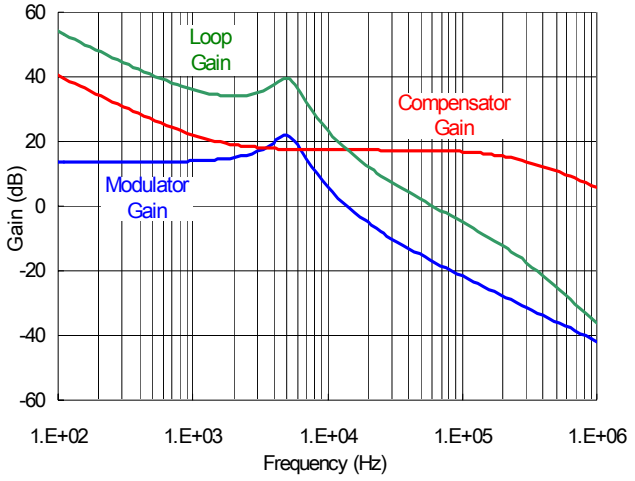


Figure 17. Gain vs. Frequency for the Design Example.

The ESR zero plays an important role in type II compensation. Output capacitors with low ESR and small capacitance push the ESR zero to high frequency band. If the ESR zero is ten times higher than the LC double pole, the double pole may cause the loop phase close to 180° and make the control loop unstable. A type II compensation cannot stabilize the loop since it has only one zero.

Type III Compensation

A type III compensation network as shown in Figure 18 that features 2 poles and 2 zeros is necessary for such applications where ESR zero is far away from the LC double pole. Adding a feedforward capacitor C3 on original type II compensation network introduces an additional pole-zero pair (Z2 and P2) as illustrated in Figure 19. The new pole-zero pair are expressed as:

$$Z2 = \frac{1}{2\pi \times R3 \times C3}\ ;\ P2 = \frac{1}{2\pi \times C3 \times (R2 \times R3)/(R2 + R3)}$$

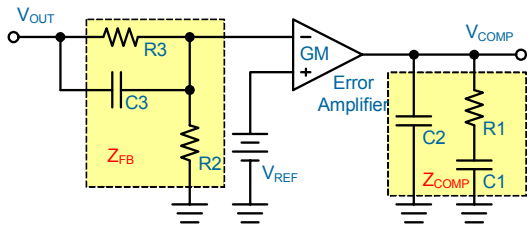


Figure 19. Type III Compensation Network.

While the Mid-Band Gain remains unchanged, the additional pole-zero pair causes a gain boost at the flat gain region. The gain-boost is limited by the ratio (R1 +R2)/R2. Figures 20 and 21 show the DC-DC converter's gain vs. frequency.

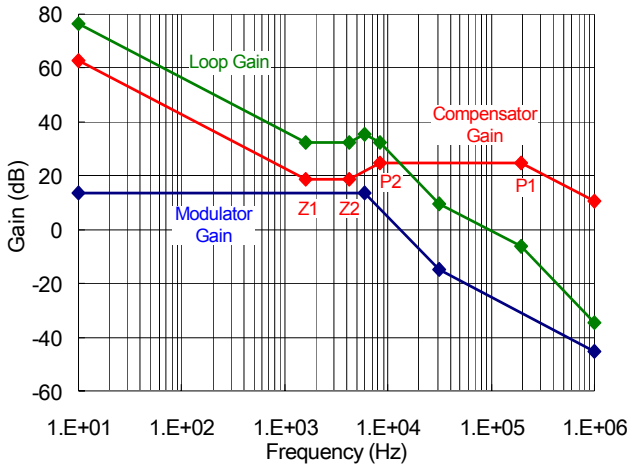


Figure 20. Loop Gain of Type III Compensation Network.

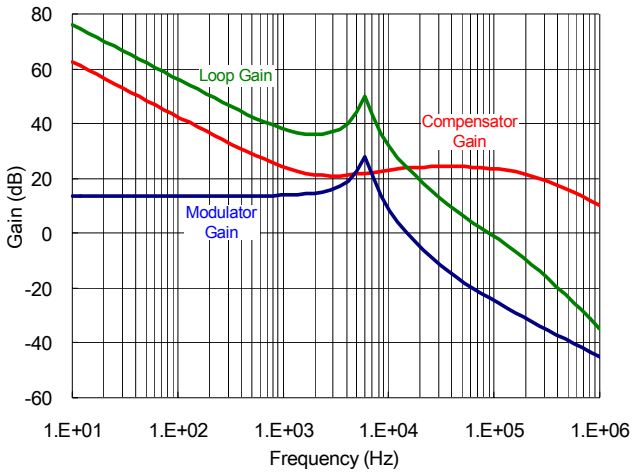


Figure 21. Frequency Response of Type III Compensation.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}x(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP6201A/B.

1 The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting wires indicated by red heavy lines conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.

2 Place the power components as physically close as possible.

2.1 Place the input capacitors, especially the high frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units

2.2 Place the output capacitor between the converter and load.

3 Place the uP6201A/B near the upper and lower MOSFETs with UGATE and LGATE facing the power components. Keep the components connected to noise sensitive pins near the uP6201A/B and away from the inductor and other noise sources.

4 Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP6201A/B Use several bigger vias for power components.

5 Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

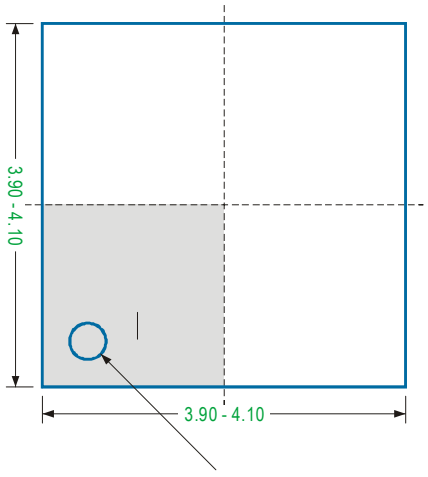
6 The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

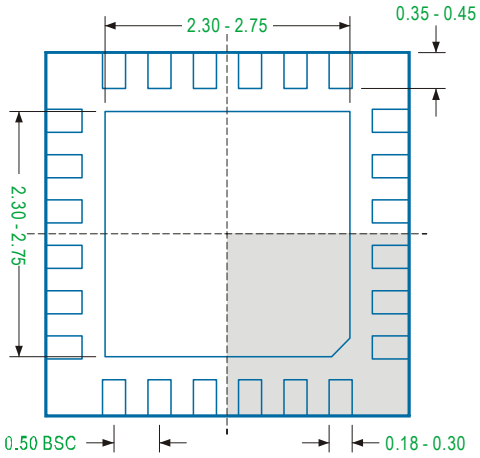
7 The uP6201A/B sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.

8 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.

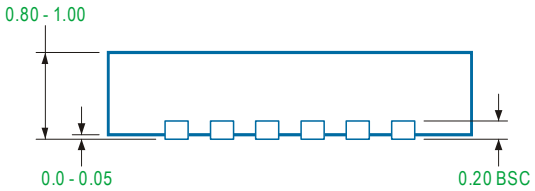
9 Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as possible to the BOOT and PHASE pins.

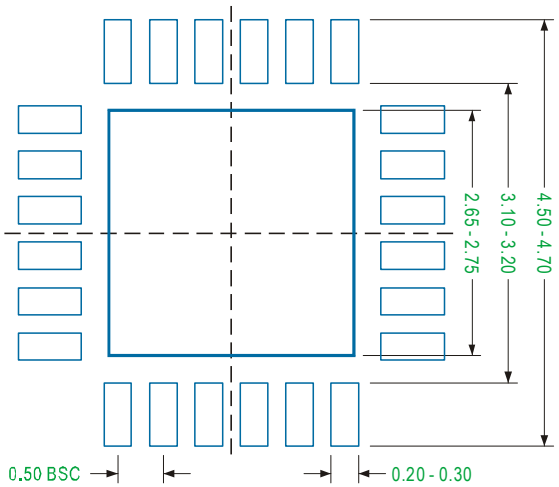
Package Information





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.