Compact Three-Phase Synchronous-Rectified Buck Controller

General Description

The uP6204 is a compact three-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 90A output current thanks to its embedded bootstrapped drivers that support 12V + 12V driving capability. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to the reference inputs R1/R2/R3/R4 that are selected by VID inputs VID1 and VID0. The reference voltage can also be programmed by I2C interface.

The uP6204 adopts DCR current sensing technique for over current protection and droop tuning. Current balance is achieved by sensing the phase current through $R_{DS(ON)}$ of lower MOSFET when it turns on.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes to VQFN6x6-40L package.

Applications

- **Middle-High End GPU Core Power**
- **High End Desktop PC Memory Core Power**
- **Low Output Voltage, High Power Density DC-DC Converters**
- **Voltage Regulator Modules**

Ordering Information

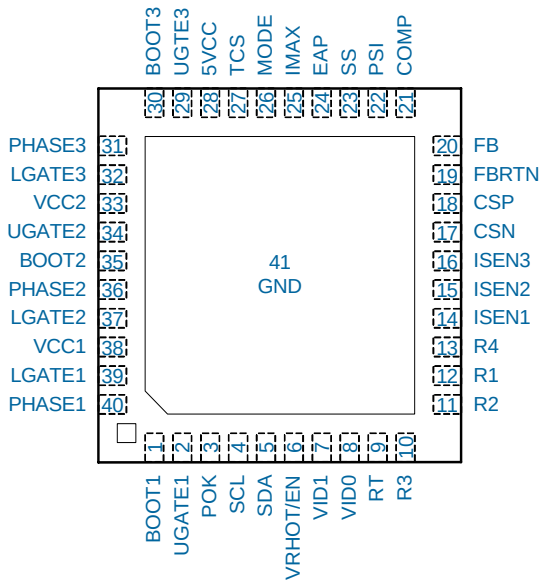
Order Number	Package Type	Remark
uP6204AQAJ	VQFN6x6-40L	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

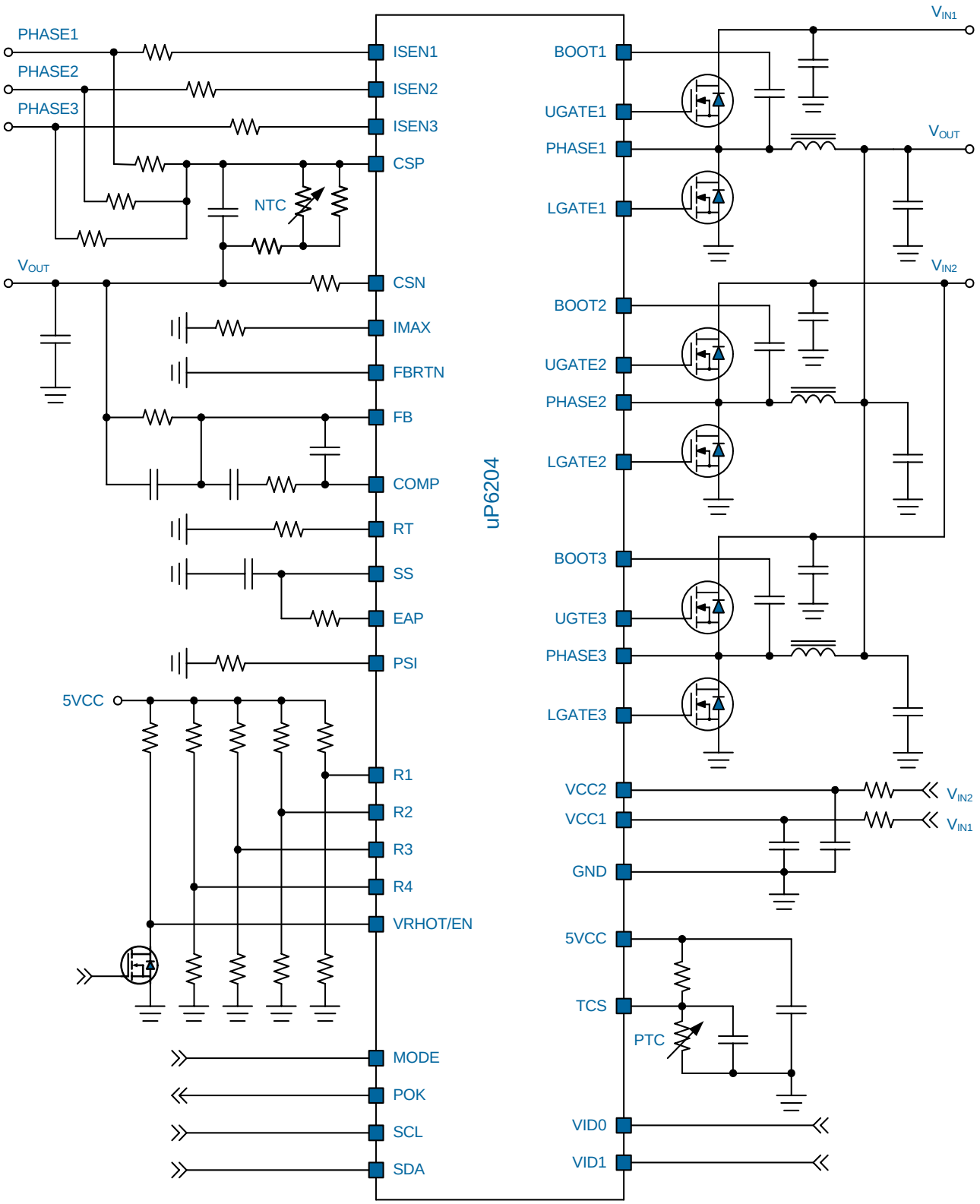
Features

- **Operate with 10.8V ~13.2V Supply Voltage**
- **12V Bootstrapped Drivers with Internal Bootstrap Diode**
- **Flexible Reference Voltage for Power Play**
  - **External Reference Input R1/R2/R3/R4 Selected by VID1 and VID0**
  - **Internal Reference Voltage Programmed by I2C**
- **Simple Single-Loop Voltage-Mode Control**
- **DCR Current Sensing for Over Current Protection and Droop Tuning**
- **$R_{DS(ON)}$ Current Sensing for Current Balance**
- **Adjustable Operation Frequency form 50kHz to 1MHz Per Phase**
- **External Compensation**
- **Adjustable Soft Start**
- **VQFN6x6-40L Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Pin Configuration



Typical Application Circuit



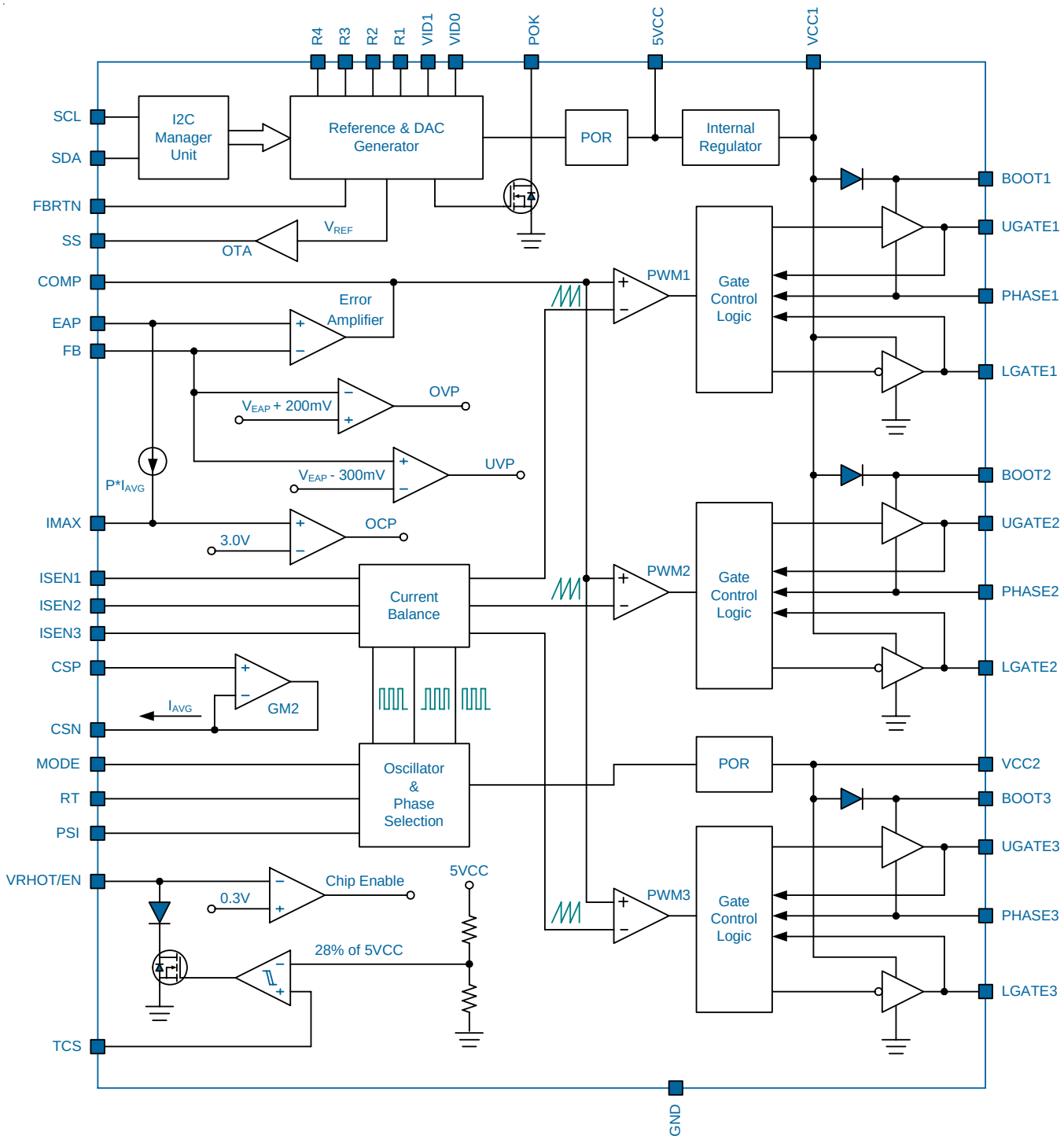
Functional Pin Description

No.	Pin Name	Pin Function
1/35/30	BOOT1/2/3	**Bootstrap Supply** for the floating upper gate drivers of channel 1/2/3 respectively. Connect the bootstrap capacitor C_{BOOT} between BOOT1/2/3 pin and the PHASE1/2/3 pin to form bootstrap circuits. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.47uF to 1uF. Ensure that C_{BOOT} is placed near the IC.
2/34/29	UGATE1/2/3	**Upper Gate Driver Output for Channel 1/2/3.** Connect these pins to the gates of corresponding upper MOSFET. These pins are monitored by the adaptive shoot-through protection circuitry to determine when the corresponding upper MOSFET has turned off.
3	POK	**Power OK Indication.** This is an open-drain output for power OK indication. This pin is set to high impedance after soft start end and no fault occurs.
4	SCL	**Serial Clock Input.** This pin receives serial bus clock signal.
5	SDA	**Serial Data Input.** This pin is input or output of serial bus data signal.
6	VRHOT/EN	**Chip Enable and High Temperature Warning Output.** Pulling this pin to GND shuts down the uP6204. All gate drivers output low to turn off both upper and lower MOSFETs. This pin is clamped at 0.45V when the output voltage is within regulation and set to high impedance when the output voltage is during soft start or out of regulation.
7/8	VID1/0	**Digital Inputs 1/0 for Power Play.** See the related sections for detail.
9	RT	**Operation Frequency Setting.** Connect a resistor between this pin and GND to set the operation frequency.
10/11/ 12/13	R3/R2/ R1/R4	**Reference Voltage Inputs for Power Play.** Connect voltage dividers from 5VCC to these pins to ground to set the reference voltages for power play. The FB pin voltage is regulated to these voltages when selected by VID0 and VID1. See the related sections for detail.
14/15/16	ISEN1/2/3	**Phase Current Sening Input 1/2/3.** These pins sense the phase current by sensing the voltage drop across the respective lower MOSFET. Connect these pins to the corresponding PHASE node through an external resistor. See the related sections for details.
17	CSN	**Negative Input for Total Current Sensing.** This pin along with CSN pin senses the total inductor current. See the related sections for details.
18	CSP	**Positive Input for Total Current Sensing**. This pin along with CSP pin senses the total inductor current. See the related sections for details.
19	FBRTN	**Return Path for Remote Voltage Sensing.** Connect this pin directly to the ground node where the output voltage is to be regulated.
20	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. Connect this pin directly to the node where the output voltage is to be regulated. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
21	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
22	PSI	**Phase Reduction Threshlold Setting.** Connect a resistor from this pin to GND to set the phase reduction threshold level. Pull this pin lower than 0.2V to disable the phase reduction function.

Functional Pin Description

No.	Pin Name	Pin Function
23	SS	**Soft Start Output.** Connect a capacitor from this pin to GND to set the soft start interval.
24	EAP	**Positive Input of the Error Amplifier.** The FB voltage is regulated to track this voltage during soft start, power play and steady state operation. Connect a resistor to SS pin to tuning the droop slope.
25	IMAX	**Output Current Indication and Over Current Setting.** Connect a resistor between this pin and GND to set the trigger threshold level for over current protection. This pin also intends for output current indication since its voltage is directly proportional to the output current.
26	MODE	**Phase Number of Operation Setting.** Connect this pin to GND for three phase operation. Connect this pin to 5VCC for two phase operation. Let this pin open for single phase operation. Only phase 1 is enabled when single phase operation. Only phase 1 & 2 are enabled when two phase operation.
27	TCS	**Temperature Sensing.**
28	5VCC	**Internal Regulator Output.** This is the output pin of linear regulator for internal bias and external usage. The output current capability is 20mA.
40/36/31	PHASE1/2/3	**Switch Node for Channel 1/2/3.** Connect these pins to the source of the corresponding upper MOSFET and the drain of the corresponding lower MOSFET. These pins are also monitored by the adaptive shoot-through protection circuitry to determine when the upper corresponding MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
39/37/32	LGATE1/2/3	**Lower Gate Driver Output for Channel 1/2/3.** Connect these pins to the corresponding gate of lower MOSFET. These pins are monitored by the adaptive shoot-through protection circuitry to determine when the corresponding lower MOSFET has turned off.
33	VCC2	**Supply Input for Gate Driver 3.** This pin provides current for lower gate drivers, and the bootstrap circuit for upper drivers of channel2/3. Connect this pin to the power input of channel 2 or channel 3.
38	VCC1	**Supply Input for Gate Driver 1/2 and the Chip.** This pin provides current for lower gate drivers, and the bootstrap circuit for upper drivers of channel1 and the control circuit of the uP6204. Connect this pin to the power input of of channel1.
Exposed Pad 41 GND		**Ground for the IC.** The exposed pad should be well solder to PCB and electraically connected ground island/plane with short and wide traces.

Functional Block Diagram



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Selecting Phase Number of Operation

The uP6204 supports single/two/three-phase operation that is important for PCIE interfaced graphic cards where neither bus power nor external power is capable of delivering full load current. Take a two-phase buck converter as shown in Figure 1 for example. Two-phase operation will make the phase 2 converter act like a boost converter if the external power is not available, boosting the output voltage V_{OUT} to the input voltage V_{IN2}. The relationship between input voltage and output voltage is governed by conventional boost converter equation. Offset of the current balance function may make the duty cycle of phase 2 converter smaller than that of phase 1 converter. This results in input voltage V_{IN2} higher than 15V that may damage the input capacitors and other devices. Therefore, phase 2 must be turned off when input voltage VIN2 is not present to eliminate the possibility of over voltage on input capacitors and other devices of the phase 2 converter.

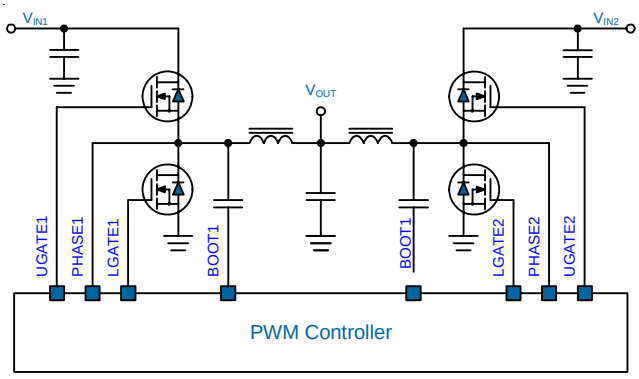


Figure 1. Simplified Two-Phase Buck Converter.

The uP6204 selects phase number of operation according to the MODE pin and VCC2 status. The MODE pin is a tri-state input. When the MODE pin is pulled low, the uP6204 operates in three phases. When the MODE pin is left floating, only phase 1 is activated. When the MODE pin is pulled high, only phase 1 & 2 are activated. The uP6204 does not support real-time phase number of operation change. If any change of MODE state has been detected, the uP6204 will shut down the output voltage and re-soft-start again.

Table 1. Phase Number of Operation Table.

MODE	VCC2 POR	Phase Number of Operation
High	X	Phase 1 /2
Floating	X	Phase 1
Low	YES	Phase 1/2/3
Low	NO	Shutdown

VCC1 powers the gate drives for phase 1/2 while VCC2 powers the gate drivers for phase 1. When MODE pin is pulled low, the uP6204 checks the VCC2 POR status before soft start to ensure both bus and external power inputs are ready for providing current to output voltage. The VCC2 pin should be connected to V_{IN2} (external power input). Figure 2 shows an implementation example where phase 1/2 are powered by PECI bus and phase 3 is power by external cable.

Note that when operated in single/dual-phase, the rated current is reduced to fractions of normal level. Continuous demanding high current may damage the converter.

Functional Description

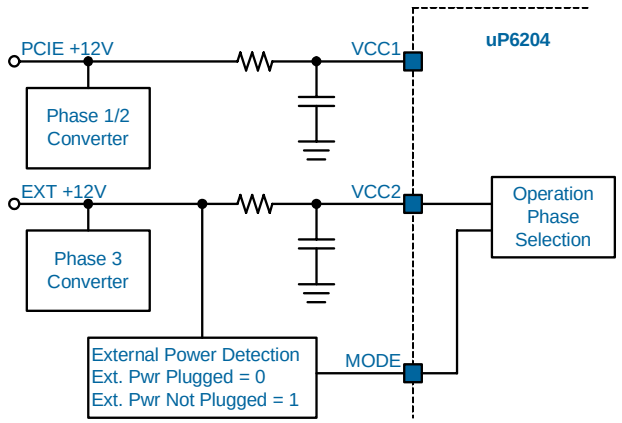


Figure 2. Single/Three Phase Operation

Dynamic Voltage Management

The uP6204 provides a comprehensive dynamic voltage management scheme as shown in Figure 3. V_{REF} is the reference voltage used for voltage control loop. V_{REF} is default connected $V_{REF/P}$ and can be programmed to either V_{REFS} or V_{REFP} by PMBUS, see the related section for details.

The V_{REFS} is a reference voltage programmed by PMBUS. The V_{REFP} is a reference voltage programmed by the VID0 and VID1 inputs. One of the voltage levels Level[1:4] is selected as V_{REFP} as illustrated in table 2. Initially, Level[1:4] are defined as $V_{R[1:4]}$ defined by R[1:4] pins. Level[1:4] can also be overwritten by PMBUS according the AMD GPU VID Table as shown in Table 3.

R1/R2/R3/R4 define four voltage levels through voltage dividers for power on default setting.

$$V_{R[1:4]} = V_{CC5} \times \frac{R_{LOW}}{R_{HIGH} + R_{LOW}}$$

where V_{CC5} is the 5.0V reference output voltage at 5VCC pin. **Note that the V_{R2} is the default reference voltage level for soft start.**

Table 2. Parallel VID Selection.

VID[1:0]	V_{REFP} Voltage	
	Set by R1/R2/R3/4	Set by PM Bus
00	V_{R1}	Level 1
01	V_{R2}	Level 2
10	V_{R3}	Level 3
11	V_{R4}	Level 4

Voltage Control Loop and Power On Sequence

Figure 4 and Figure 5 show the voltage control loop and typical power on sequence of uP6204 respectively. The power on reset is acknowledged and the controller is enabled at T0. A buffer with 160uA maximum current capability starts to charge the soft start capacitor

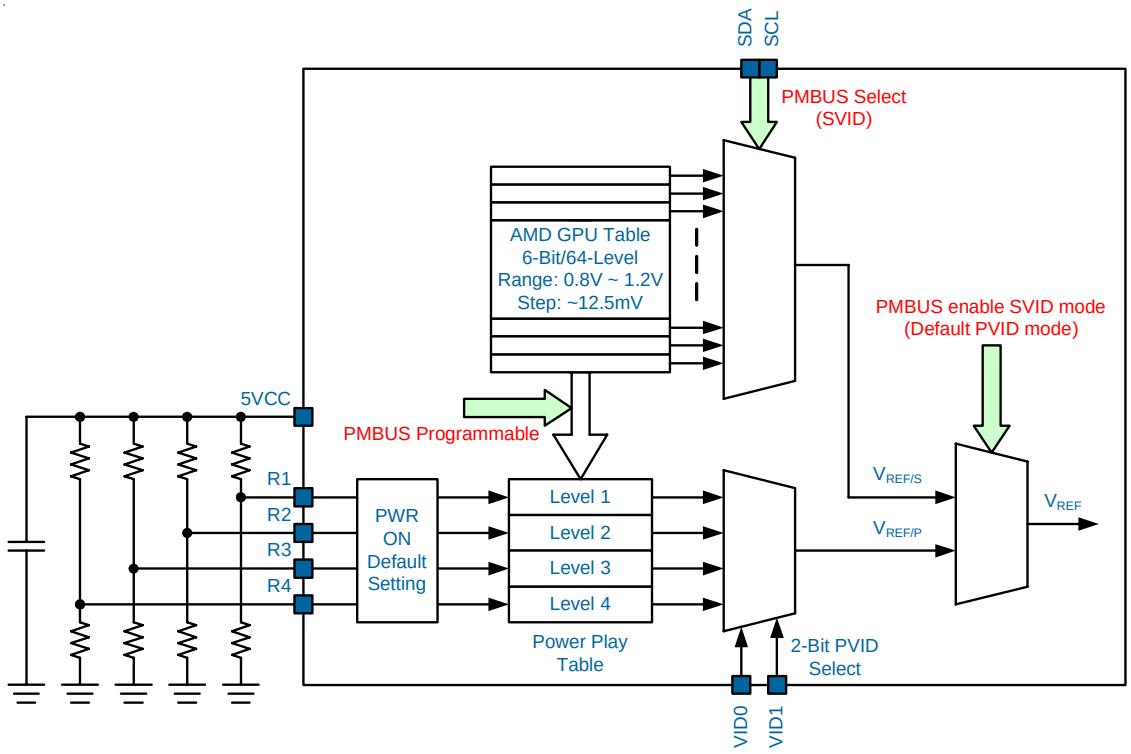


Figure 4. Dynamic Voltage Management

Table 3. AMD GPU VID Table

Step	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Output Voltage
1	0	0	0	0	0	0	1.3500
2	0	0	0	0	0	1	1.3375
3	0	0	0	0	1	0	1.325
4	0	0	0	0	1	1	1.3124
5	0	0	0	1	0	0	1.3000
6	0	0	0	1	0	1	1.2875
7	0	0	0	1	1	0	1.2750
8	0	0	0	1	1	1	1.2625
9	0	0	1	0	0	0	1.2500
10	0	0	1	0	0	1	1.2375
11	0	0	1	0	1	0	1.2250
12	0	0	1	0	1	1	1.2125
13	0	0	1	1	0	0	1.2000
14	0	0	1	1	0	1	1.1875
15	0	0	1	1	1	0	1.1750
16	0	0	1	1	1	1	1.1625
17	0	1	0	0	0	0	1.1500
18	0	1	0	0	0	1	1.1375
19	0	1	0	0	1	0	1.1250
20	0	1	0	0	1	1	1.1125
21	0	1	0	1	0	0	1.1000
22	0	1	0	1	0	1	1.0875
23	0	1	0	1	1	0	1.0750
24	0	1	0	1	1	1	1.0625
25	0	1	1	0	0	0	1.0500
26	0	1	1	0	0	1	1.0375
27	0	1	1	0	1	0	1.0250
28	0	1	1	0	1	1	1.0125
29	0	1	1	1	0	0	1.0000
30	0	1	1	1	0	1	0.9875
31	0	1	1	1	1	0	0.9750
32	0	1	1	1	1	1	0.9625

Table 3. AMD GPU VID Table

Step	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Output Voltage
33	1	0	0	0	0	0	0.9500
34	1	0	0	0	0	1	0.9375
35	1	0	0	0	1	0	0.9250
36	1	0	0	0	1	1	0.9125
37	1	0	0	1	0	0	0.9000
38	1	0	0	1	0	1	0.8875
39	1	0	0	1	1	0	0.8750
40	1	0	0	1	1	1	0.8625
41	1	0	1	0	0	0	0.8500
42	1	0	1	0	0	1	0.8375
43	1	0	1	0	1	0	0.8250
44	1	0	1	0	1	1	0.8125
45	1	0	1	1	0	0	0.8000
46	1	0	1	1	0	1	0.7875
47	1	0	1	1	1	0	0.7750
48	1	0	1	1	1	1	0.7625
49	1	1	0	0	0	0	0.7500
50	1	1	0	0	0	1	0.7375
51	1	1	0	0	1	0	0.7250
52	1	1	0	0	1	1	0.7125
53	1	1	0	1	0	0	0.7000
54	1	1	0	1	0	1	0.6875
55	1	1	0	1	1	0	0.6750
56	1	1	0	1	1	1	0.6625
57	1	1	1	0	0	0	0.6500
58	1	1	1	0	0	1	0.6375
59	1	1	1	0	1	0	0.6250
60	1	1	1	0	1	1	0.6125
61	1	1	1	1	0	0	0.6000
62	1	1	1	1	0	1	0.5875
63	1	1	1	1	1	0	0.5750
64	1	1	1	1	1	1	0.5625

connected to SS pin after a 800us delay time T_{DLY} at T1. The non-inverting input of the error amplifier V_{EAP} is equal to V_{SS} and ramp up linearly to V_{REF}. (Neglect the voltage drop caused by droop setting resistor R_{DRP}, see the related section for details.) Consequently, the FB voltage V_{FB} is regulated to V_{EAP} and ramp up linearly to V_{REF}.

VR2 is default selected as V_{REF} during soft start cycle regardless of the status of VID0 and VID1. The output voltage reaches power on default output voltage defined by R2 pin at T2 and stays there for a time interval T_{DFT}.

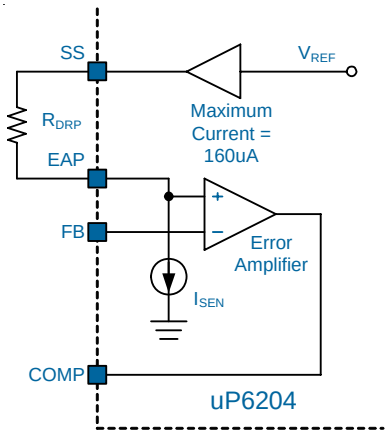


Figure 4. Voltage Control Loop

The uP6204 enters PVID mode (parallel VID mode) and moves the output voltage to its final level selected by VID[1:0] and voltages at R1/R2/R3/R4 after T3. The output voltage transition slew rate is identical to the slew rate during T_{SS}. Table 4 shows typical time period of soft start cycle of uP6204.

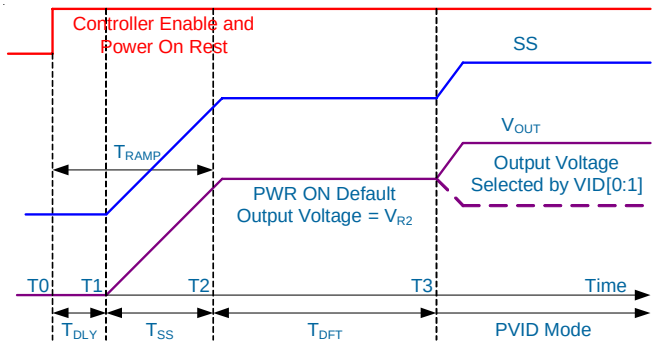


Figure 5. Power On Sequence

Table 4. Typical Power On Periods with C_{SS} = 4.7nF

Parameter	Symbol	Nominal Value	Adjustable Range
Start Delay Time	T_{DLY}	200us	NA
Soft Start Time	T_{SS}	3ms	1~4ms
Enable to Output in Regulation	T_{RAMP} = T_{DLY} + T_{SS}	3.2ms	1.2~4.2ms
PWR ON Default Voltage Period	T_{DFT}	200ms	NA

Operation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency as:

$$f_{OSC} = \frac{10000}{R_{RT}(k\Omega)} \quad (kHz)$$

Figure 6 shows the relationship between oscillation frequency and R_{RT}.

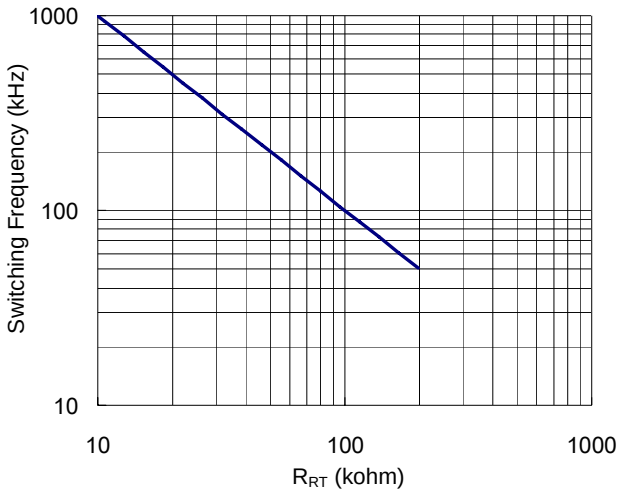


Figure 6. Switching Frequency vs. R_{RT}.

Channel Current Sensing and Current Balance

The uP6204 senses the phase currents for current balance by sensing the voltage across the lower switches when they turn on as shown in Figure 7. The sampled-and-held current is calculated as:

$$I_{SEN}[1:3] = \frac{10mV - V_{PHASE}[1:3]}{R_{SEN}[1:3]}$$

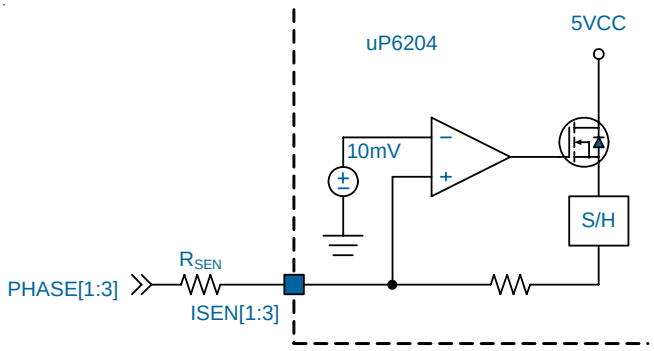


Figure 7. Phase Current Sensing.

The uP6204 fine tunes the duty cycle of each channel for current balance according to the sensed inductor current signals. If the current of channel 1 is smaller than the current of channel 2 and 3, the uP6204 increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice versa. The user can adjust R_{SEN} to adjust current ratio between phases.

The sampled-and-held current I_{SEN}[1:3] are monitored for phase over current protection. If any one of I_{SEN}[1:3] is higher than 20uA, phase over current protection is activated and shuts down the uP6204.

Total Current Sensing

The uP6204 extracts output current by parasitic DCR of the inductors for over current protection. A RC network is paralleled to the inductor for current sensing as shown in Figure 8 where DCR is the parasitic resistance. The V_C across the capacitor equals to $V_{DCR} = I_L$ x DCR across the DCR of the inductor if the time constants match:

$R1C_S = R2C_S = R3C_S = 3xL/DCR$

The GM amplifier will source a current source $I_{AVG} = V_C/R_{CSN}$ to virtually short its two inputs. Consequently I_{CSN} is calculated as:

$$I_{CSN} = \frac{V_C}{R_{CSN}} = \frac{I_L \times DCR}{R_{CSN}} = \frac{I_{OUT} \times DCR}{3 \times R_{CSN}}$$

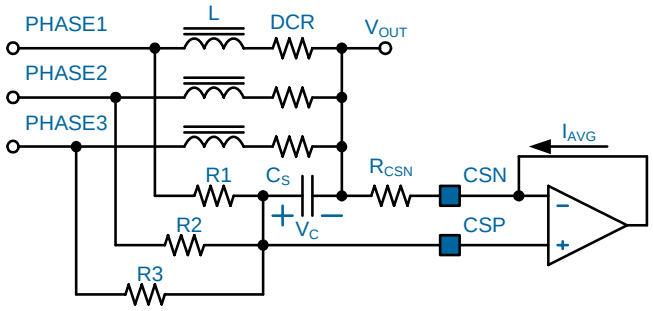


Figure 8. DCR Current Sensing Scheme

The sourcing capability of the GM amplifier is 100uA. It is recommended to scale ***I_{CSN} = 40uA*** at rated inductor current. Take a 90A converter for example. Assume DCR = 2mΩ, select the sense resistor according to

$$R_{CSN} = \frac{90A \times 2m\Omega}{3 \times 40uA} = 1.5k\Omega$$

Output Voltage Droop Tuning

The uP6204 dynamically adjusts the output voltage according to the output current the droop tuning resistor RDRP as shown in Figure 4. The sensed current signal IAVG is mirrored and injected to EAP pin, producing a voltage drop between SS pin and EAP pin.

$$V_{EAP} = V_{SS} - 3 \times I_{AVG} \times R_{DRP} = V_{REF} - \frac{I_{OUT} \times DCR}{R_{CSN}} \times R_{DRP}$$

Since the FB voltage is regulated to track VEAP, it shows a load line with slope = (DCR x R_{DRP} / 3 / R_{CSN}).

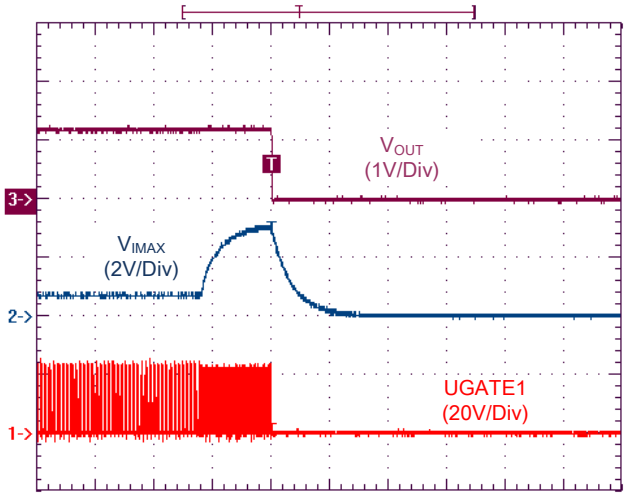
Short the R_{DRP} to disable the droop function.

Over Current Protection

The sensed current signal I_{AVG} is mirrored and injected to IMAX pin for over current protection. If the IMAX pin voltage is higher than 3.0V, over current protection is activated and shuts down the uP6204 as shown in Figure 9. A resistor connected to IMAX set the over current protection level as:

$$I_{MAX} = \frac{3 \times 3V \times R_{CSN}}{R_{IMAX} \times DCR}$$

For example, if DCR = 2mΩ, R_{CSN} = 1.5kΩ, and R_{IMAX} = 47kΩ, the over current protection level is calculated as 144A.



Time: (10ms/Div)

Figure 8. Over Current Protection.

Dynamic Phase Reduction

The uP6204 dynamically reduces the phase number of operation to reduce the switching and conduction loss at light load condition. This yield high efficiency over wide range of output current.

The 20uA current source out of PSI pin produces a voltage cross the resistor R_{PSI} connected to this pin.

$$V_{PSI} = I_{PSI} \times R_{PSI}$$

The uP6204 operates with single phase if V_{IMAX} is smaller than V_{PSI}. (V_{PSI} < 0.2V) disables the dynamic phase reduction function.

Over Voltage and Under Voltage Protection

The FB voltage is monitored for under voltage and over voltage protection. The OVP is triggered and turns on the lower MOSFETs if $V_{FB} > V_{REF}$ + 200mV with 10us dealy. The OVP function is latch-off type and can only be reset by POR or toggling the VRHOT/EN pin.

The UVP is triggered and turns off upper/lower MOSFETs if VFB < VEAP - 300mV with 10us dealy. The UVP function is latch-off type and can only be reset by POR or toggling the VRHOT/EN pin.

The OVP and UVP functions are blocked about 20us when reference voltage is changed either by PVID or SVID.

Temperature Monitoring and Chip Enable

The VRHOT/EN is multifunctional pin: high temperature warning and chip enable as shown in Figure 9. Pulling this pin low shuts down the uP6204. The VRHOT/EN is pulled high to 5VCC when released. This enables the uP6204. This pin is clamped to 0.45V when the sensed temperature is over the over temperature warning level.

A PTC network is used to monitor the converter temperature. The uP6204 asserts over demarcature warning and turns on the internal MOSFET if

$$\frac{R_{PTC}}{R_{PTC} + R1} > 0.28$$

The VRHOT/EN is clamped to 0.45V by internal diode and is OK to keep the uP6204 enabled. **It is highly suggest to use 10kΩ pull high resistance so that the VRHOT/EN can be properly clamped.**

The uP6204 asserts thermal shutdown and turns off upper/lower MOSFETs if

$$\frac{R_{PTC}}{R_{PTC} + R1} > 0.33$$

An NTC network is also OK for temperature monitoring.

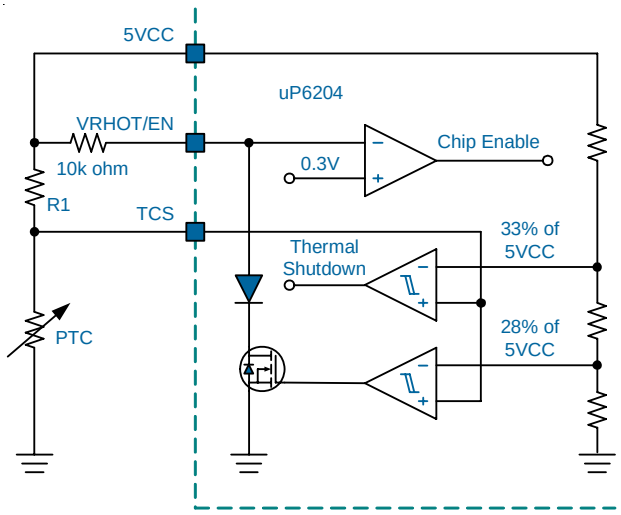


Figure 9. Temperature Monitoring and Chip Enable.

Absolute Maximum Rating

Supply Input Voltage, VCC1/VCC2 (Note 1) ---------- -0.3V to +15V
PHASE to GND
DC ---------- -1V to 15V
< 200ns ---------- -5V to 30V
BOOT to PHASE ---------- 15V
BOOT to GND
DC ---------- -0.3V to PHASE +15V
< 200ns ---------- -0.3V to 42V
Input, Output or I/O Voltage ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN6x6-40L θ_{JA} ---------- TBD
Power Dissipation, P_D @ TA = 25°C
VQFN6x6-40L ---------- TBD

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- 10.8V to 13.2V

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}		10.8	--	13.2	V
Supply Current	I_{CC}	UGATE and LGATE Open; V_{CC} = 12V, Switching	--	5	--	mA
Quiescent Supply Current	I_{CC_Q}		--	4	--	mA
POR Threshold	V_{CCRTH}		8	9	10	V
POR Hysteresis	V_{CCHYS}		--	0.3	--	V
Soft Start						
Soft Start Current	I_{SS}	V_{CC} = 12V	120	160	200	uA
5VCC						
5VCC Output Voltage Accuracy	V_{CC5}	V_{CC1} = 12V, I_{CC5} = 0mA	4.95	5.00	5.05	V
5VCC Output Voltage Load Regulation	ΔV_{CC5}	I_{CC5} = 0mA ~ 20mA	-0.5	--	0.5	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy						
Output Voltage Accuracy		V_{FB} - $V_{R1[1:4]}$ when V_{REF} set by R1[1:4], I_{OUT} = 0A.	-10	--	10	mV
		V_{REF} set by I2C. I_{OUT} = 0A	1.5	--	1.5	%
Oscillator						
Free Running Frequency	f_{OSC}	R_{RT} = 33k	270	300	330	kHz
Frequency Variation			-10	--	10	%
Frequency Range			50	--	1000	kHz
Maximum Duty Cycle			85	90	95	%
Minimum Duty Cycle			--	0	--	%
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	4.0	--	V_{P-P}
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	60	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	6	10	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Current Sense						
Current Sense Ratio	I_{IMAX}/I_{AVG}	I_{AVG} = 40uA, R_{IMAX} = 10kΩ	90	100	110	%
Maximum Sorcing Current	I_{CSN_MAX}		100	--	--	uA
GM Amplifier Offset	V_{OFFSET}	V_{OFFSET} = $\lvert V_{CSP} - V_{CSN} \rvert$, V_{CSP} = 1.1V, Connect a resistor R_{ICSN} = 20kΩ from CSN to GND	-3	--	3	mV
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	V_{BOOT} - V_{PHASE} = 12V, I_{UG_SRC} = 150mA	--	1.3	2.6	Ω
Upper Gate Sink	R_{UG_SNK}	V_{BOOT} - V_{PHASE} = 12V, I_{UG_SNK} = 150mA	--	1	2.0	Ω
Lower Gate Source	I_{LG_SRC}	I_{LG_SRC} = 150mA	--	1.3	1.6	Ω
Lower Gate Sink	I_{LG_SNK}	I_{LG_SNK} = 150mA	--	0.8	1.6	Ω
Dead Time	T_{DT}		--	30	--	ns
Temperature Monitoring						
Over Temperature Warning Threshold Level	V_{TCS}	percentage of 5VCC	--	28	--	%
Thermal Shutdown Threshold Level	V_{TCS}	percentage of 5VCC	--	33	--	%
OT Warning Clamp Voltage	$V_{VRHOT/EN}$	V_{TCS} = 30% of 5VCC, $I_{VRHOT/EN}$ = 50uA	--	0.45	--	V
Chip Eanble Threshold Level	$V_{VRHOT/EN}$	$V_{VRHOT/EN}$ rising	0.4	--	--	V
Chip Eanble Threshold Level	$V_{VRHOT/EN}$	$V_{VRHOT/EN}$ falling	--	--	0.2	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Control Inputs						
VID Input High Threshold Level	$V_{VID[0:1]}$	VID0, VID1 rising	1.4	--	--	V
VID Input Low Threshold Level	$V_{VID[0:1]}$	VID0, VID1 falling	--	--	0.4	V
Protections						
Over Current Protection Threshold Level	V_{IMAX}		--	3.0	--	V
Over Vooltage Protection Threshold Level	V_{FB}	V_{FB} - V_{REF}	--	200	--	mV
Under Voltage Protection Threshold Level	V_{FB}	V_{FB} - V_{REF}	--	-300	--	mV
Power OK Threshold Level	V_{FB}	V_{FB} - V_{REF}, V_{REF} rising.	--	30	--	mV
Power OK Sinking Capability	V_{POK}	I_{POK} = 4mA	--	--	100	mV

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

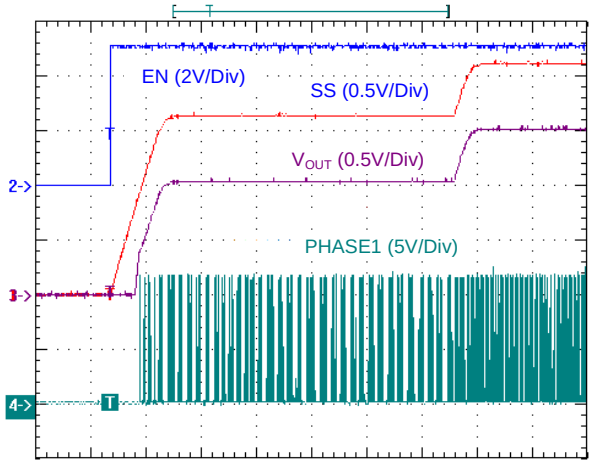
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

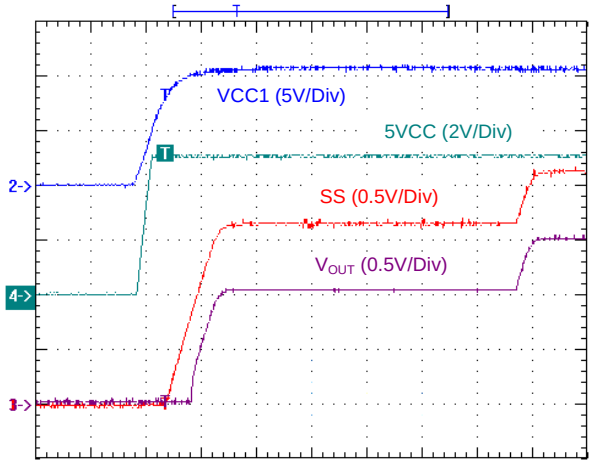
Typical Operation Characteristics

Turn On Waveforms



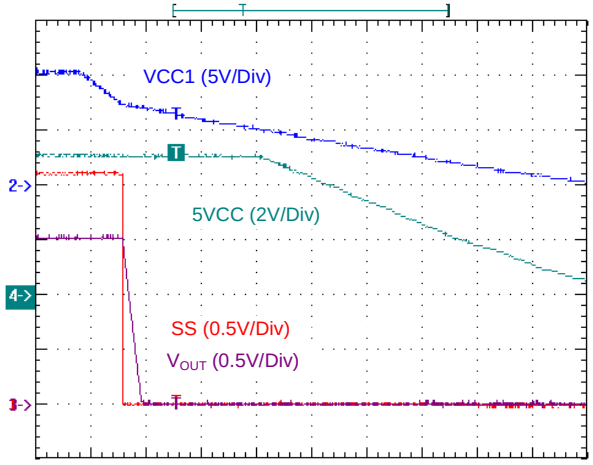
Time: (10ms/Div)

Power On Waveforms



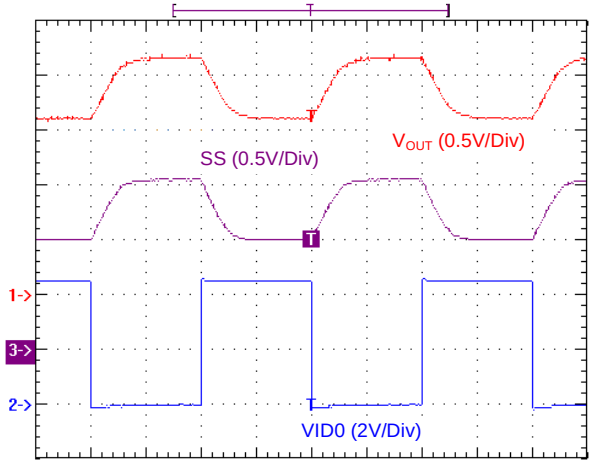
Time: (10ms)

Power Off Waveforms



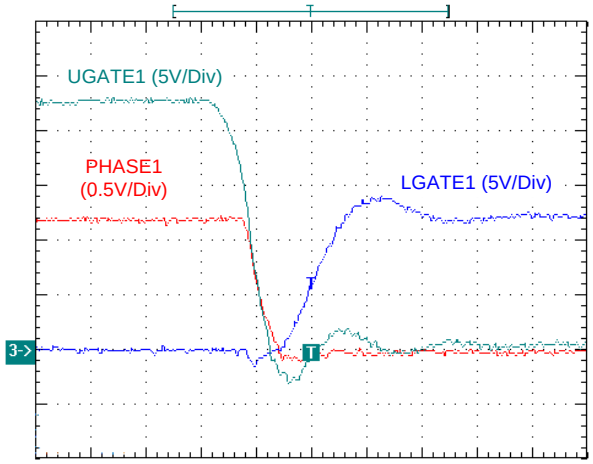
Time: (10ms)

Power Play



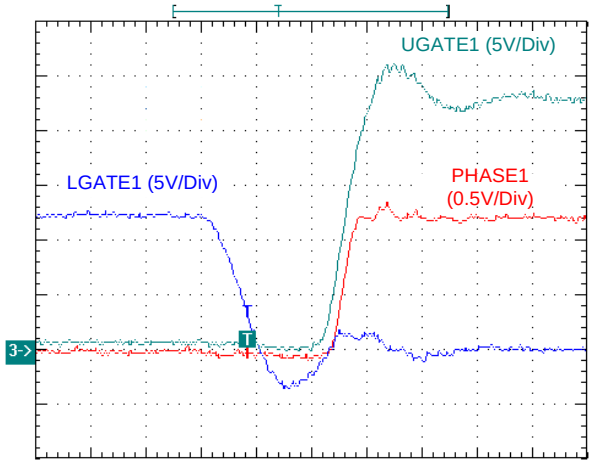
Time: (10ms)

Gate Waveforms (UGATE Falling)



Time: (25ns)

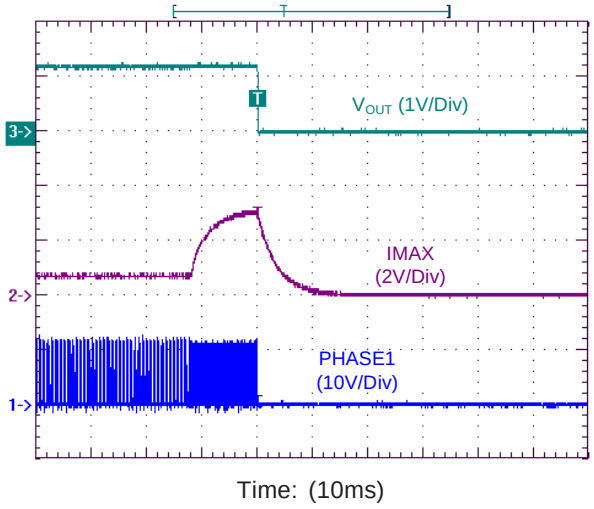
Gate Waveforms (UGATE Rising)



Time: (25ns)

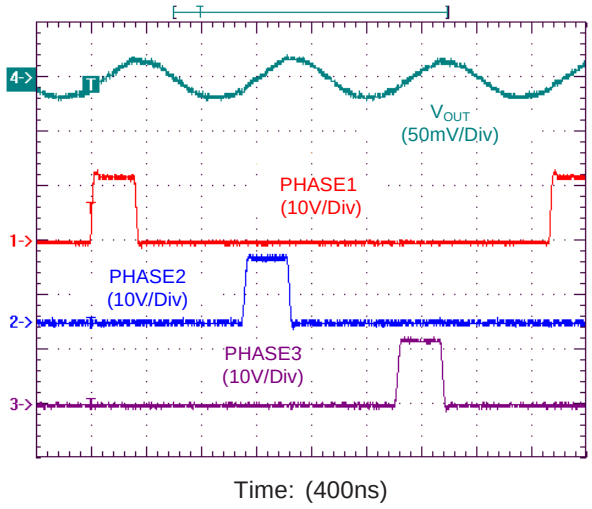
Typical Operation Characteristics

Over Current Protection



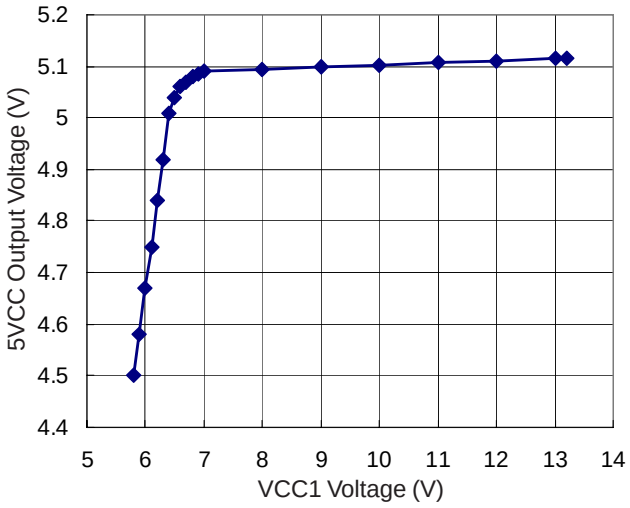
Time: (10ms)

Steady State Operation

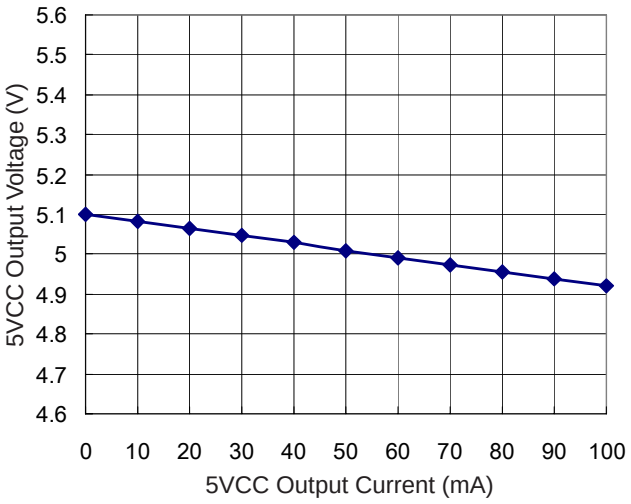


Time: (400ns)

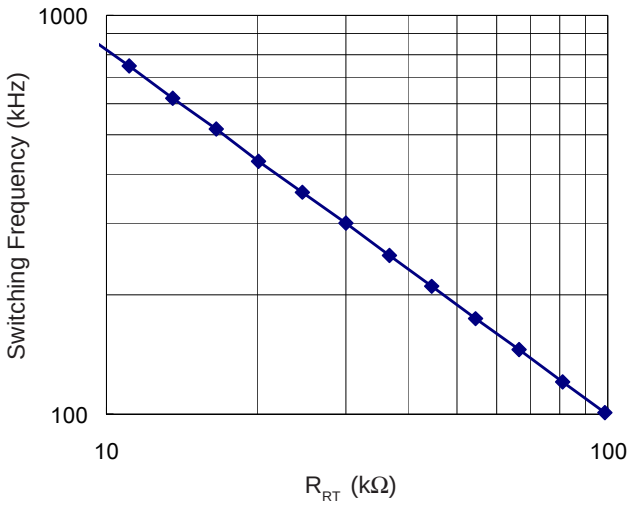
5VCC Line Regulation



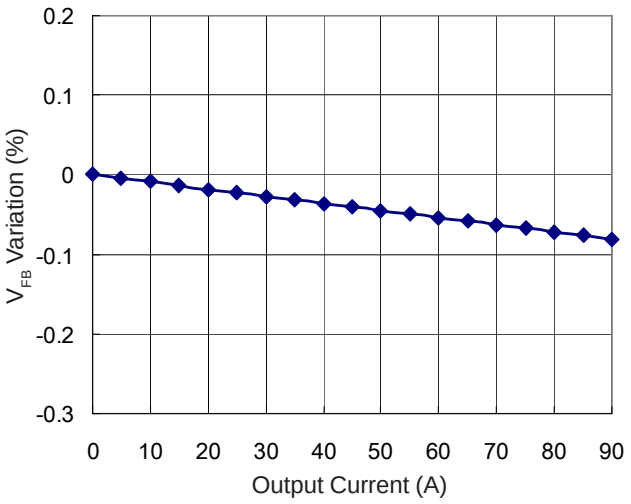
5VCC Load Regulation



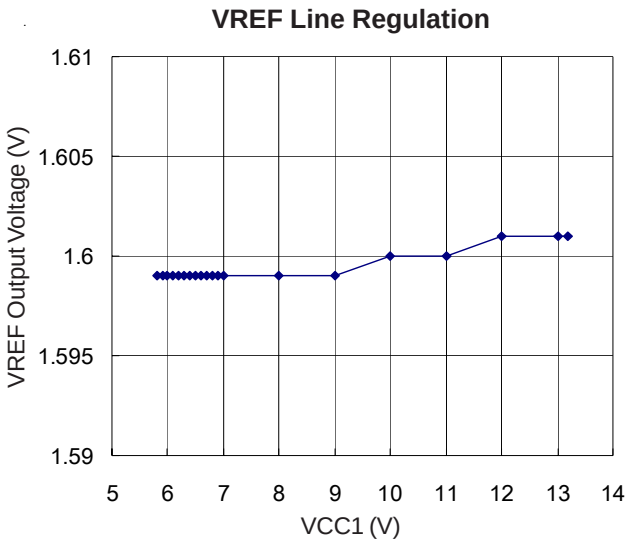
Switching Frequency

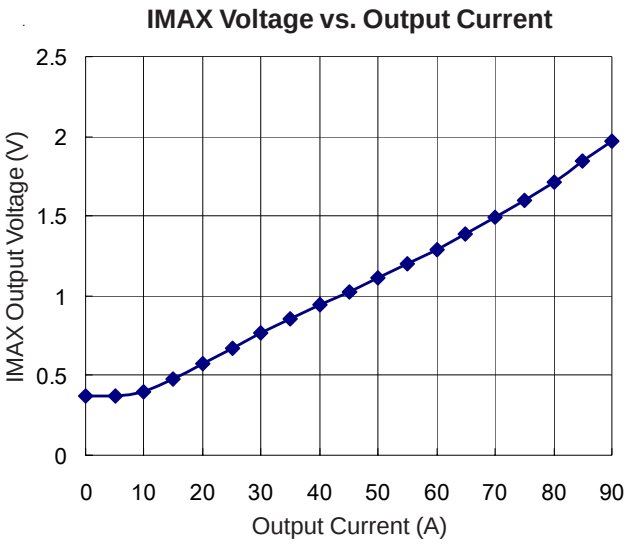


V_{FB} Loag Regulation



Typical Operation Characteristics





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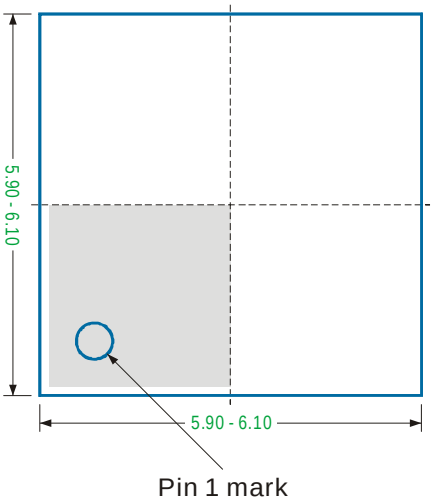
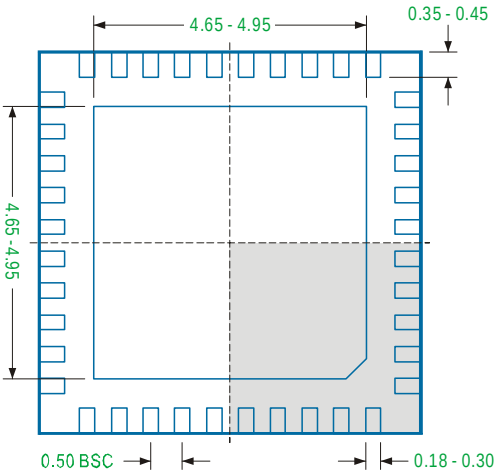
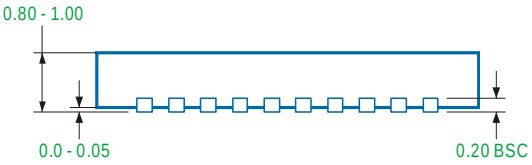
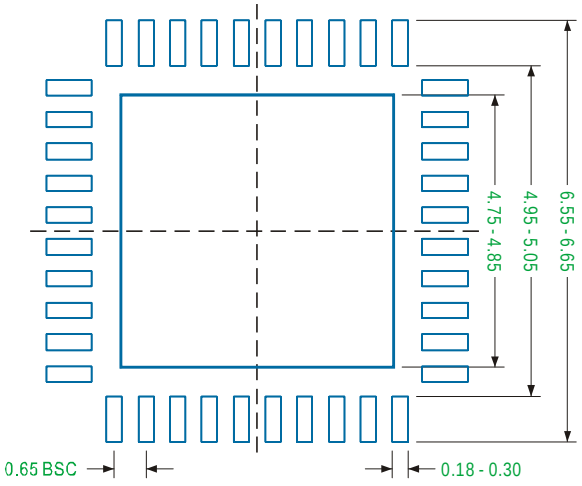
Package Information





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.