

**Schematics Page Index (Title / Revision / Change Date)**

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.0	07'07'17	36	PCI (i.LINK) 2/3	1.0	07'07'17
02	Block Diagram	1.0	07'07'17	37	PCI (SD/MS-DUO) 3/3	1.0	07'07'17
03	Merom(HOST BUS) 1/3	1.0	07'07'17	38	USB2.0	1.0	07'07'17
04	Merom(HOST BUS) 2/3	1.0	07'07'17	39	LAN (88E8039)	1.0	07'07'17
05	Merom(Power/Gnd) 3/3	1.0	07'07'17	40	LAN Transformer	1.0	07'07'17
06	CLOCK GEN	1.0	07'07'17	41	Touch/Lid/LED	1.0	07'07'17
07	Crestline (HOST) 1/7	1.0	07'07'17	42	Power Bottom & USB Board	1.0	07'07'17
08	Crestline (DMI) 2/7	1.0	07'07'17	43	Power Design Diagram	1.0	07'07'17
09	Crestline (GRAPHIC) 3/7	1.0	07'07'17	44	DCIN&Charger	1.0	07'07'17
10	Crestline (DDRII) 4/7	1.0	07'07'17	45	SYS Power (+3_3V/+5V)	1.0	07'07'17
11	Crestline (POWER,VCC) 5/7	1.0	07'07'17	46	SYS Power(+1_5V/+1_05V)	1.0	07'07'17
12	Crestline (VCC CORE) 6/7	1.0	07'07'17	47	DDR2 Power(+1_8V/+0_9V)	1.0	07'07'17
13	Crestline (VSS) 7/7	1.0	07'07'17	48	CPU_Vcore---ISL6262A	1.0	07'07'17
14	DDRII(SO-DIMM_0) 1/3	1.0	07'07'17	49	Others power plane	1.0	07'07'17
15	DDRII(SO-DIMM_1) 2/3	1.0	07'07'17	50	OVP protection	1.0	07'07'17
16	DDRII(Termination) 3/3	1.0	07'07'17	51	GMCH power	1.0	07'07'17
17	CRT	1.0	07'07'17	52	HOLE	1.0	07'07'17
18	LVDS	1.0	07'07'17	53	History ( 1 )	1.0	07'07'17
19	ICH8-M( PCI/USB ) 1/5	1.0	07'07'17	54	History ( 2 )	1.0	07'07'17
20	ICH8-M( LPC,IDE,SATA )2/5	1.0	07'07'17	55	History ( 3 )	1.0	07'07'17
21	ICH8-M( GPIO) 3/5	1.0	07'07'17	56	History ( 4 )	1.0	07'07'17
22	ICH8-M( POWER) 4/5	1.0	07'07'17	57	History ( 5 )	1.0	07'07'17
23	ICH8-M( GND) 5/5	1.0	07'07'17	58			
24	SATA HDD/CD-ROM	1.0	07'07'17	59			
25	EC+KBC(3910)	1.0	07'07'17	60			
26	Flash ROM/XBUS	1.0	07'07'17	61			
27	Mini-PCIE Card	1.0	07'07'17	62			
28	OIDE/MODEM	1.0	07'07'17	63			
29	EXPRESS	1.0	07'07'17	64			
30	AUDIO(CODEC/POWER) 1/4	1.0	07'07'17	65			
31	AUDIO( AMP/HP/SPK) 2/4	1.0	07'07'17	66			
32	AUDIO( EXTMIC) 3/4	1.0	07'07'17	67			
33	AUDIO(MUTE) 4/4	1.0	07'07'17	68			
34	FAN/Thermal-Sensor	1.0	07'07'17	69			
35	PCI (PCI BUS) 1/3	1.0	07'07'17	70			

**M720 Main Board**

**M/B P/N:** 1P-0076102-6010 (FUBAI)  
 1P-0076200-6010 (NANYA)  
 1P-0076502-6010 (HANSTAR)  
 1P-0076G00-6010 (TRIPOD)

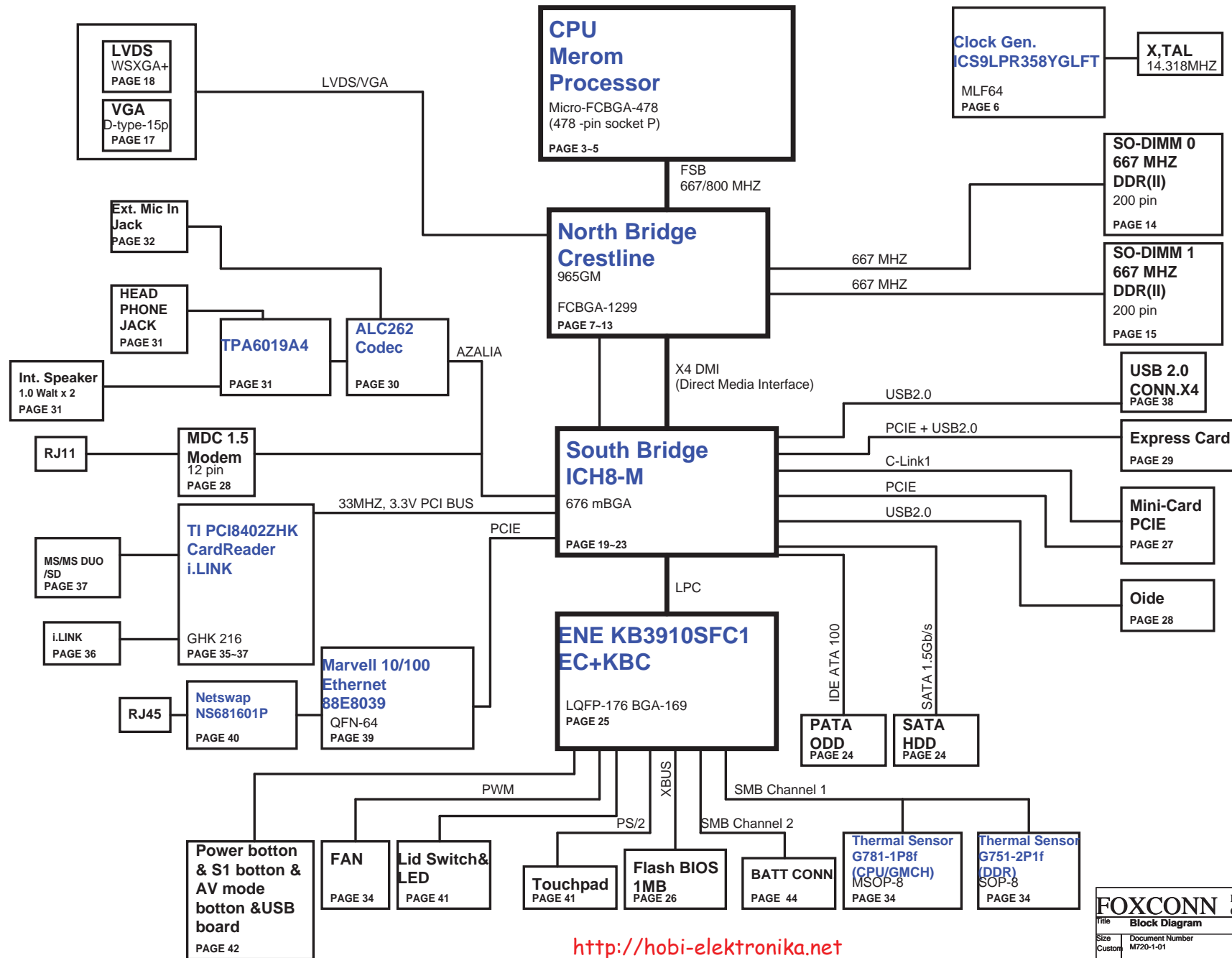
**P/B P/N:** 1P-1076105-6010 (FUBAI)  
 1P-1076200-6010 (NANYA)  
 1P-1076505-6010 (HANSTAR)  
 1P-1076G00-6010 (TRIPOD)

**U/B P/N:** 1P-1076106-6010 (FUBAI)  
 1P-1076201-6010 (NANYA)  
 1P-1076506-6010 (HANSTAR)  
 1P-1076G01-6010 (TRIPOD)

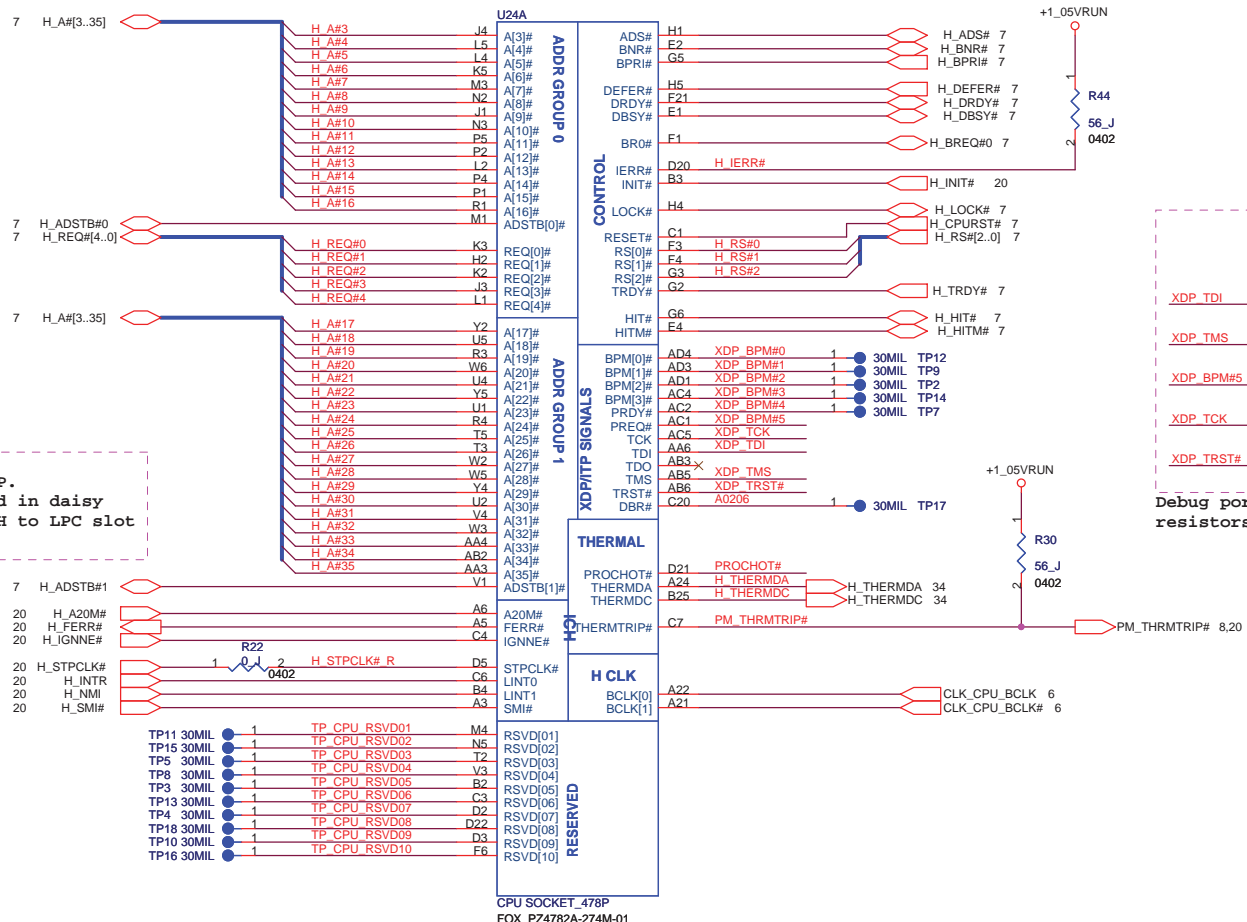
P. Leader	Check by	Design by

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Index Page	
Size	Document Number	Rev
A3	M720-1-01	1.0
Date:	Wednesday, July 18, 2007	Sheet 1 of 56

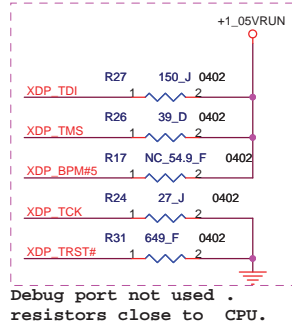
# M720(Crestline GM Block Diagram)



<http://hobi-elektronika.net>



**Layout note:**  
no stub on H\_STPCLK TP.  
H\_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

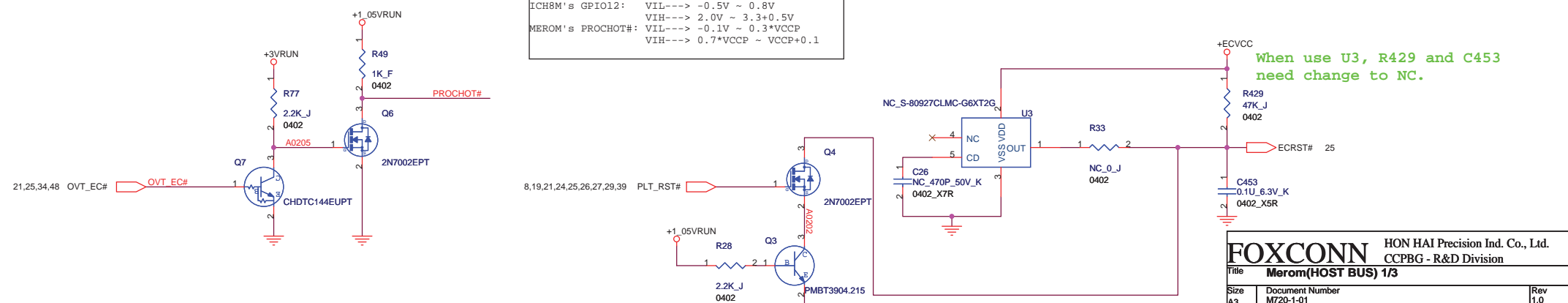


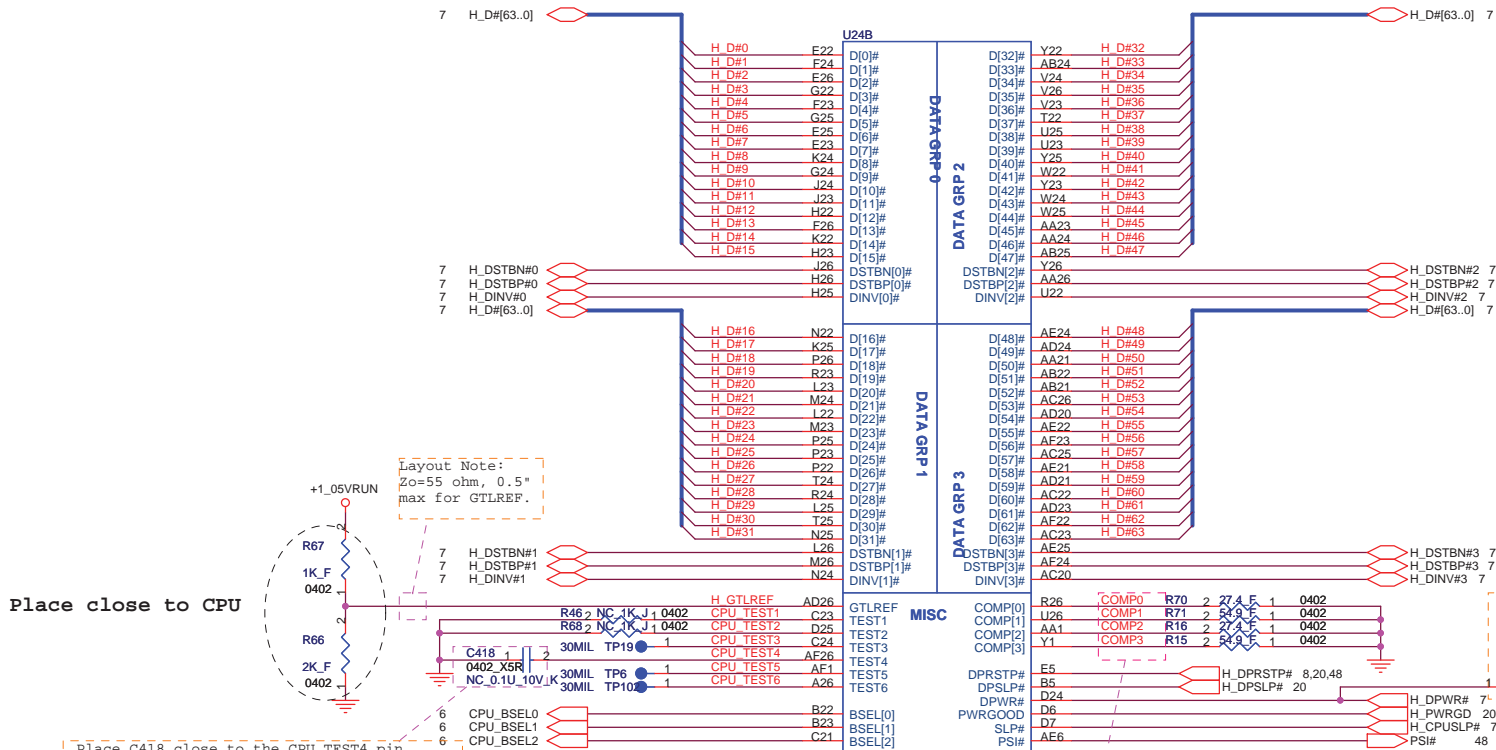
Debug port not used. resistors close to CPU.

PM\_THRMTRIP# should connect to ICH8-M and GMCH without T-ing (No stub)

ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V  
VIH---> 2.0V ~ 3.3+0.5V  
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3\*VCCP  
VIH---> 0.7\*VCCP ~ VCCP+0.1

When use U3, R429 and C453 need change to NC.





Layout Note:  
 $Z_0=55 \text{ ohm}$ , 0.5"  
 max for GTLREF.

Place close to CPU

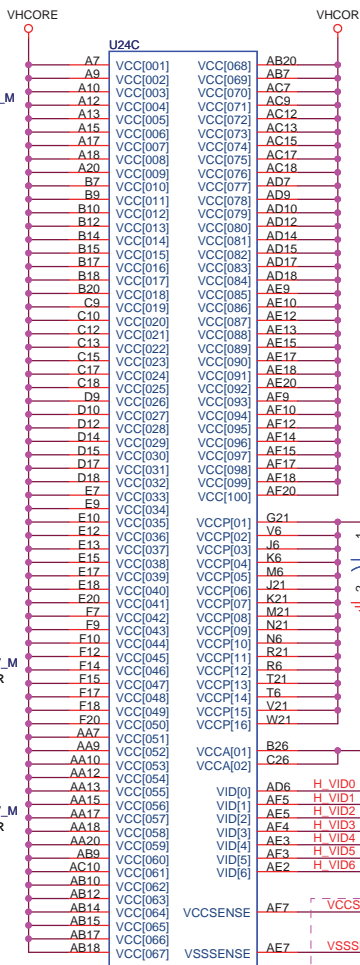
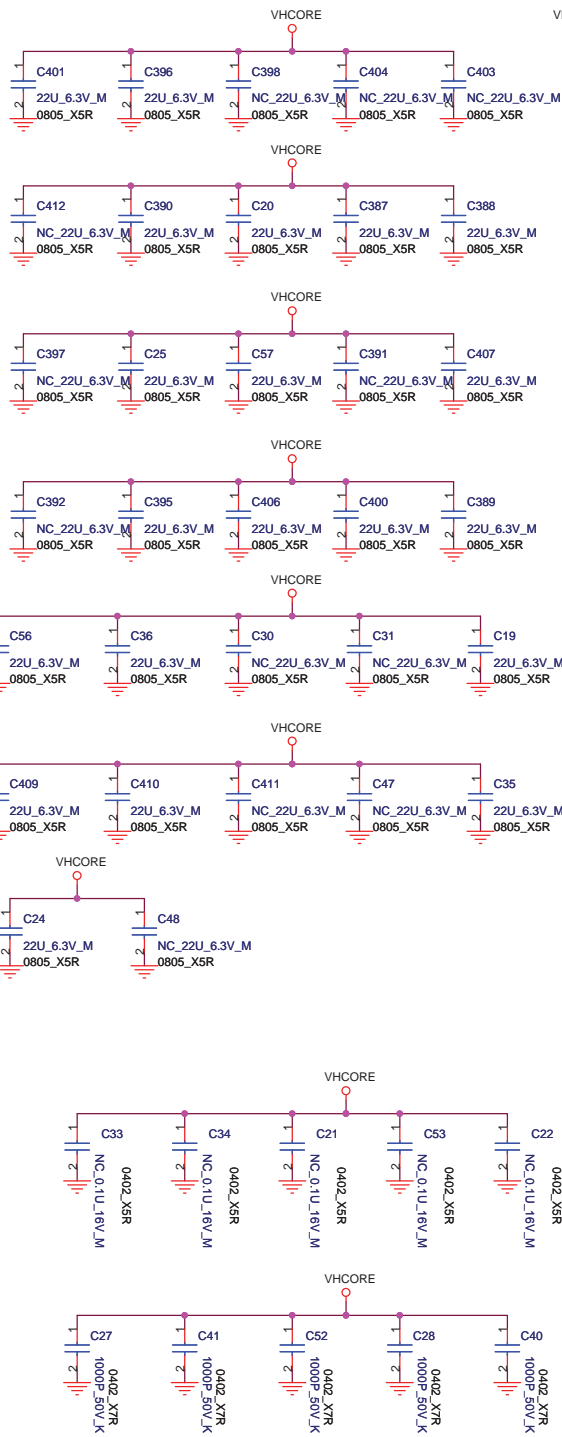
Place C418 close to the CPU\_TEST4 pin.  
 Make sure CPU\_TEST4 routing is reference  
 to GND and away from other noisy signals.

Layout:  
 Connect test  
 point with no  
 stub

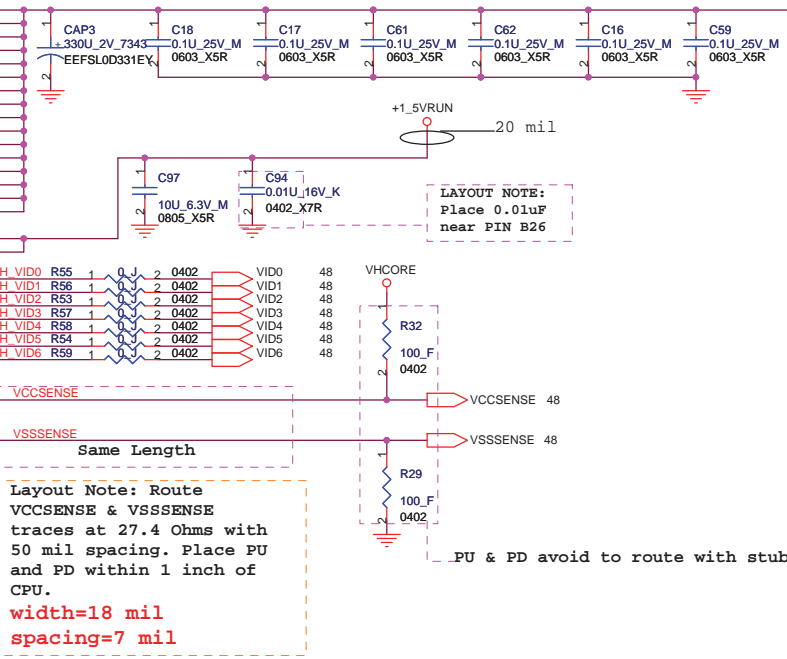
Layout Note:  
 Comp0,2 connect with  $Z_0=27.4 \text{ ohm}$ , make  
 trace length shorter then 0.5".  
 Comp1,3 connect with  $Z_0=55 \text{ ohm}$ , make  
 trace length shorter then 0.5".

IMVP6 (ISL6262ACRZ-T)  
 cpu PSI# <-> ISL6262ACRZ-T PSI#  
 ISL6262ACRZ-T: VIHmin=0.315V  
 VILmax=0.735V  
 (ref. IMVP-6 NO:18904)

CPU SOCKET\_478P  
 FOX\_P24782A-274M-01



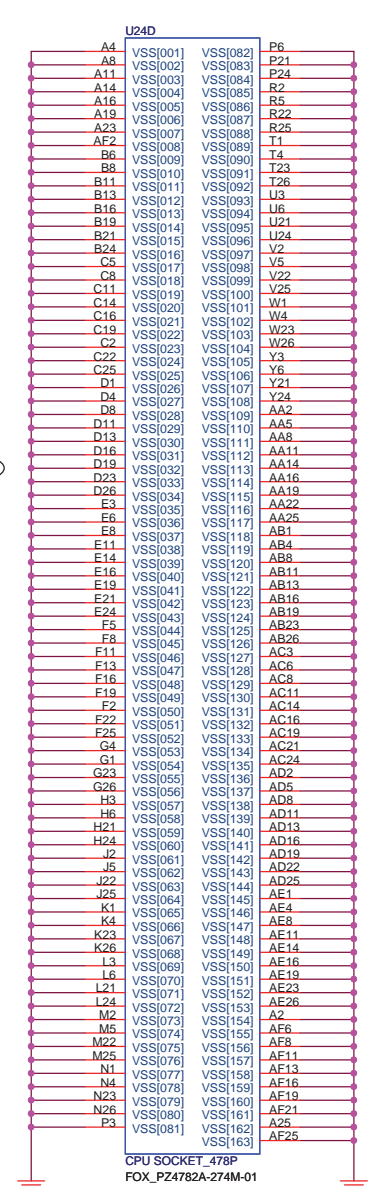
CPU\_VCCA----->120mA  
 CPU\_VCCP----->2.5A  
 CPU\_VCC----->36A

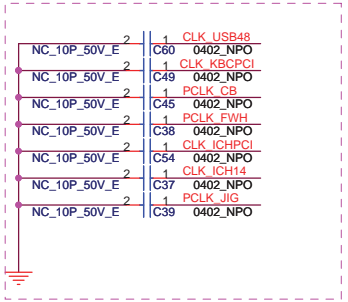
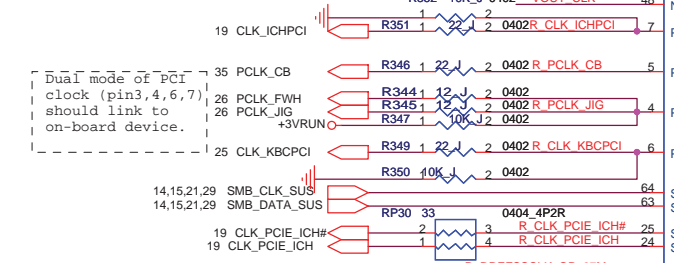
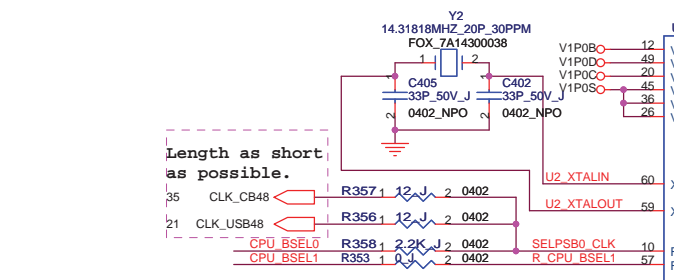
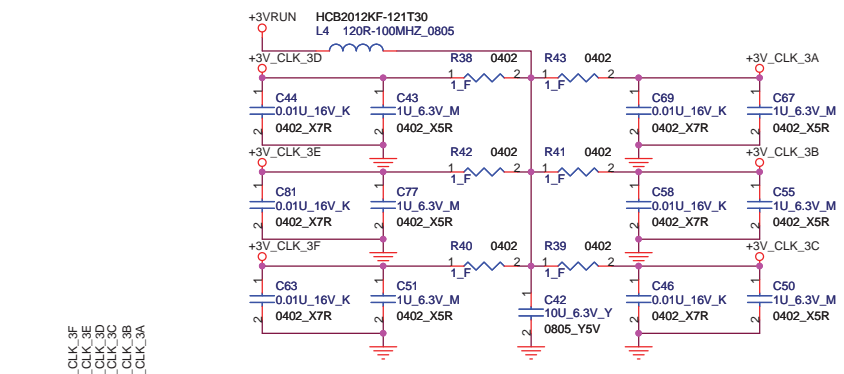
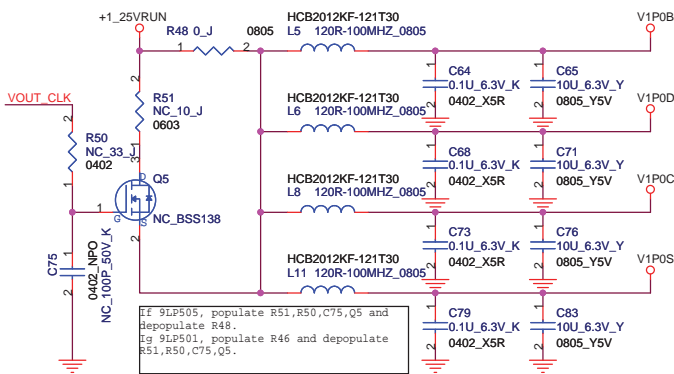


LAYOUT NOTE:  
Place 0.1uF near PIN B26

Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of CPU.  
 width=18 mil  
 spacing=7 mil

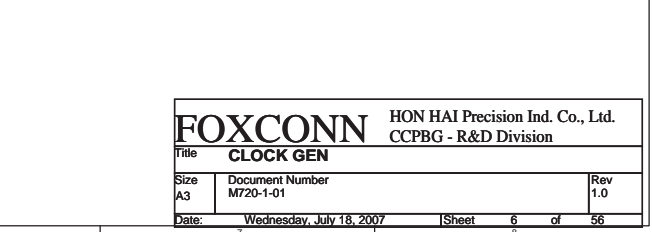
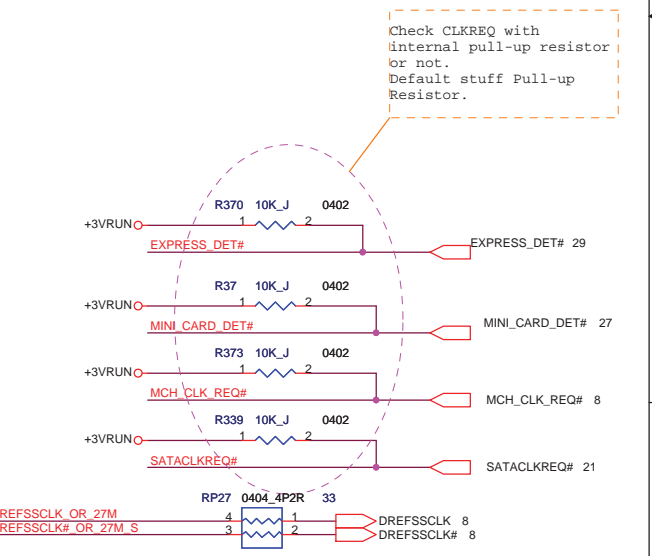
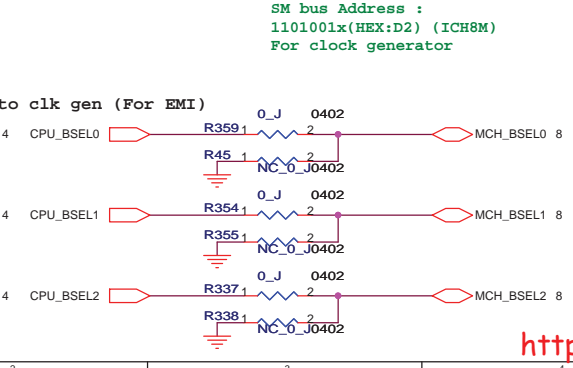
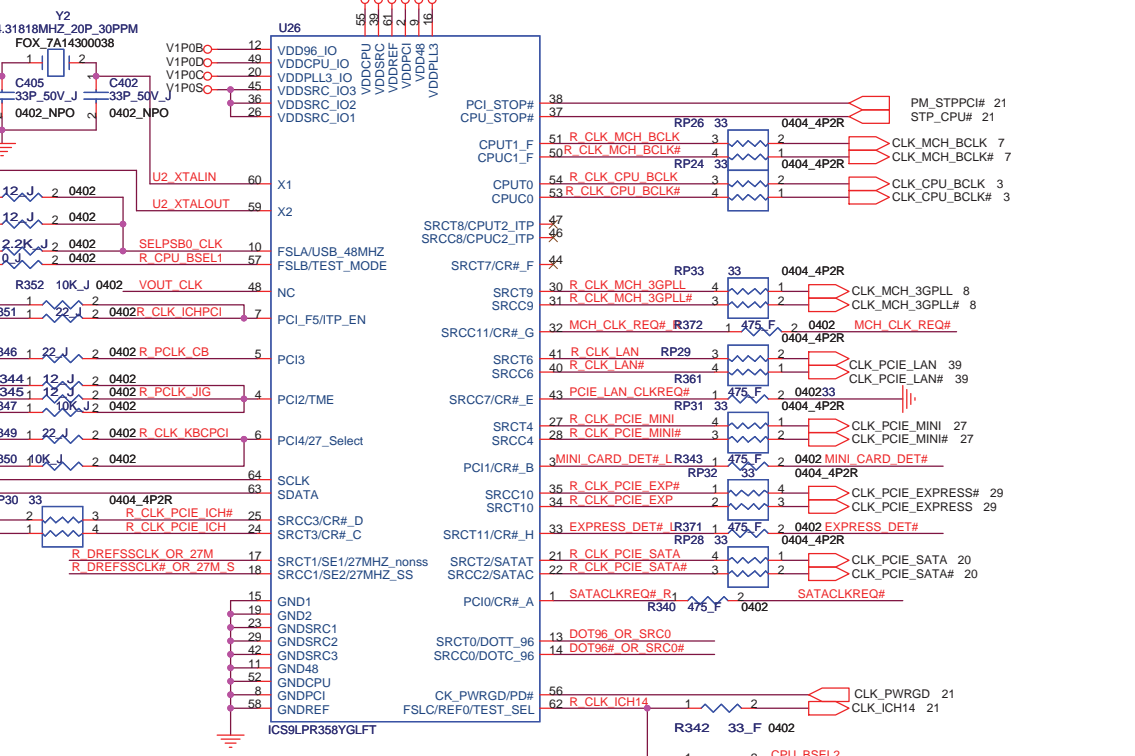
PU & PD avoid to route with stub



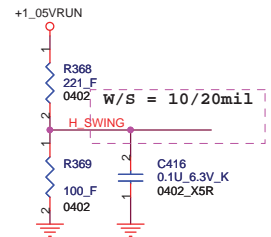


**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33



Check CLKREQ# with internal pull-up resistor or not. Default stuff Pull-up Resistor.



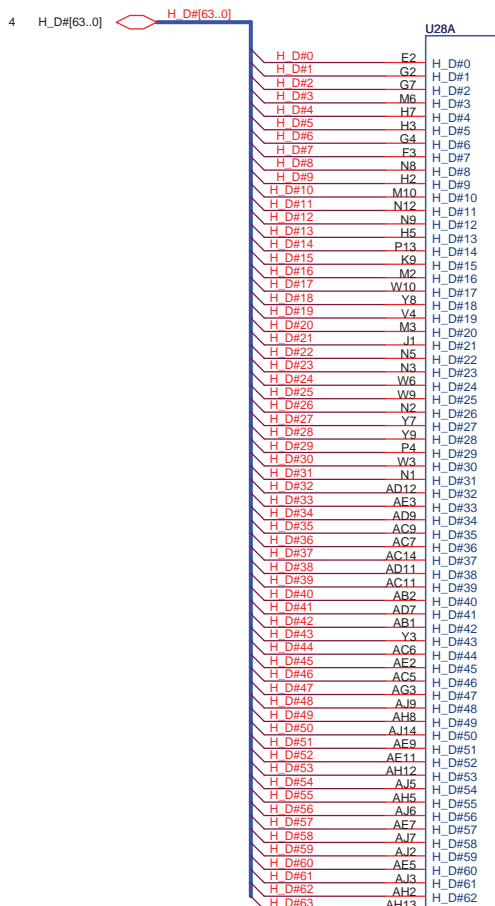
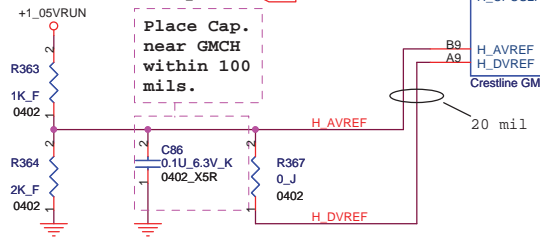
W/S = 10/20mil  
H\_RCOMP



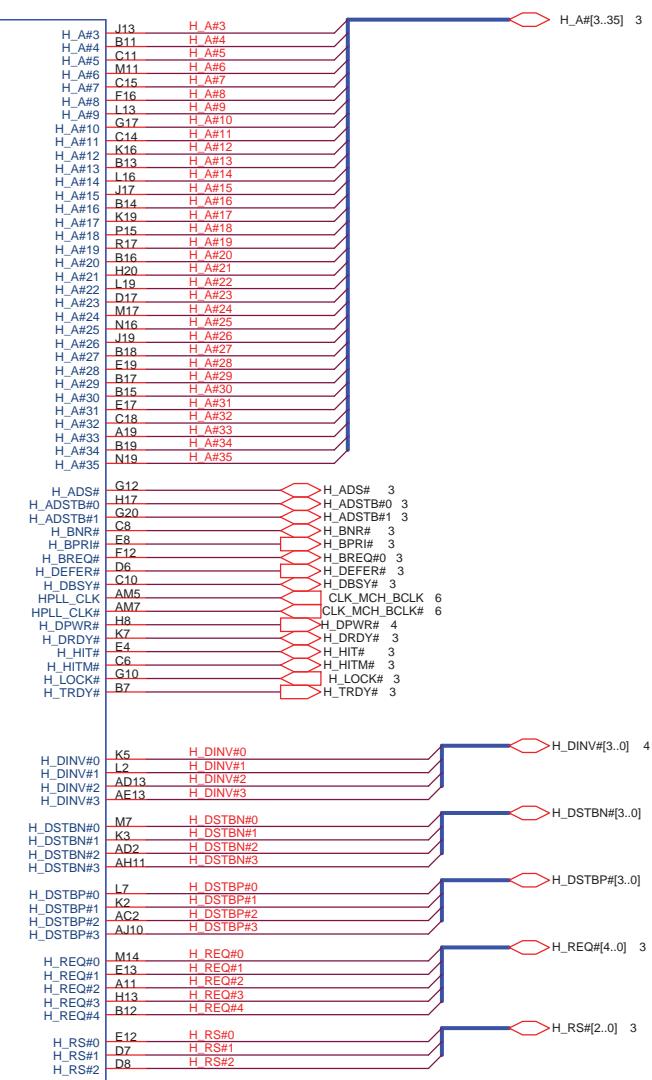
H\_SCOMP

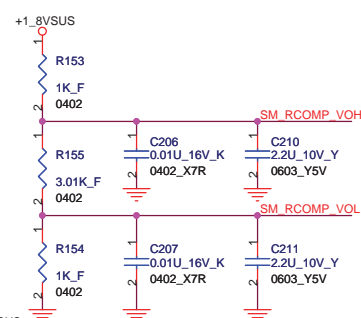
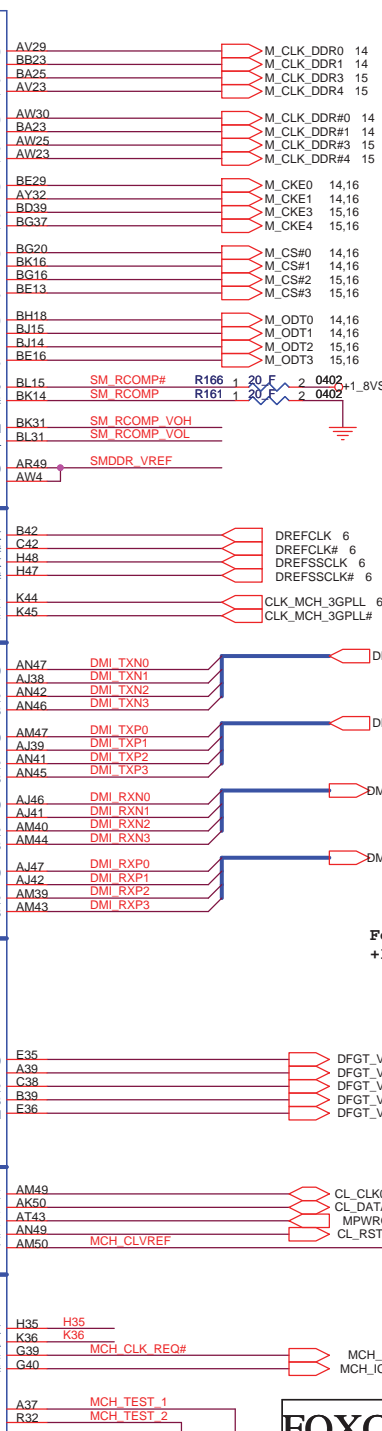
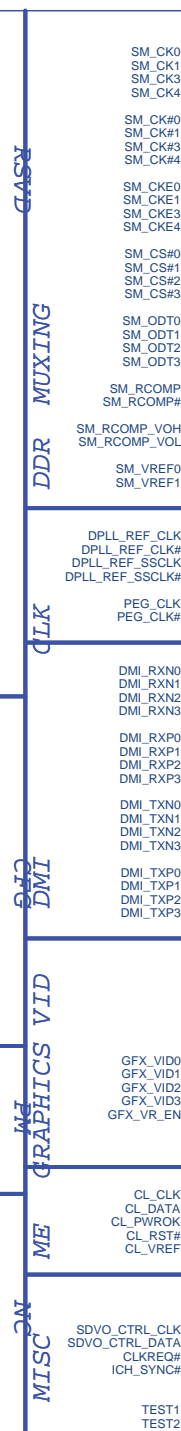
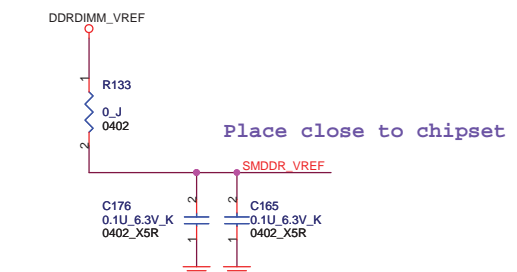
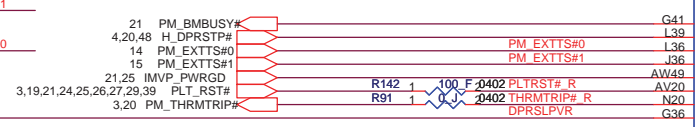
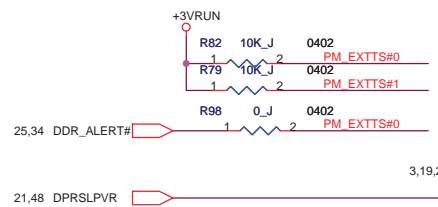
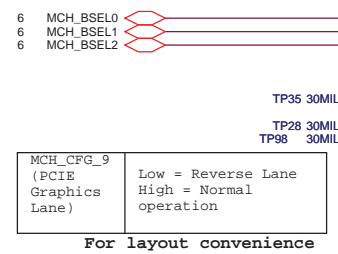
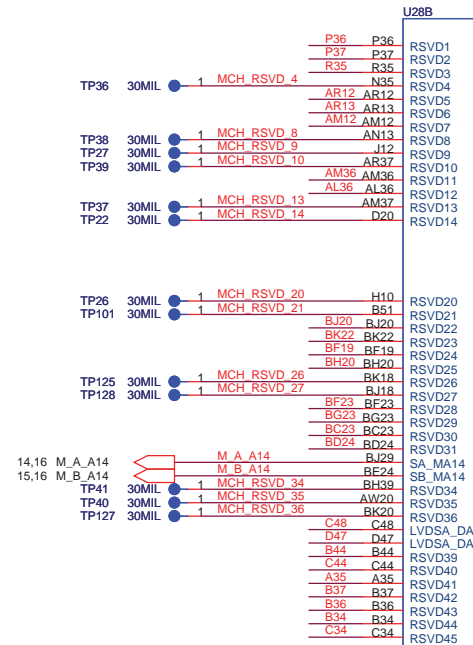


H\_SCOMP#

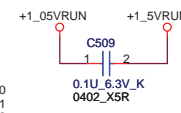


HOST





For CL\_CLK0 and CL\_DATA0 through +1\_05VRUN, +1\_5VRUN.

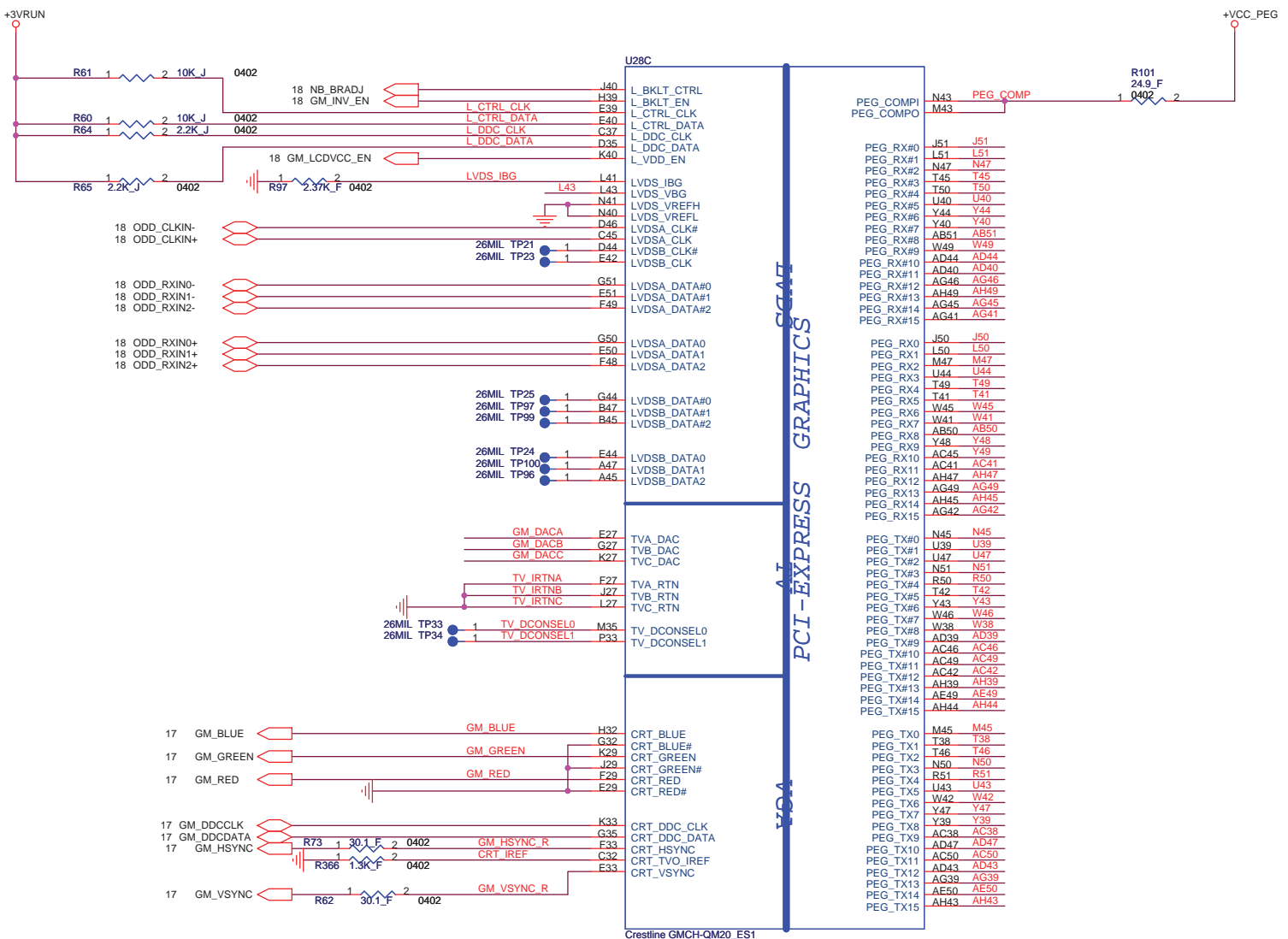


Crestline GMCH-QM20\_ES1

<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Crestline (DMI) 2/7		CCPBG - R&D Division	
Title	Document Number	Rev	
M720-1-01	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	8 of 56



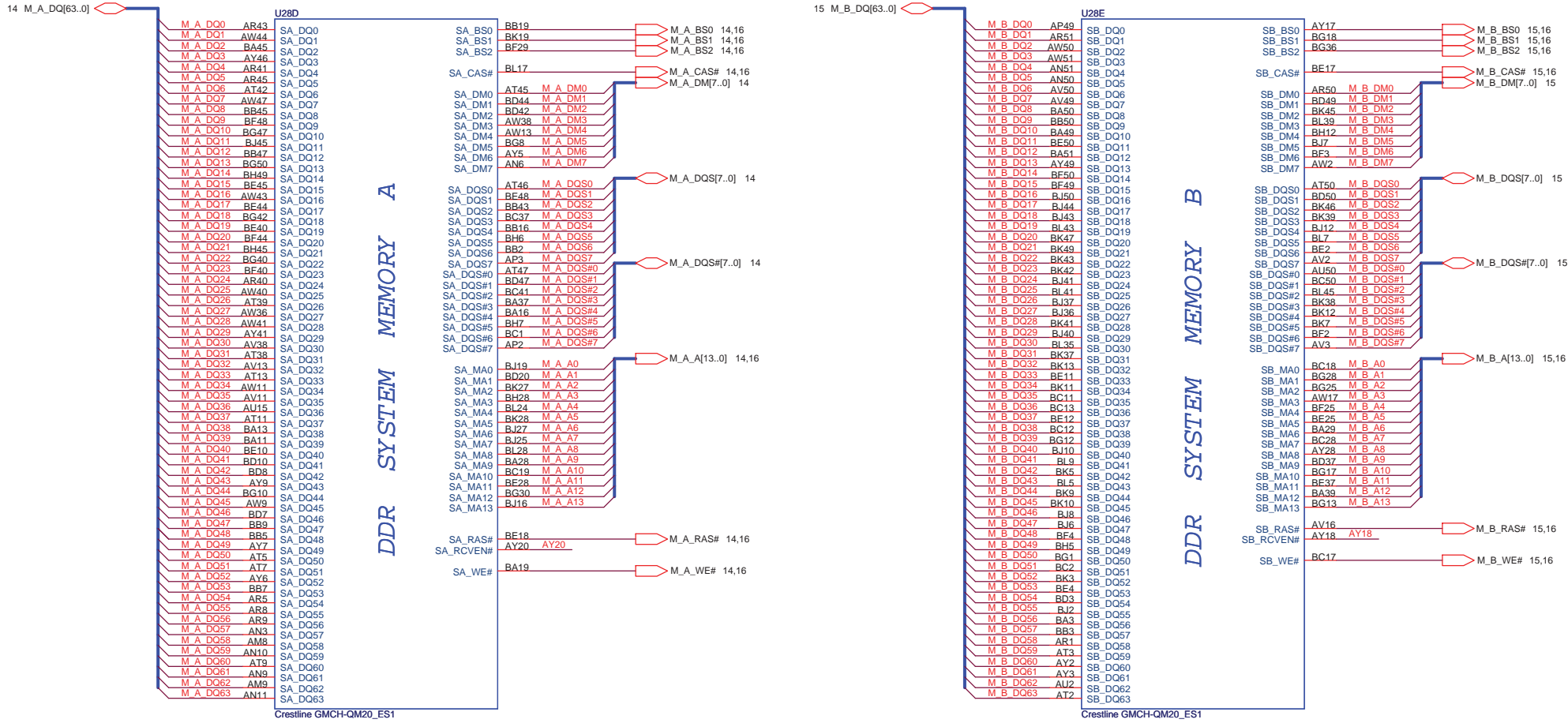


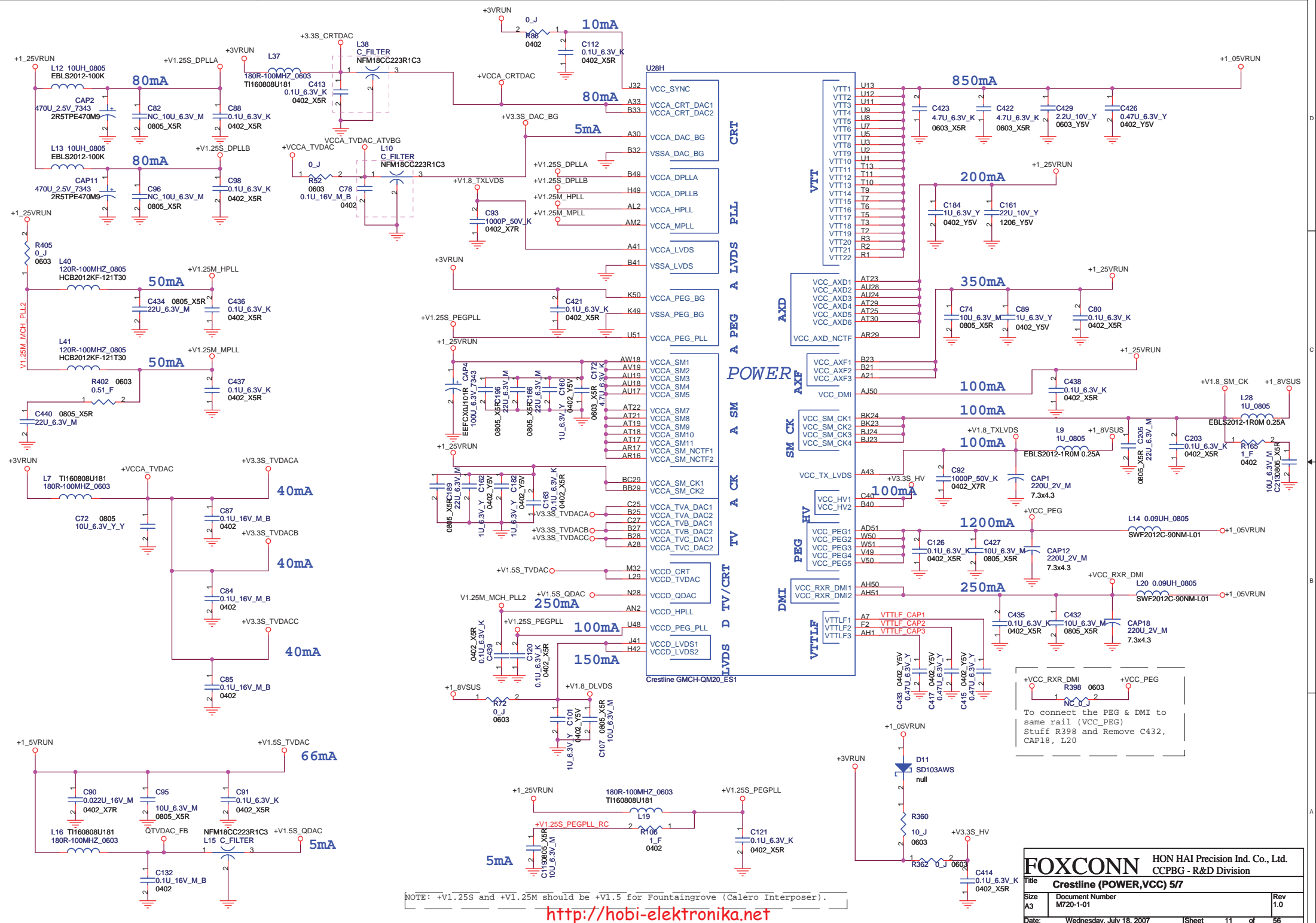
Crestline GMCH-QM20\_ES1



GMCH-QM20  
 PCI-EXPRESS GRAPHICS  
 VGA

PEG_COMP1	N43	PEG_COMP	1	0402	2
PEG_COMP0	M43				
PEG_RX#0	J51	J51			
PEG_RX#1	L51	L51			
PEG_RX#2	N47	N47			
PEG_RX#3	T45	T45			
PEG_RX#4	T50	T50			
PEG_RX#5	U40	U40			
PEG_RX#6	Y44	Y44			
PEG_RX#7	Y40	Y40			
PEG_RX#8	AB51	AB51			
PEG_RX#9	W49	W49			
PEG_RX#10	AD44	AD44			
PEG_RX#11	AD40	AD40			
PEG_RX#12	AG46	AG46			
PEG_RX#13	AH49	AH49			
PEG_RX#14	AG45	AG45			
PEG_RX#15	AG41	AG41			
PEG_RX0	J50	J50			
PEG_RX1	L50	L50			
PEG_RX2	M47	M47			
PEG_RX3	U44	U44			
PEG_RX4	T49	T49			
PEG_RX5	T41	T41			
PEG_RX6	W45	W45			
PEG_RX7	W41	W41			
PEG_RX8	AB50	AB50			
PEG_RX9	Y48	Y48			
PEG_RX10	AC45	Y49			
PEG_RX11	AC41	AC41			
PEG_RX12	AH47	AH47			
PEG_RX13	AG49	AG49			
PEG_RX14	AH45	AH45			
PEG_RX15	AG42	AG42			
PEG_TX#0	N45	N45			
PEG_TX#1	U39	U39			
PEG_TX#2	U47	U47			
PEG_TX#3	N51	N51			
PEG_TX#4	R50	R50			
PEG_TX#5	T42	T42			
PEG_TX#6	Y43	Y43			
PEG_TX#7	W46	W46			
PEG_TX#8	W38	W38			
PEG_TX#9	AD39	AD39			
PEG_TX#10	AC46	AC46			
PEG_TX#11	AC49	AC49			
PEG_TX#12	AC42	AC42			
PEG_TX#13	AH38	AH38			
PEG_TX#14	AE49	AE49			
PEG_TX#15	AH44	AH44			
PEG_TX0	M45	M45			
PEG_TX1	T38	T38			
PEG_TX2	T46	T46			
PEG_TX3	N50	N50			
PEG_TX4	U43	U43			
PEG_TX5	W42	W42			
PEG_TX6	Y47	Y47			
PEG_TX7	Y39	Y39			
PEG_TX8	AC38	AC38			
PEG_TX9	AD47	AD47			
PEG_TX10	AC50	AC50			
PEG_TX11	AD43	AD43			
PEG_TX12	AG39	AG39			
PEG_TX13	AE50	AE50			
PEG_TX14	AH43	AH43			
PEG_TX15	AH43	AH43			





NOTE: +V1.25S and +V1.25M should be +V1.5 for Fountaingrove (Calero Interposer).

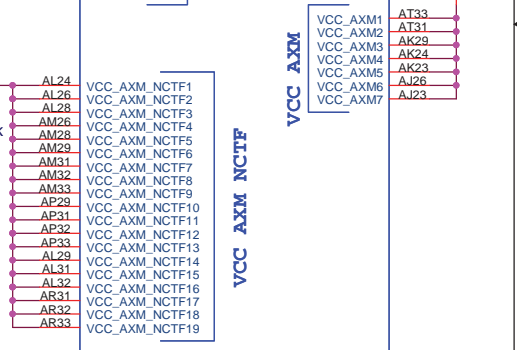
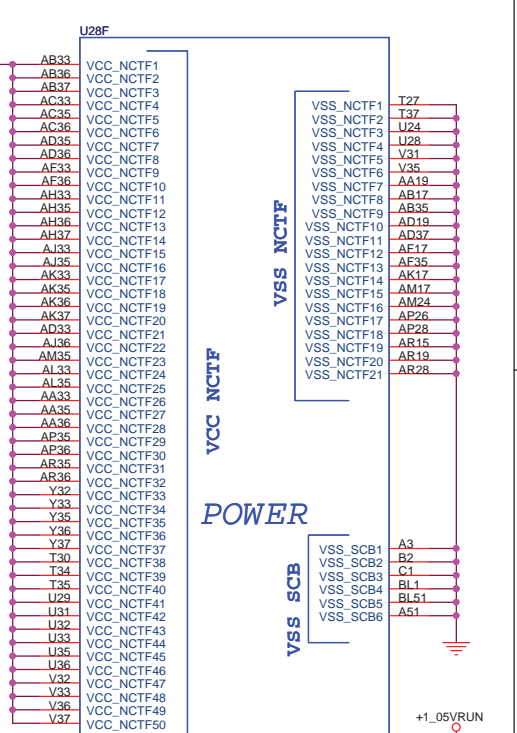
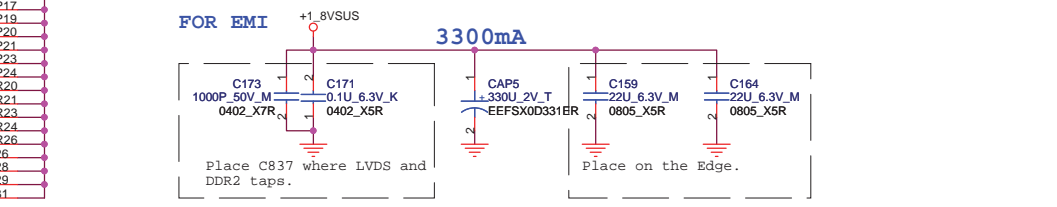
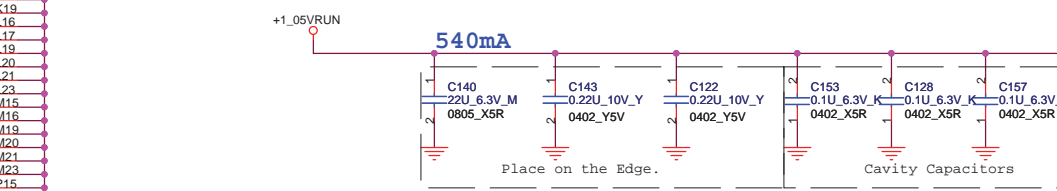
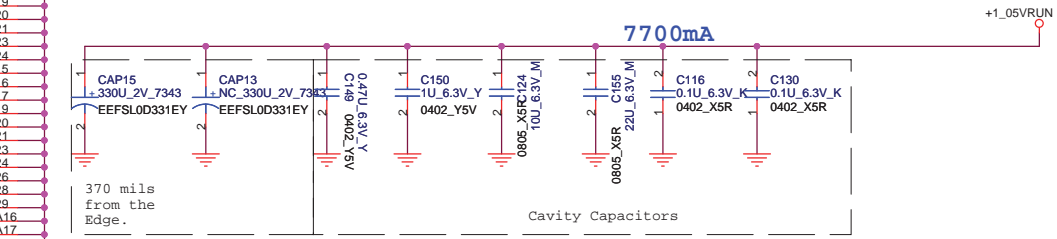
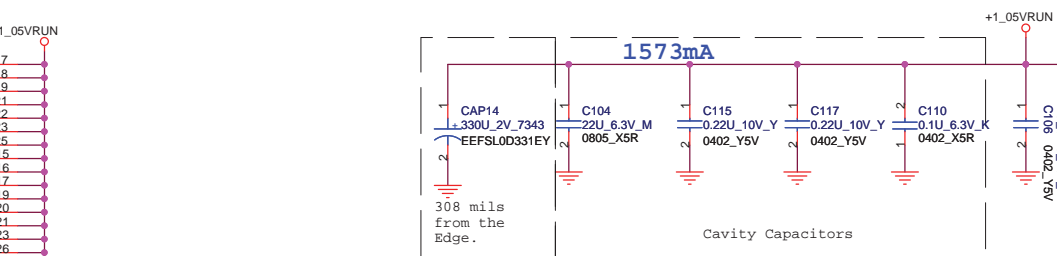
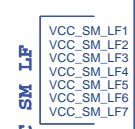
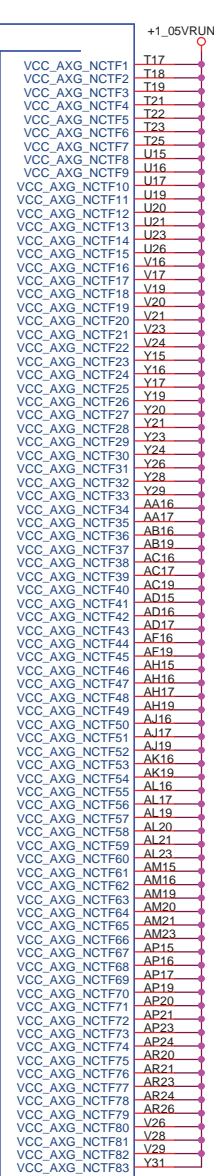
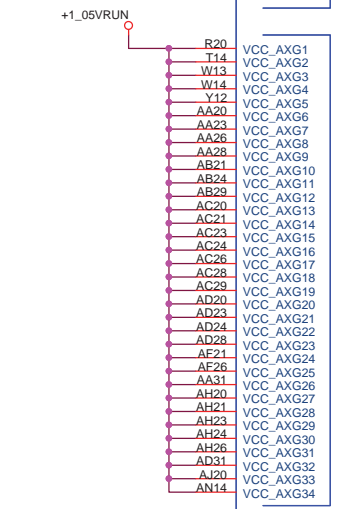
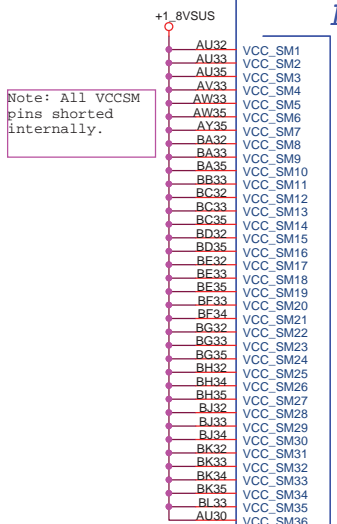
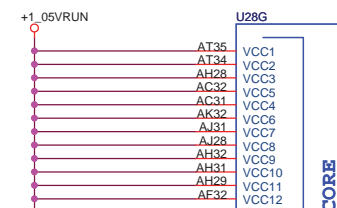
<http://hobi-elektronika.net>

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **Crestline (POWER,VCC) 57**

Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 11	of 56

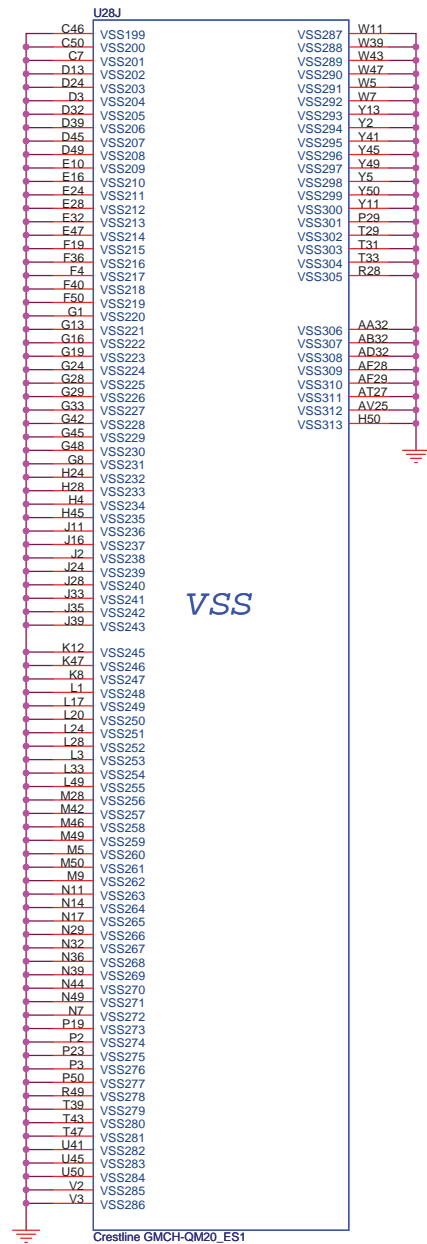
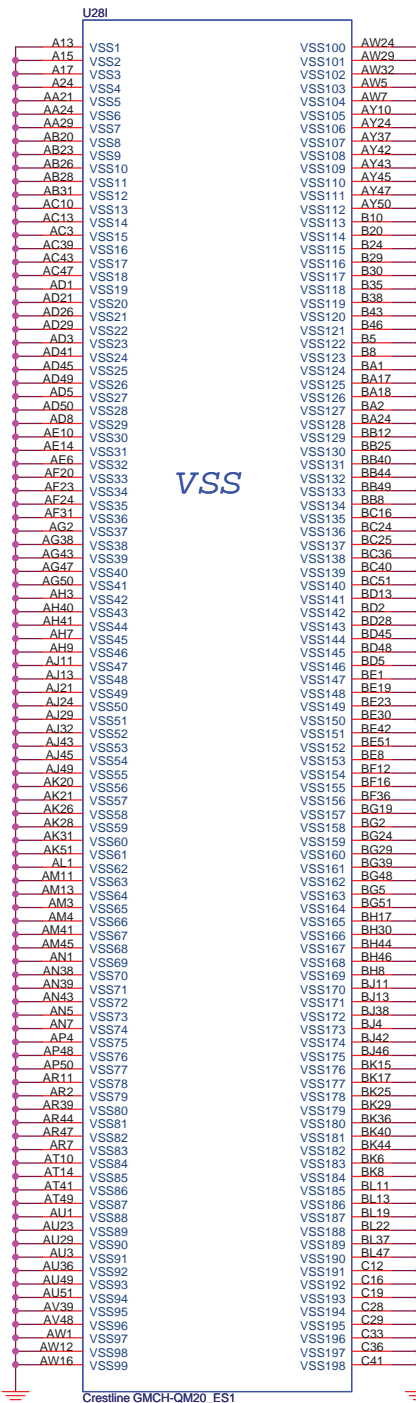
To connect the PEG & DMI to same rail (VCC\_PEG) Stuff R398 and Remove C432, CAP18, L20



**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **Crestline (VCC CORE) 67**

Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 12	of 56

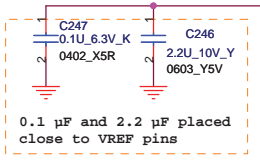


Crestline GMCH-QM20\_ES1

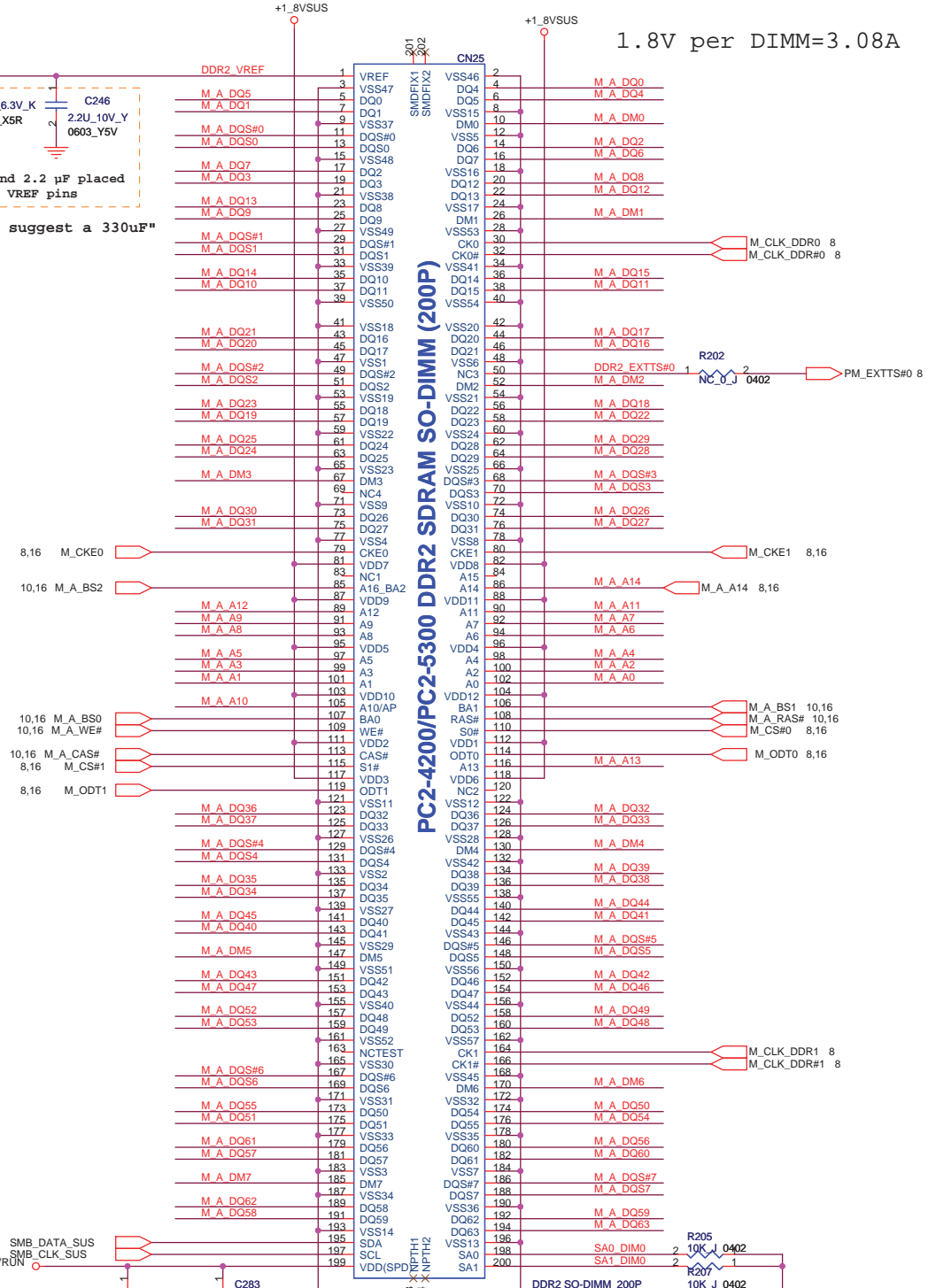
Crestline GMCH-QM20\_ES1

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Crestline (VSS) 7/7		CCPBG - R&D Division	
Title	Document Number	Rev	
Size	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	13 of 56

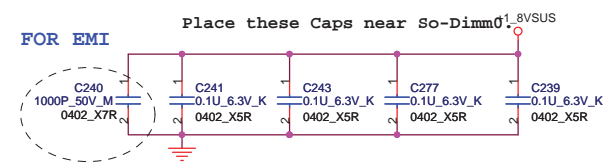
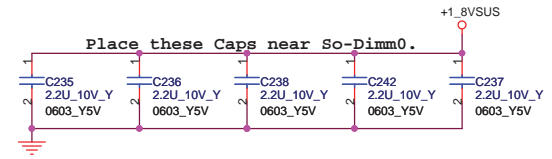
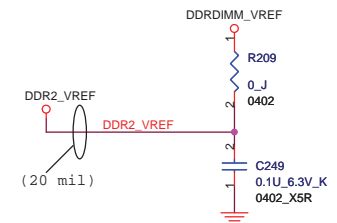
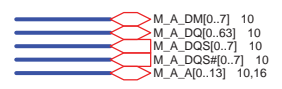
1.8V per DIMM=3.08A



"Intel check list suggest a 330uF"



PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

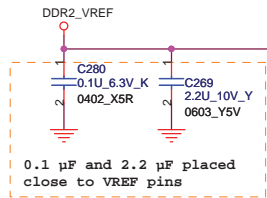


SMBus Address: A0 (W) / A1 (R)

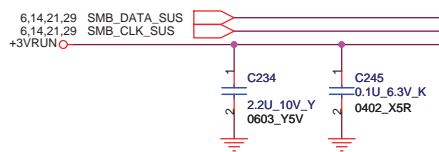
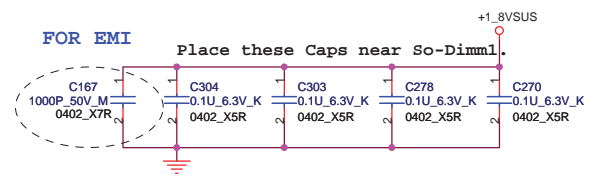
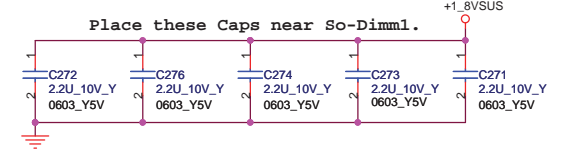
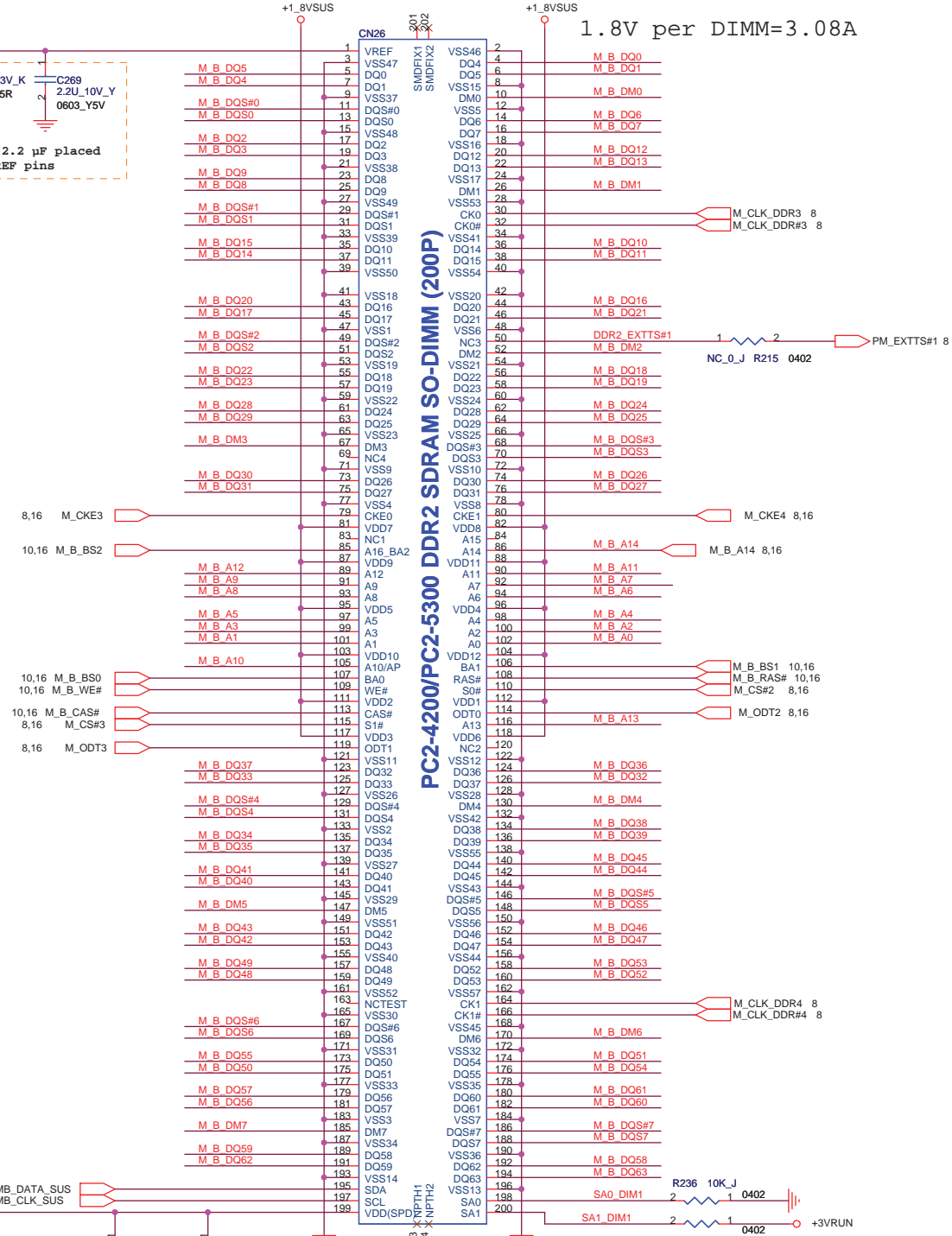
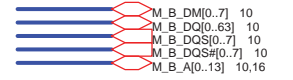
Place DIMM\_0 near CPU

<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>DDR(H)SO-DIMM_0</b>			
Size A3	Document Number M720-1-01	Rev 1.0	
Date: Wednesday, July 18, 2007	Sheet 14	of 56	



1.8V per DIMM=3.08A

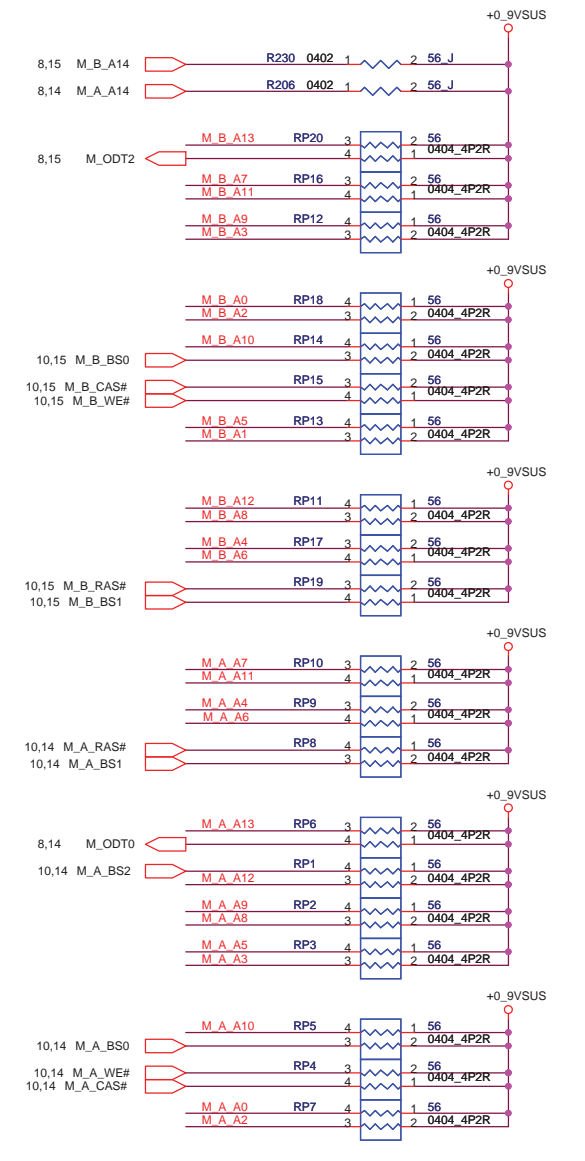
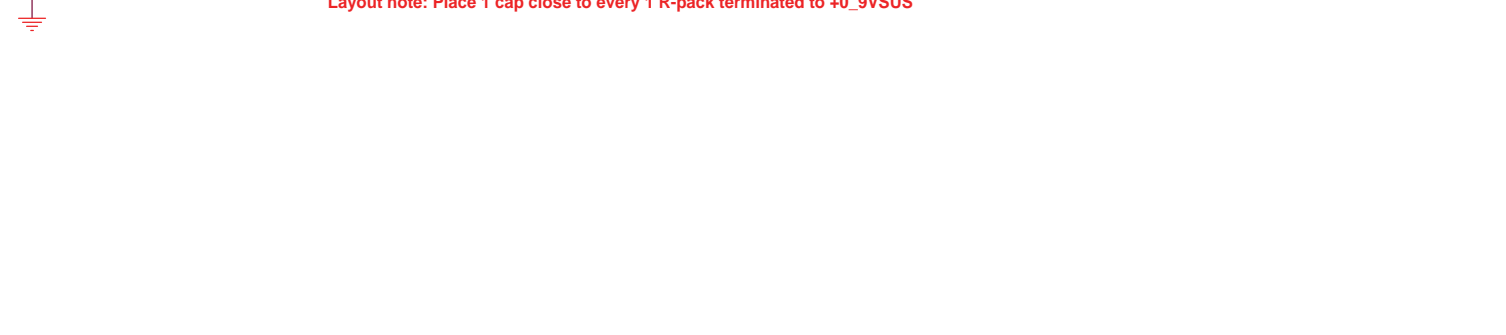
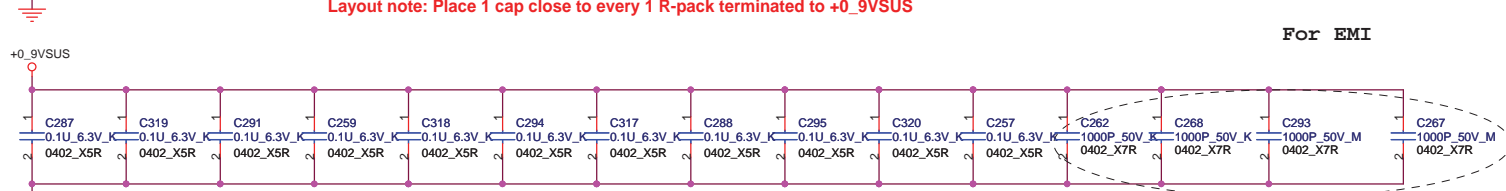
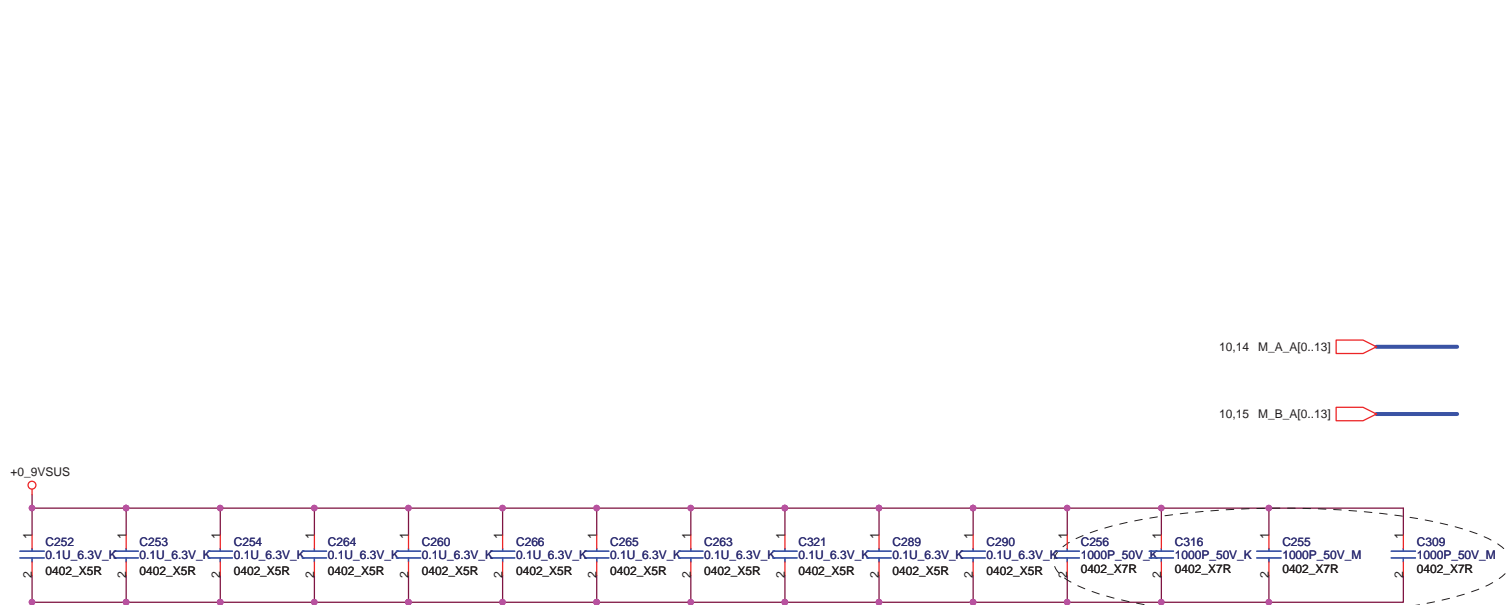


**DIMM\_1**

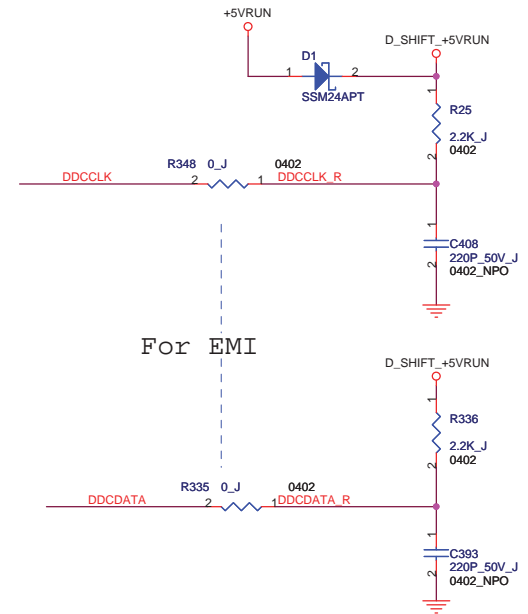
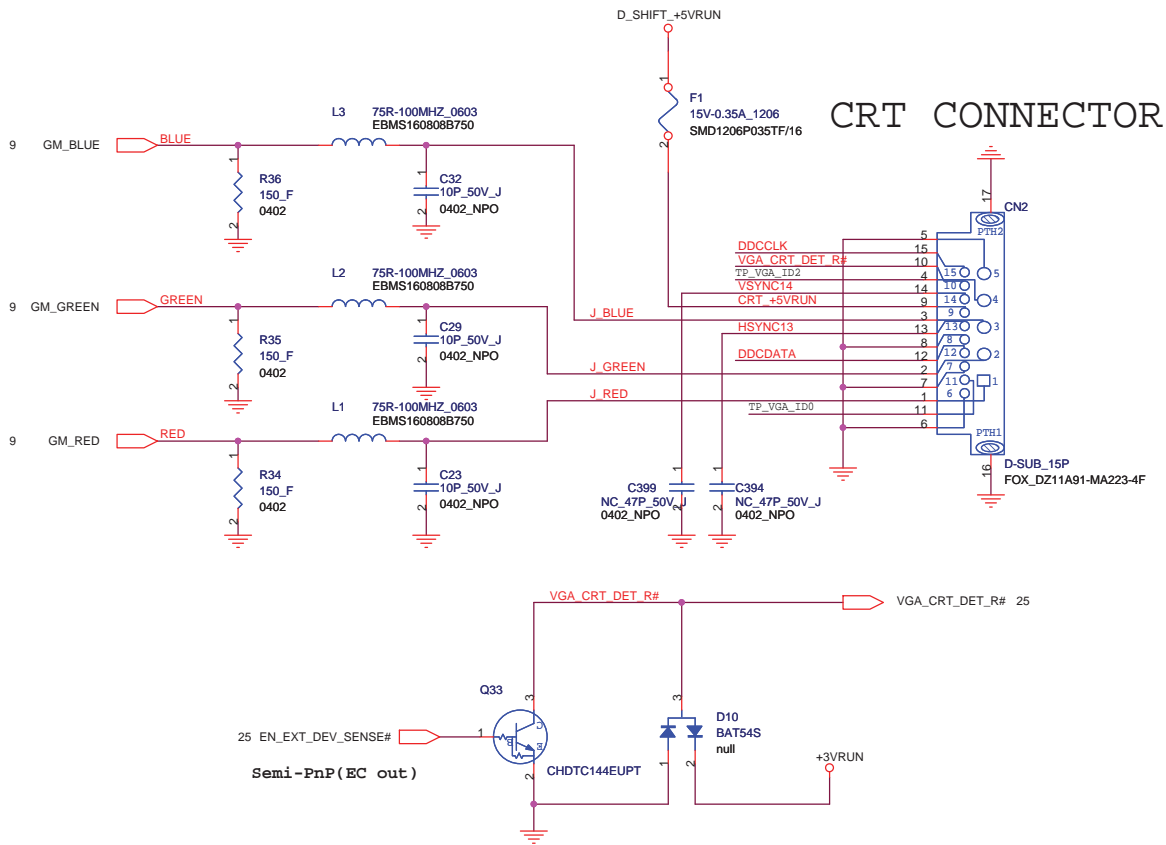
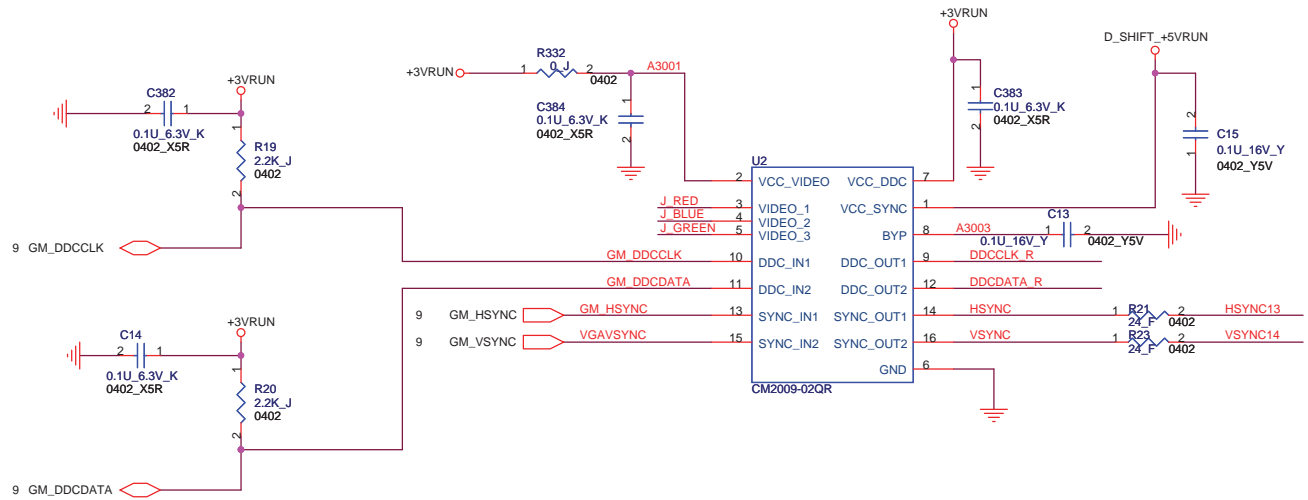
SMBus Address: A4(W)/A5(R)

DIMM 1 is placed farther from the GMCH than DIMM 0  
<http://hobi-elektronika.net>

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>DDR(II)SO-DIMM_1</b>		
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 15	of 56

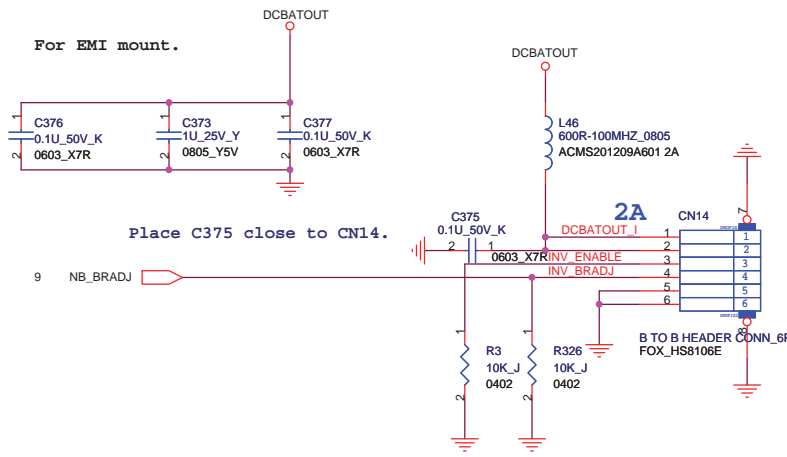
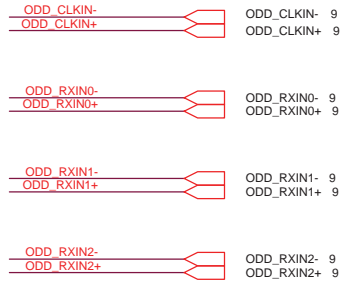




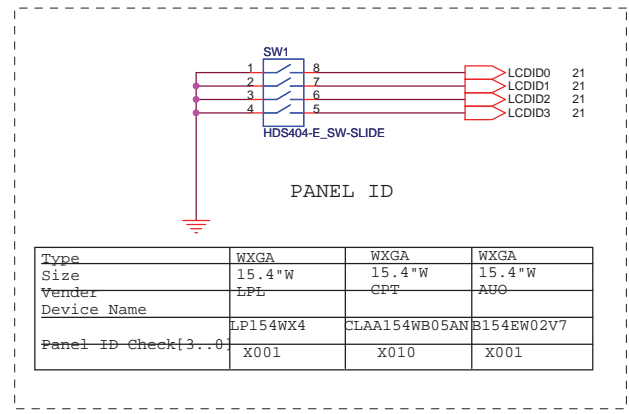
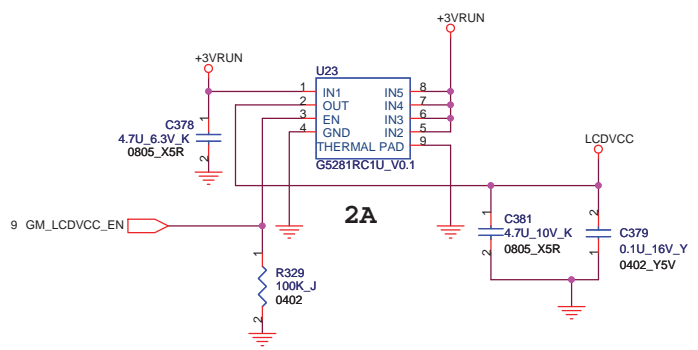
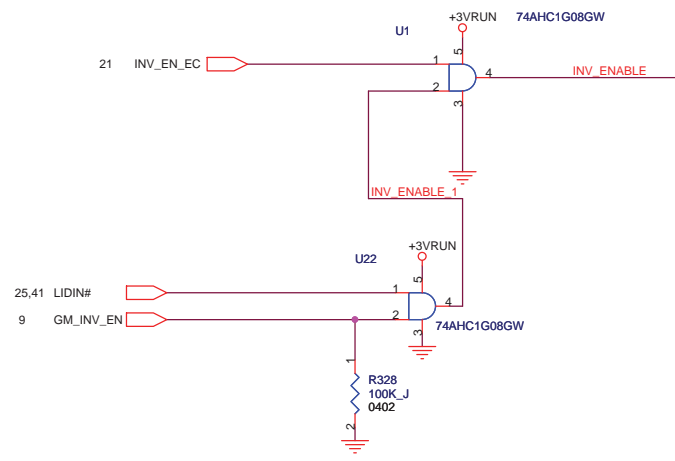
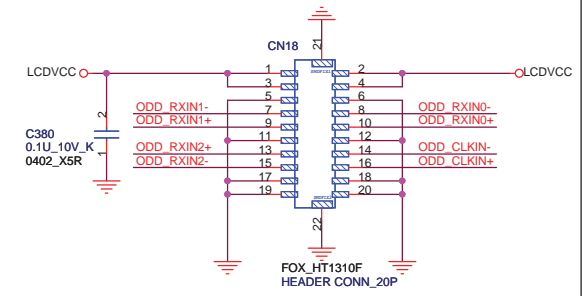


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.
Title		CCPBG - R&D Division
Title <b>CRT</b>		
Size	Document Number	Rev
A3	M720-1-01	1.0
Date:	Wednesday, July 18, 2007	Sheet 17 of 56

# LVDS



## INVERTER CONN.

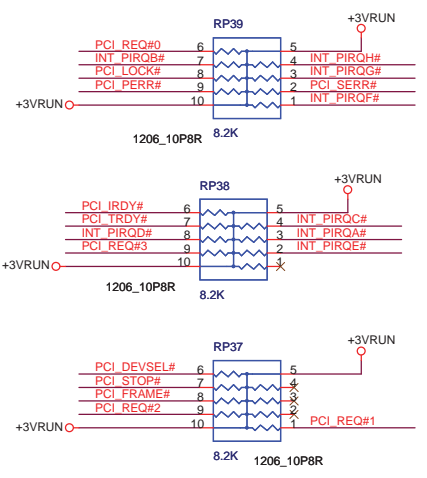


<http://hobi-elektronika.net>

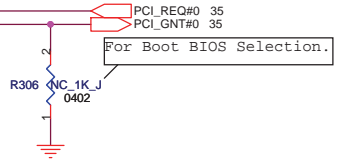
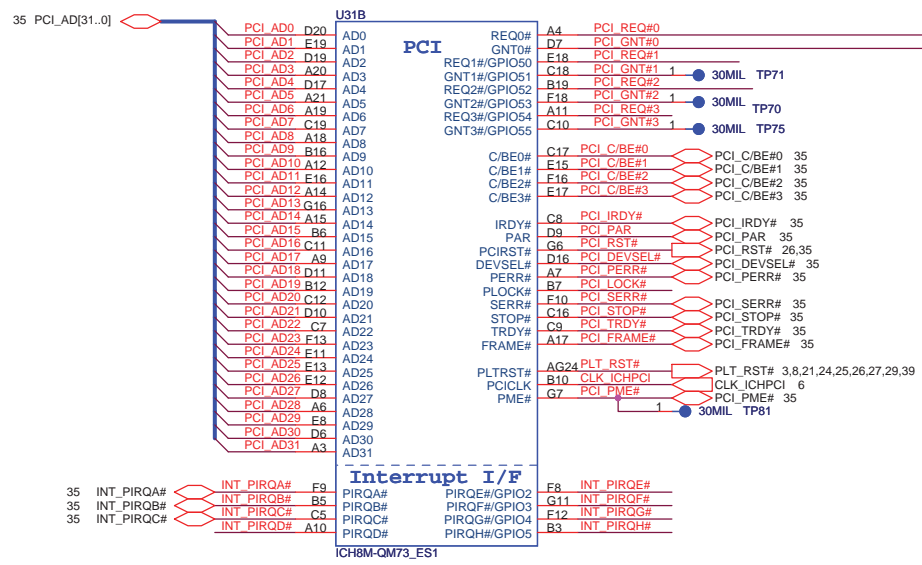
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title **LVDS**

Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 18	of 56



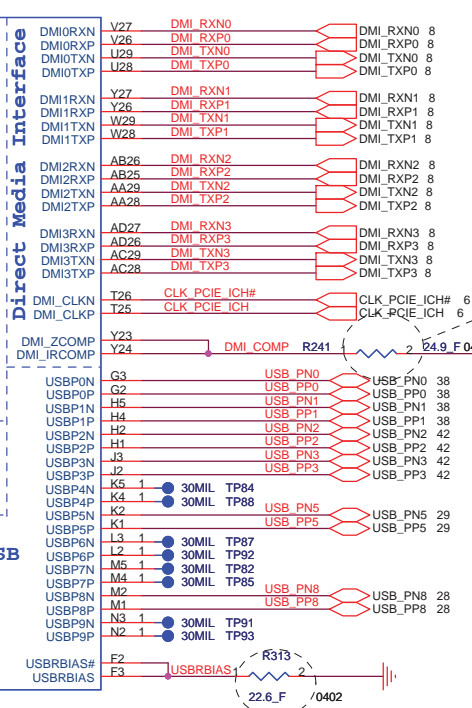
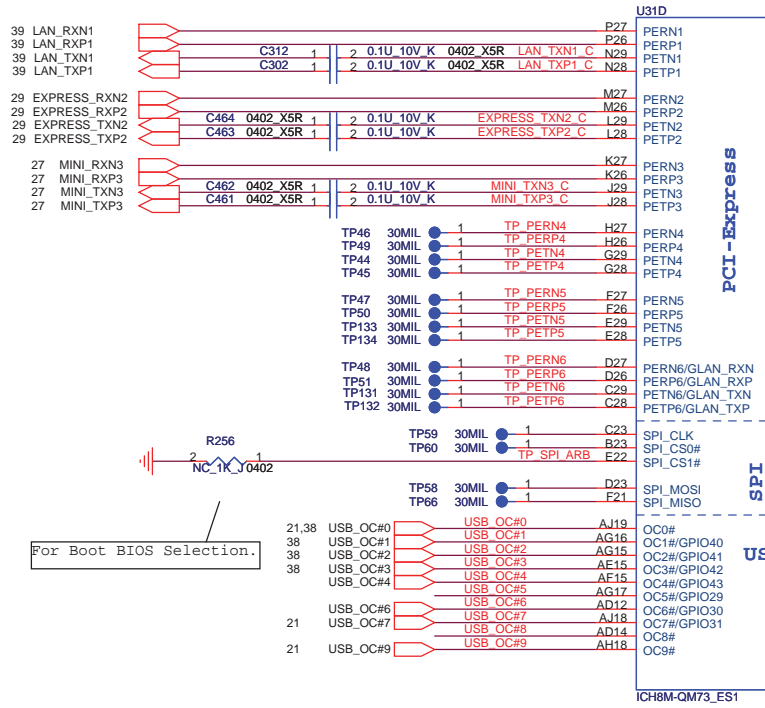
PCI Pullups



For Boot BIOS Selection.

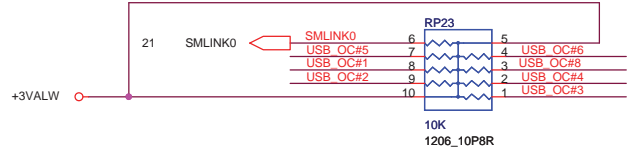
Strap for Boot-BIOS

	GNT#	SPI_CS1#
LPC(Default)	H1	H1
PCI	H1	LOW
SPI	LOW	H1

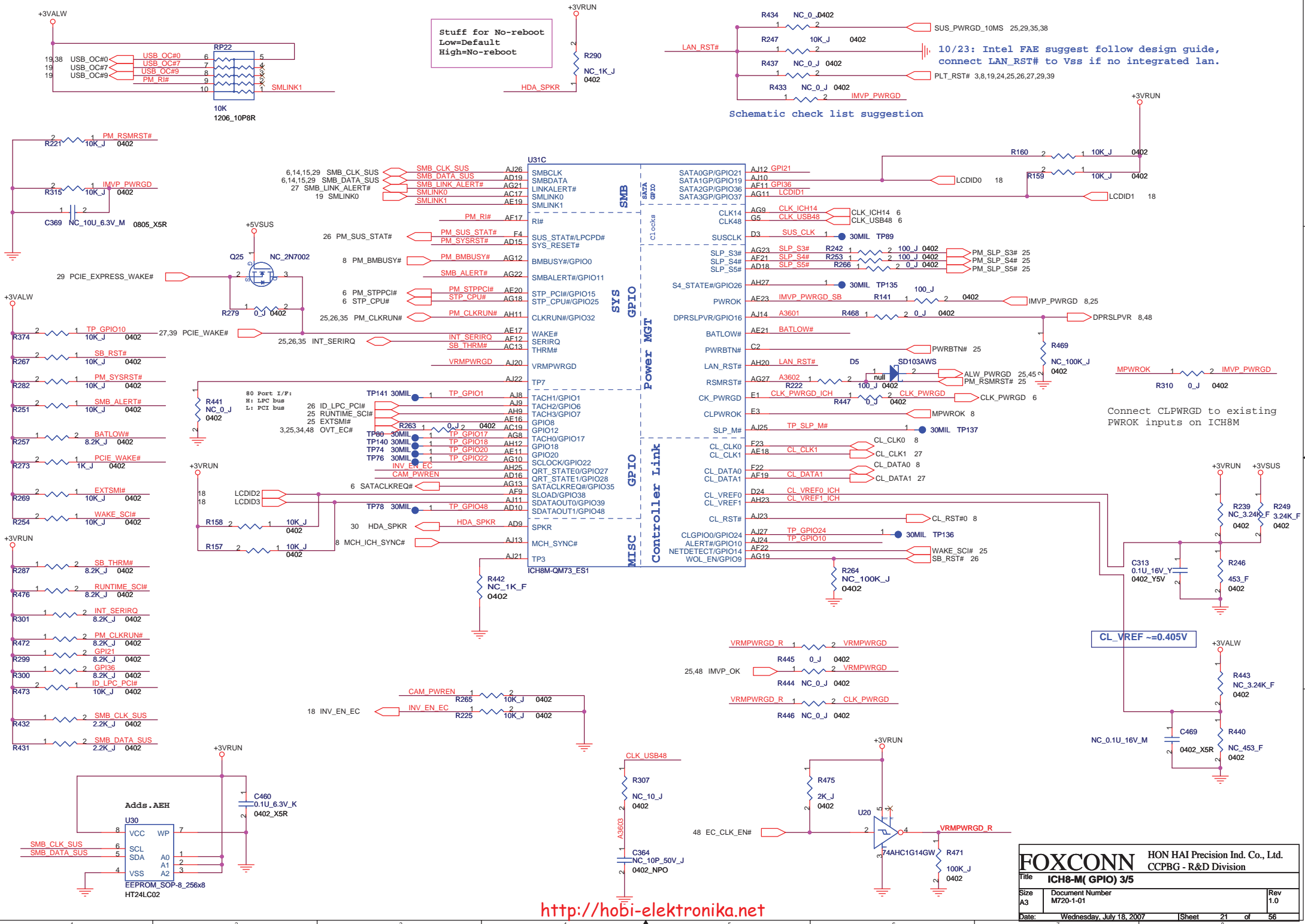


Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals







Stuff for No-reboot  
Low=Default  
High=No-reboot

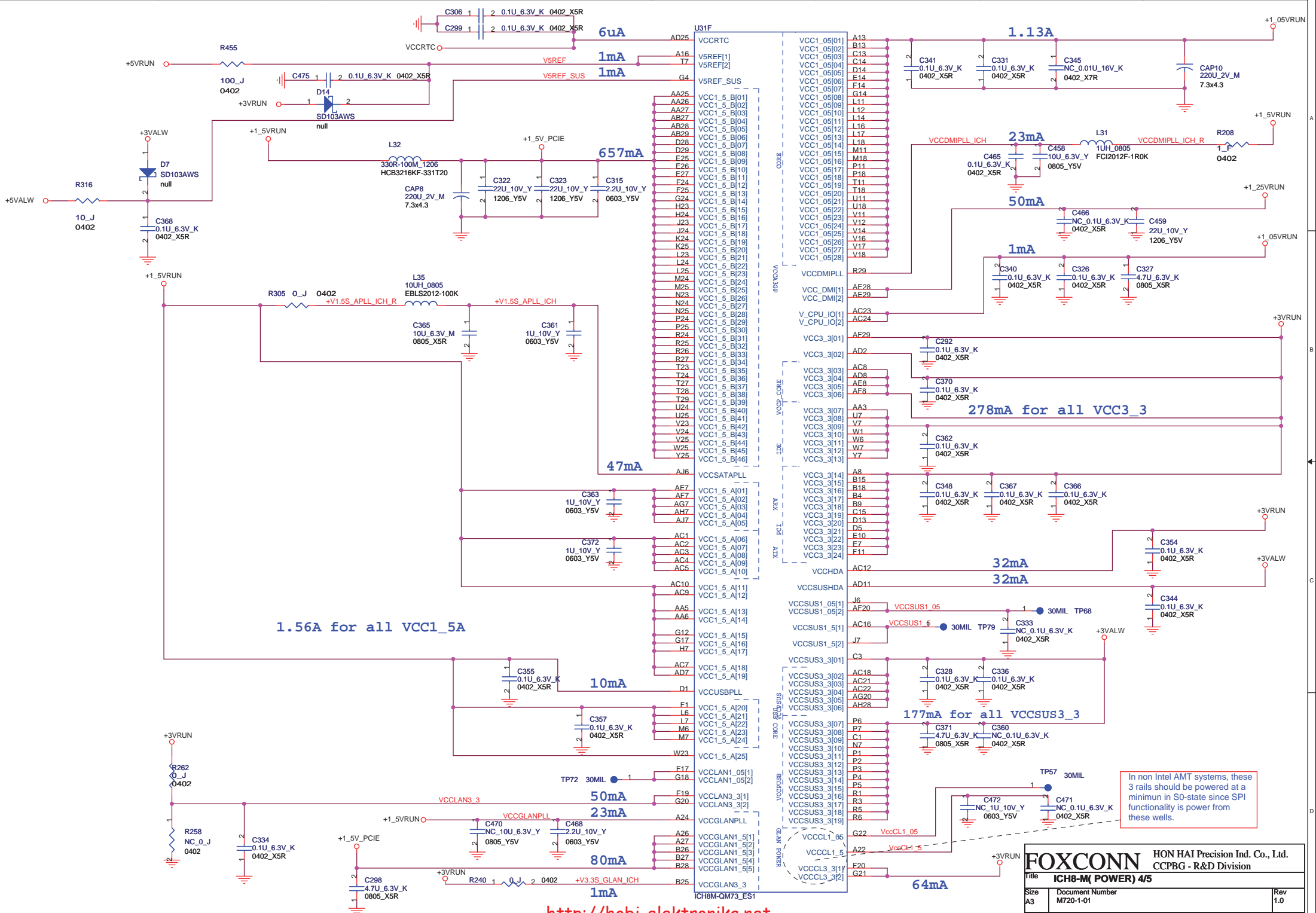
10/23: Intel FAE suggest follow design guide,  
connect LAN\_RST# to Vss if no integrated lan.

Schematic check list suggestion

Connect CLPWROK to existing  
PWROK inputs on ICH8M

CL\_VREF ~0.405V

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>ICH8-M (GPIO) 3/5</b>	
Size A3	Document Number M720-1-01
Date: Wednesday, July 18, 2007	Sheet 21 of 56



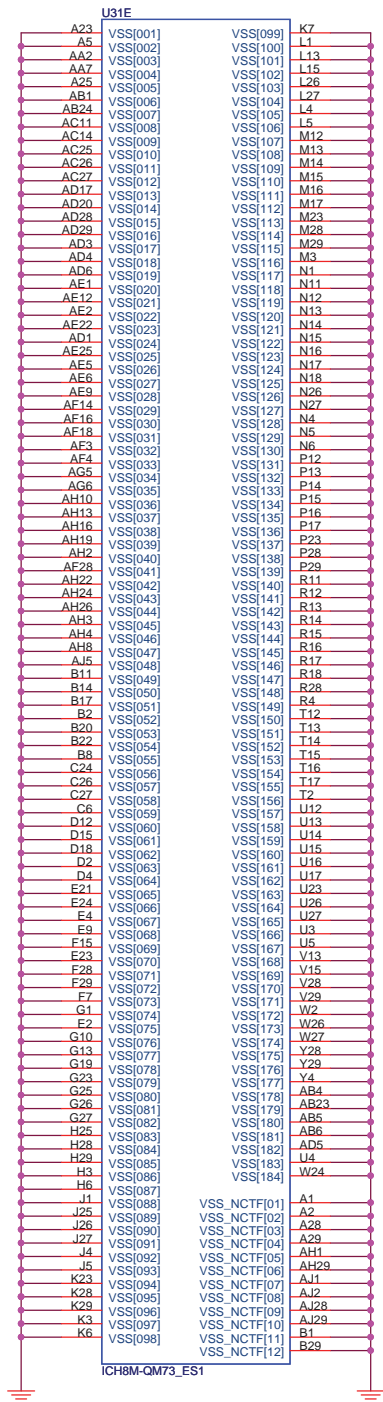
In non Intel AMT systems, these 3 rails should be powered at a minimum in S0-state since SPI functionality is power from these wells.

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **ICH8-M(POWER) 4/5**

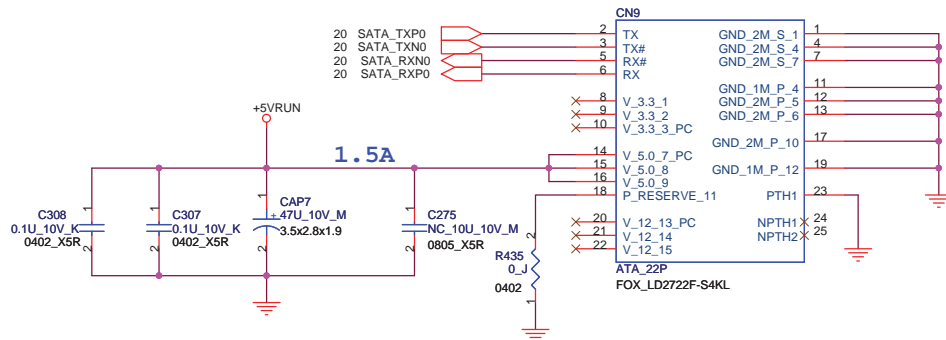
Size	Document Number	Rev
A3	M720-1-01	1.0

Date: Wednesday, July 18, 2007 Sheet 22 of 56

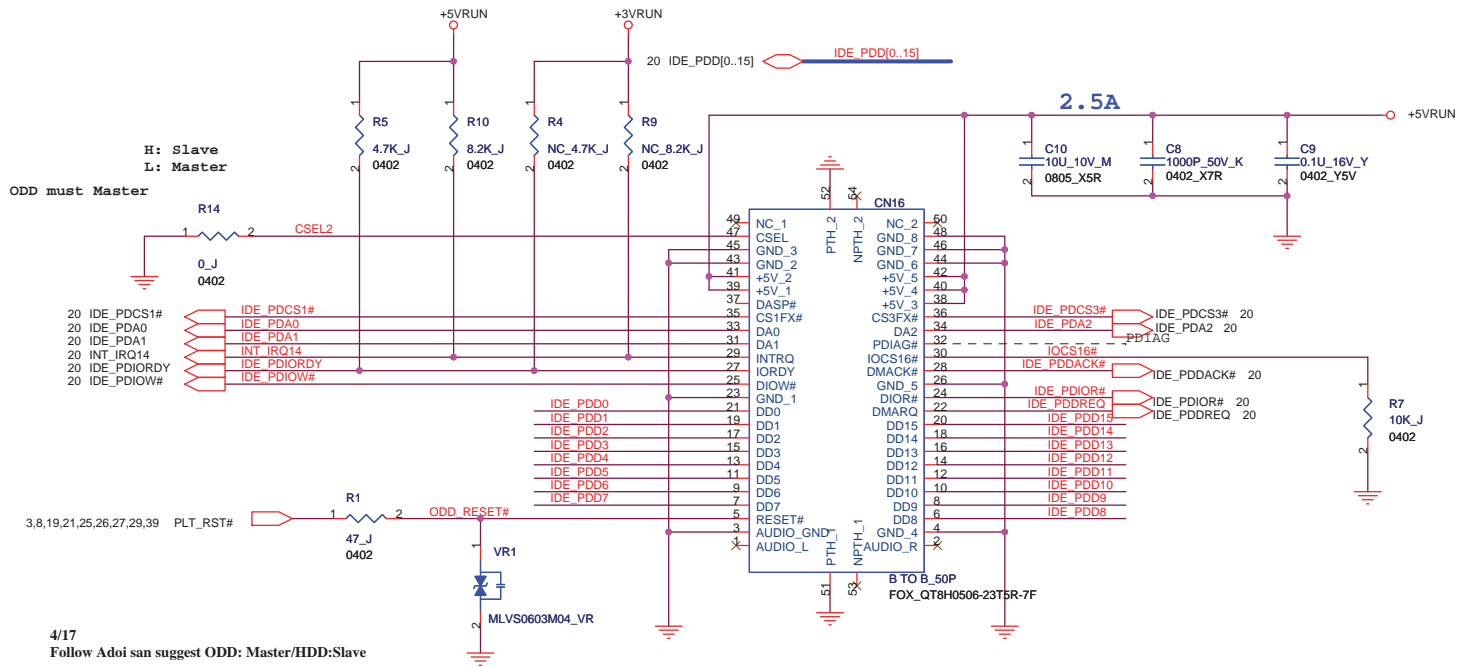


<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>ICH8-M( GND) 5/5</b>			
Size	Document Number	Rev	
A3	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	23 of 56



### SATA HDD CONN

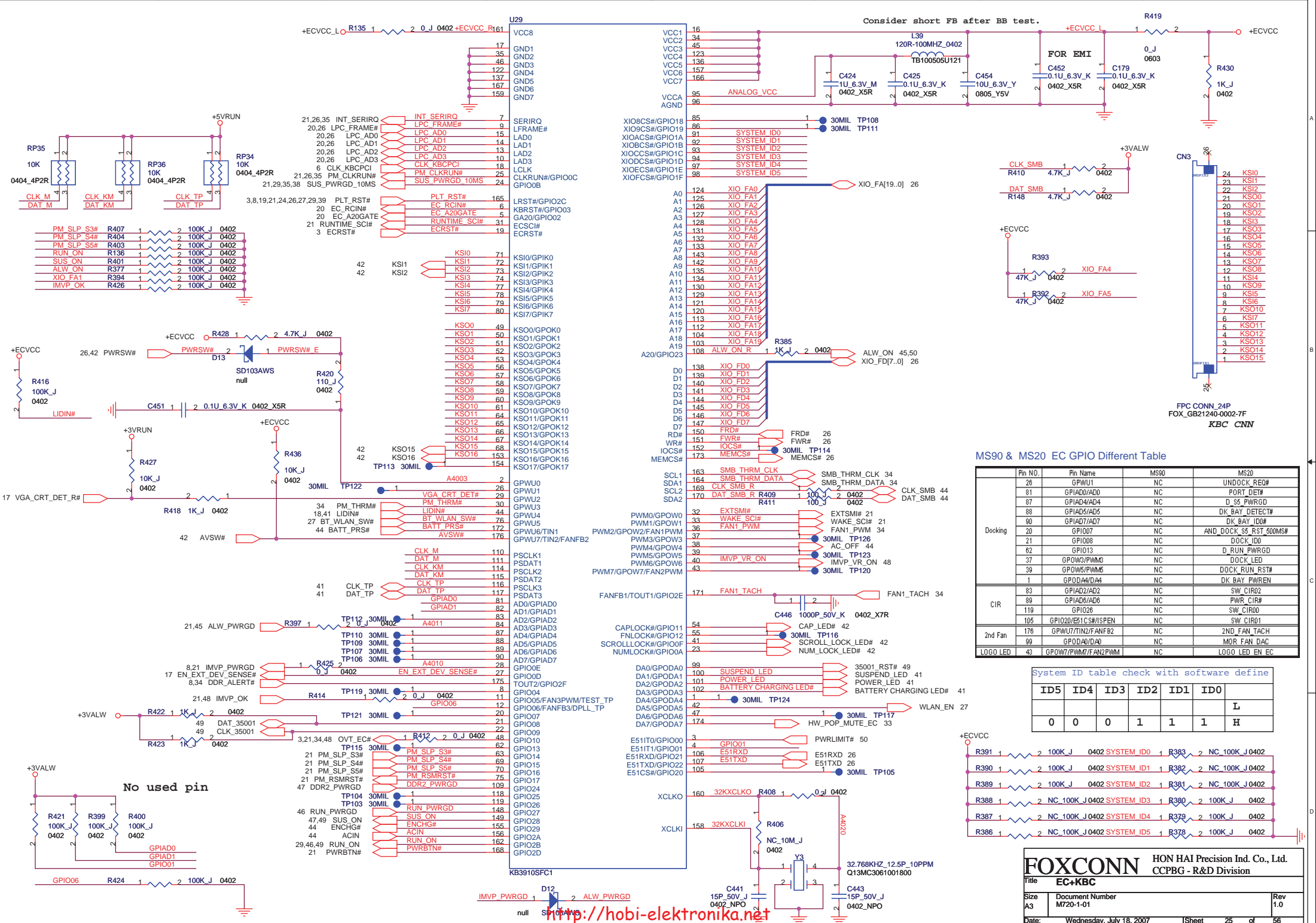


### CD-ROM CONN

<http://hobi-elektronika.net>

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>SATA HDD/CD-ROM</b>		
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 24	of 56





- 21,26,35 INT\_SERIRQ INT\_SERIRQ 7  
 20,26 LPC\_FRAME# LPC\_FRAME# 8  
 20,26 LPC\_AD0 LPC\_AD0 14  
 20,26 LPC\_AD1 LPC\_AD1 15  
 20,26 LPC\_AD2 LPC\_AD2 13  
 20,26 LPC\_AD3 LPC\_AD3 10  
 6 CLK\_KBCPC1 CLK\_KBCPC1 25  
 21,26,35 PM\_CLKRUN# PM\_CLKRUN# 25  
 21,29,35,38 SUS\_PWRGD\_10MS SUS\_PWRGD\_10MS 24
- 3,8,19,21,24,26,27,29,39 PLT\_RST# 165  
 20 EC\_RCIN# 6  
 20 EC\_A20GATE EC\_A20GATE 5  
 21 RUNTIME\_SCI# RUNTIME\_SCI# 19  
 3 ECRST# ECRST# 31

- KS10 71  
 KS11 72  
 KS12 73  
 KS13 74  
 KS14 77  
 KS15 78  
 KS16 79  
 KS17 80
- KS00 49  
 KS01 50  
 KS02 51  
 KS03 52  
 KS04 53  
 KS05 56  
 KS06 57  
 KS07 58  
 KS08 59  
 KS09 60  
 KS10 61  
 KS11 64  
 KS12 65  
 KS13 66  
 KS14 68  
 KS15 68  
 KS16 153  
 KS17 154

- KS00/GPOK0  
 KS01/GPOK1  
 KS02/GPOK2  
 KS03/GPOK3  
 KS04/GPOK4  
 KS05/GPOK5  
 KS06/GPOK6  
 KS07/GPOK7  
 KS08/GPOK8  
 KS09/GPOK9  
 KS10/GPOK10  
 KS11/GPOK11  
 KS12/GPOK12  
 KS13/GPOK13  
 KS14/GPOK14  
 KS15/GPOK15  
 KS16/GPOK16  
 KS17/GPOK17

- VGA\_CRT\_DET# 26  
 PM\_THRM# 34  
 BT\_WLAN\_SW# 18,41  
 BATT\_PRS# 27  
 AVSW# 44
- CLK\_M 110  
 DAT\_M 111  
 CLK\_KM 114  
 DAT\_KM 115  
 CLK\_TP 116  
 DAT\_TP 117

- AD0/GPIAD0  
 AD1/GPIAD1  
 AD2/GPIAD2  
 AD3/GPIAD3  
 AD4/GPIAD4  
 AD5/GPIAD5  
 AD6/GPIAD6  
 AD7/GPIAD7
- GPIO0  
 GPIO1  
 GPIO2  
 GPIO3  
 GPIO4  
 GPIO5/FAN3/PWM/TEST\_TP  
 GPIO6/FANFB3/DPLL\_TP  
 GPIO7  
 GPIO8  
 GPIO9  
 GPIO10  
 GPIO13  
 GPIO14  
 GPIO15  
 GPIO16  
 GPIO17  
 GPIO18  
 GPIO19  
 GPIO20

- GPIO06  
 GPIO01  
 GPIO02  
 GPIO03  
 GPIO04  
 GPIO05  
 GPIO06  
 GPIO07  
 GPIO08  
 GPIO09  
 GPIO10  
 GPIO11  
 GPIO12  
 GPIO13  
 GPIO14  
 GPIO15  
 GPIO16  
 GPIO17  
 GPIO18  
 GPIO19  
 GPIO20

- XIO0CS#/GPIO18  
 XIO0CS#/GPIO19  
 XIO0CS#/GPIO1A  
 XIO0CS#/GPIO1B  
 XIO0CS#/GPIO1C  
 XIO0CS#/GPIO1D  
 XIO0CS#/GPIO1E  
 XIO0CS#/GPIO1F
- XIO0CS# 85  
 XIO0CS# 86  
 XIO0CS# 91  
 XIO0CS# 92  
 XIO0CS# 93  
 XIO0CS# 94  
 XIO0CS# 97  
 XIO0CS# 98

- XIO0FA0  
 XIO0FA1  
 XIO0FA2  
 XIO0FA3  
 XIO0FA4  
 XIO0FA5  
 XIO0FA6  
 XIO0FA7  
 XIO0FA8  
 XIO0FA9  
 XIO0FA10  
 XIO0FA11  
 XIO0FA12  
 XIO0FA13  
 XIO0FA14  
 XIO0FA15  
 XIO0FA16  
 XIO0FA17  
 XIO0FA18  
 XIO0FA19
- XIO0FA[19..0] 26

- XIO0FD0  
 XIO0FD1  
 XIO0FD2  
 XIO0FD3  
 XIO0FD4  
 XIO0FD5  
 XIO0FD6  
 XIO0FD7
- XIO0FD[7..0] 26

- FRD# 26  
 FWR# 26  
 IOC# 152  
 MEMCS# 173
- FRD# 26  
 FWR# 26  
 IOC# 152  
 MEMCS# 173

- SMB\_THRM\_CLK  
 SMB\_THRM\_DATA  
 CAP\_LEM#
- SMB\_THRM\_CLK 34  
 SMB\_THRM\_DATA 34  
 CAP\_LEM# 42

- DA0/GPODA0  
 DA1/GPODA1  
 DA2/GPODA2  
 DA3/GPODA3  
 DA4/GPODA4  
 DA5/GPODA5  
 DA6/GPODA6  
 DA7/GPODA7
- DA0/GPODA0 99  
 DA1/GPODA1 100  
 DA2/GPODA2 101  
 DA3/GPODA3 102  
 DA4/GPODA4 101  
 DA5/GPODA5 102  
 DA6/GPODA6 101  
 DA7/GPODA7 102

- E511T0/GPIO00  
 E511T1/GPIO01  
 E51RXD/GPIO21  
 E51TXD/GPIO22  
 E51CS#/GPIO20
- E511T0/GPIO00 3  
 E511T1/GPIO01 4  
 E51RXD/GPIO21 106  
 E51TXD/GPIO22 107  
 E51CS#/GPIO20 105

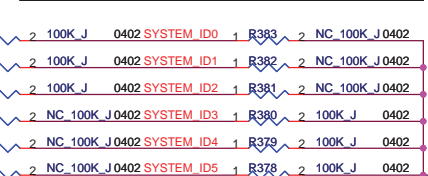
- XCLKO  
 XCLKI
- XCLKO 160  
 XCLKI 158

MS90 & MS20 EC GPIO Different Table

	Pin NO.	Pin Name	MS90	MS20
Docking	26	GPWU1	NC	UNDOCK_REQ#
	81	GPIAD0/AD0	NC	PORT_DET#
	87	GPIAD4/AD4	NC	D_35_PWRGD
	88	GPIAD5/AD5	NC	DK_BAY_DETECT#
	90	GPIAD7/AD7	NC	DK_BAY_ID#
	20	GPI007	NC	AND_DOCK_S5_RST_600MS#
	21	GPI008	NC	DOCK_ID0
	62	GPI013	NC	D_RUN_PWRGD
	37	GPDW3/PWM3	NC	DOCK_LED
	39	GPDW5/PWM5	NC	DOCK_LED
CIR	1	GPOD4/AD4	NC	DK_BAY_PWREN
	83	GPIAD2/AD2	NC	SW_CIR02
	89	GPIAD6/AD6	NC	PWR_CIR#
	119	GPI026	NC	SW_CIR00
2nd Fan	105	GPI020/ES1CS#/ISPEN	NC	SW_CIR01
	43	GPOW7/IPW7/FAN2/PWM	NC	LOGO_LED EN EC

System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0	
0	0	0	1	1	1	L
0	0	0	1	1	1	H



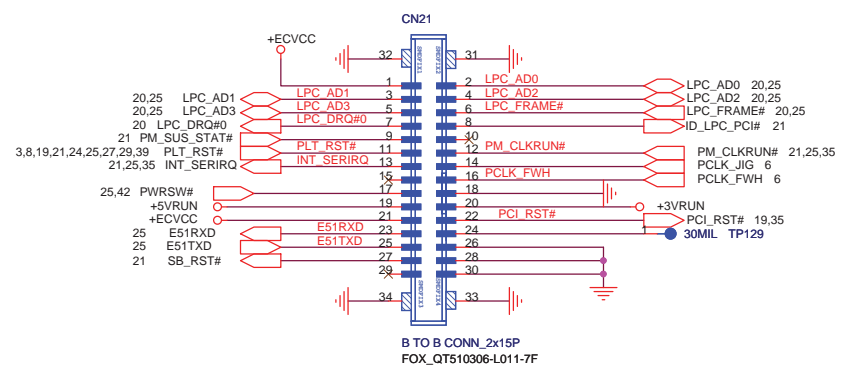
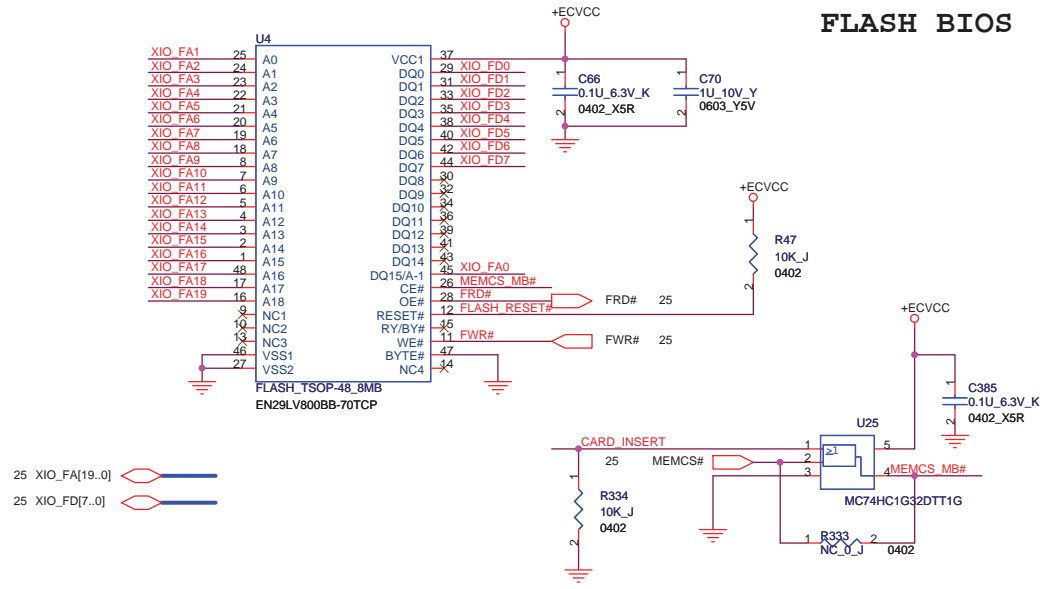
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **EC+KBC**

Size: A3  
 Document Number: M720-1-01  
 Date: Wednesday, July 18, 2007

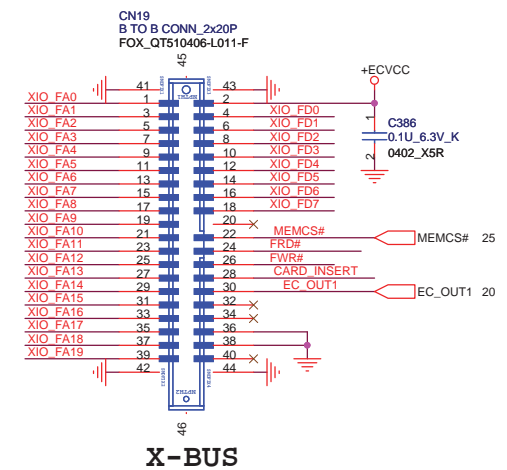
Rev: 1.0  
 Sheet: 25 of 56

# FLASH BIOS



## JIG-120

Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.

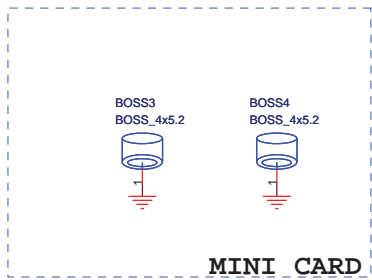


## X-BUS

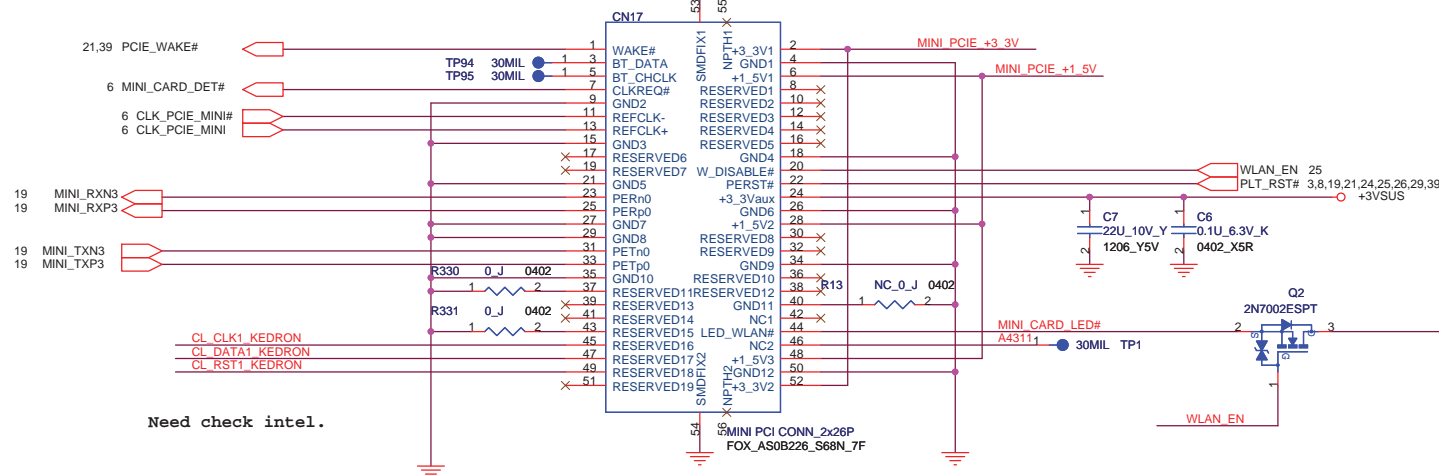
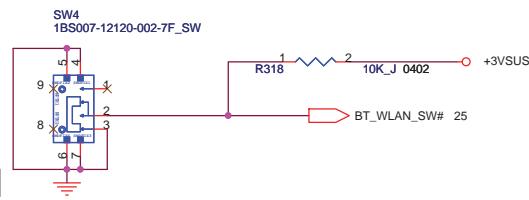
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title **Flash ROM/X-BUS CONN**

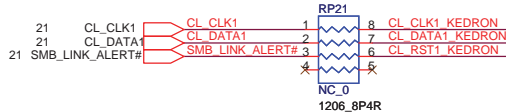
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 26	of 56



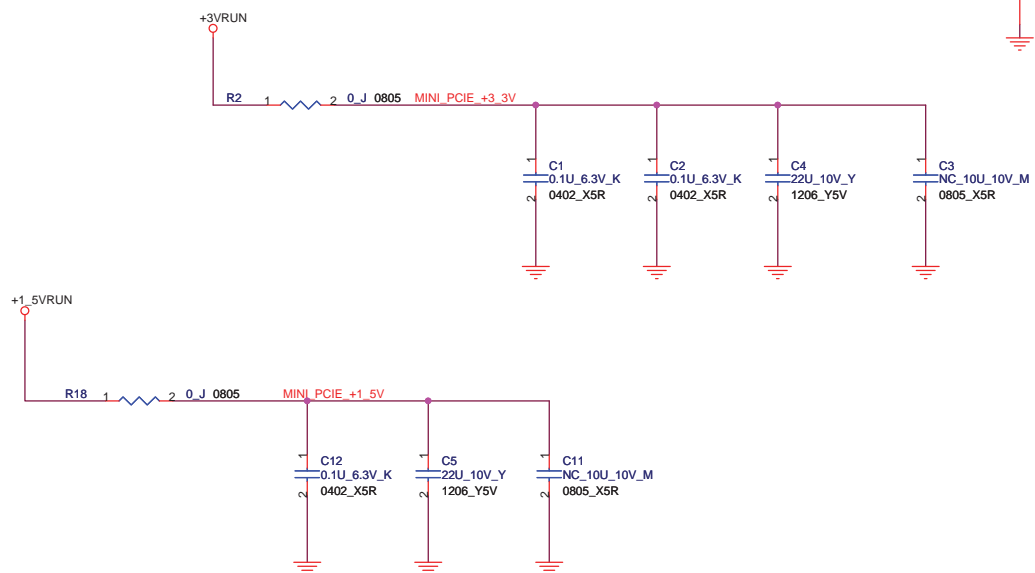
SW2 PIN8,9 : NPTH



**Mini Card.  
WLAN**



+1\_5V=>0.5A  
+3\_3VAux=>0.33A  
+3\_3V=>1A

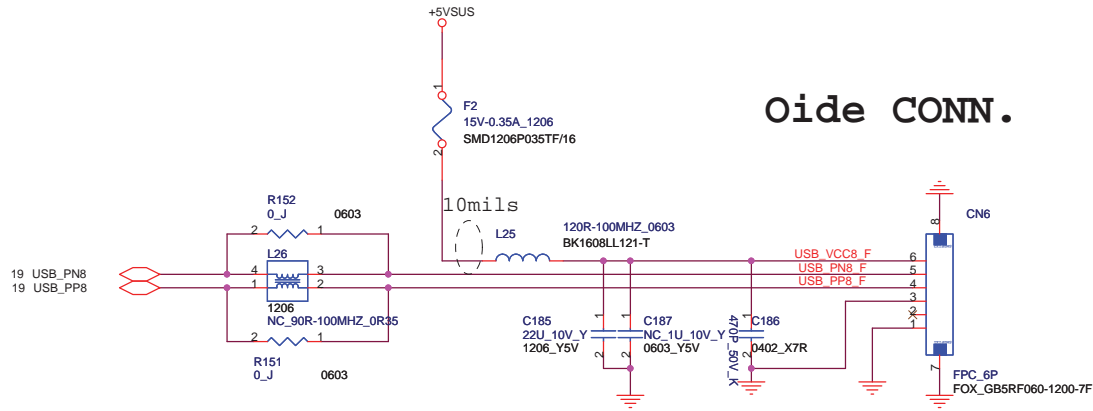


LED IF SPEC:  
20mA (TYP) , 30mA (MAX)

Green

**WLAN LED.**

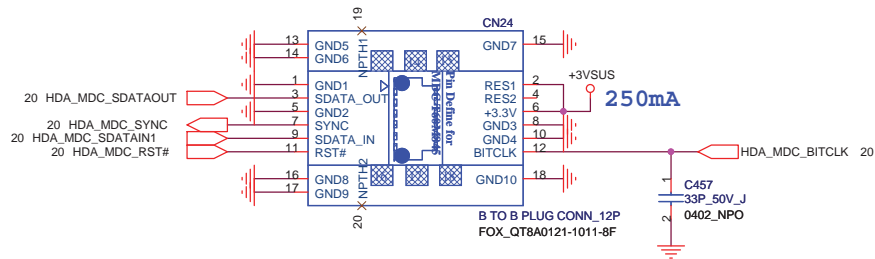
# Oide CONN.

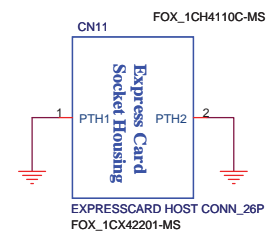
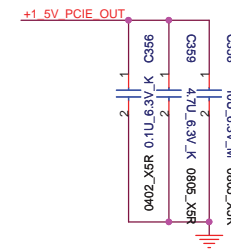
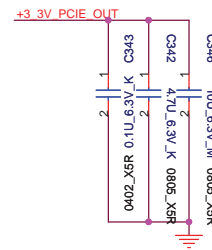
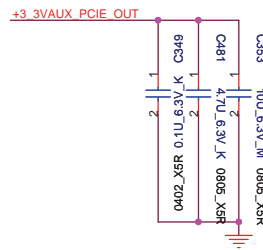
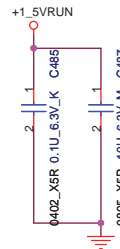
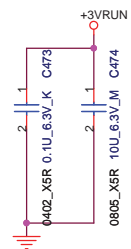
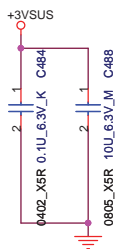
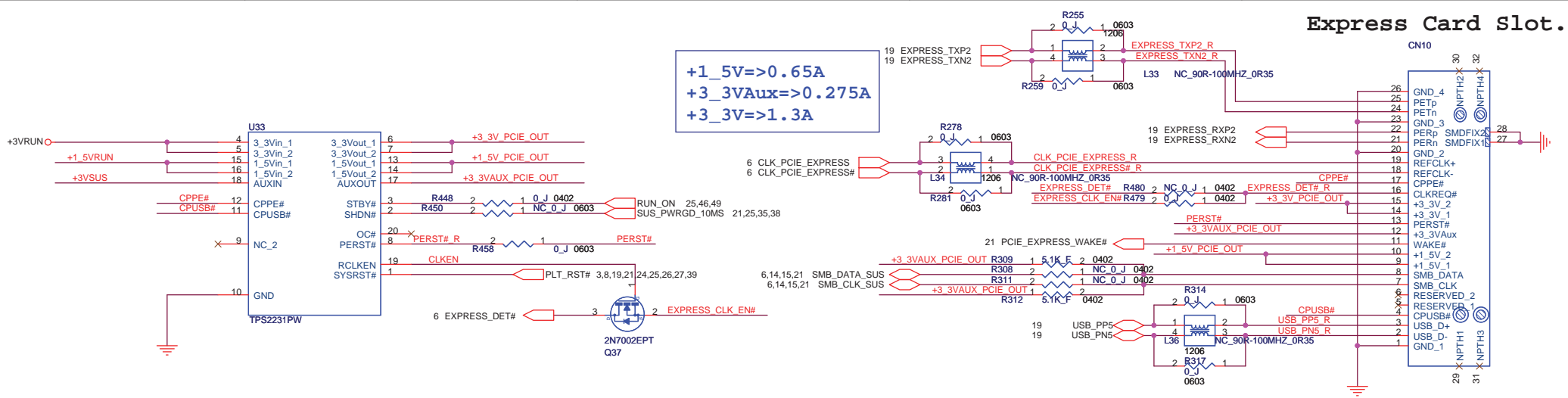


BOM Notice: OIDE\_

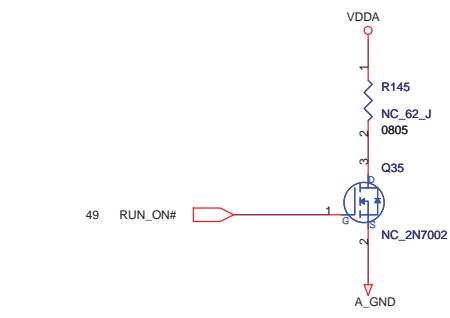
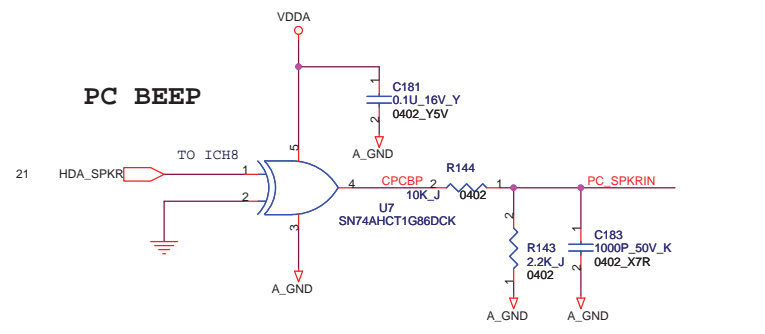
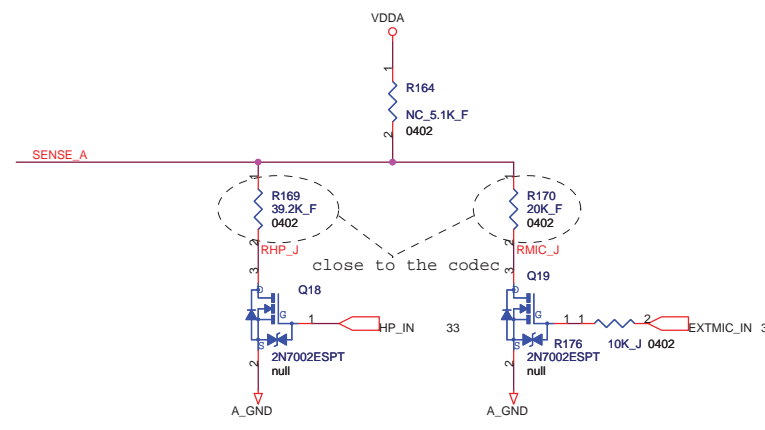
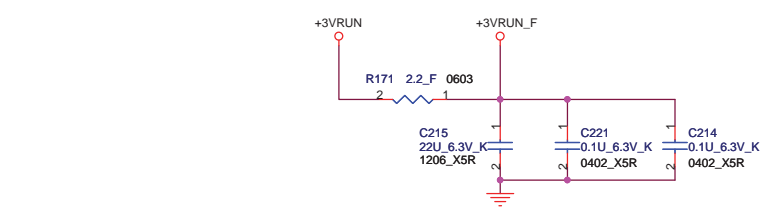
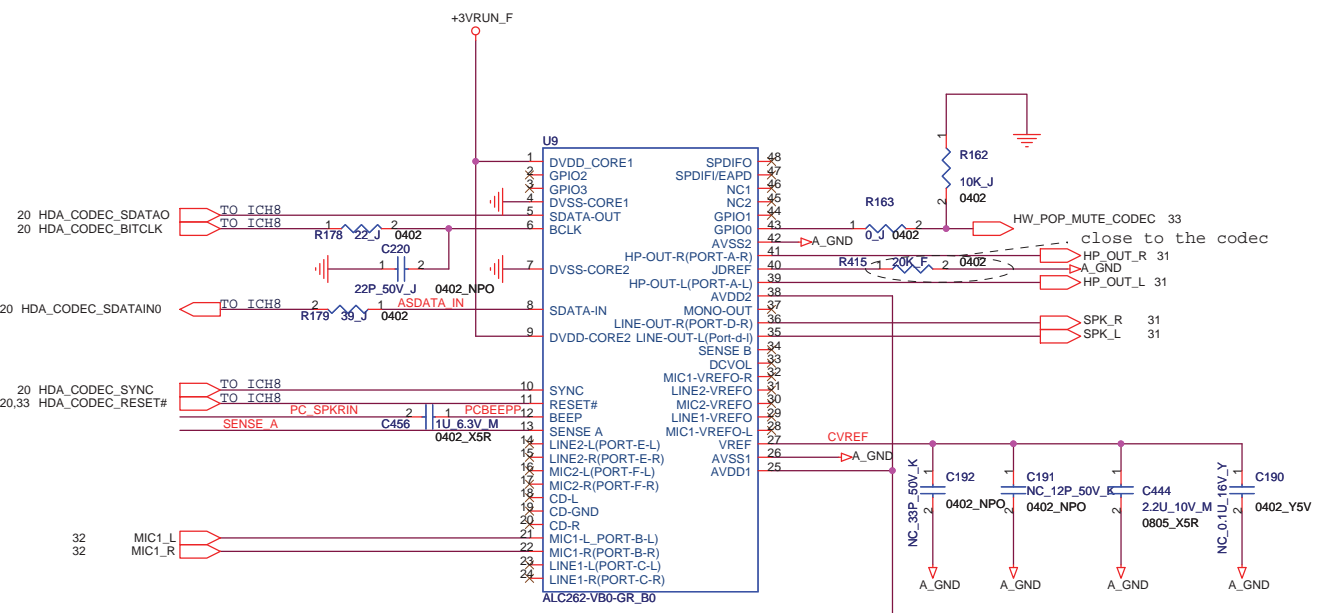
W/ Oide SKU	R151,R152,L25,C185,C186,F2,CN6	stuff
W/O Oide SKU	R151,R152,L25,C185,C186,F2,CN6	no stuff

# MDC CONN.





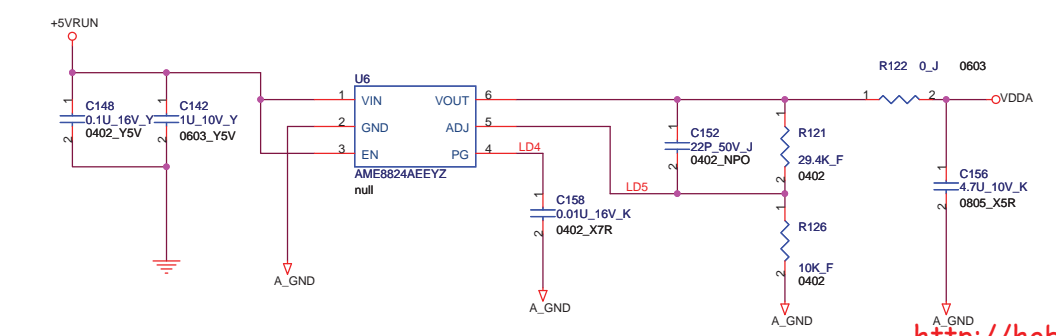
**Express Card Housing.**



Place these two capacitor together.

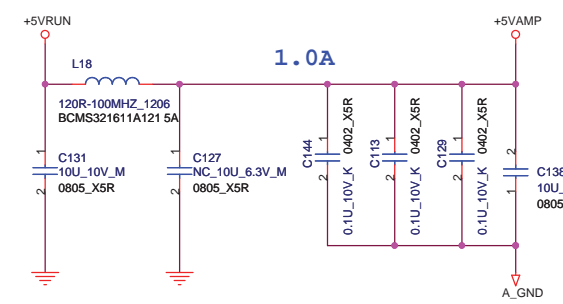
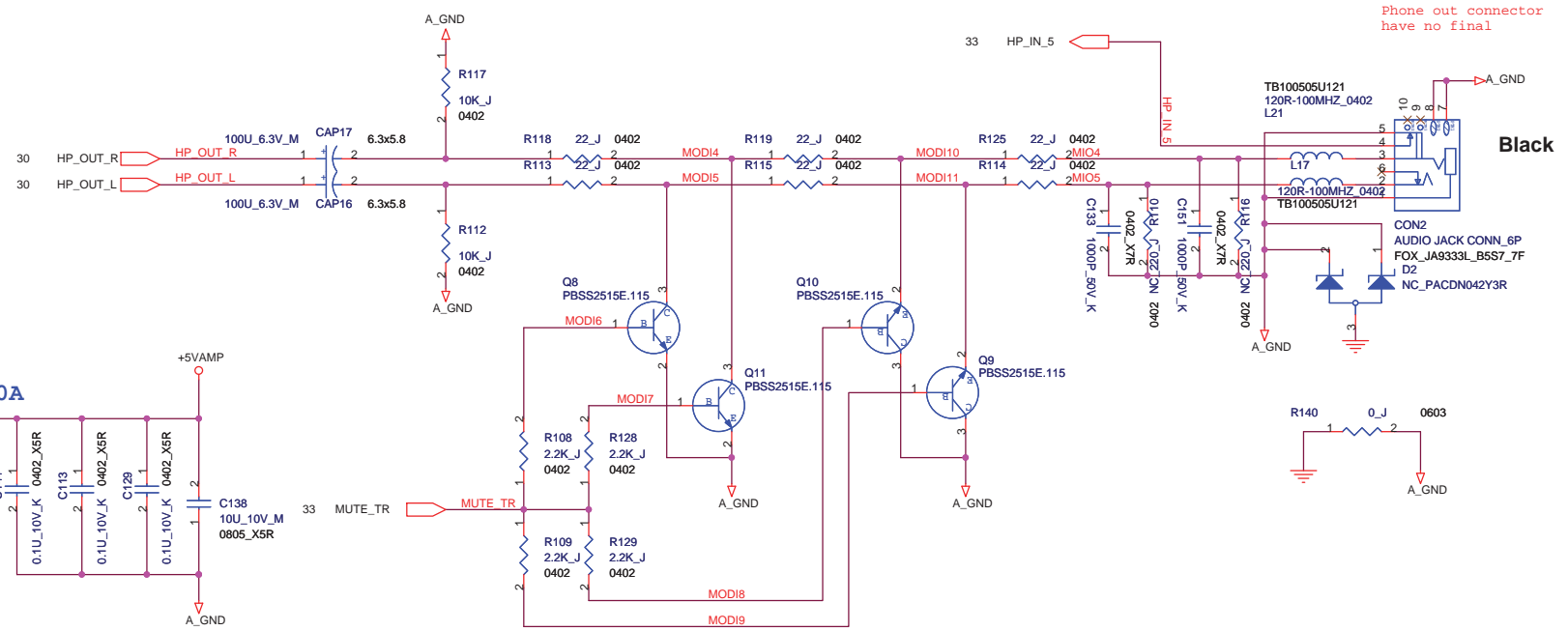
Place these two capacitor together.

AUDIO POWER(Change to 4.75V/200mA)

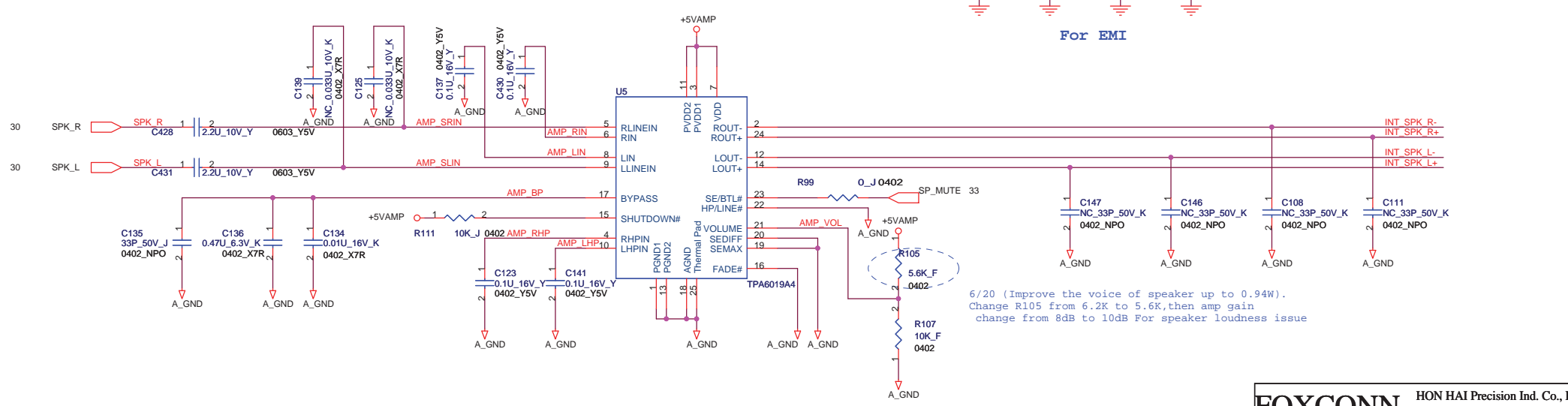
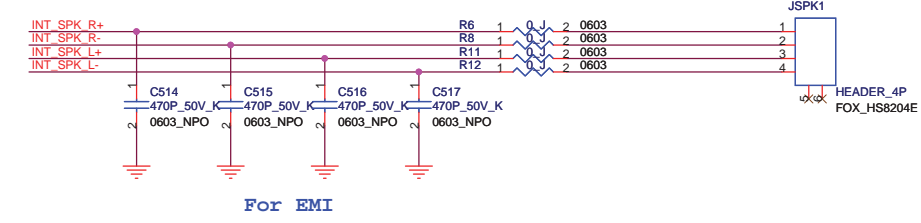


<http://hobi-elektronika.net>

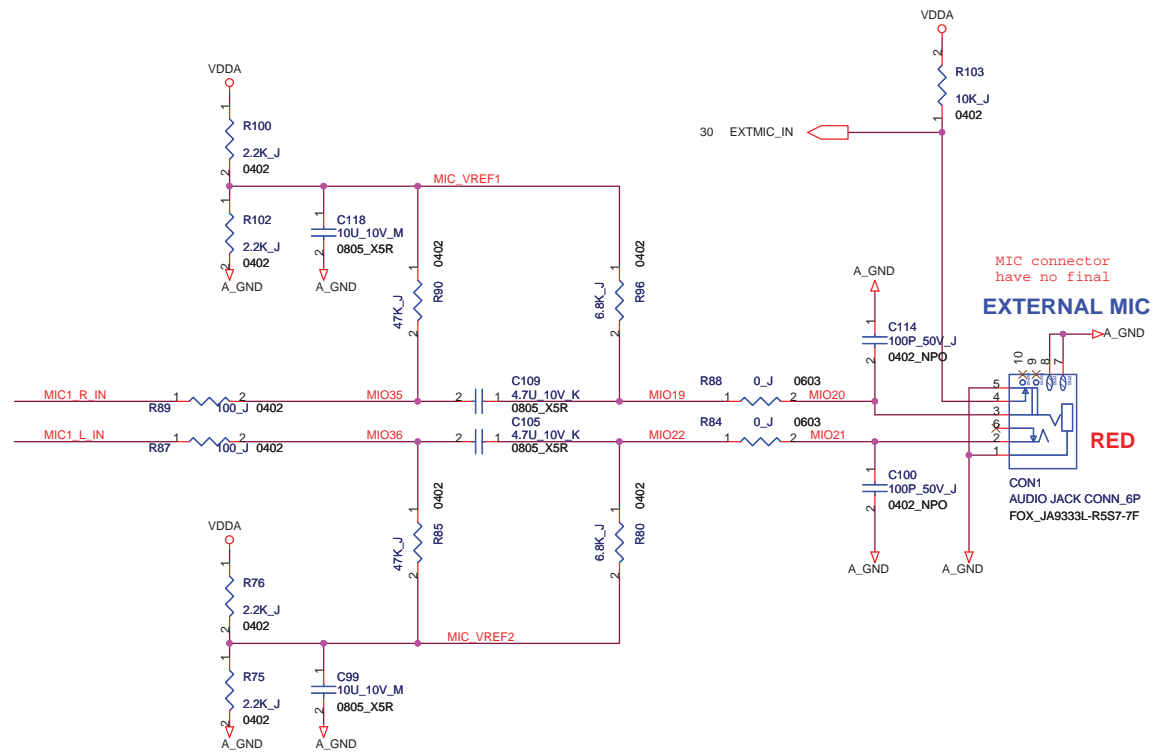
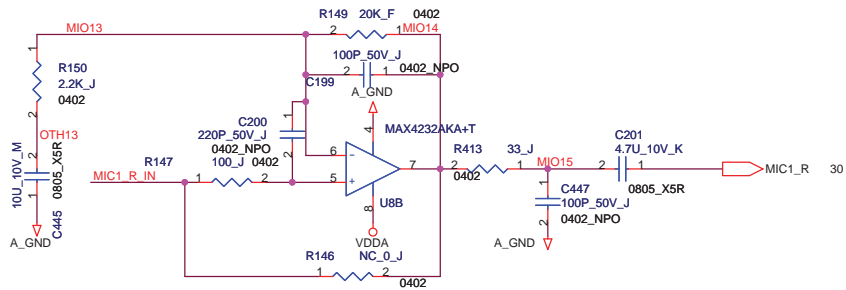
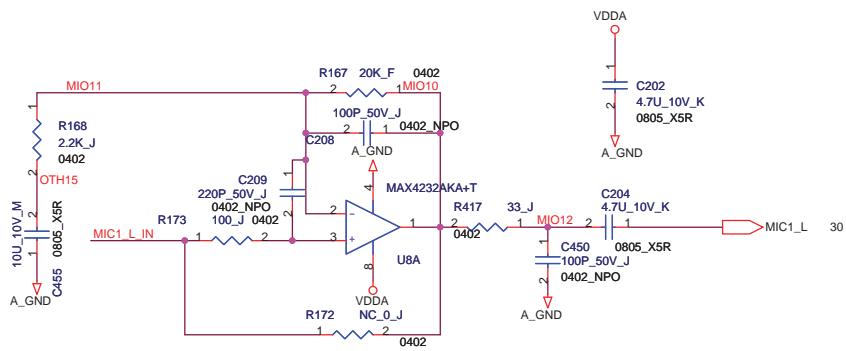
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>AUDIO(CODEC/POWER) 1/4</b>		
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 30	of 56



**INTERNAL SPEAKER**



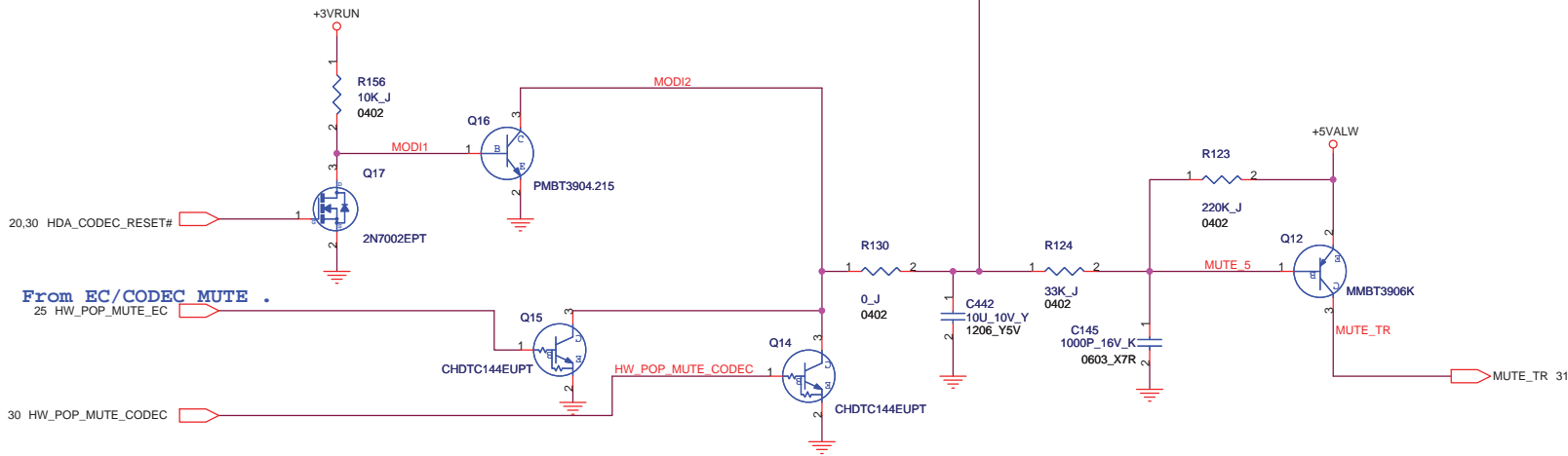
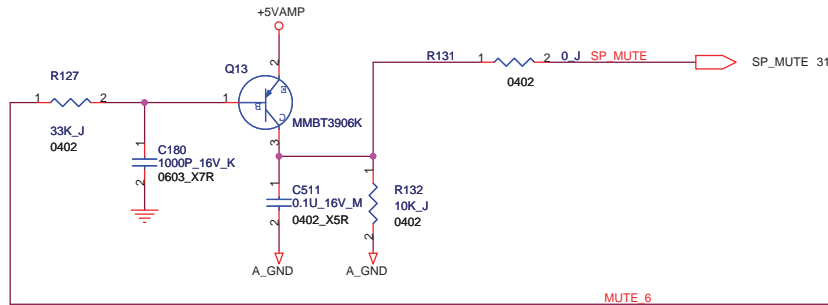
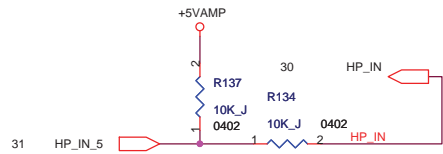
6/20 (Improve the voice of speaker up to 0.94W).  
 Change R105 from 6.2K to 5.6K, then amp gain  
 change from 8dB to 10dB For speaker loudness issue

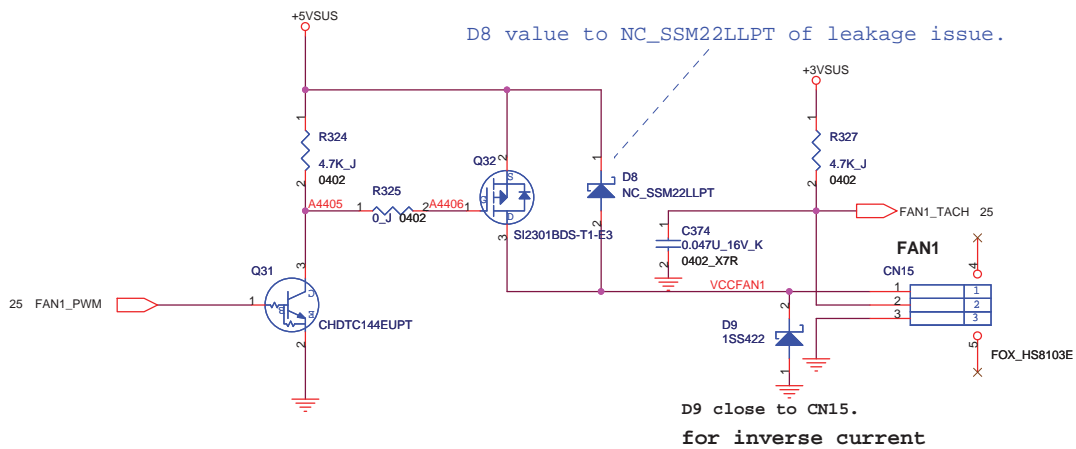


<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>AUDIO( EXT MIC &amp; PHONE OUT)</b>			
Size	Document Number	Rev	
A3	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	32 of 56

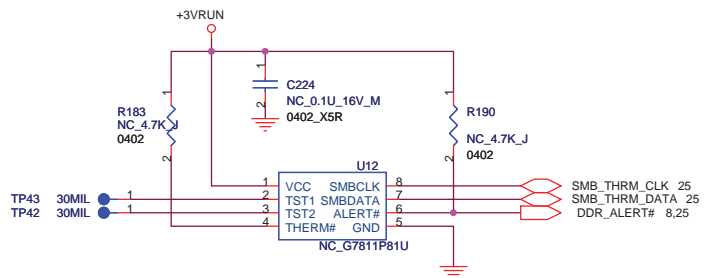




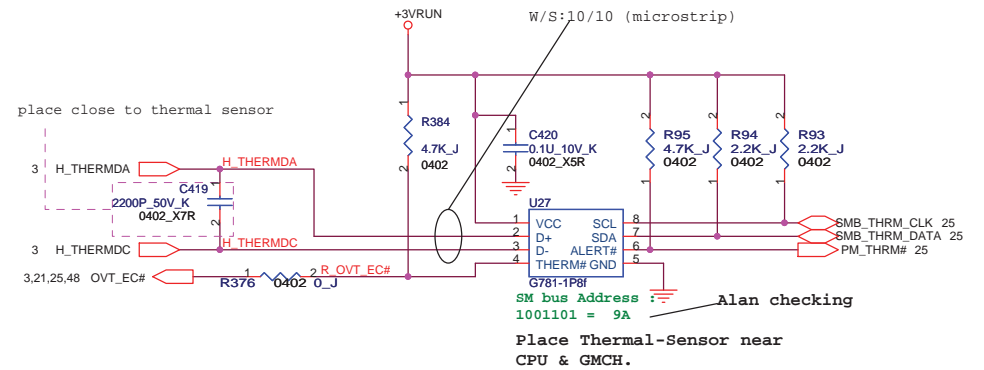


## FAN

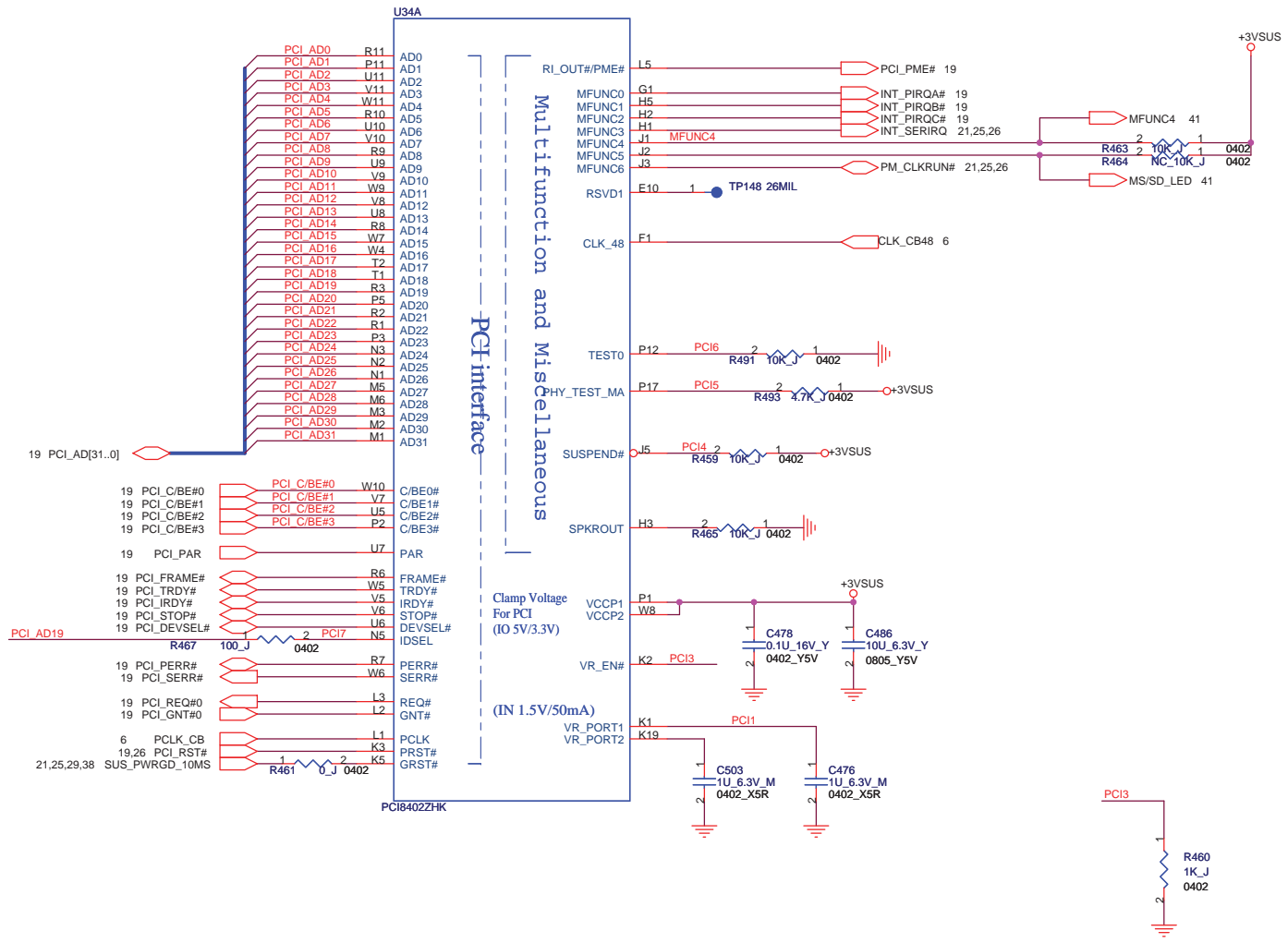
## Memory Thermal-Sensor

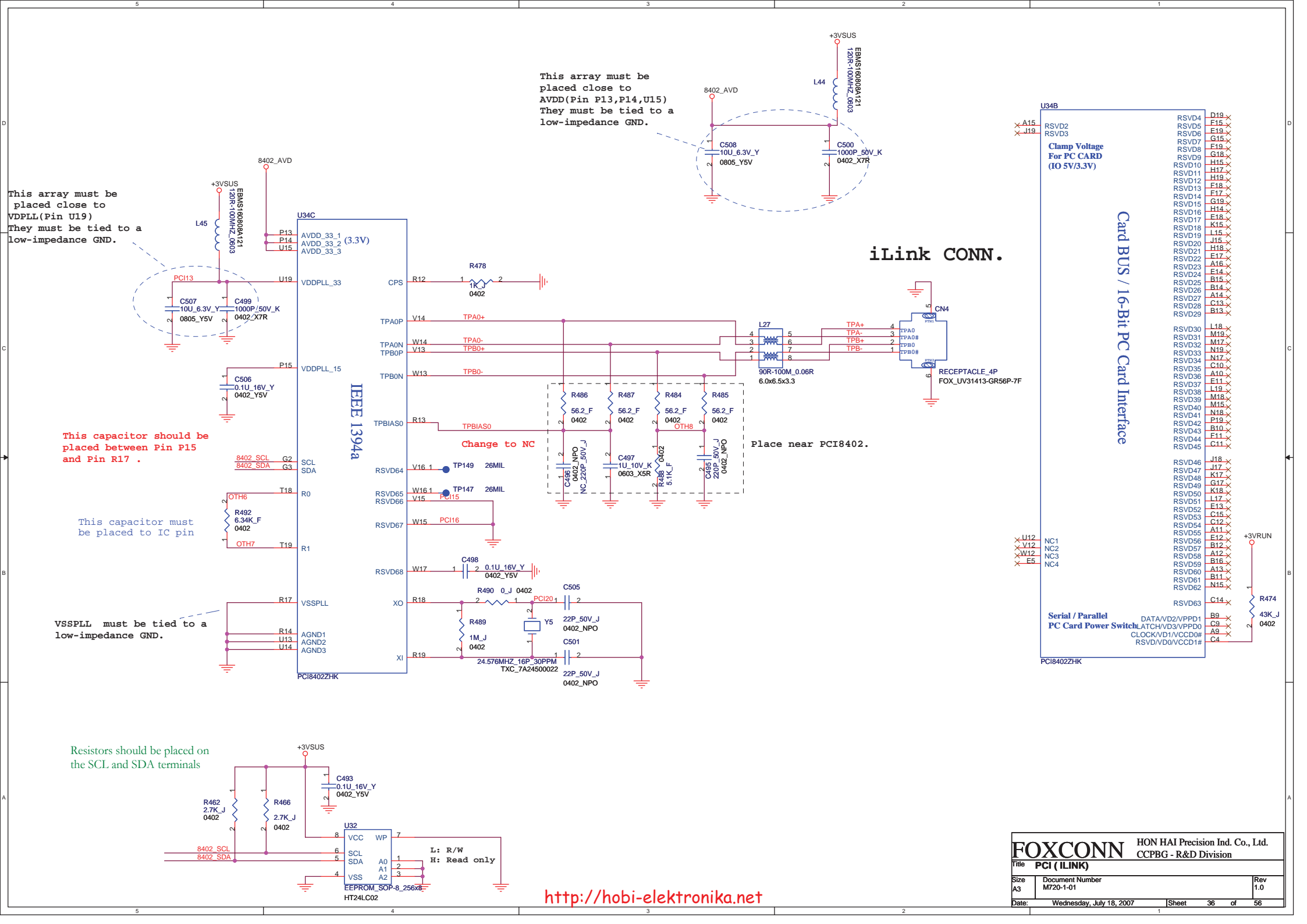


## CPU Thermal-Sensor

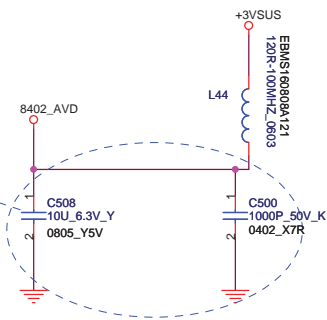


## Close to U24

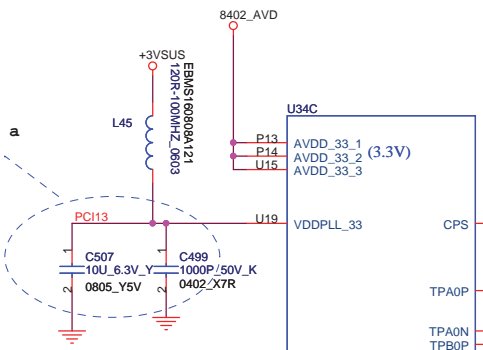




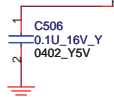
This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.



This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.

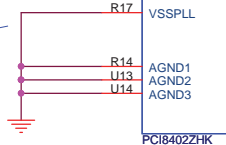


This capacitor should be placed between Pin P15 and Pin R17 .

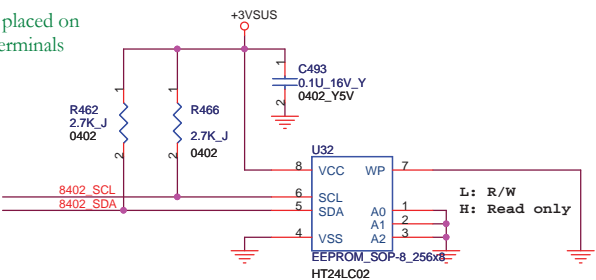


This capacitor must be placed to IC pin

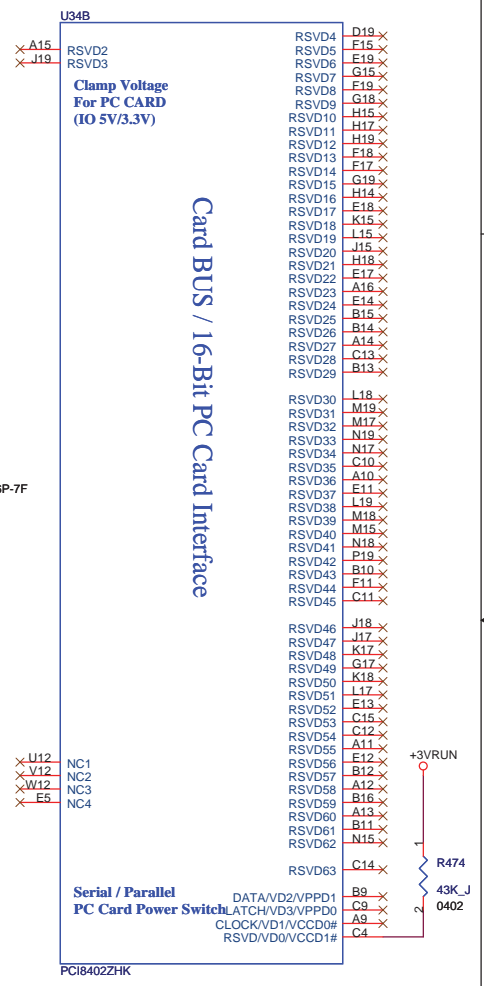
VSSPLL must be tied to a low-impedance GND.



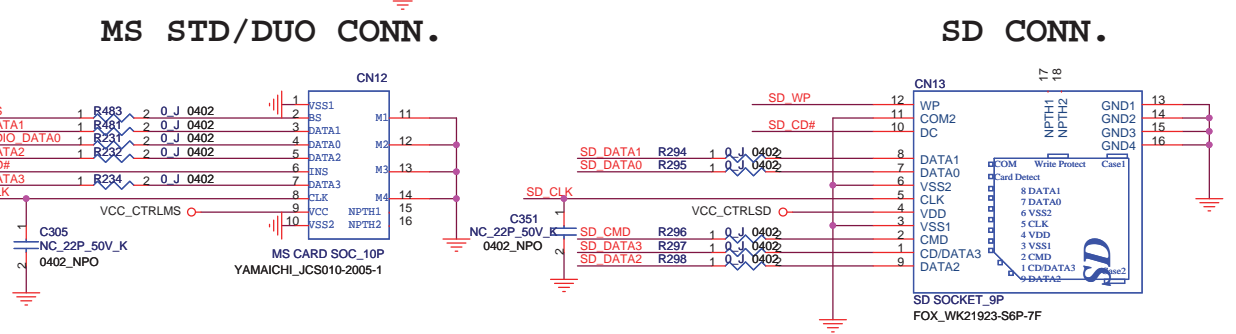
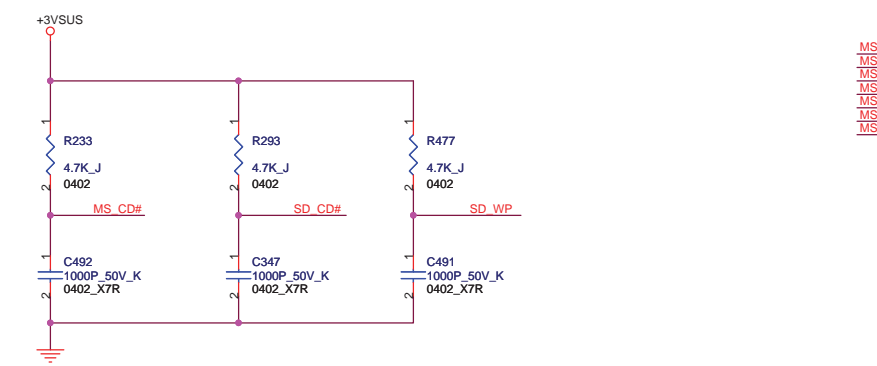
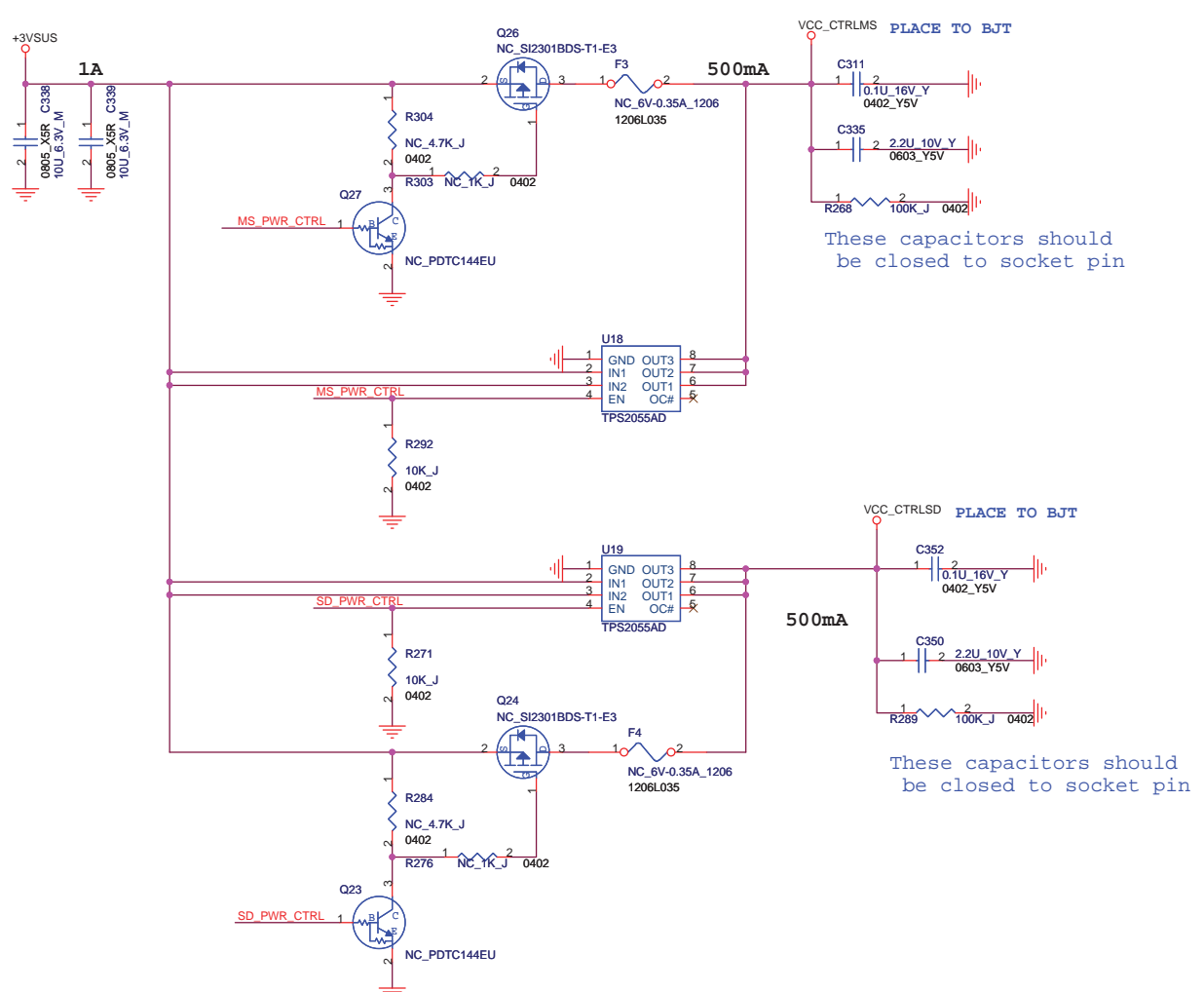
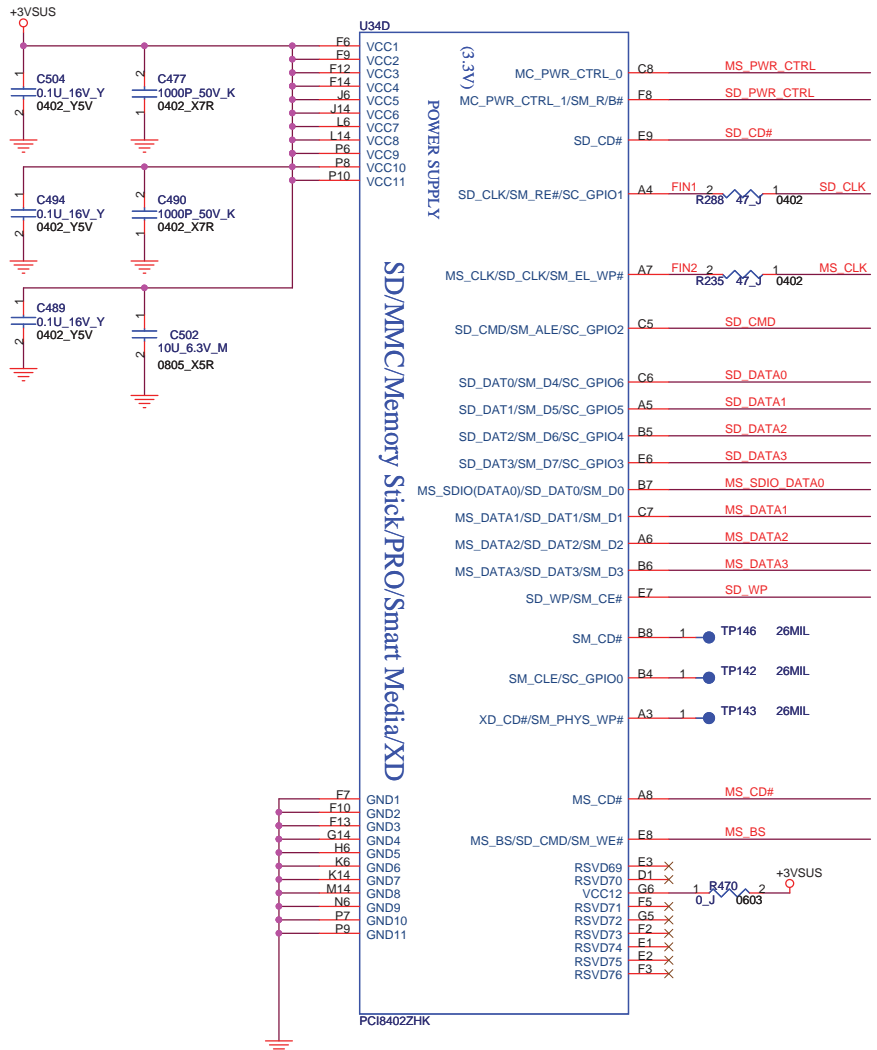
Resistors should be placed on the SCL and SDA terminals

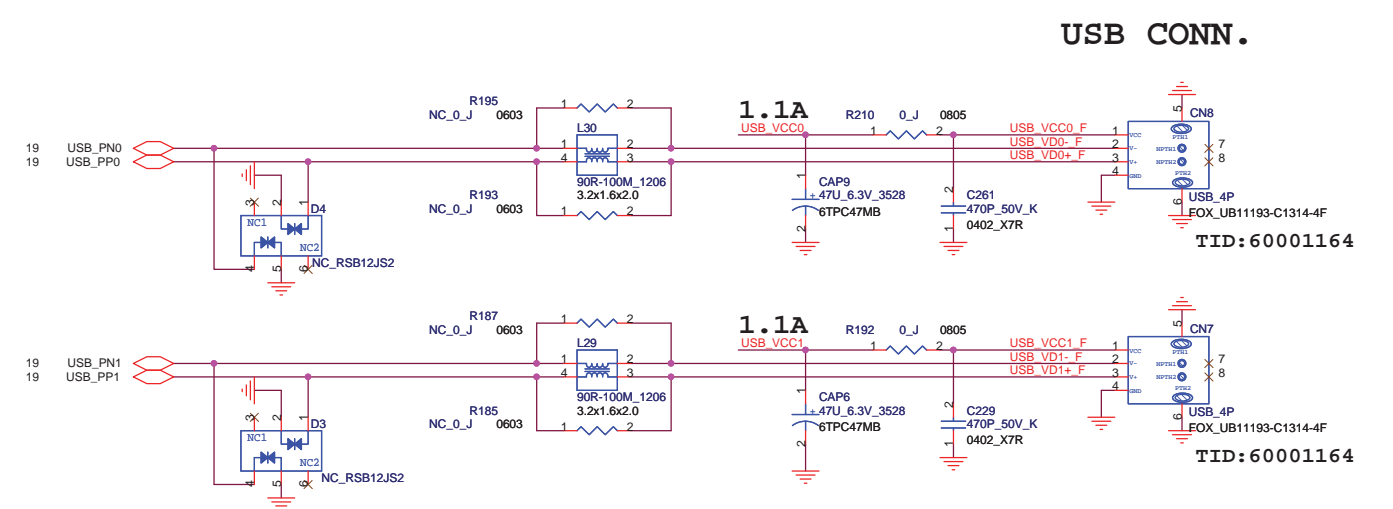
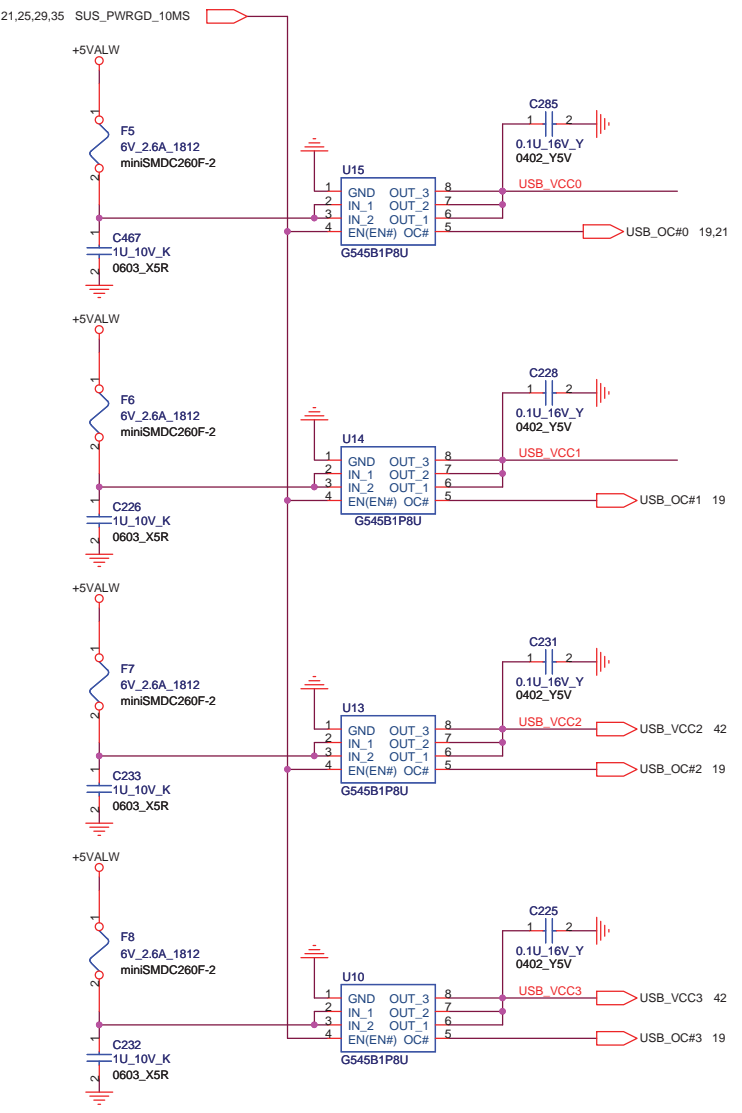


<http://hobi-elektronika.net>



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>PCI (iLINK)</b>		CCPBG - R&D Division	
Size A3	Document Number M720-1-01	Rev 1.0	
Date	Wednesday, July 18, 2007	Sheet 36	of 56

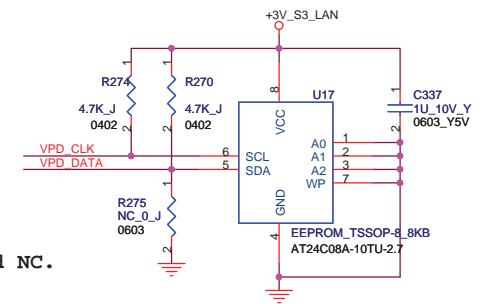
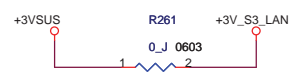
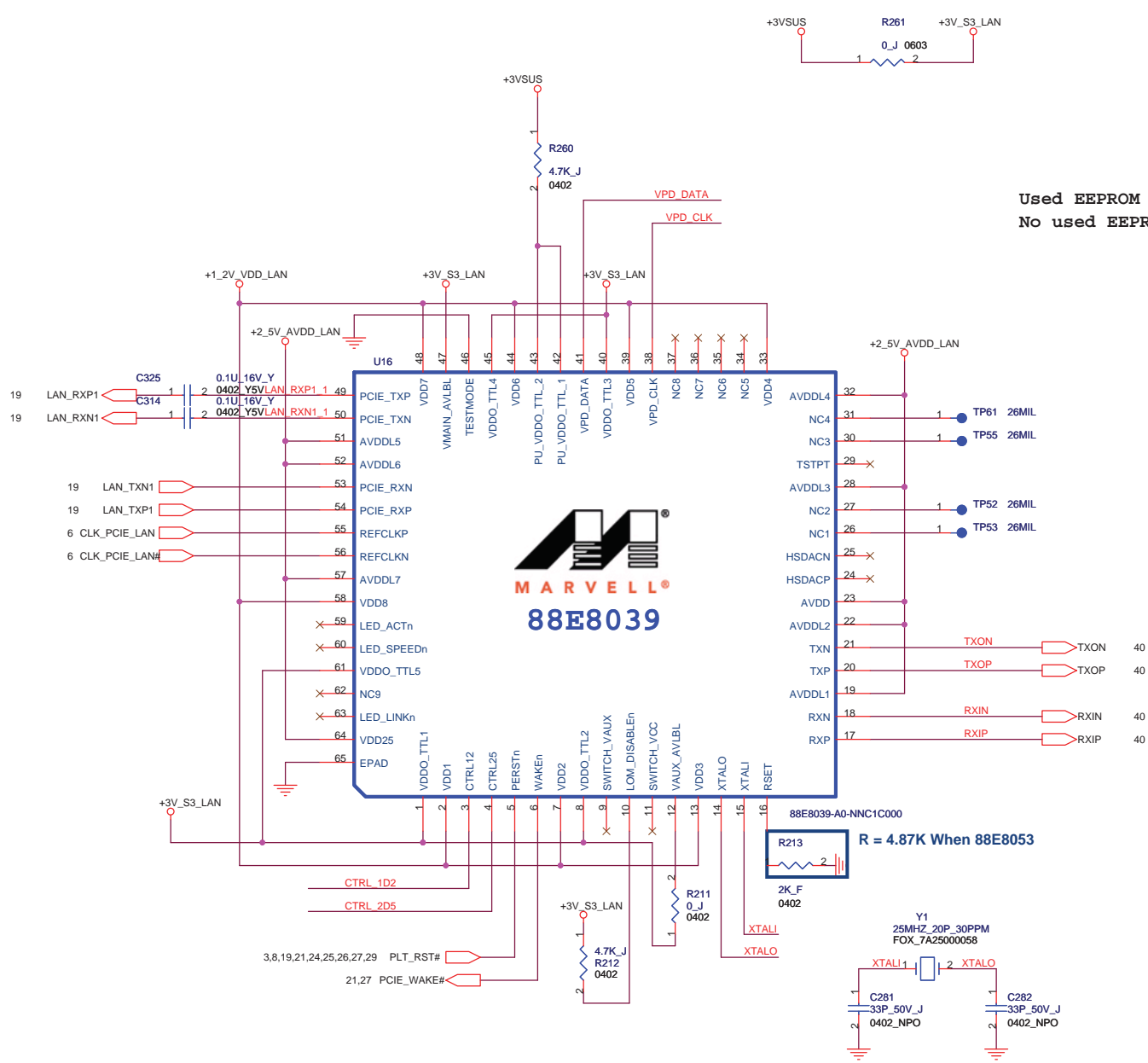




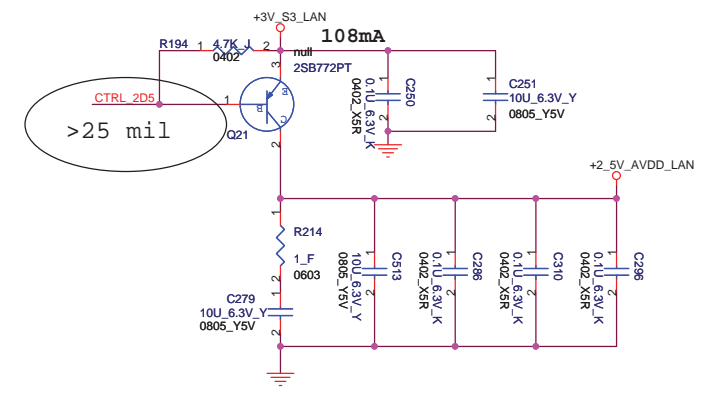
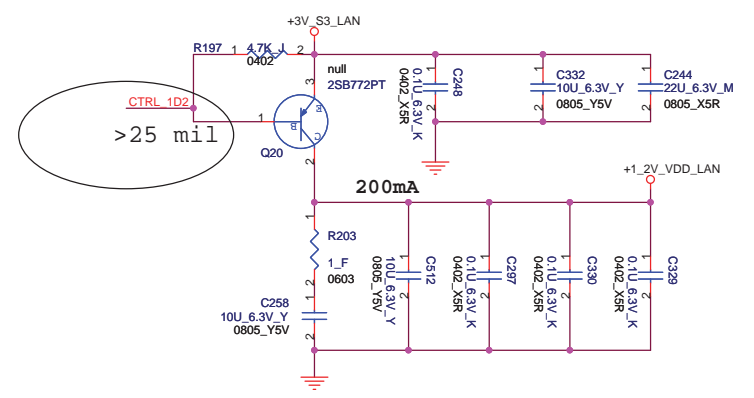
**USB CONN.**

TID:60001164

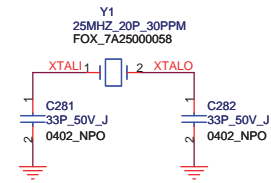
TID:60001164



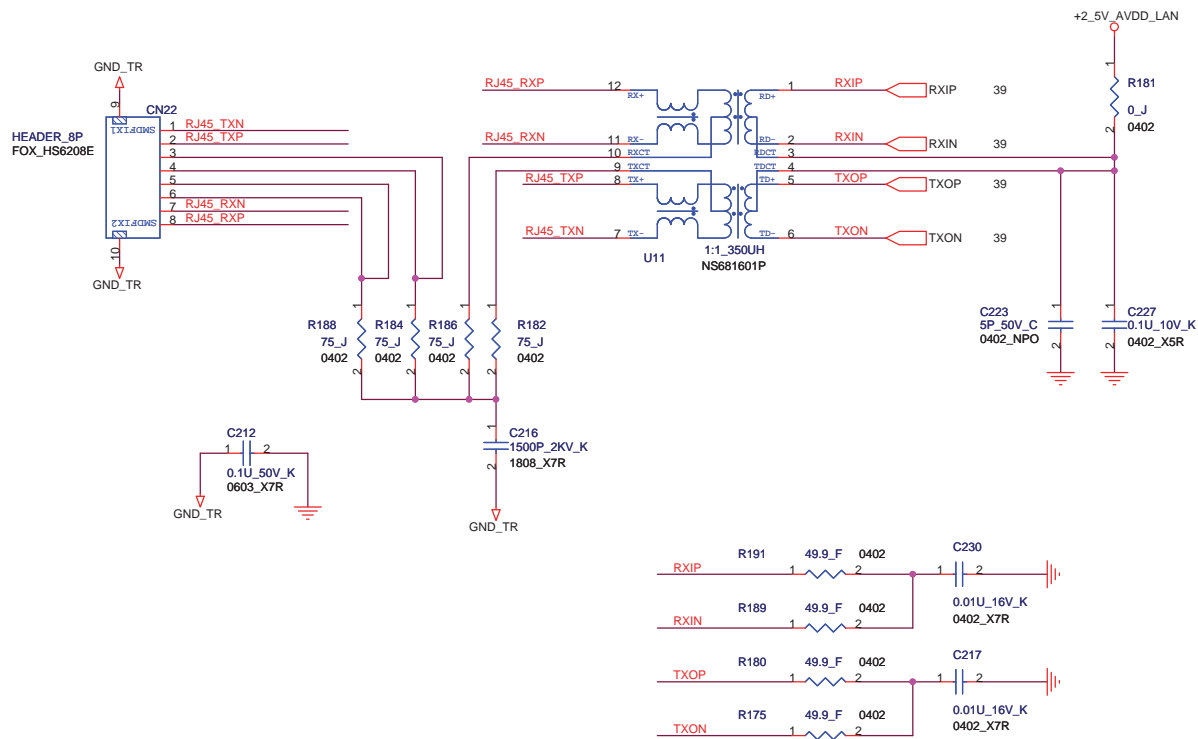
Used EEPROM R275 need NC.  
No used EEPROM R270/U17/C337 need NC.



R = 4.87K When 88E8053



<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title <b>LAN (88E8036)</b>		
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 39	of 56

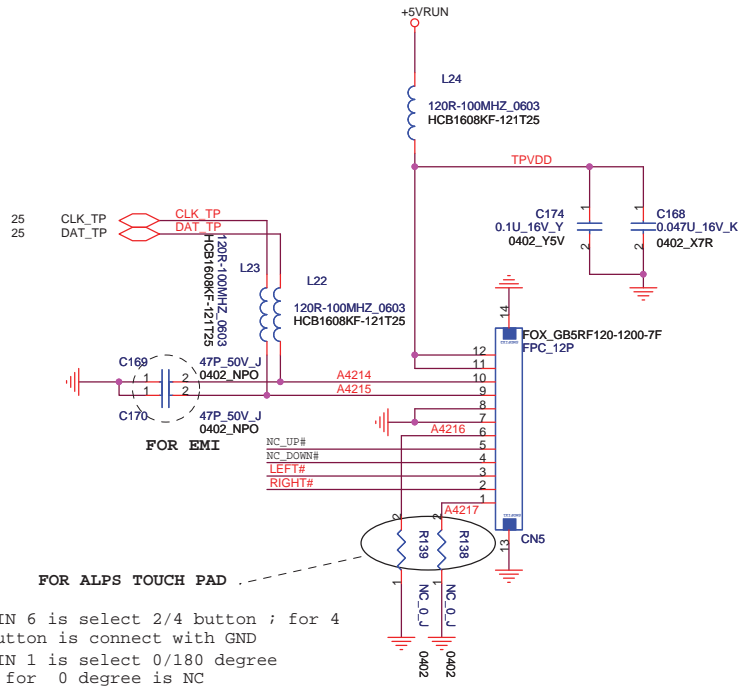


<http://hobi-elektronika.net>

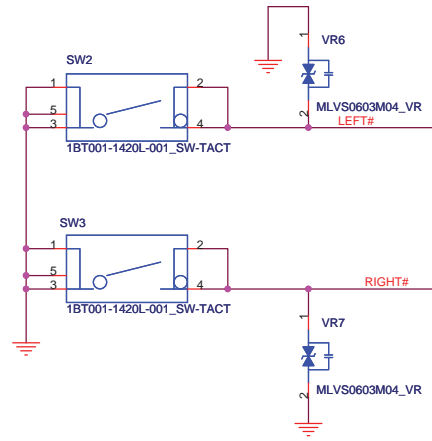
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.
Title <b>LAN Transformer</b>		CCPBG - R&D Division
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 40	of 56



# Touch Pad CONN.

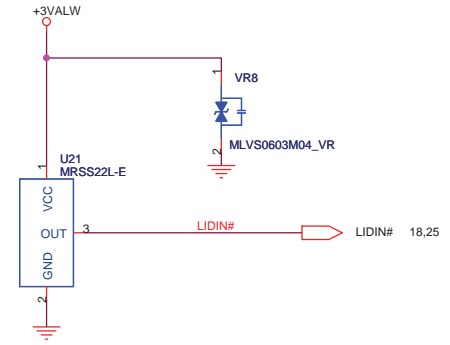


# TP\_LEFT Button

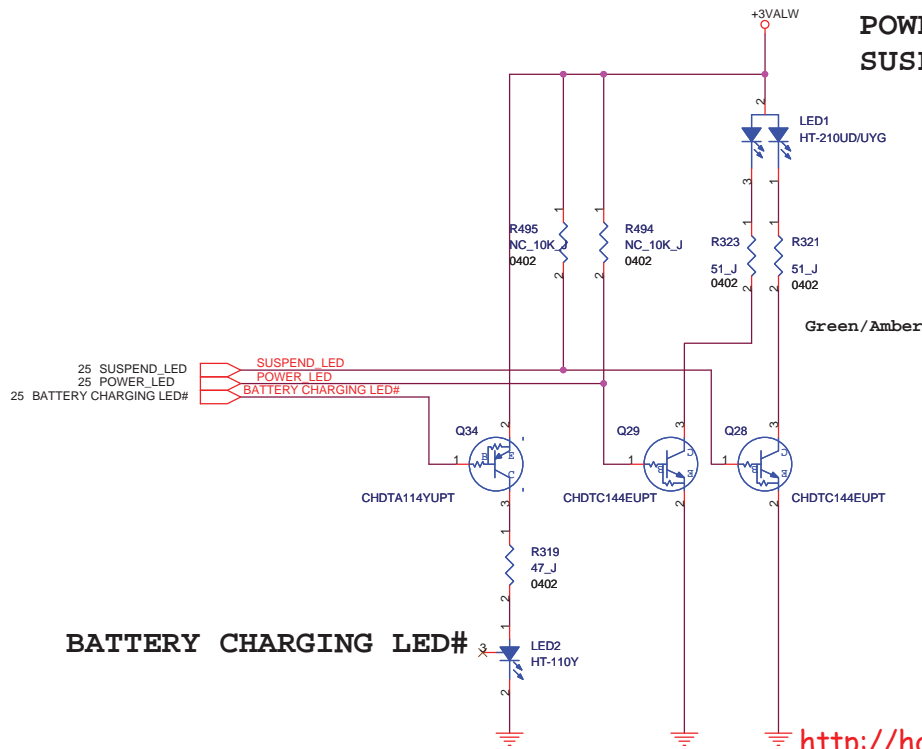


# TP\_Right Button

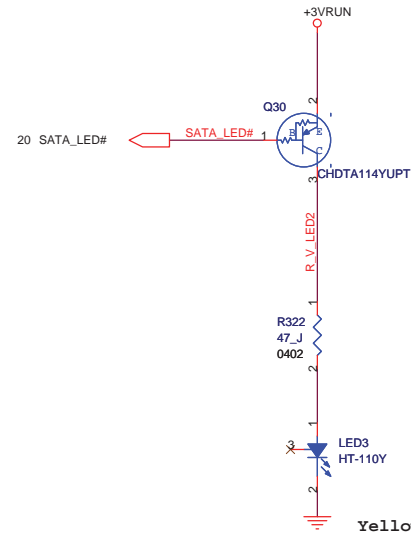
# LID Switch



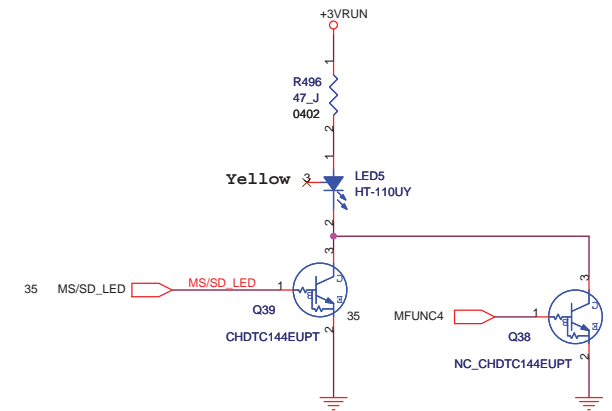
# POWER\_LED SUSPEND\_LED



# SATA\_LED#



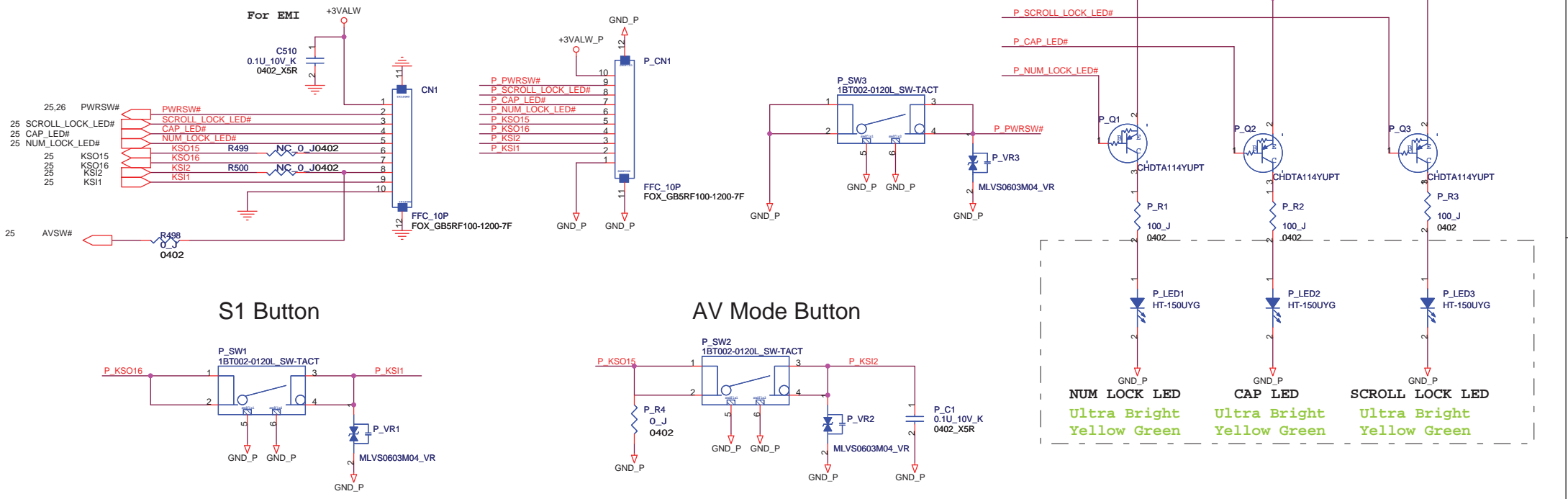
# MS/SD LED



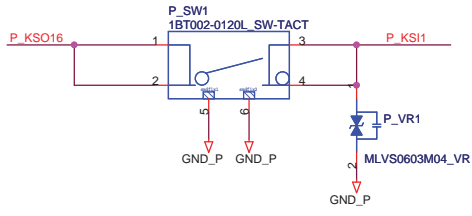
# BATTERY CHARGING LED#

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		LED/Touch/Lid	
Size	Document Number	Rev	
A3	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	41 of 56

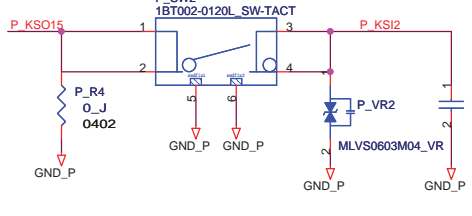
# Power Button Board



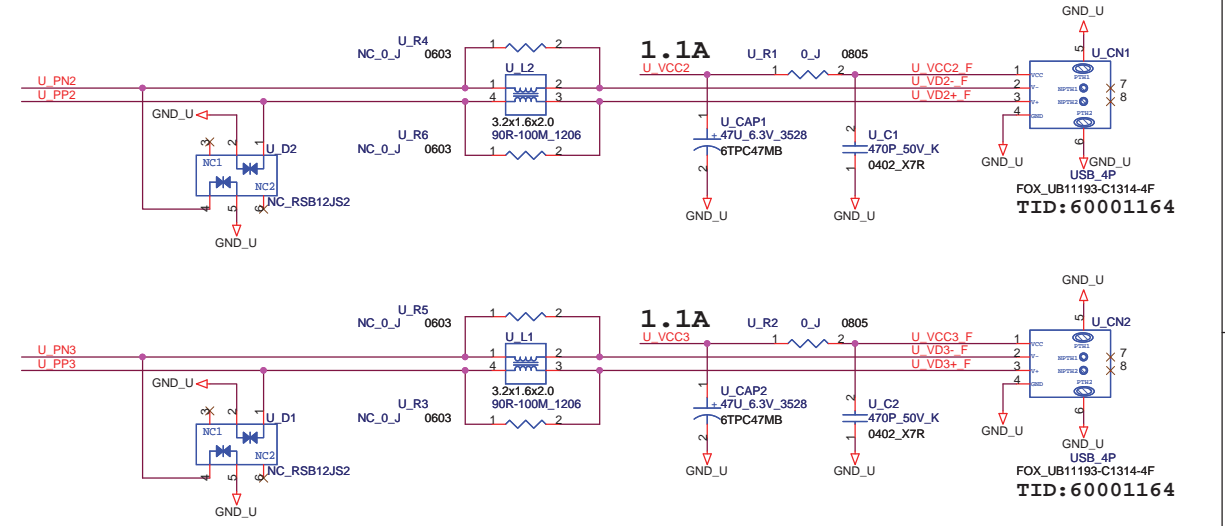
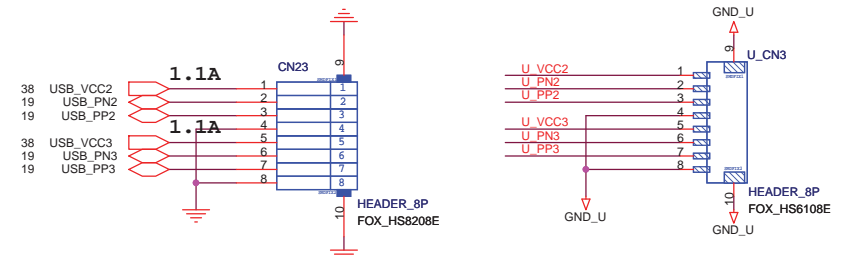
## S1 Button

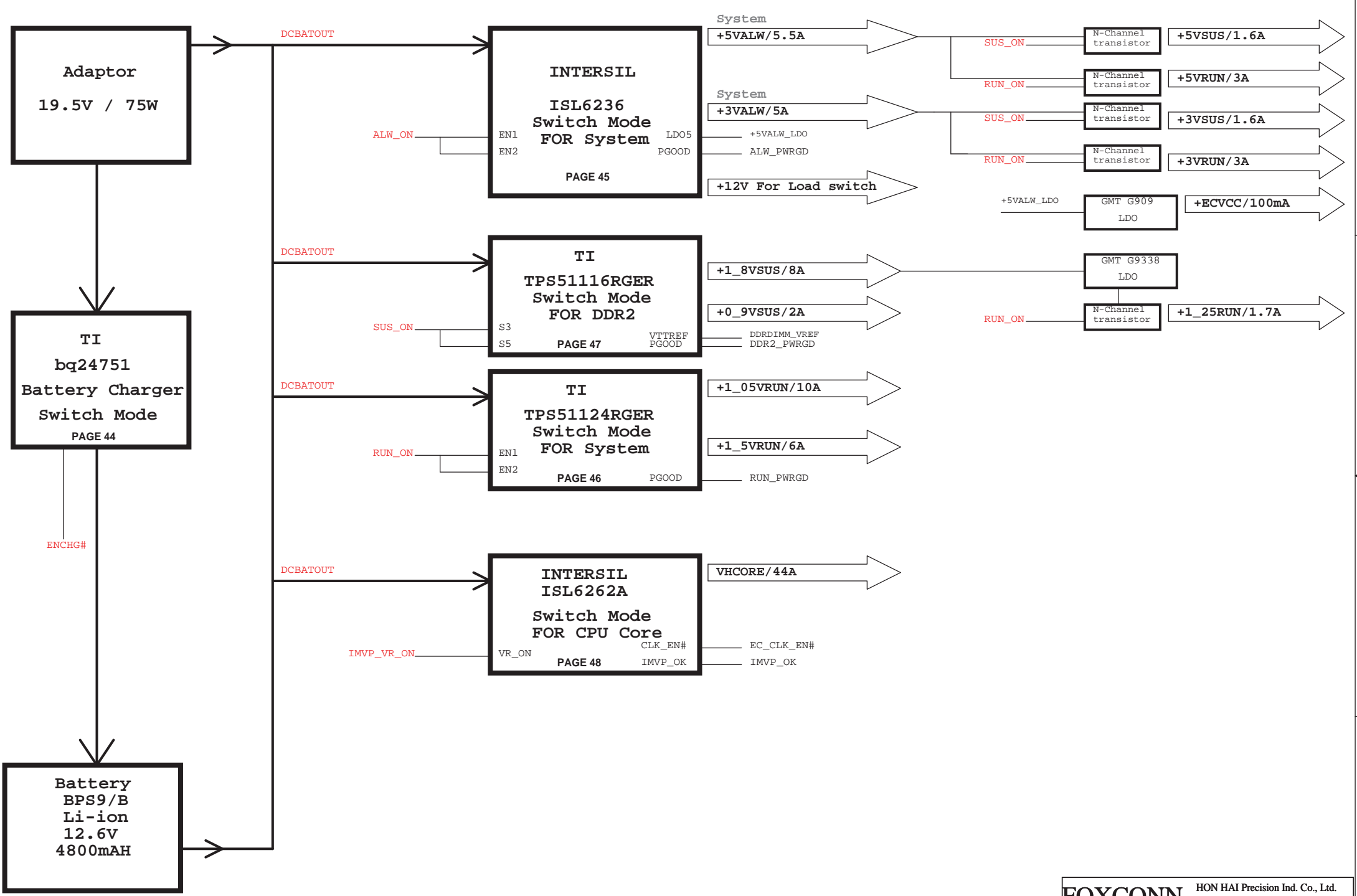


## AV Mode Button



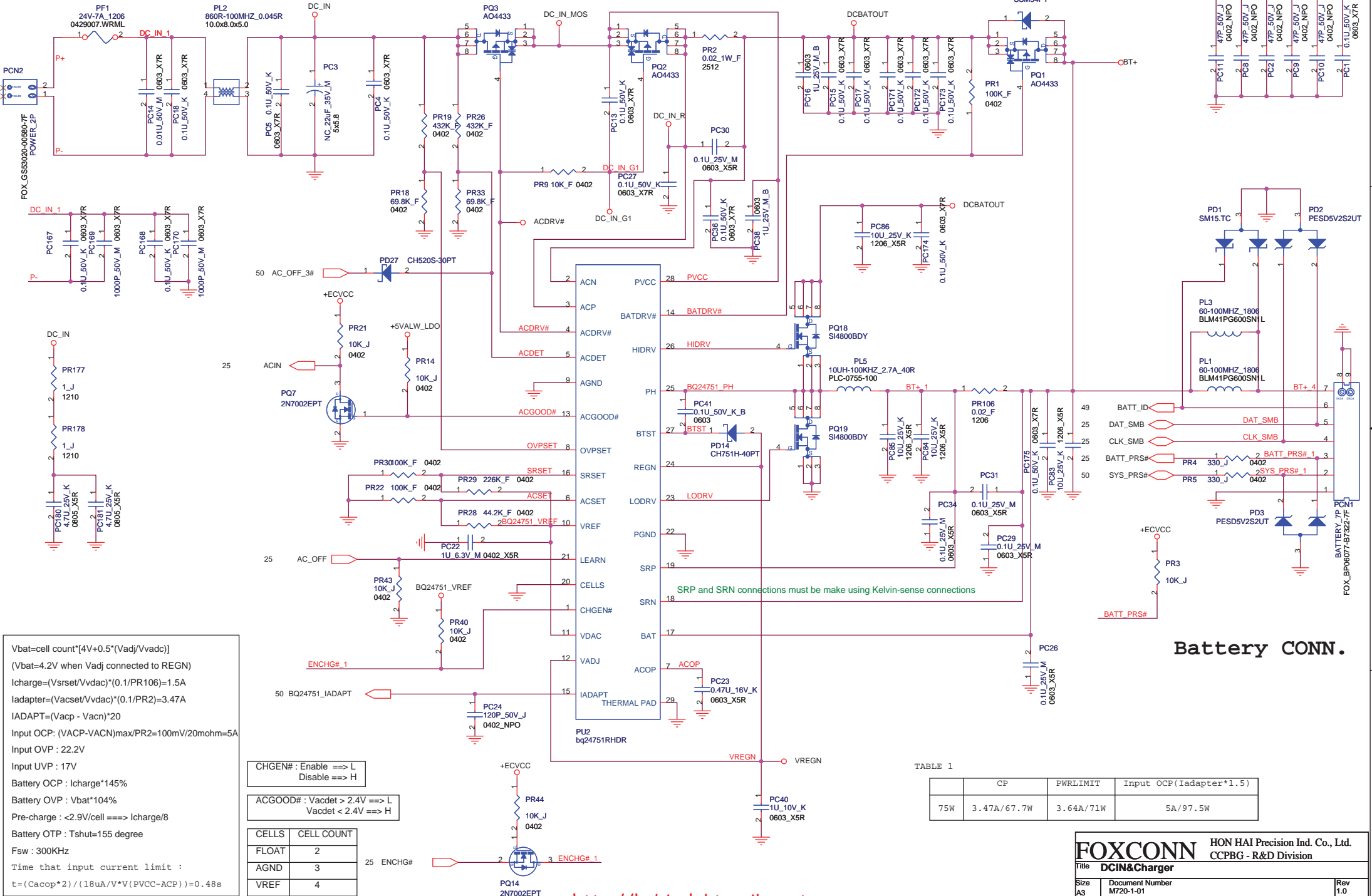
## USB Board





ACP and ACN connections must be make using Kelvin-sense connections

BT+ 4  
 DAT SMB  
 CLK SMB  
 BATT\_PRS# 1  
 SYS\_PRS# 1  
 BATT\_ID



$V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})]$   
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to REGN})$   
 $I_{charge} = (V_{srset} / V_{vdc}) * (0.1 / PR106) = 1.5A$   
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR2) = 3.47A$   
 $IADAPT = (V_{acp} - V_{vacn}) * 20$   
 Input OCP:  $(V_{acp} - V_{vacn}) / \max(PR2) = 100mV / 20m\Omega = 5A$   
 Input OVP: 22.2V  
 Input UVP: 17V  
 Battery OCP:  $I_{charge} * 145\%$   
 Battery OVP:  $V_{bat} * 104\%$   
 Pre-charge:  $< 2.9V / \text{cell} \implies I_{charge} / 8$   
 Battery OTP:  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$   
 Time that input current limit:  
 $t = (C_{acop} * 2) / (18\mu A / V * (V_{vcc} - ACP)) = 0.48s$

CHGEN# : Enable ==> L  
 Disable ==> H  
 ACGOOD# :  $V_{acdet} > 2.4V \implies L$   
 $V_{acdet} < 2.4V \implies H$

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

TABLE 1

	CP	PWRLIMIT	Input OCP(Iadapter*1.5)
75W	3.47A/67.7W	3.64A/71W	5A/97.5W

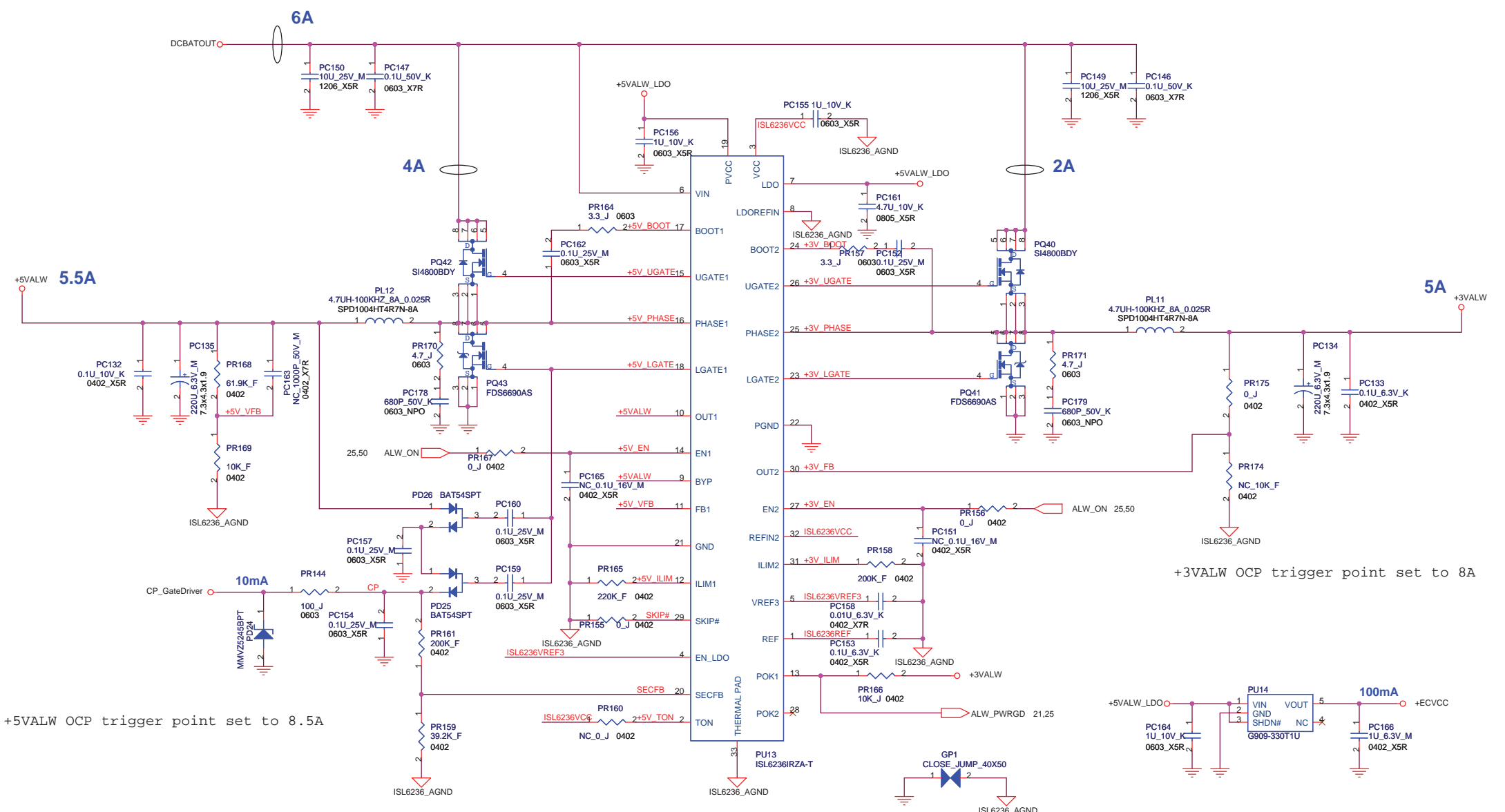
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **DCIN&Charger**

Size A3	Document Number M720-1-01	Rev 1.0
---------	---------------------------	---------

Date: Wednesday, July 18, 2007 | Sheet 44 of 56

<http://hobi-elektronika.net>



+5VALW OCP trigger point set to 8.5A

+3VALW OCP trigger point set to 8A

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / (VIN * f * LIR * ILOAD(MAX))$$

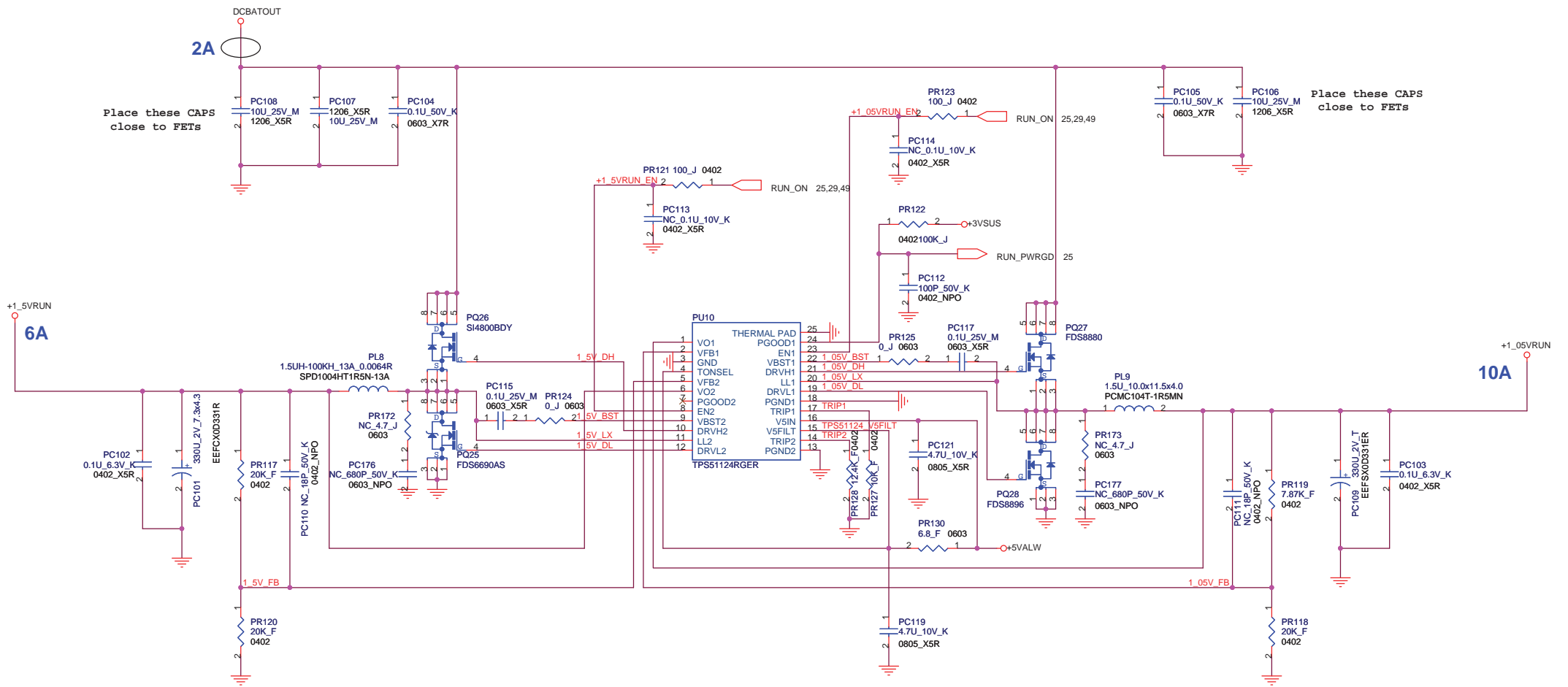
$$Rocp = (Iocp - Iripple / 2) * (10 * Rds(on)) / 5u$$

<http://hobi-elektronika.net>

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

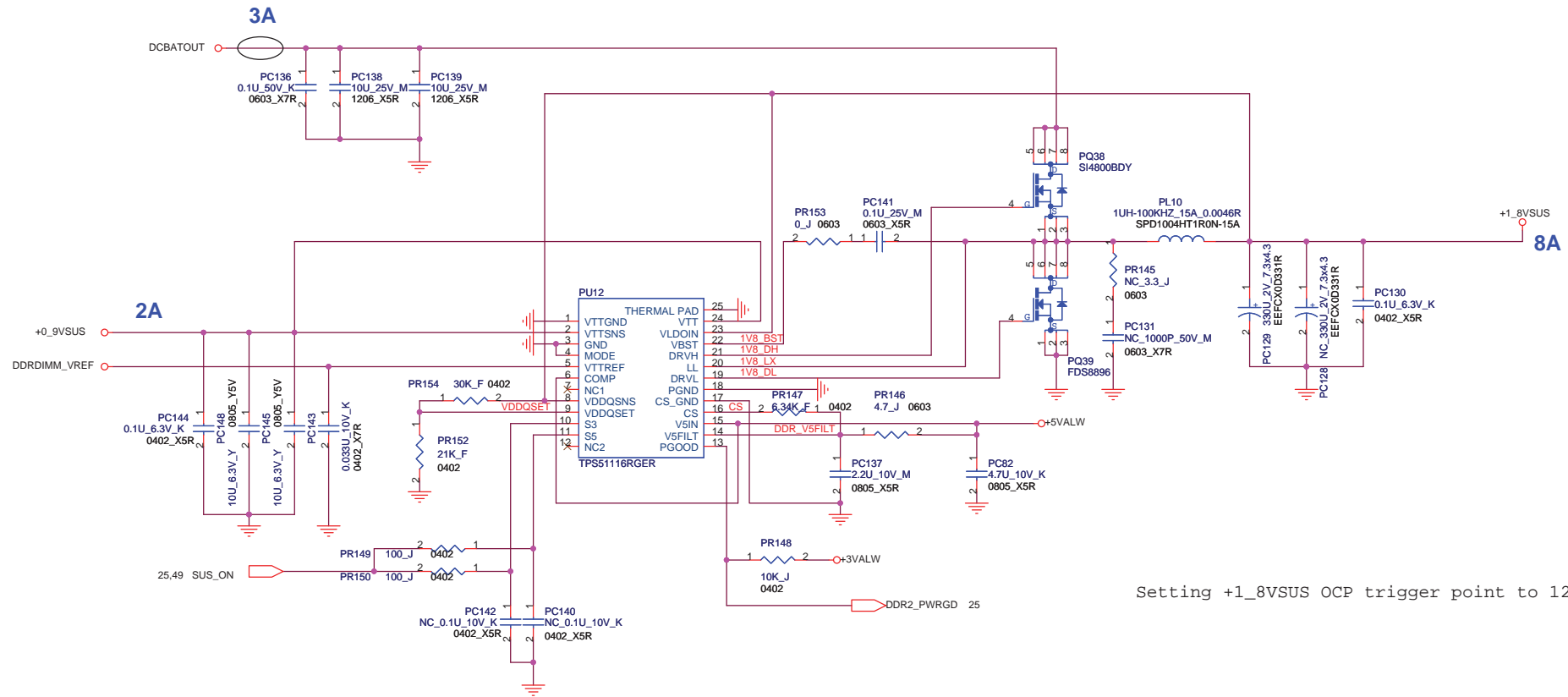
Title: **SYS Power (+3\_3V/+5V)**

Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 45	of 56



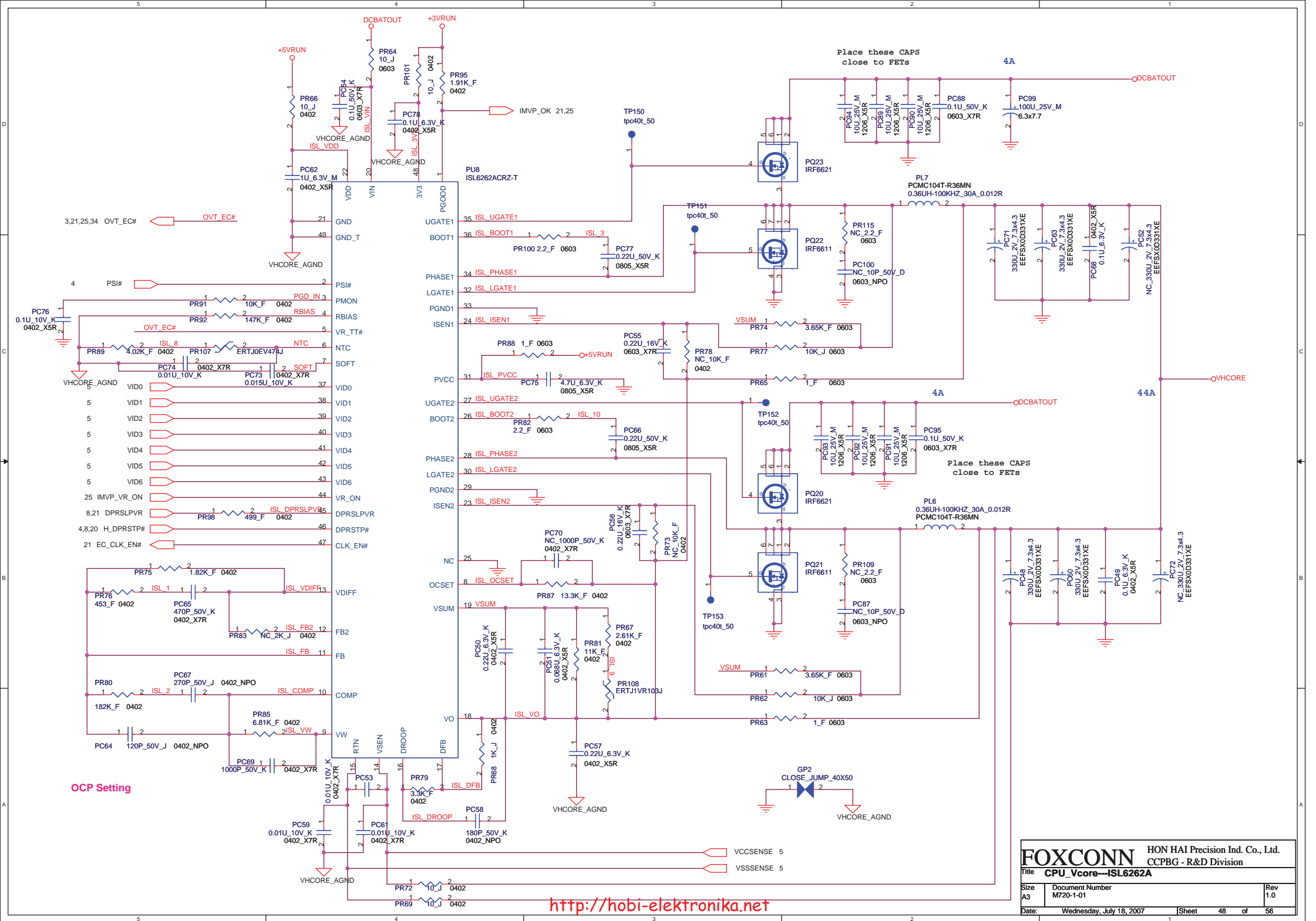
Setting +1\_5VRUN OCP trigger point to 10.6A

Setting +1\_05VRUN OCP trigger point to 14.2A

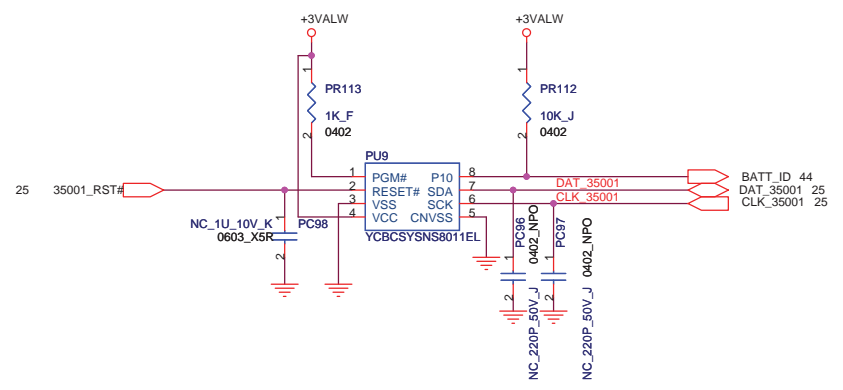
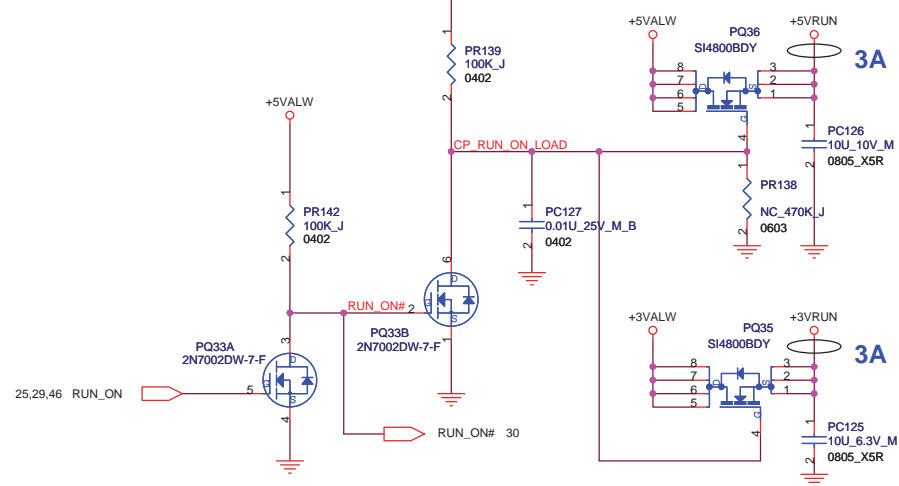
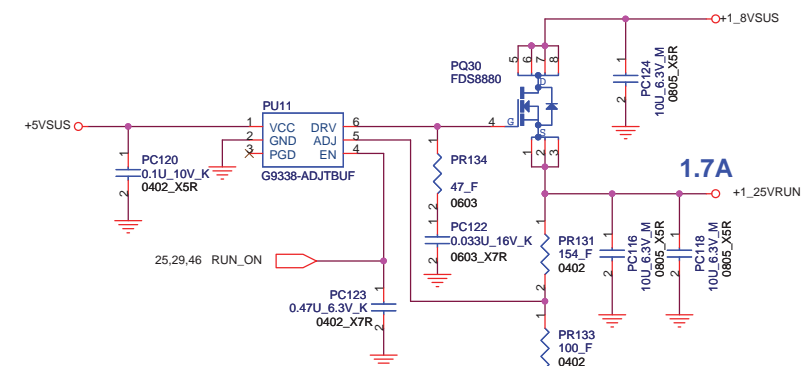
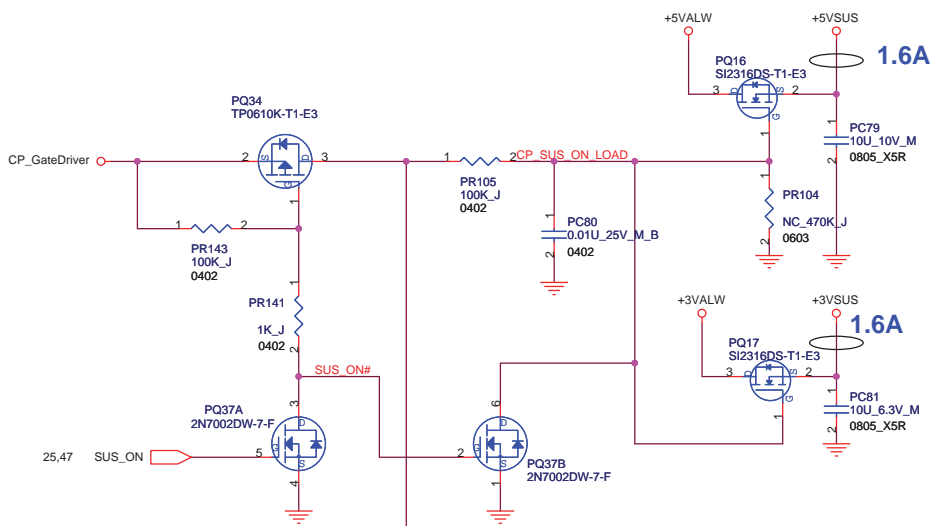


Setting +1\_8VSUS OCP trigger point to 12A

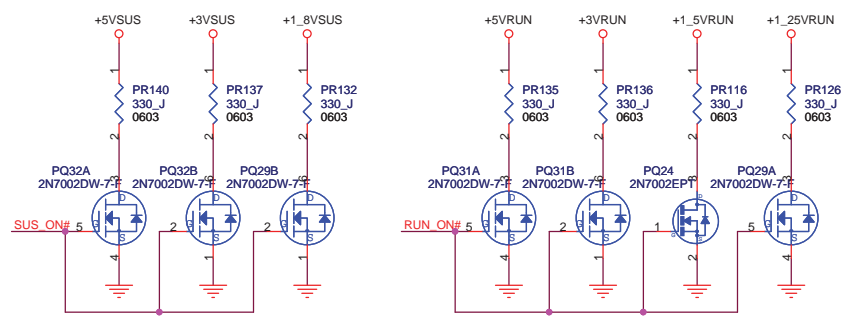
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>DDR2 Power(+1_8V/+0_9V)</b>			
Size	Document Number	Rev	
A3	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	47 of 56





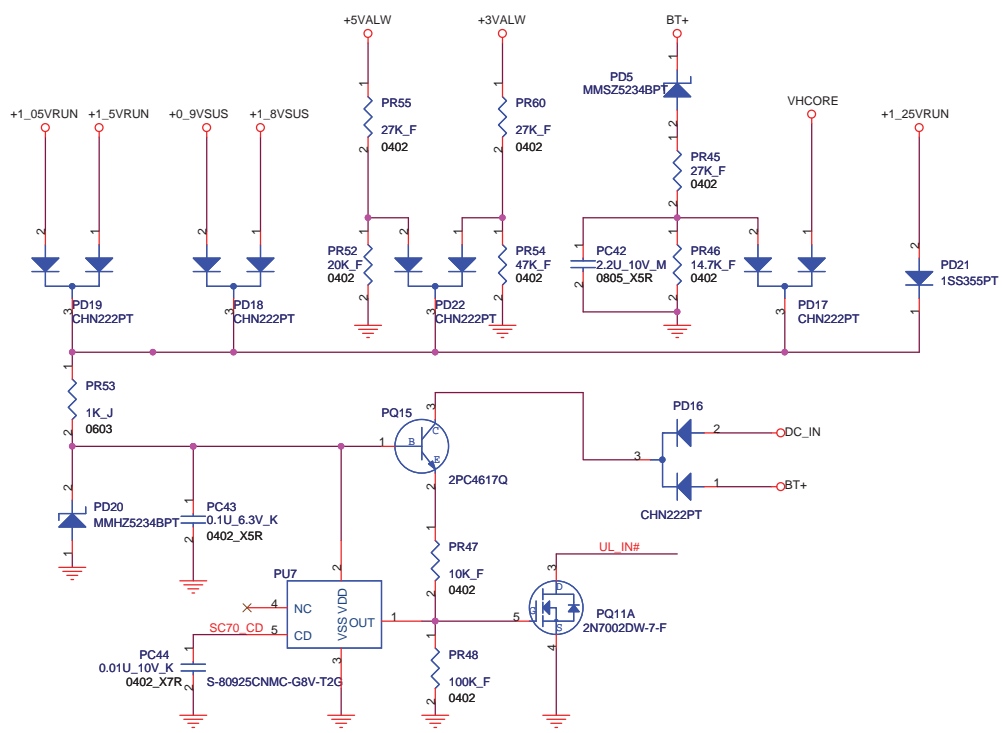


Discharge circuit for power-off

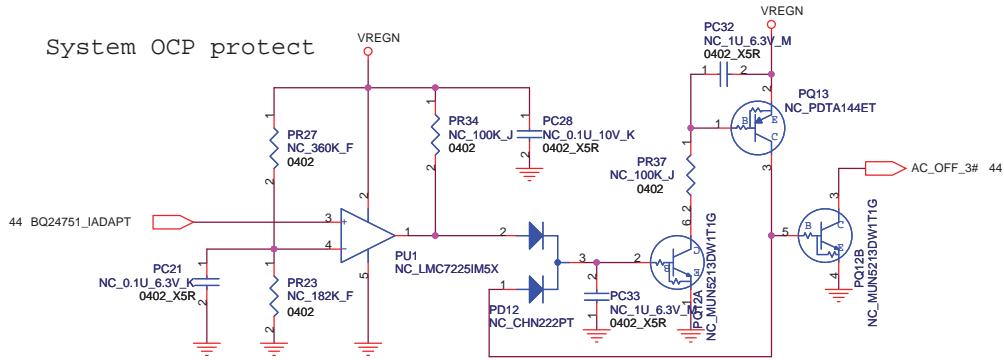


<http://hobi-elektronika.net>

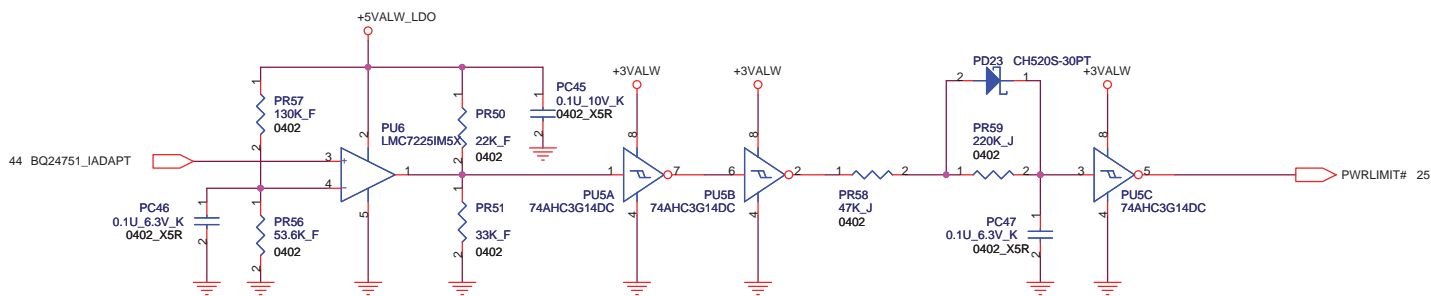
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>Others power plan</b>		CCPBG - R&D Division	
Size A3	Document Number M720-1-01	Rev 1.0	
Date: Wednesday, July 18, 2007	Sheet 49	of 56	



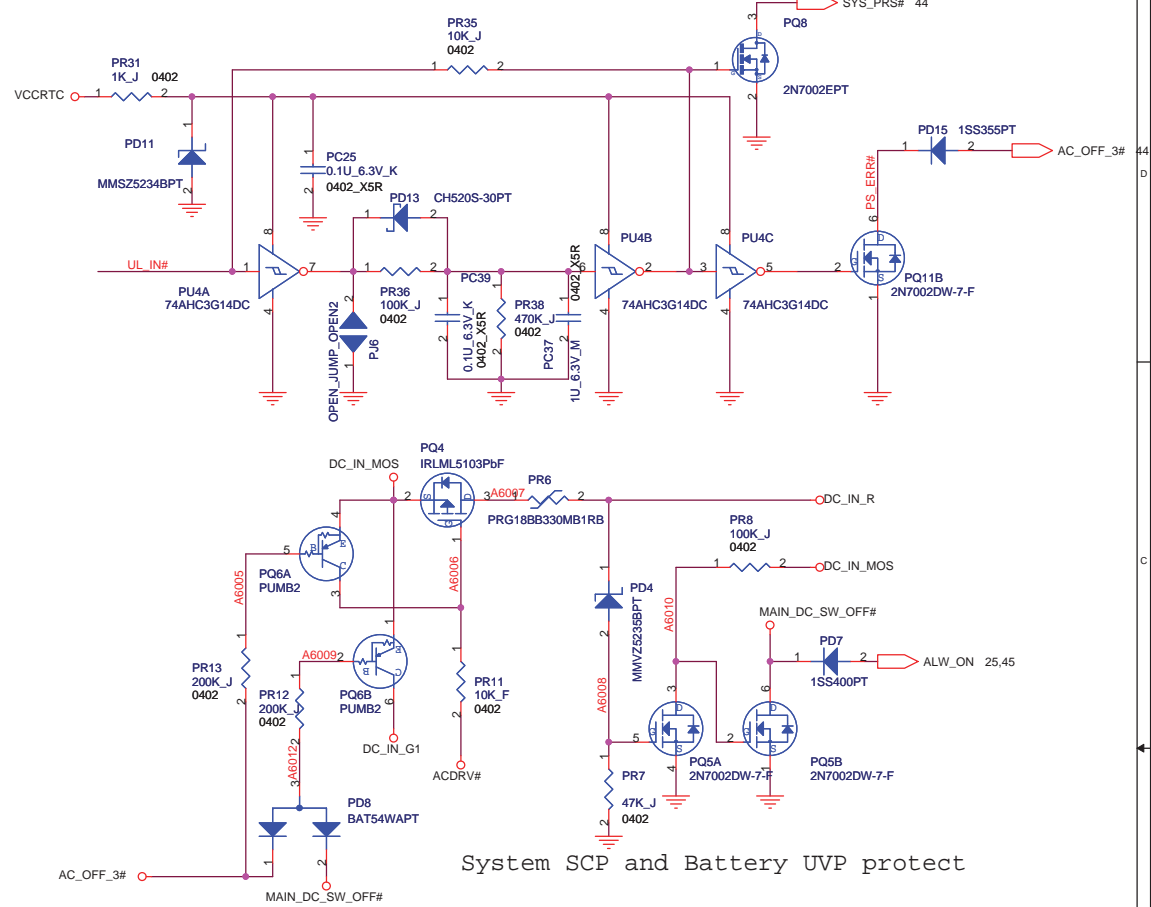
System OCP protect



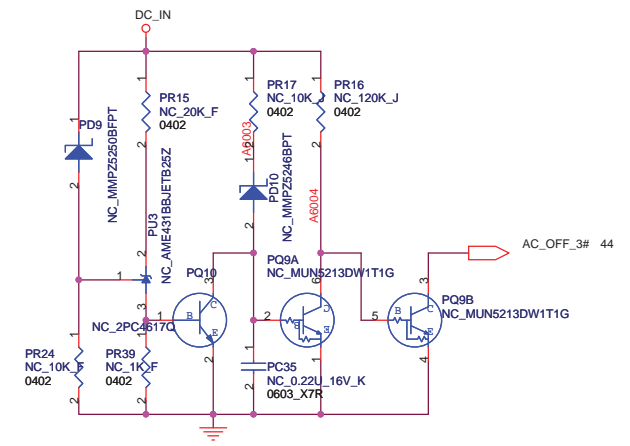
Setting System OCP trigger point to 4.2A



Setting PWRLIMIT# trigger point to 3.64A

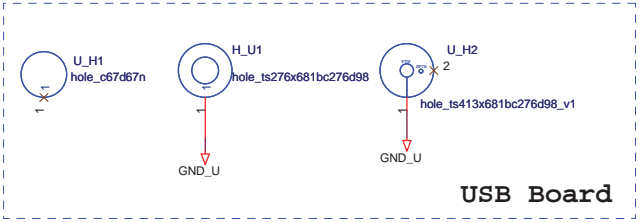
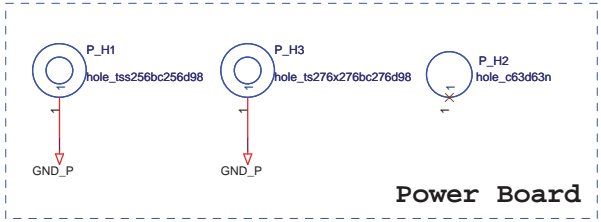
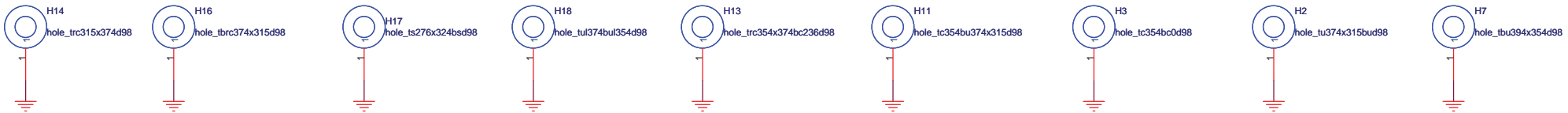
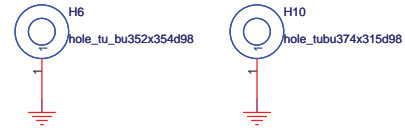
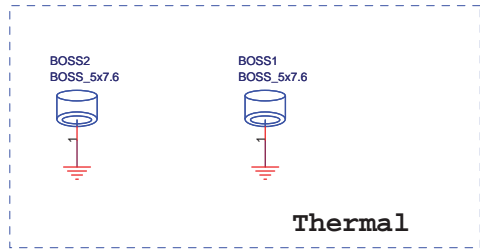
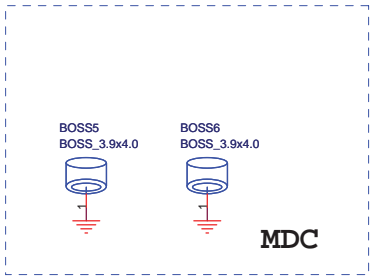
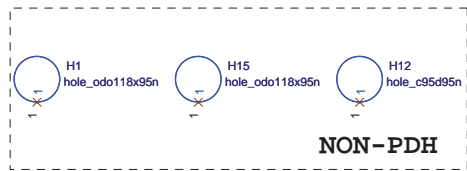
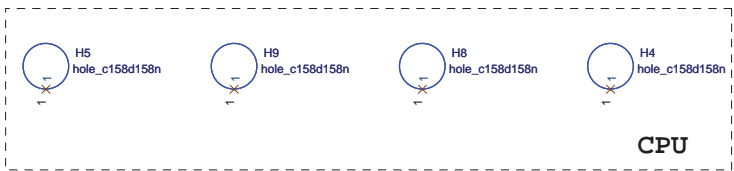


System SCP and Battery UVP protect



DC\_IN OVP and UVP protect

<http://hobi-elektronika.net>



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		HOLE	
Size	Document Number	Rev	
A3	M720-1-01	1.0	
Date:	Wednesday, July 18, 2007	Sheet	51 of 56

## M720 EVT

### (2007/02/14)

- P.27 Change Q104 for DTC144 to 2N7002,delete R2217
- P.38 Change U64,U65,U66,U69 from G5250 to G545

### (2007/02/26)

- P.41 Add Q158 for MS/SD LED.

### (2007/02/27)

- P.49 Add PC147 and PC149 0.01uF\_25V 0402 for soft start circuit.
- P.50 Add DC\_IN OVP, DC\_IN UVP, System\_OCP and System\_SCP protection circuit.
- P.50 Change PR270 from 33K\_F 0402 to 53.6K\_F 0402 for Setting PWRLIMIT# trigger point to 3.64A

### (2007/02/28)

- Delete GMCH power
- P.12 Delete PJ13 for +VGF\_X\_CORE power change to +1\_05VVRUN.
- P.20 Delete TP263,add R1790 pull down for LAN\_RST function on intel ICH8M request.
- P.49 Delete PR243~PR245,PQ8 for GMCH power IC delete.
- P.50 PD21 from CHN222PT change to 1SS355PT for GMCH power IC delete.

### (2007/03/05)

- P.50 Change DC\_IN OVP, DC\_IN UVP, System\_OCP and System\_SCP protection circuit to no mount.

### (2007/03/06)

- For layout request swap L69,L75,L80,LVDS signal.
- P.44 Change PF1.
- P.48 Change PU8 pin25 from VHCORE\_AGND to GND for layout convenient

### (2007/03/07)

- For layout request swap U\_L1,U\_L2 signal.

### (2007/03/08)

- Update LED tepe for ID.
- P.25 Update system ID table.
- P.42 Add S1/S2 function,Change CN22,P\_CN1 to 10pin.
- P.44 Add PR7 10K\_F 0402 and PC38 0.1uF\_50V 0603 X7R for DC\_IN soft start circuit.
- P.46 Change PL11 from MP0104-1R5 to PCMC104T-1R5MN
- P.49 Add PR220 1K\_J 0603 for soft start circuit.
- P.50 Mount System SCP circuit.

### (2007/03/12)

- Battery/LVDS/RJ45/USB board connector,change new type,Touch pad/Wlan switch change new type.
- P.44 Change PC20 from 0.01U\_25V 0402 to 0.01U\_50V 0603.
- P.44 Change PR10 from 40.2K\_F 0402 to 226K\_F 0402 for setting charger current to 1.5A.
- P.44 Change PR13 from 24.9K\_F 0402 to 44.2K\_F 0402 for setting constant power to 3.47A.
- P.46 Change +1\_05VVRUN power rating to 10A.
- P.48 Add PR361, PR362, PR363 and PR364 0\_J 0603 for testing.
- P.51 Update Screw pad size.

### (2007/03/13)

- P.11 Add L98,C1089,L22,R678,C155,L89,L21,C168,Change +V1.5S\_CRT to +V1.5S\_TVDAC,Change +VCC\_DMI to +VCC\_RXR\_DMI.
- P.17 Delete R1145,R1146,Change F6 to 1206L035,R1148,R1149 to 24ohm,D7 to SSM24APT.
- P.18 Delete R457,R1272,ODD\_RXIN3-,ODD\_RXIN3+ signal.

### (2007/03/14)

- P.9 Add R124,R125,R126
- P.11 Delete R149
- P.18 Delete R461

### (2007/03/15)

- P.11 Delete L92,L94,L96,L97
- P.18 Delete R1268,R2225.
- P.27 Delete CN39
- P.52 Update Power /USB board screw pad.Change H28,H29 to Boss5,Boss6,Delete H3,H4,H6,H7,H10,H19~H22,Add Boss3.Boss4 for Mini-PCI-E

### (2007/03/16)

- P.17 Change D7 to SSM24APT
- P.18 Update LVDS connector pin define.
- P.44 Delete close jump GP1 and change PU3 bq24751\_AGND to GND for layout convenient

### (2007/03/19)

- SWAP RP9,RP10,RP12,RP13,RP17,RP20,RP22,RP23,RP25,RP30 for layout.
- CON1/CON2 pin7,pin8 connector to D\_GND
- P.51 Update Power /USB board screw pad GND.

### (2007/03/20)

- P.27 Change Q104 to 2N7002ESPT,Add R2225.
- P.44 Change PR2 from NC\_4.7\_J 0805 to 1\_J 0805.  
Change PC24 from NC\_4.7U\_25V 0805 to 10U\_25V 1206  
Add PC39 10U\_25V 1206  
Change PC6 from 0.1U\_50V to no mount  
Change PC8 from 10U\_25V\_K to no mount  
Delete PC2 and PC3 10U\_25V  
Above change are for damping input inrush voltage from TI application note.
- P.44 Change PC29 from 10U\_25V\_K to no mount for TI application note.
- P.45 Add PR139 0\_J 0402 for testing
- P.46 Delete GP3 Close\_Jump for TI application note.
- P.47 Delete GP4 Close\_Jump for TI application note.
- P.49 Change PQ70 from 2N7002EPT to 2N7002DW-7-F  
Change PR220 from 1K\_J 0603 to 100K\_J 0402  
These change are for load switch slow ON and fast OFF.
- P.51 Update H18,P\_H1,P\_H2,U\_H2,U\_H3,Add P\_H3

### (2007/03/21)

- P.19 SWAP RP92~RP94 for Layout.
- P.24 Update ODD/HDD connector.

### (2007/03/22)

- P.16 SWAP RP21 for Layout.
- P.31 SWAP JSPK1 for Layout.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History (1)</b>			
Size A3	Document Number M720-1-01	Rev 1.0	
Date Wednesday, July 18, 2007	Sheet 52	of 56	

**(2007/03/23)**

P.8 Delete R1929,R1930.  
 P.9 Change R124~R127 to 75ohm.  
 P.25 Delete R2029,Add TP322.  
 P.27 Delete R2225.  
 P.30 Delete C1840.Change SNESE\_A to SENSE\_A.  
 P.31 Change R2153,R2154,R2156,R2157 to 2.2Kohm.HP\_IN\_DET to SP\_MUTE.  
 P.32 Change C1811,C1819 to 100P,C1814,C1824,C1810 tp 4.7uF/10V.  
 P.33 Delete R2185,U146,U147,Change HP\_IN\_DET to SP\_MUTE.  
 P.48 Delete PJ7 for layout convenient.  
 P.42 Change netname of U\_D1.2 and U\_D2.2 from GND to GND\_U.  
 P.51 Delete U\_H1.1 net for U\_H1 is N-PTH.

**(2007/03/26)**

Add C1858~C1860 for EMI request.  
 P.46 Change PC67 to mount for +1\_05VRUN 10A loading.

**(2007/03/27)**

Add C1861~C1864\_NC for EMI request.  
 P.41 Change LED12 to HT-110Y for MOR request.

**(2007/03/28)**

Rename location.  
 P.8 U8 nc pin add net for repair. Add C509 for CL\_CLK0 and CL\_DATA0 through +1\_05VRUN,+1\_5VRUN.  
 P.9 U8 nc pin add net for repair.  
 P.42 Add C510 for EMI request.

**(2007/03/29)**

P.29 Change Q37,R479 to mount,R480 to NC.

**DVT****(2007/04/11)**

P.25 Add KSI015/KSI2 for AV mode function.  
 P.42 Update CN1,P\_CN1 pin define for AV mode functin,Mirror P\_CN1 for M/E easy a'ssy.

**(2007/04/12)**

P.34 Mirror U12 SMBUS\_CLK and SMBUS\_DATA signal.  
 P.44 ACGOOD# pull high voltage change from BQ24751\_VREF to +5VALW\_LDO for charger LED abnormal issue.  
 P.44 PR32 0 ohm change to PD27 CH520S-30PT Schottky Diode for PU2 OVP issue.

**(2007/04/20)**

P.20 Add PM\_THRMTRIP# signal and R497 connect to N.B and CPU.  
 P.41 Change LED5 to HT-110UY for MS/SD LED brightness issue.

**(2007/04/24)**

P.19/39 Change Express LAN interface to port5 for S/W issue.  
 P.44 Delete PL4 BCMS451616A600 8A  
 P.44 Change PL2 from BCMS451616A600 8A to SMH 100805-4T for EMI request

**(2007/04/30)**

P.22 Delete R436,L43,NC C470 for Intel D.G.(2.0).

**(2007/05/08)**

P.41 Change SW2/SW3 botton switch for MOR request.

**(2007/05/10)**

P.27 Change SW4 WLAN switch.

**(2007/05/11)**

P.20 Change C300/C301 to 12pF.  
 P.39 Change C281/C282 to 33pF.

**(2007/05/15)**

P.16 Mount C255,C267,C293,C309 for EMI.  
 P.18 Mount C376 for EMI.  
 P.44 Add PC167~PC175 for EMI.  
 P.45 Change PR157,PR164 to 3.3ohm,Add PC178,PC179(680pF), PR170,PR171(4.7ohm) to mount for EMI.  
 P.46 Add PC176,PC177(680pF),PR172,PR173 no mount for EMI.  
 P.48 Change PC88,PC95 to mount for EMI.

**(2007/05/17)**

P.44 PC84 change from NC to mount for reducing charger ripple/noise.  
 P.44 PC23 change from 0.47U\_16V\_M 20% to 0.47U\_16V\_K 10% for Purchase difficult.  
 P.45 Add PR174 NC\_10K\_F 0402 and PR175 0\_J 0402 for reserving +3VALW output adjustable.  
 P.49 Change PQ30 from VISHAY SI4800BDY to FAIRCHILD FDS8880 for more safety power rating.

**(2007/05/18)**

P.30 Change C444 from 10uF to 2.2uF,add C511 for Audio POP issue.  
 P.20 Change R223 to no mount.

**(2007/05/21)**

P.44 Delete PC6, PC7 and PC12 for layout space.  
 P.44 Delete PR10, PC19, PC20  
 Change PC3 from 10uF\_25V\_1206 to 22uF\_35V EC CAP  
 Change PC38 from 1uF\_25V\_0603 to 4.7uF\_25V\_0805  
 Add PR176 10\_J\_0805  
 These change are for DC\_IN damping circuit.  
 P.44 Change PU2 pin28 net-name from DC\_IN\_MOS to PVCC  
 P.44 Change PR2 from 0.02\_F\_1206 to 0.02\_F\_2512 for more safety power rating.

**(2007/05/22)**

P.19 Back PCI-E from port5 to port1.

**(2007/05/24)**

P.38 Add F5~F8 for MOR request.  
 P.44 Change PL2 from SMH 100805-4T to 860R-100MHZ\_0.045R for purchase difficult.  
 P.50 Change PU1 and PQ13 supply voltage from +5VALW\_LDO to VREGN for application modification.  
 P.51 Change BOSS1 and BOSS2 for Thermal request.

**(2007/05/25)**

P.34 Change U12,R183,R190,C224 to no mount for DDR thrermal disable..

**(2007/05/26)**

P.25 Add R436 for AV mode botton function.  
 P.41 Add R498~R500 P\_R4,P\_C1 for AV mode botton function.

**(2007/05/28)**

P.25 Change GPWU1 to GPWU7 for AV botton.

**(2007/05/29)**

P.30 Change R171 to 22ohm,C215 to 22uf.  
 P.33 Change C201,C202,C204 to X5R.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>History (2)</b>		CCPBG - R&D Division	
Size A3	Document Number M720-1-01	Rev 1.0	
Date:	Wednesday, July 18, 2007	Sheet	53 of 56

# PVT

## (2007/06/25)

- P.24 Change CAP7 to mount, and C275 to no mount for HDD noise issue.
- P.28 Update OIDE pin define foe A'SSY issue.
- P.39 Add C512,C513 for LAN noise issue
- P.51 Update H17 screw hole pad.

## (2007/06/27)

- P.44 Change PR2 vendor from YAGEO to CYNTEC for purchase difficult.
- P.44 Change PC24 from 120pF 10% to 120pF 5% for purchase difficult.
- P.44 Delete PR25, PR41 and PR42 0ohm for application note.
- P.45 Delete PR162 and PR163 0ohm for application note.
- P.45 Delete PJ4 and PJ5 for application note.
- P.46 Delete PR129 0ohm for application note.
- P.46 Delete PJ1 and PJ2 for application note.
- P.47 Delete PR151 0ohm for application note.
- P.47 Delete PJ3 for application note.
- P.48 Change PC67 from 270pF 10% to 270pF 5% for purchase difficult.
- P.48 Delete PR70, PR71, PR84, PR86, PR90, PR93, PR94, PR96, PR97, PR99 and PR102 0ohm for application note.
- P.48 Add TP150, TP151, TP152 and TP153 test pin for application note.
- P.49 Delete PR110, PR111 and PR114 0ohm for application note.
- P.50 Delete PR20 and PR49 0ohm for application note.
- P.51 Update H14 screw hole pad.

## (2007/06/29)

- P.45 Change PU13 pin9,10 net name to +5VALW.

## (2007/07/02)

- P.27 Change LED4 to HT-110YG for LED issue.
- P.41 Change R321,R323 to 51ohm,LED2,LED3 to HT-110Y for LED issue.

## (2007/07/03)

- P.38 Change F5~F8 to 2.6A poly-switch for USB loading and noise issue.
- P.42 Change CN23 to HS-8208E.

## (2007/07/04)

- P.44 Change PC3 from mount to dummy for application note.
- P.44 Change PC38 from 4.7uF\_25V 0805 to 1uF\_25V 0603 for application note.
- P.44 Remove PR176 10\_J for application note.
- P.44 Add PR177, PR178 1\_J 1206 and PC180, PC181 4.7uF\_25V 0805 for DC\_IN RC snubber circuit.

## (2007/07/09)

- P.11 Change L9,L28 to 250mA for component spec. issue.
- P.44 Change PR177, PR178 from 1\_J 1206 to 1\_J 1210 for power rating safety.

## (2007/07/12)

- P.18 Add L46 for EMI issue.
- P.31 Add C514~C517 for EMI issue.

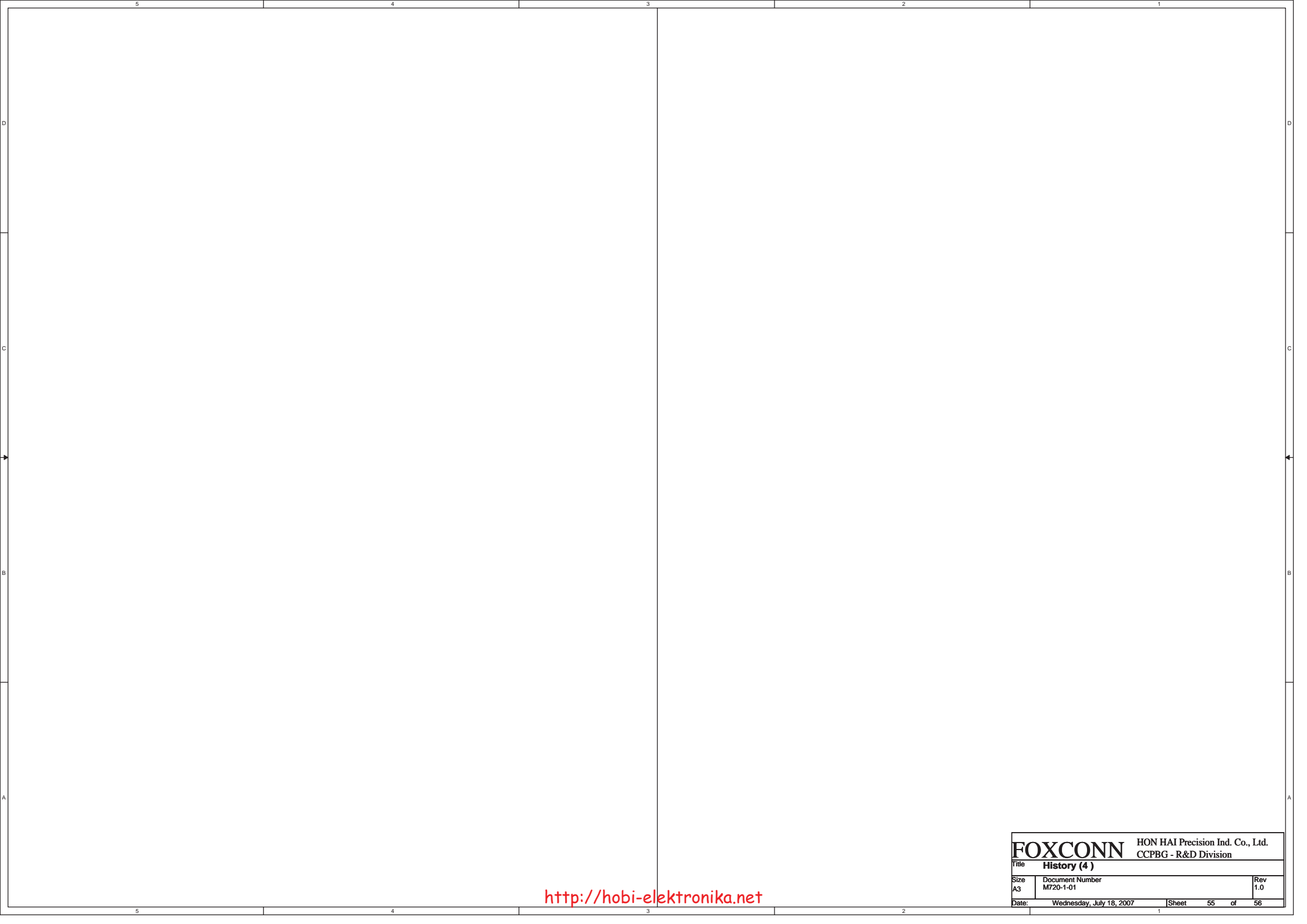
## (2007/07/16)

- P.32 Change C455,C445 to 10uF,R167,R149 to 20 Kohm for MIC. THD+N issue.

## (2007/07/17)

- P.27 Change LED4 to HT-110UYG for MOR request.
- P.45 Change PR177,PR178 to 1/3W for PUR issue.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>History (3)</b>			
Size A3	Document Number M720-1-01	Rev 1.0	
Date:	Wednesday, July 18, 2007	Sheet	54 of 56



<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	<b>History (4)</b>	
Size	Document Number	Rev
A3	M720-1-01	1.0
Date:	Wednesday, July 18, 2007	Sheet 55 of 56



<http://hobi-elektronika.net>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	<b>History ( 5 )</b>	
Size	Document Number	Rev
A3	M720-1-01	1.0
Date:	Wednesday, July 18, 2007	Sheet 56 of 56