VOLTERRA

REVISION - April 6, 2006

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

Smart Slave™	Current Rating	Input Voltage	Output Voltage	VID
VT1105S	25A per Phase	10.8V to 13.2V	0.800V to 1.850V or 0.450V to 2.0375V	VRs 9, 10.X, and Opteron™ or Serial VID (SVID) Mode
VT1125S				
VT1115S*	30A per Phase			
VT1135S*				

GENERAL DESCRIPTION

The VT1165M chipset, Volterra's fourth-generation chipset, is a complete, integrated, scalable architecture for the highest density multi-phase synchronous buck regulators. This ultra high density solution minimizes external components and offers enhanced regulator performance, comprehensive control and reporting features, ease of design and the smallest footprint available for demanding multi-phase synchronous buck converters. The chipset is targeted for applications such as servers and networking systems.

The VT1165M system architecture consists of a master controller (VT1165M), multiple Smart Slave™ integrated output devices, input capacitors, output capacitors and output inductors. The actual number of Smart Slaves™ can be set by the designer and application requirements. The desired slave and load operating conditions are controlled and monitored via an interconnecting digital bus as shown in Figure 1.

With this chipset, Volterra implements enhancements to the digital SMBus interface for monitoring and controlling of the voltage regulator. Regulator parameters can be set and monitored via the two-way SMBus for control, protection and shutdown of the regulator. The SMBus can provide a reading of faults such as VX short-circuit or slave over-temperature, so that the regulator can be controlled and protected during all operating conditions. The SMBus can also provide temperature readings of individual slaves.

A key benefit of the VT1165M is that it provides excellent scalability. This flexibility allows the designer to trade-off cost and performance for a given application using one VT1165M controller and different slave configurations with no redesign or re-layout. The number of phases can be determined by the designer and easily populated or de-populated to meet different load and performance targets.

***NOTE: The VT1165M, VT1105S and VT1125S have a status of NEW PRODUCT. The VT1115S and VT1135S have a status of PRELIMINARY. See the back page of this datasheet for details on these statuses.**

KEY FEATURES

- **Smallest Footprint: Typical Solution Occupies Less than 1600mm^2 in a 150A VRM Application**
- **Lowest Profile: 5mm Maximum Height**
- **Highest Accuracy Current Sharing**
- **Differential Voltage Sense at Point of Load**
- **1A/ns Step Load Transient Response**
- **Scalable Output Current: Up to 8 Slaves**
- **Slave Temperature Reporting**
- **Compatible with Coupled Inductors**
- **Programmable Switching Frequency: 500kHz-1.3MHz**
- **6-Bit VID Input, with 12.5mV Steps and Setpoint Trim for Programmable V_{OUT}**
  - **Intel® VR 9: 1.100V-1.850V**
  - **Intel® VR 10.X: 0.8375V-1.6000V**
  - **AMD® Opteron™: 0.800V-1.550V**
  - **Serial VID (SVID) Mode: 0.450V-2.0375V**
- **Dynamic VID**
- **Programmable VID via SMBUS**
- **Programmable Setpoint and Droop**
- **Programmable OVP, OVLO and UVLO**
- **Cycle-by-Cycle Current Limiting**
- **Power Good Flag, Fault Flag and Output Enable**

SYSTEMS

- **Servers and Workstations**
- **Enterprise Storage**
- **Broadband Communication & Networking**
- **Small Form Factor Desktops**

APPLICATIONS

Voltage Regulator Modules (VRMs) and On-Board Regulators (VR Down)

- **Microprocessors (µP): 32 and 64 Bit I/A and RISC Architectures**
- **Memory**
- **Graphics Processors**

BASIC APPLICATION CIRCUIT

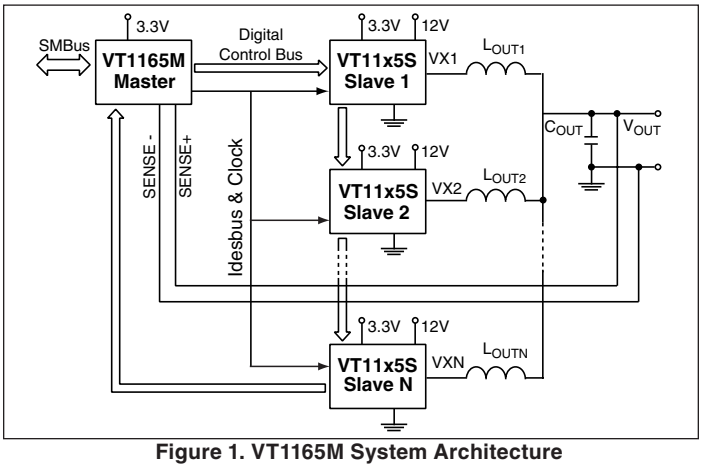


Figure 1. VT1165M System Architecture

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ORDERING INFORMATION

Part Number	IC	Package Style	Drawing Number	Shipment Method	Package Marking
VT1105SCR	25A Smart Slave™	CSP-52	ES AP-0588	250u Tape & Reel	VT1105S
VT1105SCX				2.5ku Tape & Reel	
VT1115SCR	30A Smart Slave™	CSP-53	ES AP-0794	250u Tape & Reel	VT1115S
VT1115SCX				2.5ku Tape & Reel	
VT1125SCR	25A Smart Slave™	CSP-69	ES AP-0760	250u Tape & Reel	VT1125S
VT1125SCX				2.5ku Tape & Reel	
VT1135SCR	30A Smart Slave™	CSP-41	ES AP-0804	250u Tape & Reel	VT1135S
VT1135SCX				2.5ku Tape & Reel	
Lead-Free Options (RoHS Compliant)					
VT1165MFQ	Master	QFN-40	ES AP-0906	Trays	VT1165MF
VT1165MFQX				2.5ku Tape & Reel	
VT1105SFCR	25A Smart Slave™	CSP-52	ES AP-0588	250u Tape & Reel	VT1105SF
VT1105SFCX				2.5ku Tape & Reel	
VT1115SFCR	30A Smart Slave™	CSP-53	ES AP-0794	250u Tape & Reel	VT1115SF
VT1115SFCX				2.5ku Tape & Reel	
VT1125SFCR	25A Smart Slave™	CSP-69	ES AP-0760	250u Tape & Reel	VT1125SF
VT1125SFCX				2.5ku Tape & Reel	
VT1135SFCR	30A Smart Slave™	CSP-41	ES AP-0804	250u Tape & Reel	VT1135SF
VT1135SFCX				2.5ku Tape & Reel	

ABSOLUTE MAXIMUM RATINGS (SEE NOTE 1)

Supply Voltage (12V) ..... -0.3V to 16V
Supply & Input Pin Voltages (3.3V) ..... -0.3V to 4V
VT1165M SC and SD Pin Voltages ..... -0.3V to 7V
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Peak Reflow Temperature Eutectic ..... 245°C
Peak Reflow Temperature Lead-Free ..... 260°C

THERMAL RATINGS

Θ_{JC} Max (QFN-40) ..... 14.8°C/W
Θ_{JC} Max (CSP-41) ..... 0.6°C/W
Θ_{JC} Max (CSP-52) ..... 0.5°C/W
Θ_{JC} Max (CSP-53) ..... 0.5°C/W
Θ_{JC} Max (CSP-69) ..... 0.3°C/W
Θ_{JA}[2] Typ (CSP-41) ..... 21°C/W
Θ_{JA}[2] Typ (CSP-52) ..... 19°C/W
Θ_{JA}[2] Typ (CSP-53) ..... 19°C/W
Θ_{JA}[2] Typ (CSP-69) ..... 17°C/W

OPERATING RATINGS

Input 3.3V Voltages (Master &Slave) ..... 2.97V to 3.63V
Slave 12V Supply ..... 10.8V to 13.2V
Junction Temperature (T_J) Master & Slave ..... 0°C to 125°C
Frequency (Fsw) ..... 500kHz to 1.3MHz
Design Guideline for Maximum Slave DC Output Current (VT1105S, VT1125S) 25A
Design Guideline for Maximum Slave DC Output Current (VT1115S, VT1135S) 30A
Electrical DC Current Limit Per Slave Assuming No Thermal Limitations (VT1105S, VT1125S) 30A
Electrical DC Current Limit Per Slave Assuming No Thermal Limitations (VT1115S, VT1135S) 36A
Peak Instantaneous Slave Current (VT1105S, VT1125S) 56A
Peak Instantaneous Slave Current (VT1115S, VT1135S) 63A

NOTE 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2: Data taken with Volterra's evaluation kit. Assumes no heatsink and 200LFM of airflow.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ELECTRICAL CHARACTERISTICS

V_{DD-M} = V_{DD-S} = V_{CC-S} = 3.3V ±10%, V_{DD-H} = 10.8V to 13.2V unless otherwise specified. The ∗ symbol denotes specifications which apply over the following junction temperature ranges: $T_{J-SLAVE}$ = 0 to 125°C and $T_{J-MASTER}$ = 0 to 100°C, otherwise specifications are for T_J = 25°C. The # denotes parameters that are programmable.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
Supply Voltages, V_{DD} and V_{CC}								
V_{DD-M}	Supply Voltage Range (Master)			∗	2.97	3.3	3.63	V
V_{DD-S}, V_{CC-S}	Supply Voltage Range (Slave 3.3V)			∗	2.97	3.3	3.63	V
V_{DDH}	Supply Voltage Range (Slave 12V)			∗	10.8	12.0	13.2	V
I_{DD-M}	Supply Current (Master)	PWM				13		mA
		Shutdown, OE = 0				10		mA
I_{DD-S}, I_{CC-S}	Supply Current (Slave 3.3V)	VT1105S	PWM			45		mA
			Shutdown			20		mA
		VT1115S	PWM			25		mA
			Shutdown			20		mA
		VT1125S	PWM			55		mA
			Shutdown			20		mA
		VT1135S	PWM			25		mA
			Shutdown			20		mA
I_{DDH}	Quiescent Supply Current (Slave 12V)	VT1105S				1		mA
		VT1115S				2		mA
		VT1125S				1		mA
		VT1135S				2		mA
Output Voltage and DC Accuracy								
V_{OUT}	Output Voltage Range	VR 9 VID Code		∗	1.100		1.850	V
		VR 10.X VID Code		∗	0.8375		1.6000	V
		Opteron™ VID Code		∗	0.800		1.550	V
$ERROR_{MASTER-REF}$	DC Setpoint Accuracy (including voltage reference and master amplifier)	Full VID Range: The Greater of		∗	-6 or -0.8		+9 or +0.8	mV %
Regulation and System Specifications (Specified by design, tested using circuits in Figures 5 & 6)								
ΔV_{OUT}	Line Regulation	V_{DDH} = 12V ±10%				5		mV
	Output Ripple					10		mV
SR_{OUT}	Output Slew Rate					1000		A/µs
$T_{TURN-ON}$	Turn-On Response Time. Time to V_{OUT} > 95% of Final Value.	From V_{DD-M} > UVLO (8 slaves, I_{MAX} = 28A, 800kHz, 300µF/slave, C_{NOM} = 6.8nF). Includes configuration time.			4.6		5.4	ms
		From OE Positive Edge (8 slaves, I_{MAX} = 28A, 800kHz, 300µF/slave, C_{NOM} = 6.8nF)			0	100	200	µs
$V_{OVERSHOOT}$	Turn-On Overshoot	Built in Soft Start					0	%
$V_{UNDERSHOOT}$	Turn-Off Undershoot	30Ω Load				0		mV
$CMRR_{SENSE}$	Common-Mode Rejection Ratio of Differential Sense					40		dB
I_{SENSE}	SENSE Pin Currents	SENSE+ Sinking, SENSE- Sourcing				60	100	µA

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
Regulation and System Specifications (Specified by design, tested using circuits in Figures 5 & 6) (CONTINUED)								
Eff	Efficiency (Measured at Inductor), 6 Phases	VT1105S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			80		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			83		%
		VT1115S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			83		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			85		%
		VT1125S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			83		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			85		%
		VT1135S	VID = 1.4V, V_{OUT} = 1.197V, I_{OUT} = 150A			80		%
			VID = 1.4V, V_{OUT} = 1.233V, I_{OUT} = 130A			83		%
Slave Scalability and Peak Current Limit								
N_{SLAVE}	Maximum Total Number of Slaves						8	
I_{LIM-SL}	Peak Current Limit Per Slave	VT1105S, VT1125S					56	A
		VT1115S, VT1135S					63	A
$I_{MAX-SL(DC)}$	DC Maximum Output Current Per Slave	VT1105S, VT1125S		#			25	A
		VT1115S, VT1135S		#			30	A
-	Slave DC Current Accuracy Relative to Full Load	VT1105S, VT1115S, VT1125S, VT1135S		*		5	7	%
MASTER DIGITAL CONTROL AND STATUS PINS								
Data (SD) and Clock (SC) Pins (SMBus High Power Specification Version 2.0)								
V_{IL}	Input Low Voltage						0.8	V
V_{IH}	Input High Voltage				2.1			V
V_{OL}	Output Low Voltage (SD)	@ I_{SINK} = 2.5mA					0.4	V
OE and VID[0:5] Pins for VR 9, Opteron™ and Programmable VID Mode								
V_{IL}	Input Low Voltage						0.8	V
V_{IH}	Input High Voltage				1.7			V
OE and VID[0:5] Pins for VR 10.X								
V_{IL}	Input Low Voltage						0.4	V
V_{IH}	Input High Voltage				0.8			V

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

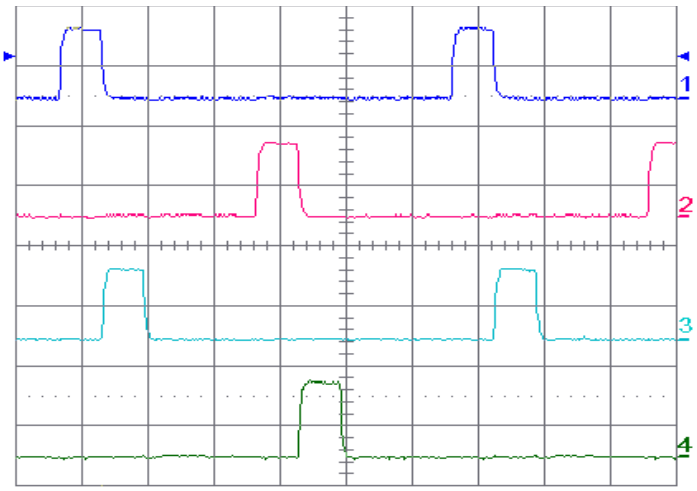
ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PWRGD and FAULTB Pins							
-	PWRGD DC Threshold Error			-40		+40	mV
-	Delay from V_{OUT} to PWRGD	After Startup		8		20	µs
-	PWRGD Lockout after OE Goes High (UVLO & OVLO Low)			1.6	2.0	2.4	ms
V_{OL}	Output Low Voltage	@ I_{SINK} = 2.5mA				0.4	V
OVP							
-	DC Threshold Error			-40		+40	mV
-	OVP Lockout OE Goes High (UVLO & OVLO Low)			1.6	2.0	2.4	ms
OCP							
I_{OCP}	OCP Inception Point	Refer to Table 1C (I_{OCP} for all I_{MAX} settings)					
I_{SC-PK}	Peak Current for Short Circuit	Refer to Table 1D (I_{SC-PK} for all I_{MAX} settings)					
-	Hiccup Period			46	50	54	ms
-	Hiccup Duty Cycle				10		%
-	Latch Off Delay			4.5	5.0	5.5	ms
Undervoltage and Overvoltage Lockout 12V Supply							
IN_UVLO_{RE}	12V UVLO Reference Voltage Rising Edge			1.262	1.301	1.338	V
IN_UVLO_{FE}	12V UVLO Reference Voltage Falling Edge			1.191	1.238	1.269	V
$IN\_UVLO_{HYSTERESIS}$	UVLO Hysteresis			45	67		mV
IN_OVLO_{RE}	12V OVLO Reference Voltage Rising Edge			1.262	1.305	1.338	V
IN_OVLO_{FE}	12V OVLO Reference Voltage Falling Edge			1.191	1.236	1.269	V
$IN\_OVLO_{HYSTERESIS}$	OVLO Hysteresis			45	67		mV
t_{UVLO}, t_{OVLO}	12V UVLO and OVLO Response Time	Including time to shut down the slave			7.25		µs
$t_{UVLO-REC}$, $t_{OVLO-REC}$	12V UVLO and OVLO Recovery Time	Not including soft-start delay			7.25		µs
Undervoltage Lockout 3.3V Supply (Master-Internal)							
3_3V_UVLO	3.3V Internal UVLO	Rising Threshold				2.85	V
		Falling Threshold		2.69			V
$3\_3V\_UVLO_{HYSTERESIS}$	Hysteresis				100		mV
Slave FAULTB Ball (VT1115S, VT1125S, VT1135S)							
$V_{OL-FAULTB}$	FAULTB Output Low Voltage	With 4.7kΩ external pull-up			0.1	0.4	V
$R_{PULLDOWN-FAULTB}$	FAULTB Pull-Down Resistance				50	200	Ω
SMBus Reporting							
-	SMBus Current Reporting Accuracy			-10		+10	% of I_{MAX}
-	SMBus Temperature Reporting Accuracy				±2		°C
SPHASE							
-	SPHASE Clock Period Tolerance	Including 1% Resistor Tolerance	*	-6		+6	%

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS

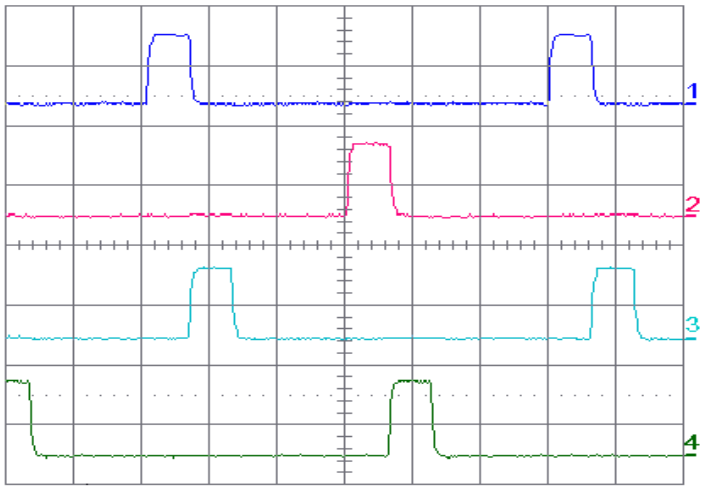
Output Switching Nodes - Eight Slaves Switching Out-of-Phase (Slaves 1-4)



Time/Div: 200ns

Conditions: V_{OUT} = 1.2V, No Load
1: Vx Switching Node for Slave #1 (10V/div)
2: Vx Switching Node for Slave #2 (10V/div)
3: Vx Switching Node for Slave #3 (10V/div)
4: Vx Switching Node for Slave #4 (10V/div)
(Triggered From Slave #1)

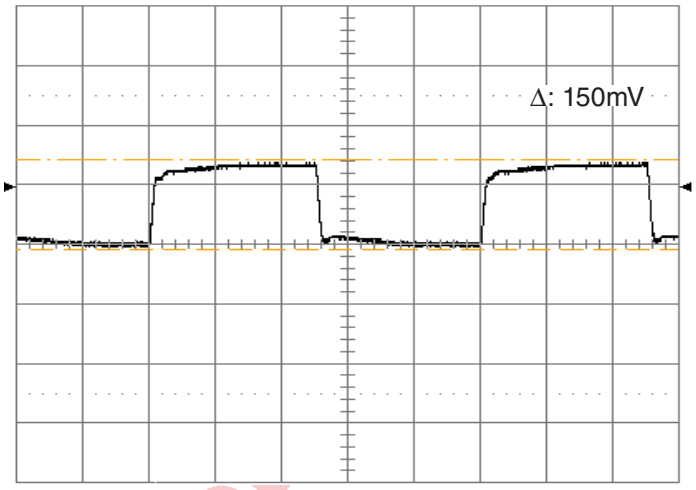
Output Switching Nodes - Eight Slaves Switching Out-of-Phase (Slaves 5-8)



Time/Div: 200ns

Conditions: V_{OUT} = 1.2V, No Load
1: Vx Switching Node for Slave #5 (10V/div)
2: Vx Switching Node for Slave #6 (10V/div)
3: Vx Switching Node for Slave #7 (10V/div)
4: Vx Switching Node for Slave #8 (10V/div)
(Triggered From Slave #1)

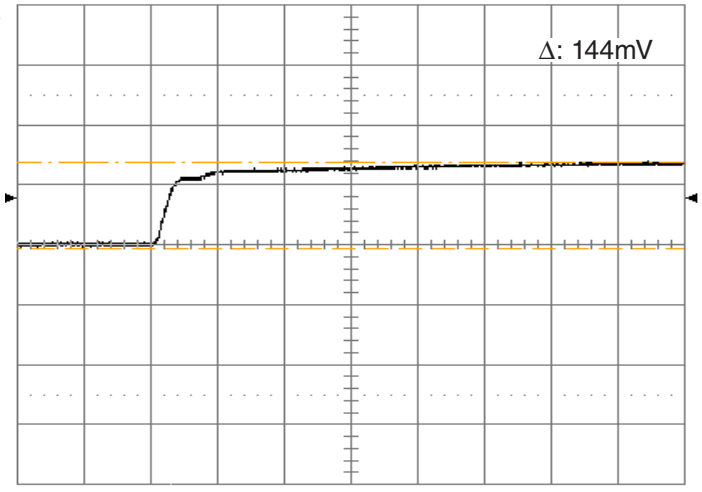
Load Transient Response - 8 Slave VT1105S System



Time/Div: 20µs

Conditions: V_{OUT} = 1.2V, No Load
I_{OUT} = 100A-0A Load Step
Slew Rate > 1000A/µs
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

Output Voltage Overshoot - 8 Slave VT1105S System



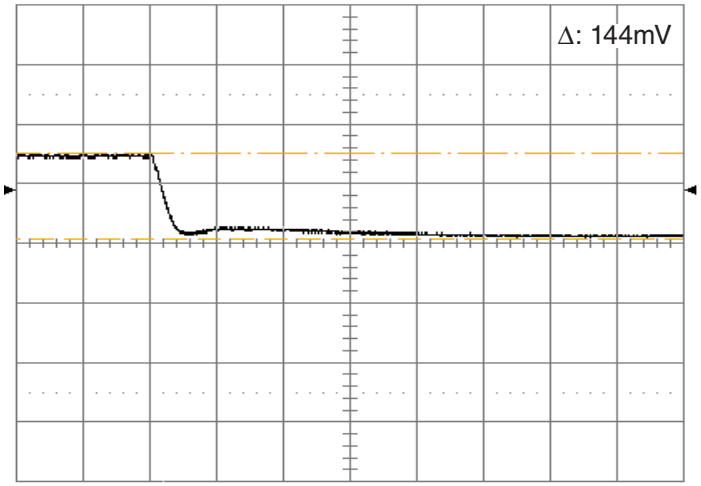
Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 100A-0A Load Step
Loadline = 1.28mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

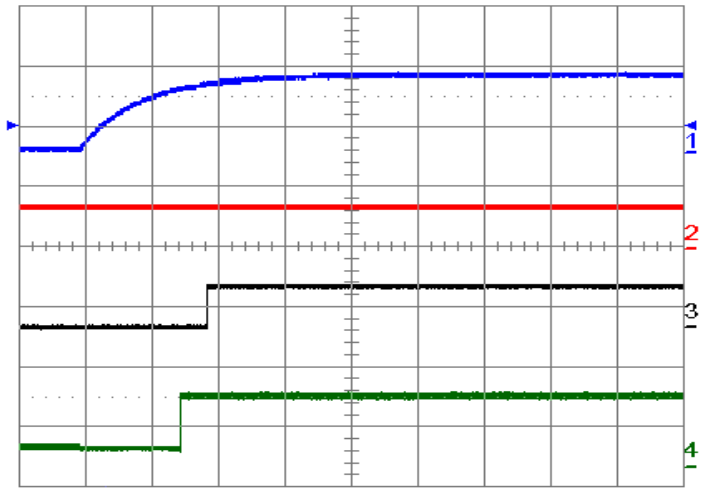
Output Voltage Undershoot - 8 Slave VT1105S System



Time/Div: 5µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 0-100A Load Step
Loadline = 1.28mΩ
C_{OUT} = 58 x 22µF
1: Output Voltage (100mV/div)

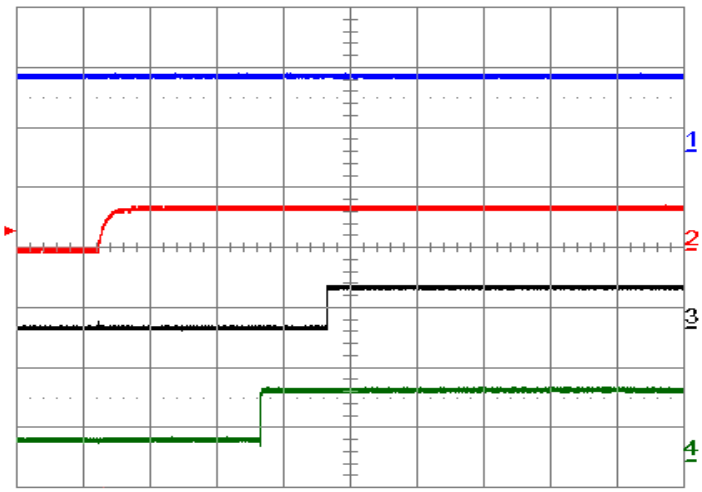
Startup Response References 12V Supply



Time/Div: 5ms

Conditions: V_{OUT} = 1.2V, No Load
1: 12V Input Voltage (10V/div)
2: 3.3V Input Voltage (5V/div)
3: PWRGD Signal (5V/div)
4: Output Voltage (1V/div)

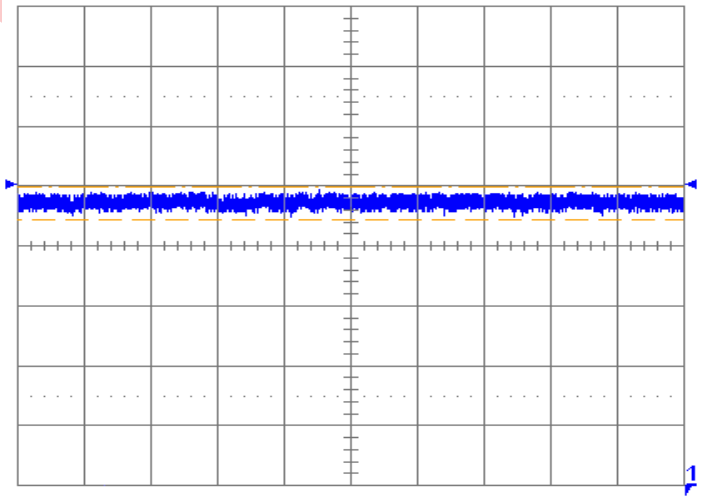
Startup Response References 3.3V Supply



Time/Div: 2ms

Conditions: V_{OUT} = 1.2V, No Load
1: 12V Input Voltage (10V/div)
2: 3.3V Input Voltage (5V/div)
3: PWRGD Signal (5V/div)
4: Output Voltage (1V/div)

Output Ripple - 8 Slave VT1105S System



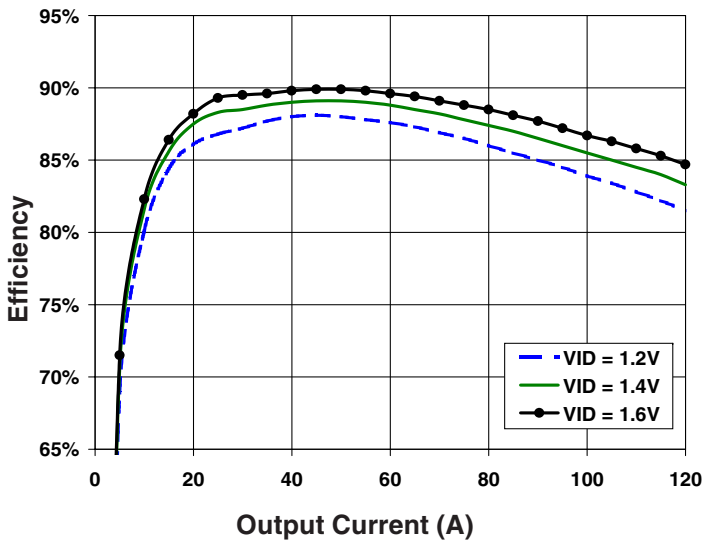
Time/Div: 20µs

Conditions: V_{OUT} = 1.2V
I_{OUT} = 160A
C_{OUT} = 58 x 22µF
1: Output Voltage (20mV/div)
25MHz BWL
Measured @ Output Capacitor

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

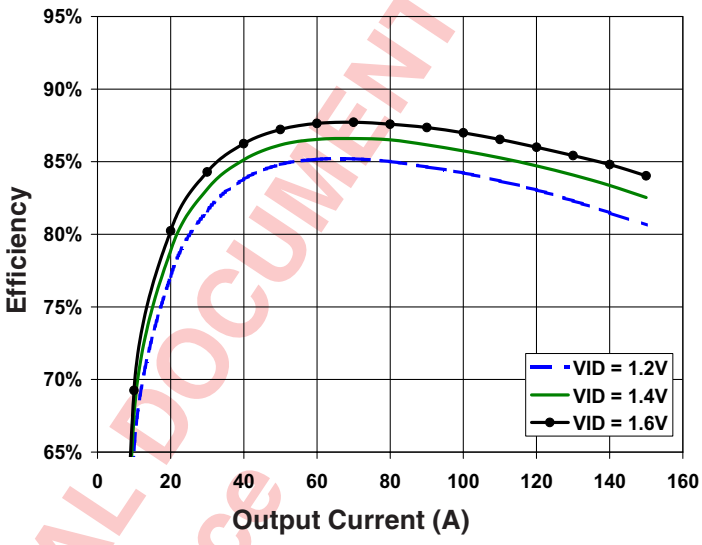
TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

System Efficiency - 5 VT1105S Slaves



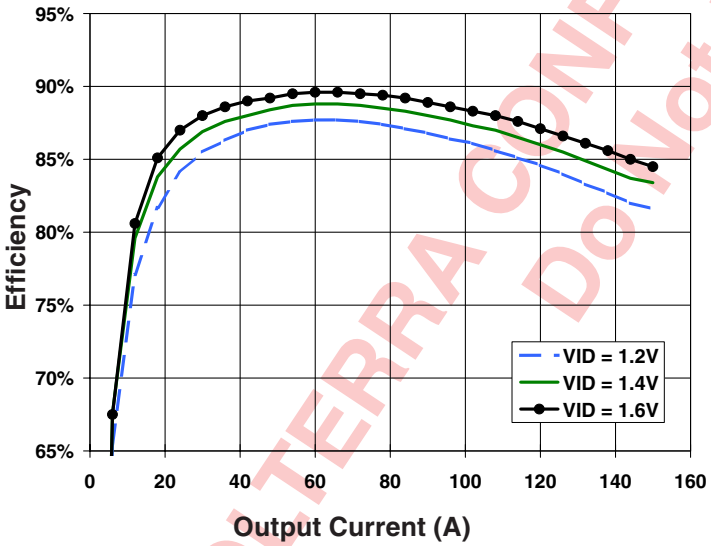
Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 804kHz
T_A = 25°C
Loadline (@ V_{SENSE}) = 1.25mΩ
V_{OUT} Measured @ Inductor

Typical System Efficiency - 5 VT1115S Slaves



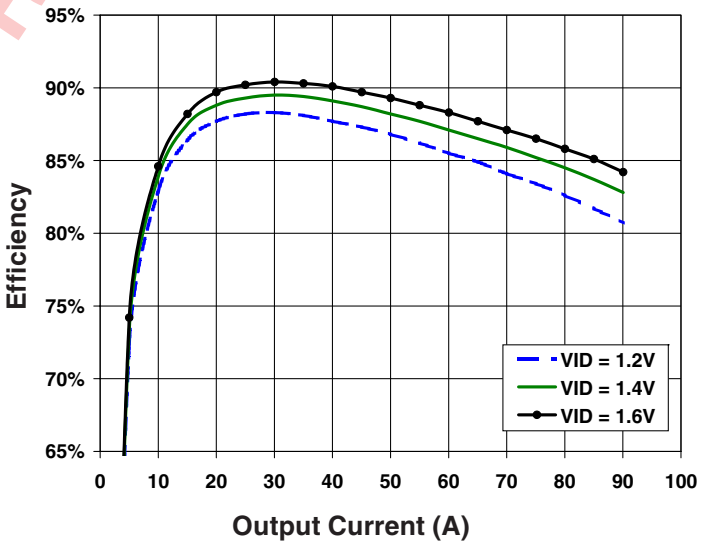
Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 800kHz
T_A = 25°C
Loadline (@ V_{SENSE}) = 1.25mΩ
V_{OUT} Measured @ Inductor

Typical System Efficiency - 6 VT1125S Slaves



Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 800kHz
T_A = 25°C
Loadline (@ V_{SENSE}) = 1.2mΩ
V_{OUT} Measured @ Inductor

Typical System Efficiency - 3 VT1135S Slaves

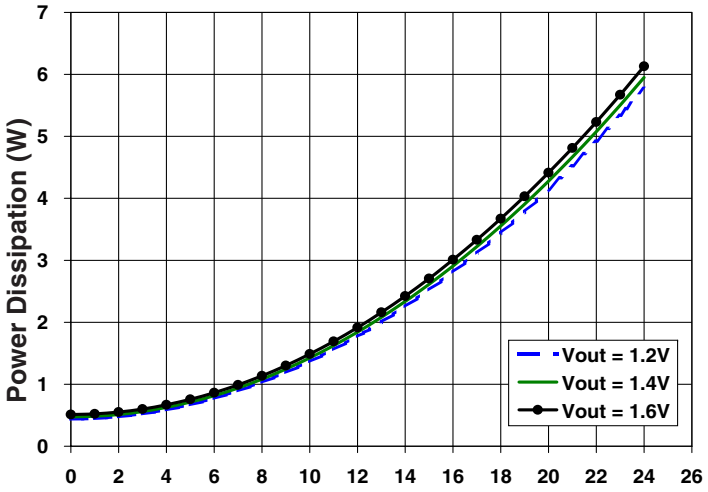


Conditions: V_{IN} = 12V
L_{OUT} = 100nH
Fsw = 800kHz
T_A = 25°C
System Loadline = 1.4mΩ
V_{OUT} Measured @ Inductor

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

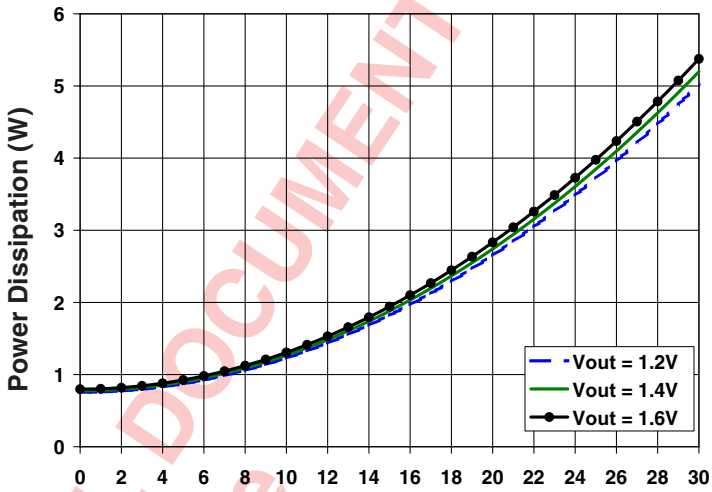
TYPICAL OPERATING CHARACTERISTICS (CONTINUED)

Estimated Power Dissipation - 1 VT1105S Slave



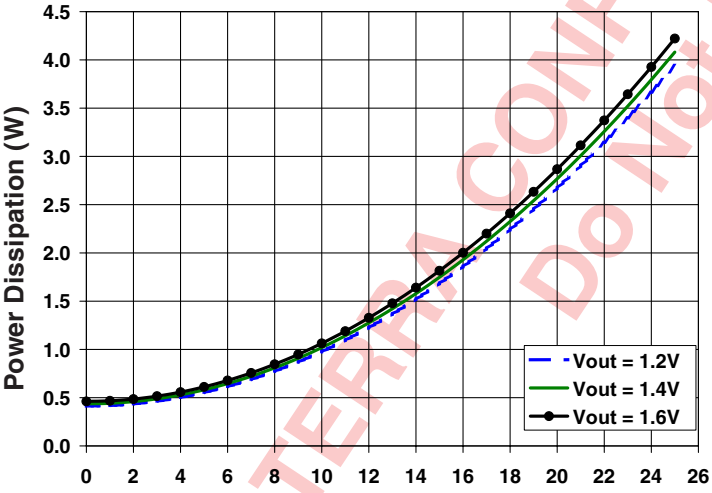
Conditions: V_{IN} = 1.2V
L_{OUT} = 120nH
Fsw = 850kHz
T_J = 100°C

Estimated Power Dissipation - 1 VT1115S Slave



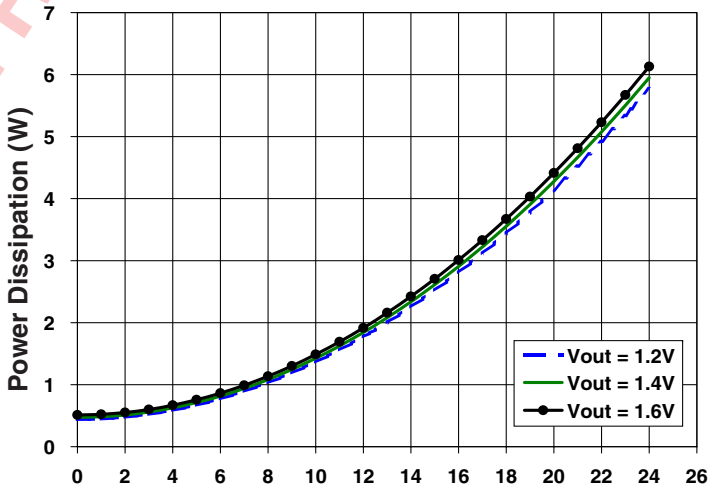
Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 850kHz
T_J = 100°C

Estimated Power Dissipation - 1 VT1125S Slave



Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 850kHz
T_J = 100°C

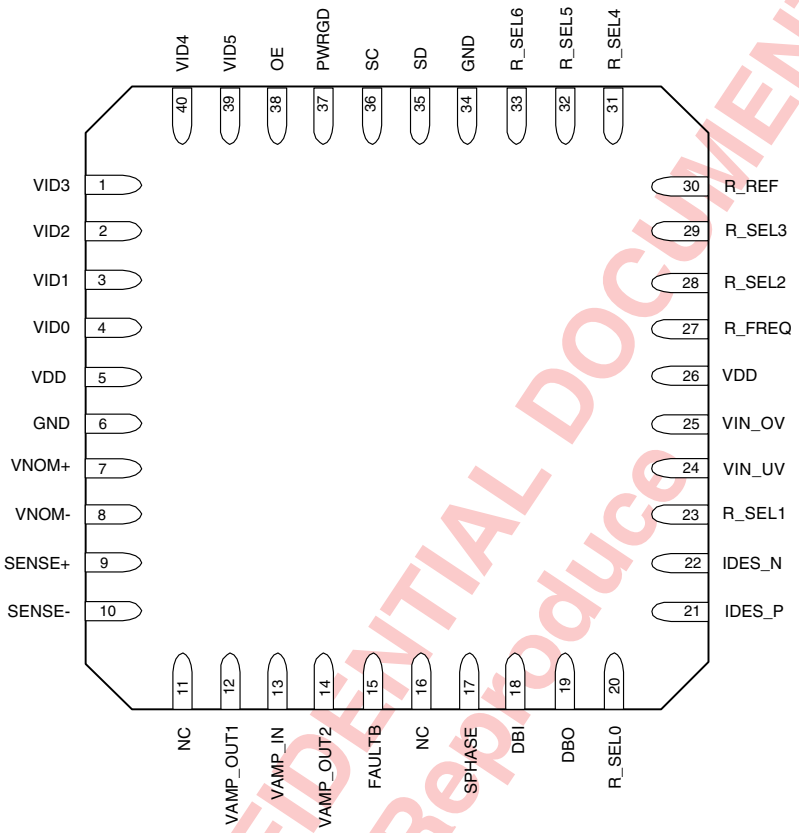
Estimated Power Dissipation - 1 VT1135S Slave



Conditions: V_{IN} = 12V
L_{OUT} = 120nH
Fsw = 850kHz
T_J = 100°C

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1165M (QFN-40) PINOUT



PIN INFORMATION FOR MASTER CONTROLLER

VID[5:0] (Pins 1-4, 39, 40): Output voltage identification code.

VDD (Pins 5, 26): 3.3V power.

GND (Pins 6, 34): Ground.

VNOM+, VNOM- (Pins 7, 8): DAC output used as the regulation reference. The no-load output voltage is equal to this reference. See the Output Voltage Programming section for additional design information.

SENSE+ (Pin 9): Positive remote sense.

SENSE- (Pin 10): Negative remote sense.

NC (Pin 11, 16): No connect.

VAMP_OUT1 (Pin 12): Sense amplifier output.

VAMP_IN (Pin 13): Error amplifier inverting input.

VAMP_OUT2 (Pin 14): Error amplifier output.

FAULTB (Pin 15): Active low fault condition flag. This open drain output should be externally pulled high with a resistor.

SPHASE (Pin 17): Slave phase clock output. This pin provides a switching frequency reference clock signal to each slave in the system. It should be connected to each slave's SPHASE input.

DBI (Pin 18): Digital control bus input.

DBO (Pin 19): Digital control bus output.

R_SEL[6:0] (Pins 20, 23, 28, 29, 31-33): System configuration resistors. (Programmable features detailed in Table 5.)

IDES_P (Pin 21): Idesired command (+).

IDES_N (Pin 22): Idesired command (-).

VIN_UV (Pin 24): Scaled version of slave VDDH voltage for undervoltage shutdown. This pin is used to program the input undervoltage lockout threshold for the slave VDDH supply. See the Undervoltage and Overvoltage Programming and Protection section for additional design information.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VIN_OV (Pin 25): Scaled version of slave VDDH voltage used for overvoltage shutdown. This pin is used to program the input overvoltage lockout threshold for the slave VDDH supply. See the Undervoltage and Overvoltage Programming and Protection section for additional design information.

R_FREQ (Pin 27): Resistor used to program switching frequency.

R_REF (Pin 30): Reference resistor used to calibrate R_SEL.

SD (Pin 35): Serial data pin for SMBus interface. See the SMBus Communication with the VT1165M section for additional design information. When not in use, this pin should be connected to VDD.

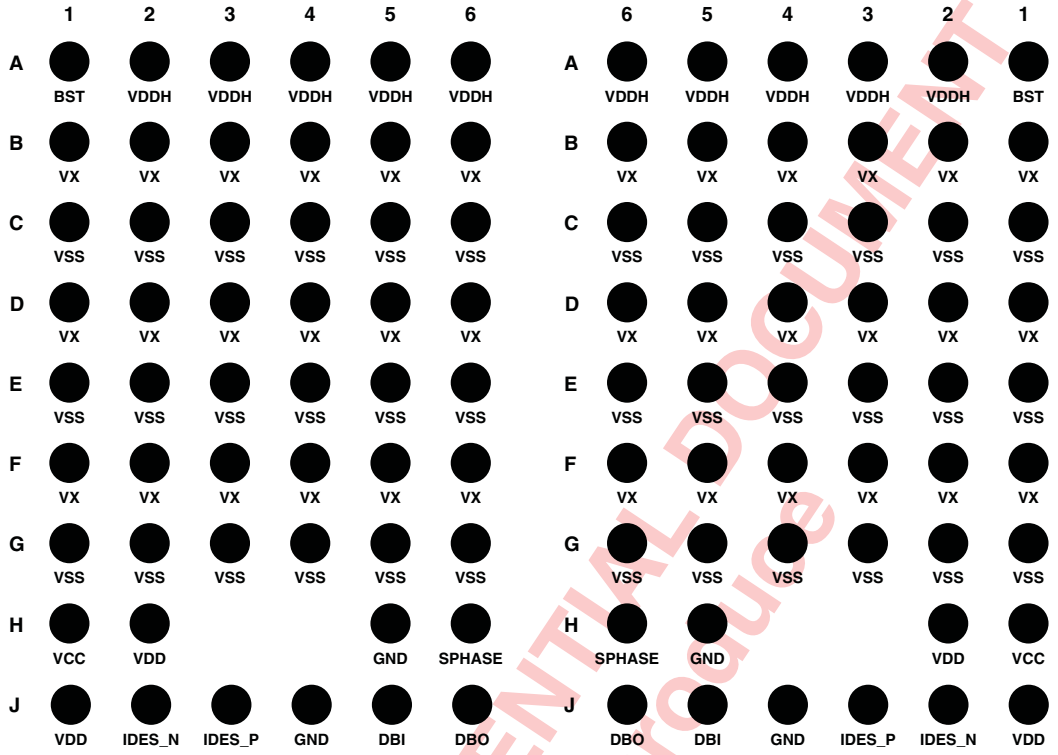
SC (Pin 36): Serial clock pin for SMBus interface. See the SMBus Communication with the VT1165M section for additional design information. When not in use, this pin should be connected to VDD.

PWRGD (Pin 37): Power good output pin. This pin indicates whether the output voltage is within regulation. This open-drain output should be externally pulled HIGH with a resistor. See the Power Good and Undervoltage and Overvoltage Programming and Protection sections for additional design information.

OE (Pin 38): Output enable input pin. When this pin is HIGH, the output voltage is enabled. When this pin is LOW, the output voltage is disabled.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1105S (CSP-52) PINOUT



PIN INFORMATION FOR VT1105S SMART SLAVE™

BST (Ball A1): Bootstrap supply for high side drivers.

VDDH (Balls A2-A6): 12V input supply voltage node. These balls connect to the 12V input power supply source.

VX (Balls B1-B6, D1-D6, F1-F6): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls C1-C6, E1-E6, G1-G6): Power FETs ground node. These balls connect directly to the ground plane.

VCC (Ball H1): 3.3V supply for low side drivers.

VDD (Balls H2, J1): 3.3V supply for control circuits.

GND (Balls H5, J4): Ground for control circuits.

SPHASE (Ball H6): SPHASE clock input from VT1165M master controller.

IDES_N (Ball J2): Negative input side of differential desired current signal.

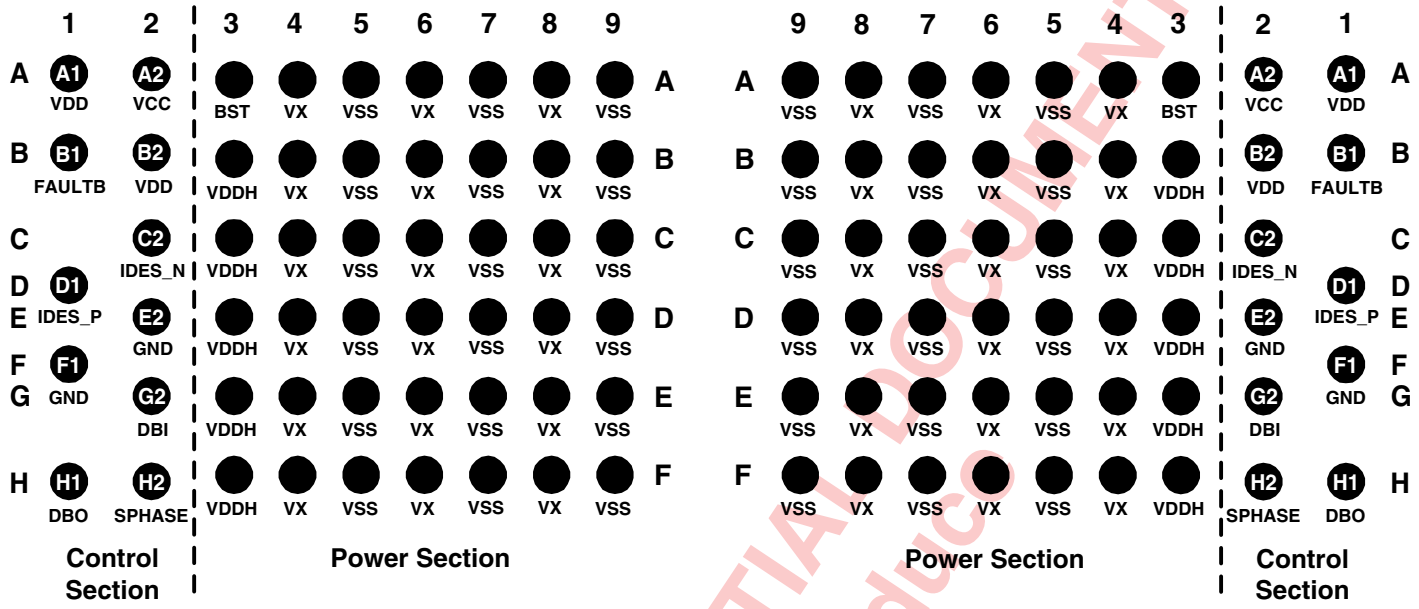
IDES_P (Ball J3): Positive input side of differential desired current signal.

DBI (Ball J5): Digital control bus input.

DBO (Ball J6): Digital control bus output.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1115S (CSP-53) PINOUT



PIN INFORMATION FOR VT1115S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-F4, A6-F6, A8-F8): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-F5, A7-F7, A9-F9): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low. This open-drain output should be externally pulled high with a resistor.

VDDH (Balls B3-F3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

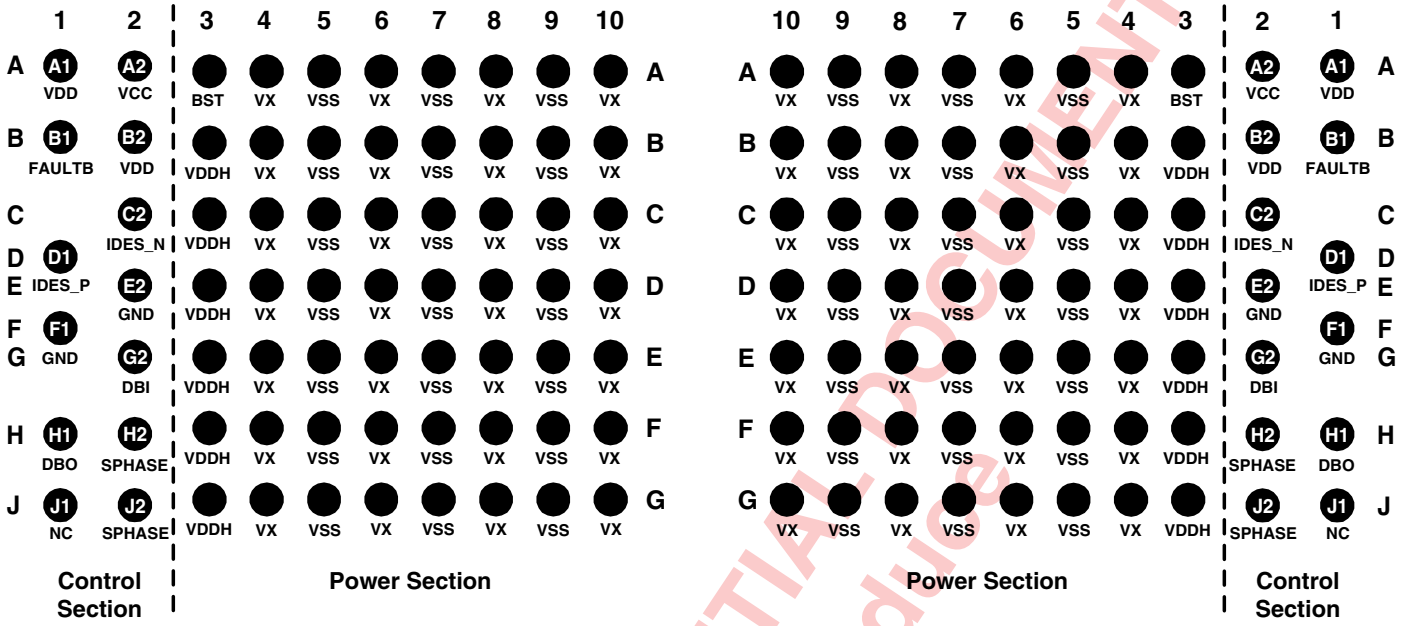
DBI (Ball G2): Digital control bus input.

DBO (Ball H1): Digital control bus output.

SPHASE (Ball H2): SPHASE clock input from VT1165M master controller. A 1kΩ resistor is recommended in series with each slave's SPHASE line.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1125S (CSP-69) PINOUT



PIN INFORMATION FOR VT1125S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-G4, A6-G6, A8-G8, A10-G10): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-G5, A7-G7, A9-G9): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low. This open-drain output should be externally pulled high with a resistor.

VDDH (Balls B3-G3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

DBI (Ball G2): Digital control bus input.

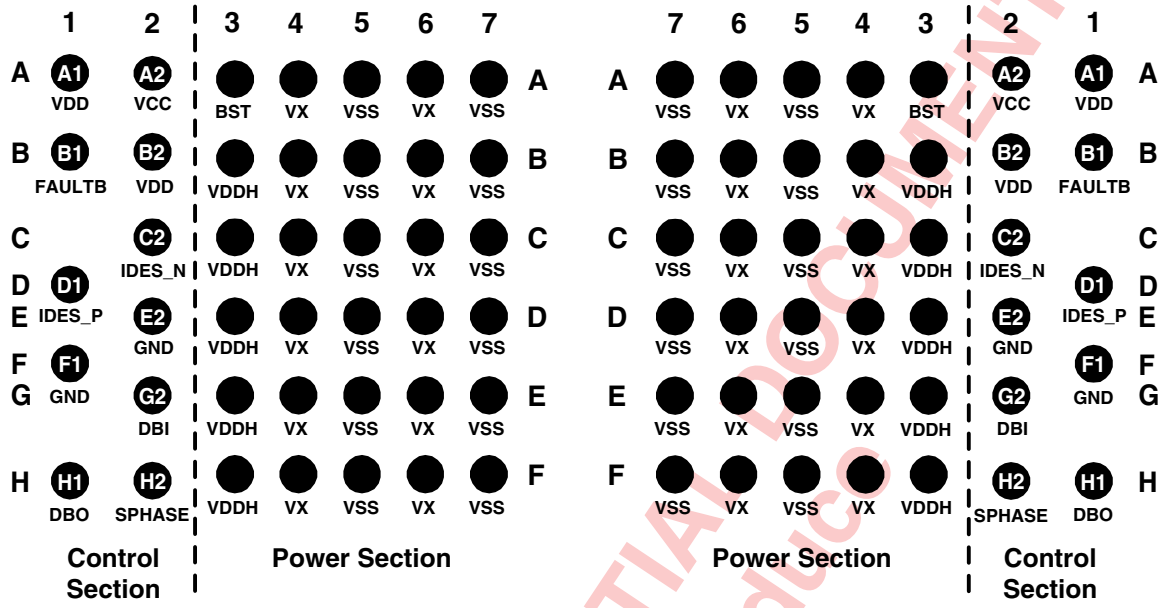
DBO (Ball H1): Digital control bus output.

SPHASE (Balls H2, J2): SPHASE clock input from VT1165M master controller. A 1kΩ resistor is recommended in series with each slave's SPHASE line.

NC (Ball J1): No connect.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

VT1135S (CSP-41) PINOUT



PIN INFORMATION FOR VT1135S SMART SLAVE™

VDD (Balls A1, B2): 3.3V supply for control circuits.

VCC (Ball A2): 3.3V supply for low side drivers.

BST (Ball A3): Bootstrap supply for high side drivers.

VX (Balls A4-F4, A6-F6): Switching node. These balls connect the switching node of the power devices to the output inductor.

VSS (Balls A5-F5, A7-F7): Power FETs ground node. These balls connect directly to the ground plane.

FAULTB (Ball B1): Fault signal. Active low. This open-drain output should be externally pulled high with a resistor.

VDDH (Balls B3-F3): 12V input supply voltage node. These balls connect to the 12V input power supply source.

IDES_N (Ball C2): Negative input side of differential desired current signal.

IDES_P (Ball D1): Positive input side of differential desired current signal.

GND (Balls E2, F1): Ground for control circuits.

DBI (Ball G2): Digital control bus input.

DBO (Ball H1): Digital control bus output.

SPHASE (Ball H2): SPHASE clock input from VT1165M master controller. A 1kΩ resistor is recommended in series with each slave's SPHASE line.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

REFERENCE DESIGNS

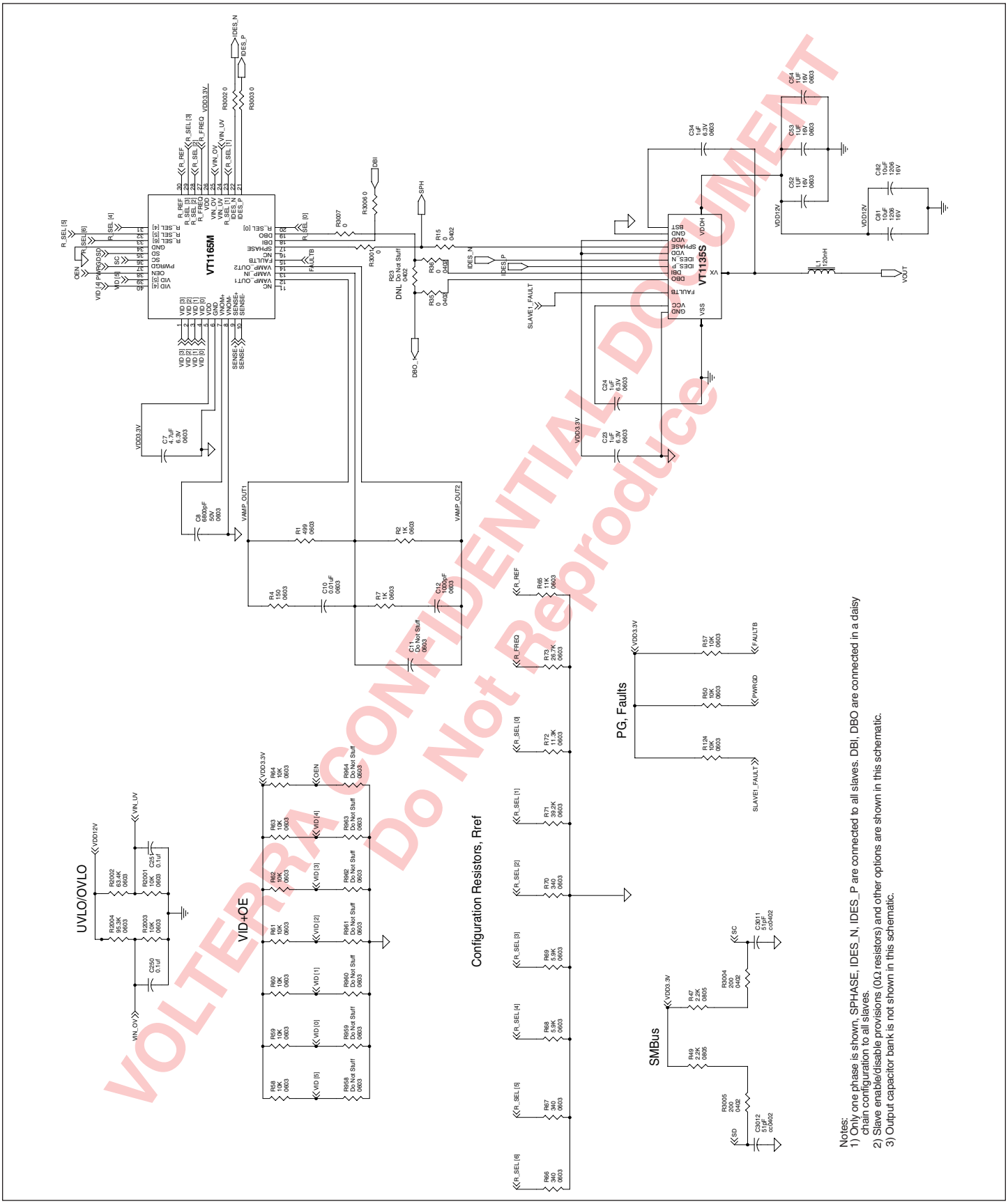


Figure 5. VT1165M/VT1135S Chipset Reference Design Schematic

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

REFERENCE DESIGNS (CONTINUED)

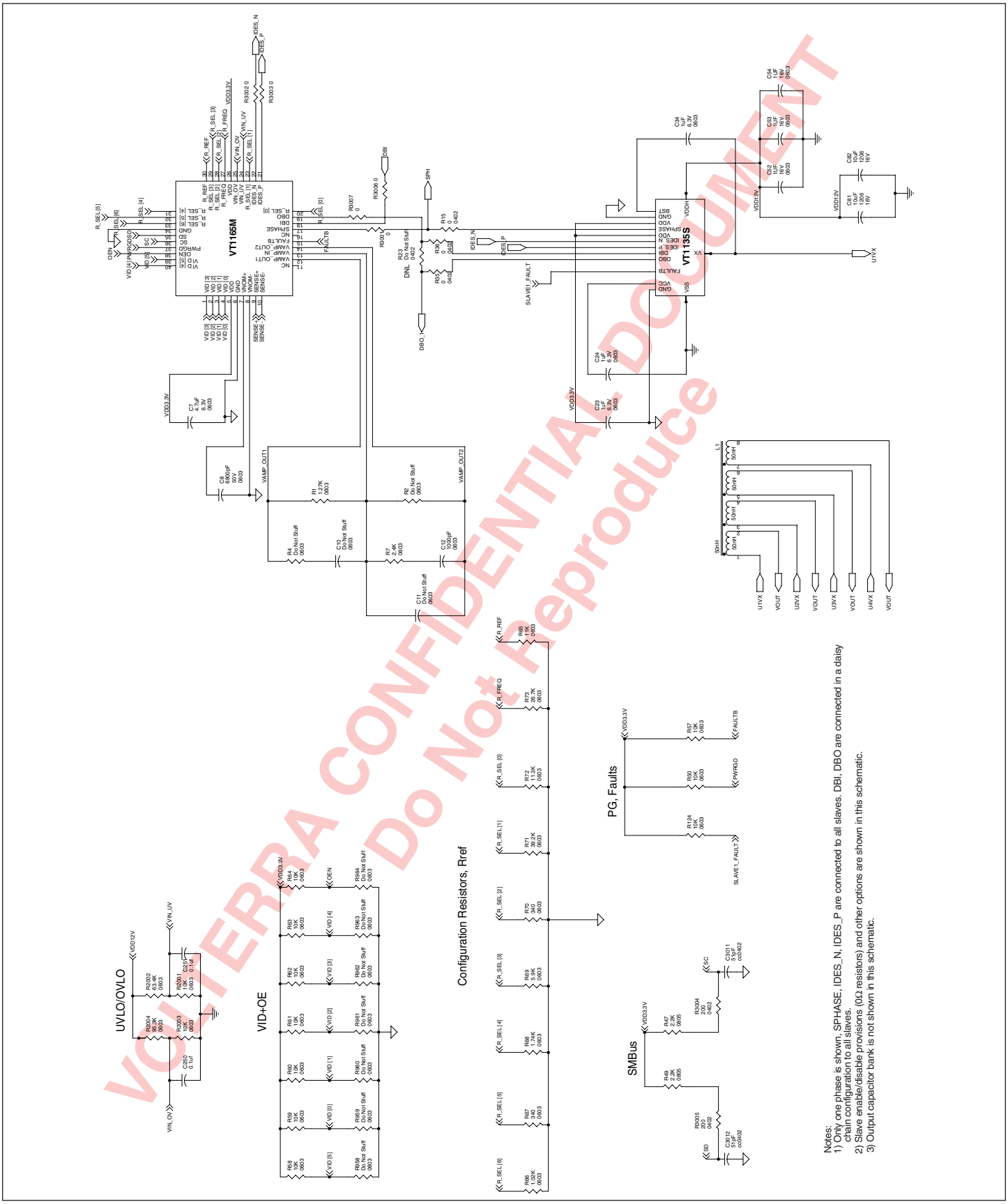
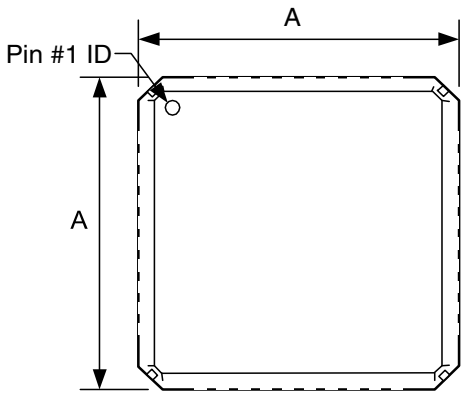


Figure 6. VT1165M/VT1135S Coupled Inductor Chipset Reference Design Schematic

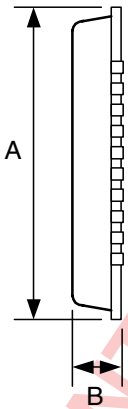
PACKAGE DIMENSIONS - VT1165M

VOLTERRA	Title: Package Outline - 40 Lead QFN	Doc No. ES AP-0906	Rev. 0
		Page 1 of 2	

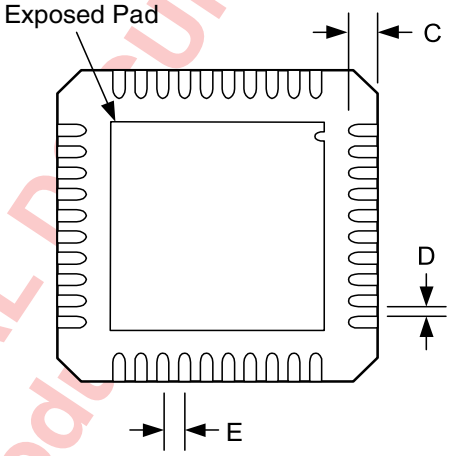
TOP VIEW



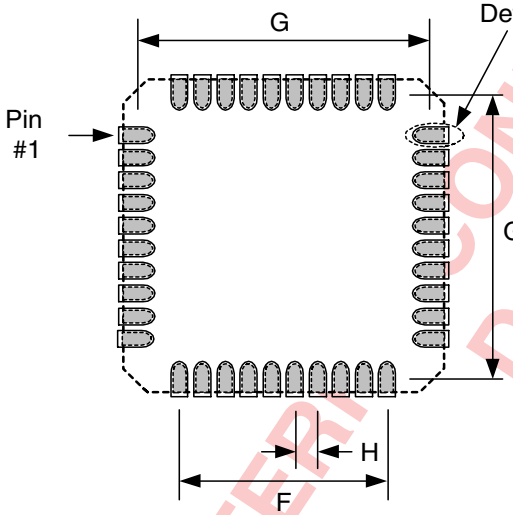
SIDE VIEW



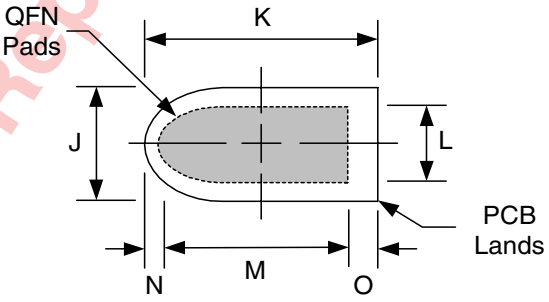
BOTTOM VIEW



RECOMMENDED LAND PATTERN



DETAIL A



DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
A	5.9000		6.1000	0.2323		0.2402
B	0.8000		0.9000	0.0315		0.0354
C	0.3000		0.5000	0.0118		0.0197
D	0.1800		0.3000	0.0071		0.0118
E		0.5000			0.0197	
F		4.5000			0.1772	
G		5.6000			0.2205	
H		0.5000			0.0197	
J		0.2800			0.0110	
K		0.6000			0.0236	
L	0.1800		0.3000	0.0071		0.0118
M	0.3000		0.5000	0.0118		0.0197
N	0.0500			0.0020		
O	0.1500			0.0059		

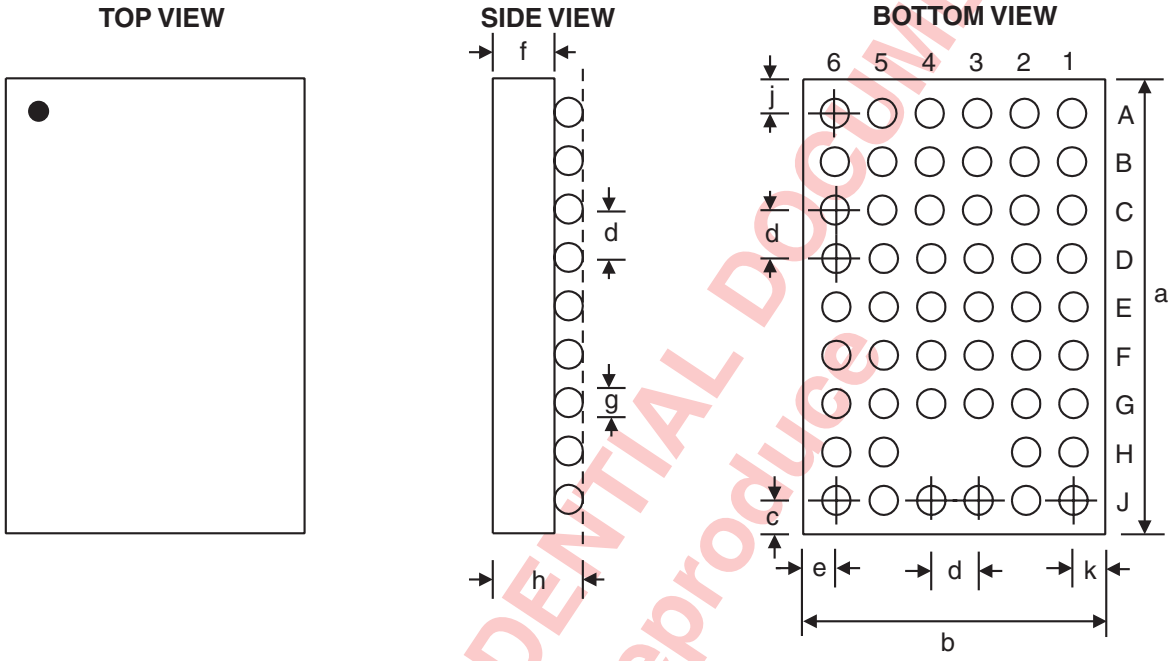
**Inches provided for reference only.*

Notes:
1. Drawings not to scale
2. Controlling dimensions are in millimeters

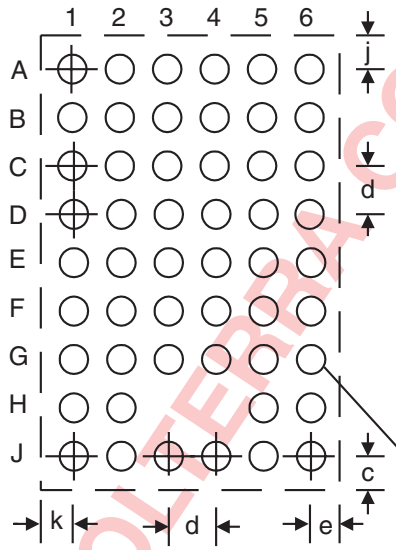
PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

PACKAGE DIMENSIONS - VT1105S

VOLTERRA	Title: Package Outline - 52 Ball CSP VSC1054 / VSC1200 / VT1105S	Doc No. ES AP-0588	Rev. 3
		Page 1 of 2	

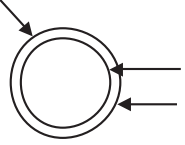


LAND PATTERN



DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	5.014		5.064	0.1974		0.1994
b	3.174		3.224	0.1250		0.1269
c		0.453			0.0178	
d		0.500			0.0197	
e		0.341			0.0134	
f	0.635		0.685	0.0250		0.0270
g		0.375			0.0148	
h		0.950			0.0374	
j		0.586			0.0231	
k		0.358			0.0141	

** Inches provided for reference only*



TYPICAL PAD DESIGN

0.280mm ±0.05mm PCB Solder Mask Opening

0.355mm Minimum PCB Pad Diameter

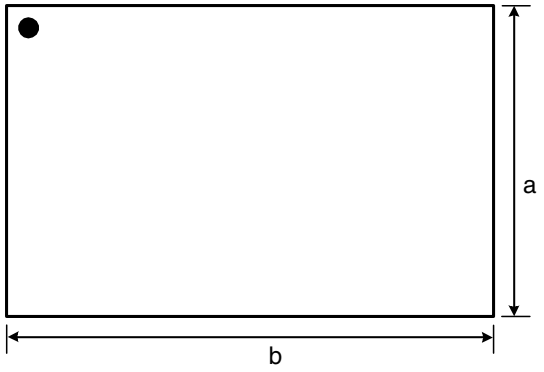
Notes

1. Drawing not to scale.
2. Controlling dimensions are in millimeters

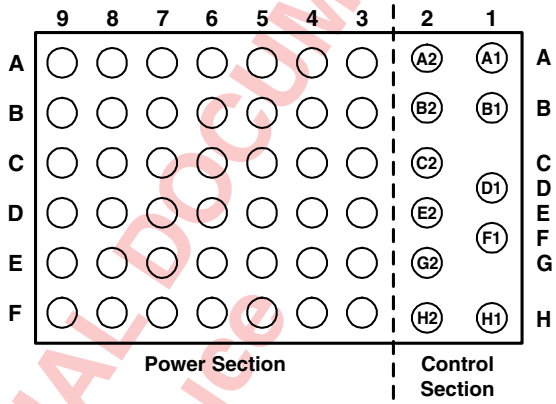
PACKAGE DIMENSIONS - VT1115S

VOLTERRA	Title: Package Outline - 53 Ball CSP VSC1088 / VT1115S	Doc No. ES AP-0794	Rev. 2
		Page 1 of 2	

TOP VIEW

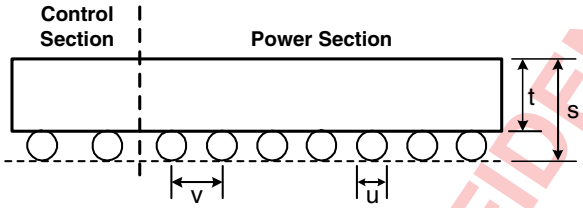


BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

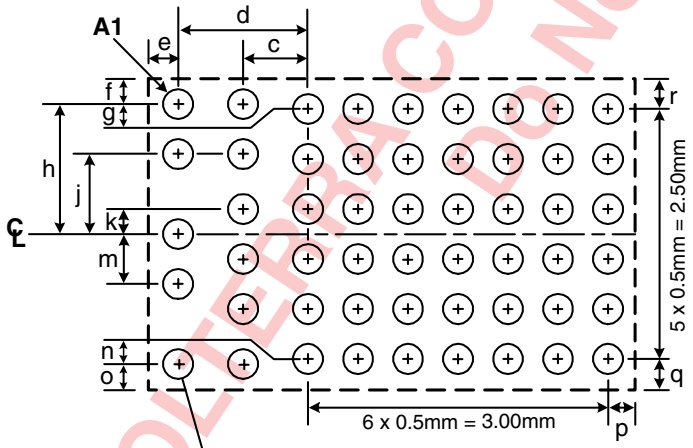
SIDE VIEW



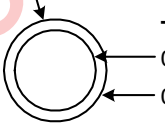
DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	3.173		3.223	0.1249		0.1269
b	5.003		5.053	0.1970		0.1989
c		0.650			0.0256	
d		1.300			0.0512	
e	0.426		0.451	0.0168		0.0177
f	0.284		0.309	0.0112		0.0121
g		0.075			0.0030	
h		1.325			0.0522	
j		0.825			0.0325	
k		0.250			0.0098	
m		0.500			0.0197	
n		0.075			0.0030	
o	0.239		0.264	0.0094		0.0104
p	0.278		0.303	0.0109		0.0119
q	0.314		0.339	0.0123		0.0133
r	0.359		0.384	0.0141		0.0151
s	0.915	0.930	0.945	0.0360	0.0366	0.0372
t	0.635	0.650	0.665	0.0250	0.0256	0.0262
u		0.375			0.0148	
v		0.500			0.0197	

Inches provided for reference only.

LAND PATTERN
(Ball Side Down)



TYPICAL PAD DESIGN



0.280 ±0.05mm PCB Solder Mask Opening

0.355mm Minimum PCB Pad Diameter

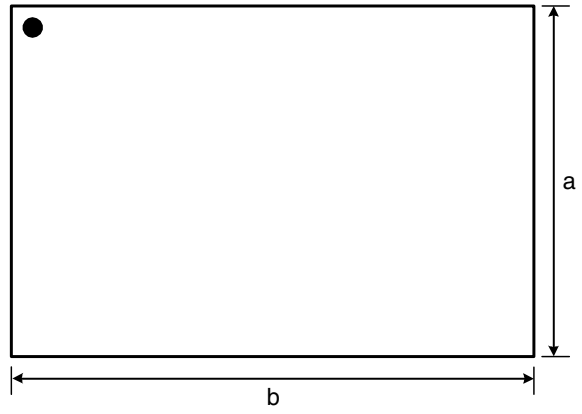
Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters.

PROGRAMMABLE OUTPUT, MULTIPHASE SWITCHING REGULATOR WITH SMBus

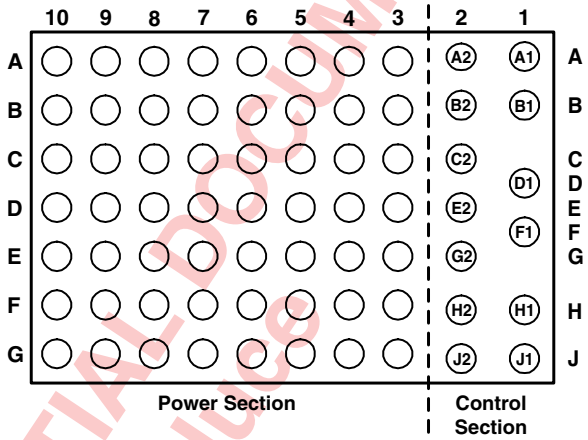
PACKAGE DIMENSIONS - VT1125S

VOLTERRA	Title: Package Outline - 69 Ball CSP VSC1075 / VT1125S	Doc No. ES AP-0760	Rev. 0
		Page 1 of 2	

TOP VIEW

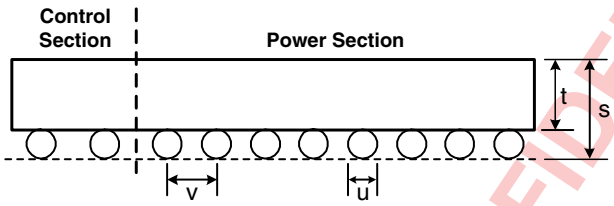


BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

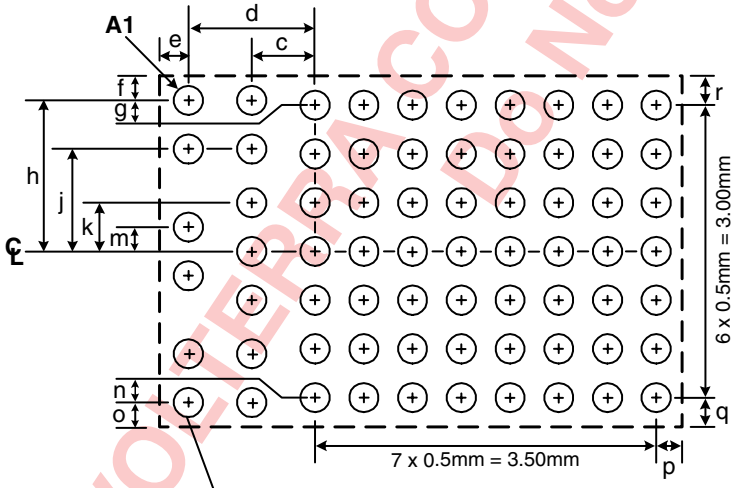
SIDE VIEW



DIM	MILLIMETERS MIN	TYP	MAX	INCHES* MIN	TYP	MAX
a	3.673		3.723	0.1446		0.1466
b	5.503		5.553	0.2167		0.2186
c		0.650			0.0256	
d		1.300			0.0512	
e	0.413		0.463	0.0163		0.0182
f	0.271		0.321	0.0107		0.0126
g		0.075			0.0030	
h		1.575			0.0620	
j		1.075			0.0423	
k		0.500			0.0197	
m		0.250			0.0098	
n		0.075			0.0030	
o	0.226		0.276	0.0089		0.0109
p	0.265		0.315	0.0104		0.0124
q	0.301		0.351	0.0119		0.0138
r	0.346		0.396	0.0136		0.0156
s		0.930			0.0366	
t		0.650			0.0256	
u		0.375			0.0148	
v		0.500			0.0197	

Inches provided for reference only.

LAND PATTERN
(Ball Side Down)



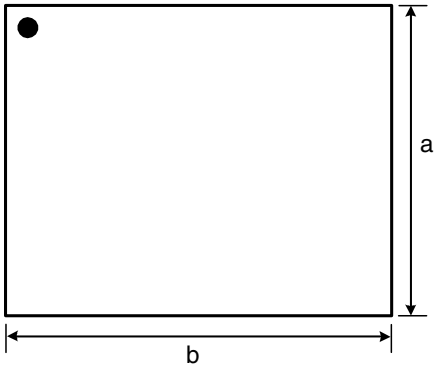
TYPICAL PAD DESIGN

Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters.

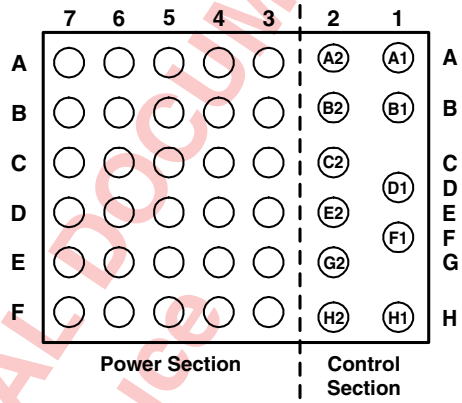
PACKAGE DIMENSIONS - VT1135S

VOLTERRA	Title: Package Outline - 41 Ball CSP VSC1099 / VT1135S	Doc No. ES AP-0804	Rev. 3
		Page 1 of 2	

TOP VIEW

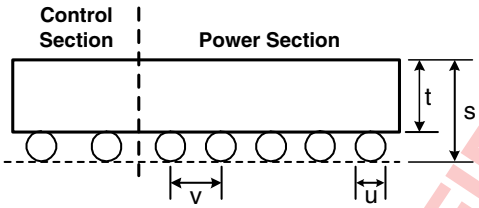


BOTTOM VIEW



Note: Rows & columns on the Control Section are NOT on a common grid with the Power Section. See Land Pattern for detailed dimensions.

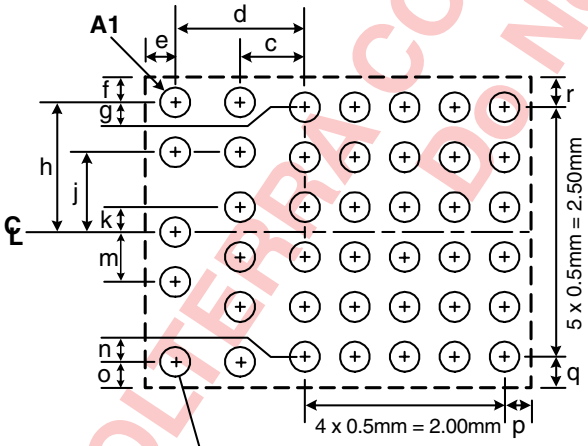
SIDE VIEW



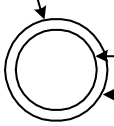
	MILLIMETERS			INCHES*		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
a	3.213		3.263	0.1265		0.1285
b	3.988		4.038	0.1570		0.1590
c		0.650			0.0256	
d		1.300			0.0512	
e	0.416		0.441	0.0164		0.0173
f	0.264		0.289	0.0104		0.0114
g		0.075			0.0030	
h		1.325			0.0522	
j		0.825			0.0325	
k		0.250			0.0098	
m		0.500			0.0197	
n		0.075			0.0030	
o	0.300		0.325	0.0118		0.0128
p	0.274		0.299	0.0108		0.0118
q	0.375		0.400	0.0148		0.0157
r	0.339		0.364	0.0133		0.0143
s	0.915	0.930	0.945	0.0360	0.0366	0.0372
t	0.635	0.650	0.665	0.0250	0.0256	0.0262
u		0.375			0.0148	
v		0.500			0.0197	

**Inches provided for reference only.*

LAND PATTERN
(Ball Side Down)



TYPICAL PAD DESIGN



0.280 ±0.05mm PCB Solder Mask Opening

0.355mm Minimum PCB Pad Diameter

Notes
1. Drawing not to scale.
2. Controlling dimensions are in millimeters.