ET901 Fast Ethernet Transceiver

Features

- Single-chip 10Base-T/100Base-TX transceiver.
- Dual speed: 10/100 Mbits/s.
- Half-/full-duplex operation.
- Media-independent interface (MII) to *IEEE 802.3*® MAC.
- MDC/MDIO interface for configuration and status.
- Autonegotiation support.
- 48-pin LQFP package.

Overview

The ET901 series are physical layer devices for Ethernet 10Base-T and 100Base-TX using category five unshielded and type 1 shielded cable. This VLSI device is designed for easy implementation of 10/100 Mbits/s fast Ethernet LANs. It interfaces to a MAC (either a single chip or integrated in south-bridge/CPU/switch) through an MII interface ensuring interoperability between products from different vendors.

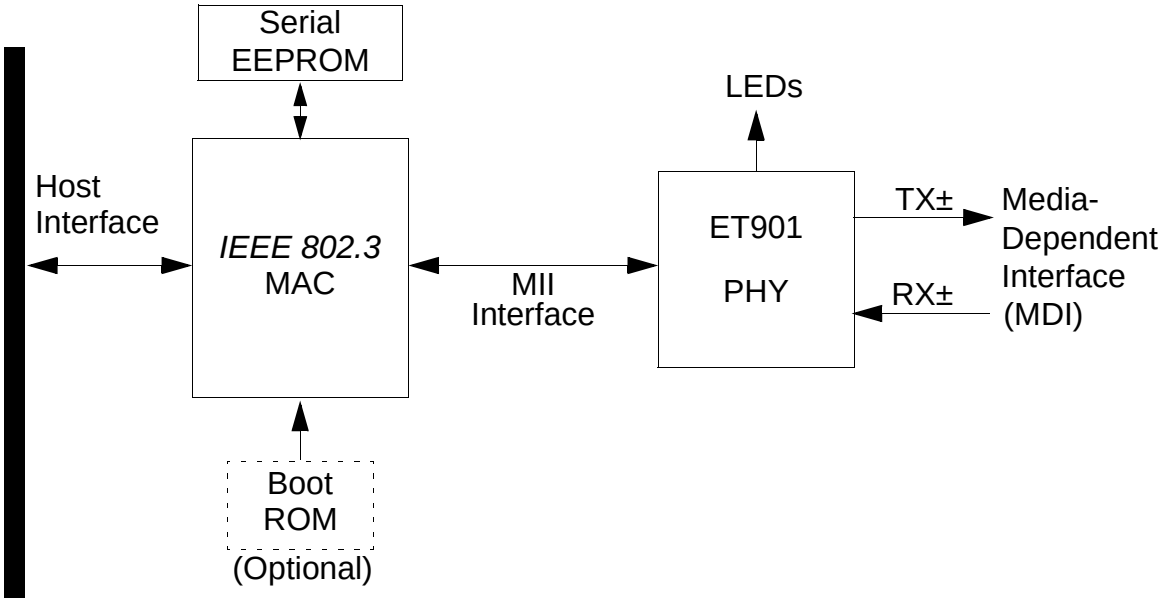

Figure 1. Typical System Block Diagram

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Functional Description

General

The ET901 is a complete 10/100 Mbits/s ethernet media interface IC. The ET901 has the following main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, and MI serial port. A block diagram is shown in Figure 2.

The ET901 can operate as a 100Base-TX device (hereafter referred to as 100 Mbits/s mode) or as a 10Base-T device (hereafter referred to as 10 Mbits/s mode). The differences between 100 Mbits/s mode and 10 Mbits/s mode are data rate, signaling protocol, and allowed wiring. 100 Mbits/s TX mode uses two pairs of category 5 or better UTP or STP twisted-pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a throughput of 100 Mbits/s. 10 Mbits/s mode uses two pairs of category 3 or better UTP or STP twisted-pair cable with Manchester-encoded, 10 MHz binary data to achieve a 10 Mbits/s. The data symbol format on the twisted-pair cable for the 100 Mbits/s and 10 Mbits/s modes is defined in the *IEEE 802.3* specification.

On the transmit side for 100 Mbits/s TX operation, data is received on the controller interface from an external Ethernet controller. The data is then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, preshapes the output, and drives the twisted-pair cable.

On the receive side for 100 Mbits/s TX operation, the twisted-pair receiver receives incoming encoded and scrambled MLT-3 data from the twisted pair cable, removes any high-frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted-pair levels to internal digital levels. The output of the twisted-pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses the clock to latch in valid data into the device, and converts the data back to NRZ format. The NRZ data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and outputted to an external Ethernet controller by the controller interface. 10 Mbits/s operation is similar to 100 Mbits/s TX operation except (1) there is no scrambler/descrambler, (2) the encoder/decoder is Manchester instead of 4B5B, (3) the data rate is 10 Mbits/s instead of 100 Mbits/s, and (4) the twisted-pair symbol data is two-level Manchester instead of ternary MLT-3.

The management interface (hereafter referred to as the MI serial port) is a two-pin bidirectional link through which configuration inputs can be set and status outputs can be read. Each block plus the operating modes is described in more detail in the following sections. Since the ET901 can operate as either a 100Base-TX or a 10Base-T device, each of the following sections describes the performance of the respective section in both 100 Mbits/s and 10 Mbits/s modes.

Status Information

ET901 status information is available on the LED output pins. Transmit activity, receive activity, link status, link polarity and collision activity information is output to the four LED output pins, selectable via LEDSEL in Rx16 (Rx10h) bit[6:5] as follows.

Table 1. LED Output Pin List (Alphabetical Order)

LEDSEL	LED0	LED1	LED2	LED3
00	Link/Act	Speed	Duplex	Collision
01	Power/TxAct	Link/RxAct	Speed	Duplex
10	Speed 100	Speed 10	Act	Duplex
11	Power/TxAct	Link/RxAct	Speed	Collision

Functional Description (continued)

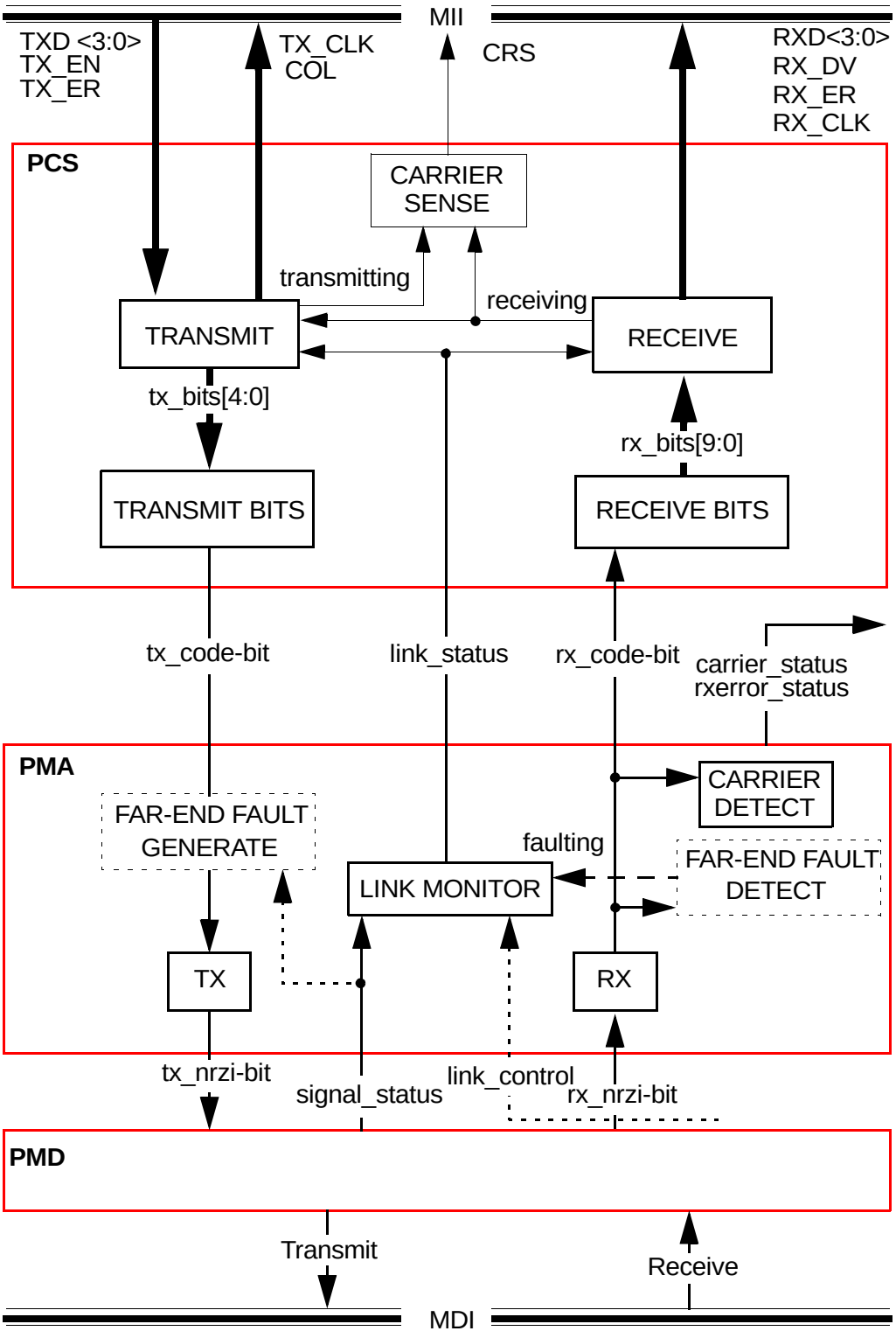


Figure 2. Internal Block Diagram

Pin Information

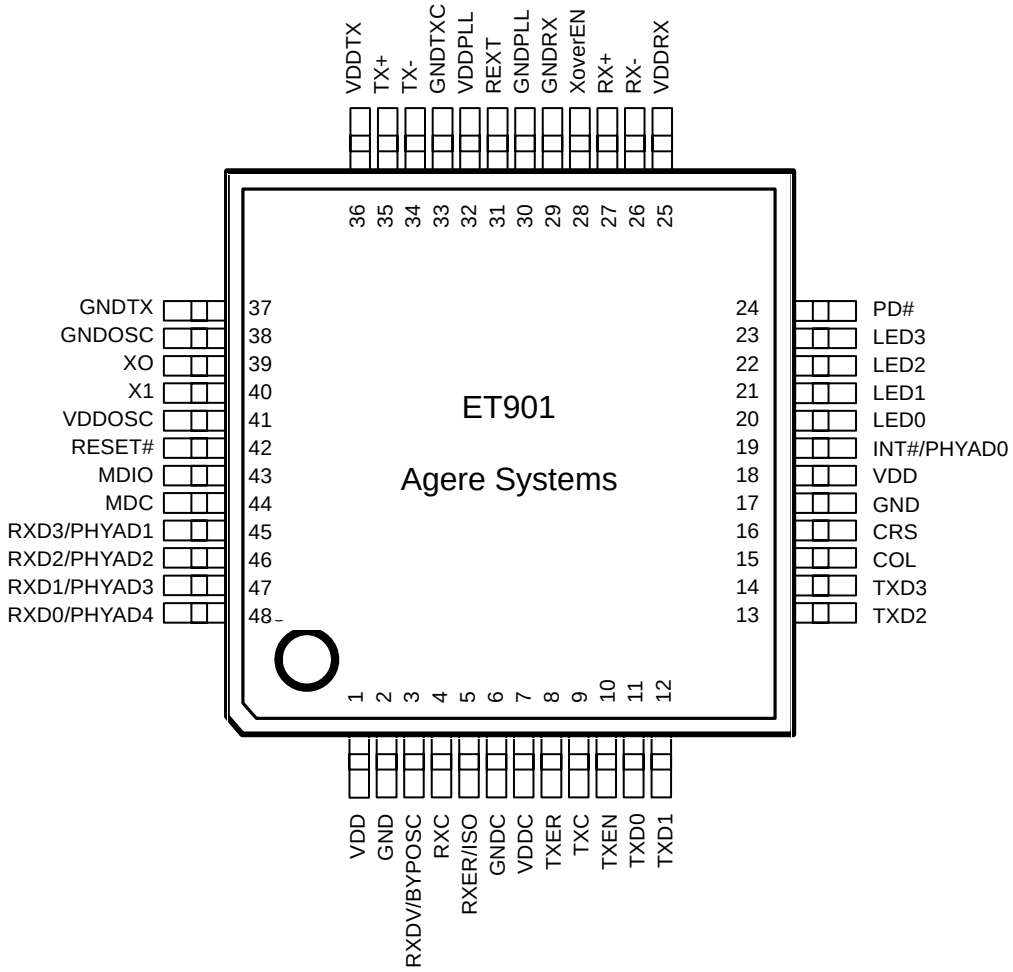


Figure 3. 48-Pin LQFP Package
(Top View)

Pin Information (continued)

Table 2. Pin List (Alphabetical Order)

Number	Type	Name	Number	Type	Name
15	O	COL	47	I/O	RXD1/PHYAD3
16	O	CRS	46	I/O	RXD2/PHYAD2
2, 17	P	GND	45	I/O	RXD3/PHYAD1
6	P	GNDC	3	I/O	RXDV/BYPOSC
38	P	GNDOSC	5	O	RXER/ISO
30	P	GNDPLL	28	I	XoverEN
29	P	GNDRX	34	O	TX–
37	P	GNDTX	35	O	TX+
33	P	GNDTXC	9	O	TXC
19	O	INT#/PHYAD0	11	I	TXD0
20	O	LED0	12	I	TXD1
21	O	LED1	13	I	TXD2
22	O	LED2	14	I	TXD3
23	O	LED3	10	I	TXEN
44	I	MDC	8	I	TXER
43	I/O	MDIO	7	P	VDDC
24	I	PD#	41	P	VCCOSC
42	I	RESET#	32	P	VCCPLL
31	A	REXT	25	P	VCCRX
26	I	RX–	36	P	VCCTX
27	I	RX+	1, 18	P	VDD
4	O	RXC	40	I	XI
48	I/O	RXD0/PHYAD4	39	O	XO

Note: I = input, I/O = input/output, O = output, P = power/ground, A = analog.

Pin Descriptions

In the pin descriptions that follow, the following abbreviations are used to stand for signal type:

I	Input	Input is a standard input-only signal.
O	Output	Output is a standard output-only signal.
I/O	Input/Output	Input/output is a standard input/output signal.
PU	Pull-Up	Pull-up pad.
PD	Pull-Down	Pull-down pad.

Table 3. Media-Independent Interface (MII)

Signal Name	Pin #	I/O	Signal Description
RXC	4	O PD	Receive clock. Timing reference for transfer of RXD and RXDV. 25 MHz when operating at 100 Mbits/s and 2.5 MHz when operating at 10 Mbits/s (always active).
RXD3	45	O PD	Receive data. These bits transition synchronously to RXC. RXD[3:0] should be accepted by the external MAC for each RXC period in which RXDV is asserted. RXD0 is the least significant bit. While RXDV is deasserted, RXD[3:0] have no effect upon the MAC and the value of RXD[3:0] is unspecified.
RXD2	46		
RXD1	47		
RXD0	48		
RXDV	3	O PD	Receive data valid. RXDV is driven to indicate that nibbles are being presented on the MII for receiving. RXDV transition is synchronous to RXC. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be received are presented to the MII.
TXC	9	O PD	Transmit clock. Timing reference for transfer of TXD and TXEN. 25 MHz when operating in 100 Mbits/s and 2.5 MHz when operating in 10 Mbits/s (always active).
TXD3	14	I PD	Transmit data. These bits transition synchronously to TXC. TXD[3:0] are accepted from the external MAC for each TXC period in which TXEN is asserted. TXD0 is the least significant bit. While TXEN is deasserted, TXD[3:0] have no effect and the value of TXD[3:0] is unspecified.
TXD2	13		
TXD1	12		
TXD0	11		
TXEN	10	I PD	Transmit enable. Indicates transmit active from the MII port. TXEN transitions synchronously to TXC. TXEN indicates that the nibbles presented on TXD[3:0] are valid for transmission. TXEN is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented to the MII interface.
TXER	8	I PD	Transmit error. The MAC asserts this input when an error has occurred in the input stream.
COL	15	O PD	Collision detect. Asserted asynchronously upon detection of a collision on the medium and remains asserted while the collision condition persists.
CRS	16	O PD	Carrier sense. Asserted asynchronously upon detection of a nonidle medium or while TXEN is asserted. Deasserted asynchronously upon detection of idle conditions on both transmit and receive media. Remains asserted throughout the duration of a collision condition.

Pin Descriptions (continued)

Table 4. Management Interface (MI)

Signal Name	Pin #	I/O	Signal Description
MDIO	43	I/O PU	Management interface (MI) data I/O. Received from the external MAC.
MDC	44	I PD	Management interface (MI) clock. Received from the external MAC as a timing reference for DIO.

Table 5. LED Outputs

Signal Name	Pin #	I/O	Signal Description
LED0	20	O PU*	LED Output 0. Default = Link/Activity. See Register 16 (10H) bits 5—6 and Table 12 for LED function. Must be pulled high with 330 Ω resistor, or be pulled high with 10 kΩ resister when it is unused.
LED1	21	O PU*	LED Output 1. Default = Speed. See Register 16 (10H) bits 5—6 and Table 12 for LED function. Must be pulled high with 330 Ω resistor, or be pulled high with 10 kΩ resister when it is unused.
LED2	22	O PU*	LED Output 2. Default = Duplex. See Register 16 (10H) bits 5—6 and Table 12 for LED function. Must be pulled high with 330 Ω resistor, or be pulled high with 10 kΩ resister when it is unused.
LED3	23	O PU*	LED Output 3. Default = Collision. See Register 16 (10H) bits 5—6 and Table 12 for LED function. Must be pulled high with 330 Ω resistor, or be pulled high with 10 kΩ resister when it is unused.

* Do not leave LED[3:0] pins floating, even unused. Please refer to the latest ET901 reference schematics.

Table 6. Physical Cable Connection

Signal Name	Pin #	I/O	Signal Description
TX+	35	O	Transmit Plus. Differential outputs for 100Base-TX, or 10Base-T transmission.
TX–	34	O	Transmit Minus. Differential outputs for 100Base-TX, or 10Base-T transmission.
RX+	27	I	Receive Plus. Differential inputs for 100Base-TX, or 10Base-T reception.
RX–	26	I	Receive Minus. Differential inputs for 100Base-TX, or 10Base-T reception.

Pin Descriptions (continued)

Table 7. Resets, Clocks, Control, and Status

Signal Name	Pin #	I/O	Signal Description
XI	40	I	Crystal in. Connect to 25 MHz crystal. Can alternately be driven by an external clock source (3.3 V swing) with XO unconnected.
XO	39	O	Crystal feedback. Connect to other side of 25 MHz crystal.
REXT	31	A	External resistor. Connect a 6.49 kΩ 1% resistor to GNDOSC.
XoverEN	28	I	Auto-crossover Enable. Should be pulled high to enable auto-crossover (MDIX). Pull low to force on MDI mode only.
PD#	24	I	Powerdown. Active-low. Must be pulled up externally.
RESET#	42	I PU	Reset. Active-low. Schmitt input for improved noise immunity. Internally pulled high with approximate 50 kΩ, can be connected to an external 2 µF capacitor for self-reset or an external reset input.

Table 8. Power and Ground

Signal Name	Pin #	I/O	Signal Description
VDD	1, 18	P	Digital I/O power. 3.3 V nominal (3.15 V to 3.45 V). For digital I/O.
GND	2, 17	P	Ground. Connect to primary ground plane.
VDDC	7	P	Core power. 3.3 V nominal (3.15 V to 3.45 V). For internal digital logic.
GNDC	6	P	Core ground. Connect to primary ground plane.
VDDOSC	41	P	Oscillator power. 3.3 V. Isolate from digital supply voltage with a ferrite bead.
GNDOSC	38	P	Oscillator ground. Connect to primary ground plane.
VDDRX	25	P	Receiver power. 3.3 V. Isolate from digital supply voltage with a ferrite bead.
GNDRX	29	P	Receiver ground. Connect to primary ground plane.
VDDTX	36	P	Transmitter power. 3.3 V. Isolate from digital supply voltage with a ferrite bead.
GNDTX	37	P	Transmitter ground. Connect to primary ground plane.
GNDTXC	33	P	Transmit clock ground. Connect to primary ground plane.
VDDPLL	32	P	PLL power. 3.3 V. Isolate from digital supply voltage with a ferrite bead.
GNDPLL	30	P	PLL ground. Connect to primary ground plane.

Pin Strapping

Table 9. Strap Options

Signal Name	Pin #	I/O	Signal Description
BYPOSC/RXDV	3	I PD	Bypass oscillator. Clock source select. Default = crystal. Pull-up externally for using oscillator.
ISO/RXER	5	I PD	Isolate. Latched into register 0, bit 10 at powerup/reset. Internally pulled low for default disabled.
PHYAD4/RXD0	48	I	PHY address. Latched into register 16 (register 10H), bits 15—11 at powerup/reset. Internally pulled (low, low, low, low, high) for default 00001b.
PHYAD3/RXD1	47		
PHYAD2/RXD2	46		
PHYAD1/RXD3	45		
PHYAD0/INT#	19		

Note: For the pins listed above, pull-up/pull-down status is latched during powerup/reset. External strap option values may be set by connecting the indicated pin to a 10 kΩ pull-down for 0 (L) or to a 10 kΩ pull-up for 1 (H).

Registers

Register Overview

The ET901 internal register set consists of thirty-two 16-bit registers.

The bits of PHY registers 0—8 are defined by the *IEEE 802.3u*™ standard. The remaining PHY registers have vendor-specific bit definitions.

PHY registers are addressed by the MAC by sending register address pointer information via the MI interface (serially over the MDIO pin clocked by MDC) with register read/write data transfer via the same pins. For more information on this mechanism, refer to *IEEE 802.3* section 22.2.4.

In the register descriptions that follow, the following terms are used:

RW:	Read/Write	
RO:	Read Only	
SC:	Self Clearing	Self-clearing bits are normally 0. If set to 1, they will perform the indicated function and then automatically be cleared back to 0 by the chip.
LH:	Latch High	Latch high and latch low bits are used to record that an event (level) occurred. For latch high bits, if the bit ever goes high, it will latch at that high level until read (the read will clear the bit).
LL:	Latch Low	Latch high and latch low bits are used to record that an event (level) occurred. For latch low bits, if the bit goes low, it will stay at a low level until read (the read will set the bit high).

Table 10. Register Summary

Offset (Decimal)	Offset (Hex)	Management Interface Registers	Bits	Default	Access
00	00H	Management Interface Control	16	3100H	RW
01	01H	Management Interface Status	16	7849H	RO
02	02H	PHY Identifier 0	16	0101H	RO
03	03H	PHY Identifier 1	16	8F20H	RO
04	04H	Autonegotiation Advertisement Base	16	05E1H	RW
05	05H	Link Partner Advertisement Base	16	0000H	RO
06	06H	Autonegotiation Expansion	16	0004H	RO
07	07H	Autonegotiation Advertisement Next	16	2001H	RW
08	08H	Link Partner Advertisement Next	16	0000H	RO
9—15	09—0FH	Reserved	—	—	—
16	10H	PHY Configuration 1	16	0800H	RW
17—31	15—1FH	Reserved	—	—	—

Registers (continued)

Register Bit Summary

Table 11. Registers Defined by *IEEE 802.3u* Standard

Bit	Register								
	0	1	2	3	4	5	6	7	8
15	Reset	Cap 100T4	OUI (msb)	OUI (lsb)	Next Pg	LP Next Pg	—	Next Page	LP NxtPg
14	Loopback	Cap Tx100F			Ack	LP Ack	—	Ack1	LP Ack1
13	Speed	Cap Tx100H			Rem Flt	LP Rem Flt	—	Msg Page	LP MP
12	Aneg Ena	Cap Tx10F			—	—	—	Ack2	LP Ack2
11	Power-Down	Cap Tx10H			—	—	—	Toggle	LP Toggle
10	Isolate	Cap 100T2F		Part Number	Pause	LP Pause	—	Message Code Field or Unformatted Code Field	Link Partner Message Code Field or Unformatted Code Field
9	Aneg Restart	Cap 100T2H			100T4	LP 100T4	—		
8	Duplex	Extd Status			Tx100F	LP Tx100F	—		
7	COL Test	–			Tx100H	LP Tx100H	—		
6	—	Cap Supr			Tx10F	LP Tx10F	—		
5	—	Aneg Complete			Tx10H	LP Tx10H	Parallel Fault Det LP Cap Next Pg Cap Next Page Aneg Page Rcvd LP Cap Aneg		
4	—	Remote Fault			Selector Field	Link Partner Selector Field			
3	—	Cap Aneg		Revision Number					
2	—	Link Status							
1	—	Jabber Detect							
0	—	Extd Reg							

Registers (continued)

Register Bit Summary (continued)

Table 12. Vendor-Defined Registers

Bit	Register 9~15	Register 16	Register 17~19	Register 20	Register 21~31
15	—	PHY Address	—	—	—
14	—		—	—	—
13	—		—	—	—
12	—		—	—	—
11	—		—	—	—
10	—	—	—	—	—
9	—	—	—	—	—
8	—	—	—	—	—
7	—	—	—	—	—
6	—	LEDOutput Select	—	—	—
5	—		—	—	—
4	—	—	—	—	—
3	—	—	—	—	—
2	—	—	—	—	—
1	—	—	—	Duplex	—
0	—	—	—	Speed	—

Table 13. Offset 0 (00H)—MI Control (3100H) RW

Bit	Description			
15	PHY reset.	—	—	Default = 0, SC
14	Loopback mode.	0	Disable	Default
		1	Enable	—
13	Speed select LSB.	0	10	—
		1	100	Default
12	Autonegotiation process.	0	Disable	
		1	Enable	Default
11	Powerdown.	0	Disable	Default
		1	Enable	
10	Electrically isolate PHY from MII.	0	Disable	Default
		1	Enable	—
9	Autonegotiation restart.	—	—	Default = 0, SC
8	Duplex mode select.	0	Half	—
		1	Full	Default
7	COL test.	0	Disable	Default
		1	Enable	—
6	Speed select MSB.	—	—	Reserved, always reads 0
5—0	Reserved.	—	—	Always reads 0

Registers (continued)

Register Descriptions (continued)

Table 14. Offset 1 (01H)—MI Status (7849H) RO

Bit	Description	
15	Capable of 100 Base-T4 operation.	Default = 0.
14	Capable of 100 Base-TX full duplex.	Default = 1.
13	Capable of 100 Base-TX half duplex.	Default = 1.
12	Capable of 10 Base-TX full duplex.	Default = 1.
11	Capable of 10 Base-TX half duplex.	Default = 1.
10	Capable of 100 Base-T2 full duplex.	Default = 0.
9	Capable of 100 Base-T2 half duplex.	Default = 0.
8	Extended status information in Rx15.	Default = 0.
7	Reserved.	Always reads 0.
6	Capable of accepting MI frames with MI preamble suppressed.	Default = 1.
5	Autonegotiation process completed.	Default = 0.
4	Remote fault condition detected.	LH, default = 0.
3	Capable of autonegotiation operation.	Default = 1.
2	Link status.	LL, default = 0.
1	Jabber condition detected.	LH, default = 0.
0	Capable of extended register.	Default = 1.

Table 15. Offset 2 (02H)—PHY Identifier 0 (0101H) RO

Bit	Dcscription	
15—0	Company ID MSBs.	Always reads 0101H.

Table 16. Offset 3 (03H)—PHY Identifier 1 (8F20H) RO

Bit	Description	
15—10	Company ID LSBs.	Always reads 23H.
9—4	Manufacturer’s part number.	Always reads 32H.
3—0	Manufacturer’s revision number.	Always reads 0.

Table 17. Offset 4 (04H)—Autonegotiation Advertisement Base Page (05E1H) RW

Bit	Description	
15	Next page.	Default = 0.
14	Received code word recognized.	RO, Default = 0.
13	Remote fault.	Default = 0.
12—11	Reserved.	Always reads 0.
10	Pause operation for full-duplex link.	Default = 1.
9	100 Base-T4 capable.	Default = 0.
8	100 Base-TX full-duplex capable.	Default = 1.
7	100 Base-TX half-duplex capable.	Default = 1.
6	10 Base-TX full-duplex capable.	Default = 1.
5	10 Base-TX half-duplex capable.	Default = 1.
4—0	Selector field.	Default = 00001b.

Registers (continued)

Register Descriptions (continued)

Table 18. Offset 5 (05H)—Link Partner Advertisement Base Page (0000H) RO

Bit	Description	
15	Next page.	Default = 0.
14	Received code word recognized.	Default = 0.
13	Remote fault.	Default = 0.
12—11	Reserved.	Always reads 0.
10	Pause operation for full-duplex link.	Default = 0.
9	100 Base-T4 capable.	Default = 0.
8	100 Base-TX full-duplex capable.	Default = 0.
7	100 Base-TX half-duplex capable.	Default = 0.
6	10 Base-TX full-duplex capable.	Default = 0.
5	10 Base-TX half-duplex capable.	Default = 0.
4—0	Selector field.	Default = 0.

Table 19. Offset 6 (06H)—Autonegotiation Expansion (0004H) RO

Bit	Description	
15—5	Reserved.	Always reads 0.
4	Parallel fault detect in autonegotiation process.	LH, default = 0.
3	Link partner capable of next page process.	Default = 0.
2	Capable of next page process.	Default = 0.
1	Page received in autonegotiation process.	LH, default = 0.
0	Link partner capable of autonegotiation process.	Default = 0.

Table 20. Offset 7 (07H)—Autonegotiation Advertisement Next Page (2001H) RW

Bit	Description	
15	Next page.	Default = 0.
14	Received code word recognized.	RO, default = 0.
13	Message page.	Default = 1.
12	Capable of complying with message.	Default = 0.
11	Toggle bit.	RO, default = 0.
10—0	Message code field or unformatted code field.	Default = 001H.

Table 21. Offset 8 (08H)—Link Partner Advertisement Next Page (0000H) RO

Bit	Description	
15	Next page.	Default = 0.
14	Received code word recognized.	Default = 0.
13	Message page.	Default = 0.
12	Capable of complying with message.	Default = 0.
11	Toggle bit.	Default = 0.
10—0	Message code field or unformatted code field.	Default = 0.

Registers (continued)

Register Descriptions (continued)

Table 22. Offset 16 (10H)—PHY Configuration 1 (0800H) RW

Bit	Description				
15—11	PHY Address	Default = 01H	—	—	—
10	—	0	Disable	Default	—
		1	Enable	—	—
9—7	Reserved (Do Not Program)				
6—5	**Programmable LED Output Select**				
	Bit	**LED0**	**LED1**	**LED2**	**LED3**
	00	Link/Act	Speed	Duplex	Default = Collision
	01	Pwr/TxAct	Link/RxAct	Speed	Duplex
	10	Speed 100	Speed 10	Act	Duplex
	11	Pwr/TxAct	Link/RxAct	Speed	Collision
4—0	Reserved (Do Not Program)				

Table 23. Offset 20 (14H)—PHY Status (0000H) RO

Bit	Description			
15—13	Reserved (do not program).			
12	PHY link status.	0	Unlink	Default
		1	Link	—
11—2	Reserved (do not program).			
1	PHY speed status.	0	10 Mbits/s	Default
		1	100 Mbits/s	—
0	PHY duplex status.	0	Half Duplex	Default
		1	Full Duplex	—

Electrical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 24. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comment
Storage Temperature	–40	125	^{o}C	TS
Case Temperature	0	110	^{o}C	TC
Ambient Temperature	0	70	^{o}C	TA
Electrostatic Discharge	—	2	kV	Human-body model (HBM)
Power Supply Voltages (All)	–0.5	4.0	V	VDD, VCC, VCCOSC, VCCPLL, VCCRX, VCCTX
Input Voltage	–0.5	VDD + 0.5	V	
Output Voltage At Any Output	–0.5	VDD – 0.5	V	

dc Characteristics

Table 25. dc Characteristics

TC = 0 ^{o}C—110 ^{o}C, VDD = 3.3 V ± 0.3 V, GND = 0 V

Symbol	Parameter	Min	Max	Unit	Comment
VIL	Input Low Voltage	–0.5	0.9	V	—
VIH	Input High Voltage	2.4	VDD + 0.5	V	—
VOL	Output Low Voltage	—	0.1 VDD	V	LED0—3
VOH	Output High Voltage	0.9 VDD	—	V	LED0—3
IIL	Input Leakage Current	—	±50	µA	—
IOZ	Tristate Leakage Current	—	±50	µA	—
CIN	Input Capacitance	—	7.5	pF	Fc = 1 MHz, TXD, TXEN, TXER
COUT	Output Capacitance	—	7.5	pF	Fc = 1 MHz, RXD, RXDV, RXER, RXCK, TXCK
IDD	Power Supply Current	—	130	mA	10Base-T
IDD	Power Supply Current	—	80	mA	100Base-Tx
TPU	Powerup Reset Time	2	—	ms	—
TSETUP	Setup Time	6	—	ns	50% to 50%, 10 pF load
THOLD	Hold Time	0	—	ns	50% to 50%, 10 pF load
TDELAY	Delay Time	—	6	ns	50% to 50%, 10 pF load

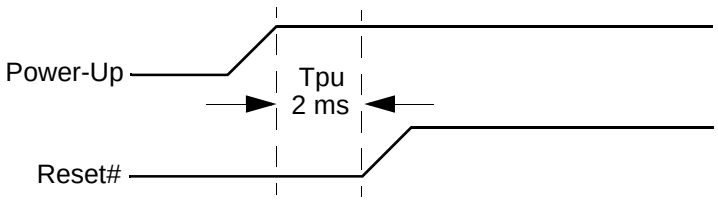


Figure 4. Power Reset Timing

Electrical Specifications (continued)

ac Characteristics

ac timing specifications provided assume an REXT of 6.49 kΩ ± 1%, clock rate of 25 MHz ± 0.005%, power supply voltage of 3.0 V to 3.6 V, and case temperature between 0 ^{o}C—100 ^{o}C.

Table 26. 100Base-T Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
—	Output Differential Amplitude	1.9	2	2.1	Vpp	UTP (100 Ω)
—	Output Differential Amplitude	1.9	2	2.1	Vpp	STP (100 Ω)
—	Output Differential Amplitude	—	2.45		Vpp	STP (150 Ω)
—	Output Symmetry	0.98	—	1.02	V/V	Differential pos/neg
TR/TF	Output Rise/Fall	3	—	5	ns	—
—	Output Rise/Fall Skew	—	—	0.5	ns	—
—	Output Overshoot	—	—	5	%	—
—	Output Timing Jitter (peak to peak)	—	—	1.4	ns	Scrambled
—	Return Loss	10	—	—	dB	2 ~ 30 MHz
—	Return Loss	16	—	—	dB	30 ~ 60 MHz
—	Return Loss	20log(f/30M)10	—	—	dB	60 ~ 80 MHz
DCD	Duty Cycle Distortion	—	—	0.5	ns	—
—	Transmitter On-Chip Power Consumption	—	—	45	mA	100 Ω

Table 27. 10Base-T Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
—	Output Differential Amplitude	4.4	—	5.6	Vpp	UTP (100 Ω)
—	Harmonic Content	27	—	—	dB	All 1 and all 0
—	Idle Pulse Width	250	—	—	ns	—
—	Link Pulse Width	—	100	—	ns	—
—	Output Jitter Without Cable	—	—	±8	ns	—
—	Output Jitter with Cable	—	—	±3.5	ns	—

Table 28. Crystal Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comment
—	Input Frequency	24.9975	25	25.0025	MHz	—
—	TXC/RXC Output Frequency	24.9975	25	25.0025	MHz	—
—	TXC/RXC Output Frequency Jitter, Short Term	—	—	50	ps	—
—	TXC/RXC Output Frequency Jitter, Long Term	—	—	500	ps	—

Electrical Specifications (continued)

ac Characteristics (continued)

Table 29. PLL Frequency Multiplier Characteristics

Parameter	Min	Typ	Max	Unit	Comment
PLL Loop Bandwidth	—	2.5	5	MHz	—
PLL Acquisition Time	—	—	50	µs	25% frequency change
VCO Operating Frequency, 100Base Mode	—	250	—	MHz	—
VCO Operating Frequency, 10Base Mode	—	200	—	MHz	—
PLL Output Clock Jitter, Short Term	—	—	200	ps	—
PLL Output Clock Jitter, Long Term	—	—	1000	ps	—

Table 30. Transformer Characteristics

Parameter	TX	RX
Turn Ratio	1:1 CT	1:1 CT
Inductance (max.)	350 µH @ 8 mA	350 µH @ 8 mA
Capacitance (max.)	15 pF	15 pF
dc Resistance (max.)	0.4 Ω	0.4 Ω

Note: For ET901 with auto-crossover enabled, both CTs of TX and RX must be tied together and pulled up. Please see the schematic diagram for details.

Table 31. MI Interface MDIO Output Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T4/TMC	MDCK Frequency	—	—	10	MHz	—
T2/TMIOS	MDIO Input Setup Time	10	—	—	ns	To MDCK rising edge
T3/TMIOH	MDIO Input Hold Time	10	—	—	ns	To MDCK rising edge
T1/TMOD	MDIO Output Delay	0	—	300	ns	To MDCK rising edge

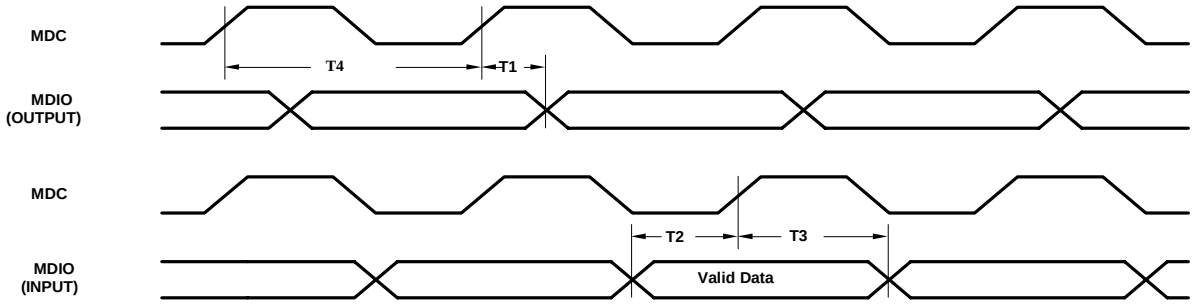


Figure 5. MI Interface MDIO Timing

Electrical Specifications (continued)

Table 32. LED On/Off Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	LED[3:0] On Time	—	68	—	ms	—
T2	LED[3:0] Off Time	—	68	—	ms	—

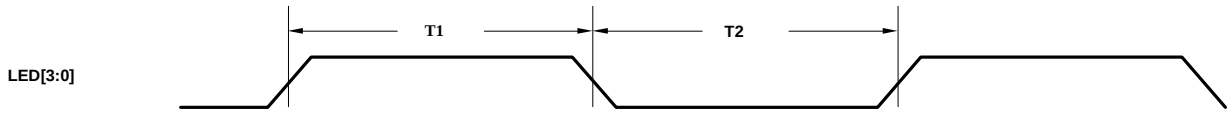


Figure 6. LED On/Off Timing

Table 33. MII Transmit Data Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	TXD[3:0], TXEN, TXER Setup to TXC	10	—	—	ns	—
T2	TXD[3:0], TXEN, TXER Hold from TXC	0	—	—	ns	—

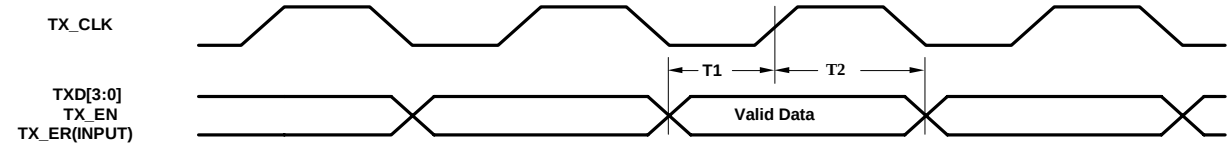


Figure 7. MII Transmit Data Timing

Table 34. MII Receive Data Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	RXD[3:0], RXDV, RXER to RXC Output Delay	—	—	25	ns	—
T2	RXC Clock Period	—	40	—	ns	—

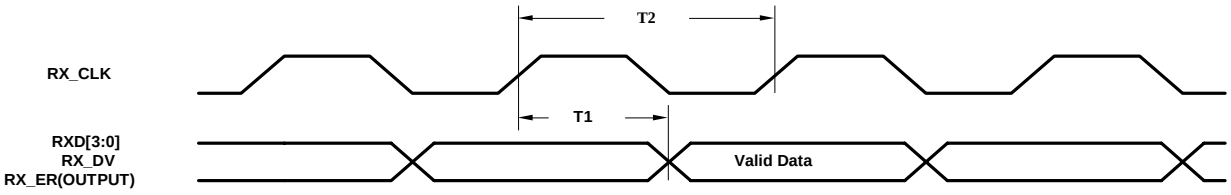


Figure 8. MII Receive Data Timing

Electrical Specifications (continued)

Table 35. MII Heartbeat Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	COL Heartbeat Delay	—	900	—	ns	—
T2	COL Heartbeat Duration	—	1000	—	ns	—

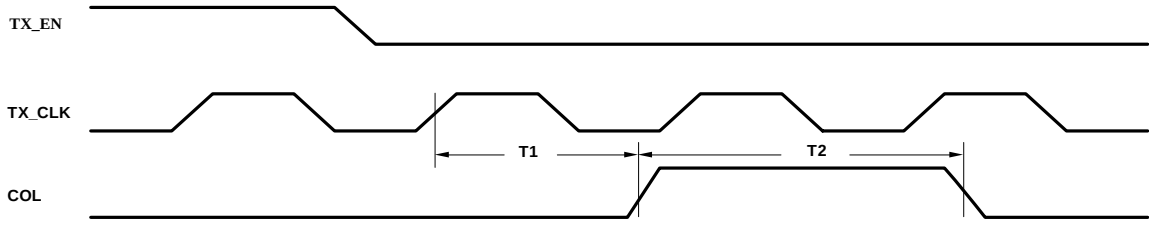


Figure 9. MII Heartbeat Timing

Table 36. MII Jabber Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	Jabber Activation Time	—	20	150	ms	—
T2	Jabber Deactivation Time	—	490	—	ms	—

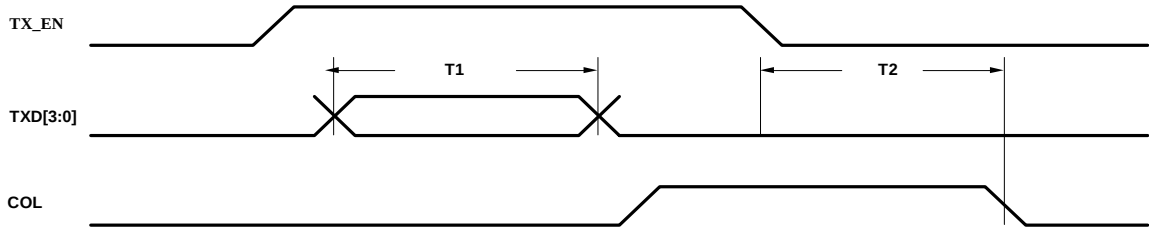


Figure 10. MII Jabber Timing

Table 37. MII 10Base-T Normal Link Pulse Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	Clock, Data Pulse Width	—	100	—	ns	—
T2	Link Pulse to Link Pulse Period	—	8	—	ms	—

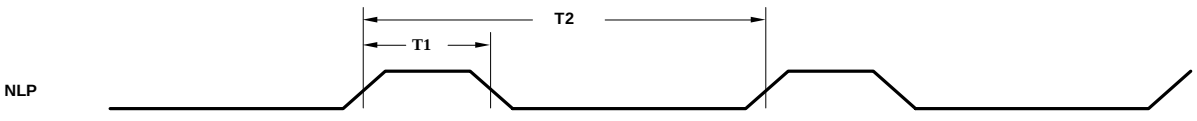


Figure 11. MII Normal Link Pulse Timing

Electrical Specifications (continued)

Table 38. MII Xnegotiation Fast Link Pulse Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	Clock, Data Pulse Width	—	100	—	ns	—
T2	Clock Pulse to Clock Pulse Period	—	125	—	µs	—
T3	Clock Pulse to Data Pulse Period	—	62.5	—	µs	—
T4	Burst Width	—	2	—	ms	—
T5	FLP Burst to FLP Burst Period	—	8	—	ms	—

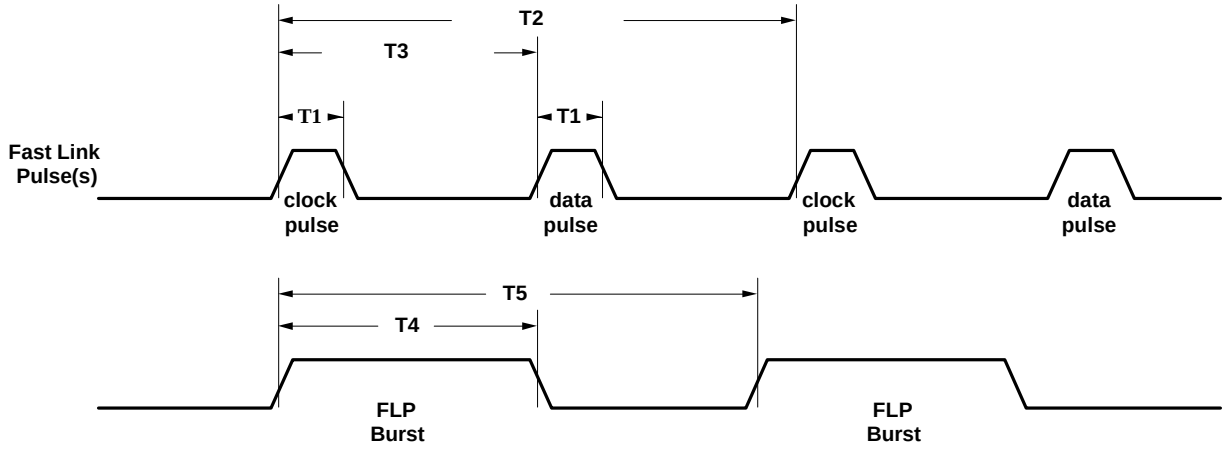


Figure 12. MII Autonegotiation Fast Link Pulse Timing

Table 39. 100 Mbits/s Receive Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	Carrier Sense On Delay	—	100	—	ns	—
T2	Receive Data Latency	—	160	—	ns	—

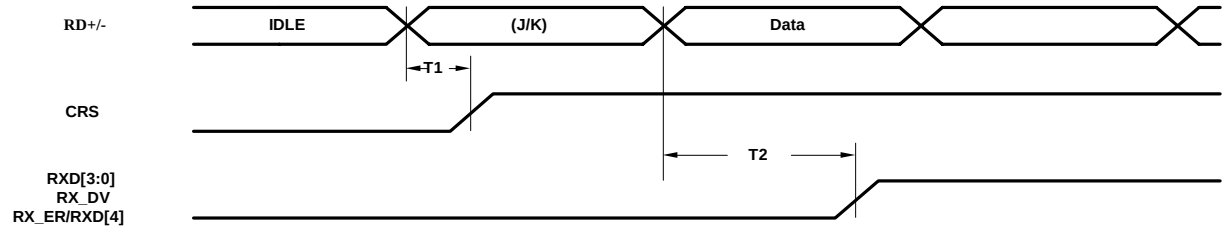


Figure 13. 100 Mbits/s Receive Packet Timing

Electrical Specifications (continued)

Table 40. 100 Mbits/s Transmit Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	TXC to TX +/– Latency	—	—	120	ns	—
T2	TXC to TX +/– Deassertion	—	—	120	ns	—

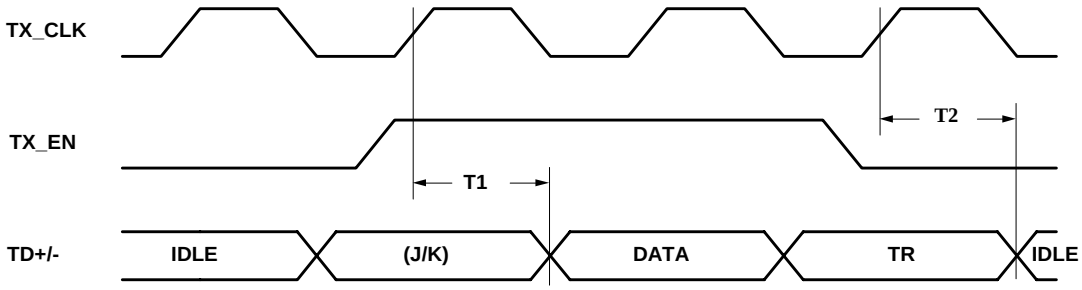


Figure 14. 100 Mbits/s Transmit Packet Timing

Table 41. 10 Mbits/s Receive Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	Carrier Sense On Delay	—	550	—	ns	—
T2	Receive Data Valid Delay	—	2200	—	ns	—
T3	Receive Data Latency	—	750	—	ns	—

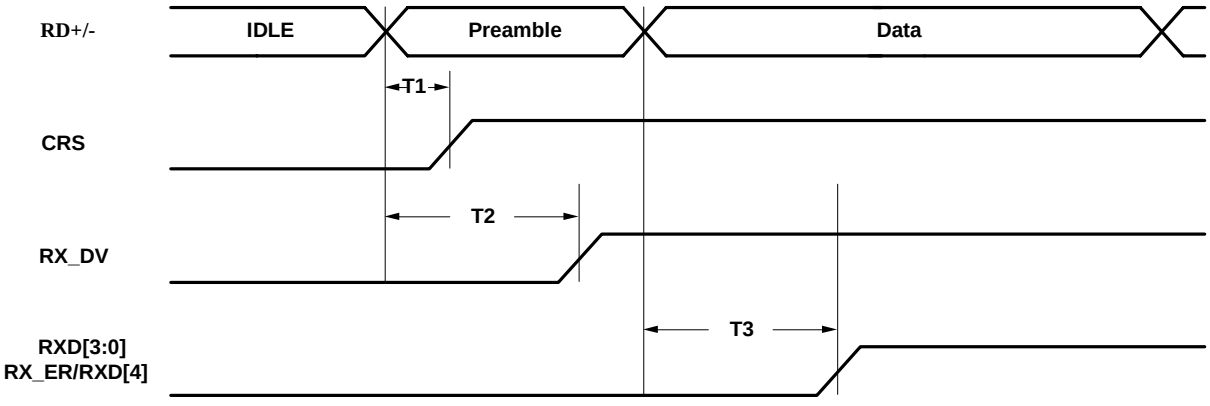


Figure 15. 10 Mbits/s Receive Packet Timing

Electrical Specifications (continued)

Table 42. 10 Mbits/s Transmit Packet Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comment
T1	TXC to TX+/– Latency	—	470	—	ns	—
T2	TXC to TX+/– Deassertion	—	700	—	ns	—

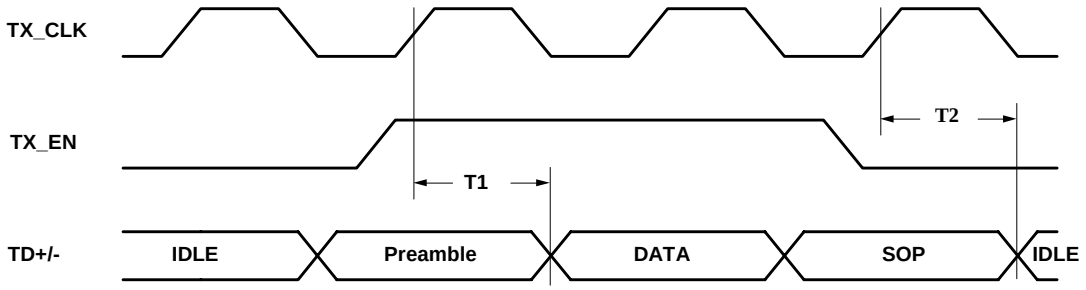
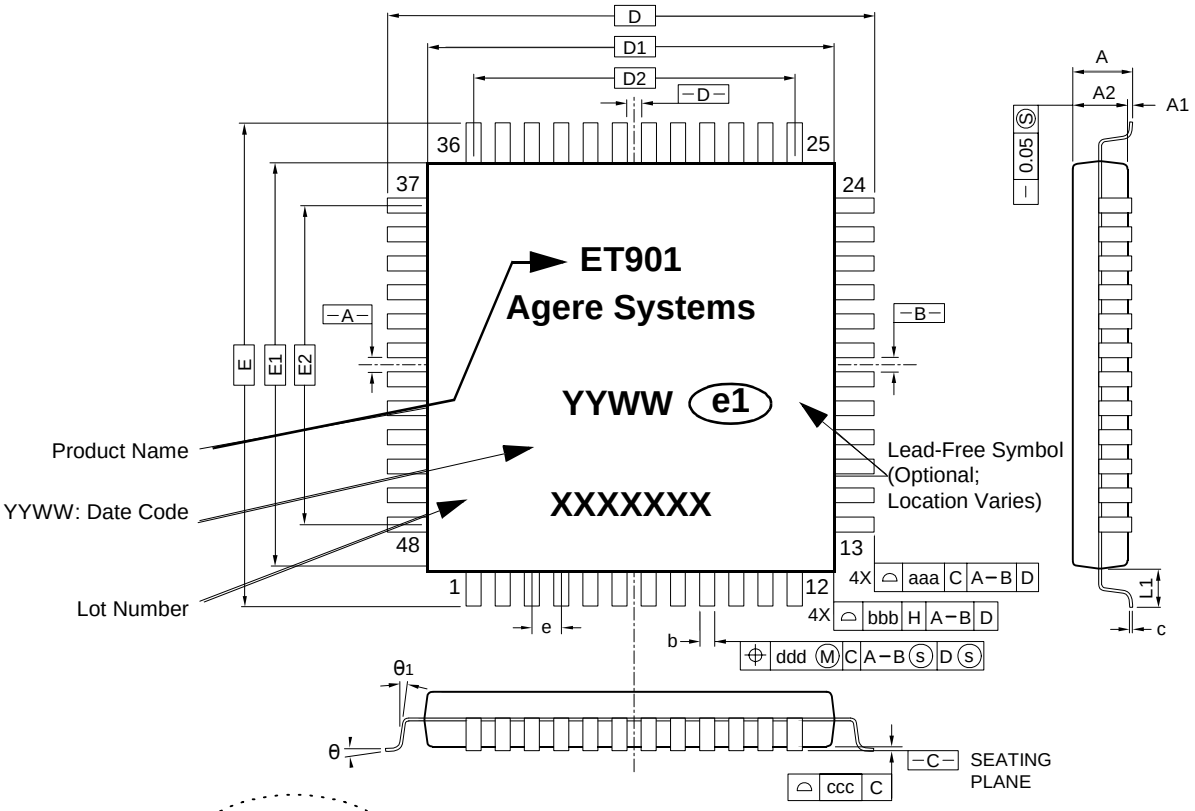
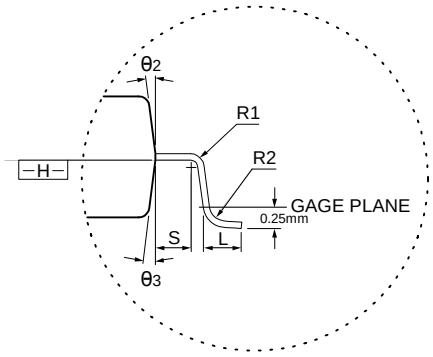


Figure 16. 10 Mbits/s Transmit Packet Timing

Package Mechanical Specifications





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTE:

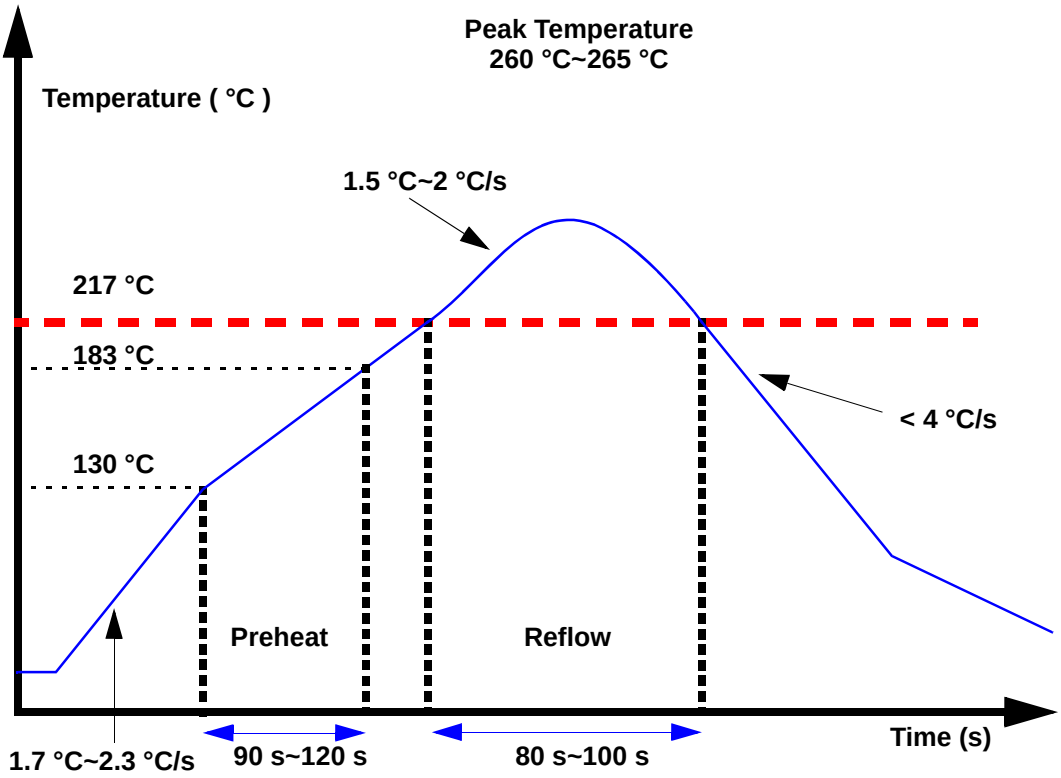
1) DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2) DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

Figure 17. ET901 LQFP-48 Package (7 mm × 7 mm)

Lead-Free Package Infrared Reflow

The profile chart as following is recommended for lead-free package in infrared reflow process of production.



Ordering Information

Device	Package	Description		Part Number	Comcode
ET901	48-pin LQFP	Fast Ethernet Transceiver, Lead-Free.	Dry Baked Tray.	L-ET901-L-DB	711010964
			Dry Baked Reel.	L-ET901-L-DT	711010965

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