Wistron Confidential

PV1

2009/12/28 REV :PV-01

<Core Design>

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Hsichih, Taipei

Title: *Cover*		
Size: A3	Document Number: PATEK	Rev: SA
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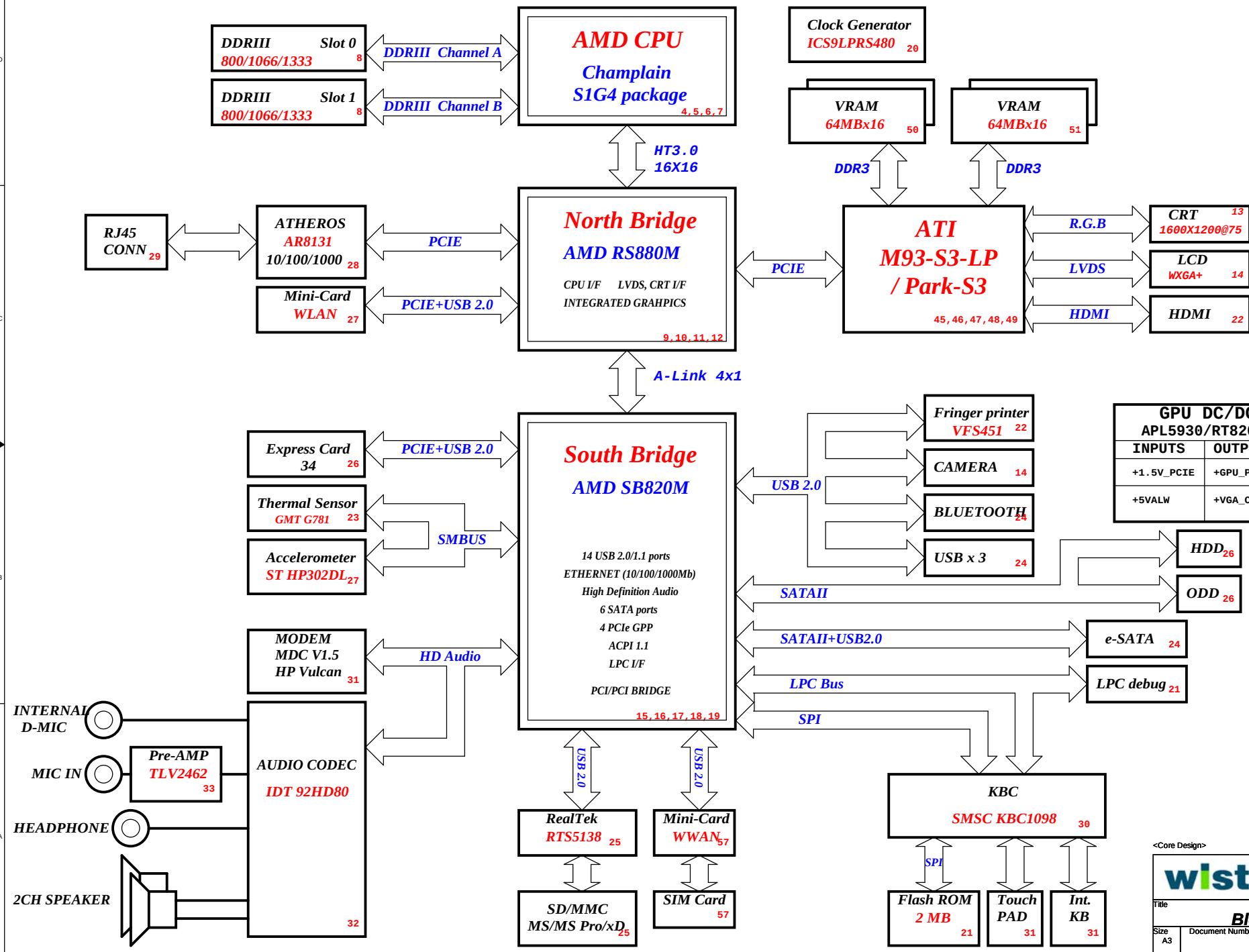
Patek DIS Block Diagram



SYSTEM DC/DC
RT8205A

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VL +3VALW +3VL 39

SYSTEM DC/DC
RT8209B

INPUTS	OUTPUTS
+5VALW	+1.1VALW 41

SYSTEM DC/DC
G972

INPUTS	OUTPUTS
+3VS	+1.8VS 38

SYSTEM DC/DC
G9091/RT9205

INPUTS	OUTPUTS
+3VS	+2.5VS_LDO_CPU
+1.5VS	+1.05VS 37

SYSTEM DC/DC
RT8207

INPUTS	OUTPUTS
+5VALW	+1.5V +0.75V 40

GPU DC/DC
APL5930/RT8209B

INPUTS	OUTPUTS
+1.5V_PCIE	+GPU_PCIE 38
+5VALW	+VGA_CORE 52

MAXIM CHARGER
BQ24740

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 42

CPU DC/DC
ISL6265/RT8209B

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE +VDDNB 36
+5VALW	+NB_VDDC 54

PCB 6 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

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Title: Block Diagram

Size	Document Number	Rev
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RS880M strapping

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS880M--> VSYNC)
0 : Enable * 1 : Disable

RS880: Enables Side port memory (RS880 use HSYNC)

0 : Enable * 1 : Disable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

PCIE routing

Page 9

LANE 0	LAN
LANE 3	NEW CARD
LANE 4	WLAN

USB table

Page 18

Pair	Device
USB-FSD1 FPR	
USB-9 Bluetooth	
USB-8 WLAN	
USB-7 WWAN	
USB-6 USB Card Reader	
USB-5 Right Side	
USB-4 USB Camera	
USB-3 Right Side	
USB-2 Left Side (e-SATA combo)	
USB-1 New Card	
USB-0 Left Side (S/W Debug port)	

SB820M strapping

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK_KBC (LPCCLK0)	LPC_CLK_DB (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM L, L = FWH ROM

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	SB-TSI
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SB_SMB_CLK1 SB_SMB_DAT1	SB820M	X	X	X	X	X	X	X
SB_SMB_CLK0 SB_SMB_DAT0	SB820M	X	V	V	V	V	X	X
CPU_SIC_SB700 CPU_SID_SB700	CPU	X	X	X	X	X	X	V

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Title: NOTES

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HT

CPU VLDT MAX 1.5A

LAYOUT: PLACE CLOSE TO CPU
ALONG HT POWER SHAPE

+1.1VS

C1 SCD22U25V3KX-GP
C2 SCD22U25V3KX-GP
C3 SC180P50V2JN-1GP
C4 SC180P50V2JN-1GP

091221-1
6 HDT_RST#
R3 0R0402-PAD-1-GP
LDT_RST#_CPU
LDT_PWROK
CPU_LDT_STOP#

CPU1A
SEC 1 OF 6
LDT

D1	V_HT_A1	
D2	V_HT_A2	
D3	V_HT_A3	
D4	V_HT_A4	
B7	RESET*	LDT_RST#_CPU
A7	PWROK	LDT_PWROK
F10	LDTSTOP*	CPU_LDT_STOP#

9 NB0CADOUT[15..0]
9 NB0CADOUTJ[15..0]

N5	HT_RXD_P15	NB0CADOUT15
M3	HT_RXD_P14	NB0CADOUT14
L5	HT_RXD_P13	NB0CADOUT13
K3	HT_RXD_P12	NB0CADOUT12
H3	HT_RXD_P11	NB0CADOUT11
G5	HT_RXD_P10	NB0CADOUT10
F3	HT_RXD_P9	NB0CADOUT9
E5	HT_RXD_P8	NB0CADOUT8
N3	HT_RXD_P7	NB0CADOUT7
L1	HT_RXD_P6	NB0CADOUT6
L3	HT_RXD_P5	NB0CADOUT5
J1	HT_RXD_P4	NB0CADOUT4
G1	HT_RXD_P3	NB0CADOUT3
G3	HT_RXD_P2	NB0CADOUT2
E1	HT_RXD_P1	NB0CADOUT1
E3	HT_RXD_P0	NB0CADOUT0
P5	HT_RXD_N15	NB0CADOUTJ15
M4	HT_RXD_N14	NB0CADOUTJ14
M5	HT_RXD_N13	NB0CADOUTJ13
K4	HT_RXD_N12	NB0CADOUTJ12
H4	HT_RXD_N11	NB0CADOUTJ11
H5	HT_RXD_N10	NB0CADOUTJ10
F4	HT_RXD_N9	NB0CADOUTJ9
F5	HT_RXD_N8	NB0CADOUTJ8
N2	HT_RXD_N7	NB0CADOUTJ7
M1	HT_RXD_N6	NB0CADOUTJ6
L2	HT_RXD_N5	NB0CADOUTJ5
K1	HT_RXD_N4	NB0CADOUTJ4
H1	HT_RXD_N3	NB0CADOUTJ3
G2	HT_RXD_N2	NB0CADOUTJ2
F1	HT_RXD_N1	NB0CADOUTJ1
E2	HT_RXD_N0	NB0CADOUTJ0

J5	HT_RXCLK_P1	NB0HTTCLKOUT1
J3	HT_RXCLK_P0	NB0HTTCLKOUT0
K5	HT_RXCLK_N1	NB0HTTCLKOUTJ1
J2	HT_RXCLK_N0	NB0HTTCLKOUTJ0
P3	HT_RXCTL_P1	NB0HTTCTLOUT1
N1	HT_RXCTL_P0	NB0HTTCTLOUT0
P4	HT_RXCTL_N1	NB0HTTCTLOUTJ1
P1	HT_RXCTL_N0	NB0HTTCTLOUTJ0

9 NB0HTTCLKOUT1
9 NB0HTTCLKOUT0
9 NB0HTTCLKOUTJ1
9 NB0HTTCLKOUTJ0
9 NB0HTTCTLOUT1
9 NB0HTTCTLOUT0
9 NB0HTTCTLOUTJ1
9 NB0HTTCTLOUTJ0

DANUB

DY
C7 SC4D7U25V5KX-GP
C5 SC4D7U25V5KX-GP
C6 SC4D7U25V5KX-GP

091215-1

V_HT_B1	AE2	
V_HT_B2	AE3	
V_HT_B3	AF4	
V_HT_B4	AE5	
LDTREQ*	C6	LDT_REQ#

CPUCADOUT[15..0] 9
CPUCADOUTJ[15..0] 9

T4	HT_TXD_P15	CPUCADOUT15
V5	HT_TXD_P14	CPUCADOUT14
V4	HT_TXD_P13	CPUCADOUT13
Y5	HT_TXD_P12	CPUCADOUT12
AB5	HT_TXD_P11	CPUCADOUT11
AB4	HT_TXD_P10	CPUCADOUT10
AD5	HT_TXD_P9	CPUCADOUT9
AD4	HT_TXD_P8	CPUCADOUT8
T1	HT_TXD_P7	CPUCADOUT7
U2	HT_TXD_P6	CPUCADOUT6
V1	HT_TXD_P5	CPUCADOUT5
W2	HT_TXD_P4	CPUCADOUT4
AA2	HT_TXD_P3	CPUCADOUT3
AB1	HT_TXD_P2	CPUCADOUT2
AC2	HT_TXD_P1	CPUCADOUT1
AD1	HT_TXD_P0	CPUCADOUT0
T3	HT_TXD_N15	CPUCADOUTJ15
U5	HT_TXD_N14	CPUCADOUTJ14
V3	HT_TXD_N13	CPUCADOUTJ13
W5	HT_TXD_N12	CPUCADOUTJ12
AA5	HT_TXD_N11	CPUCADOUTJ11
AB3	HT_TXD_N10	CPUCADOUTJ10
AC5	HT_TXD_N9	CPUCADOUTJ9
AD3	HT_TXD_N8	CPUCADOUTJ8
R1	HT_TXD_N7	CPUCADOUTJ7
U3	HT_TXD_N6	CPUCADOUTJ6
U1	HT_TXD_N5	CPUCADOUTJ5
W3	HT_TXD_N4	CPUCADOUTJ4
AA3	HT_TXD_N3	CPUCADOUTJ3
AA1	HT_TXD_N2	CPUCADOUTJ2
AC3	HT_TXD_N1	CPUCADOUTJ1
AC1	HT_TXD_N0	CPUCADOUTJ0
Y4	HT_TXCLK_P1	CPUHTTCLKOUT1
Y1	HT_TXCLK_P0	CPUHTTCLKOUT0
Y3	HT_TXCLK_N1	CPUHTTCLKOUTJ1
W1	HT_TXCLK_N0	CPUHTTCLKOUTJ0
T5	HT_TXCTL_P1	CPUHTTCTLOUT1
R2	HT_TXCTL_P0	CPUHTTCTLOUT0
R5	HT_TXCTL_N1	CPUHTTCTLOUTJ1
R3	HT_TXCTL_N0	CPUHTTCTLOUTJ0

CPUHTTCLKOUT1 9
CPUHTTCLKOUT0 9
CPUHTTCLKOUTJ1 9
CPUHTTCLKOUTJ0 9
CPUHTTCTLOUT1 9
CPUHTTCTLOUT0 9
CPUHTTCTLOUTJ1 9
CPUHTTCTLOUTJ0 9

P6	HTREF1	L0_REF1
R6	HTREF0	L0_REF0

R10 44D2R2F-GP
R11 44D2R2F-GP
+1.1VS
PLACE WITHIN 1"
5MIL TRACE
10MIL SPACE

091222-1
+1.5VS
RN141
SRN300J-3-GP
LDT_PWROK
LDT_RST#_CPU
LDT_REQ#
R5 300R2J-4-GP
DY

S1G3 & S1G4 not support LDT_REQ#

091221-1
15 CPU_LDT_RST#
R6 0R0402-PAD-1-GP
LDT_RST#_CPU 10
15 CPU_PWRGD
R7 0R0402-PAD-1-GP
LDT_PWROK 36

+1.5VS
R2 300R2J-4-GP
+1.8VS
090817-1
R2283 2K2R2F-GP
C994 SCD1U16V2ZY-2GP
091222-1
U155
NC#1 VCC
A
GND Y
74LVC1G07GW-GP
15 CPU_LDT_STOP#
LDT_STP#_CPU 10

<Core Design>

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Title: CPU(1/4) HT
Size: A3
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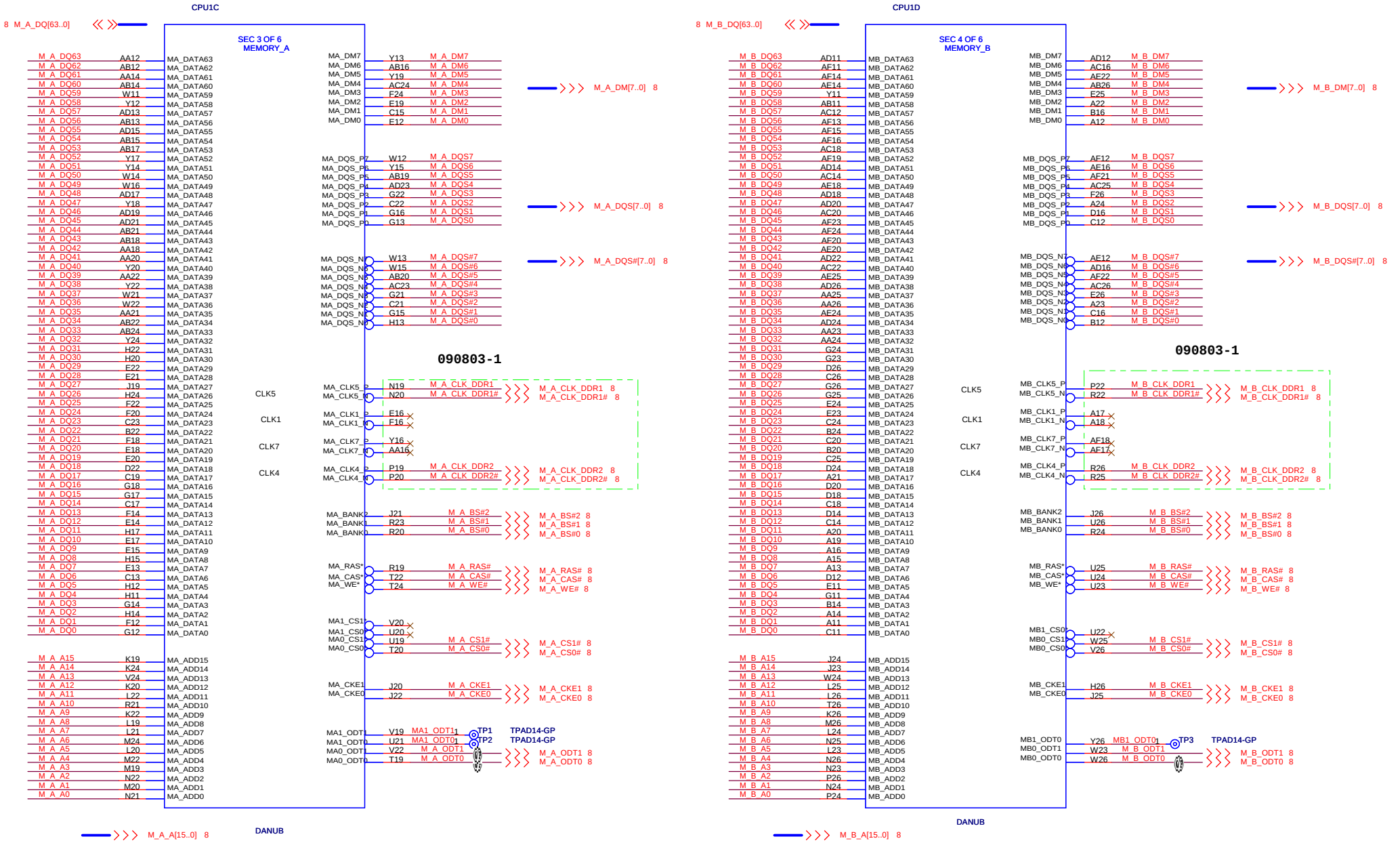

<Core Design>

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Title

CPU(2/4) DDR III

Size	Document Number	Rev
A3	PATEK	SA

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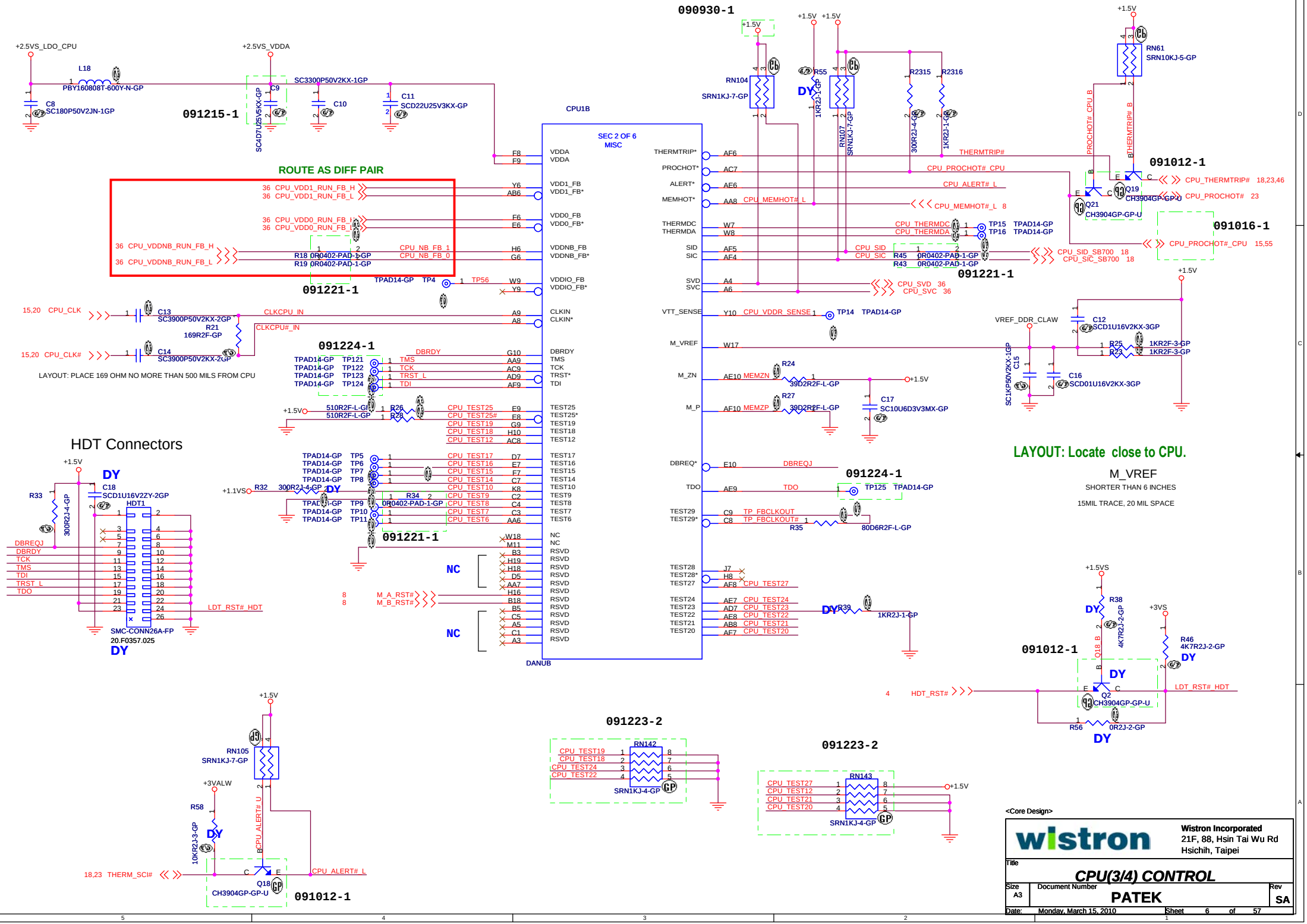
090930-1
+2.5VS_LDO_CPU
+2.5VS_VDDA
L18
PBY160808T-600Y-N-GP
C8
SC180P50V2JN-1GP
091215-1
SC4D7U25V6KX-GP
C9
SC3300P50V2KX-1GP
C10
C11
SCD22U25V3KX-GP
CPU1B
SEC 2 OF 6
MISC
DANUB
ROUTE AS DIFF PAIR
36 CPU_VDD1_RUN_FB_H
36 CPU_VDD1_RUN_FB_L
VDD1_FB
VDD1_FB*
36 CPU_VDD0_RUN_FB_H
36 CPU_VDD0_RUN_FB_L
VDD0_FB
VDD0_FB*
36 CPU_VDDNB_RUN_FB_H
36 CPU_VDDNB_RUN_FB_L
R18 0R0402-PAD-1-GP
R19 0R0402-PAD-1-GP
CPU_NB_FB_1
CPU_NB_FB_0
VDDNB_FB
VDDNB_FB*
091221-1
TPAD14-GP TP4
TP56
VDDIO_FB
VDDIO_FB*
15,20 CPU_CLK
15,20 CPU_CLK#
C13
SC3900P50V2KX-2GP
C14
SC3900P50V2KX-2GP
R21
169R2F-GP
CLKCPU_IN
CLKCPU#_IN
CLKIN
CLKIN*
LAYOUT: PLACE 169 OHM NO MORE THAN 500 MILS FROM CPU
091224-1
DBRDY
TMS
TCK
TRST*
TDI
TPAD14-GP TP121
TPAD14-GP TP122
TPAD14-GP TP123
TPAD14-GP TP124
+1.5V
510R2F-L-GP
R26
R29
CPU_TEST25
CPU_TEST25#
CPU_TEST19
CPU_TEST18
CPU_TEST12
TEST25
TEST25*
TEST19
TEST18
TEST12
HDT Connectors
DY
C18
SCD1U16V2ZY-2GP
R33
300R2J-4-GP
HDT1
DBREQJ
DBRDY
TCK
TMS
TDI
TRST_L
TDO
SMC-CONN26A-FP
20.F0357.025
LDT_RST#_HDT
+1.1VS
R32
300R2J-4-GP
R34
0R0402-PAD-1-GP
TPAD14-GP TP5
TPAD14-GP TP6
TPAD14-GP TP7
TPAD14-GP TP8
TPAD14-GP TP9
TPAD14-GP TP10
TPAD14-GP TP11
CPU_TEST17
CPU_TEST16
CPU_TEST15
CPU_TEST14
CPU_TEST10
CPU_TEST9
CPU_TEST8
CPU_TEST7
CPU_TEST6
TEST17
TEST16
TEST15
TEST14
TEST10
TEST9
TEST8
TEST7
TEST6
091221-1
NC
NC
RSVD
M_A_RST#
M_B_RST#
THERMTRIP*
PROCHOT*
ALERT*
MEMHOT*
THERMDC
THERMDA
SID
SIC
SVD
SVC
VTT_SENSE
M_VREF
M_ZN
M_P
DBREQ*
TDO
TEST29
TEST29*
TEST28
TEST28*
TEST27
TEST24
TEST23
TEST22
TEST21
TEST20
RN104
SRN1KJ-7-GP
R55
1KR2J-1-GP
RN107
SRN1KJ-7-GP
R2315
R2316
300R2J-4-GP
1KR2J-1-GP
THERMTRIP#
CPU_PROCHOT# CPU
CPU_ALERT# L
CPU_MEMHOT# L
CPU_THERMDC
CPU_THERMDA
TP15 TPAD14-GP
TP16 TPAD14-GP
CPU_SID
CPU_SIC
R45 0R0402-PAD-1-GP
R43 0R0402-PAD-1-GP
CPU_SID_SB700 18
CPU_SIC_SB700 18
091221-1
CPU_SVD 36
CPU_SVC 36
TP14 TPAD14-GP
CPU_VDDR_SENSE
R24
39D2R2F-L-GP
R27
39D2R2F-L-GP
C17
SC10U6D3V3MX-GP
091224-1
TP125 TPAD14-GP
TDO
TP_FBCLKOUT
TP_FBCLKOUT#
R35
80D6R2F-L-GP
R39
1KR2J-1-GP
RN61
SRN10KJ-5-GP
PROCHOT# CPU_B
BTHERMTRIP# B
091012-1
Q19
CH3904GP-GP-U
Q21
CH3904GP-GP-U
CPU_THERMTRIP# 18,23,46
CPU_PROCHOT# 23
091016-1
CPU_PROCHOT#_CPU 15,55
VREF_DDR_CLAW
C12
SCD1U16V2KX-3GP
C15
SC1KP50V2KX-1GP
C16
SCD01U16V2KX-3GP
R25
R23
1KR2F-3-GP
LAYOUT: Locate close to CPU.
M_VREF
SHORTER THAN 6 INCHES
15MIL TRACE, 20 MIL SPACE
+1.5VS
R38
4K7R2J-2-GP
+3VS
R46
4K7R2J-2-GP
091012-1
Q2
CH3904GP-GP-U
R56
0R2J-2-GP
4 HDT_RST#
LDT_RST#_HDT
091223-2
RN142
CPU_TEST19
CPU_TEST18
CPU_TEST24
CPU_TEST22
SRN1KJ-4-GP
091223-2
RN143
CPU_TEST27
CPU_TEST12
CPU_TEST21
CPU_TEST20
SRN1KJ-4-GP
RN105
SRN1KJ-7-GP
+3VALW
R58
10KR2J-3-GP
CPU_ALERT# U
18,23 THERM_SCI#
Q18
CH3904GP-GP-U
CPU_ALERT# L
091012-1
<Core Design>
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Title
CPU(3/4) CONTROL
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
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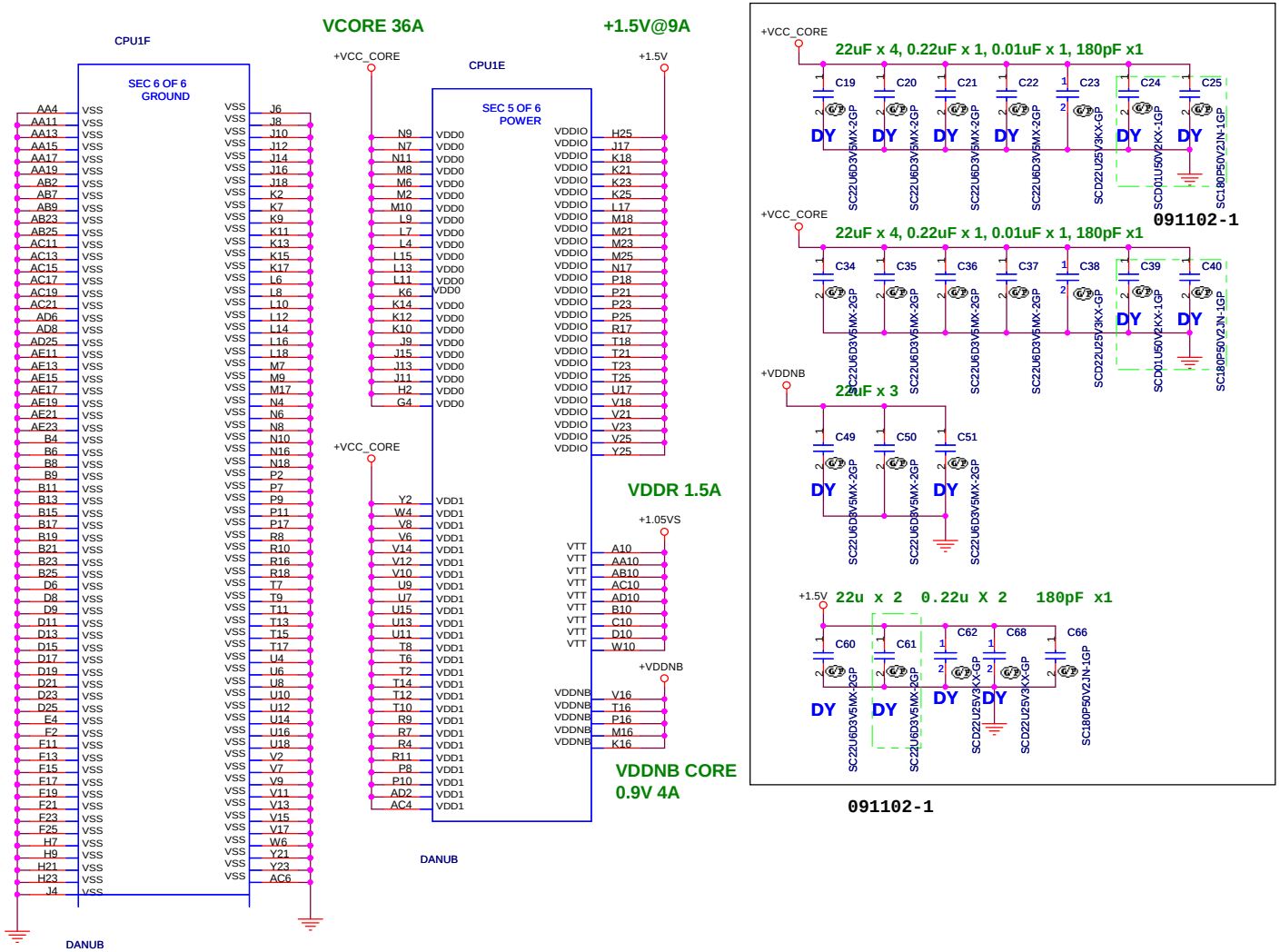
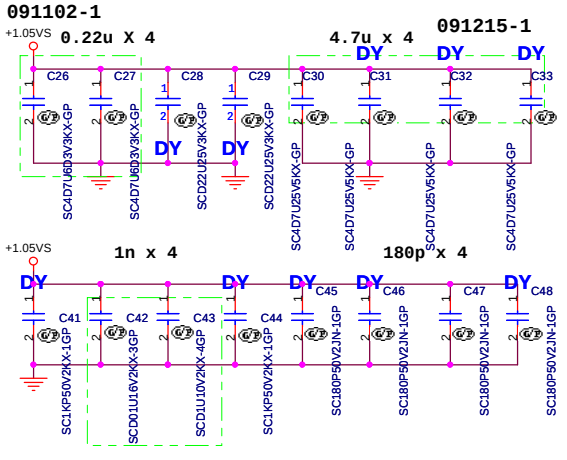
CPU MEMORY VTT

LAYOUT: PLACE UNDER CPU ON BACK

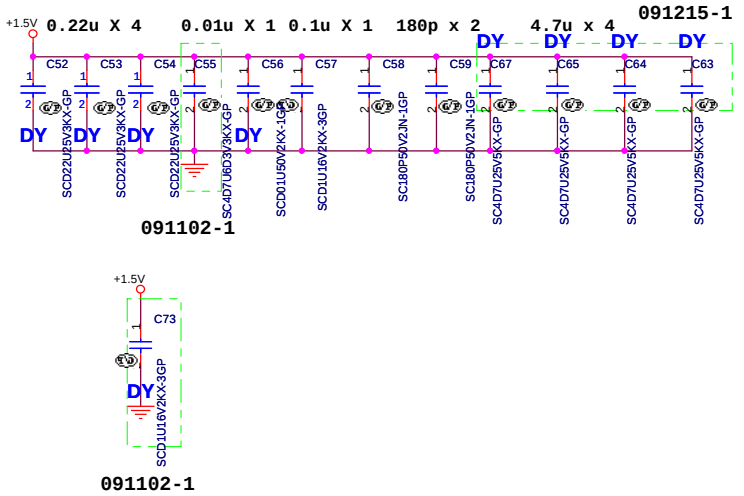


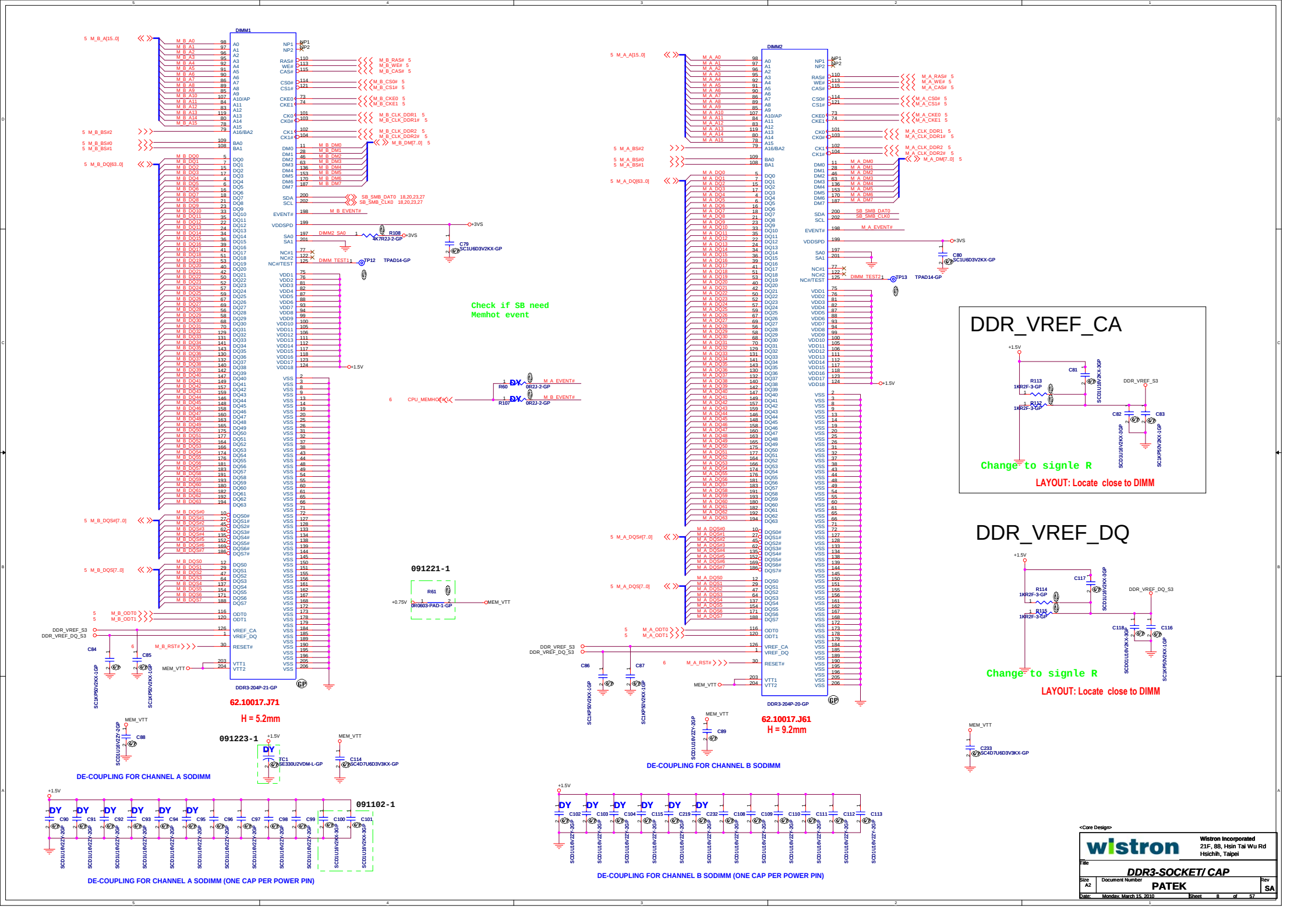
LAYOUT: PLACE CLOSE TO CPU socket



CPU VDDIO

LAYOUT: PLACE CLOSE TO CPU BETWEEN CPU AND MEMORY





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Title: DDR3-SOCKET/ CAP

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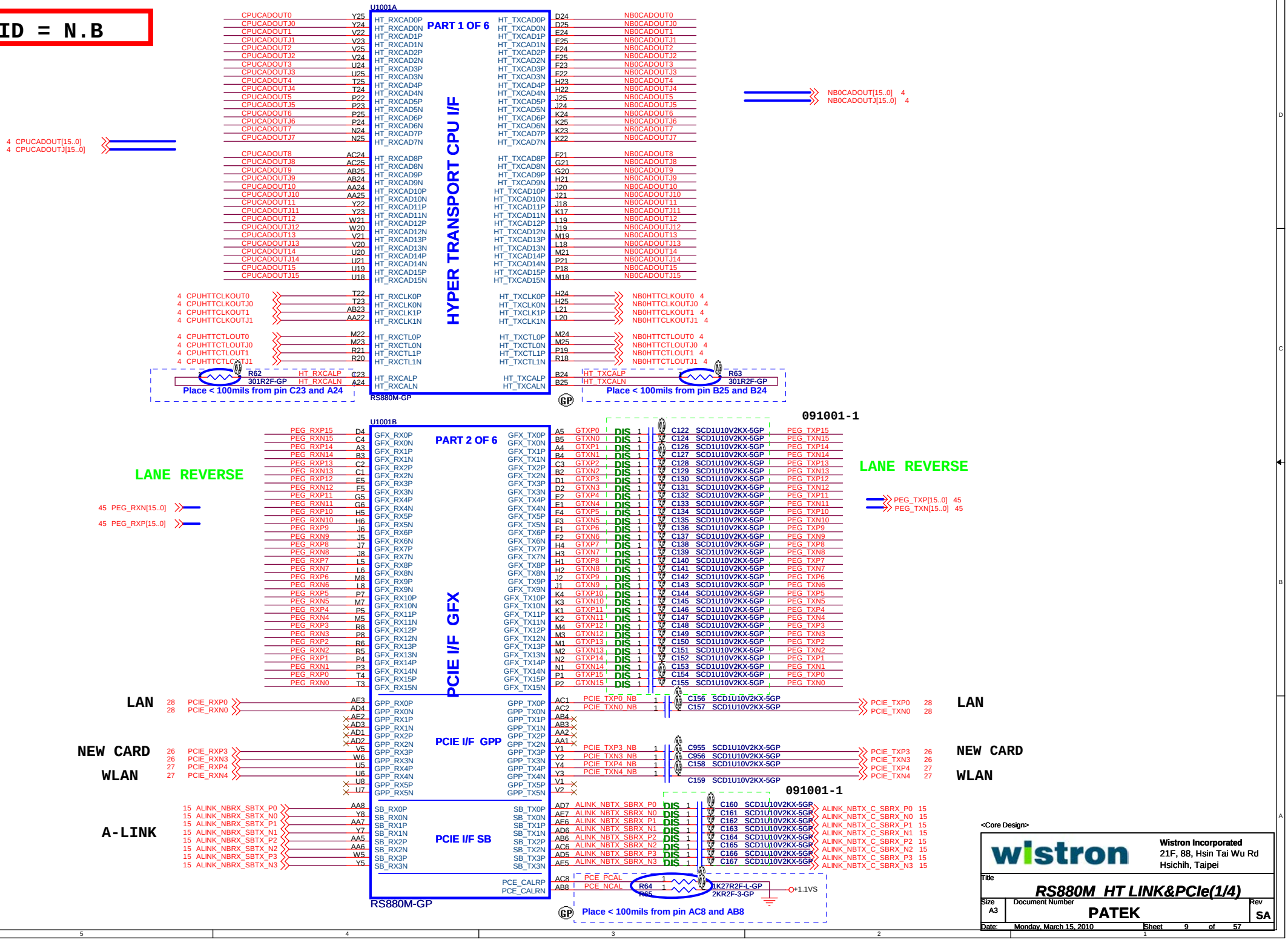
SSID = N.B



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Hsichih, Taipei

Title: RS880M HT LINK&PCIe(1/4)

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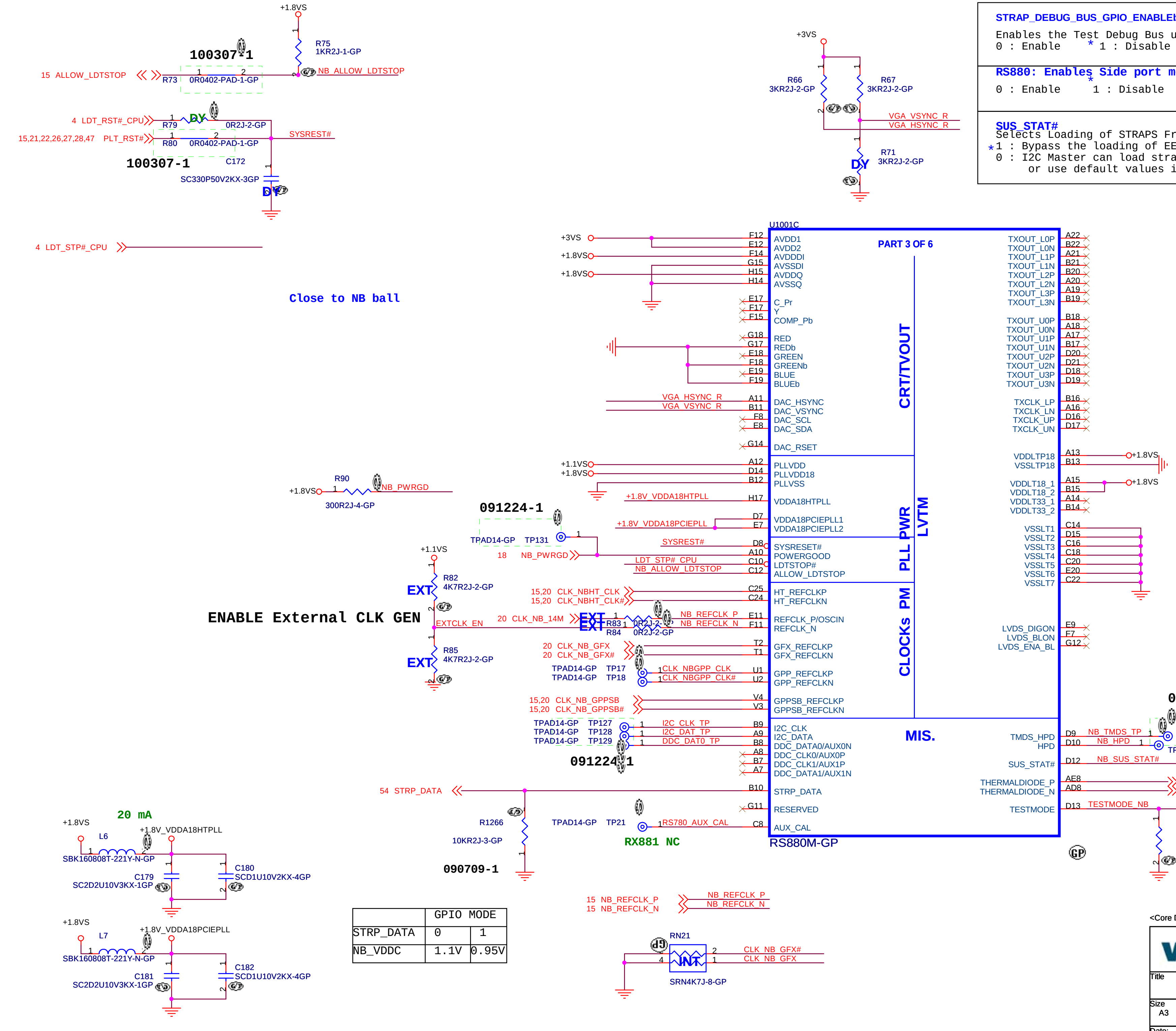

100307-1
+1.8VS
R75
1KR2J-1-GP
15 ALLOW_LDTSTOP
R73
0R0402-PAD-1-GP
NB_ALLOW_LDTSTOP
4 LDT_RST#_CPU
R79
DY
0R2J-2-GP
15,21,22,26,27,28,47 PLT_RST#
R80
0R0402-PAD-1-GP
SYSREST#
100307-1
C172
SC330P50V2KX-3GP
DY
4 LDT_STP#_CPU
Close to NB ball
+3VS
R66
3KR2J-2-GP
R67
3KR2J-2-GP
VGA_VSYNC_R
VGA_HSYNC_R
R71
DY
3KR2J-2-GP
U1001C
PART 3 OF 6
AVDD1
AVDD2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C_Pr
Y
COMP_Pb
RED
REDb
GREEN
GREENb
BLUE
BLUEb
DAC_HSYNC
DAC_VSYNC
DAC_SCL
DAC_SDA
DAC_RSET
CRT/TVOUT
PLLVDD
PLLVDD18
PLLVSS
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
PLL PWR
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
PM
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN
REFCLK_N
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP
GPPSB_REFCLKN
CLOCKs
I2C_CLK
I2C_DATA
DDC_DATA0/AUX0N
DDC_CLK0/AUX0P
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
STRP_DATA
RESERVED
AUX_CAL
MIS.
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
LVTM
VDDLTP18
VSSLTP18
VDDLT18_1
VDDLT18_2
VDDLT33_1
VDDLT33_2
VSSLT1
VSSLT2
VSSLT3
VSSLT4
VSSLT5
VSSLT6
VSSLT7
LVDS_DIGON
LVDS_BLON
LVDS_ENA_BL
TMDS_HPD
HPD
SUS_STAT#
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
RS880M-GP
+3VS
+1.8VS
+1.1VS
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL
VGA_HSYNC_R
VGA_VSYNC_R
R90
300R2J-4-GP
NB_PWRGD
091224-1
TPAD14-GP TP131
18 NB_PWRGD
SYSREST#
LDT_STP#_CPU
NB_ALLOW_LDTSTOP
R82
4K7R2J-2-GP
EXT
ENABLE External CLK GEN
EXTCLK_EN
20 CLK_NB_14M
R83
R84
0R2J-2-GP
NB_REFCLK_P
NB_REFCLK_N
R85
4K7R2J-2-GP
15,20 CLK_NBHT_CLK
15,20 CLK_NBHT_CLK#
20 CLK_NB_GFX
20 CLK_NB_GFX#
TPAD14-GP TP17
TPAD14-GP TP18
CLK_NBGPP_CLK
CLK_NBGPP_CLK#
15,20 CLK_NB_GPPSB
15,20 CLK_NB_GPPSB#
TPAD14-GP TP127
TPAD14-GP TP128
TPAD14-GP TP129
I2C_CLK_TP
I2C_DAT_TP
DDC_DAT0_TP
091224-1
54 STRP_DATA
R1266
10KR2J-3-GP
TPAD14-GP TP21
RS780_AUX_CAL
RX881 NC
090709-1
+3VS
R94
4K7R2J-2-GP
NB_SUS_STAT#
R76
3KR2J-2-GP
DY
091224-1
NB_TMDS_TP
NB_HPD
TP130 TPAD14-GP
TP19 TPAD14-GP
NB_SUS_STAT#
R91
0R2J-2-GP
SUS_STAT# 18
NB_DXP1 23
NB_DXN1 23
To G781
TESTMODE_NB
TP126 TPAD14-GP
R93
1K8R2F-GP
091224-1
20 mA
+1.8VS
+1.8V_VDDA18HTPLL
L6
SBK160808T-221Y-N-GP
C179
SC2D2U10V3KX-1GP
C180
SCD1U10V2KX-4GP
+1.8VS
+1.8V_VDDA18PCIEPLL
L7
SBK160808T-221Y-N-GP
C181
SC2D2U10V3KX-1GP
C182
SCD1U10V2KX-4GP
15 NB_REFCLK_P
15 NB_REFCLK_N
NB_REFCLK_P
NB_REFCLK_N
RN21
INT
SRN4K7J-8-GP
CLK_NB_GFX#
CLK_NB_GFX

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable *1 : Disable

RS880: Enables Side port memory (RS880 use HSYNC)

0 : Enable *1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

	GPIO MODE	
STRP_DATA	0	1
NB_VDDC	1.1V	0.95V

<Core Design>

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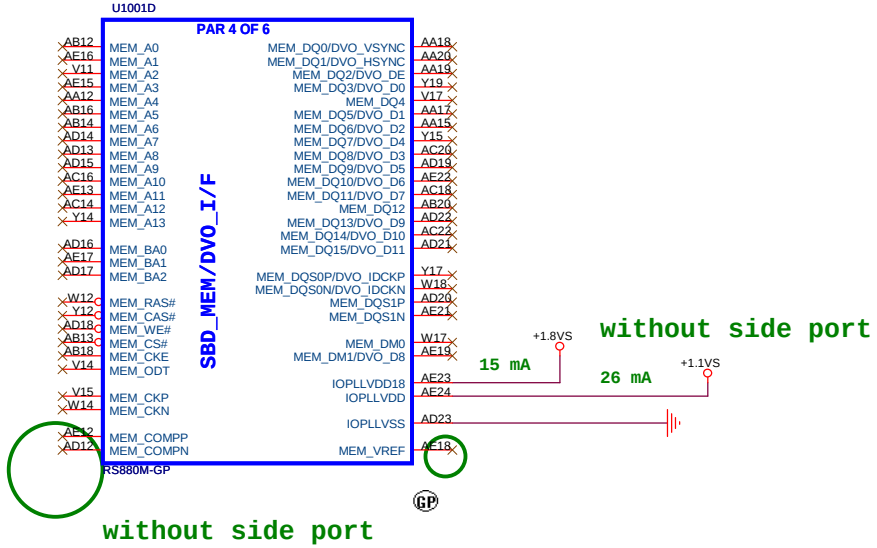
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **RS880M LVDS&CRT(2/4)**

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 10 of 57



<Core Design>

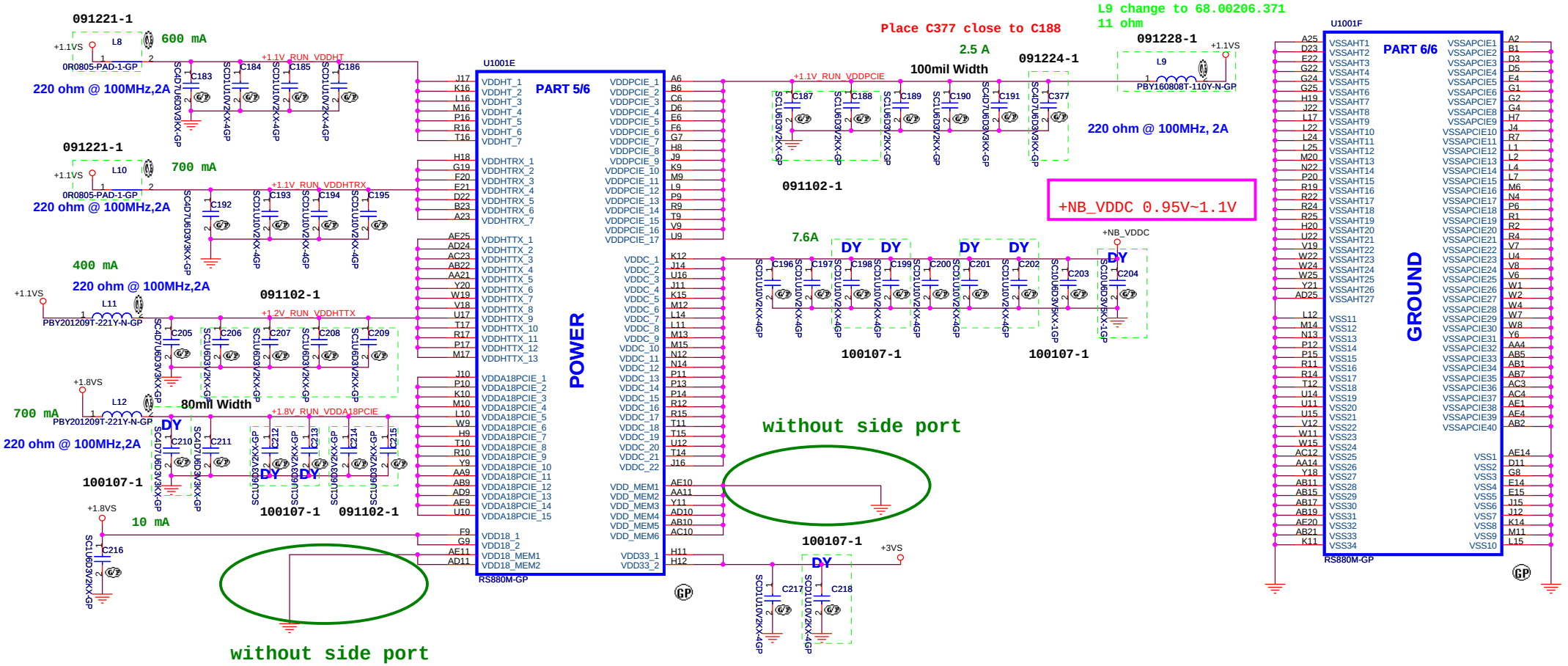
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M Side Port(3/4)

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 11 of 57

SSID = N.B



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: RS880M PWR&GND(4/4)

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 12 of 57

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

46 M93_RED
46 M93_GREEN
46 M93_BLUE

L13 NBQ160808T-470Y-N-GP → CRT_R
L14 NBQ160808T-470Y-N-GP → CRT_G
L15 NBQ160808T-470Y-N-GP → CRT_B

C221 C222 C223 C224 C225 C226 SC10P50V2JN-4GP

091225-1

091225-1

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

M93_RED
M93_GREEN
M93_BLUE
R100 150R2F-1-GP
R101 150R2F-1-GP
R102 150R2F-1-GP

091009-1

+5VS_CRT
C231 SCD1U16V2KX-3GP

46 VGA_HSYNC
46 VGA_VSYNC

U3 74AHCT1G125GW-1-GP
U4 74AHCT1G125GW-1-GP

HSYNC_5
VSYNC_5

SRN33J-5-GP-U RN12
JVGA_HS
JVGA_VS

Hsync & Vsync level shift

091125-1

+5VS_CRT
DY C1193 SC4D7U10V5ZY-3GP
C220 SCD1U16V2ZY-2GP

Q87 DMP2305U-7-GP
+5VS_CRT_FUSE
F1 FUSE-1D1A6V-4GP-U
69.50007.691
+5VS

091021-1 091019-1

R1248 10KR2J-3-GP
R1249 10KR2J-3-GP
CRTVDD_EN#

+5VS_CRT +5VS_CRT
EC1369 EC1370 SC1K1P50V2KX-1GP
DY

Q88 2N7002E-1-GP
SB_PWRGD 18,30
DY C1194 SCD1U16V2ZY-2GP

CRT1
VCC_CRT
NC#4 NC#11
DDC_CRT_DAT
DDC_CRT_CLK
DDCDATA_ID1
DDCCLK_ID3
CRT_R
CRT_G
CRT_B
CRT_RED
CRT_GREEN
CRT_BLUE
JVGA_VS
JVGA_HS
VSYNC
HSYNC
GND
D-SUB-15-27-GP-U2

DY DY C230 C229 SC22P50V2JN-4GP
DY DY C227 C228 SC33P50V2JN-3GP

0803??
0804 check ok

AFTE14P-GP AFTP82 CRT_R
AFTE14P-GP AFTP85 CRT_G
AFTE14P-GP AFTP86 CRT_B
AFTE14P-GP AFTP87 GND
AFTE14P-GP AFTP88 +5VS_CRT

+5VS_CRT
RN11 SRN4K7J-8-GP
DDC_CRT_DAT 46
DDC_CRT_CLK 46

DDC_CRT_DAT& DDC_CRT_CLK
The signal is 5V-tolerant on RS880M.

ESD
close to connector

+5VS_CRT
CRT_R
D3 BAV99-8-GP

+5VS_CRT
D5 BAV99S-GP
DDC_CRT_CLK
DDC_CRT_DAT

+5VS_CRT
D6 BAV99S-GP
CRT_B
CRT_G

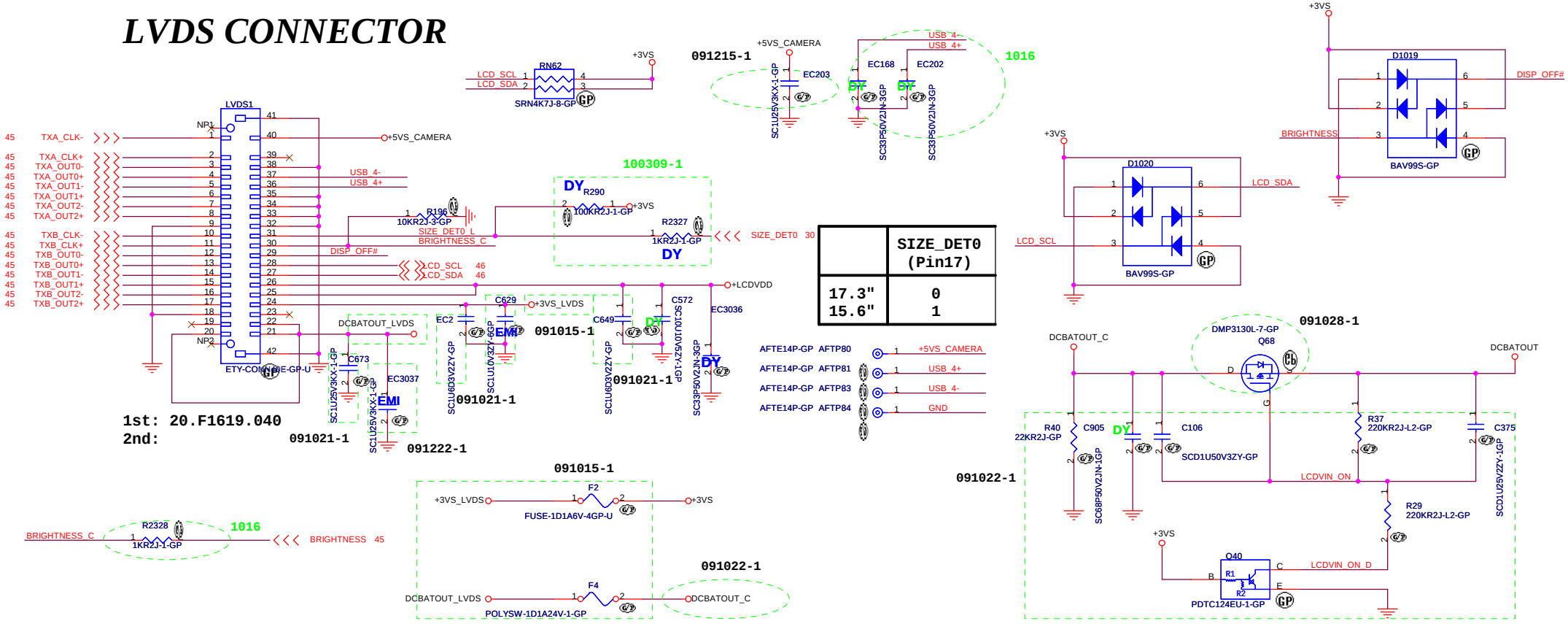
+5VS_CRT
D4 BAV99S-GP
JVGA_HS
JVGA_VS

<Core Design>

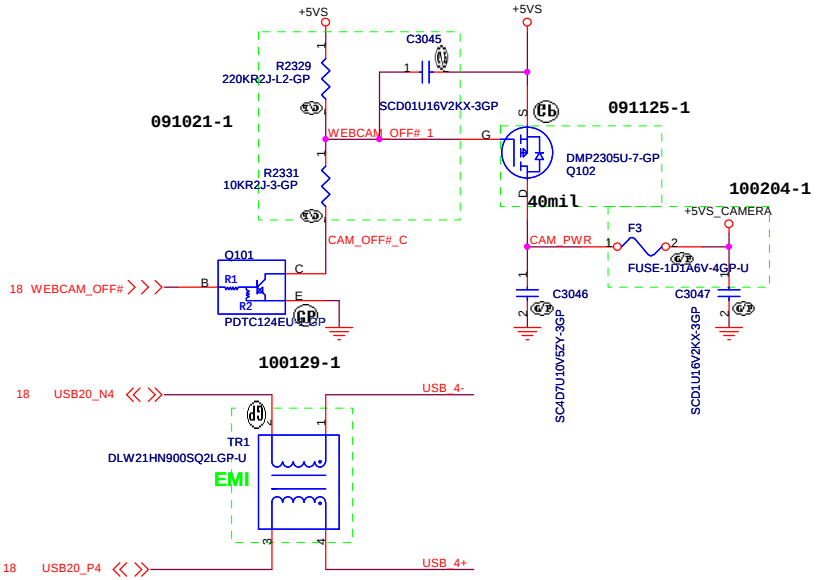
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CRT CONNECTOR
Size: A3
Document Number: PATEK
Rev: SA
Date: Monday, March 15, 2010
Sheet 13 of 57

LVDS CONNECTOR

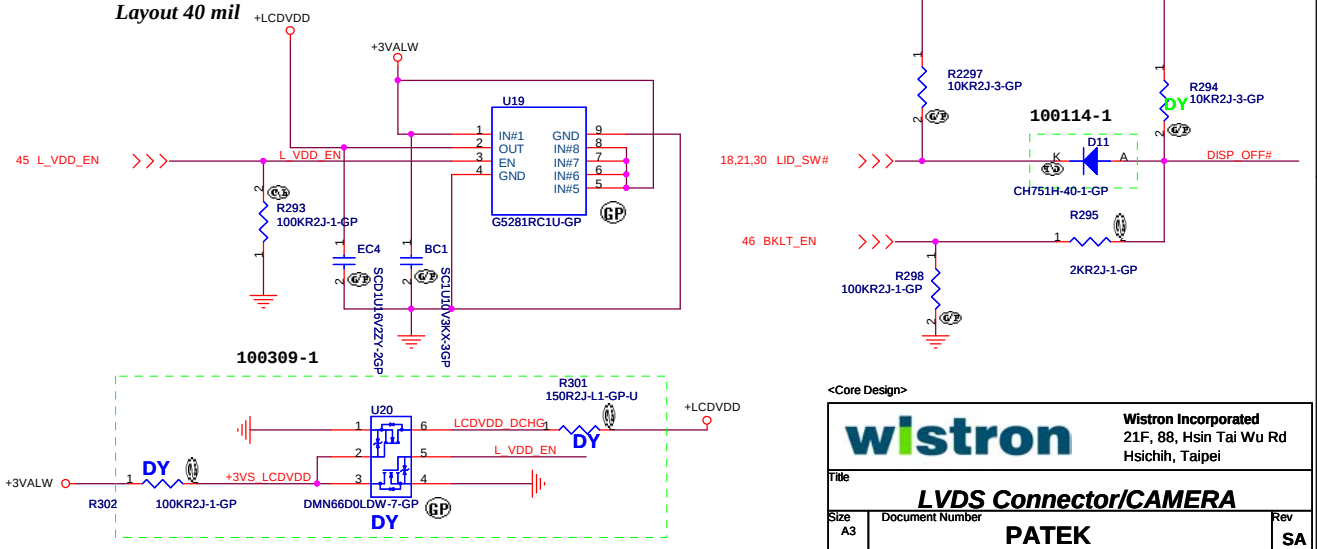


Camera Power&Interface



LCD Power&Discharge

Layout 40 mil



<Core Design>

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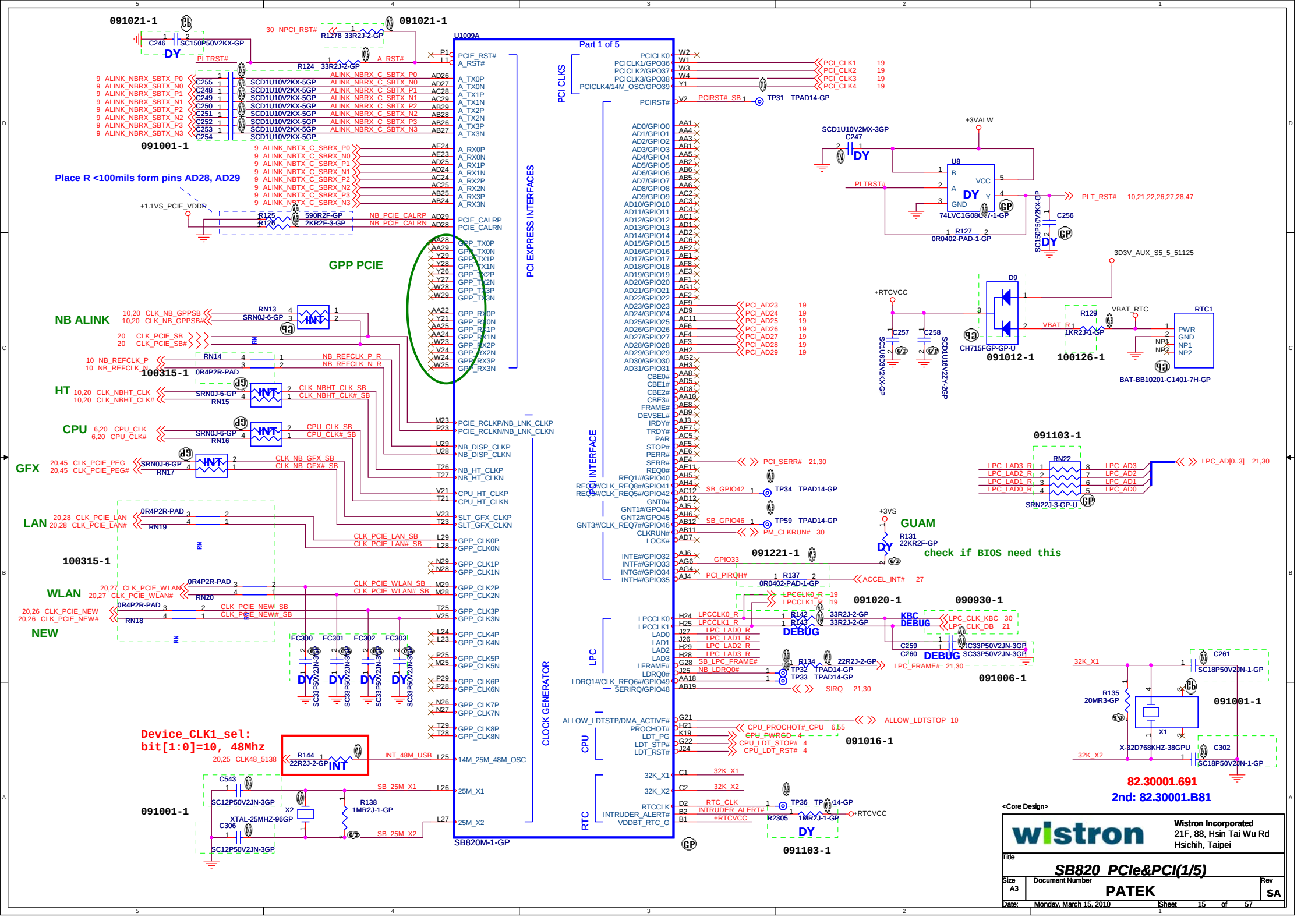
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LVDS Connector/CAMERA

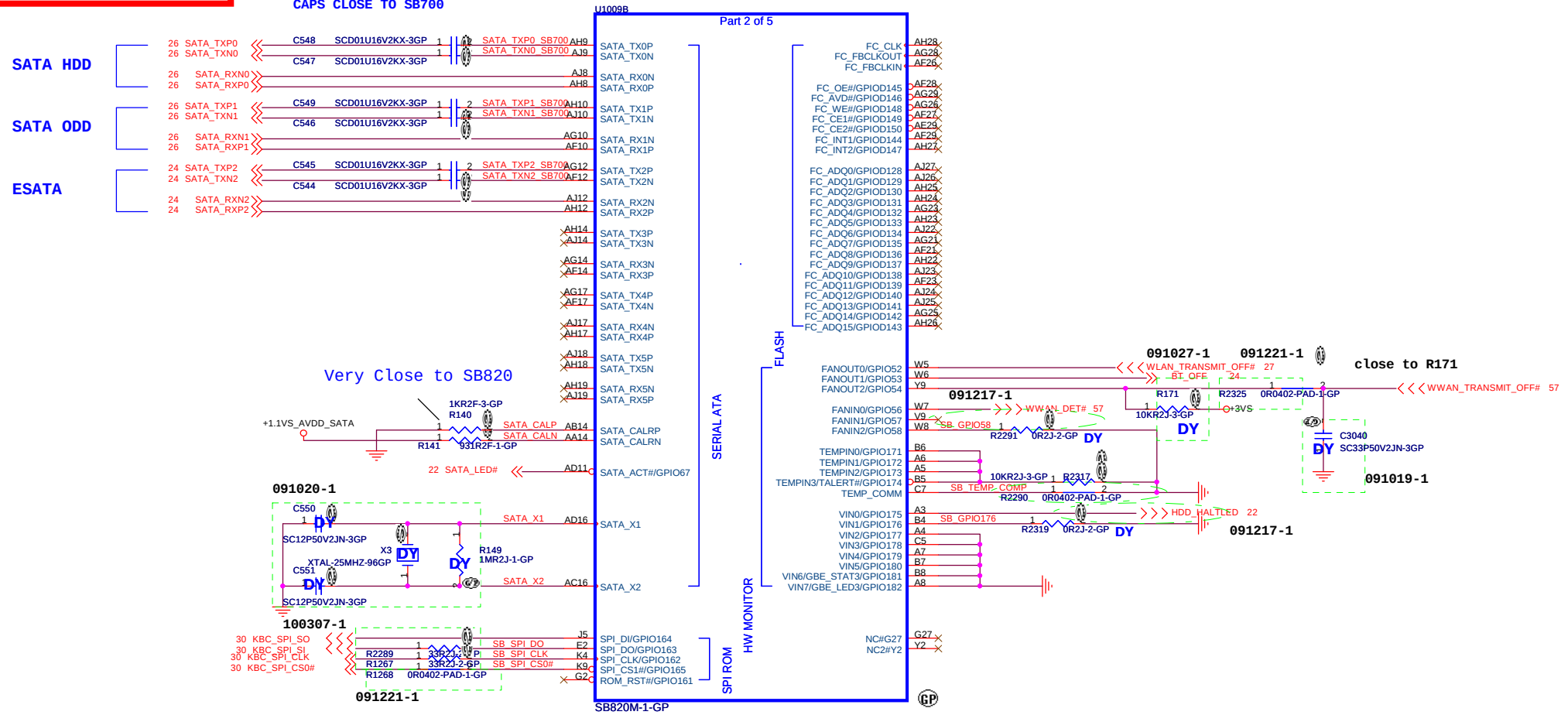
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 14 of 57


091021-1
C246
SC150P50V2KX-GP
DY
PLTRST#
30 NPCI_RST#
R1278 33R2J-2-GP
091021-1
R124 33R2J-2-GP
A_RST#
U1009A
Part 1 of 5
PCIE_RST#
A_RST#
9 ALINK_NBRX_SBTX_P0
9 ALINK_NBRX_SBTX_N0
9 ALINK_NBRX_SBTX_P1
9 ALINK_NBRX_SBTX_N1
9 ALINK_NBRX_SBTX_P2
9 ALINK_NBRX_SBTX_N2
9 ALINK_NBRX_SBTX_P3
9 ALINK_NBRX_SBTX_N3
C255 SCD1U10V2KX-5GP
C248 SCD1U10V2KX-5GP
C249 SCD1U10V2KX-5GP
C250 SCD1U10V2KX-5GP
C251 SCD1U10V2KX-5GP
C252 SCD1U10V2KX-5GP
C253 SCD1U10V2KX-5GP
C254 SCD1U10V2KX-5GP
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
AD26 AD27 AC28 AC29 AB29 AB28 AB26 AB27
A_TX0P A_TX0N A_TX1P A_TX1N A_TX2P A_TX2N A_TX3P A_TX3N
091001-1
9 ALINK_NBTX_C_SBRX_P0
9 ALINK_NBTX_C_SBRX_N0
9 ALINK_NBTX_C_SBRX_P1
9 ALINK_NBTX_C_SBRX_N1
9 ALINK_NBTX_C_SBRX_P2
9 ALINK_NBTX_C_SBRX_N2
9 ALINK_NBTX_C_SBRX_P3
9 ALINK_NBTX_C_SBRX_N3
AE24 AE23 AD25 AD24 AC24 AC25 AB25 AB24
A_RX0P A_RX0N A_RX1P A_RX1N A_RX2P A_RX2N A_RX3P A_RX3N
Place R <100mils form pins AD28, AD29
+1.1VS_PCIE_VDDR
R125 590R2F-GP
R126 2KR2F-3-GP
NB_PCIE_CALRP AD29
NB_PCIE_CALRN AD28
PCIE_CALRP
PCIE_CALRN
PCI EXPRESS INTERFACES
GPP PCIE
AA28 GPP_TX0P
AA29 GPP_TX0N
Y29 GPP_TX1P
Y28 GPP_TX1N
Y26 GPP_TX2P
Y27 GPP_TX2N
W28 GPP_TX3P
W29 GPP_TX3N
AA22 GPP_RX0P
Y21 GPP_RX0N
AA25 GPP_RX1P
AA24 GPP_RX1N
W23 GPP_RX2P
Y24 GPP_RX2N
W24 GPP_RX3P
W25 GPP_RX3N
NB ALINK
10,20 CLK_NB_GPPSB
10,20 CLK_NB_GPPSB#
RN13 SRN0J-6-GP
20 CLK_PCIE_SB
20 CLK_PCIE_SB#
RN14 0R4P2R-PAD
10 NB_REFCLK_P
10 NB_REFCLK_N
NB_REFCLK_P_R
NB_REFCLK_N_R
100315-1
HT
10,20 CLK_NBHT_CLK
10,20 CLK_NBHT_CLK#
SRN0J-6-GP RN15
CLK_NBHT_CLK_SB
CLK_NBHT_CLK#_SB
CPU
6,20 CPU_CLK
6,20 CPU_CLK#
SRN0J-6-GP RN16
CPU_CLK_SB
CPU_CLK#_SB
GFX
20,45 CLK_PCIE_PEG
20,45 CLK_PCIE_PEG#
SRN0J-6-GP RN17
CLK_NB_GFX_SB
CLK_NB_GFX#_SB
M23 PCIE_RCLKP/NB_LNK_CLKP
P23 PCIE_RCLKN/NB_LNK_CLKN
U29 NB_DISP_CLKP
U28 NB_DISP_CLKN
T26 NB_HT_CLKP
T27 NB_HT_CLKN
V21 CPU_HT_CLKP
T21 CPU_HT_CLKN
V23 SLT_GFX_CLKP
T23 SLT_GFX_CLKN
LAN
20,28 CLK_PCIE_LAN
20,28 CLK_PCIE_LAN#
0R4P2R-PAD RN19
CLK_PCIE_LAN_SB
CLK_PCIE_LAN#_SB
L29 GPP_CLK0P
L28 GPP_CLK0N
100315-1
WLAN
20,27 CLK_PCIE_WLAN
20,27 CLK_PCIE_WLAN#
0R4P2R-PAD RN20
CLK_PCIE_WLAN_SB
CLK_PCIE_WLAN#_SB
N29 GPP_CLK1P
N28 GPP_CLK1N
M29 GPP_CLK2P
M28 GPP_CLK2N
NEW
20,26 CLK_PCIE_NEW
20,26 CLK_PCIE_NEW#
0R4P2R-PAD RN18
CLK_PCIE_NEW_SB
CLK_PCIE_NEW#_SB
T25 GPP_CLK3P
V25 GPP_CLK3N
EC300 EC301 EC302 EC303
SC33P50V2JN-3GP
L24 GPP_CLK4P
L23 GPP_CLK4N
P25 GPP_CLK5P
M25 GPP_CLK5N
P29 GPP_CLK6P
P28 GPP_CLK6N
N26 GPP_CLK7P
N27 GPP_CLK7N
T29 GPP_CLK8P
T28 GPP_CLK8N
CLOCK GENERATOR
Device_CLK1_sel:
bit[1:0]=10, 48Mhz
R144 22R2J-2-GP
20,25 CLK48_5138
INT_48M_USB
L25 14M_25M_48M_OSC
C543 SC12P50V2JN-3GP
X2 XTAL-25MHZ-96GP
C306 SC12P50V2JN-3GP
R138 1MR2J-1-GP
SB_25M_X1
SB_25M_X2
L26 25M_X1
L27 25M_X2
091001-1
SB820M-1-GP
PCI CLKS
PCICLK0 W2
PCICLK1/GPO36 W1
PCICLK2/GPO37 W3
PCICLK3/GPO38 W4
PCICLK4/14M_OSC/GPO39 Y1
PCI_CLK1 19
PCI_CLK2 19
PCI_CLK3 19
PCI_CLK4 19
PCIRST# V2
PCIRST#_SB
TP31 TPAD14-GP
PCI INTERFACE
AD0/GPIO0 AA1
AD1/GPIO1 AA4
AD2/GPIO2 AA3
AD3/GPIO3 AB1
AD4/GPIO4 AA5
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1
AD22/GPIO22 AF2
AD23/GPIO23 AE9
AD24/GPIO24 AD9
AD25/GPIO25 AC11
AD26/GPIO26 AF6
AD27/GPIO27 AF4
AD28/GPIO28 AF3
AD29/GPIO29 AH2
AD30/GPIO30 AG2
AD31/GPIO31 AH3
CBE0# AA8
CBE1# AD5
CBE2# AD8
CBE3# AA10
FRAME# AE8
DEVSEL# AB9
IRDY# AJ3
TRDY# AE7
PAR AC5
STOP# AF5
PERR# AE6
SERR# AE4
REQ0# AE11
REQ1#/GPIO40 AH5
REQ2#/CLK_REQ8#/GPIO41 AH4
REQ3#/CLK_REQ5#/GPIO42 AC12
GNT0# AD12
GNT1#/GPO44 AJ5
GNT2#/GPO45 AH6
GNT3#/CLK_REQ7#/GPIO46 AB12
CLKRUN# AB11
LOCK# AD7
INTE#/GPIO32 AJ6
INTF#/GPIO33 AG6
INTG#/GPIO34 AG4
INTH#/GPIO35 AJ4
PCI_AD23 19
PCI_AD24 19
PCI_AD25 19
PCI_AD26 19
PCI_AD27 19
PCI_AD28 19
PCI_AD29 19
PCI_SERR# 21,30
SB_GPIO42
TP34 TPAD14-GP
SB_GPIO46
TP59 TPAD14-GP
PM_CLKRUN# 30
GPIO33
PCI_PIRQH#
R137 0R0402-PAD-1-GP
ACCEL_INT# 27
091221-1
LPC
LPCCLK0 H24
LPCCLK1 H25
LAD0 J27
LAD1 J26
LAD2 H29
LAD3 H28
LFRAME# G28
LDRQ0# J25
LDRQ1#/CLK_REQ6#/GPIO49 AA18
SERIRQ/GPIO48 AB19
LPCCLK0_R 19
LPCCLK1_R 19
091020-1
090930-1
R142 33R2J-2-GP
R143 33R2J-2-GP
DEBUG
KBC
LPC_CLK_KBC 30
LPC_CLK_DB 21
C259 SC33P50V2JN-3GP
C260 SC33P50V2JN-3GP
LPC_LAD0_R
LPC_LAD1_R
LPC_LAD2_R
LPC_LAD3_R
SB_LPC_FRAME#
NB_LDRQ0#
R134 22R2J-2-GP
TP32 TPAD14-GP
TP33 TPAD14-GP
LPC_FRAME# 21,30
SIRQ 21,30
091006-1
CPU
ALLOW_LDTSTP/DMA_ACTIVE# G21
PROCHOT# H21
LDT_PG K19
LDT_STP# G22
LDT_RST# J24
CPU_PROCHOT#_CPU 6,55
CPU_PWRGD 4
CPU_LDT_STOP# 4
CPU_LDT_RST# 4
ALLOW_LDTSTOP 10
091016-1
RTC
32K_X1 C1
32K_X2 C2
RTCCLK D2
INTRUDER_ALERT# B2
VDDBT_RTC_G B1
RTC_CLK
INTRUDER_ALERT#
+RTCVCC
TP36 TPAD14-GP
R2305 1MR2J-1-GP
091103-1
SCD1U10V2MX-3GP C247
+3VALW
U8
74LVC1G08GW-1-GP
PLT_RST# 10,21,22,26,27,28,47
R127 0R0402-PAD-1-GP
C256
SC150P50V2KX-GP
3D3V_AUX_S5_5_51125
+RTCVCC
D9
CH715FGP-GP-U
VBAT_R
R129 1KR2J-1-GP
VBAT_RTC
RTC1
BAT-BB10201-C1401-7H-GP
C257 SCU16D3V2KX-GP
C258 SCD1U16V2ZY-2GP
091012-1
100126-1
091103-1
RN22 SRN22J-3-GP-U
LPC_LAD3_R
LPC_LAD2_R
LPC_LAD1_R
LPC_LAD0_R
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
LPC_AD[0..3] 21,30
+3VS
GUAM
R131 22KR2F-GP
check if BIOS need this
32K_X1
32K_X2
C261 SC18P50V2JN-1-GP
R135 20MR3-GP
X1
X-32D768KHZ-38GPU
C302 SC18P50V2JN-1-GP
091001-1
82.30001.691
2nd: 82.30001.B81
<Core Design>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
SB820 PCIe&PCI(1/5)
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
Sheet 15 of 57

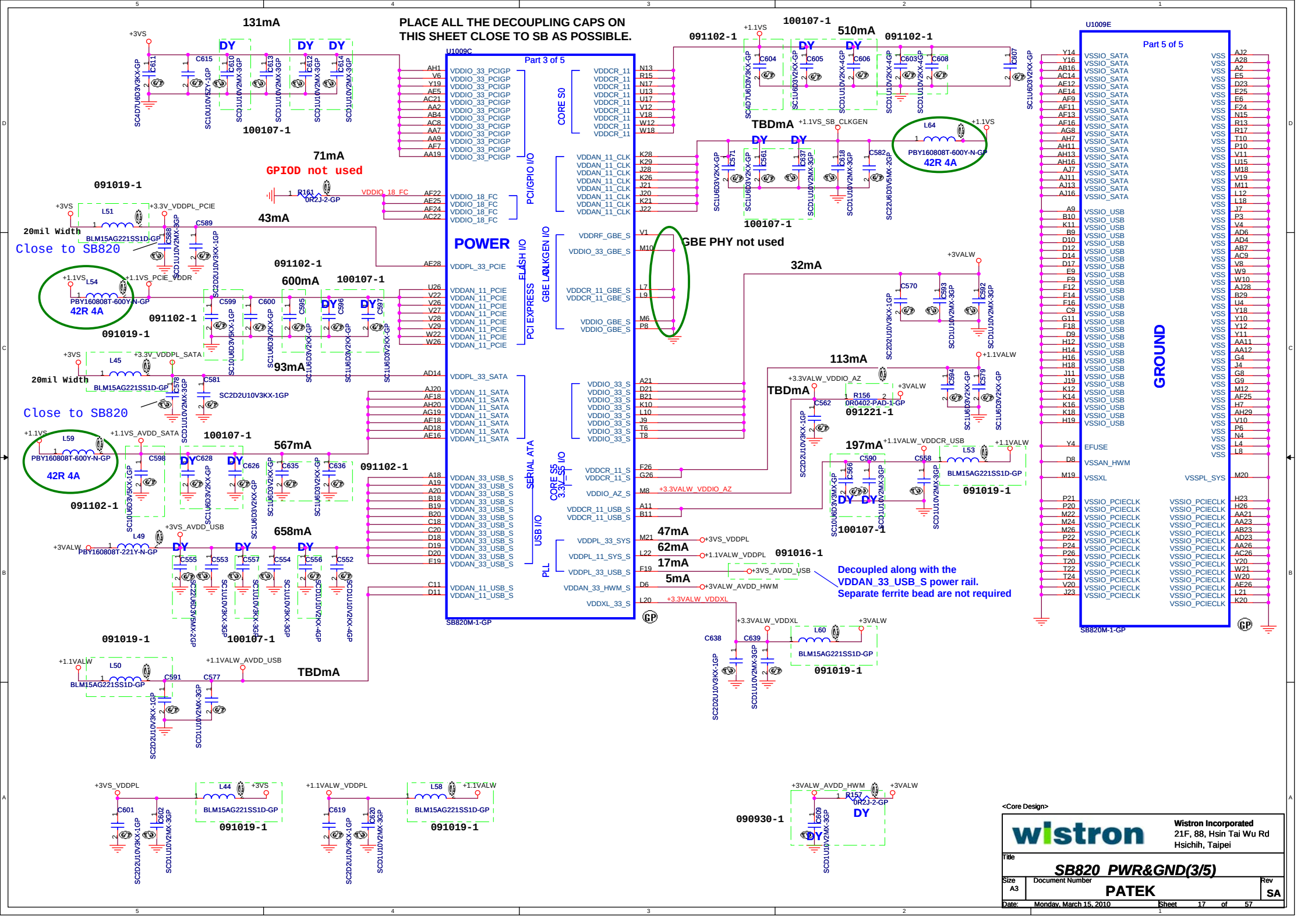
SSID = S.B

PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



<Core Design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	SB820 SATA&IDE(2/5)
Size A3	Document Number PATEK
Rev	SA
Date: Monday, March 15, 2010	Sheet 16 of 57


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
U1009C
Part 3 of 5
POWER
CORE S0
PCI/GPIO I/O
FLASH I/O
GBE LAN/KGEN I/O
PCI EXPRESS
SERIAL ATA
CORE SS
3.3V_SS I/O
USB I/O
PLL
SB820M-1-GP
U1009E
Part 5 of 5
GROUND
131mA
71mA
GPIOD not used
43mA
600mA
93mA
567mA
658mA
TBDmA
510mA
32mA
113mA
197mA
47mA
62mA
17mA
5mA
GBE PHY not used
Close to SB820
20mil Width
42R 4A
Decoupled along with the VDDAN_33_USB_S power rail.
Separate ferrite bead are not required
<Core Design>
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
SB820 PWR&GND(3/5)
Size A3
Document Number PATEK
Rev SA
Date: Monday, March 15, 2010
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SSID = S.B

Part 4 of 5

U1009D

SB820M-1-GP

Internal 10K PU

Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

USB-FSD1 FPR

USB-9 Bluetooth

USB-8 WLAN

USB-7 WWAN

USB-6 USB Card Reader

USB-5 Right Side

USB-4 USB Camera

USB-3 Right Side

USB-2 Left Side (e-SATA combo)

USB-1 New Card

USB-0 Left Side (S/W Debug port)

Need to check leakage

Strap Pin / define to use LPC or SPI ROM

Low Power Mode

Performance Mode

<Core Design>

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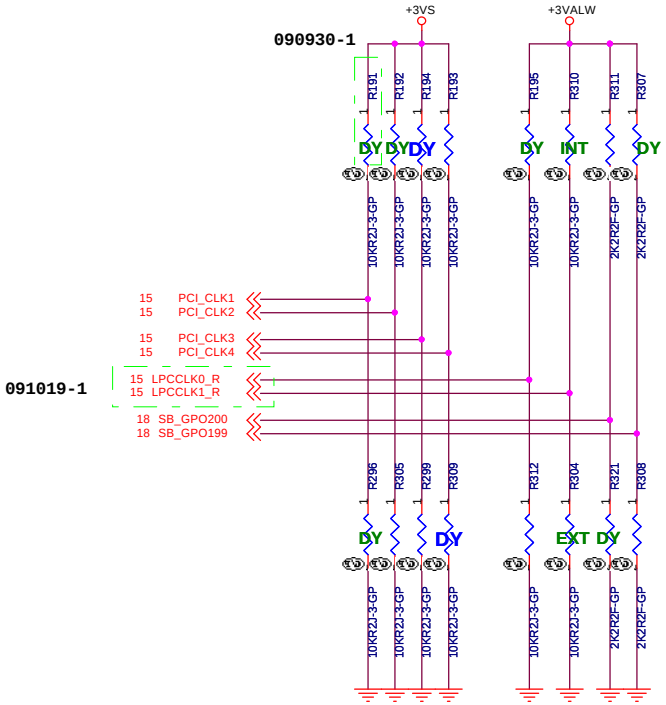
Title	SB820 USB&GPIO(4/5)
Size A3	Document Number PATEK
Rev	SA
Date: Monday, March 15, 2010	Sheet 18 of 57

REQUIRED STRAPS

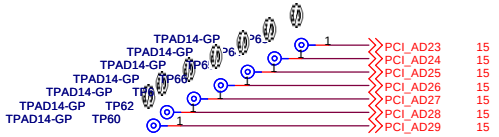


USE this pin to determine INT/EXT CLK

091020-1

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPCCLK0_R (LPCCLK0)	LPCCLK1_R (LPCCLK1)	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	L, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

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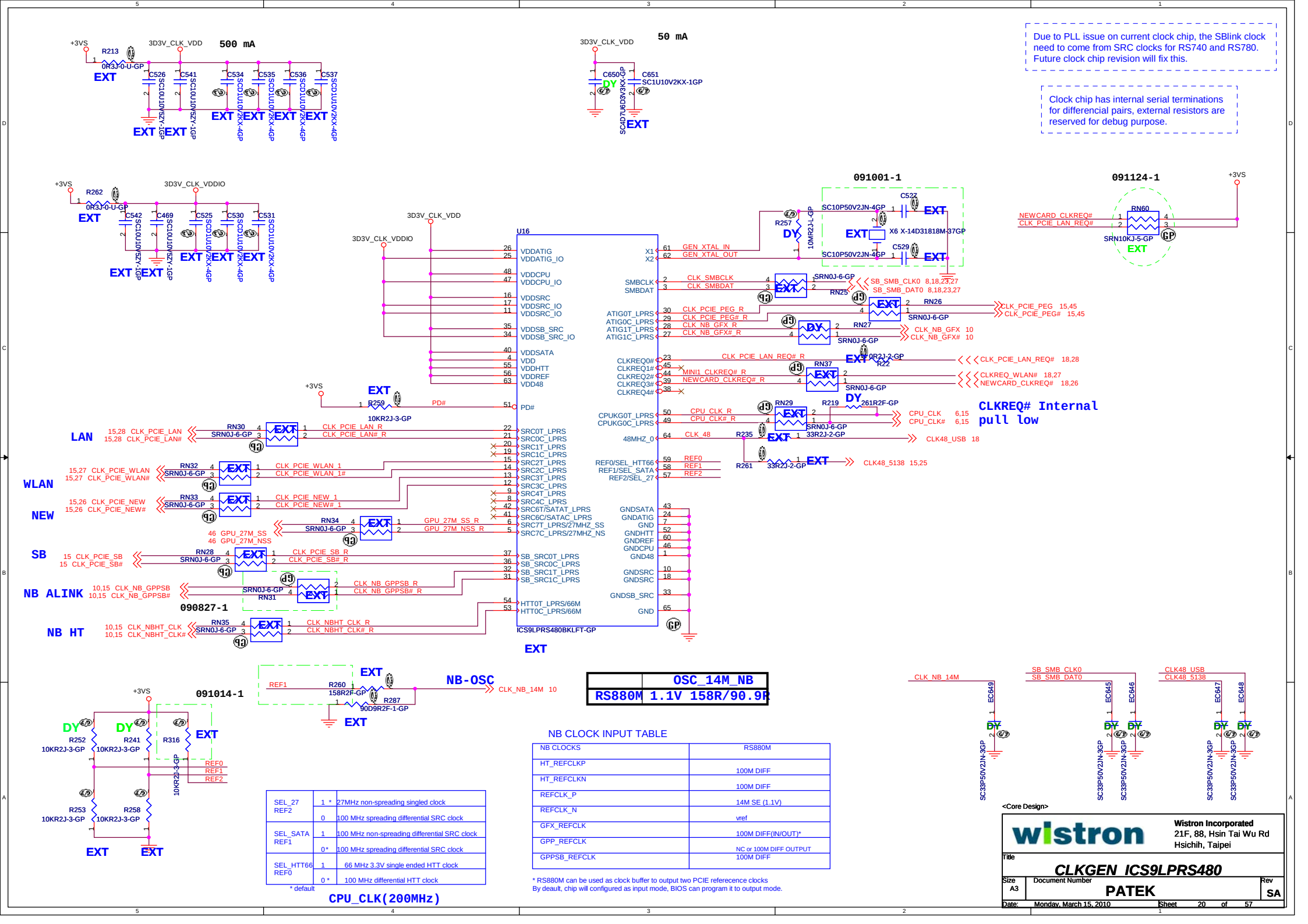
Hsichih, Taipei

Title: *SB820 STRAPPING(5/5)*

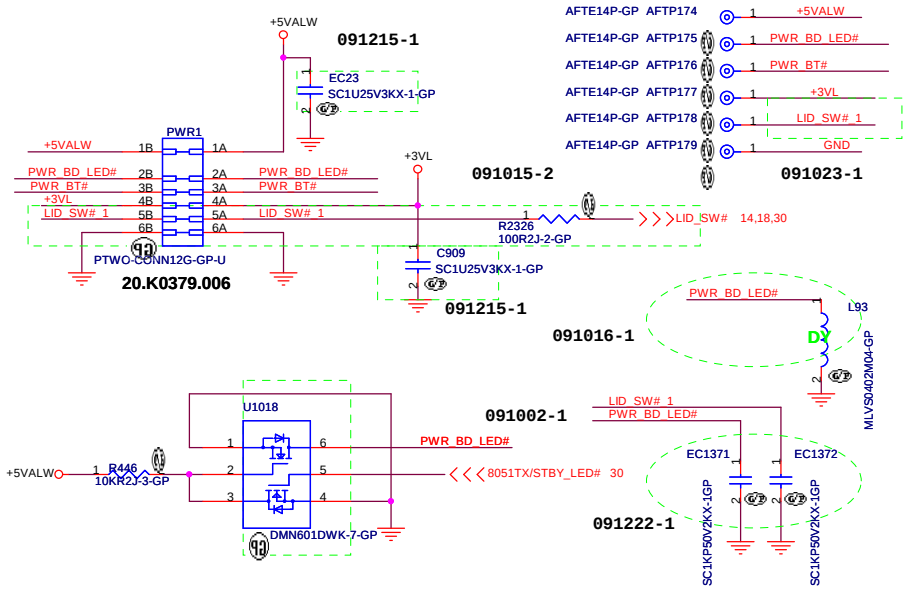
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 19 of 57

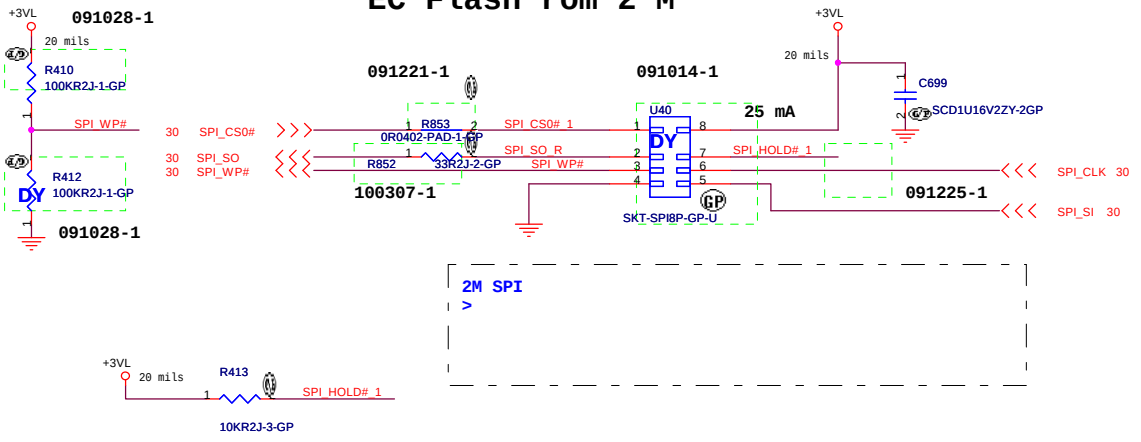

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.
500 mA
50 mA
091001-1
091124-1
090827-1
091014-1
U16
ICS9LPRS480BKLFT-GP
LAN
WLAN
NEW
SB
NB ALINK
NB HT
CLKREQ# Internal pull low
NB-OSC
OSC_14M_NB
RS880M 1.1V 158R/90.9R
NB CLOCK INPUT TABLE
CPU_CLK(200MHz)
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CLKGEN_ICS9LPRS480
PATEK
Monday, March 15, 2010

POWER SW CONN.

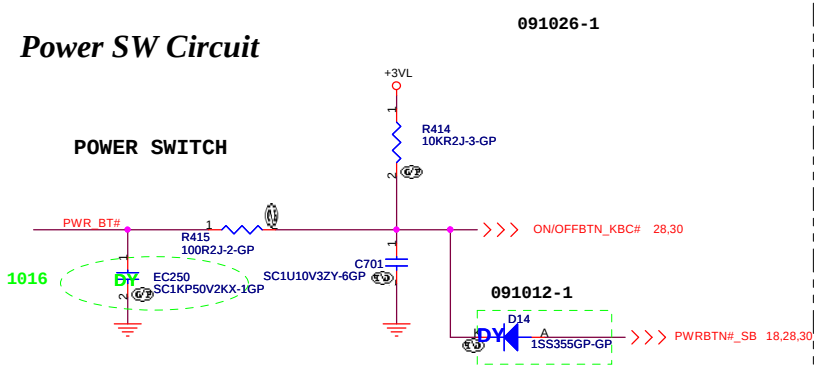
COVER SWITCH

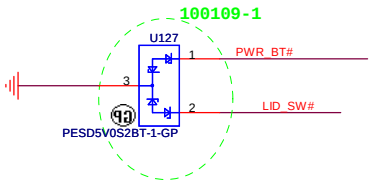


EC Flash rom 2 M

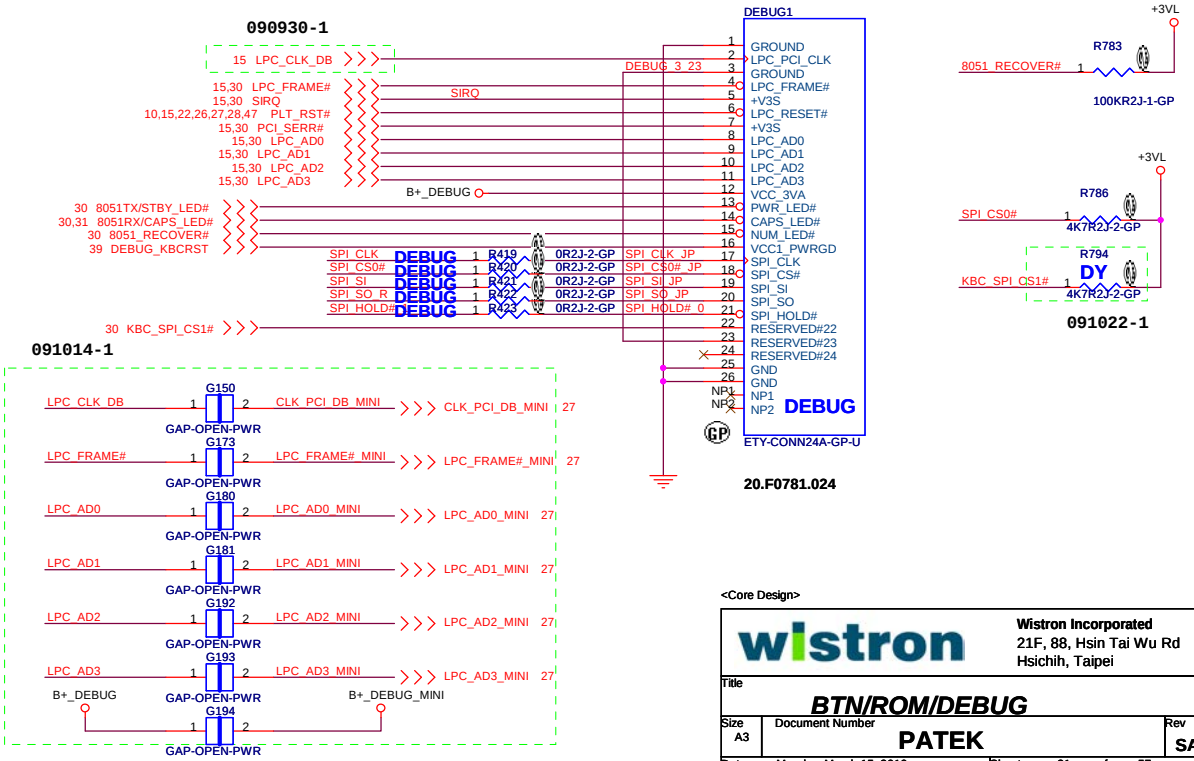


Power SW Circuit





24 PIN LPC DEBUG CONN.



<Core Design>

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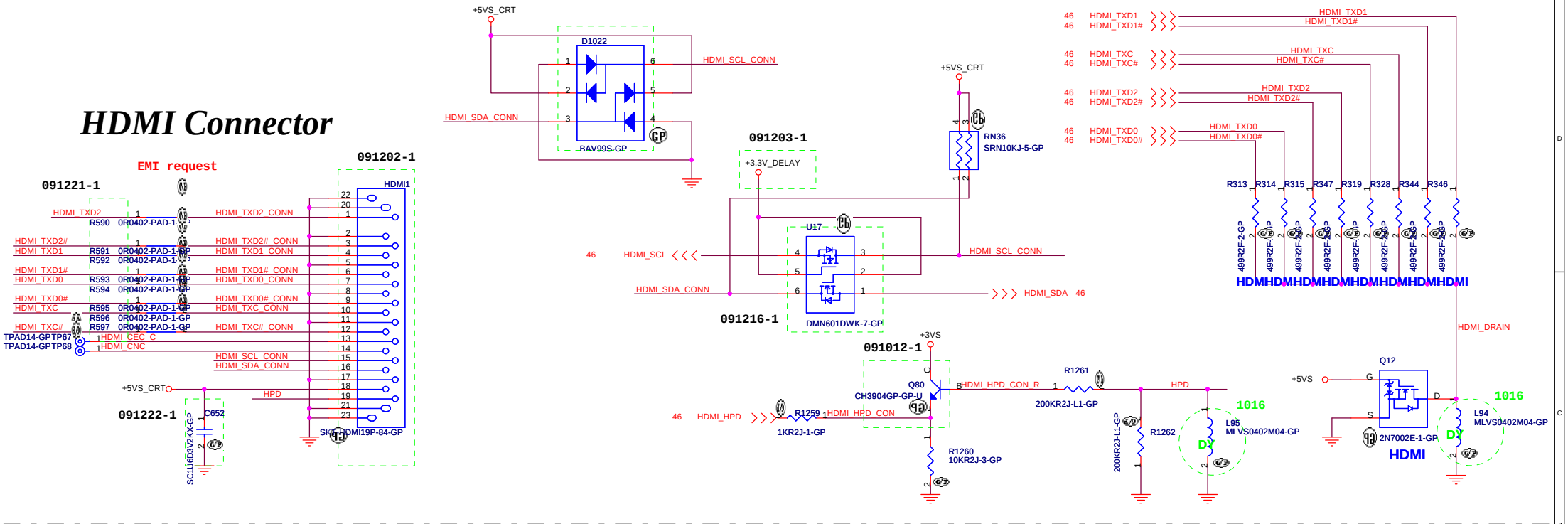
Title: BTN/ROM/DEBUG

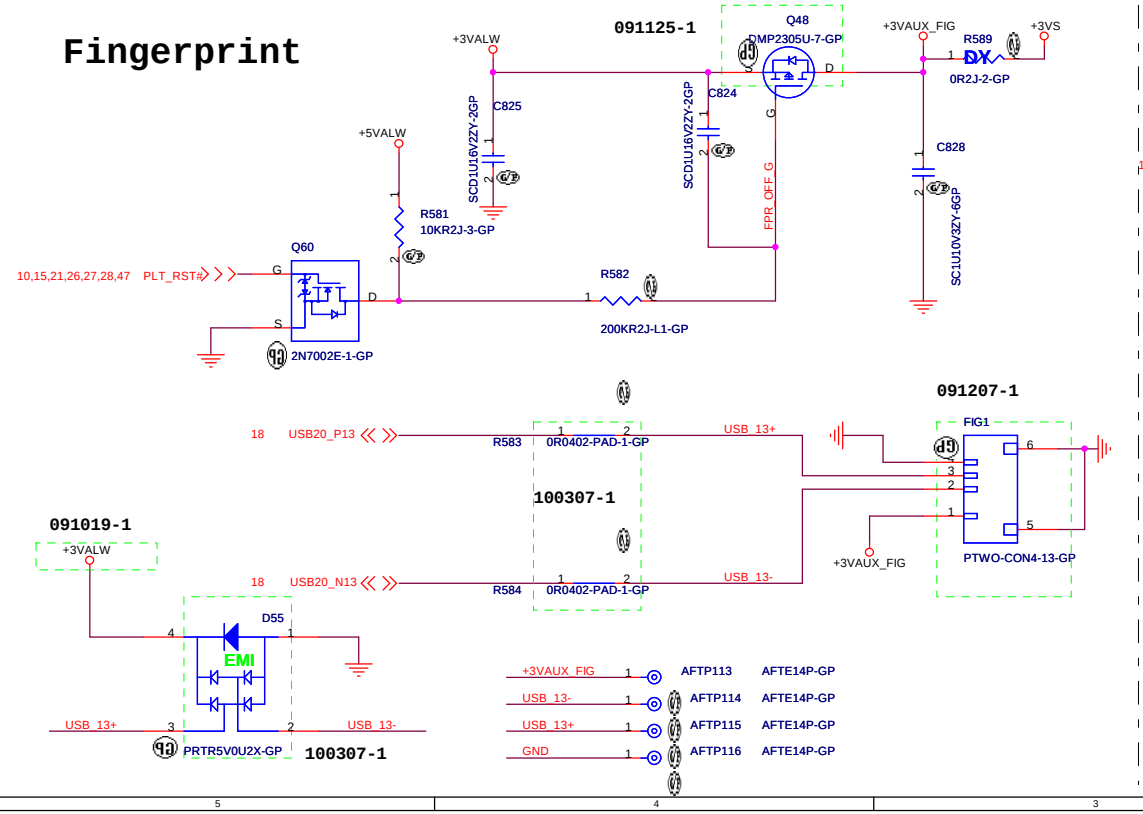
Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 21 of 57

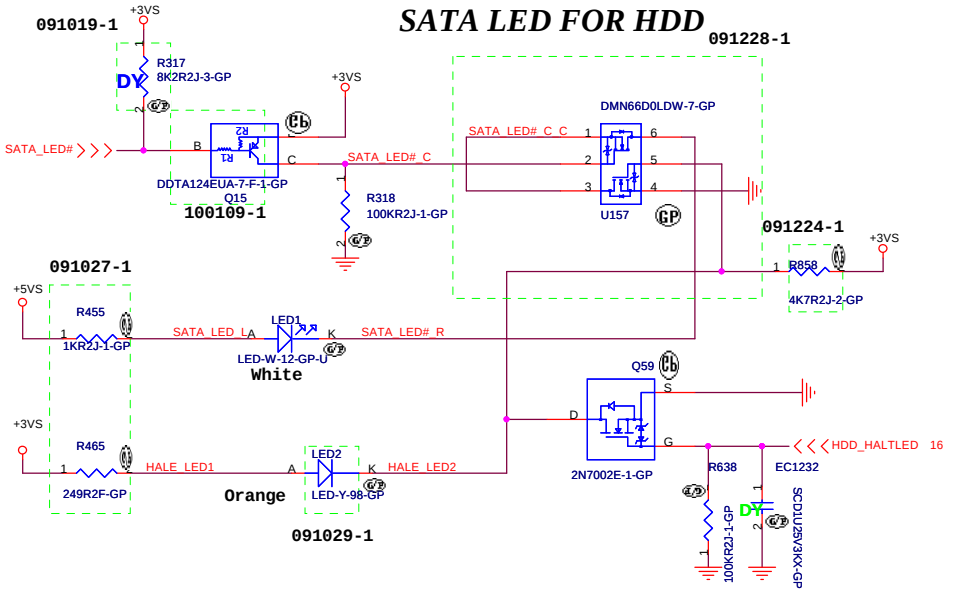
HDMI Connector



Fingerprint



SATA LED FOR HDD



<Core Design>

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Title: HDMI/FPR/SATA LED

Size	Document Number	Rev
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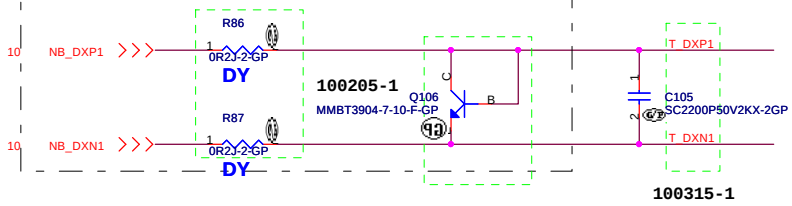
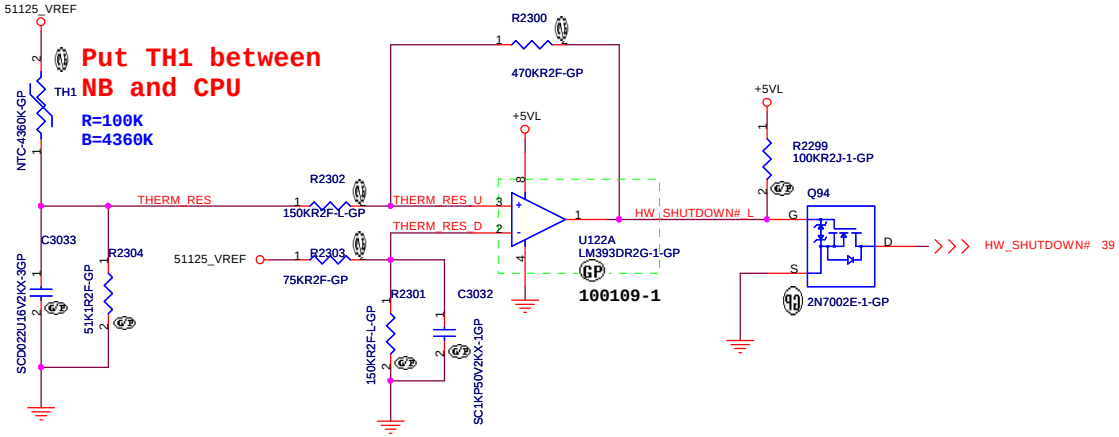
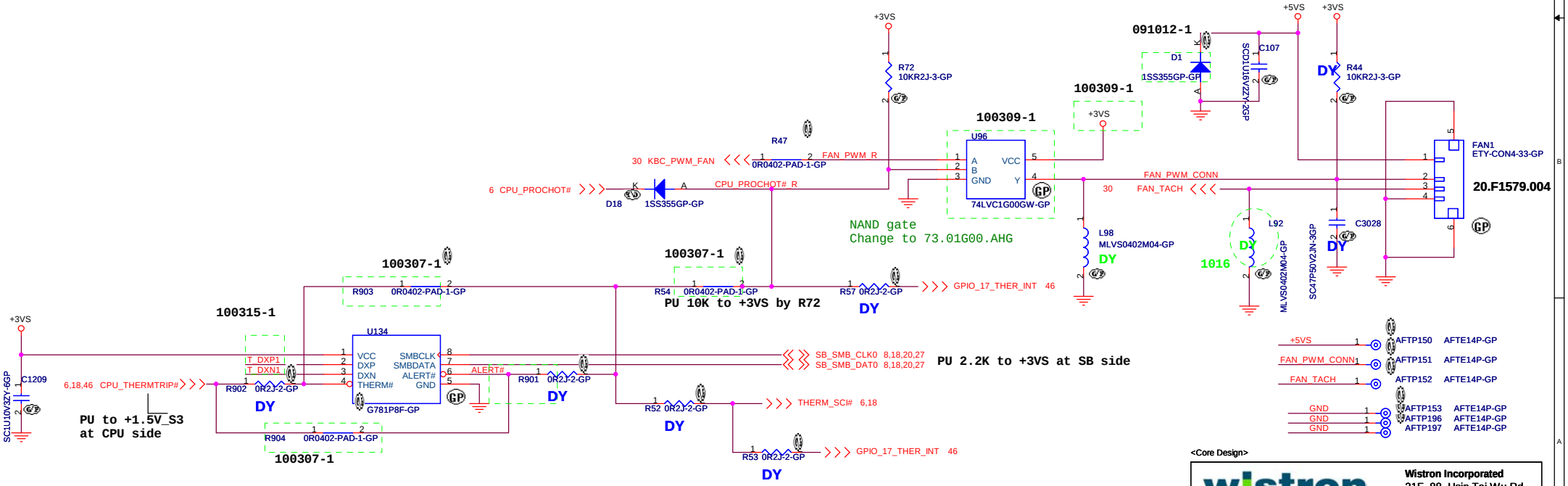
CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal chip.





4 WIRE PWM Fan Control circuit



<Core Design>

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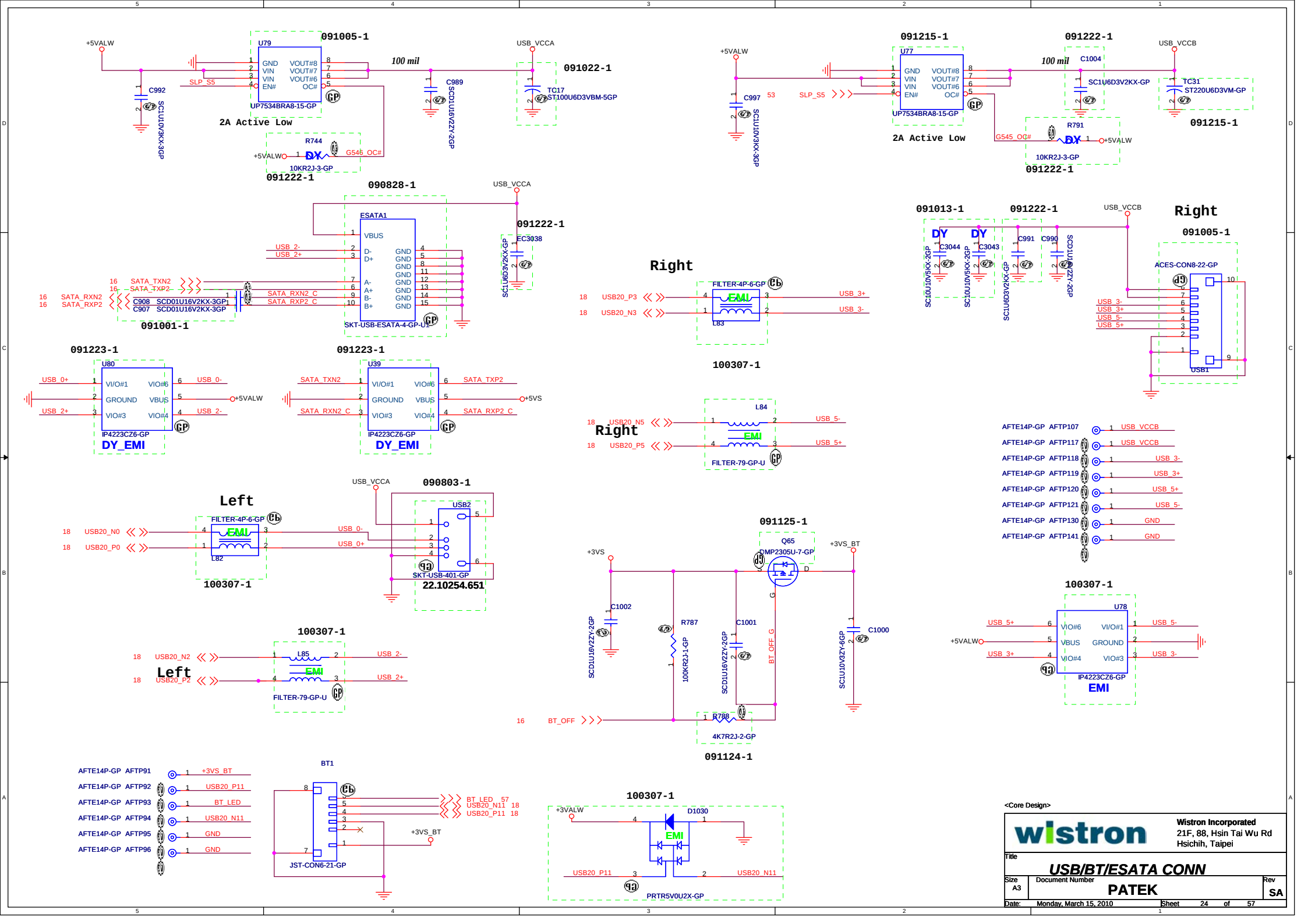
Title: G781P8F THERMAL

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 23 of 57


091005-1
U79
UP7534BRA8-15-GP
2A Active Low
100 mil
091022-1
TC17
ST100U6D3VBM-5GP
091222-1
R744
10KR2J-3-GP
091215-1
U77
C1004
SC1U6D3V2KX-GP
TC31
ST220U6D3VM-GP
R791
10KR2J-3-GP
090828-1
ESATA1
EC3038
SKT-USB-ESATA-4-GP-U1
091001-1
C908 SCD01U16V2KX-3GP1
C907 SCD01U16V2KX-3GP
091223-1
U80
IP4223CZ6-GP
DY_EMI
U39
Right
FILTER-4P-6-GP
L83
100307-1
L84
FILTER-79-GP-U
091013-1
091005-1
ACES-CON8-22-GP
USB1
Left
L82
090803-1
USB2
SKT-USB-401-GP
22.10254.651
L85
091125-1
Q65
DMP2305U-7-GP
R787
100KR2J-1-GP
R788
4K7R2J-2-GP
091124-1
AFTE14P-GP AFTP107
AFTE14P-GP AFTP117
AFTE14P-GP AFTP118
AFTE14P-GP AFTP119
AFTE14P-GP AFTP120
AFTE14P-GP AFTP121
AFTE14P-GP AFTP130
AFTE14P-GP AFTP141
U78
AFTE14P-GP AFTP91
AFTE14P-GP AFTP92
AFTE14P-GP AFTP93
AFTE14P-GP AFTP94
AFTE14P-GP AFTP95
AFTE14P-GP AFTP96
BT1
JST-CON6-21-GP
D1030
PRTR5V0U2X-GP
<Core Design>
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
USB/BT/ESATA CONN
Size A3
Document Number
PATEK
Rev SA
Date: Monday, March 15, 2010
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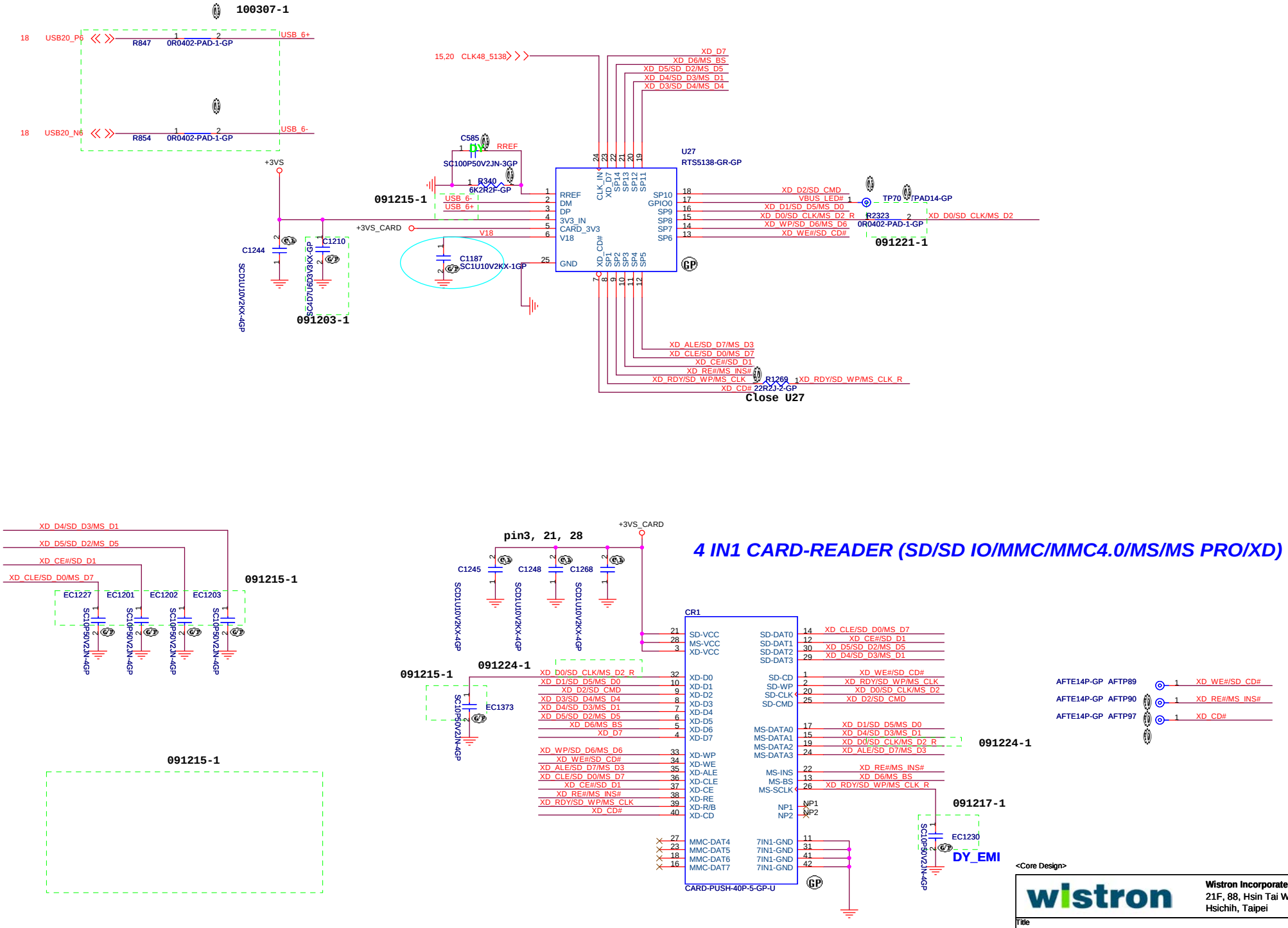

<Core Design>

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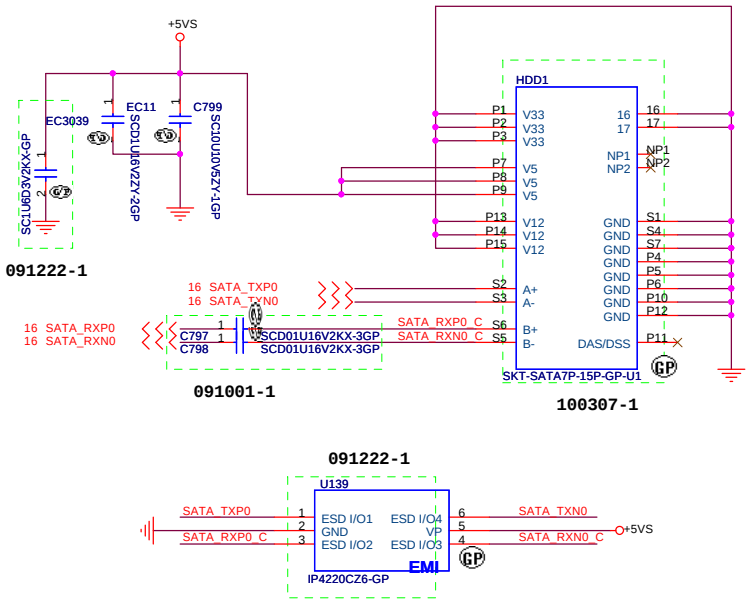
Title: CardReader RTS5138

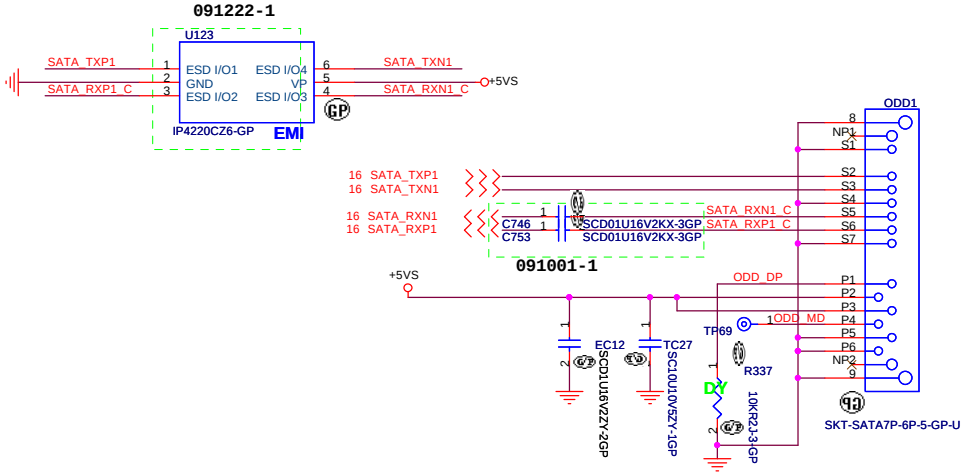
Size	Document Number	Rev
A3	PATEK	SA

Date: Monday, March 15, 2010 Sheet 25 of 57

SATA HD Connector

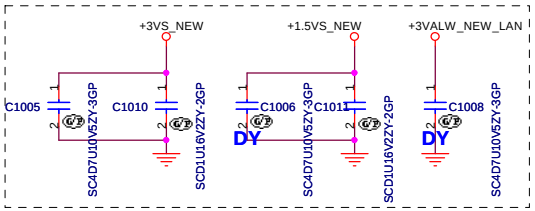


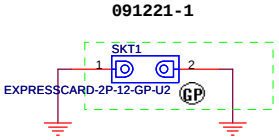
ODD Connector

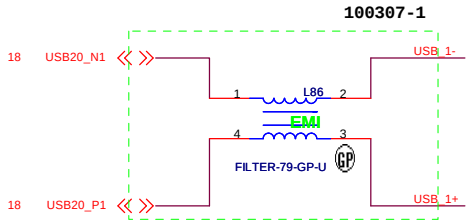


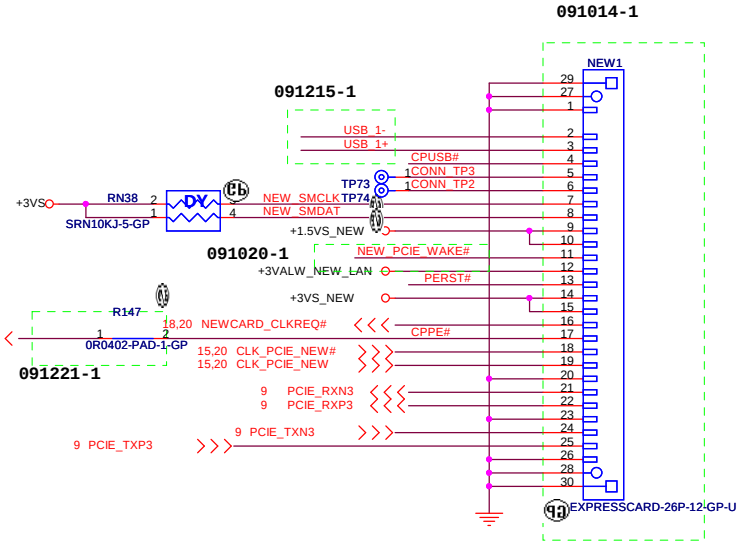
EXPRESS CARD Connector

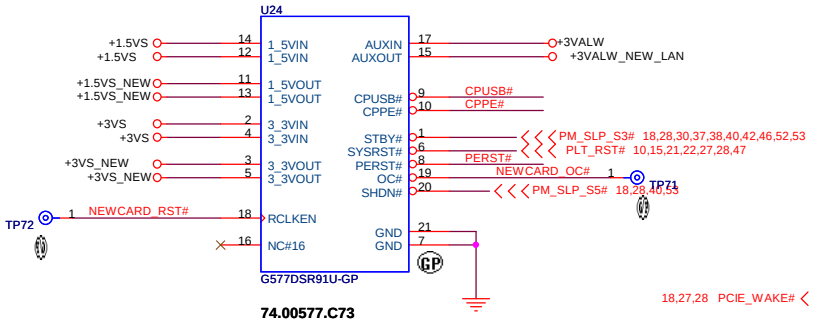
Place them Near to Connector

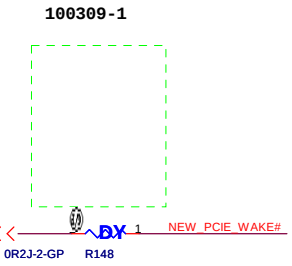


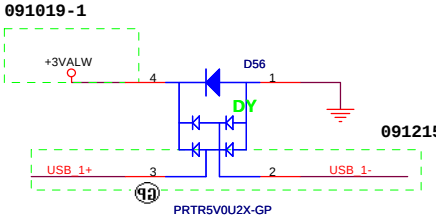












<Core Design>

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Title: HDD/ODD/NEW CARD

Size	Document Number	Rev
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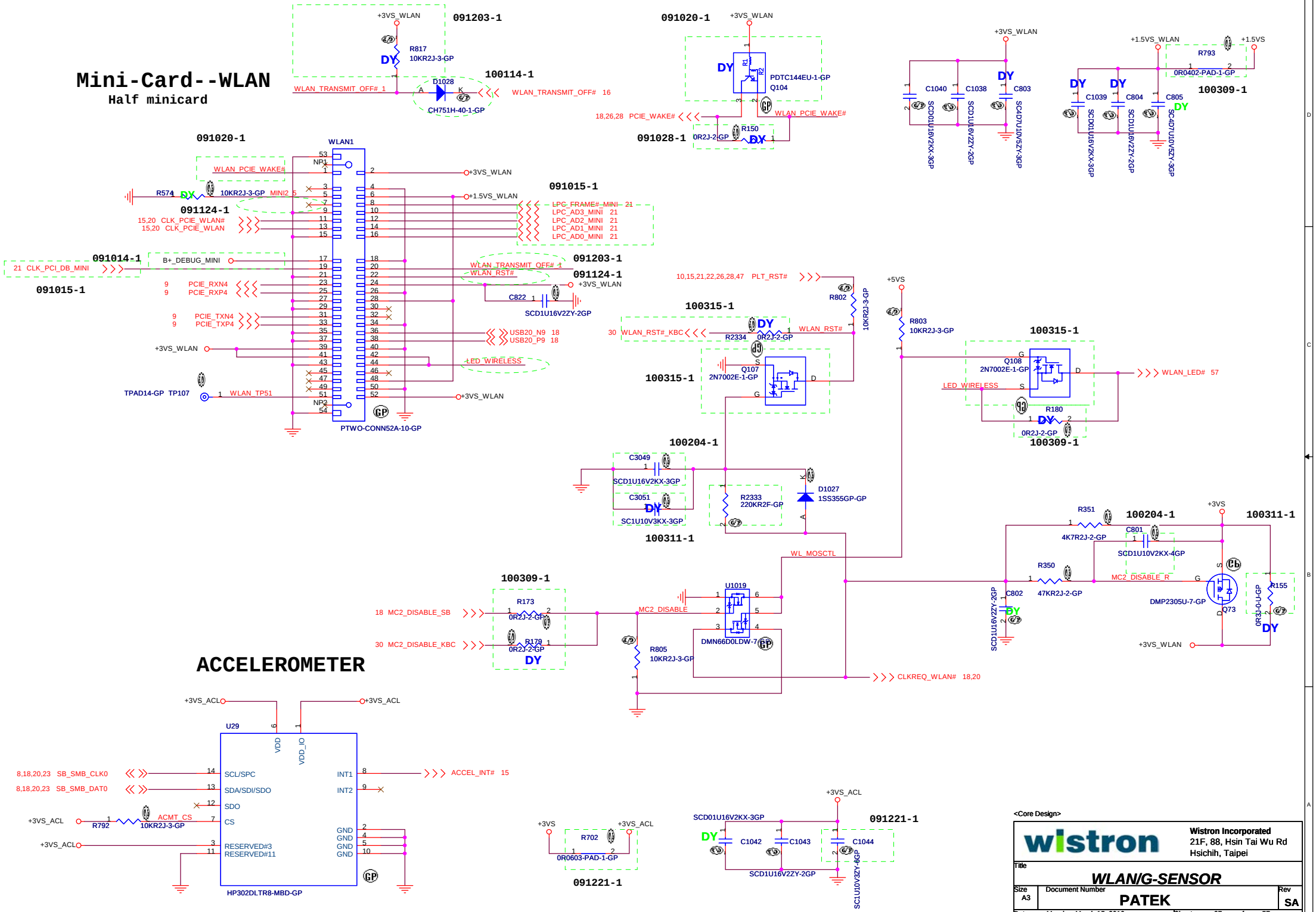
Mini-Card--WLAN

Half minicard



<Core Design>

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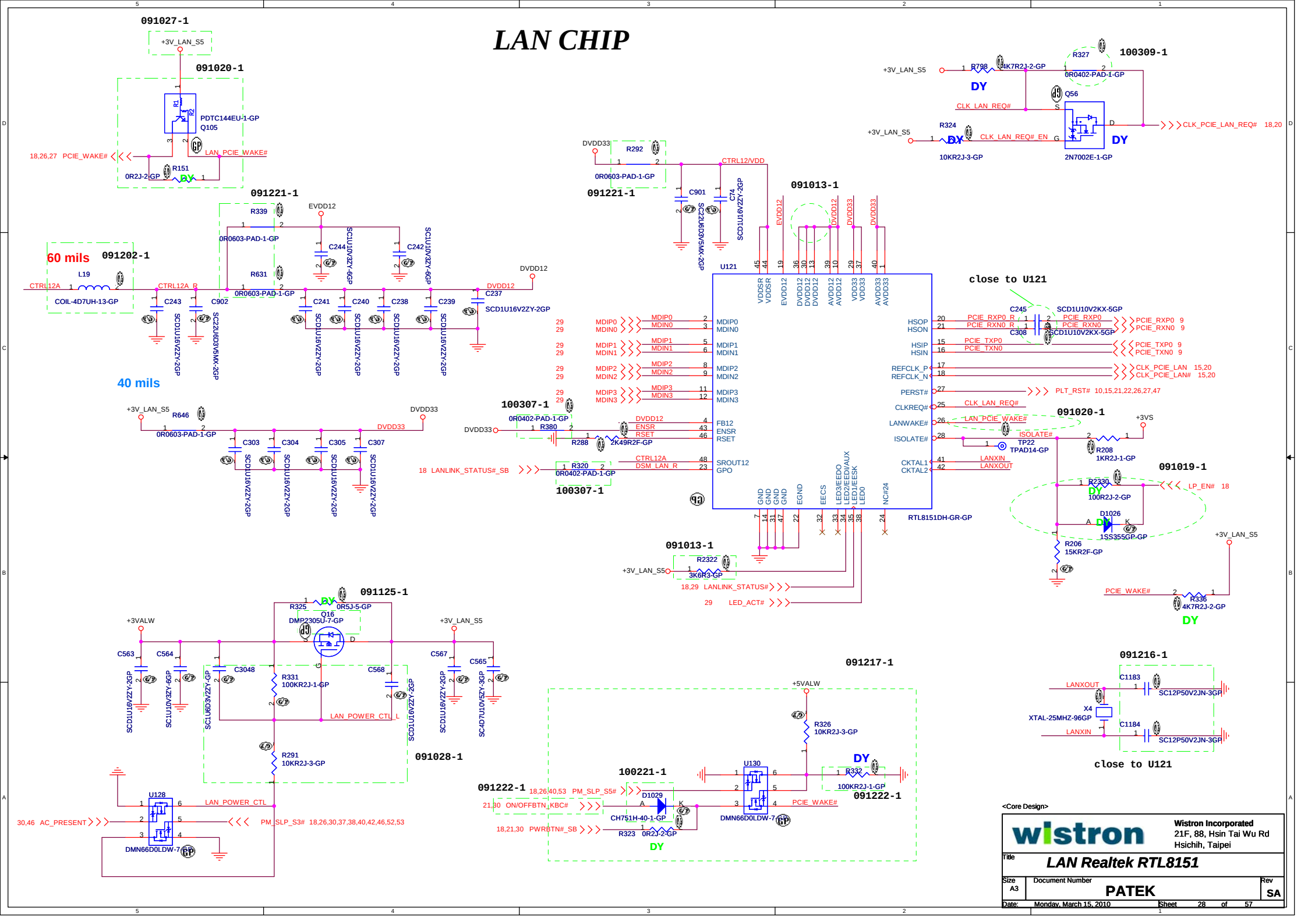
Title: WLAN/G-SENSOR

Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 27 of 57

LAN CHIP



<Core Design>

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Hsichih, Taipei

Title: LAN Realtek RTL8151

Size: A3 | Document Number: PATEK | Rev: SA

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close to XF1 pin1,4,7,10

VDD17
C1025 1 SCD01U16V2KX-3GP
C1029 1 SCD01U16V2KX-3GP
C1031 1 SCD01U16V2KX-3GP
C1023 1 SCD01U16V2KX-3GP

Transformer

091014-1
68.89240.30B
XFORM-24P-27-GP

28	MDIP0	12	13	MDO0+	
	VDD17	10			
28	MDIN0	11	14	MDO0-	MCT0 C1215 1 SCD01U50V2KX-1GP MCT0_R
			15		
28	MDIP1	9	16	MDO1+	
	VDD17	7			
28	MDIN1	8	17	MDO1-	MCT1 C1216 1 SCD01U50V2KX-1GP MCT1_R
			18		
28	MDIP2	6	19	MDO2+	
	VDD17	4			
28	MDIN2	5	20	MDO2-	MCT2 C1217 1 SCD01U50V2KX-1GP MCT2_R
			21		
28	MDIP3	3	22	MDO3+	
	VDD17	1			
28	MDIN3	2	23	MDO3-	MCT3 C1218 1 SCD01U50V2KX-1GP MCT3_R
			24		

XF1

MDO_C
RN71
C580 1 SC1KP2KV6KX-GP
SRN75J-1-GP
090930-1
091016-1

LAN Conn

28 LED_ACT# → LED_ACT#
18,28 LANLINK_STATUS# → LANLINK_STATUS#
DY DY
C583 SCD1U16V2ZY-2GP
C584 SCD1U16V2ZY-2GP

091102-1
GREEN
YELLOW
RJ1
RJ45-8P-10-GP-U2

+3V_LAN_S5 → R335 470R2J-2-GP → LANLINK_STATUS# / LAN_LED_G
+3V_LAN_S5 → R334 470R2J-2-GP → LAN_LED_Y

A1	LAN_LED_G
A2	
A3	
1	MDO0+
2	MDO0-
3	MDO1+
4	MDO2+
5	MDO2-
6	MDO1-
7	MDO3+
8	MDO3-
B1	LAN_LED_Y
B2	LED_ACT#
9	
10	

Yellow
B1(+),B2(-)
Green
A1(-),A2(+)

<Core Design>

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Hsichih, Taipei

Title: Magnetic & RJ45
Size: A3
Document Number: PATEK
Rev: SC
Date: Monday, March 15, 2010
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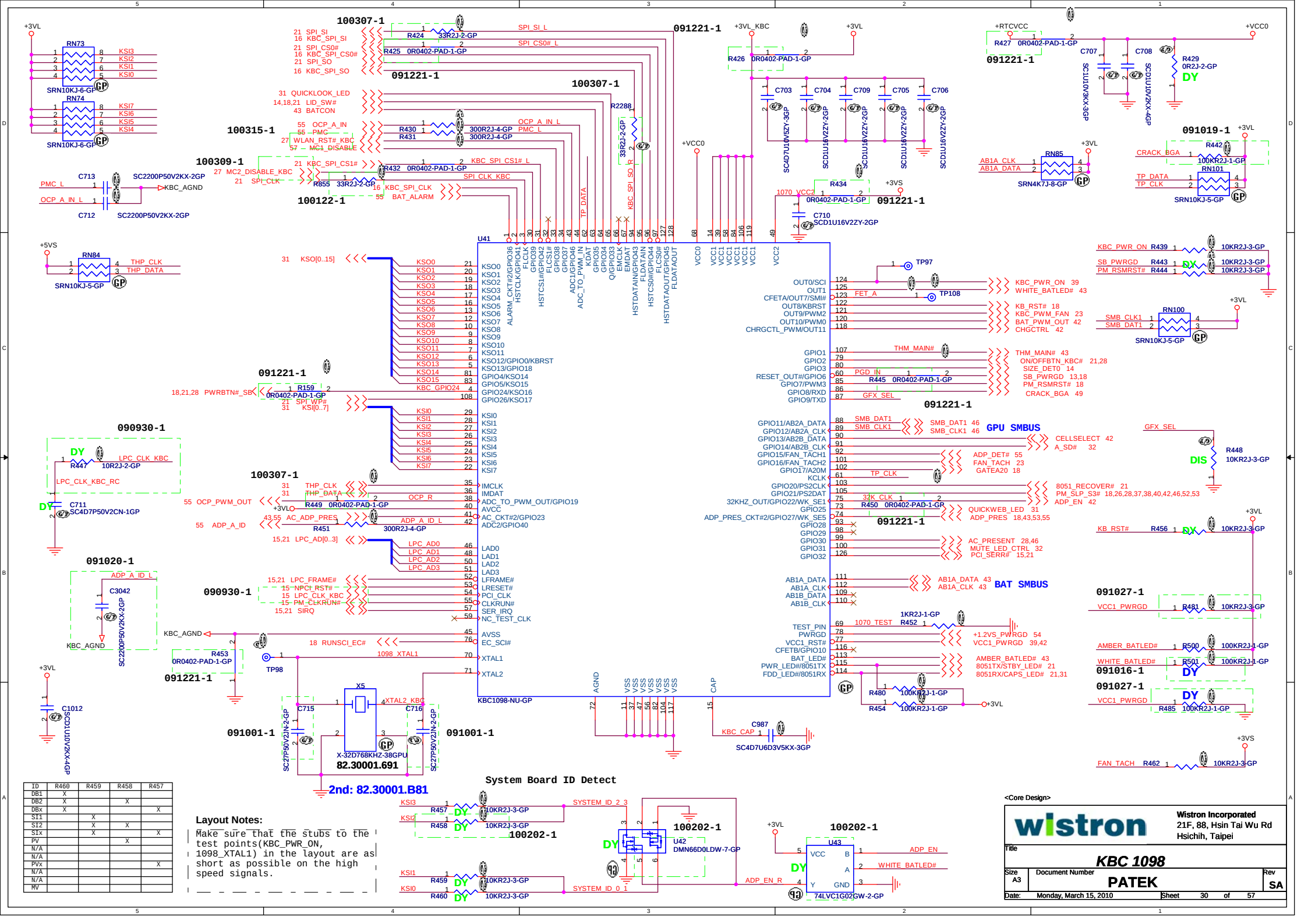
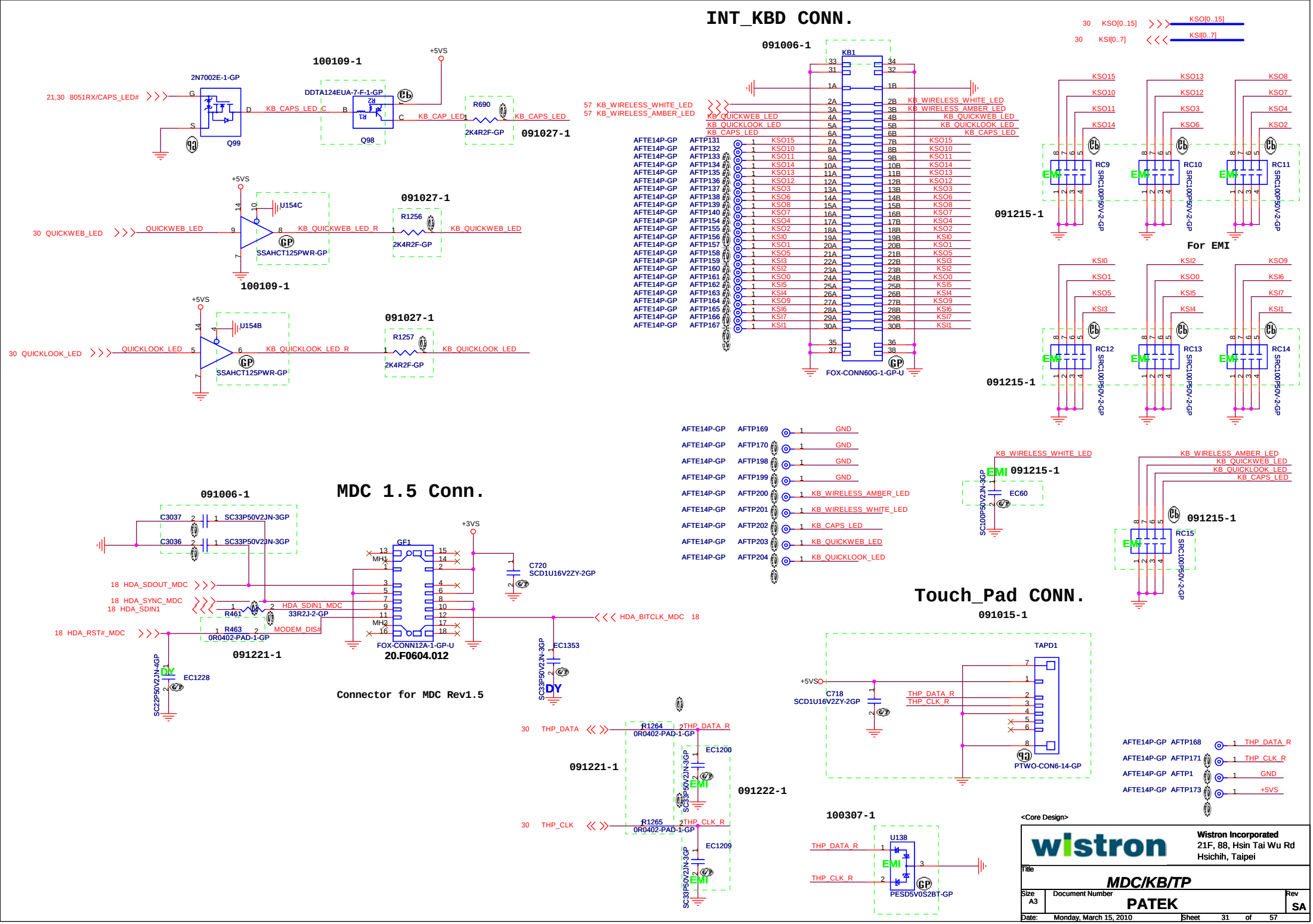


ID	R460	R459	R458	R457
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2		X	X	
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				

INT_KBD CONN.



MDC 1.5 Conn.

Touch_Pad CONN.

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: MDC/KB/TP

Size	Document Number	Rev
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AUDIO CODEC(92HD80)

Port Arrangement
Port A---> Ext Mic
Port B---> HP
Port C---> FREE
Port D---> SPKR
Port E---> FREE
Port F---> FREE

Place close to Codec chip

Close to Pin13

Close to Pin14

audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

<Core Design>

Wistron Incorporated
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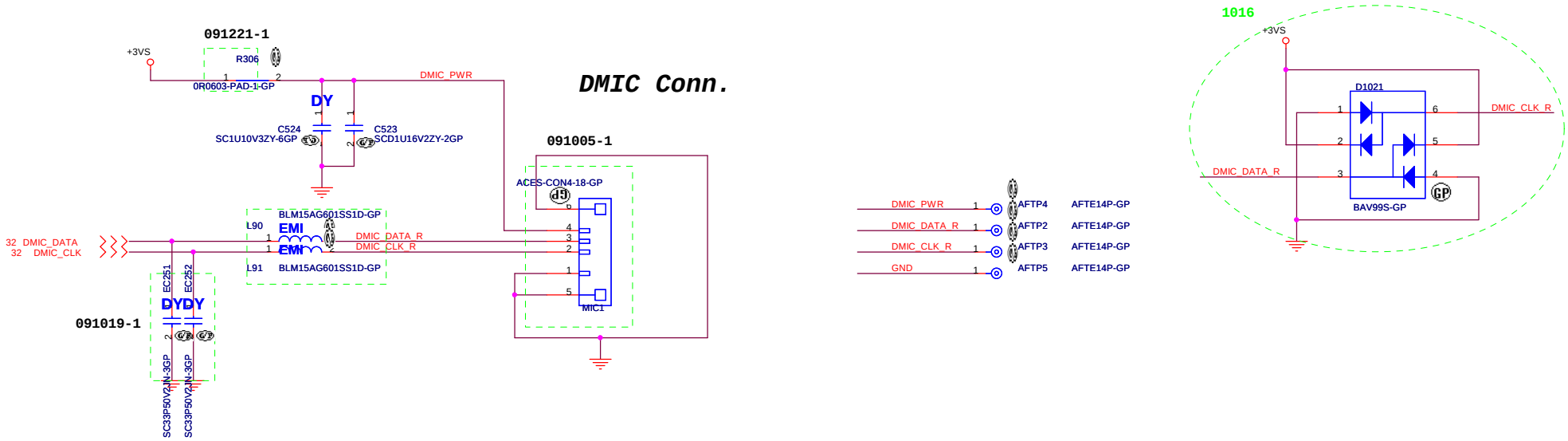
Hsichih, Taipei

Title: AUDIO 92HD80 / OP AMP

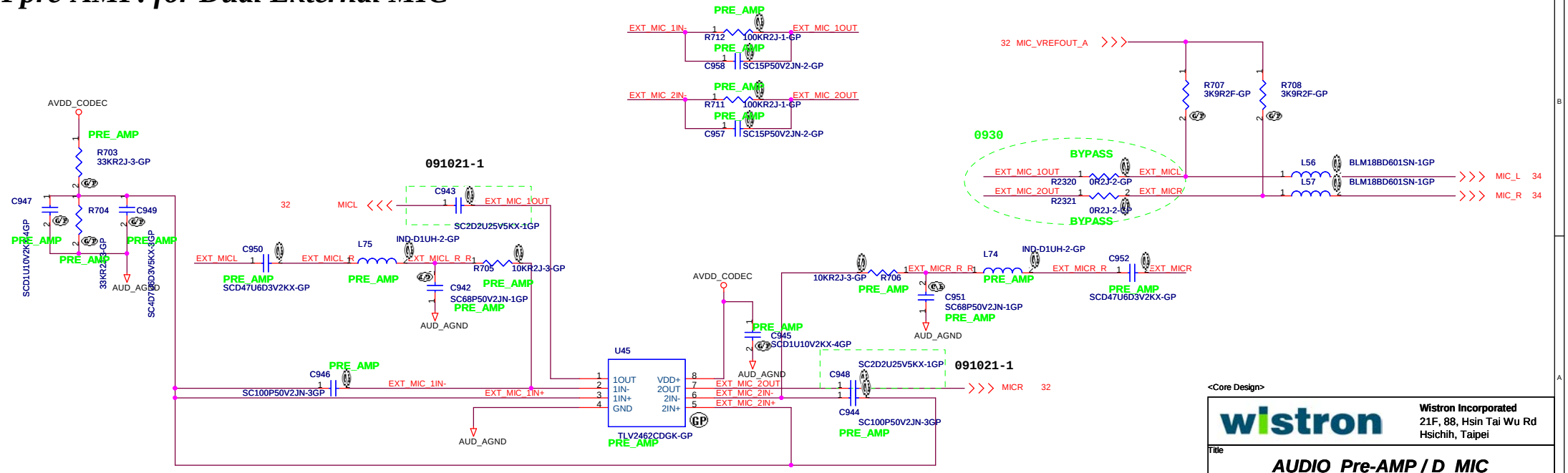
Size: A3 | Document Number: PATEK | Rev: SA

Date: Monday, March 15, 2010 | Sheet 32 of 57

Dual Internal Digital MIC



Ppre-AMP. for Dual External MIC



<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO Pre-AMP / D MIC

Size	Document Number	Rev
A3	PATEK	SA

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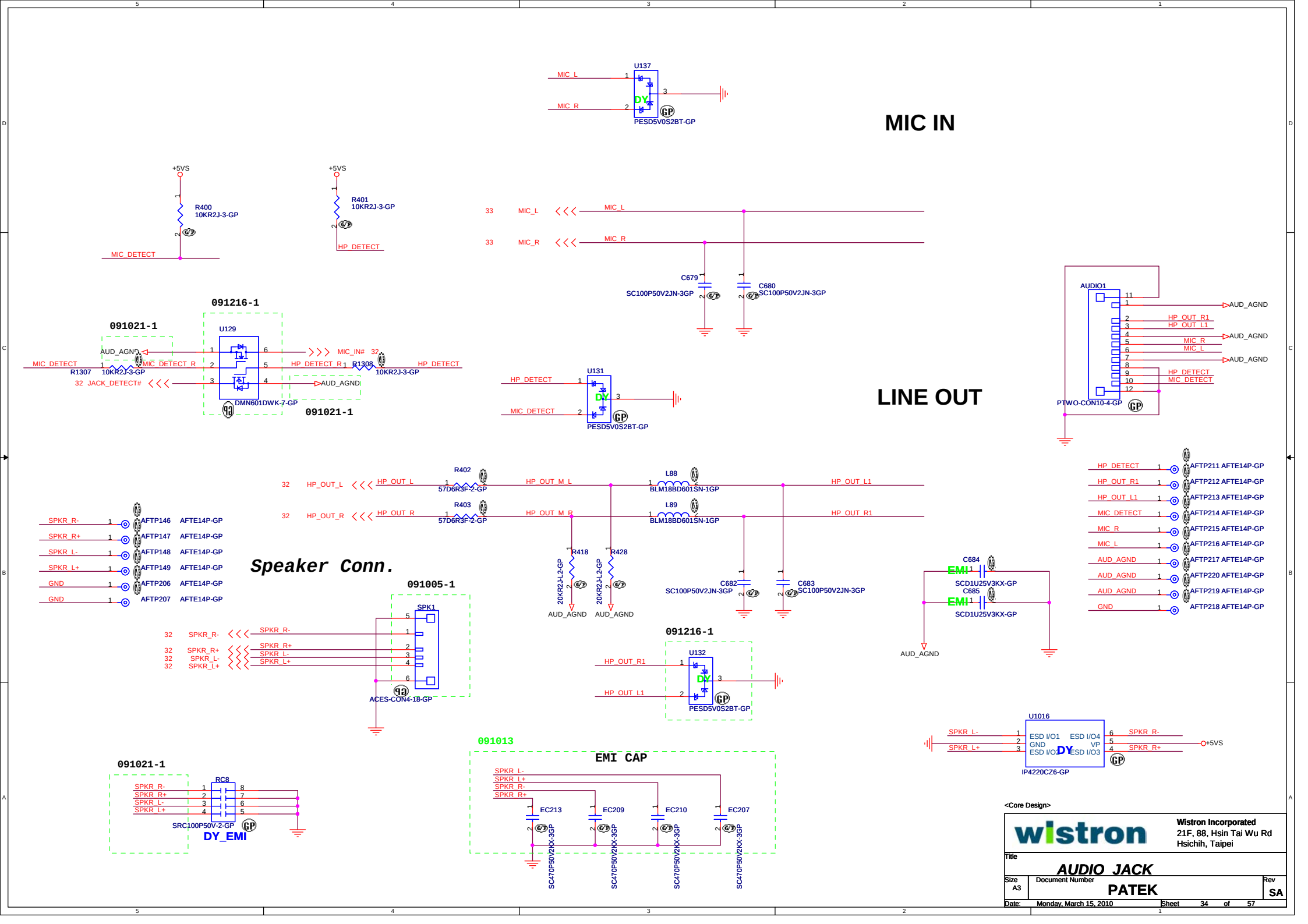
MIC IN
LINE OUT
Speaker Conn.
EMI CAP
U137
PESD5V0S2BT-GP
R400
10KR2J-3-GP
R401
10KR2J-3-GP
MIC_DETECT
HP_DETECT
+5VS
C679
C680
SC100P50V2JN-3GP
091216-1
091021-1
U129
DMN601DWK-7-GP
R1307
R1308
MIC_DETECT_R
HP_DETECT_R
JACK_DETECT#
AUD_AGND
U131
AUDIO1
PTWO-CON10-4-GP
R402
R403
57D6R3F-2-GP
L88
L89
BLM18BD601SN-1GP
R418
R428
20KR2J-L2-GP
C682
C683
C684
C685
SCD1U25V3KX-GP
AFTP146 AFTE14P-GP
AFTP147 AFTE14P-GP
AFTP148 AFTE14P-GP
AFTP149 AFTE14P-GP
AFTP206 AFTE14P-GP
AFTP207 AFTE14P-GP
AFTP211 AFTE14P-GP
AFTP212 AFTE14P-GP
AFTP213 AFTE14P-GP
AFTP214 AFTE14P-GP
AFTP215 AFTE14P-GP
AFTP216 AFTE14P-GP
AFTP217 AFTE14P-GP
AFTP220 AFTE14P-GP
AFTP219 AFTE14P-GP
AFTP218 AFTE14P-GP
091005-1
SPK1
ACES-CON4-18-GP
U132
U1016
IP4220CZ6-GP
091013
EC213
EC209
EC210
EC207
SC470P50V2KX-3GP
RC8
SRC100P50V-2-GP
DY_EMI
<Core Design>
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Title
AUDIO JACK
Size A3
Document Number PATEK
Rev SA
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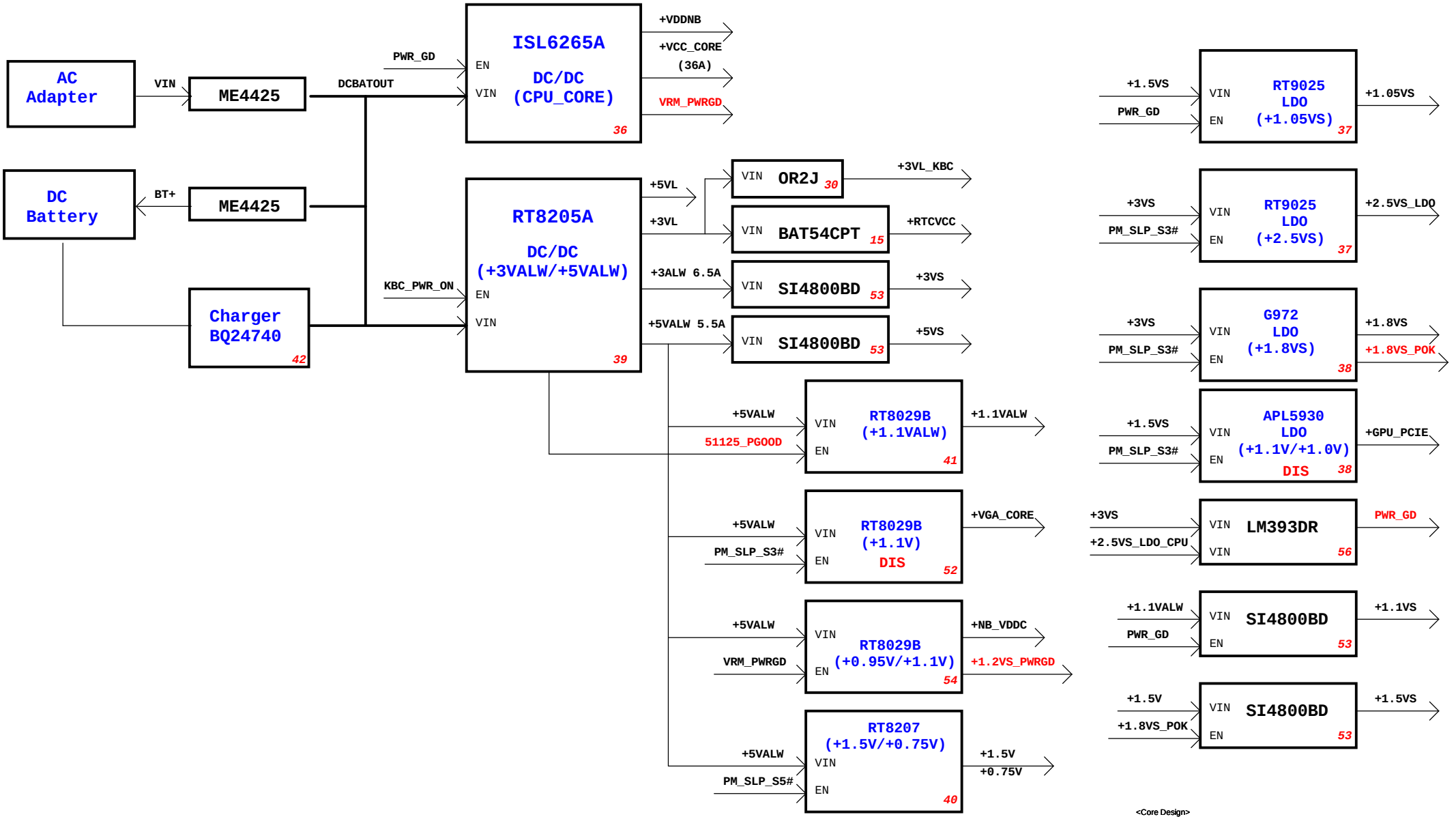
Patek DIS POWER Block Diagram



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Title: Power Block Diagram

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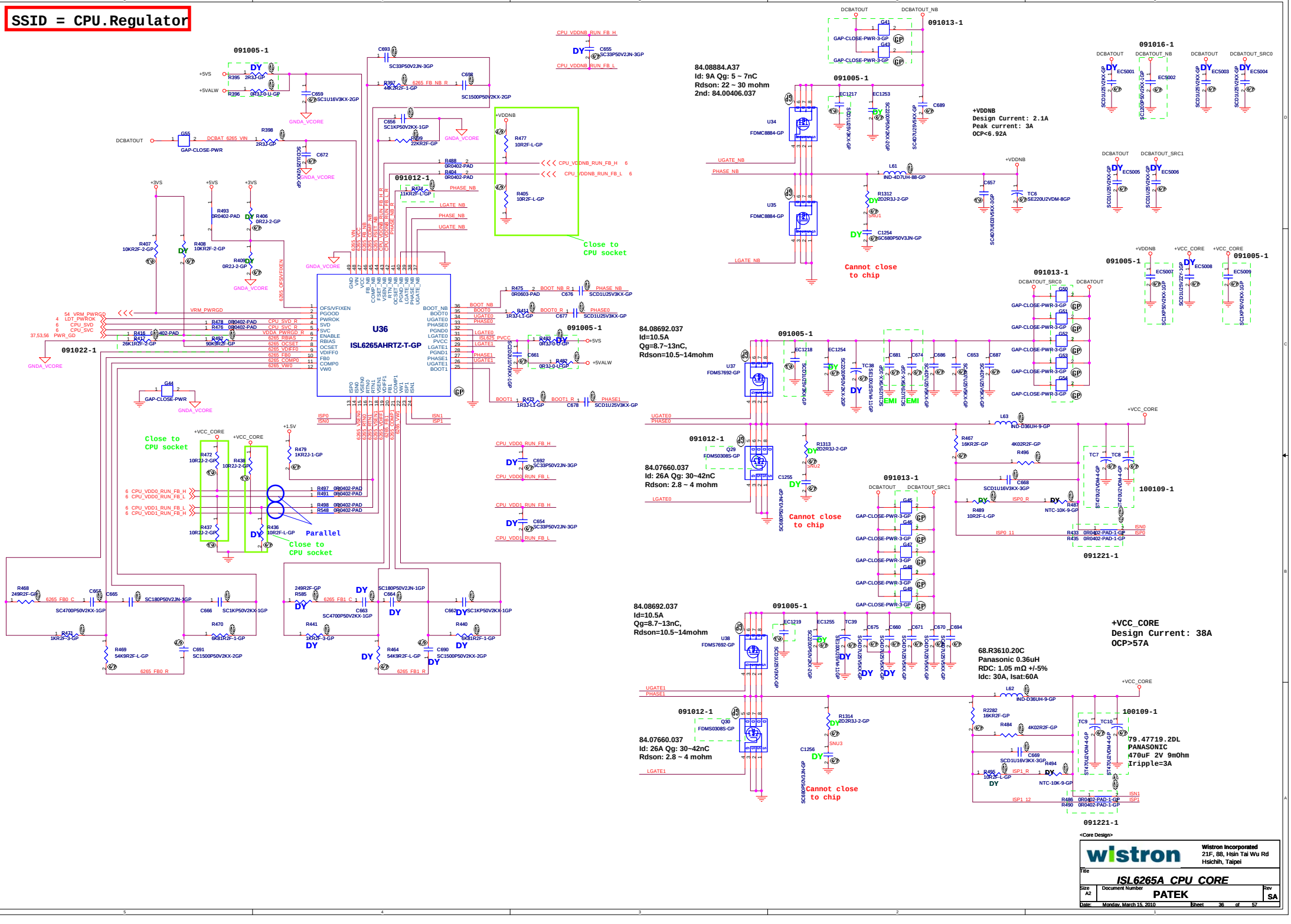
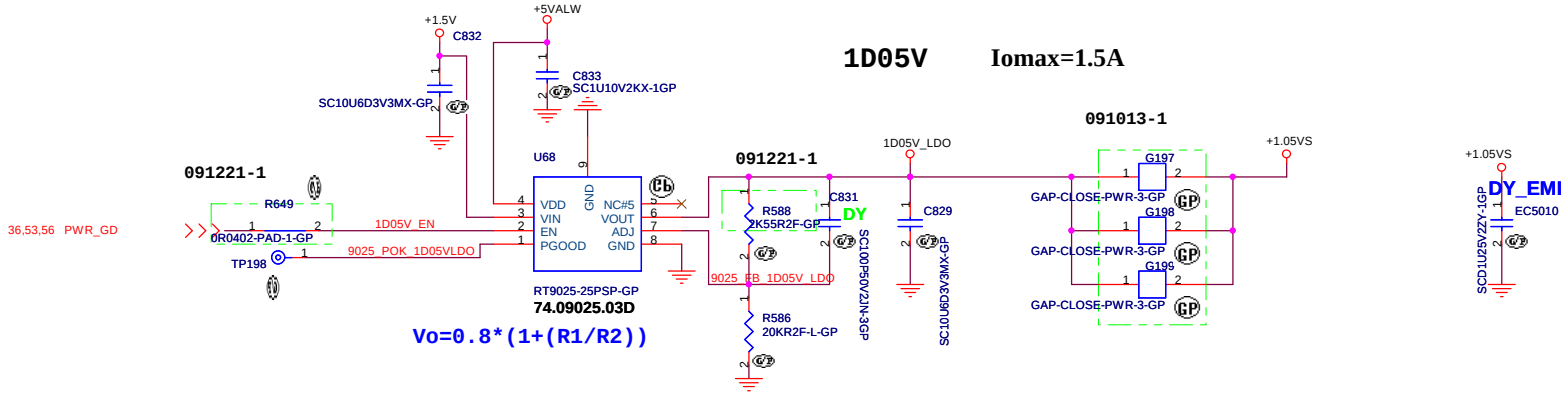
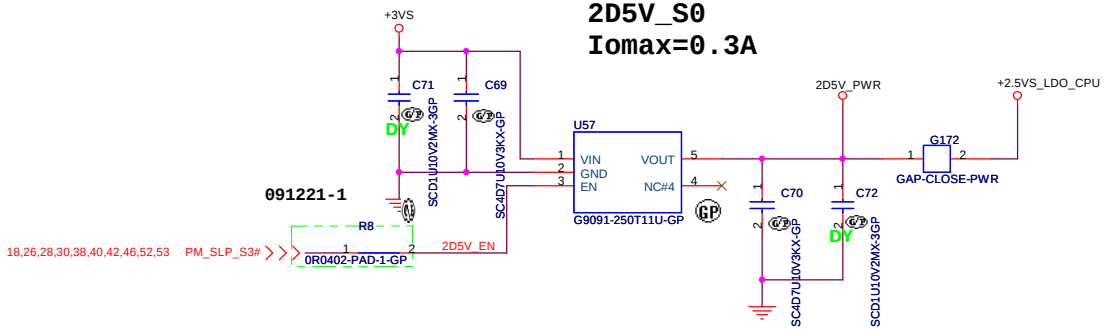
SSID = CPU.Regulator







<Core Design>

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Title: RT8209B +1.05VS / +2.5VS

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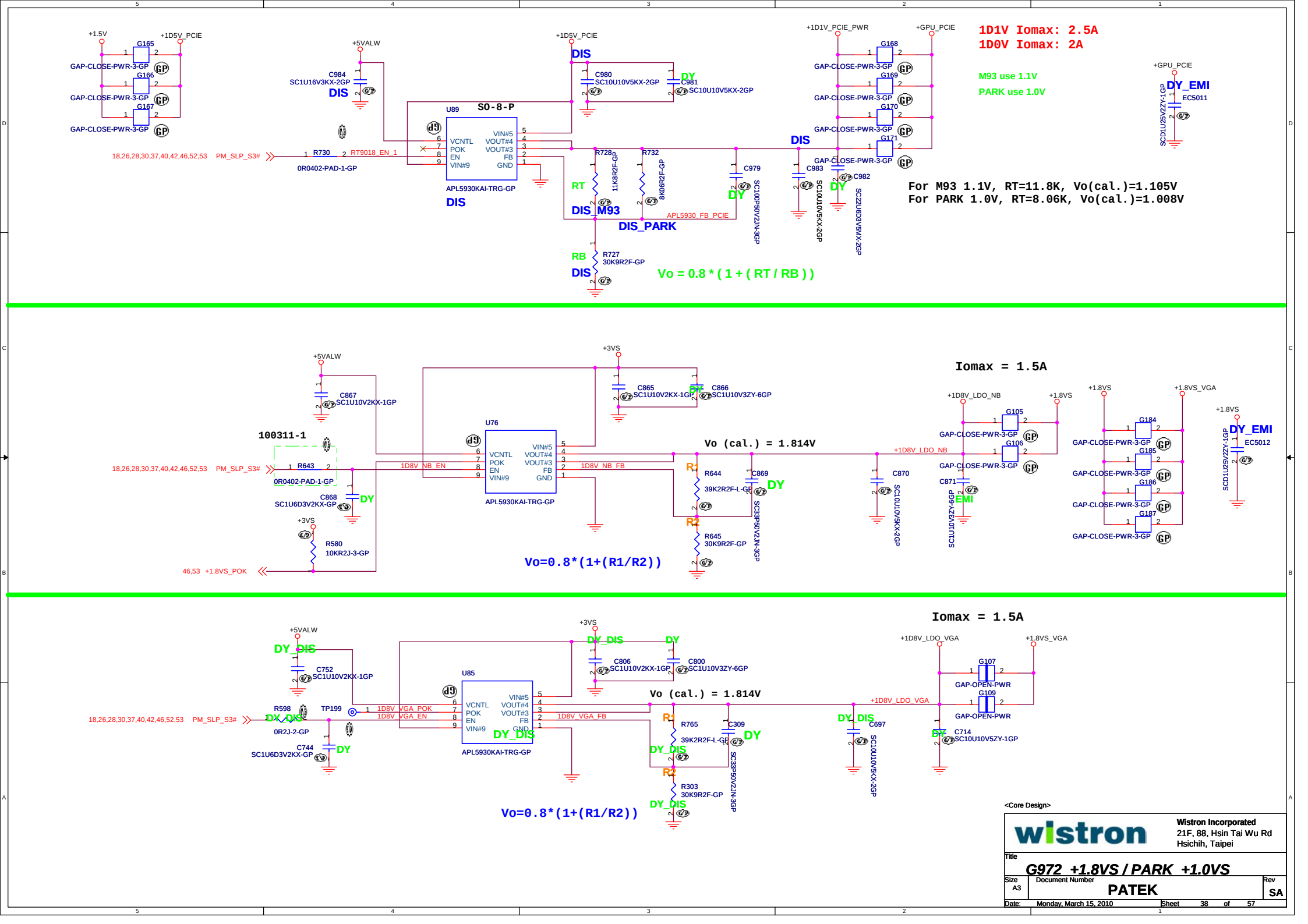
1D1V Iomax: 2.5A
1D0V Iomax: 2A
M93 use 1.1V
PARK use 1.0V
For M93 1.1V, RT=11.8K, Vo(cal.)=1.105V
For PARK 1.0V, RT=8.06K, Vo(cal.)=1.008V
Vo = 0.8 * (1 + (RT / RB))
U89
S0-8-P
APL5930KAI-TRG-GP
R730
0R0402-PAD-1-GP
RT9018_EN_1
PM_SLP_S3#
R728
11K8R2F-GP
R732
8K06R2F-GP
R727
30K9R2F-GP
APL5930_FB_PCIE
DIS
DIS_M93
DIS_PARK
RT
RB
DY
DY_EMI
Iomax = 1.5A
Vo (cal.) = 1.814V
Vo=0.8*(1+(R1/R2))
U76
100311-1
R643
0R0402-PAD-1-GP
1D8V_NB_EN
1D8V_NB_FB
R644
39K2R2F-L-GP
R645
30K9R2F-GP
R580
10KR2J-3-GP
46,53 +1.8VS_POK
U85
R598
0R2J-2-GP
TP199
1D8V_VGA_POK
1D8V_VGA_EN
1D8V_VGA_FB
R765
39K2R2F-L-GP
R303
30K9R2F-GP
DY_DIS
<Core Design>
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Title
G972 +1.8VS / PARK +1.0VS
Size A3
Document Number
PATEK
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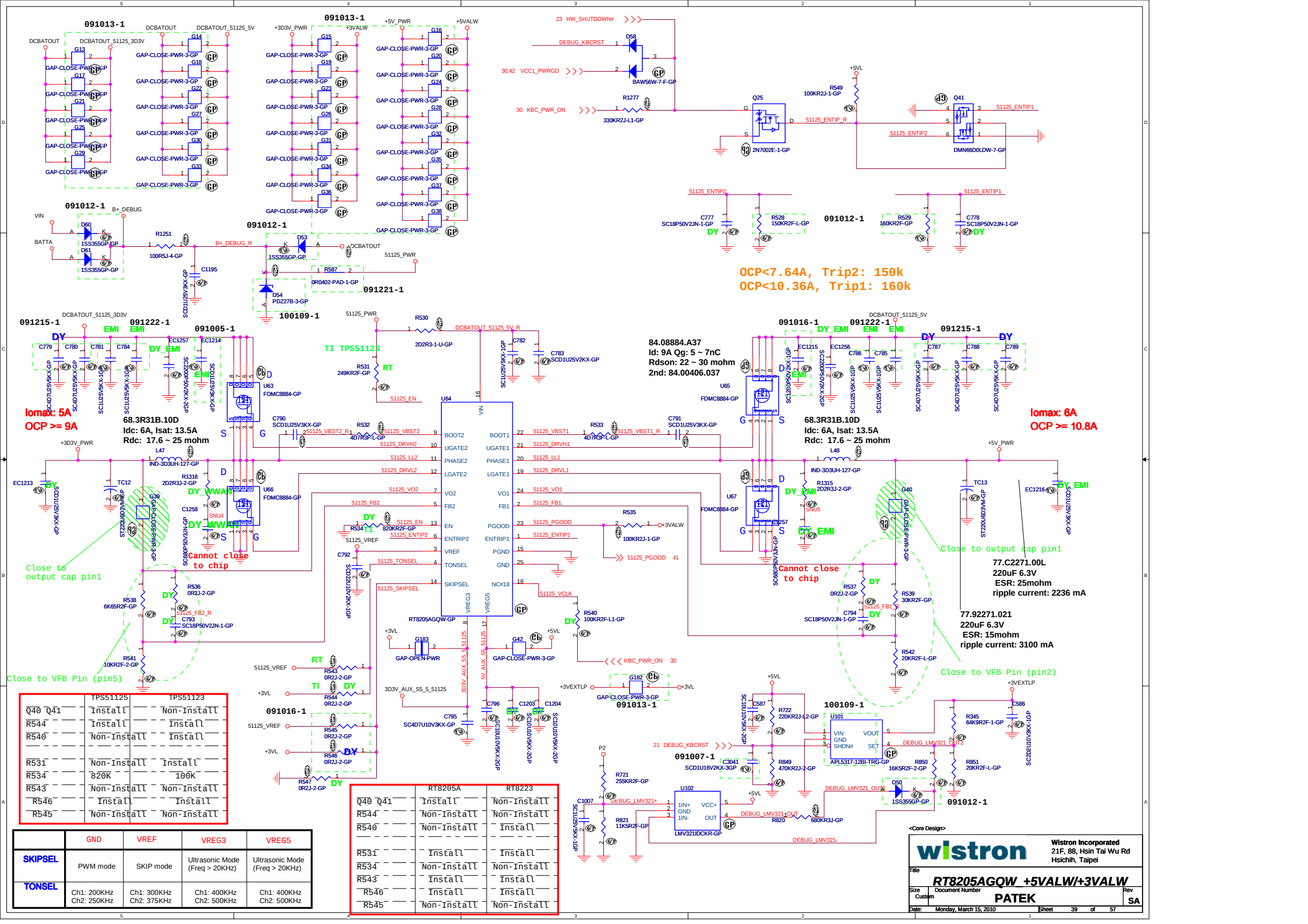
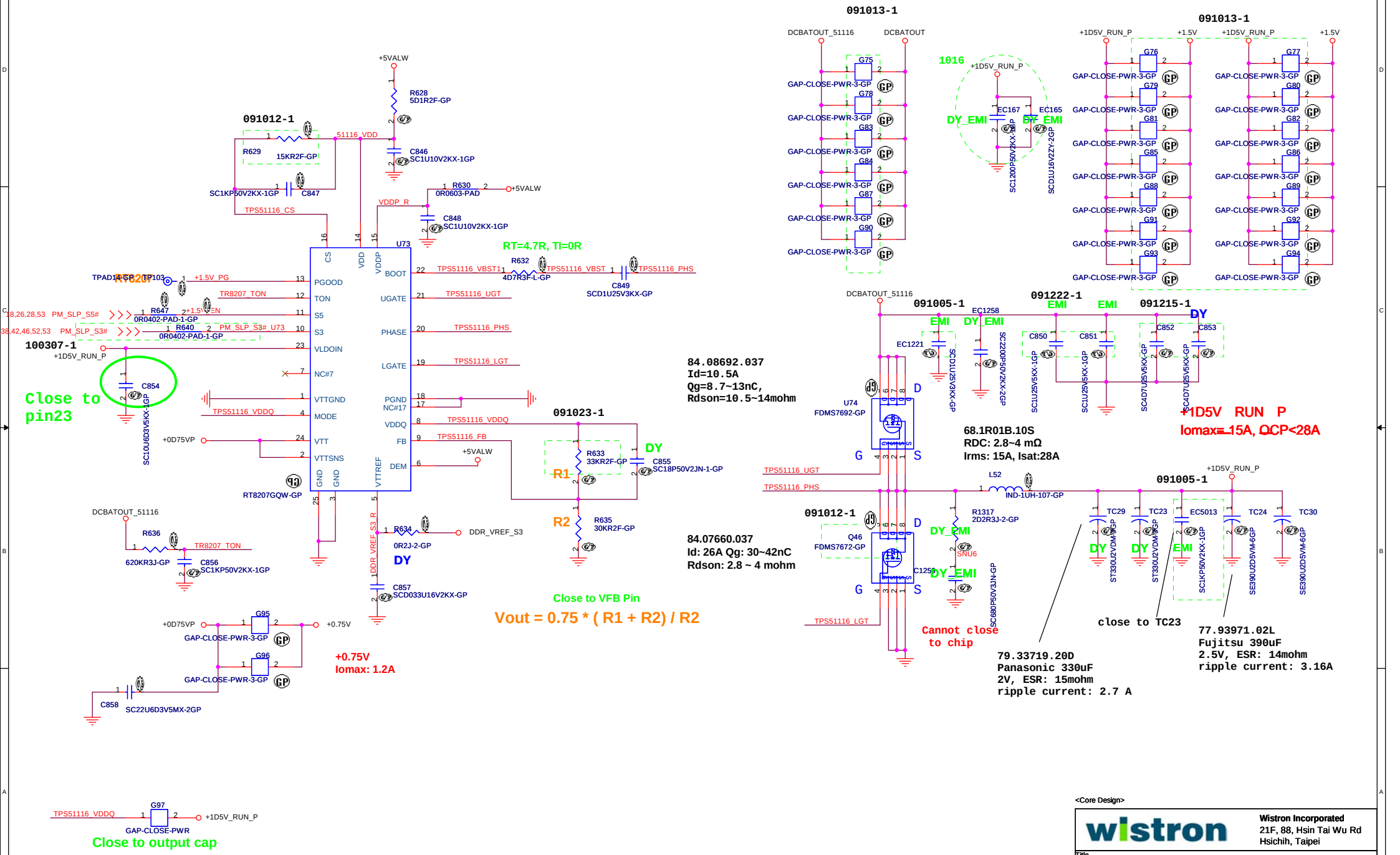


	TPS51125	TPS51123
Q40 Q41	Install	Non-Install
R544	Install	Install
R540	Non-Install	Install
R531	Non-Install	Install
R534	820K	100K
R543	Non-Install	Non-Install
R546	Install	Install
R545	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R544	Non-Install	Non-Install
R540	Non-Install	Install
R531	Install	Install
R534	Non-Install	Non-Install
R543	Install	Install
R546	Install	Install
R545	Non-Install	Non-Install

RT8207 for 1D5V and 0D75V



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Title: RT8209B +1.5V / +0.75V

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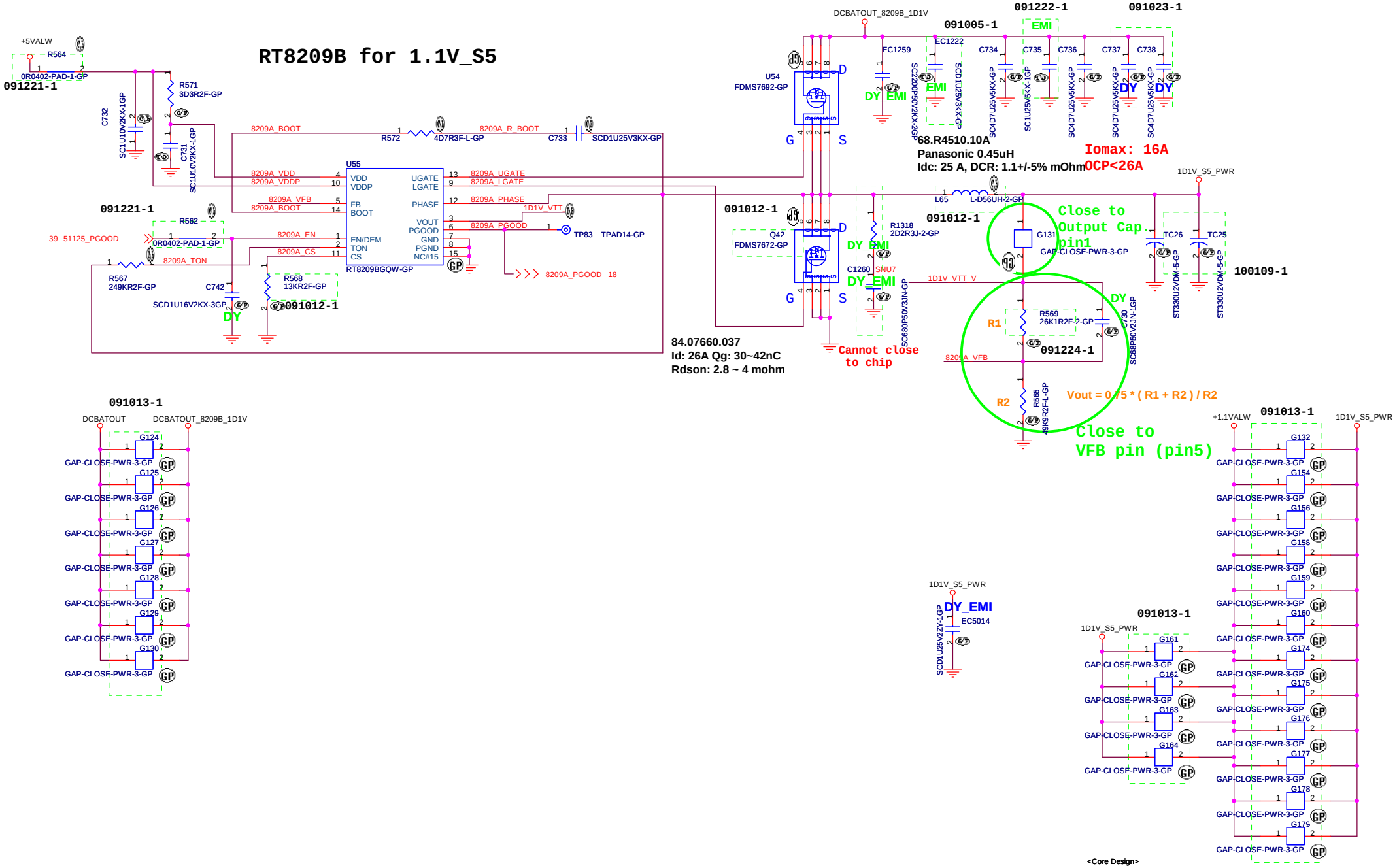
RT8209B for 1.1V_S5



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Title: RT8209B +1.1VALW

Size	Document Number	Rev
A3	PATEK	SA

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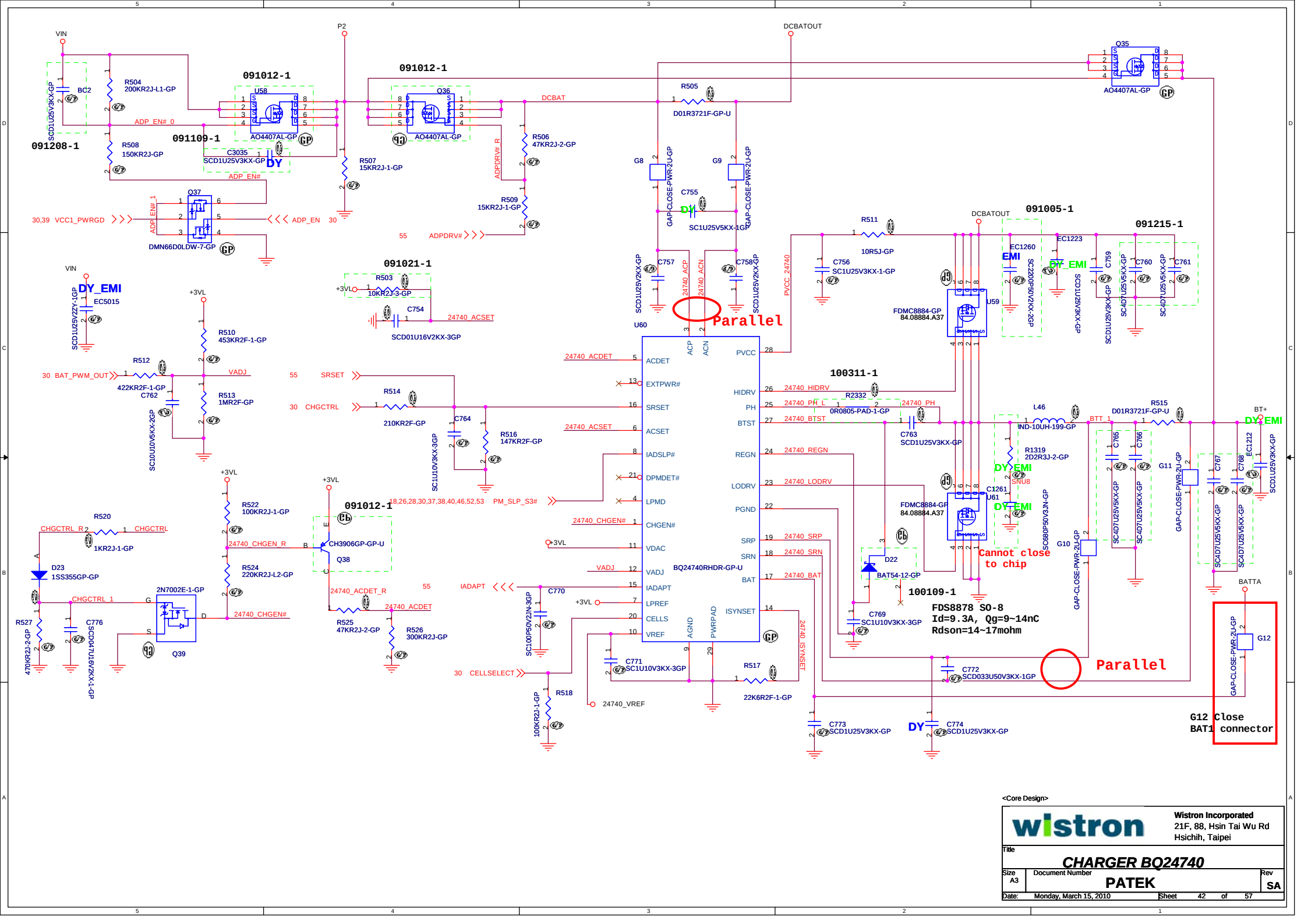
VIN
P2
DCBATOUT
091012-1
091208-1
091109-1
091021-1
091005-1
091215-1
100311-1
100109-1
BQ24740RHDR-GP-U
Parallel
Parallel
Cannot close to chip
FDS8878 SO-8
Id=9.3A, Qg=9~14nC
Rdson=14~17mohm
G12 Close BAT1 connector
<Core Design>
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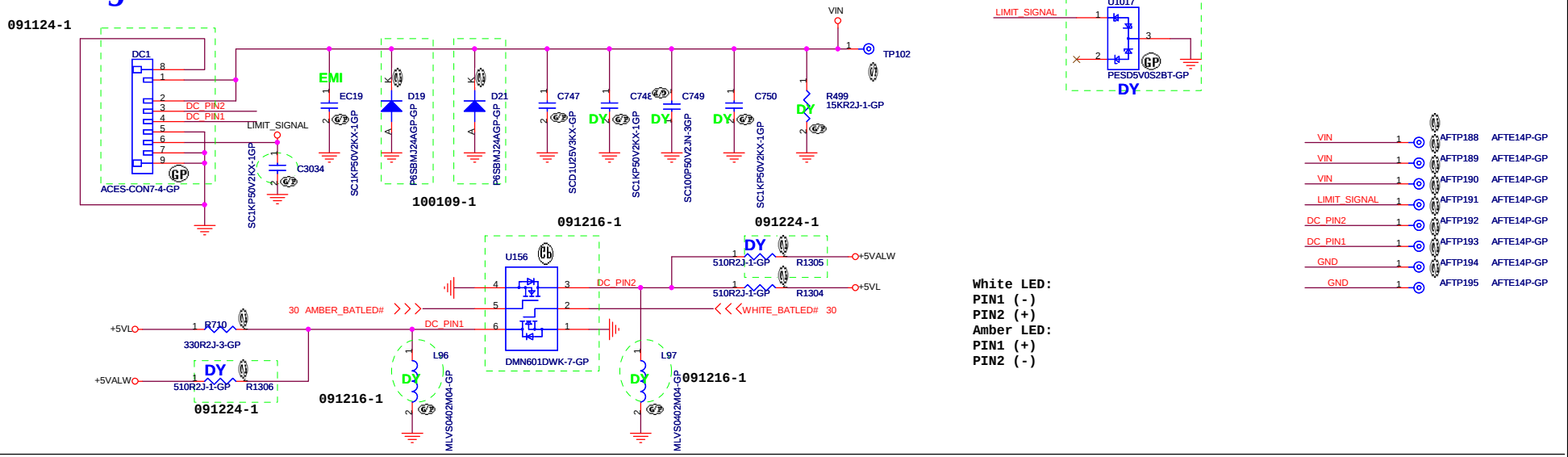
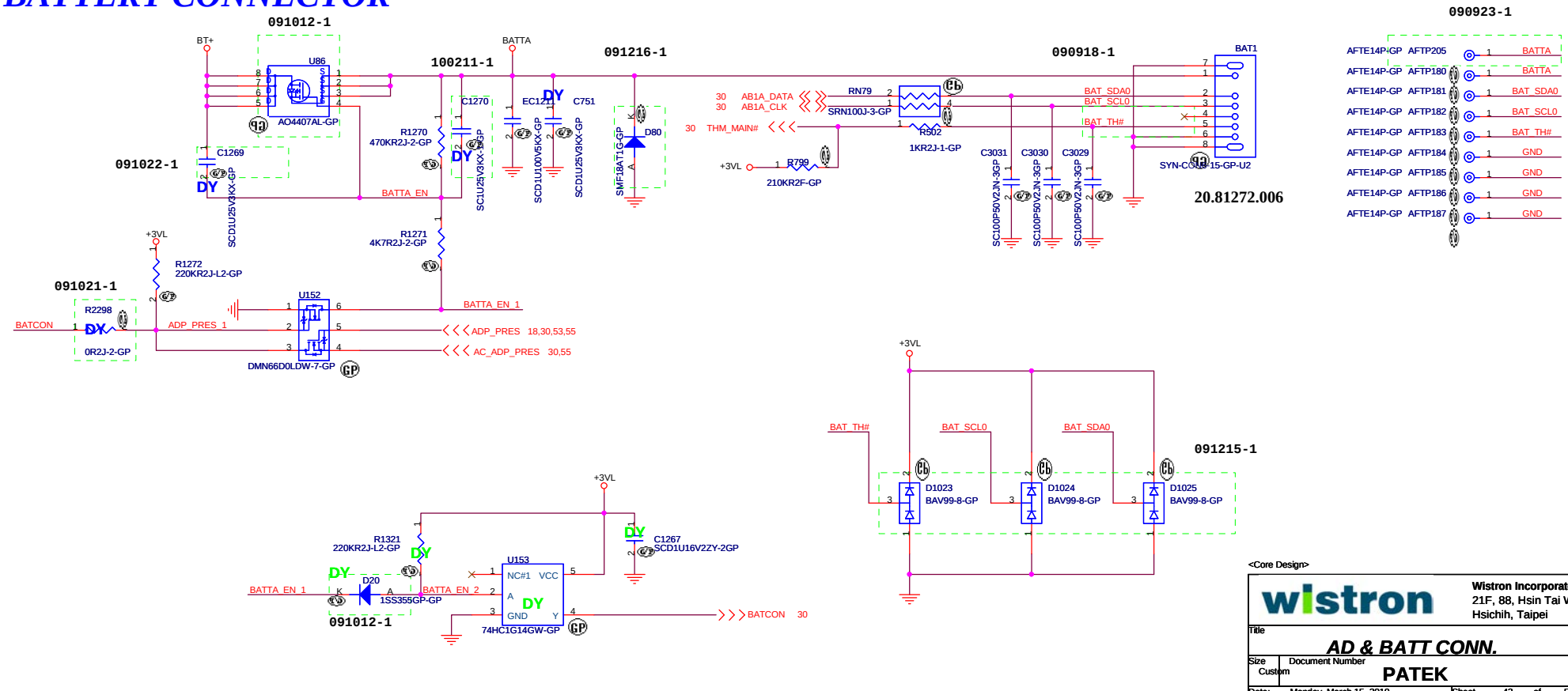
CHARGER BQ24740
PATEK
Monday, March 15, 2010

Adaptor in to generate DCBATOUT



White LED:
PIN1 (-)
PIN2 (+)
Amber LED:
PIN1 (+)
PIN2 (-)

BATTERY CONNECTOR



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Title: **AD & BATT CONN.**

Size: Custom | Document Number: **PATEK** | Rev: SA

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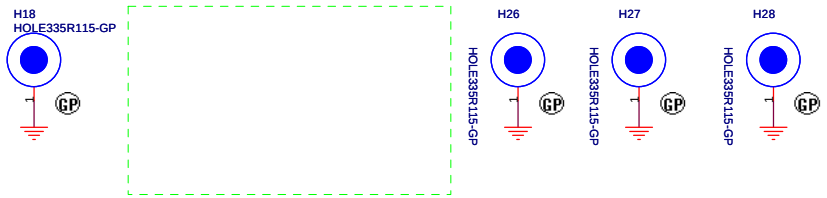
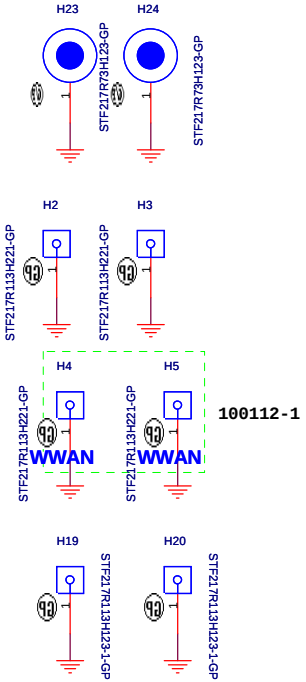
HOLE

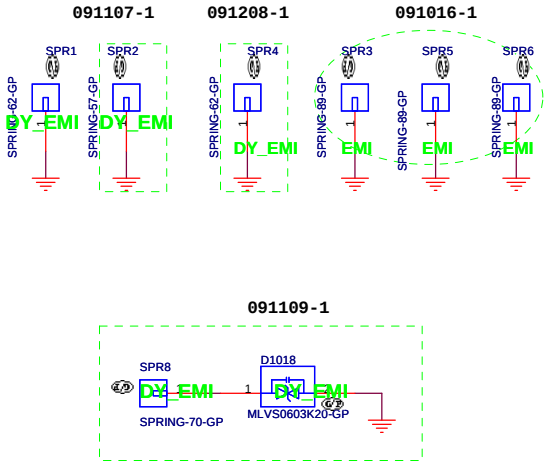
091016-1



StandOff

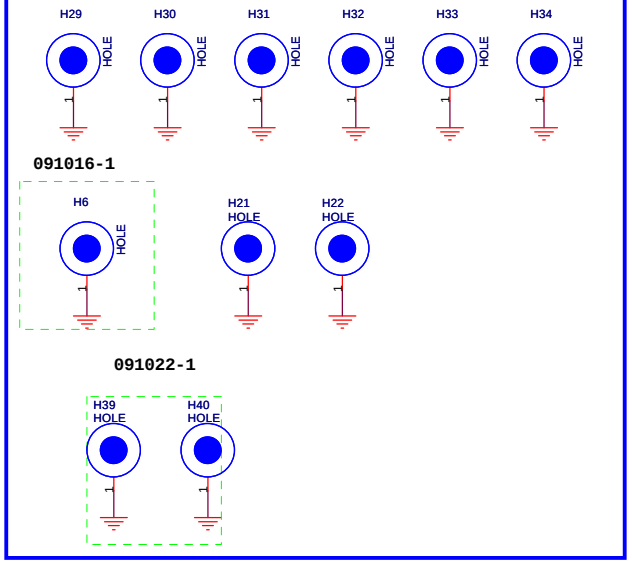


Spring

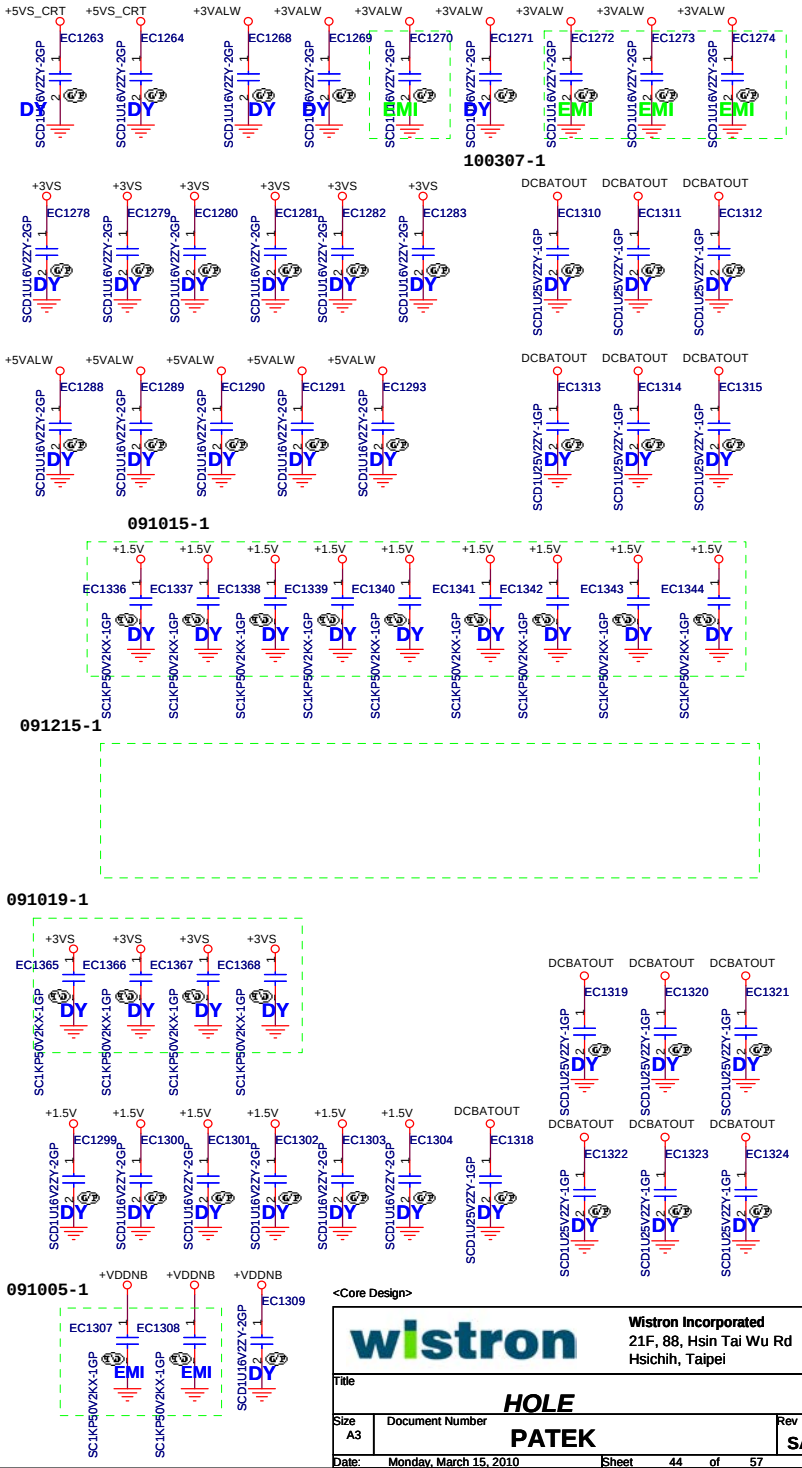


P/N: ZZ.0HOLE.XXX

Ground PAD



EMI CAP



<Core Design>

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Title: HOLE

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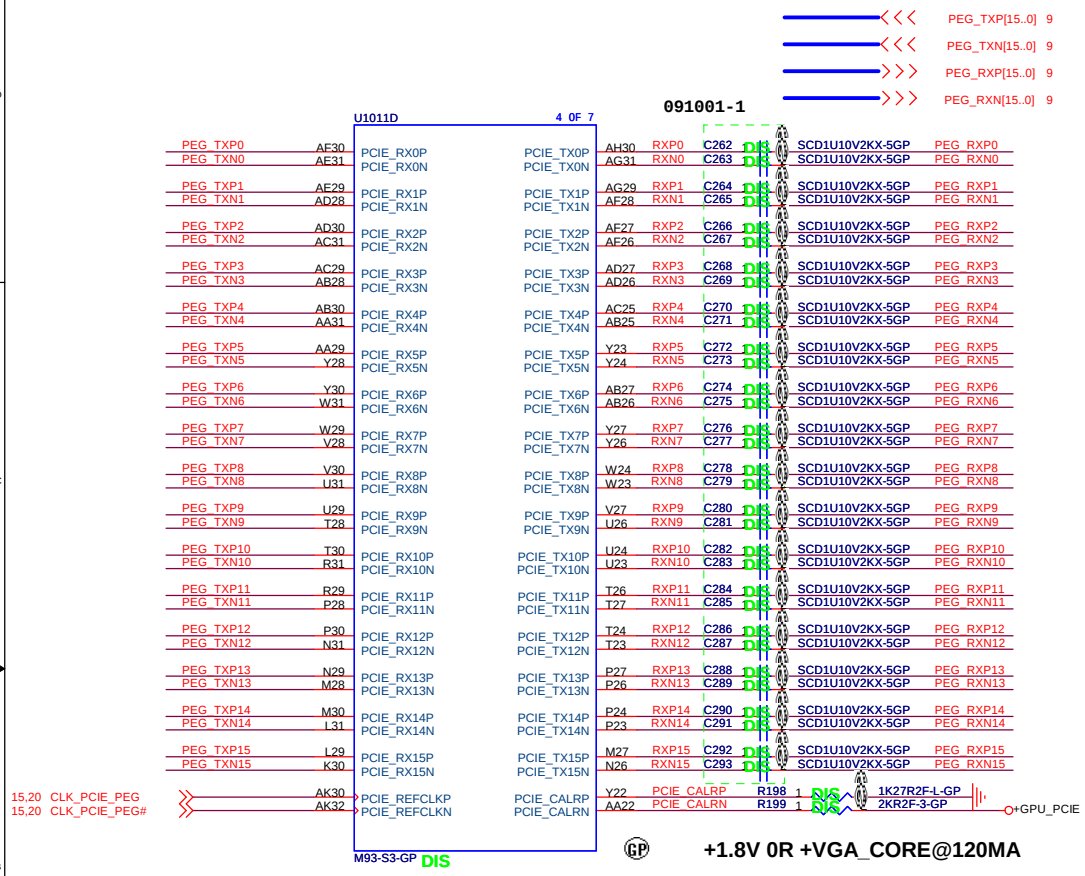
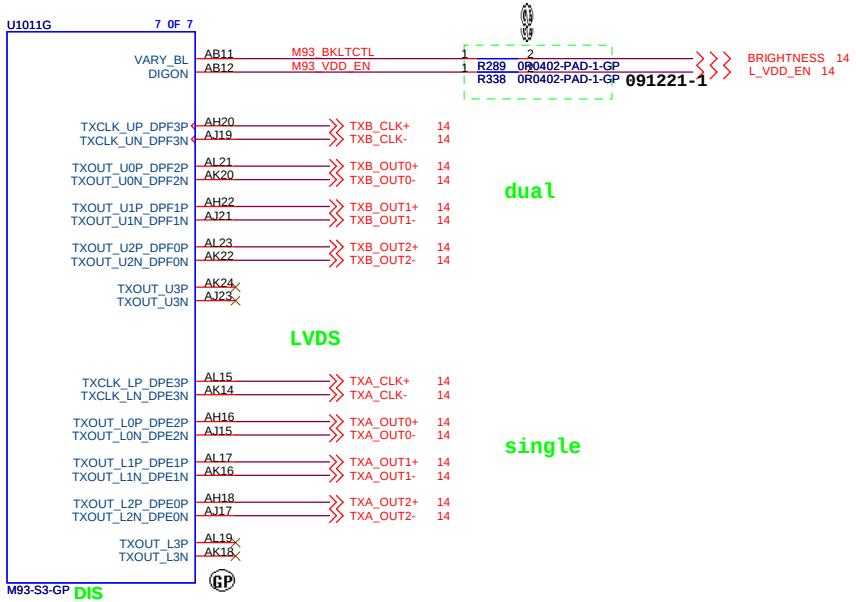
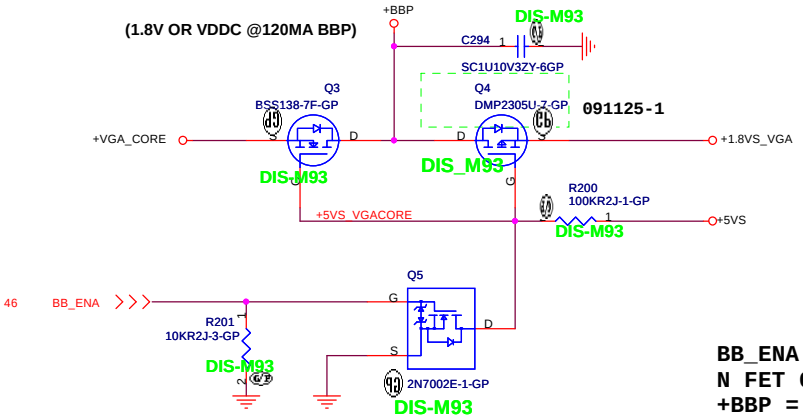
M93 GPU(1/5)







BB_ENA = 0V FOR BACK BIASING DISABLED
N FET Q5 = OFF, P FET Q4 = OFF, N FET Q3 = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET Q5 = ON, P FET Q4 = ON, N FET Q3 = OFF
+BBP = +1.8V

<Core Design>

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Title: VGA-PCIE/LVDS(1/5)

Size	Document Number	Rev
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M93 GPU(2/5)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 XX

Aperture Conig. PIN	M93S3 GPIO	Strapping Resistor	64MB	128MB	256MB
CONFIG0	GPIO_11	R209	0	0	1
CONFIG1	GPIO_12	R210	1	0	0
CONFIG2	GPIO_13	R211	0	0	0

M93 VRAM ID

Bit0 Low=Quanta ,H=Wistron

Bit1 Low=512MB, H=1GB

Bit2 Low=Samsung ,H=Hynix

Bit3 Low

VRAM ID

090625

M93 LP: VDDC=0.9/1.1V

VID1	VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

HDMI

CRT

LVDS

HDMI

CRT

DIS_PARK

Only for PARK-S3
DO NOT INSTALL for M93-S3

Optional RC network to fine tune PWR SEQ.

<Core Design>

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Title: LCD/CRT/HDMI PORT(2/5)

Size: A2 | Document Number: PATEK | Rev: SA

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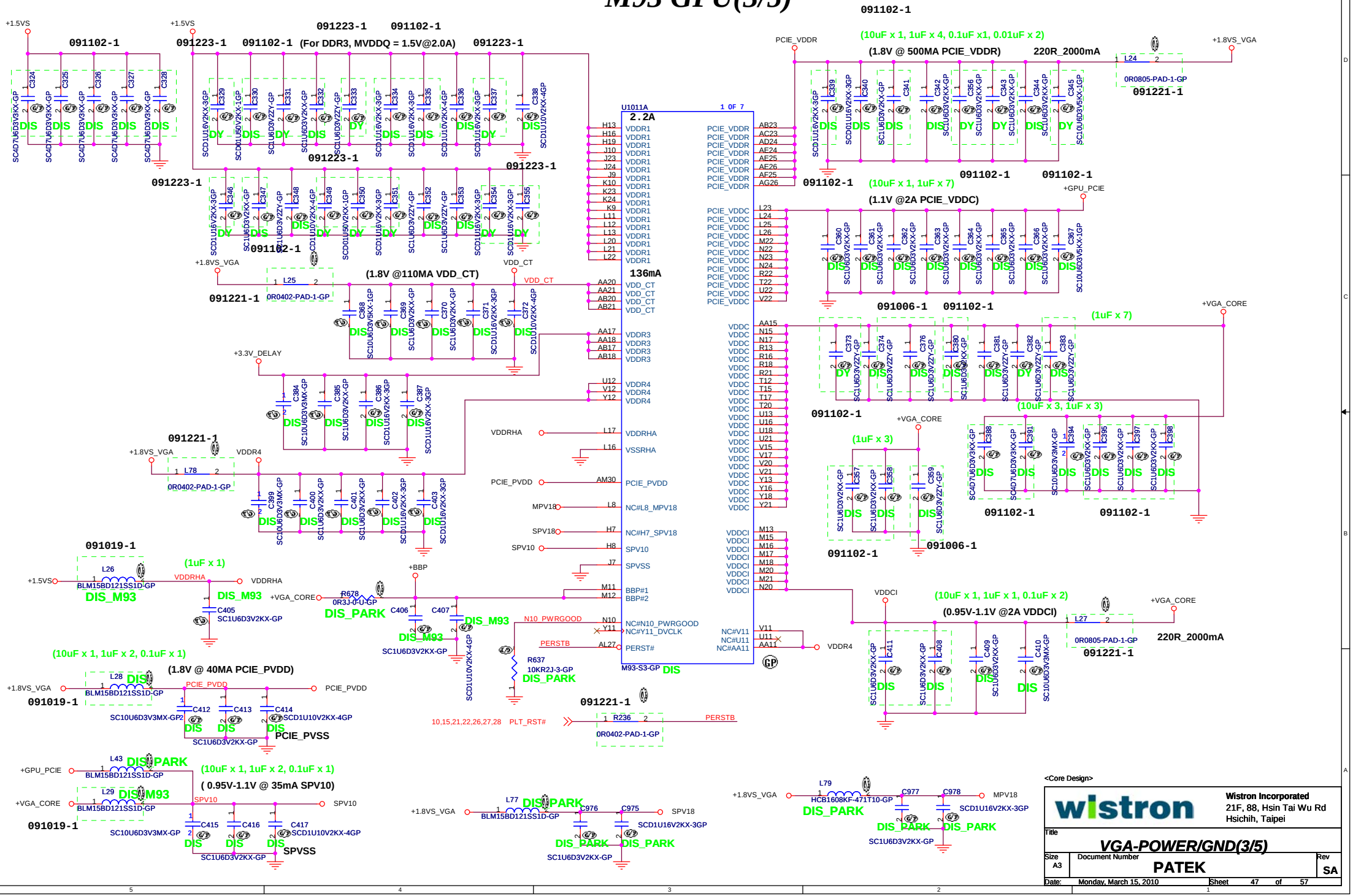
M93 GPU(3/5)


091102-1
091223-1
091102-1 (For DDR3, MVDDQ = 1.5V@2.0A)
091223-1
+1.5VS
U1011A
2.2A
1 0F 7
136mA
VDD_CT
(1.8V @110MA VDD_CT)
091221-1
0R0402-PAD-1-GP
+3.3V_DELAY
VDDR4
VDDRHA
VSSRHA
PCIE_PVDD
NC#L8_MPV18
NC#H7_SPV18
SPV10
SPVSS
BBP#1
BBP#2
NC#N10_PWRGOOD
NC#Y11_DVCLK
PERST#
M93-S3-GP
DIS
091019-1
(1uF x 1)
VDDRHA
DIS_M93
+VGA_CORE
R678
0R3J-0-U-GP
DIS_PARK
+BBP
C406
C407
SC1U6D3V2KX-GP
N10_PWRGOOD
PERSTB
R637
10KR2J-3-GP
10,15,21,22,26,27,28
PLT_RST#
R236
(10uF x 1, 1uF x 2, 0.1uF x 1)
(1.8V @ 40MA PCIE_PVDD)
+1.8VS_VGA
PCIE_PVDD
SC10U6D3V3MX-GP2
SC1U6D3V2KX-GP
PCIE_PVSS
+GPU_PCIE
+VGA_CORE
(0.95V-1.1V @ 35mA SPV10)
SPV10
SPVSS
PCIE_VDDR
(10uF x 1, 1uF x 4, 0.1uF x1, 0.01uF x 2)
(1.8V @ 500MA PCIE_VDDR)
220R_2000mA
0R0805-PAD-1-GP
091221-1
(10uF x 1, 1uF x 7)
(1.1V @2A PCIE_VDDC)
+GPU_PCIE
091006-1
+VGA_CORE
(1uF x 7)
(10uF x 3, 1uF x 3)
(1uF x 3)
VDDCI
(10uF x 1, 1uF x 1, 0.1uF x 2)
(0.95V-1.1V @2A VDDCI)
+VGA_CORE
220R_2000mA
VDDR4
+1.8VS_VGA
MPV18
SPV18
SCD1U16V2KX-3GP
SC1U6D3V2KX-GP
DIS_PARK
<Core Design>
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Title
VGA-POWER/GND(3/5)
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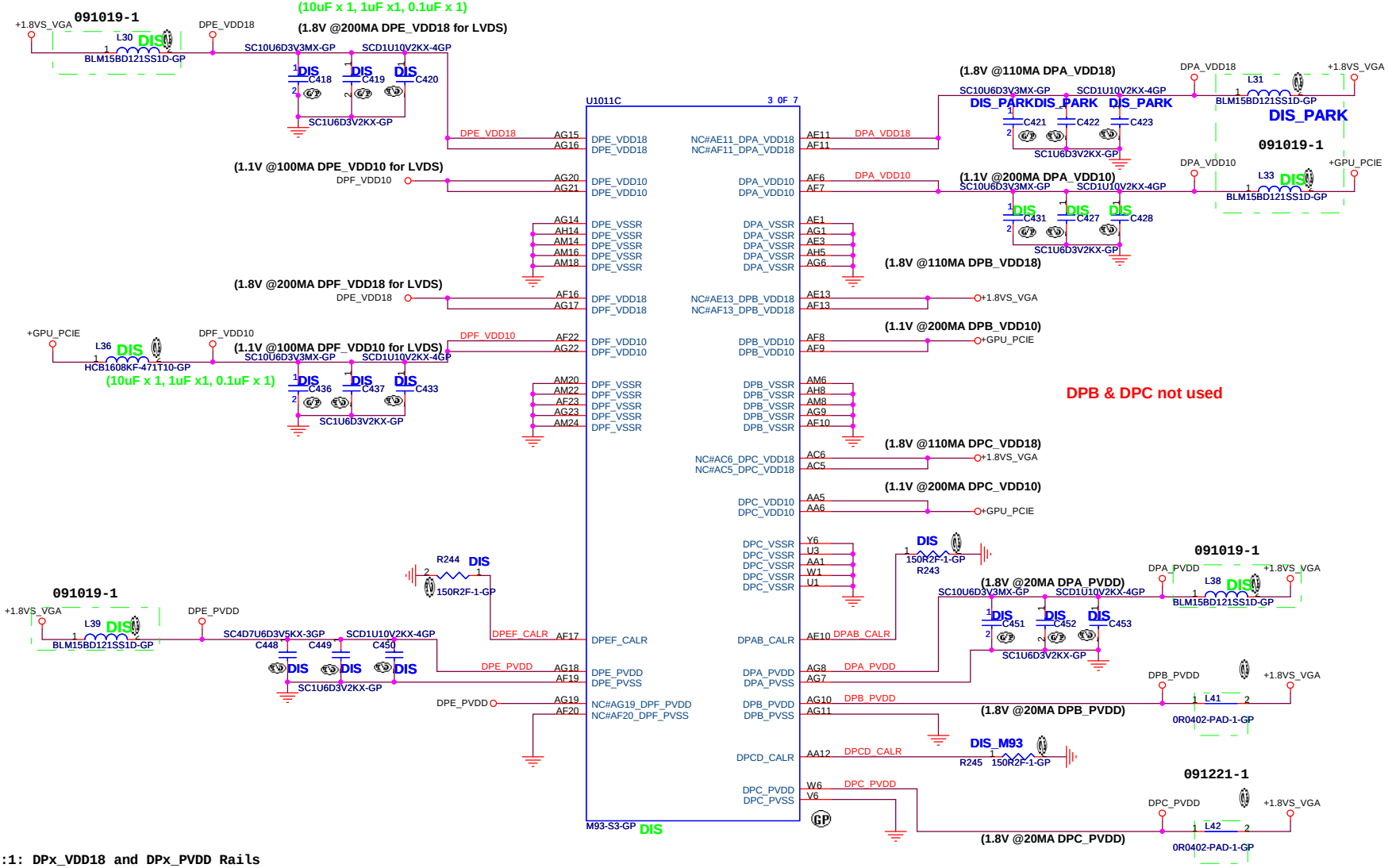
M93 GPU(4/5)

When space is not enough
Consider that use one bead to share



NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEADfor one rail of each pair if signal integrity for DP lanes are OK.
We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove DecouplingCapacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK.
We need at least 500mA Bead to supportjoin rails.

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Title: VGA-POWER/GND(4/5)

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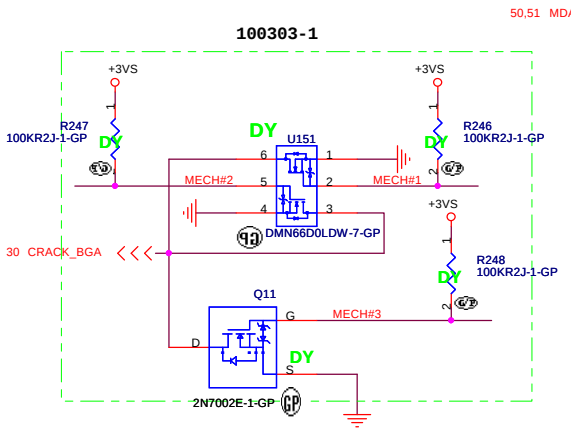
GPU(5/5)



MVREF	0.5 * VDDR1	0.7 * VDDR1
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

<Core Design>
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Title: VGA-MEM INTERFACE(5/5)

Size: A3 | Document Number: PATEK | Rev: SA

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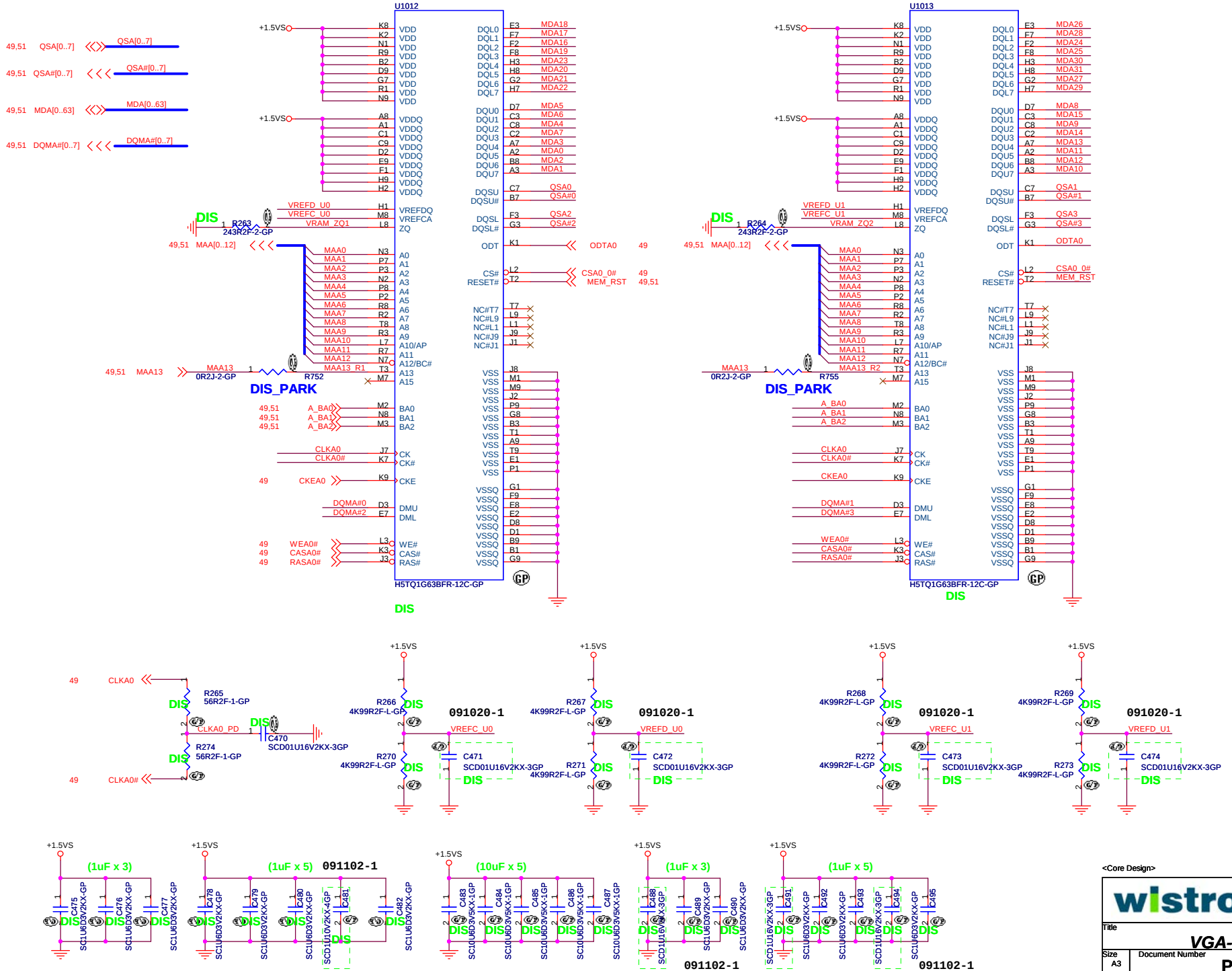
VRAM DDR3 (1/2)

256MB/512MB DDR3



<Core Design>

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Title: VGA-MEMORY

Size	Document Number	Rev
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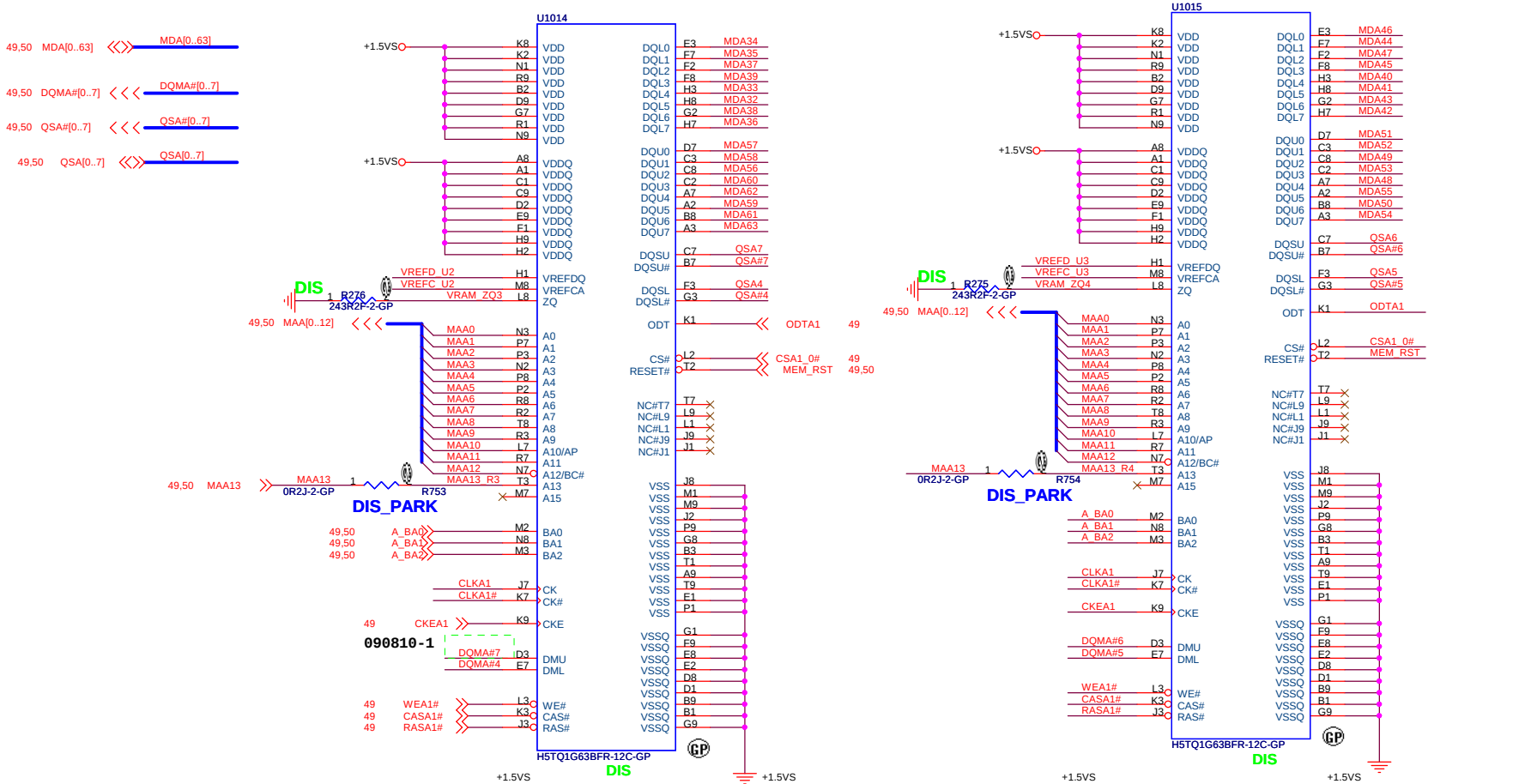
VRAM DDR3 (2/2)

256MB/512MB DDR3



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Title: VGA-MEMORY

Size	Document Number	Rev
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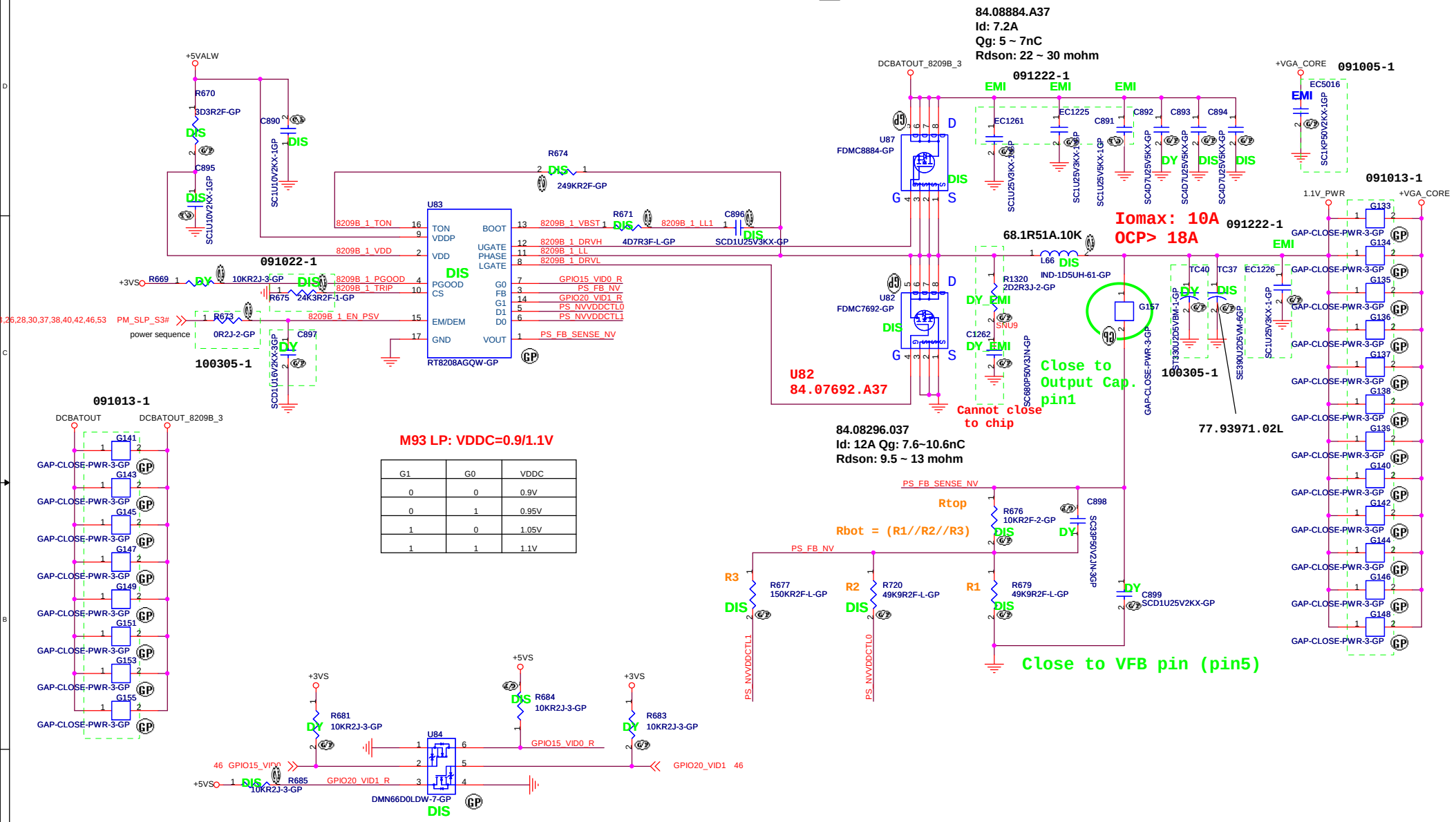
RT8209B for +VGA_CORE



G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V

<Core Design>

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Title: RT8208A +VGA CORE

Size: A3 | Document Number: PATEK | Rev: SA

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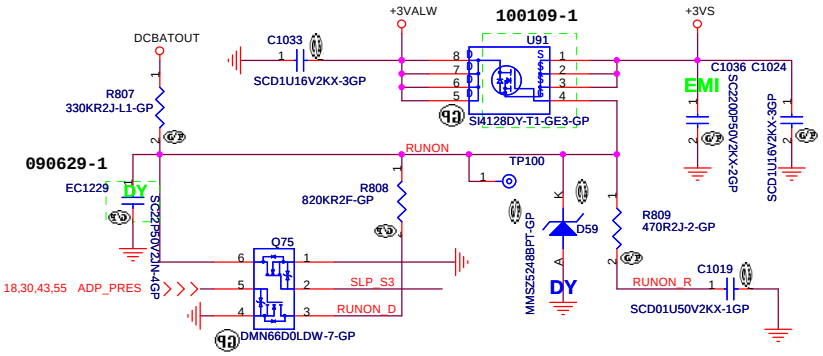
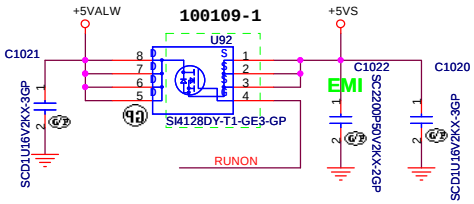
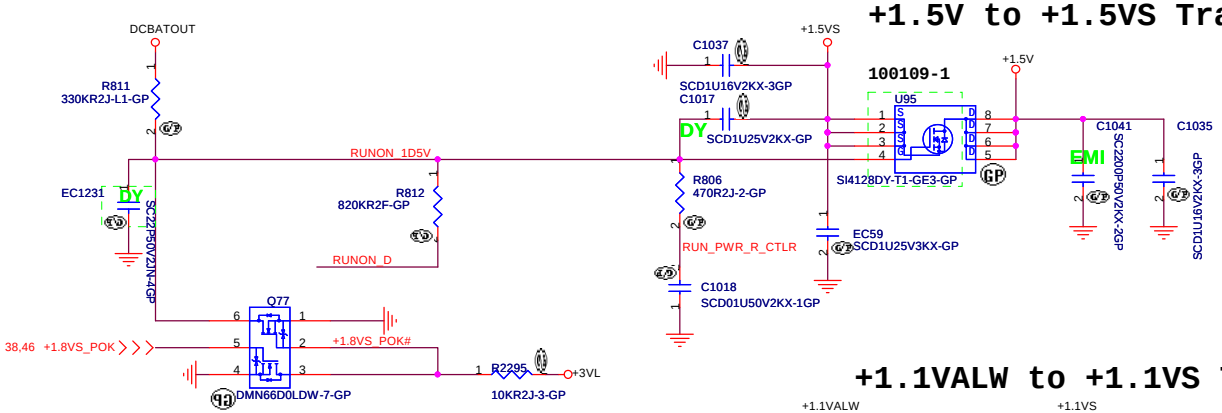
+3VALW to +3VS Transfer



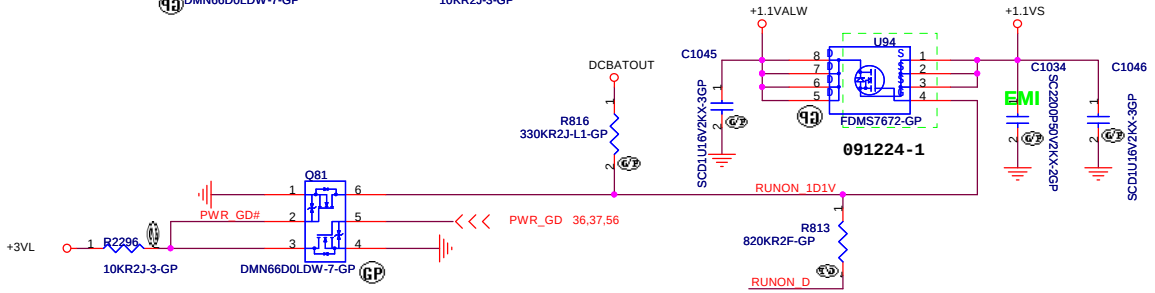
+5VALW to +5VS Transfer



+1.5V to +1.5VS Transfer



+1.1VALW to +1.1VS Transfer



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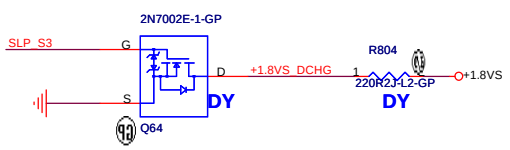
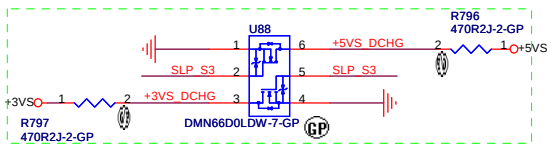
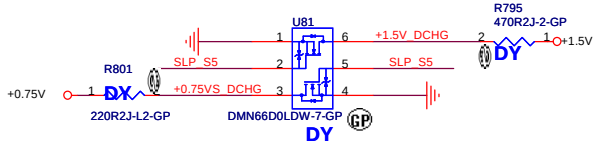


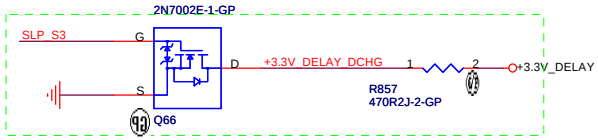
091103-1

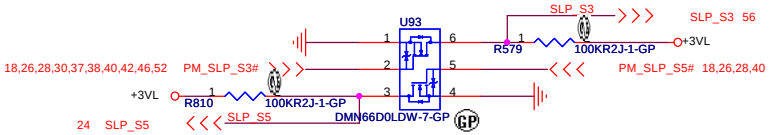


Discharge circuit-1



091215-2





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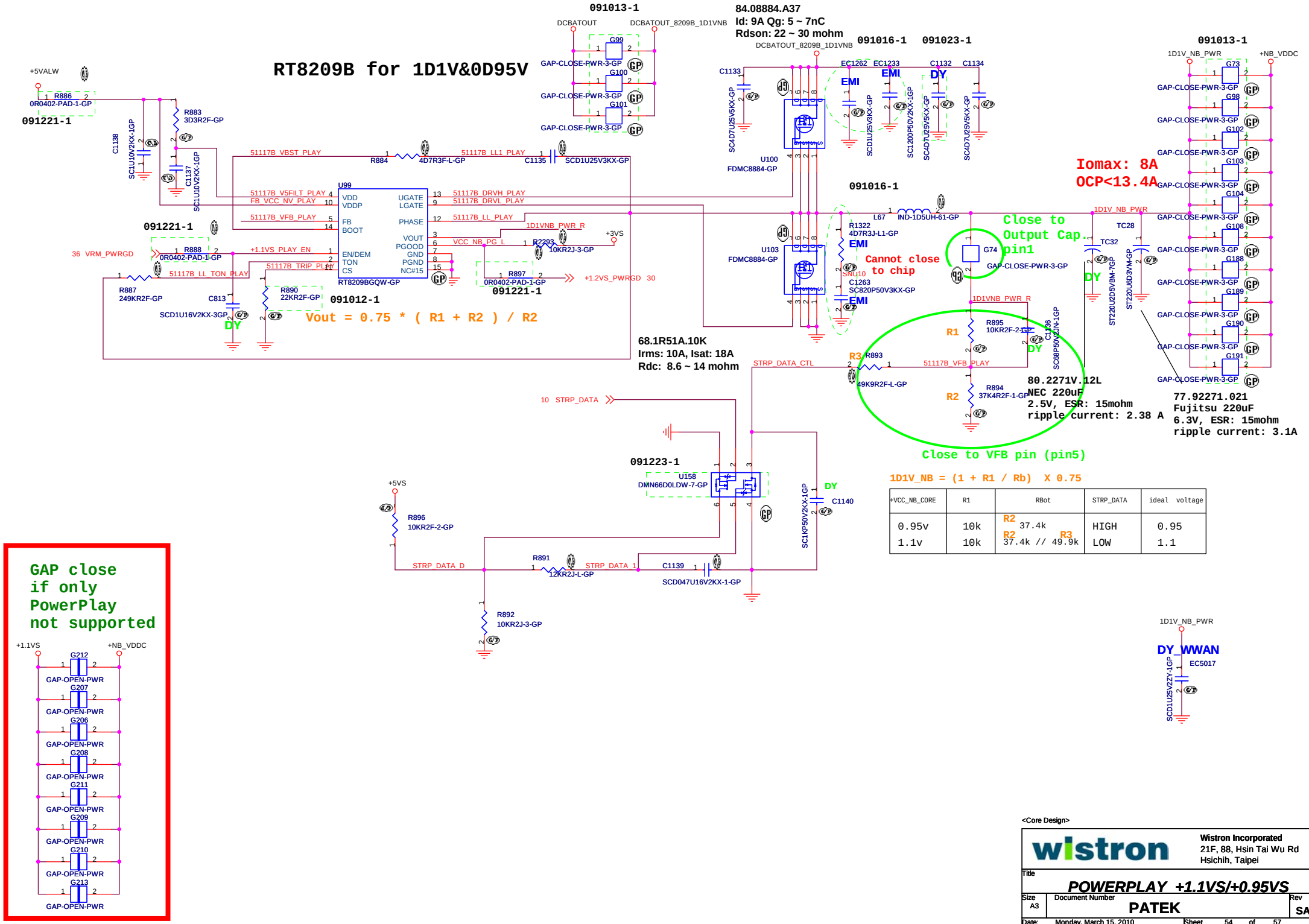
RT8209B for 1D1V&0D95V



+VCC_NB_CORE	R1	RBot	STRP_DATA	ideal voltage
0.95v	10k	R2 37.4k	HIGH	0.95
1.1v	10k	R2 37.4k // R3 49.9k	LOW	1.1

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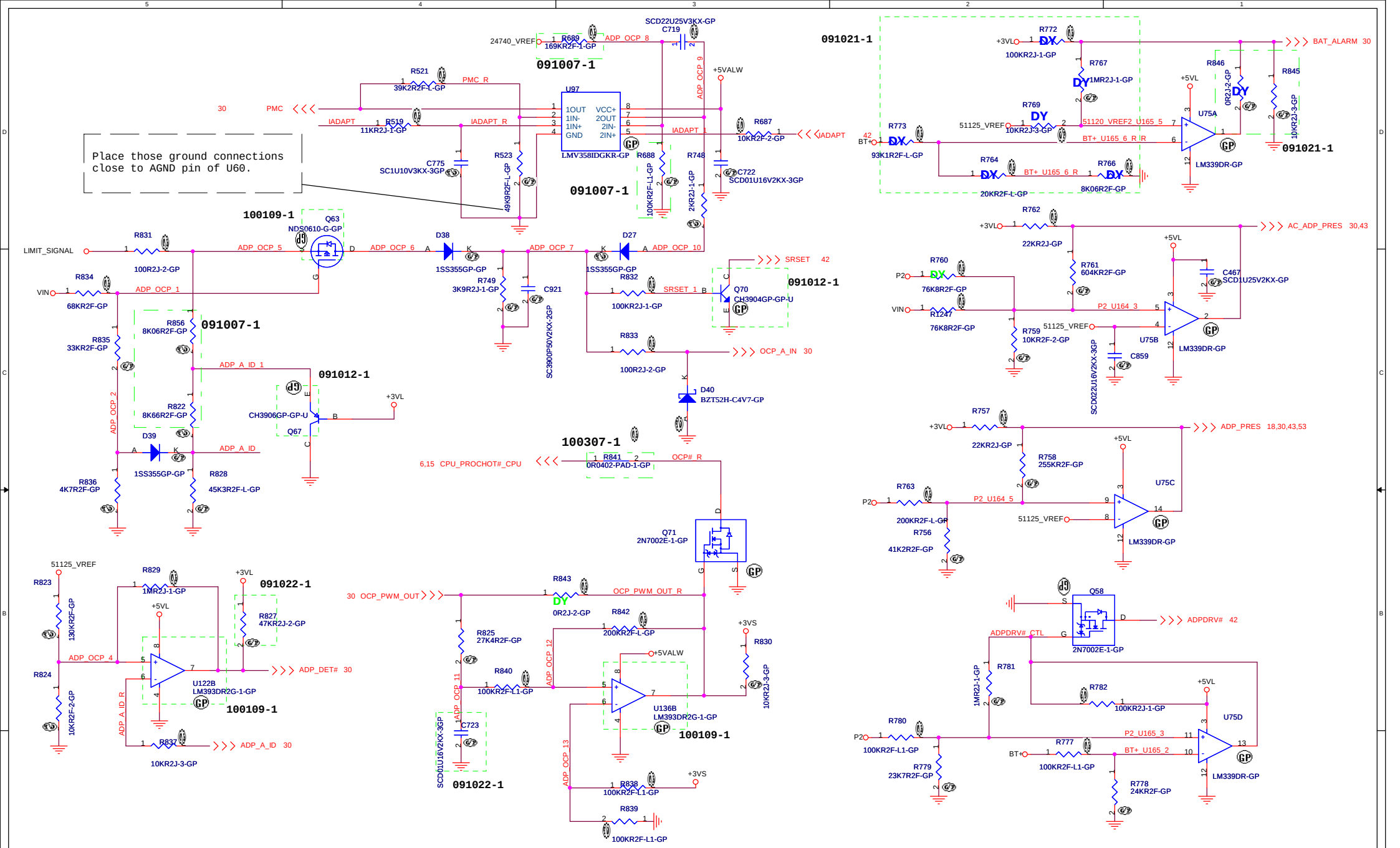

NOTE:

When AC_ADP_PRES=0 -->1
Vin*(R759//R761)/ [(R759//R761)+R1247]=51125_VREF
Vin=17.6145V

When AC_ADP_PRES=1 --> 0
[(Vin-51125_VREF)/R1247]+[(+3VL-51125_VREF)/(R761+R762)]=51125_VREF/R759
Vin=17.212554V

When ADP_PRES=0->1
P2*(R756//R758)/ [(R756//R758)+R763]=51125_VREF
P2=13.325V

When ADP_PRES=1->0
[(P2-51125_VREF)/R756]+[(+3VL-51125_VREF)/(R757+R758)]=51125_VREF/R756
P2=10.894V

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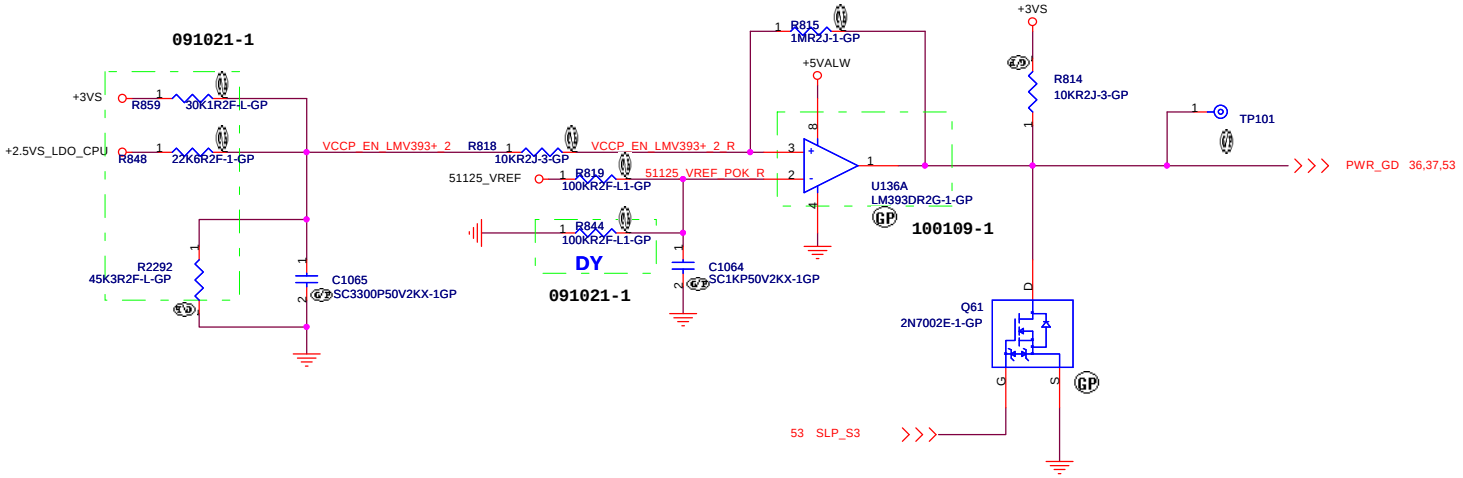

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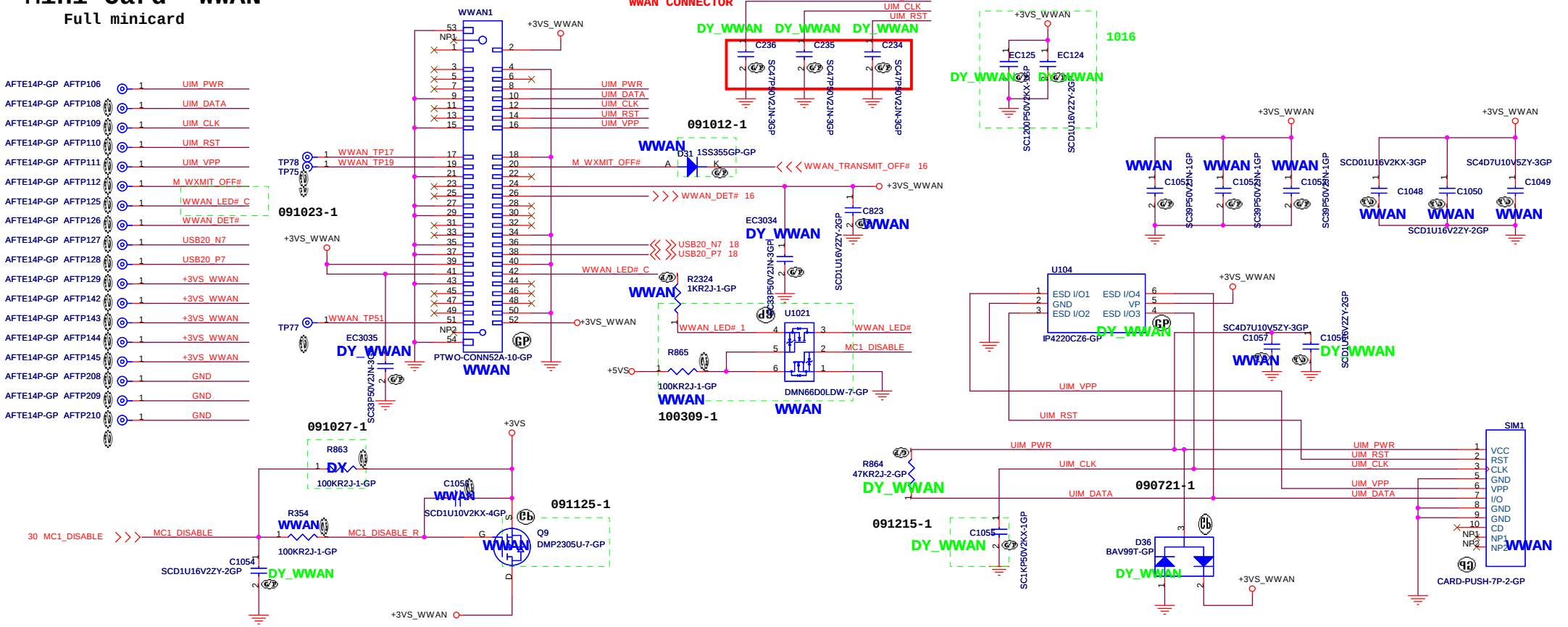
Mini-Card--WWAN

Full minicard

C234, C235 and C236 near WWAN CONNECTOR



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Rev	SA
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